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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
14/945,003	11/18/2015	Shih-Yuan WANG	309-0004US

CONFIRMATION NO. 1200

POA ACCEPTANCE LETTER

139982
Wissing Miller LLP
The Lofts at Manhattan West
434 West 33rd Street
12th Floor
New York, NY 10001

OC000000121343399

Date Mailed: 11/17/2020

NOTICE OF ACCEPTANCE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 11/10/2020.

The Power of Attorney in this application is accepted. Correspondence in this application will be mailed to the above address as provided by 37 CFR 1.33.

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at **(571) 272-4000** or **(571) 272-4200** or **1-888-786-0101**.

/afessehaye/

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Alexandria, Virginia 22313-1450
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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
14/945,003	11/18/2015	Shih-Yuan WANG	5176-88184-2

CONFIRMATION NO. 1200

POWER OF ATTORNEY NOTICE

23432
COOPER & DUNHAM LLP
845 Third Avenue, 6th Floor
NEW YORK, NY 10022

OC000000121343357

Date Mailed: 11/17/2020

NOTICE REGARDING CHANGE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 11/10/2020.

- The Power of Attorney to you in this application has been revoked by the assignee who has intervened as provided by 37 CFR 3.71. Future correspondence will be mailed to the new address of record(37 CFR 1.33).

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at **(571) 272-4000** or **(571) 272-4200** or **1-888-786-0101**.

/afessehaye/

Doc Code: PA..
Document Description: Power of Attorney

PTO/AIA/82A (07-13)
Approved for use through 03/31/2021. OMB 0651-0035
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

TRANSMITTAL FOR POWER OF ATTORNEY TO ONE OR MORE REGISTERED PRACTITIONERS

NOTE: This form is to be submitted with the Power of Attorney by Applicant form (PTO/AIA/82B) to identify the application to which the Power of Attorney is directed, in accordance with 37 CFR 1.5, unless the application number and filing date are identified in the Power of Attorney by Applicant form. If neither form PTO/AIA/82A nor form PTO/AIA82B identifies the application to which the Power of Attorney is directed, the Power of Attorney will not be recognized in the application.

Application Number	14/945,003
Filing Date	November 18, 2015
First Named Inventor	Yu Chen
Title	MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES
Art Unit	2893
Examiner Name	Eduardo A. Rodela
Attorney Docket Number	309-0004US

SIGNATURE of Applicant or Patent Practitioner

Signature	/Gerard M. Wissing/	Date (Optional)	November 10, 2020
Name	Gerard M. Wissing	Registration Number	36309
Title (if Applicant is a juristic entity)			
Applicant Name (if Applicant is a juristic entity)			

NOTE: This form must be signed in accordance with 37 CFR 1.33. See 37 CFR 1.4(d) for signature requirements and certifications. If more than one applicant, use multiple forms.

☑ *Total of 1 forms are submitted.

This collection of information is required by 37 CFR 1.131, 1.32, and 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Doc Code: PA..
Document Description: Power of Attorney

PTO/AIA/82B (07-13)
Approved for use through 03/31/2021. OMB 0651-0035
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number

POWER OF ATTORNEY BY APPLICANT

I hereby revoke all previous powers of attorney given in the application identified in either the attached transmittal letter or the boxes below.

Application Number	Filing Date

(Note: The boxes above may be left blank if information is provided on form PTO/AIA/82A.)

☑ I hereby appoint the Patent Practitioner(s) associated with the following Customer Number as my/our attorney(s) or agent(s), and to transact all business in the United States Patent and Trademark Office connected therewith for the application referenced in the attached transmittal letter (form PTO/AIA/82A) or identified above: 139982

OR

☐ I hereby appoint Practitioner(s) named in the attached list (form PTO/AIA/82C) as my/our attorney(s) or agent(s), and to transact all business in the United States Patent and Trademark Office connected therewith for the patent application referenced in the attached transmittal letter (form PTO/AIA/82A) or identified above. (Note: Complete form PTO/AIA/82C.)

Please recognize or change the correspondence address for the application identified in the attached transmittal letter or the boxes above to:

☑ The address associated with the above-mentioned Customer Number

OR

☐ The address associated with Customer Number:

OR

☐ Firm or Individual Name					
Address					
City		State		Zip	
Country					
Telephone		Email			

I am the Applicant (if the Applicant is a juristic entity, list the Applicant name in the box):

W&WSens Devices, Inc.

☐ Inventor or Joint Inventor (title not required below)

☐ Legal Representative of a Deceased or Legally Incapacitated Inventor (title not required below)

☑ Assignee or Person to Whom the Inventor is Under an Obligation to Assign (provide signer's title if applicant is a juristic entity)

☐ Person Who Otherwise Shows Sufficient Proprietary Interest (e.g., a petition under 37 CFR 1.46(b)(2) was granted in the application or is concurrently being filed with this document) (provide signer's title if applicant is a juristic entity)

SIGNATURE of Applicant for Patent

The undersigned (whose title is supplied below) is authorized to act on behalf of the applicant (e.g., where the applicant is a juristic entity).

Signature	[signature]	Date (Optional)	Oct 20, 2020
Name	Shanpu Wang		
Title	President CEO		

NOTE: Signature - This form must be signed by the applicant in accordance with 37 CFR 1.33. See 37 CFR 1.4 for signature requirements and certifications. If more than one applicant, use multiple forms.

☐ Total of forms are submitted.

This collection of information is required by 37 CFR 1.131, 1.32, and 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Electronic Acknowledgement Receipt

EFS ID:	41089561
Application Number:	14945003
International Application Number:	
Confirmation Number:	1200
Title of Invention:	MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES
First Named Inventor/Applicant Name:	Shih-Yuan WANG
Customer Number:	23432
Filer:	Gerard Michael Wissing/Mary Ellen Finnegan
Filer Authorized By:	Gerard Michael Wissing
Attorney Docket Number:	5176-88184-2
Receipt Date:	10-NOV-2020
Filing Date:	18-NOV-2015
Time Stamp:	19:28:57
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Assignee showing of ownership per 37 CFR 3.73	309-0004US_StatementUnder37CFR373.pdf	121334 c09a6caa37cd43429f5e31d42670fd73dfb9b9b7	no	3

Warnings:

Information:					
2	Power of Attorney	309-0004US_POA.pdf	643066 3ef96d23916db22650b080125815f668ccf96831	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	764400		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PTO/AIA/96 (08-12)
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STATEMENT UNDER 37 CFR 3.73(c)

Applicant/Patent Owner: W&WSens Devices, Inc.

Application No./Patent No.: 14/945,003 Filed/Issue Date: November 18, 2015

Titled: MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES

W&WSens Devices, Inc., a corporation

(Name of Assignee) (Type of Assignee, e.g., corporation, partnership, university, government agency, etc.)

states that, for the patent application/patent identified above, it is (choose **one** of options 1, 2, 3 or 4 below):

1. ☑ The assignee of the entire right, title, and interest.

2. ☐ An assignee of less than the entire right, title, and interest (check applicable box):

   ☐ The extent (by percentage) of its ownership interest is _____%. Additional Statement(s) by the owners holding the balance of the interest must be submitted to account for 100% of the ownership interest.

   ☐ There are unspecified percentages of ownership. The other parties, including inventors, who together own the entire right, title and interest are:

   Additional Statement(s) by the owner(s) holding the balance of the interest must be submitted to account for the entire right, title, and interest.

3. ☐ The assignee of an undivided interest in the entirety (a complete assignment from one of the joint inventors was made). The other parties, including inventors, who together own the entire right, title, and interest are:

   Additional Statement(s) by the owner(s) holding the balance of the interest must be submitted to account for the entire right, title, and interest.

4. ☐ The recipient, via a court proceeding or the like (*e.g.*, bankruptcy, probate), of an undivided interest in the entirety (a complete transfer of ownership interest was made). The certified document(s) showing the transfer is attached.

The interest identified in option 1, 2 or 3 above (not option 4) is evidenced by either (choose **one** of options A or B below):

A. ☑ An assignment from the inventor(s) of the patent application/patent identified above. The assignment was recorded in the United States Patent and Trademark Office at Reel 040072, Frame 0570, or for which a copy thereof is attached.

B. ☐ A chain of title from the inventor(s), of the patent application/patent identified above, to the current assignee as follows:

   1. From: _____ To: _____

      The document was recorded in the United States Patent and Trademark Office at

      Reel _____, Frame _____, or for which a copy thereof is attached.

   2. From: _____ To: _____

      The document was recorded in the United States Patent and Trademark Office at

      Reel _____, Frame _____, or for which a copy thereof is attached.

This collection of information is required by 37 CFR 3.73(b). The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

PTO/AIA/96 (08-12)
Approved for use through 01/31/2013. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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STATEMENT UNDER 37 CFR 3.73(c)

3. From: _____ To: _____

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Reel _____, Frame _____, or for which a copy thereof is attached.

4. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at

Reel _____, Frame _____, or for which a copy thereof is attached.

5. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at

Reel _____, Frame _____, or for which a copy thereof is attached.

6. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at

Reel _____, Frame _____, or for which a copy thereof is attached.

☐ Additional documents in the chain of title are listed on a supplemental sheet(s).

☑ As required by 37 CFR 3.73(c)(1)(i), the documentary evidence of the chain of title from the original owner to the assignee was, or concurrently is being, submitted for recordation pursuant to 37 CFR 3.11.

[NOTE: A separate copy (i.e., a true copy of the original assignment document(s)) must be submitted to Assignment Division in accordance with 37 CFR Part 3, to record the assignment in the records of the USPTO. See MPEP 302.08]

The undersigned (whose title is supplied below) is authorized to act on behalf of the assignee.

/Gerard M. Wissing/	November 10, 2020
Signature	Date
Gerard M. Wissing	36309
Printed or Typed Name	Title or Registration Number

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

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United States Patent and Trademark Office
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APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/945,003	12/20/2016	9525084	5176-88184-2	1200

23432 7590 11/30/2016

COOPER & DUNHAM, LLP
30 Rockefeller Plaza
20th Floor
NEW YORK, NY 10112

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment is 0 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Data Management (ODM) at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site http://pair.uspto.gov for additional applicants):

Shih-Yuan WANG, Palo Alto, CA;
W&Wsens, Devices Inc., Los Altos, CA;
Shih-Ping Wang, Los Altos, CA;

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	14945003
Filing Date	2015-11-18
First Named Inventor	Shih-Yuan WANG et al.
Art Unit	
Examiner Name	RODELA, EDUARDO A
Attorney Docket Number	5176/88184-2

	1	WO2012149441A2	wo		2012-11-01	CHANG-HASNAIN, Connie et al.		
	2	PCT/JP2014/39208	~~JP~~ WO		2014-11-28	International Search Report		
Change(s) applied to document, /P.H./ 11/17/2016	3	PCT/US1561120	~~US~~ WO		2015-11-17	WANG, S		
	4	PCT/US1439208	~~US~~ WO		2014-05-22	WANG, S		
	5	PCT/US15/61120	~~US~~ WO		2015-11-17	WANG, S		
	6	PCT/US11/51091	~~US~~ WO		2011-09-09	WANG, S		
	7	WO2012034078	WO		03/2012 ~~2015-03-05~~	Wang, S		
	8	WO2014190189	WO		2014-11-27	Wang, S		

If you wish to add additional Foreign Patent Document citation information please click the Add button Add

NON-PATENT LITERATURE DOCUMENTS Remove

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T5
	1	M. K. Emsley, O. Dosunmu, and M. S. Unlu, "High-speed resonant-cavity-enhanced silicon photodetectors on reflecting silicon-on-insulator substrates," Ieee Photonics Technology Letters, vol. 14, pp. 519-521, Apr 2002.	

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /E.A.R/

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	14945003
	Filing Date	2015-11-18
	First Named Inventor	Shih-Yuan WANG et al.
	Art Unit	
	Examiner Name	not yet assigned
	Attorney Docket Number	5176/88184-2

	9	20090188557		2009-07-30	Wang, et al.		
Change(s) applied to document, /P.H./ 11/18/2016	10	20080265449		10/2008 ~~2008-09-05~~	Meinders et al. ~~Meinders~~		

If you wish to add additional U.S. Published Application citation information please click the Add button.

FOREIGN PATENT DOCUMENTS

Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2]	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]
	1	WO2012149441A2	wo		2012-11-01	CHANG-HASNAIN, Connie et al.		☐
Change(s) applied to document, /P.H./ 11/17/2016	2	PCT/JP2014/39208	~~JP~~ WO		2014-11-28	International Search Report		☐
	3	PCT/US1561120	~~US~~ WO		2015-11-17	WANG, S		☐
	4	PCT/US1439208	~~US~~ WO		2014-05-22	WANG, S		☐
	5	PCT/US15/61120	~~US~~ WO		2015-11-17	WANG, S		☐
	6	PCT/US11/51091	~~US~~ WO		2011-09-09	WANG, S		☐
	7	WO2012034078	WO		03/2012 ~~2012-03-08~~	Wang, S		☐

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /E.A.R/

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	14945003
	Filing Date	2015-11-18
	First Named Inventor	Shih-Yuan WANG et al.
	Art Unit	
	Examiner Name	RODELA, EDUARDO A
	Attorney Docket Number	5176/88184-2

	5	20100193768		2010-08-05	Habib	
	6	20100197068		2010-08-05	Poon	
	7	20100126548		2010-05-27	JANG, ET AL.	
	8	20080265449		2008-10-30	Meinders et al.	
	9	20090188557		2009-07-30	Wang, et al.	
	10	20080265449		10/2008 ~~2008-08-25~~	Meinders et al. ~~Heidari~~	
Change(s) applied to document, /P.H./ 11/17/2016	11	20080047604		2008-02-28	Korevaar et al.	
	12	20090267049		2009-10-29	Cho et al.	
Change(s) applied to document, /P.H./ 11/21/2016	13	20080102582 ~~20081012582~~		05/2008 ~~2008-01-05~~	Takei	
	14	20070190434		2007-08-16	Suda	
	15	20100313941		2010-12-01	Huang	

EFS Web 2.1.17

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /E.A.R/

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	14945003	WANG ET AL.
	Examiner	**Art Unit**
	EDUARDO A RODELA	2893

CPC							
Symbol						**Type**	**Version**
H01L		31	/	02363		F	2013-01-01
H01L		27	/	1443		I	2013-01-01
H01L		27	/	14625		I	2013-01-01
H04B		10	/	6971		I	2013-01-01
H01L		27	/	1446		I	2013-01-01
H01L		31	/	02		I	2013-01-01
H01L		31	/	0232		I	2013-01-01
H01L		31	/	02327		I	2013-01-01
H01L		31	/	0236		I	2013-01-01
H01L		31	/	09		I	2013-01-01
H01L		31	/	103		I	2013-01-01
H04B		10	/	691		I	2013-01-01
H01L		31	/	02325		I	2013-01-01
H01L		31	/	028		I	2013-01-01
H01L		31	/	107		I	2013-01-01
H04B		10	/	25		I	2013-01-01
H04B		10	/	40		I	2013-01-01
H04B		10	/	801		I	2013-01-01

CPC Combination Sets							
Symbol					**Type**	**Set**	**Ranking**	**Version**
			/					
			/					

NONE		**Total Claims Allowed:**	
(Assistant Examiner)	(Date)	28	
/EDUARDO A RODELA/ Primary Examiner.Art Unit 2893	10/13/2016	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	6B

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	14945003	WANG ET AL.
	Examiner	**Art Unit**
	EDUARDO A RODELA	2893

US ORIGINAL CLASSIFICATION		INTERNATIONAL CLASSIFICATION										
CLASS	SUBCLASS	CLAIMED					NON-CLAIMED					
		H	0	1	L	31 / 0236 (2006.01.01)						
CROSS REFERENCE(S)												
CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)											

NONE		Total Claims Allowed:	
(Assistant Examiner)	(Date)	28	
/EDUARDO A RODELA/ Primary Examiner.Art Unit 2893	10/13/2016	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	6B

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	14945003	WANG ET AL.
	Examiner	**Art Unit**
	EDUARDO A RODELA	2893

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☒ T.D. ☐ R.1.47

Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
1	1	16	17	27	33										
2	2	17	18		34										
3	3	18	19		35										
4	4		20	28	36										
5	5		21												
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10	11		27												
11	12	22	28												
12	13	23	29												
13	14	24	30												
14	15	25	31												
15	16	26	32												

NONE		**Total Claims Allowed:**	
(Assistant Examiner)	(Date)	28	
/EDUARDO A RODELA/ Primary Examiner.Art Unit 2893	10/13/2016	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	6B

UNITED STATES PATENT AND TRADEMARK OFFICE

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/945,003	11/18/2015	Shih-Yuan WANG	5176-88184-2	1200

23432 7590 10/25/2016

COOPER & DUNHAM, LLP
30 Rockefeller Plaza
20th Floor
NEW YORK, NY 10112

EXAMINER	
RODELA, EDUARDO A	

ART UNIT	PAPER NUMBER
2893	

MAIL DATE	DELIVERY MODE
10/25/2016	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Response to Rule 312 Communication	Application No.	Applicant(s)
	14/945,003	WANG ET AL.
	Examiner	Art Unit
	Eduardo A. Rodela	2893

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address –

1. ☒ The amendment filed on *19 October 2016* under 37 CFR 1.312 has been considered, and has been:

a) ☒ entered.

b) ☐ entered as directed to matters of form not affecting the scope of the invention.

c) ☐ disapproved because the amendment was filed after the payment of the issue fee.
Any amendment filed after the date the issue fee is paid must be accompanied by a petition under 37 CFR 1.313(c)(1) and the required fee to withdraw the application from issue.

d) ☐ disapproved. See explanation below.

e) ☐ entered in part. See explanation below.

/Eduardo A. Rodela/
Primary Examiner, Art Unit 2893

OK To Enter - /EAR/ - 10/21/2016

Dkt. 5176/88184-2

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application of: Shih-Yuan WANG

Group Art Unit: 2893

Application No.: 14/945,003

Examiner: Eduardo A. Rodela

Date Filed: November 18, 2015

For: MICROSTRUCTURE ENHANCED ABSORPTIO00N PHOTOSENSITIVE DEVICES

Conf. No.: 1200

Class-Subclass: 257-432000

Issue Fee Due Date: January 17, 2017

This correspondence is being filed electronically with the U.S. Patent and Trademark Office via EFS-Web.

/maria arap/ October 19, 2016
Maria Arap

30 Rockefeller Plaza, 20th Floor
New York, New York 10112
Tel.: (212) 278-0400

Mail Stop Issue Fee
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

AMENDMENT AFTER NOTICE OF ALLOWANCE
PURSUANT TO 37 C.F.R. §1.312(a)

Sir:

Amendments to the claims are reflected in the **Listing of Claims** section which begins on page 2. (Only claim 12 is amended.)

Remarks begin on page 11 of this paper.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
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Alexandria, Virginia 22313-1450
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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
14/945,003	11/18/2015	Shih-Yuan WANG	5176-88184-2

CONFIRMATION NO. 1200

23432
COOPER & DUNHAM, LLP
30 Rockefeller Plaza
20th Floor
NEW YORK, NY 10112

PUBLICATION NOTICE

OC000000086626687

Title:MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES

Publication No.US-2016-0308075-A1
Publication Date:10/20/2016

NOTICE OF PUBLICATION OF APPLICATION

The above-identified application will be electronically published as a patent application publication pursuant to 37 CFR 1.211, et seq. The patent application publication number and publication date are set forth above.

The publication may be accessed through the USPTO's publically available Searchable Databases via the Internet at www.uspto.gov. The direct link to access the publication is currently http://www.uspto.gov/patft/.

The publication process established by the Office does not provide for mailing a copy of the publication to applicant. A copy of the publication may be obtained from the Office upon payment of the appropriate fee set forth in 37 CFR 1.19(a)(1). Orders for copies of patent application publications are handled by the USPTO's Office of Public Records. The Office of Public Records can be reached by telephone at (703) 308-9726 or (800) 972-6382, by facsimile at (703) 305-8759, by mail addressed to the United States Patent and Trademark Office, Office of Public Records, Alexandria, VA 22313-1450 or via the Internet.

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Further assistance in electronically accessing the publication, or about PAIR, is available by calling the Patent Electronic Business Center at 1-866-217-9197.

Office of Data Managment, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101

PART B - FEE(S) TRANSMITTAL

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P.O. Box 1450
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23432 7590 10/17/2016
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30 Rockefeller Plaza
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Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

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I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

Ivan S. Kavrukov	(Depositor's name)
/ivan s. kavrukov/	(Signature)
October 20, 2016	(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/945,003	11/18/2015	Shih-Yuan WANG	5176-88184-2	1200

TITLE OF INVENTION: MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	SMALL	$480	$0	$0	$480	01/17/2017

EXAMINER	ART UNIT	CLASS-SUBCLASS
RODELA, EDUARDO A	2893	257-432000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.
1 Cooper & Dunham LLP
2
3

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE: W&Wsens Devices, Inc.

(B) RESIDENCE: (CITY and STATE OR COUNTRY): Los Altos, CA

Please check the appropriate assignee category or categories (will not be printed on the patent) : ☐ Individual ☒ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:
☒ Issue Fee
☐ Publication Fee (No small entity discount permitted)
☐ Advance Order - # of Copies _____

4b. Payment of Fee(s): **(Please first reapply any previously paid issue fee shown above)**
☐ A check is enclosed.
☐ Payment by credit card. Form PTO-2038 is attached.
☒ The director is hereby authorized to charge the required fee(s), any deficiency, or credits any overpayment, to Deposit Account Number 033125 (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)
☐ Applicant certifying micro entity status. See 37 CFR 1.29
NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.
☐ Applicant asserting small entity status. See 37 CFR 1.27
NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.
☐ Applicant changing to regular undiscounted fee status.
NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature Ivan S. Kavrukov Date October 20, 2016
Typed or printed name /ivan s. kavrukov/ Registration No. 25,161

PTOL-85 Part B (10-13) Approved for use through 10/31/2013. OMB 0651-0033 U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Electronic Acknowledgement Receipt

EFS ID:	27269300
Application Number:	14945003
International Application Number:	
Confirmation Number:	1200
Title of Invention:	MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES
First Named Inventor/Applicant Name:	Shih-Yuan WANG
Customer Number:	23432
Filer:	Ivan Kavrukov/Erin Finnegan
Filer Authorized By:	Ivan Kavrukov
Attorney Docket Number:	5176-88184-2
Receipt Date:	20-OCT-2016
Filing Date:	18-NOV-2015
Time Stamp:	10:21:15
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	DA
Payment was successfully received in RAM	$480
RAM confirmation Number	102016INTEFSW00009466033125
Deposit Account	033125
Authorized User	Erin Finnegan

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

37 CFR 1.21 (Miscellaneous fees and charges)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Issue Fee Payment (PTO-85B)	IssueFeeTransmittal_14945003.pdf	1627687 51515d185343f40c68182a063559bba3dc948eea	no	1
Warnings:					
Information:					
2	Fee Worksheet (SB06)	fee-info.pdf	30824 a4cbdc1d6e3731d7fcb79071902b45942cd6caa5	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	1658511		

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New International Application Filed with the USPTO as a Receiving Office
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Electronic Patent Application Fee Transmittal

Application Number:	14945003
Filing Date:	18-Nov-2015
Title of Invention:	MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES
First Named Inventor/Applicant Name:	Shih-Yuan WANG
Filer:	Ivan Kavrukov/Erin Finnegan
Attorney Docket Number:	5176-88184-2

Filed as Small Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
UTILITY APPL ISSUE FEE	2501	1	480	480

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Extension-of-Time:				
Miscellaneous:				
			Total in USD ($)	**480**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application of: Shih-Yuan WANG

Group Art Unit: 2893

Application No.: 14/945,003

Examiner: Eduardo A. Rodela

Date Filed: November 18, 2015

For: MICROSTRUCTURE ENHANCED ABSORPTIO00N PHOTOSENSITIVE DEVICES

Conf. No.: 1200

Class-Subclass: 257-432000

Issue Fee Due Date: January 17, 2017

This correspondence is being filed electronically with the U.S. Patent and Trademark Office via EFS-Web.

/maria arap/ October 19, 2016
Maria Arap

30 Rockefeller Plaza, 20th Floor
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AMENDMENT AFTER NOTICE OF ALLOWANCE
PURSUANT TO 37 C.F.R. §1.312(a)

Sir:

Amendments to the claims are reflected in the **Listing of Claims** section which begins on page 2. (Only claim 12 is amended.)

Remarks begin on page 11 of this paper.

Electronic Acknowledgement Receipt

EFS ID:	27260465
Application Number:	14945003
International Application Number:	
Confirmation Number:	1200
Title of Invention:	MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES
First Named Inventor/Applicant Name:	Shih-Yuan WANG
Customer Number:	23432
Filer:	Ivan Kavrukov/Maria arap
Filer Authorized By:	Ivan Kavrukov
Attorney Docket Number:	5176-88184-2
Receipt Date:	19-OCT-2016
Filing Date:	18-NOV-2015
Time Stamp:	14:07:43
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Amendment after Notice of Allowance (Rule 312)	Rule_312_Amend_14945003--.pdf	99758 9bed08309d5c5051a1f76378afce7d1518521fdc	no	11

Warnings:

Information:	
Total Files Size (in bytes):	99758

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New Applications Under 35 U.S.C. 111
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National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Listing of Claims

The following listing of claims will replace all prior versions, and listings, of claims in the subject application:

1. (Previously Submitted) An integrated detector/processor circuit for data communication comprising both a photodetector with microstructure-enhanced photoabsorption and an electronic processor formed into a single semiconductor chip, comprising:

a photodetector formed on a semiconductor substrate and comprising a photon absorbing region configured to absorb photons from an optical source signal modulated for data communication and provide an output electrical signal corresponding thereto;

said photon absorbing region comprising an I-region that is between an N-region and a P-region and comprises a substantially continuous layer interrupted by a plurality of holes extending in said I-region toward said substrate and configured to concurrently receive the same source signal at a plural number of the holes;

an electronic processor also formed on said semiconductor substrate and operatively associated with said photon absorbing region to receive therefrom and process said output electrical signal into a processed output, thereby forming a single semiconductor chip that receives the optical source signal and outputs the processed output;

wherein said photon absorbing region and said electronic processor have respective thicknesses that are of the same order of magnitude; and

a cathode region and an anode region operatively associated with said photon absorbing region and reverse biasing circuitry configured to apply a voltage between said cathode and anode regions such that said cathode region is driven to a more positive voltage than said anode region.

2. (Original) The integrated detector/processing circuit of claim 1, wherein the thickness of the photon absorbing region is in the range of 0.5 to 5 micrometers.

3. (Original) The integrated detector/processing circuit of claim 1, wherein the electronic

processor comprises an application specific integrated circuit (ASIC) comprising at least one of complementary metal oxide semiconductor (CMOS) devices, bipolar (Bi) devices, and BiCMOS devices.

4.(Original) The integrated detector/processing circuit of claim 1, wherein the photon absorbing region is configured to absorb in excess of 60% of the incident source signal at wavelengths from 800 nm to 900 nm and provide an output electrical signal corresponding thereto.

5. (Original) The integrated detector/processing circuit of claim 1, wherein the photon absorbing region is configured to absorb the incident source signal at an absorption percentage that varies by less than 20% over selected wavelength spans of at least 20 nm of source signal wavelengths from 800 nm to 900 nm.

6. (Canceled) The integrated detector/processing circuit of claim 1, wherein the photon absorbing region is configured to absorb the incident source signal at an absorption percentage that varies by less than 20% over selected wavelength spans of at least 20 nm of source signal wavelengths from 800 nm to 900 nm.

7. (Original) The integrated detector/processing circuit of claim 1, wherein the photon absorbing region is configured to absorb in excess of 60% of the incident source signal at wavelengths from 800 nm to 900 nm and provide an output electrical signal corresponding thereto

8. (Previously Submitted) The integrated detector/processing circuit of claim 1, further including one or more additional photodetectors formed on said semiconductor substrate and having respective photon absorbing regions receiving respective additional source signals and providing respective output electrical signals corresponding thereto, and one or more additional electronic processors also formed on said semiconductor substrate and operatively associated with the respective photon absorbing regions of said additional

photodetectors to receive therefrom and [procces] process said respective output electrical signals therefrom.

9. (Previously Submitted) The integrated detector/processing circuit of claim 1, wherein the plurality of holes enhances absorption of photons compared to a hole-free but otherwise same photodetector at a range of wavelengths that includes a wavelength of said source signal.

10. (Original) The integrated detector/processing circuit of claim 1, wherein the electronic processor includes one or more types selected from a group consisting of: transimpedance amplifier, signal processing electronics, and routing electronics.

11. (Original) The integrated detector/processing circuit of claim 1, wherein a capacitance associated with the photodetector is decreased compared to an otherwise same photodetector having its anode and cathode regions operatively connected to a conventional bond pad.

12. (Currently Amended) A photodetector with microstructure-enhanced photoabsorption comprising:

a photon absorbing region that comprises an I-region between an N-region and a P-region, said I-region having a thickness between 0.5 and 5 micrometers and configured to absorb photons from a source signal modulated for data communication and provide an output electrical signal corresponding thereto;

said photon absorbing region comprising silicon in a substantially continuous layer interrupted by a plurality of holes extending through at least a portion of the thickness of the I-region and configured to concurrently receive the same source signal at a plural number of the holes; and

said photon absorbing region being configured to absorb in excess of 40% of the incident source signal at wavelengths in at least one of the ranges from 800 nm to 900 nm and from 1400 nm to 1700 nm and provide an output electrical signal

corresponding thereto.

13. (Original) The photodetector of claim 12, wherein the photon absorbing region is configured to absorb in excess of 40% of the incident source signal at wavelengths from 800 nm to 900 nm and provide an output electrical signal corresponding thereto.

14. (Original) The photodetector of claim 12, wherein the photon absorbing region is configured to absorb in excess of 50% of the incident source signal at wavelengths from 800 nm to 900 nm and provide an output electrical signal corresponding thereto.

15. (Original) The photodetector of claim 12, wherein the photon absorbing region is configured to absorb the incident source signal at an absorption percentage that varies by less than 20% over wavelength spans of at least 20 nm of source signal wavelengths from 800 nm to 900 nm.

16. (Original) The photodetector of claim 12, wherein each hole has a cross-section parallel to the upper surface of the substrate and has a maximum dimension of between 400 nm and 2500 nm, and each hole has a center that is spaced apart by less than 3500 nm from a center of a nearest adjacent hole of the plurality of holes.

17. (Previously Submitted) The photodetector of claim 12, wherein the photodetector comprises a reflecting structure configured to cause multiple reflections of the source signal thereby traversing the photon absorbing region with said source signal multiple times.

18. (Previously Submitted) A photodetector with microstructure-enhanced photoabsorption comprising:

a cathode region;

an anode region;

reverse biasing circuitry configured to apply a voltage between said cathode and anode regions such that said cathode region is driven to a more positive voltage than said

anode region;

a substrate material having an upper surface; and

a photon absorbing I-region comprising silicon, operatively associated with the cathode and anode regions, and configured to absorb photons from a source signal, said photon absorbing I-region including a substantially continuous layer interrupted by a plurality of holes each having a cross section parallel to the upper substrate surface having a maximum dimension of between 400 nm and 2500 nm, and each hole having a center that is spaced apart by less than 3500 nm from a center of a nearest adjacent hole of the plurality of holes, said I-region being configured to absorb photons from a source signal that has a substantially continuous profile illuminating an area that includes plural holes in the I-region.

19. (Original) The photodetector of claim 18 wherein the source signal has a wavelength that is greater than 800 nm and less than 1000 nm.

20. (Canceled) The photodetector according to claim 18 wherein the plurality of holes are arranged into a periodically-spaced array.

21. (Canceled) The photodetector according to claim 20 wherein the periodically-spaced array has a hexagonal or square lattice pattern.

22. (Previously Submitted) The photodetector according to claim 18 wherein the plurality of holes enhances absorption of photons compared to a hole-free but otherwise same photodetector at a range of wavelengths that includes a wavelength of said source signal.

23. (Previously Submitted) The photodetector according to claim 18 wherein each of the holes has a predominately circular cross-section parallel to the upper substrate surface.

24. (Original) The photodetector according to claim 18 wherein the cathode and anode regions

are operatively connected to integrated circuit electronics and the photodetector and integrated circuit electronics are integrated into a single silicon chip.

25. (Canceled) The photodetector according to claim 24 wherein the integrated circuit electronics includes one or more types selected from a group consisting of: transimpedance amplifier, signal processing electronics and routing electronics.

26. (Canceled) The photodetector according to claim 18 wherein said photodetector is configured to detect said source signal at a data bandwidth of greater than 2.5 gigabits per second at source signal wavelengths of 850 nanometers with a quantum efficiency of at least 30%.

27. (Canceled) The photodetector according to claim 18 wherein said photodetector is configured to detect said source signal at a data bandwidth of greater than 2.5 gigabits per second at source signal wavelengths of 850 nanometers with a quantum efficiency of at least 50%.

28. (Original) The photodetector according to claim 18 wherein said photodetector is configured to detect said source signal at a data bandwidth of greater than or equal to 5 gigabits per second, at source signal wavelengths of 850 nanometers with a quantum efficiency of at least 30%.

29. (Original) The photodetector according to claim 18 wherein said photodetector is configured to detect said source signal at a data bandwidth of greater than or equal to 5 Gb/s, at source signal wavelengths of 850 nanometers with a quantum efficiency of at least 50%.

30. (Original) The photodetector according to claim 18 further including a substrate and wherein the cathode, absorbing and anode regions are formed above the substrate and the photodetector is configured to receive the source signal from directions facing a side of the photodetector opposite of the substrate.

31. (Previously Submitted) A single silicon substrate on which are fabricated and integrated a photodetector, an active electronic circuit, and electrical interconnects that operatively couple the photodetector and the active electronic circuit to each other and provide an output for use by other circuits, comprising:

a photodetector fabricated on the single silicon substrate and comprising a P-doped region, an N-doped region, and an I-region that is between the P-doped region and the N-doped region and is not intentionally doped or is doped to a lower dopant concentration than the P-doped region and the N-doped region, wherein:

said I-region:

comprises at least one of silicon and germanium;

is no more than 5000 nanometers thick in a direction from one toward the other of said P-doped region and said N-doped region;

comprises a substantially continuous layer interrupted by intentionally formed holes, said holes being spaced from each other and extending in said direction from one toward the other of said P-doped region and N-doped region;

said photodetector is configured to receive an optical beam that:

is modulated at 10 Gigabits per second or more;

is substantially continuous in cross-section; and

impinges on plural ones of said holes at the same time;

said photodetector is further configured to provide, in response to impingement thereon of said optical beam, a photodetector electrical output that:

represents the modulation of said optical beam; and

has a bandwidth of 10 Gigabits per second or more;

said photodetector has quantum efficiency of at least 30% (i) when the optical beam wavelength in 850-1000 nm and the I-region comprises silicon, and (ii) when the optical beam wavelength is 1550-1600 nm and the I-region comprises germanium; and

an active electronic circuit that:

is fabricated on the substrate on which the photodetector is fabricated;

comprises at least one of CMOS and BiCMOS integrated circuit fabricated with at least one of silicon and germanium; and

is configured to:

receive the photodetector electrical output from the photodetector; and

process the received photodetector electrical output to thereby produce a processed electrical output that has at least some different characteristics compared with the photodetector electrical output; and

electrical interconnects that:

also are fabricated on the same silicon substrate;

are configured to operatively couple said photodetector and said active electronic circuit to each other, including by transferring said photodetector electrical output from said photodetector to said active electronic circuit; and

are further configured to output the processed electrical output from the active electronic circuit for use by other circuits.

32. (Previously Submitted) The single silicon substrate of claim 31 in which the I-region comprises said holes.

33. (Previously Submitted) The single substrate of claim 32 in which the holes are arranged in an aperiodic array.

34. (Canceled) The single silicon substrate of claim 31 in which the I-region comprises said pillars.

35. (Canceled) The single silicon substrate of claim 31 in which said pillars are arranged in an aperiodic array.

36. (Previously Submitted) The single silicon substrate of claim 31 in which said pillars or holes are tapered.

REMARKS

This Rule 312 Amendment corrects a minor error in the text added to claim 12 by the Examiner's Amendment included in the Notice of Allowability mailed 10/17/2016.

The claims in this paper include the text added by said Examiner's Amendment and the cancelation of claims 34 and 35.

Respectfully submitted,

/Ivan S. Kavrukov/

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application of: Shih-Yuan WANG

Group Art Unit: 2893

Application No.: 14/945,003

Examiner: Eduardo A. Rodela

Date Filed: November 18, 2015

For: MICROSTRUCTURE ENHANCED ABSORPTIO00N PHOTOSENSITIVE DEVICES

Conf. No.: 1200

Class-Subclass: 257-432000

Issue Fee Due Date: January 17, 2017

This correspondence is being filed electronically with the U.S. Patent and Trademark Office via EFS-Web.

/maria arap/ October 19, 2016
Maria Arap

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Mail Stop Issue Fee
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

AMENDMENT AFTER NOTICE OF ALLOWANCE
PURSUANT TO 37 C.F.R. §1.312(a)

Sir:

Amendments to the claims are reflected in the **Listing of Claims** section which begins on page 2. (Only claim 12 is amended.)

Remarks begin on page 11 of this paper.

Electronic Acknowledgement Receipt

EFS ID:	27259968
Application Number:	14945003
International Application Number:	
Confirmation Number:	1200
Title of Invention:	MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES
First Named Inventor/Applicant Name:	Shih-Yuan WANG
Customer Number:	23432
Filer:	Ivan Kavrukov/Maria ARAP
Filer Authorized By:	Ivan Kavrukov
Attorney Docket Number:	5176-88184-2
Receipt Date:	19-OCT-2016
Filing Date:	18-NOV-2015
Time Stamp:	13:46:21
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Amendment after Notice of Allowance (Rule 312)	Rule_312_Amend_14945003.pdf	75185 cd229051fcde73c1adf8c116be81f70f135c69ee	no	1

Warnings:

Information:	
Total Files Size (in bytes):	75185

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Dkt. 5176/88184-2

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application of: Shin-Yann WANG et al.

Application No.: 14/945,003 Date Filed: November 18, 2015

For: MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES

This correspondence is being filed electronically with the U.S. Patent and Trademark Office via EFS-Web.

Maria Arap August 10, 2016

Maria Arap Date

30 Rockefeller Plaza, 20th Floor
New York, New York 10112
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INFORMATION DISCLOSURE STATEMENT

Applicants hereby advise the Examiner of several co-pending applications with related subject matter:

1. Ser. No. 14/947,718, filed November 20, 2015 as a continuation of PCT/US14/39208 (of which the subject application is a national stage filing);
2. Ser. No. 14/943,898 filed November 17, 2015;
3. Ser. No.14/892,821, filed November 20, 2015; and
4. International Application Number PCT/US15/61120 filed November 17, 2015.

No fees are believed to be required in connection with this filing. Nevertheless, the Patent Office is hereby authorized to charge any fees that are required for consideration of this Information Disclosure Statement, and to credit any overpayment during prosecution of this application, to our Deposit Account No. 03-3125.

Respectfully submitted,

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/EDUARDO A RODELA/ 10/05/2016

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /E.A.R/

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L3	0	(wang near shih near yuan).in. and (W&W near sens).as.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2016/10/1 11:21
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S3	36214	H01L31/00,02,0216,02161,02164,02165,0232,02327,0236,02363,02366,,035281,06,09,10,101,102,11.cpc.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2016/09/1 09:40
S4	653	(micro near (cavity or structure or aperture$1 or hole$1)) with absorption	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/09/1 09:40
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S6	128707	apd or (avalanche near photo near diode)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/09/1 09:44
S7	40550	micro adj (cavity or structure or aperture$1 or hole$1)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/09/1 09:44
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S10	10	398/115.ccls. and apd	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/09/1 10:25
S11	10	(@pd<="20141118" or @rlpd<="20141118" or @ad<="20141118" or @rlad<="20141118") and S10	US-PGPUB; USPAT;	OR	ON	2016/09/1 10:25

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S12	8	"945003".ap.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/09/1 10:37
S13	58821	(photon or photo or light) near (detect$3 or absorb$3 or sens$3 or sensitive or transduc$3 or convers$3 or convert$3) with (diode or P-I-N)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/09/2 08:38
S14	12532630	holes or cavities or apertures	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/09/2 08:39
S15	1469	(@pd<="20140901" or @ad<="20140901" or @rlad<="20140901" or @rlpd<="20140901") and ("SiGe" or (silicon near germanium)) and S13 and S14	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/09/2 08:40
S16	575288	communicat$3 with (optical or light)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/09/2 08:42
S17	63533	broad near band	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/09/2 08:42
S18	70	(@pd<="20140901" or @ad<="20140901" or @rlad<="20140901" or @rlpd<="20140901") and ("SiGe" or (silicon near germanium)) and S13 and S14 and S16 and S17	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/09/2 08:42
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S22	78	rodela.xp. and optical	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/09/2 08:55
S23	7675	optical near confinement	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO;	OR	ON	2016/09/2 08:59

			DERWENT; IBM_TDB			
S24	6400	photonic near band near gap	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/09/2 08:59
S25	263	S23 and S24	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/09/2 08:59
S26	263	(@pd<="20140901" or @ad<="20140901" or @rlad<="20140901" or @rlpd<="20140901") and S25	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/09/2 09:00
S27	168254	("SiGe" or (silicon near germanium))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/09/2 09:02
S28	263	(@pd<="20140901" or @ad<="20140901" or @rlad<="20140901" or @rlpd<="20140901") and S25 and S23 and S24	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/09/2 09:02
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S31	34	(@pd<="20140901" or @ad<="20140901" or @rlad<="20140901" or @rlpd<="20140901") and (S24 same S30)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/09/2 09:33
S32	164	(@pd<="20140901" or @ad<="20140901" or @rlad<="20140901" or @rlpd<="20140901") and S24 and S30	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/09/2 09:35
S33	25	(892821|943898).ap.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/09/2 10:10
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S35	11803	photonic with (cavit$3 or hole or aperture$1)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/09/2 10:21
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			DERWENT; IBM_TDB			
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EAST Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
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L2	0	(wang near shih near yuan).in. and (W&W near sens).as.	US-PGPUB; USPAT	AND	ON	2016/10/13 11:20

10/13/2016 11:22:05 AM
C:\Users\erodela\Documents\eDAN\EAST\Workspaces\14945003.wsp

Dkt. 5176/88184-2

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application of: Shih-Yuan WANG et al.

Application No.: 14/945,003

Confirmation No.: 1200

GAU: 2893

Filed: November 18, 2015

Examiner: Rodela, Eduardo A.

For: MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES

This correspondence is being filed electronically with the U.S. Patent and Trademark Office via EFS-Web.	
/erin finnegan/	**September 27, 2016**
Erin Finnegan	Date

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INFORMATION DISCLOSURE STATEMENT

Applicants hereby advise the Examiner of the following co-pending applications with related subject matter:

1. Ser. No. 14/943,898 filed November 17, 2015;
2. PCT/US15/61120, filed November 17, 2015;
3. Ser. No.14/892,821, filed November 20, 2015 (allowed September 14, 2016);
4. Ser. No. 14/947,718, filed November 20, 2015;
5. PCT/US14/190189, filed May 22, 2014;
6. Ser. No. 13/821,963, filed October 22, 2013 (allowed September 13, 2016); and
7. PCT/US11/51091, filed September 9, 2011.

/EDUARDO A RODELA/ 10/05/2016

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /E.A.R/

No fees are believed to be required in connection with this filing. Nevertheless, the Patent Office is hereby authorized to charge any fees that are required for consideration of this Information Disclosure Statement, and to credit any overpayment during prosecution of this application, to our Deposit Account No. 03-3125.

Respectfully submitted,

/ivan s. kavrukov/

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Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	14945003	WANG ET AL.
	Examiner	Art Unit
	EDUARDO A RODELA	2893

CPC- SEARCHED		
Symbol	Date	Examiner
H01L31/00,02,0216,02161,02164,02165,0232,02327,0236,02363,02366,035281,06,09,10,101,102,11	10/13/2016	EAR

CPC COMBINATION SETS - SEARCHED		
Symbol	Date	Examiner

US CLASSIFICATION SEARCHED			
Class	Subclass	Date	Examiner

SEARCH NOTES		
Search Notes	Date	Examiner
EAST Search - see history for complete details	10/13/2016	EAR
Inventor's name and assignee search	10/13/2016	EAR

INTERFERENCE SEARCH			
US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner
noted cpc search area	in conjunction with a text search	10/13/2016	EAR

PTO/SB/08a (01-10)
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	14945003
Filing Date	2015-11-18
First Named Inventor	Shih-Yuan WANG et al.
Art Unit	
Examiner Name	RODELA, EDUARDO A
Attorney Docket Number	5176/88184-2

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Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	4637129		1987-01-20	DERKITS G. JR et al.	
	2	5457327A		1995-10-10	TAGUCHI, K	
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	5	7893348		2011-02-22	Korevan, B	
	6	8129710		2012-03-06	Cho, et al.	
	7	7601597		2009-10-13	Takei, M.	
	8	7115971		2006-10-03	Stumbo	

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Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
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Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2] i	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]

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	7	WO2012034078	WO		2015-03-05	Wang, S		
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Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T5
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EXAMINER SIGNATURE

Examiner Signature	/EDUARDO A RODELA/	Date Considered	10/05/2016

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

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Art Unit	
Examiner Name	RODELA, EDUARDO A
Attorney Docket Number	5176/88184-2

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

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☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

See attached certification statement.

The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/ivan s. kavrukov/	Date (YYYY-MM-DD)	2016-09-27
Name/Print	Ivan S. Kavrukov	Registration Number	25161

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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Notice of References Cited	Application/Control No. 14/945,003	Applicant(s)/Patent Under Reexamination WANG ET AL.	
	Examiner Eduardo A. Rodela	Art Unit 2893	Page 1 of 1

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*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	CPC Classification	US Classification
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	B	US-				
	C	US-				
	D	US-				
	E	US-				
	F	US-				
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SERIAL NUMBER	FILING or 371(c) DATE RULE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
14/945,003	11/18/2015	257	2893	5176-88184-2

APPLICANTS

W&Wsens, Devices Inc., Los Altos, CA;

INVENTORS

Shih-Yuan WANG, Palo Alto, CA;
Shih-Ping Wang, Los Altos, CA;

**** CONTINUING DATA ***************************

This appln claims benefit of 62/232,716 09/25/2015
and claims benefit of 62/213,556 09/02/2015
and claims benefit of 62/209,311 08/24/2015
and claims benefit of 62/205,717 08/15/2015
and claims benefit of 62/199,607 07/31/2015
and claims benefit of 62/197,120 07/27/2015
and claims benefit of 62/188,876 07/06/2015
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and claims benefit of 62/139,511 03/27/2015
and claims benefit of 62/111,582 02/03/2015
and claims benefit of 62/100,025 01/05/2015
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**** FOREIGN APPLICATIONS ***************************

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	5	20100193788		2010-08-05	Habib	
	6	20100197068		2010-08-05	Poon	
	7	20100126548		2010-05-27	JANG, ET AL.	
	8	20080265449		2008-10-30	Meinders et al.	

EFS Web 2.1.17

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /E.A.R/

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	14945003
	Filing Date	2015-11-18
	First Named Inventor	Shih-Yuan WANG et al.
	Art Unit	
	Examiner Name	not yet assigned
	Attorney Docket Number	5176/88184-2

	9	20090188557		2009-07-30	Wang, et al.	
	10	20080265449		2008-09-25	Heidari	

If you wish to add additional U.S. Published Application citation information please click the Add button.

FOREIGN PATENT DOCUMENTS

Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2] i	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]
	1	WO2012149441A2	wo		2012-11-01	CHANG-HASNAIN, Connie et al.		☐
	2	PCT/JP2014/39208	JP		2014-11-28	International Search Report		☐
	3	PCT/US1561120	US		2015-11-17	WANG, S		☐
	4	PCT/US1439208	US		2014-05-22	WANG, S		☐
	5	PCT/US15/61120	US		2015-11-17	WANG, S		☐
	6	PCT/US11/51091	US		2011-09-09	WANG, S		☐
	7	WO2012034078	WO		2015-03-05	Wang, S		☐

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
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	Filing Date	2015-11-18
	First Named Inventor	Shih-Yuan WANG et al.
	Art Unit	
	Examiner Name	not yet assigned
	Attorney Docket Number	5176/88184-2

	8	WO2014190189	WO		2014-11-27	Wang, S		☐

If you wish to add additional Foreign Patent Document citation information please click the Add button

NON-PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T§
	1	Ren, R., et al., "Enhanced absorption in elliptical silicon nanowire arrays for solar energy harvesting", Optical Engineering, Vol 53(2), 027102, February, (2014), http://opticalengineering.spiedigitallibrary.org/article.aspx?articleid=1828860	☐
	2	Dayal, G., et al, "Broadband infrared metamaterial absorber with visible transparency using ITO as ground plane", OPTICS EXPRESS 15104 June (2014).	☐
	3	Donnelly, J. L., et al., "Mode-based analysis of silicon nanohole arrays for photovoltaic applications," Vol. 22, No. S5, OPTICS EXPRESS, A1343 25, August (2014).	☐
	4	Gasca, L., "From O to L: The Future of Optical-Wavelength Bands," BROADBAND PROPERTIES," June, (2008) www.broadbandproperties.com	☐
	5	Finisar, "World's Largest Supplier of Optical Solutions for the Communications Industry," http://files.shareholder.com/downloads/FNSR/0x0x382377/0b3893ee-fb06-417d-ac71-84f2f9084b0d/Finisar_Investor_Presentation.pdf.)	☐
	6	Silvaco., "Investigation of the SiGe Waveguide Phototides Using FDTD Method for High Speed Optical Communication," Simulation Standard, http://www.silvaco.com/tech_lib_TCAD/simulationstandard/2010/apr_may_jun/a1/a1.html)	☐
	7	Kolodzey, J., et al, "Optical and electronic properties of SiGeC alloys grown on Si substrates," Journal of Crystal Growth 157, 386-391, (1995).	☐
	8	Kraus, T.F., "Slow light in photonic crystal waveguides," Journal of Physics D: Applied Physics, Vol. 40, (2007).	☐

EFS Web 2.1.17

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	Examiner Name	not yet assigned
	Attorney Docket Number	5176/88184-2

	9	Liu, A., et al., "Quantum dot lasers for silicon photonics [invited]," Photonics Research, Vol. 3, No. 5, October, (2015).	☐
	10	Liu, N., et al, "Infrared Perfect Absorber and Its Application As Plasmonic Sensor," Nano Lett. 10, 2342–2348, (2010).	☐
	11	Kang, Y., "Monolithic Ge/Si Avalnache Photodiodes," 978-1-4244-4403, IEEE, (2009).	☐
	12	Liu, A.Y., et al., Quantum Dot Lasers on Silicon," aUCSB Materials Department, Santa Barbara, California, USA, bUCSB Department of Electrical and Computer Engineering, Santa Barbara, California, USA	☐
	13	Logeeswaran, V.J., "A 14-ps full width at half maximum high-speed photoconductor fabricated with intersecting InP nanowires on an amorphous surface," Applied Physics A, Vol. 91, 1-5., (2008).	☐
	14	Hu, L., et al. "Analysis of Optical Absorption in Silicon Nanowire Arrays for Photovoltaic Applications," NANO LETT. Vol. 7, No. 11, 2007.	☐
	15	Meng, L., et al. "Polarization-sensitive perfect absorbers at near-infrared wavelengths," OPTICS EXPRESS, A111, December, (2012).	☐
	16	Molin, D., "850-950nm WideBand OM4 Multimode Fiber for Next-Generation WDM Systems," OFC (2015).	☐
	17	Piels, et al., "40 GHz Si/Ge uni-traveling carrier waveguide phototiode", Journal of Lightwave Technology, 15908, (2014).	☐
	18	Fountaine, K., et al., "Near-unity broadband absorption designs for semiconducting nanowire arrays via localized radial mode excitation", Vol. 22, No. OPTICS EXPRESS A930, 5 May (2014).	☐
	19	Feng, D., et al, "High-speed Ge photodetector monolithically integrated with large cross-section silicon-on-insulator waveguide," Applied Physics Letters 95, 261105 (2009).	☐

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
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	First Named Inventor	Shih-Yuan WANG et al.
	Art Unit	
	Examiner Name	not yet assigned
	Attorney Docket Number	5176/88184-2

	20	Schaub, J.D., et al. "Resonant-Cavity-Enhanced High-Speed Si Photodiode Grown by Epitaxial Lateral Overgrowth," IIEE Photonics Technology Letters, Vol. 11, No. 12, December, 1999.	☐
	21	Seyedi, M.A., et al., "Efficient Schottky-like junction GaAs nanowire photodetector with 9 GHz modulation bandwidth with large active area," APPLIED PHYSICS LETTERS 105, 041105 (2014).	☐
	22	Piatek, S., "Physics and Operation of an MPPC," Tutorials, Hamamatsu Phototonics, November 16, (2015); http://www.hamamatsu.com/us/en/community/optical_sensors/tutorials/physics_of_mppc/index.html?utm_source=googleplus&utm_medium=social&utm_campaign=hc-social	☐
	23	Garnett, E., "Light Trapping in Silicon Nanowire Solar Cells", Nano Letters, (2010) pg. 10, 1082--1087.	☐
	24	Tanus et al.: "High-performance 1200-nm InGaAs and 1300- nm InGaAsN quantum-well lasers by metalorganic chemical vapor deposition," Selected Topics in Quantum Electronics, IEEE Journal of SELECTED TOPICS IN QUANTUM ELECTRONICS, Vol. 9, Issue: 5 (2003).	☐
	25	Kelzenberg, et al., "Enhanced absorption and carrier collection in Si wire arrays for photovoltaic applications. Nature Materials, Vol. 9, March (2010), pg. 239-244. http://authors.library.caltech.edu/17988/	☐
	26	Lin, et al., "Optical absorption enhancement in silicon nanowire and nanohole arrays for photovoltaic applications," Proceeding of SPIE, Vol. 772, 77721G-1, (2010).	☐
	27	Chang-Hasnain, C., et al., "High contrast gratings for integrated optoelectronics, Advances in Optics and Photonics Vol. 4, (2012), pg. 379-440. http://www.eecs.berkeley.edu/Pubs/TechRpts/2014/EECS-2014-197.html	☐
	28	Chu, H-J ,et al , "Wurtzite InP nanowire arrays grown by selective area MOCVD," Phys. Status Solidi Vol. C 7, No. 10, (2010), pg. 2494 -- 2497.	☐
	29	Kang et al., "Epitaxially-grown Ge/Si avalanche photodiodes for 1.3μm light detection," OPTICS EXPRESS 9365, Vol. 16, No. 13, June 23, 2008.	☐
	30	International Search Report dated November 28, 2014 in PCT/US2014/59208.	☐

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /E.A.R/

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	14945003
	Filing Date	2015-11-18
	First Named Inventor	Shih-Yuan WANG et al.
	Art Unit	
	Examiner Name	not yet assigned
	Attorney Docket Number	5178/88184-2

	31	International Search Report dated December 23, 2011 in PCT/US2011/051091.	☐

If you wish to add additional non-patent literature document citation information please click the Add button

EXAMINER SIGNATURE

Examiner Signature	/EDUARDO A RODELA/	Date Considered	10/05/2016

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /E.A.R/

Applicant-Initiated Interview Summary	Application No.	Applicant(s)	
	14/945,003	WANG ET AL.	
	Examiner	Art Unit	
	Eduardo A. Rodela	2893	

All participants (applicant, applicant's representative, PTO personnel):

(1) *Eduardo A. Rodel, Examiner*. (3)_____.

(2) *Ivan S. Kavrukov, Applicant's Representative*. (4)_____.

Date of Interview: *05 October 2016*.

Type: ☒ Telephonic ☐ Video Conference
☐ Personal [copy given to: ☐ applicant ☐ applicant's representative]

Exhibit shown or demonstration conducted: ☐ Yes ☒ No.
If Yes, brief description: _____.

Issues Discussed ☐101 ☐112 ☒102 ☒103 ☐Others
(For each of the checked box(es) above, please describe below the issue and detailed description of the discussion)

Claim(s) discussed: *1,12,18 and 31*.

Identification of prior art discussed: *Dutta (US 8,357,960)*.

Substance of Interview
(For each issue discussed, provide a detailed description and indicate if agreement was reached. Some topics may include: identification or clarification of a reference or a portion thereof, claim interpretation, proposed amendments, arguments of any applied references etc...)

A discussion took place on how to differentiate the instant application from the prior art of Dutta Figures 3, 4A and 6B, where Dutta teaches SiGe PIN diodes. The distinction was agreed upon that the instant application's current claim set was focusing on holes within a light absorbing layer and that to specify beyond the pillars of Dutta by specifying that the photon absorbing region comprising an I-region is a single layer with a plurlaity of holes therein. Applicant's Representative suggested language the Examiner agreed would place the application in condition for allowance. The limitation of the holes in the photon absorbing region being one of several additional distinctions.

Applicant recordation instructions: The formal written reply to the last Office action must include the substance of the interview. (See MPEP section 713.04). If a reply to the last Office action has already been filed, applicant is given a non-extendable period of the longer of one month or thirty days from this interview date, or the mailing date of this interview summary form, whichever is later, to file a statement of the substance of the interview

Examiner recordation instructions: Examiners must summarize the substance of any interview of record. A complete and proper recordation of the substance of an interview should include the items listed in MPEP 713.04 for complete and proper recordation including the identification of the general thrust of each argument or issue discussed, a general indication of any other pertinent matters discussed regarding patentability and the general results or outcome of the interview, to include an indication as to whether or not agreement was reached on the issues raised.

☐ Attachment

/Eduardo A. Rodela/ Primary Examiner, Art Unit 2893	

Summary of Record of Interview Requirements

Manual of Patent Examining Procedure (MPEP), Section 713.04, Substance of Interview Must be Made of Record
A complete written statement as to the substance of any face-to-face, video conference, or telephone interview with regard to an application must be made of record in the application whether or not an agreement with the examiner was reached at the interview.

Title 37 Code of Federal Regulations (CFR) § 1.133 Interviews
Paragraph (b)

In every instance where reconsideration is requested in view of an interview with an examiner, a complete written statement of the reasons presented at the interview as warranting favorable action must be filed by the applicant. An interview does not remove the necessity for reply to Office action as specified in §§ 1.111, 1.135. (35 U.S.C. 132)

37 CFR §1.2 Business to be transacted in writing.
All business with the Patent or Trademark Office should be transacted in writing. The personal attendance of applicants or their attorneys or agents at the Patent and Trademark Office is unnecessary. The action of the Patent and Trademark Office will be based exclusively on the written record in the Office. No attention will be paid to any alleged oral promise, stipulation, or understanding in relation to which there is disagreement or doubt.

———

The action of the Patent and Trademark Office cannot be based exclusively on the written record in the Office if that record is itself incomplete through the failure to record the substance of interviews.

It is the responsibility of the applicant or the attorney or agent to make the substance of an interview of record in the application file, unless the examiner indicates he or she will do so. It is the examiner's responsibility to see that such a record is made and to correct material inaccuracies which bear directly on the question of patentability.

Examiners must complete an Interview Summary Form for each interview held where a matter of substance has been discussed during the interview by checking the appropriate boxes and filling in the blanks. Discussions regarding only procedural matters, directed solely to restriction requirements for which interview recordation is otherwise provided for in Section 812.01 of the Manual of Patent Examining Procedure, or pointing out typographical errors or unreadable script in Office actions or the like, are excluded from the interview recordation procedures below. Where the substance of an interview is completely recorded in an Examiners Amendment, no separate Interview Summary Record is required.

The Interview Summary Form shall be given an appropriate Paper No., placed in the right hand portion of the file, and listed on the "Contents" section of the file wrapper. In a personal interview, a duplicate of the Form is given to the applicant (or attorney or agent) at the conclusion of the interview. In the case of a telephone or video-conference interview, the copy is mailed to the applicant's correspondence address either with or prior to the next official communication. If additional correspondence from the examiner is not likely before an allowance or if other circumstances dictate, the Form should be mailed promptly after the interview rather than with the next official communication.

The Form provides for recordation of the following information:
- Application Number (Series Code and Serial Number)
- Name of applicant
- Name of examiner
- Date of interview
- Type of interview (telephonic, video-conference, or personal)
- Name of participant(s) (applicant, attorney or agent, examiner, other PTO personnel, etc.)
- An indication whether or not an exhibit was shown or a demonstration conducted
- An identification of the specific prior art discussed
- An indication whether an agreement was reached and if so, a description of the general nature of the agreement (may be by attachment of a copy of amendments or claims agreed as being allowable). Note: Agreement as to allowability is tentative and does not restrict further action by the examiner to the contrary.
- The signature of the examiner who conducted the interview (if Form is not an attachment to a signed Office action)

It is desirable that the examiner orally remind the applicant of his or her obligation to record the substance of the interview of each case. It should be noted, however, that the Interview Summary Form will not normally be considered a complete and proper recordation of the interview unless it includes, or is supplemented by the applicant or the examiner to include, all of the applicable items required below concerning the substance of the interview.

A complete and proper recordation of the substance of any interview should include at least the following applicable items:
1) A brief description of the nature of any exhibit shown or any demonstration conducted,
2) an identification of the claims discussed,
3) an identification of the specific prior art discussed,
4) an identification of the principal proposed amendments of a substantive nature discussed, unless these are already described on the Interview Summary Form completed by the Examiner,
5) a brief identification of the general thrust of the principal arguments presented to the examiner,
   (The identification of arguments need not be lengthy or elaborate. A verbatim or highly detailed description of the arguments is not required. The identification of the arguments is sufficient if the general nature or thrust of the principal arguments made to the examiner can be understood in the context of the application file. Of course, the applicant may desire to emphasize and fully describe those arguments which he or she feels were or might be persuasive to the examiner.)
6) a general indication of any other pertinent matters discussed, and
7) if appropriate, the general results or outcome of the interview unless already described in the Interview Summary Form completed by the examiner.

Examiners are expected to carefully review the applicant's record of the substance of an interview. If the record is not complete and accurate, the examiner will give the applicant an extendable one month time period to correct the record.

Examiner to Check for Accuracy

If the claims are allowable for other reasons of record, the examiner should send a letter setting forth the examiner's version of the statement attributed to him or her. If the record is complete and accurate, the examiner should place the indication, "Interview Record OK" on the paper recording the substance of the interview along with the date and the examiner's initials.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

23432 7590 10/17/2016

COOPER & DUNHAM, LLP
30 Rockefeller Plaza
20th Floor
NEW YORK, NY 10112

EXAMINER
RODELA, EDUARDO A

ART UNIT	PAPER NUMBER
2893	

DATE MAILED: 10/17/2016

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/945,003	11/18/2015	Shih-Yuan WANG	5176-88184-2	1200

TITLE OF INVENTION: MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	SMALL	$480	$0	$0	$480	01/17/2017

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

For purposes of this notice, small entity fees are 1/2 the amount of undiscounted fees, and micro entity fees are 1/2 the amount of small entity fees.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PTOL-85 (Rev. 02/11)

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

23432 7590 10/17/2016
COOPER & DUNHAM, LLP
30 Rockefeller Plaza
20th Floor
NEW YORK, NY 10112

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission
I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/945,003	11/18/2015	Shih-Yuan WANG	5176-88184-2	1200

TITLE OF INVENTION: MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	SMALL	$480	$0	$0	$480	01/17/2017

EXAMINER	ART UNIT	CLASS-SUBCLASS
RODELA, EDUARDO A	2893	257-432000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
- ❑ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
- ❑ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.
1 _____
2 _____
3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ❑ Corporation or other private group entity ❑ Government

4a. The following fee(s) are submitted:
- ❑ Issue Fee
- ❑ Publication Fee (No small entity discount permitted)
- ❑ Advance Order - # of Copies _____

4b. Payment of Fee(s): **(Please first reapply any previously paid issue fee shown above)**
- ❑ A check is enclosed.
- ❑ Payment by credit card. Form PTO-2038 is attached.
- ❑ The director is hereby authorized to charge the required fee(s), any deficiency, or credits any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)
- ❑ Applicant certifying micro entity status. See 37 CFR 1.29 — NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.
- ❑ Applicant asserting small entity status. See 37 CFR 1.27 — NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.
- ❑ Applicant changing to regular undiscounted fee status. — NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

PTOL-85 Part B (10-13) Approved for use through 10/31/2013. OMB 0651-0033 U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/945,003	11/18/2015	Shih-Yuan WANG	5176-88184-2	1200

23432 7590 10/17/2016

COOPER & DUNHAM, LLP
30 Rockefeller Plaza
20th Floor
NEW YORK, NY 10112

EXAMINER	
RODELA, EDUARDO A	

ART UNIT	PAPER NUMBER
2893	

DATE MAILED: 10/17/2016

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(Applications filed on or after May 29, 2000)

The Office has discontinued providing a Patent Term Adjustment (PTA) calculation with the Notice of Allowance.

Section 1(h)(2) of the AIA Technical Corrections Act amended 35 U.S.C. 154(b)(3)(B)(i) to eliminate the requirement that the Office provide a patent term adjustment determination with the notice of allowance. See Revisions to Patent Term Adjustment, 78 Fed. Reg. 19416, 19417 (Apr. 1, 2013). Therefore, the Office is no longer providing an initial patent term adjustment determination with the notice of allowance. The Office will continue to provide a patent term adjustment determination with the Issue Notification Letter that is mailed to applicant approximately three weeks prior to the issue date of the patent, and will include the patent term adjustment on the patent. Any request for reconsideration of the patent term adjustment determination (or reinstatement of patent term adjustment) should follow the process outlined in 37 CFR 1.705.

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

OMB Clearance and PRA Burden Statement for PTOL-85 Part B

The Paperwork Reduction Act (PRA) of 1995 requires Federal agencies to obtain Office of Management and Budget approval before requesting most types of information from the public. When OMB approves an agency request to collect information from the public, OMB (i) provides a valid OMB Control Number and expiration date for the agency to display on the instrument that will be used to collect the information and (ii) requires the agency to inform the public about the OMB Control Number's legal significance in accordance with 5 CFR 1320.5(b).

The information collected by PTOL-85 Part B is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450. Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Applicant-Initiated Interview Summary	Application No.	Applicant(s)	
	14/945,003	WANG ET AL.	
	Examiner	Art Unit	
	Eduardo A. Rodela	2893	

All participants (applicant, applicant's representative, PTO personnel):

(1) *Eduardo A. Rodel, Examiner*. (3)_____.

(2) *Ivan S. Kavrukov, Applicant's Representative*. (4)_____.

Date of Interview: *05 October 2016*.

Type: ☒ Telephonic ☐ Video Conference
☐ Personal [copy given to: ☐ applicant ☐ applicant's representative]

Exhibit shown or demonstration conducted: ☐ Yes ☒ No.
If Yes, brief description: _____.

Issues Discussed ☐101 ☐112 ☒102 ☒103 ☐Others
(For each of the checked box(es) above, please describe below the issue and detailed description of the discussion)

Claim(s) discussed: *1,12,18 and 31*.

Identification of prior art discussed: *Dutta (US 8,357,960)*.

Substance of Interview
(For each issue discussed, provide a detailed description and indicate if agreement was reached. Some topics may include: identification or clarification of a reference or a portion thereof, claim interpretation, proposed amendments, arguments of any applied references etc...)

A discussion took place on how to differentiate the instant application from the prior art of Dutta Figures 3, 4A and 6B, where Dutta teaches SiGe PIN diodes. The distinction was agreed upon that the instant application's current claim set was focusing on holes within a light absorbing layer and that to specify beyond the pillars of Dutta by specifying that the photon absorbing region comprising an I-region is a single layer with a plurlaity of holes therein. Applicant's Representative suggested language the Examiner agreed would place the application in condition for allowance. The limitation of the holes in the photon absorbing region being one of several additional distinctions.

Applicant recordation instructions: The formal written reply to the last Office action must include the substance of the interview. (See MPEP section 713.04). If a reply to the last Office action has already been filed, applicant is given a non-extendable period of the longer of one month or thirty days from this interview date, or the mailing date of this interview summary form, whichever is later, to file a statement of the substance of the interview

Examiner recordation instructions: Examiners must summarize the substance of any interview of record. A complete and proper recordation of the substance of an interview should include the items listed in MPEP 713.04 for complete and proper recordation including the identification of the general thrust of each argument or issue discussed, a general indication of any other pertinent matters discussed regarding patentability and the general results or outcome of the interview, to include an indication as to whether or not agreement was reached on the issues raised.

☐ Attachment

/Eduardo A. Rodela/ Primary Examiner, Art Unit 2893	

Summary of Record of Interview Requirements

Manual of Patent Examining Procedure (MPEP), Section 713.04, Substance of Interview Must be Made of Record
A complete written statement as to the substance of any face-to-face, video conference, or telephone interview with regard to an application must be made of record in the application whether or not an agreement with the examiner was reached at the interview.

Title 37 Code of Federal Regulations (CFR) § 1.133 Interviews
Paragraph (b)

In every instance where reconsideration is requested in view of an interview with an examiner, a complete written statement of the reasons presented at the interview as warranting favorable action must be filed by the applicant. An interview does not remove the necessity for reply to Office action as specified in §§ 1.111, 1.135. (35 U.S.C. 132)

37 CFR §1.2 Business to be transacted in writing.
All business with the Patent or Trademark Office should be transacted in writing. The personal attendance of applicants or their attorneys or agents at the Patent and Trademark Office is unnecessary. The action of the Patent and Trademark Office will be based exclusively on the written record in the Office. No attention will be paid to any alleged oral promise, stipulation, or understanding in relation to which there is disagreement or doubt.

———

The action of the Patent and Trademark Office cannot be based exclusively on the written record in the Office if that record is itself incomplete through the failure to record the substance of interviews.

It is the responsibility of the applicant or the attorney or agent to make the substance of an interview of record in the application file, unless the examiner indicates he or she will do so. It is the examiner's responsibility to see that such a record is made and to correct material inaccuracies which bear directly on the question of patentability.

Examiners must complete an Interview Summary Form for each interview held where a matter of substance has been discussed during the interview by checking the appropriate boxes and filling in the blanks. Discussions regarding only procedural matters, directed solely to restriction requirements for which interview recordation is otherwise provided for in Section 812.01 of the Manual of Patent Examining Procedure, or pointing out typographical errors or unreadable script in Office actions or the like, are excluded from the interview recordation procedures below. Where the substance of an interview is completely recorded in an Examiners Amendment, no separate Interview Summary Record is required.

The Interview Summary Form shall be given an appropriate Paper No., placed in the right hand portion of the file, and listed on the "Contents" section of the file wrapper. In a personal interview, a duplicate of the Form is given to the applicant (or attorney or agent) at the conclusion of the interview. In the case of a telephone or video-conference interview, the copy is mailed to the applicant's correspondence address either with or prior to the next official communication. If additional correspondence from the examiner is not likely before an allowance or if other circumstances dictate, the Form should be mailed promptly after the interview rather than with the next official communication.

The Form provides for recordation of the following information:
- Application Number (Series Code and Serial Number)
- Name of applicant
- Name of examiner
- Date of interview
- Type of interview (telephonic, video-conference, or personal)
- Name of participant(s) (applicant, attorney or agent, examiner, other PTO personnel, etc.)
- An indication whether or not an exhibit was shown or a demonstration conducted
- An identification of the specific prior art discussed
- An indication whether an agreement was reached and if so, a description of the general nature of the agreement (may be by attachment of a copy of amendments or claims agreed as being allowable). Note: Agreement as to allowability is tentative and does not restrict further action by the examiner to the contrary.
- The signature of the examiner who conducted the interview (if Form is not an attachment to a signed Office action)

It is desirable that the examiner orally remind the applicant of his or her obligation to record the substance of the interview of each case. It should be noted, however, that the Interview Summary Form will not normally be considered a complete and proper recordation of the interview unless it includes, or is supplemented by the applicant or the examiner to include, all of the applicable items required below concerning the substance of the interview.

A complete and proper recordation of the substance of any interview should include at least the following applicable items:
1) A brief description of the nature of any exhibit shown or any demonstration conducted,
2) an identification of the claims discussed,
3) an identification of the specific prior art discussed,
4) an identification of the principal proposed amendments of a substantive nature discussed, unless these are already described on the Interview Summary Form completed by the Examiner,
5) a brief identification of the general thrust of the principal arguments presented to the examiner,
   (The identification of arguments need not be lengthy or elaborate. A verbatim or highly detailed description of the arguments is not required. The identification of the arguments is sufficient if the general nature or thrust of the principal arguments made to the examiner can be understood in the context of the application file. Of course, the applicant may desire to emphasize and fully describe those arguments which he or she feels were or might be persuasive to the examiner.)
6) a general indication of any other pertinent matters discussed, and
7) if appropriate, the general results or outcome of the interview unless already described in the Interview Summary Form completed by the examiner.

Examiners are expected to carefully review the applicant's record of the substance of an interview. If the record is not complete and accurate, the examiner will give the applicant an extendable one month time period to correct the record.

Examiner to Check for Accuracy

If the claims are allowable for other reasons of record, the examiner should send a letter setting forth the examiner's version of the statement attributed to him or her. If the record is complete and accurate, the examiner should place the indication, "Interview Record OK" on the paper recording the substance of the interview along with the date and the examiner's initials.

Notice of Allowability	Application No. 14/945,003	Applicant(s) WANG ET AL.	
	Examiner Eduardo A. Rodela	Art Unit 2893	AIA (First Inventor to File) Status Yes

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *telephone interview 10/5/2016*.
   ☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on_____.
2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.
3. ☒ The allowed claim(s) is/are *1-5, 7-19, 22-24, 28-33 and 36*. As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.
4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

   Certified copies:

   a) ☐ All b) ☐ Some *c) ☐ None of the:
   1. ☐ Certified copies of the priority documents have been received.
   2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
   3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☒ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date See Continuation Sheet
3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
4. ☒ Interview Summary (PTO-413), Paper No./Mail Date *10/5/16* .
5. ☒ Examiner's Amendment/Comment
6. ☒ Examiner's Statement of Reasons for Allowance
7. ☐ Other _____.

/Eduardo A. Rodela/
Primary Examiner, Art Unit 2893

Continuation of Attachment(s) 2. Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date: 7/19/16, 8/10/16, 9/27/16.

The present application, filed on or after March 16, 2013, is being examined under the first inventor to file provisions of the AIA.

DETAILED ACTION

This office action is in response to the telephonic applicant initiated interview dated October 6, 2016. Claims 1-5, 7-19, 22-24, 28-33 and 36 are under consideration.

Terminal Disclaimer

The terminal disclaimer filed on October 6, 2016 has been reviewed and is accepted. The terminal disclaimer has been recorded.

EXAMINER'S AMENDMENT

An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in an interview with Ivan S. Kavrukov on October 6, 2016.

The application has been amended as follows:

In the Claims:

With respect to the September 29, 2016 claim set:

Regarding claim 1, on line 8, between "comprises" and "a", please insert "a substantially continuous layer interrupted by".

Regarding claim 12, on line 7, please replace "with" with "a substantially continuous layer interrupted by".

Regarding claim 18, on line 11, please insert between "including" and "a" the following, "a substantially continuous layer interrupted by".

Regarding claim 31, on lines 13 and 19, please delete all instances of "pillars or". On line 13, between "comprises" and "intentionally", please insert "a substantially continuous layer interrupted by".

Please cancel claims 34 and 35.

Regarding claim 36, on line 1, delete "pillars or".

REASONS FOR ALLOWANCE

Claims 1-5, 7-19, 22-24, 28-33 and 36 are allowed.

The following is an Examiner's statement of reasons for allowance: The PIN diode photodetector with plurality of holes therein to enhance performance characteristics as recited in the claims of the instant invention fail to be taught by the prior art cited of interest.

Regarding claims 1, 12, 18 and 31, the prior art of Dutta (US 8,357,960) teaches a PIN diode photodetector created by a plurality of neighboring PIN diode columns, but fails to disclose the specific characteristic recited in the claims of the instant invention e.g. wherein the PIN diode detector is made of a continuous layer with a plurality of holes therein.

Fax / Telephone Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eduardo A. Rodela whose telephone number is (571)272-8797. The examiner can normally be reached on M-F, 9 AM - 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (571)272-1664. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Eduardo A. Rodela/
Primary Examiner, Art Unit 2893

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	14945003	WANG ET AL.
	Examiner	**Art Unit**
	EDUARDO A RODELA	2893

CPC							
Symbol						**Type**	**Version**
H01L		31	/	02363		F	2013-01-01
H01L		31	/	02327		I	2013-01-01
H01L		27	/	1443		I	2013-01-01
H01L		27	/	1446		I	2013-01-01
H01L		31	/	103		I	2013-01-01
H04B		10	/	691		I	2013-01-01
H01L		31	/	09		I	2013-01-01
H01L		31	/	0232		I	2013-01-01
H01L		31	/	02		I	2013-01-01
H01L		31	/	0236		I	2013-01-01
			/				
			/				
			/				
			/				
			/				

CPC Combination Sets							
Symbol					**Type**	**Set**	**Ranking**	**Version**
			/					
			/					

NONE		**Total Claims Allowed:**	
(Assistant Examiner)	(Date)	29	
/EDUARDO A RODELA/ Primary Examiner.Art Unit 2893	10/13/2016	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	6B

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	14945003	WANG ET AL.
	Examiner	**Art Unit**
	EDUARDO A RODELA	2893

US ORIGINAL CLASSIFICATION		INTERNATIONAL CLASSIFICATION										
CLASS	SUBCLASS	CLAIMED					NON-CLAIMED					
		H	0	1	L	31 / 0236 (2006.01.01)						
CROSS REFERENCE(S)												
CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)											

NONE		Total Claims Allowed:	
(Assistant Examiner)	(Date)	29	
/EDUARDO A RODELA/ Primary Examiner.Art Unit 2893	10/13/2016	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	6B

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	14945003	WANG ET AL.
	Examiner	**Art Unit**
	EDUARDO A RODELA	2893

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☒ T.D. ☐ R.1.47

Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
1	1	16	17	28	33										
2	2	17	18		34										
3	3	18	19		35										
4	4	19	20	29	36										
5	5		21												
	6	20	22												
6	7	21	23												
7	8	22	24												
8	9		25												
9	10		26												
10	11		27												
11	12	23	28												
12	13	24	29												
13	14	25	30												
14	15	26	31												
15	16	27	32												

NONE (Assistant Examiner)	(Date)	**Total Claims Allowed:** 29	
/EDUARDO A RODELA/ Primary Examiner.Art Unit 2893 (Primary Examiner)	10/13/2016 (Date)	O.G. Print Claim(s) 1	O.G. Print Figure 6B

UNITED STATES PATENT AND TRADEMARK OFFICE

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APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	TOT CLAIMS	IND CLAIMS
14/945,003	11/18/2015	2893	1810	5176-88184-2	30	3

CONFIRMATION NO. 1200

CORRECTED FILING RECEIPT

23432
COOPER & DUNHAM, LLP
30 Rockefeller Plaza
20th Floor
NEW YORK, NY 10112

Date Mailed: 10/07/2016

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Inventor(s)

Shih-Yuan WANG, Palo Alto, CA;
Shih-Ping Wang, Los Altos, CA;

Applicant(s)

W&Wsens, Devices Inc., Los Altos, CA;

Power of Attorney: The patent practitioners associated with Customer Number 23432

Domestic Priority data as claimed by applicant

This appln claims benefit of 62/232,716 09/25/2015
and claims benefit of 62/213,556 09/02/2015
and claims benefit of 62/209,311 08/24/2015
and claims benefit of 62/205,717 08/15/2015
and claims benefit of 62/199,607 07/31/2015
and claims benefit of 62/197,120 07/27/2015
and claims benefit of 62/188,876 07/06/2015
and claims benefit of 62/182,602 06/21/2015
and claims benefit of 62/175,855 06/15/2015
and claims benefit of 62/174,498 06/11/2015
and claims benefit of 62/171,915 06/05/2015
and claims benefit of 62/157,876 05/06/2015
and claims benefit of 62/154,675 04/29/2015
and claims benefit of 62/153,443 04/27/2015
and claims benefit of 62/139,511 03/27/2015
and claims benefit of 62/111,582 02/03/2015
and claims benefit of 62/100,025 01/05/2015
and claims benefit of 62/090,879 12/11/2014

and claims benefit of 62/081,538 11/18/2014

Foreign Applications for which priority is claimed (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see http://www.uspto.gov for more information.) - None.
Foreign application information must be provided in an Application Data Sheet in order to constitute a claim to foreign priority. See 37 CFR 1.55 and 1.76.

Permission to Access Application via Priority Document Exchange: No

Permission to Access Search Results: No

Applicant may provide or rescind an authorization for access using Form PTO/SB/39 or Form PTO/SB/69 as appropriate.

If Required, Foreign Filing License Granted: 12/02/2015

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 14/945,003**

Projected Publication Date: 10/20/2016

Non-Publication Request: No

Early Publication Request: No
** **SMALL ENTITY** **
Title

MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES

Preliminary Class

257

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications: No

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application

serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at http://www.uspto.gov/web/offices/pac/doc/general/index.html.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, http://www.stopfakes.gov. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4258).

LICENSE FOR FOREIGN FILING UNDER

Title 35, United States Code, Section 184

Title 37, Code of Federal Regulations, 5.11 & 5.15

GRANTED

The applicant has been granted a license under 35 U.S.C. 184, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" followed by a date appears on this form. Such licenses are issued in all applications where the conditions for issuance of a license have been met, regardless of whether or not a license may be required as set forth in 37 CFR 5.15. The scope and limitations of this license are set forth in 37 CFR 5.15(a) unless an earlier license has been issued under 37 CFR 5.15(b). The license is subject to revocation upon written notification. The date indicated is the effective date of the license, unless an earlier license of similar scope has been granted under 37 CFR 5.13 or 5.14.

This license is to be retained by the licensee and may be used at any time on or after the effective date thereof unless it is revoked. This license is automatically transferred to any related applications(s) filed under 37 CFR 1.53(d). This license is not retroactive.

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NOT GRANTED

No license under 35 U.S.C. 184 has been granted at this time, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" DOES NOT appear on this form. Applicant may still petition for a license under 37 CFR 5.12, if a license is desired before the expiration of 6 months from the filing date of the application. If 6 months has lapsed from the filing date of this application and the licensee has not received any indication of a secrecy order under 35 U.S.C. 181, the licensee may foreign file the application pursuant to 37 CFR 5.15(b).

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United States Patent and Trademark Office
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P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
14/945,003	11/18/2015	Shih-Yuan WANG	5176-88184-2

CONFIRMATION NO. 1200

POA ACCEPTANCE LETTER

23432
COOPER & DUNHAM, LLP
30 Rockefeller Plaza
20th Floor
NEW YORK, NY 10112

OC000000086348127

Date Mailed: 10/07/2016

NOTICE OF ACCEPTANCE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 10/05/2016.

The Power of Attorney in this application is accepted. Correspondence in this application will be mailed to the above address as provided by 37 CFR 1.33.

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at **(571) 272-4000** or **(571) 272-4200** or **1-888-786-0101**.

/lqchau/

Application Number	Application/Control No.	Applicant(s)/Patent under Reexamination	
	14/945,003	WANG ET AL.	

Document Code - DISQ	Internal Document – DO NOT MAIL

TERMINAL DISCLAIMER	☒ APPROVED	☐ DISAPPROVED
Date Filed : 06 October, 2016	**This patent is subject to a Terminal Disclaimer**	

Approved/Disapproved by:

CHARRISSA BROWN

Technology Center: PLRC

Telephone: (571)272-1558

U.S. Patent and Trademark Office

PTO/SB/25 (07-09)
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TERMINAL DISCLAIMER TO OBVIATE A PROVISIONAL DOUBLE PATENTING REJECTION OVER A PENDING "REFERENCE" APPLICATION

Docket Number (Optional): 5178-68184-2

In re Application of: Shih-Yuan WANG

Application No.: 14/945,003

Filed: November 18, 2015

For: MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES

The owner*, W&Wsens Devices Inc., of 100 percent interest in the instant application hereby disclaims, except as provided below, the terminal part of the statutory term of any patent granted on the instant application which would extend beyond the expiration date of the full statutory term of any patent granted on pending **reference** Application Number 14/892,821, filed on 11-20-2015, as such term is defined in 35 U.S.C. 154 and 173, and as the term of any patent granted on said **reference** application may be shortened by any terminal disclaimer filed prior to the grant of any patent on the pending **reference** application. The owner hereby agrees that any patent so granted on the instant application shall be enforceable only for and during such period that it and any patent granted on the **reference** application are commonly owned. This agreement runs with any patent granted on the instant application and is binding upon the grantee, its successors or assigns.

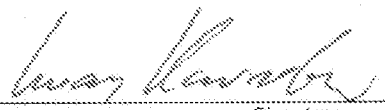
In making the above disclaimer, the owner does not disclaim the terminal part of any patent granted on the instant application that would extend to the expiration date of the full statutory term as defined in 35 U.S.C. 154 and 173 of any patent granted on said **reference** application, "as the term of any patent granted on said **reference** application may be shortened by any terminal disclaimer filed prior to the grant of any patent on the pending **reference** application," in the event that: any such patent granted on the pending **reference** application: expires for failure to pay a maintenance fee, is held unenforceable, is found invalid by a court of competent jurisdiction, is statutorily disclaimed in whole or terminally disclaimed under 37 CFR 1.321, has all claims canceled by a reexamination certificate, is reissued, or is in any manner terminated prior to the expiration of its full statutory term as shortened by any terminal disclaimer filed prior to its grant.

Check either box 1 or 2 below, if appropriate.

1. ☐ For submissions on behalf of a business/organization (e.g., corporation, partnership, university, government agency, etc.), the undersigned is empowered to act on behalf of the business/organization.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

2. ☑ The undersigned is an attorney or agent of record. Reg. No. 25,161



Signature — October 5, 2016 (Date)

Ivan S. Kavrukov
Typed or printed name

212-278-0432
Telephone Number

☑ Terminal disclaimer fee under 37 CFR 1.20(d) is included.

WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.

*Statement under 37 CFR 3.73(b) is required if terminal disclaimer is signed by the assignee (owner).
Form PTO/SB/96 may be used for making this statement. See MPEP § 324.

This collection of information is required by 37 CFR 1.321. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce. P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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Electronic Patent Application Fee Transmittal

Application Number:	14945003
Filing Date:	18-Nov-2015
Title of Invention:	MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES
First Named Inventor/Applicant Name:	Shih-Yuan WANG
Filer:	Ivan Kavrukov/Benjamin Han
Attorney Docket Number:	5176-88184-2

Filed as Small Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Miscellaneous:				
STATUTORY OR TERMINAL DISCLAIMER	2814	1	160	160
		Total in USD ($)		**160**

Electronic Acknowledgement Receipt

EFS ID:	27137527
Application Number:	14945003
International Application Number:	
Confirmation Number:	1200
Title of Invention:	MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES
First Named Inventor/Applicant Name:	Shih-Yuan WANG
Customer Number:	23432
Filer:	Ivan Kavrukov/Benjamin Han
Filer Authorized By:	Ivan Kavrukov
Attorney Docket Number:	5176-88184-2
Receipt Date:	06-OCT-2016
Filing Date:	18-NOV-2015
Time Stamp:	10:29:11
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	$160
RAM confirmation Number	10649
Deposit Account	033125
Authorized User	Finnegan, Mary Ellen

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

Charge any Additional Fees required under 37 CFR 1.16 (National application filing, search, and examination fees)

Charge any Additional Fees required under 37 CFR 1.17 (Patent application and reexamination processing fees)

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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Terminal Disclaimer Filed	5176_88184_2.pdf	775300 1dace5de461693b88ad2115e3e6b2f5b46d70e28	no	1
Warnings:					
Information:					
2	Fee Worksheet (SB06)	fee-info.pdf	30672 20d9056da72ff6112687c19f15701508cdd63b57	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	805972		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PTO/AIA/01 (06-12)
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DECLARATION (37 CFR 1.63) FOR UTILITY OR DESIGN APPLICATION USING AN APPLICATION DATA SHEET (37 CFR 1.76)

Dkt: 5176/88184-2

Title of Invention	MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES

As the below named inventor, I hereby declare that:

This declaration is directed to:

- ☐ The attached application, or
- ☑ United States application or PCT international application number 14/945,003 filed on November 18, 2015.

The above-identified application was made or authorized to be made by me.

I believe that I am the original inventor or an original joint inventor of a claimed invention in the application.

I hereby acknowledge that any willful false statement made in this declaration is punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both.

WARNING:

Petitioner/applicant is cautioned to avoid submitting personal information in documents filed in a patent application that may contribute to identity theft. Personal information such as social security numbers, bank account numbers, or credit card numbers (other than a check or credit card authorization form PTO-2038 submitted for payment purposes) is never required by the USPTO to support a petition or an application. If this type of personal information is included in documents submitted to the USPTO, petitioners/applicants should consider redacting such personal information from the documents before submitting them to the USPTO. Petitioner/applicant is advised that the record of a patent application is available to the public after publication of the application (unless a non-publication request in compliance with 37 CFR 1.213(a) is made in the application) or issuance of a patent. Furthermore, the record from an abandoned application may also be available to the public if the application is referenced in a published application or an issued patent (see 37 CFR 1.14). Checks and credit card authorization forms PTO-2038 submitted for payment purposes are not retained in the application file and therefore are not publicly available.

LEGAL NAME OF INVENTOR

Inventor: Shih-Ping WANG Date (Optional): _____

Signature: _____

Note: An application data sheet (PTO/AIA/14 or equivalent), including naming the entire inventive entity, must accompany this form. Use an additional PTO/SB/AIA/01 form for each additional inventor.

This collection of information is required by 35 U.S.C. 115 and 37 CFR 1.63. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 1 minute to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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Corrected ADS

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	~~2901-88184-2~~ 5176-88184.2
	Application Number	

Title of Invention	MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES

The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76.
This document may be completed electronically and submitted to the Office in electronic format using the Electronic Filing System (EFS) or the document may be printed and included in a paper filed application.

Secrecy Order 37 CFR 5.2

☐ Portions or all of the application associated with this Application Data Sheet may fall under a Secrecy Order pursuant to 37 CFR 5.2 (Paper filers only. Applications that fall under Secrecy Order may not be filed electronically.)

Inventor Information:

Inventor 1 Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Shih-Yuan		WANG	

Residence Information (Select One) ◉ US Residency ○ Non US Residency ○ Active US Military Service

City	Palo Alto	State/Province	CA	Country of Residence	US

Mailing Address of Inventor:

Address 1	766 Encina Grande Dr.		
Address 2			
City	Palo Alto	State/Province	CA
Postal Code	94306	Country	US

Inventor 2 Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Shih-Ping		WANG	

Residence Information (Select One) ◉ US Residency ○ Non US Residency ○ Active US Military Service

City	Los Altos	State/Province	CA	Country of Residence	US

Mailing Address of Inventor:

Address 1	38 3rd Street, Suite #307		
Address 2			
City	Los Altos	State/Province	CA
Postal Code	94022	Country	US

All Inventors Must Be Listed - Additional Inventor Information blocks may be generated within this form by selecting the **Add** button. Add

Correspondence Information:

Enter either Customer Number or complete the Correspondence Information section below.
For further information see 37 CFR 1.33(a).

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	~~2901-88184-2~~ 5176-88184-2
	Application Number	
Title of Invention	MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES	

☐ **An Address is being provided for the correspondence Information of this application.**

Customer Number	23432		
Email Address	patentdocketing@cooperdunham.com	Add Email	Remove Email
Email Address	ikavrukov@cooperdunham.com	Add Email	Remove Email

Application Information:

Title of the Invention	MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES		
Attorney Docket Number	2901-88184-2	**Small Entity Status Claimed**	☒
Application Type	Nonprovisional		
Subject Matter	Utility		
Total Number of Drawing Sheets (if any)	86	**Suggested Figure for Publication (if any)**	

Filing By Reference :

Only complete this section when filing an application by reference under 35 U.S.C. 111(c) and 37 CFR 1.57(a). Do not complete this section if application papers including a specification and any drawings are being filed. Any domestic benefit or foreign priority information must be provided in the appropriate section(s) below (i.e., "Domestic Benefit/National Stage Information" and "Foreign Priority Information").

For the purposes of a filing date under 37 CFR 1.53(b), the description and any drawings of the present application are replaced by this reference to the previously filed application, subject to conditions and requirements of 37 CFR 1.57(a).

Application number of the previously filed application	Filing date (YYYY-MM-DD)	Intellectual Property Authority or Country

Publication Information:

☐ Request Early Publication (Fee required at time of Request 37 CFR 1.219)

☐ **Request Not to Publish.** I hereby request that the attached application not be published under 35 U.S.C. 122(b) and certify that the invention disclosed in the attached application **has not and will not** be the subject of an application filed in another country, or under a multilateral international agreement, that requires publication at eighteen months after filing.

Representative Information:

Representative information should be provided for all practitioners having a power of attorney in the application. Providing this information in the Application Data Sheet does not constitute a power of attorney in the application (see 37 CFR 1.32). Either enter Customer Number or complete the Representative Name section below. If both sections are completed the customer Number will be used for the Representative Information during processing.

Please Select One:	◉ Customer Number	○ US Patent Practitioner	○ Limited Recognition (37 CFR 11.9)
Customer Number	23432		

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	~~2901-88184-2~~ 5176-88184-2
	Application Number	
Title of Invention	MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES	

Domestic Benefit/National Stage Information:

This section allows for the applicant to either claim benefit under 35 U.S.C. 119(e), 120, 121, 365(c), or 386(c) or indicate National Stage entry from a PCT application. Providing this information in the application data sheet constitutes the specific reference required by 35 U.S.C. 119(e) or 120, and 37 CFR 1.78.
When referring to the current application, please leave the application number blank.

Prior Application Status	Pending		Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)
	Claims benefit of provisional	62/232716	2015-09-25
Prior Application Status	Pending		Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)
	Claims benefit of provisional	62/213556	2015-09-02
Prior Application Status	Pending		Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)
	Claims benefit of provisional	62/209311	2015-08-24
Prior Application Status	Pending		Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)
	Claims benefit of provisional	62/205717	2015-08-15
Prior Application Status	Pending		Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)
	Claims benefit of provisional	62/199607	2015-07-31
Prior Application Status	Pending		Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)
	Claims benefit of provisional	62/197120	2015-07-27
Prior Application Status	Pending		Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)
	Claims benefit of provisional	62/188876	2015-07-06
Prior Application Status	Pending		Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)
	Claims benefit of provisional	62/182602	2015-06-21
Prior Application Status	Pending		Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)
	Claims benefit of provisional	62/175855	2015-06-15
Prior Application Status	Pending		Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)
	Claims benefit of provisional	62/174498	2015-06-11

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	~~2001-88184-2~~ 5175-88184-2
	Application Number	
Title of Invention	MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES	

Prior Application Status	Pending		Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)
	Claims benefit of provisional	62/171915	2015-06-05
Prior Application Status	Pending		Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)
	Claims benefit of provisional	62/157876	2015-05-06
Prior Application Status	Pending		Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)
	Claims benefit of provisional	62/154675	2015-04-29
Prior Application Status	Pending		Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)
	Claims benefit of provisional	62/153443	2015-04-27
Prior Application Status	Pending		Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)
	Claims benefit of provisional	62/139511	2015-03-27
Prior Application Status	Pending		Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)
	Claims benefit of provisional	62/111582	2015-02-03
Prior Application Status	Pending		Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)
	Claims benefit of provisional	62/100025	2015-01-05
Prior Application Status	Pending		Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)
	Claims benefit of provisional	62/090879	2014-12-11
Prior Application Status	Pending		Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)
	Claims benefit of provisional	62/081538	2014-11-18

Additional Domestic Benefit/National Stage Data may be generated within this form by selecting the **Add** button.

Foreign Priority Information:

This section allows for the applicant to claim priority to a foreign application. Providing this information in the application data sheet constitutes the claim for priority as required by 35 U.S.C. 119(b) and 37 CFR 1.55. When priority is claimed to a foreign application that is eligible for retrieval under the priority document exchange program (PDX)[i] the information will be used by the Office to automatically attempt retrieval pursuant to 37 CFR 1.55(i)(1) and (2). Under the PDX program, applicant bears the ultimate responsibility for ensuring that a copy of the foreign application is received by the Office from the participating foreign intellectual property office, or a certified copy of the foreign priority application is filed, within the time period specified in 37 CFR 1.55(g)(1).

PTO/AIA/14 (07-14)
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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	~~2501-88184-2~~ 5176-88184-2
	Application Number	
Title of Invention	MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES	

Remove

Application Number	Country[i]	Filing Date (YYYY-MM-DD)	Access Code[j] (if applicable)

Additional Foreign Priority Data may be generated within this form by selecting the **Add** button.

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications

☐ This application (1) claims priority to or the benefit of an application filed before March 16, 2013 and (2) also contains, or contained at any time, a claim to a claimed invention that has an effective filing date on or after March 16, 2013.
NOTE: By providing this statement under 37 CFR 1.55 or 1.78, this application, with a filing date on or after March 16, 2013, will be examined under the first inventor to file provisions of the AIA.

Authorization to Permit Access:

☐ Authorization to Permit Access to the Instant Application by the Participating Offices

If checked, the undersigned hereby grants the USPTO authority to provide the European Patent Office (EPO), the Japan Patent Office (JPO), the Korean Intellectual Property Office (KIPO), the World Intellectual Property Office (WIPO), and any other intellectual property offices in which a foreign application claiming priority to the instant patent application is filed access to the instant patent application. See 37 CFR 1.14(c) and (h). This box should not be checked if the applicant does not wish the EPO, JPO, KIPO, WIPO, or other intellectual property office in which a foreign application claiming priority to the instant patent application is filed to have access to the instant patent application.

In accordance with 37 CFR 1.14(h)(3), access will be provided to a copy of the instant patent application with respect to: 1) the instant patent application-as-filed; 2) any foreign application to which the instant patent application claims priority under 35 U.S.C. 119(a)-(d) if a copy of the foreign application that satisfies the certified copy requirement of 37 CFR 1.55 has been filed in the instant patent application; and 3) any U.S. application-as-filed from which benefit is sought in the instant patent application.

In accordance with 37 CFR 1.14(c), access may be provided to information concerning the date o f filing this Authorization.

Applicant Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

PTO/AIA/14 (07-14)
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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	~~2901-88184-2~~ 5176-88184-2
	Application Number	
Title of Invention	MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES	

Applicant 1

If the applicant is the inventor (or the remaining joint inventor or inventors under 37 CFR 1.45), this section should not be completed. The information to be provided in this section is the name and address of the legal representative who is the applicant under 37 CFR 1.43; or the name and address of the assignee, person to whom the inventor is under an obligation to assign the invention, or person who otherwise shows sufficient proprietary interest in the matter who is the applicant under 37 CFR 1.46. If the applicant is an applicant under 37 CFR 1.46 (assignee, person to whom the inventor is obligated to assign, or person who otherwise shows sufficient proprietary interest) together with one or more joint inventors, then the joint inventor or inventors who are also the applicant should be identified in this section.

Clear

☒ Assignee	◯ Legal Representative under 35 U.S.C. 117	◯ Joint Inventor
◯ Person to whom the inventor is obligated to assign.	◯ Person who shows sufficient proprietary interest	

If applicant is the legal representative, indicate the authority to file the patent application, the inventor is:

Name of the Deceased or Legally Incapacitated Inventor :

If the Applicant is an Organization check here. x W&Wsens, Devices Inc.

Prefix	Given Name	Middle Name	Family Name	Suffix

Mailing Address Information For Applicant:

Address 1	W&Wsens, Devices Inc.		
Address 2	4546 El Camino Real, Suite 215		
City	Los Altos	**State/Province**	CA
Country US		Postal Code	94022
Phone Number		Fax Number	
Email Address			

Additional Applicant Data may be generated within this form by selecting the Add button.

Assignee Information including Non-Applicant Assignee Information:

Providing assignment information in this section does not subsitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

Assignee 1

Complete this section if assignee information, including non-applicant assignee information, is desired to be included on the patent application publication . An assignee-applicant identified in the "Applicant Information" section will appear on the patent application publication as an applicant. For an assignee-applicant, complete this section only if identification as an assignee is also desired on the patent application publication.

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	~~2901-88184-2~~ 5176-88184-2
	Application Number	
Title of Invention	MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES	

If the Assignee or Non-Applicant Assignee is an Organization check here. ☐

Prefix	**Given Name**	Middle Name	**Family Name**	Suffix

Mailing Address Information For Assignee including Non-Applicant Assignee:

Address 1			
Address 2			
City		**State/Province**	
Country i		Postal Code	
Phone Number		Fax Number	
Email Address			

Additional Assignee or Non-Applicant Assignee Data may be generated within this form by selecting the Add button.

Signature:

NOTE: This form must be signed in accordance with 37 CFR 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Signature	/Ivan S. Kavrukov/			Date (YYYY-MM-DD)	2016-10-5 ~~2015-11-18~~
First Name	Ivan	Last Name	Kavrukov	Registration Number	25161

Additional Signature may be generated within this form by selecting the Add button.

This collection of information is required by 37 CFR 1.76. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 23 minutes to complete, including gathering, preparing, and submitting the completed application data sheet form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

PTO/AIA/96 (08-12)
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STATEMENT UNDER 37 CFR 3.73(c)

Applicant/Patent Owner: W&Wsens Devices, Inc.

Application No./Patent No.: 14/946,003 Filed/Issue Date: November 18, 2015

Titled: MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES

W&Wsens Devices, Inc., a Corporation

(Name of Assignee) (Type of Assignee, e.g., corporation, partnership, university, government agency, etc.)

states that, for the patent application/patent identified above, it is (choose one of options 1, 2, 3 or 4 below):

1. ☑ The assignee of the entire right, title, and interest.

2. ☐ An assignee of less than the entire right, title, and interest (check applicable box):

   ☐ The extent (by percentage) of its ownership interest is _____%. Additional Statement(s) by the owners holding the balance of the interest must be submitted to account for 100% of the ownership interest.

   ☐ There are unspecified percentages of ownership. The other parties, including inventors, who together own the entire right, title and interest are:

   Additional Statement(s) by the owner(s) holding the balance of the interest must be submitted to account for the entire right, title, and interest.

3. ☐ The assignee of an undivided interest in the entirety (a complete assignment from one of the joint inventors was made). The other parties, including inventors, who together own the entire right, title, and interest are:

   Additional Statement(s) by the owner(s) holding the balance of the interest must be submitted to account for the entire right, title, and interest.

4. ☐ The recipient, via a court proceeding or the like (*e.g.*, bankruptcy, probate), of an undivided interest in the entirety (a complete transfer of ownership interest was made). The certified document(s) showing the transfer is attached.

The interest identified in option 1, 2 or 3 above (not option 4) is evidenced by either (choose one of options A or B below):

A. ☑ An assignment from the inventor(s) of the patent application/patent identified above. The assignment was recorded in the United States Patent and Trademark Office at Reel _____, Frame _____, or for which a copy thereof is attached.

B. ☐ A chain of title from the inventor(s), of the patent application/patent identified above, to the current assignee as follows:

1. From: _____ To: _____

   The document was recorded in the United States Patent and Trademark Office at

   Reel _____, Frame _____, or for which a copy thereof is attached.

2. From: _____ To: _____

   The document was recorded in the United States Patent and Trademark Office at

   Reel _____, Frame _____, or for which a copy thereof is attached.

This collection of information is required by 37 CFR 3.73(b). The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

PTO/AIA/96 (08-12)
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STATEMENT UNDER 37 CFR 3.73(c)

3. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at

Reel _____, Frame _____, or for which a copy thereof is attached.

4. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at

Reel _____, Frame _____, or for which a copy thereof is attached.

5. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at

Reel _____, Frame _____, or for which a copy thereof is attached.

6. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at

Reel _____, Frame _____, or for which a copy thereof is attached.

☐ Additional documents in the chain of title are listed on a supplemental sheet(s).

☐ As required by 37 CFR 3.73(c)(1)(i), the documentary evidence of the chain of title from the original owner to the assignee was, or concurrently is being, submitted for recordation pursuant to 37 CFR 3.11.

[NOTE: A separate copy (i.e., a true copy of the original assignment document(s)) must be submitted to Assignment Division in accordance with 37 CFR Part 3, to record the assignment in the records of the USPTO. See MPEP 302.08]

The undersigned (whose title is supplied below) is authorized to act on behalf of the assignee.

/Ivan Kavrukov/	October 5, 2016
Signature	Date
Ivan Kavrukov	25,161
Printed or Typed Name	Title or Registration Number

ASSIGNMENT

In consideration of One Dollar ($1.00), and other good and valuable considerations, the receipt of which is hereby acknowledged, I, the undersigned,

Shih-Yuan Wang and Shih-Ping Wang

Hereby sell, assign and transfer to W&Wsens Devices, Inc., a corporation of Delaware, having a place of business at 38 Third Street, Suite 307, Los Altos, California, its successors, assigns and legal representatives, the entire right, title and interest for all countries, in and to any and all inventions which are disclosed and claimed, and as possessed by the undersigned, any and all inventions which are disclosed but not claimed, in the patent applications identified in the attached Schedule A, and in and to said applications and all divisional, continuing, substitute, renewal, reissue, and all other applications for U.S. Letters Patent or other related property rights in any and all foreign countries which have been or shall be filed on any of said inventions disclosed in said applications; and in and to all original and reissued patents or related foreign documents which have been or shall be issued on said inventions.

Authorize and request the Commissioner of Patents of the United States and non-U.S. Patent Authorities to issue to said Assignee, the corporation above named, its successors, assigns and legal representatives, in accordance with this assignment, any and all United States Letters Patent and non-U.S. Patents on said inventions or any of them disclosed in said applications;

Agree that said Assignee may apply for and receive foreign Letters Patent or rights of any other kind for said inventions, or any of them; and may claim, in applications for said foreign Letters Patent or other rights, the priority of the aforesaid United States patent application under the provisions of the International Convention of 1883 and later modifications thereof, under the Patent Cooperation Treaty, under the European Patent Convention or under any other available international agreement; and that, when requested, without charge to, but at the expense of, said Assignee, its successors, assigns and legal representatives, to carry out in good faith the intent and purpose of this assignment, the undersigned or the undersigned's executors or administrators will, for the United States and all foreign countries, execute all divisional, continuing, substitute, renewal, reissue, and all other patent applications or other documents on any and all said inventions; execute all

rightful oaths, assignments, powers of attorney and other papers; communicate to said Assignee, its successors, assigns and representatives, all facts known and documents available to the undersigned relating to said inventions and the history thereof; testify in all legal proceedings; and generally do everything possible which said Assignee, its successors, assigns or representatives shall consider desirable for aiding in securing, maintaining and enforcing proper patent protection for said inventions and for vesting title to said inventions and all applications for patents or related foreign rights and all patents on said inventions, in said Assignee, its successors, assigns and legal representatives; and

COVENANT with said Assignee, its successors, assigns and legal representatives that no assignment, grant, mortgage, license or other agreement affecting the rights and property herein conveyed has been made to others by the undersigned, and that full right to convey the same as herein expressed is possessed by the undersigned.

Shih-Yuan Wang (L.S.)
Shih-Yuan Wang
Date: 9-16-2016
Witness:
TERESA SPENCER

(L.S.)
Shih-Ping Wang
Date: 9-16-2016
Witness:
TERESA SPENCER

SCHEDULE A

	APPLICATION/PATENT NO.	COUNTRY	FILING/ISSUE/PUBLICATION DATE
1.	61/826,446	U.S.	May 5, 2013
2.	61/834,873	U.S.	June 13, 2013
3.	61/843,021	U.S.	July 4, 2013
4.	61/905,109	U.S.	November 15, 2013
5.	62/021,538	U.S.	November 18, 2014
6.	62/090,879	U.S.	December 11, 2014
7.	62/100,025	U.S.	January 5, 2015
8.	62/011,582	U.S.	February 3, 2015
9.	62/139,511	U.S.	March 27, 2015
10.	62/153,443	U.S.	April 27, 2015
11.	62/154,675	U.S.	April 29, 2015
12.	62/157,876	U.S.	May 6, 2015
13.	62/171,915	U.S.	June 5, 2015
14.	62/174,498	U.S.	June 11, 2015
15.	62/175,855	U.S.	June 15, 2015
16.	62/182,602	U.S.	June 21, 2015
17.	62/188,876	U.S.	July 6, 2015
18.	62/197,120	U.S.	July 27, 2015
19.	61/199,607	U.S.	July 31, 2015
20.	62/205,717	U.S.	August 15, 2015
21.	62/209,311	U.S.	August 24, 2015
22.	62/213,556	U.S.	September 2, 2015
23.	62/232,716	U.S.	September 25, 2015
24.	PCT/US14/039208	PCT	May 22, 2014
25.	14/892,821	U.S.	November 20, 2015
26.	14/947,718	U.S.	November 20, 2015
27.	PCT/US15/061120	U.S.	November 17, 2015
28.	14/943,898	U.S.	November 17, 2015
29.	14/945,003	U.S.	November 18, 2015

PTO/AIA/01 (06-12)
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DECLARATION (37 CFR 1.63) FOR UTILITY OR DESIGN APPLICATION USING AN APPLICATION DATA SHEET (37 CFR 1.76)

Dkt: 5176/88184-2

Title of Invention	MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES

As the below named inventor, I hereby declare that:

This declaration is directed to:

- ☐ The attached application, or
- ☑ United States application or PCT international application number 14/945,003 filed on November 18, 2015

The above-identified application was made or authorized to be made by me.

I believe that I am the original inventor or an original joint inventor of a claimed invention in the application.

I hereby acknowledge that any willful false statement made in this declaration is punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both.

WARNING:

Petitioner/applicant is cautioned to avoid submitting personal information in documents filed in a patent application that may contribute to identity theft. Personal information such as social security numbers, bank account numbers, or credit card numbers (other than a check or credit card authorization form PTO-2038 submitted for payment purposes) is never required by the USPTO to support a petition or an application. If this type of personal information is included in documents submitted to the USPTO, petitioners/applicants should consider redacting such personal information from the documents before submitting them to the USPTO. Petitioner/applicant is advised that the record of a patent application is available to the public after publication of the application (unless a non-publication request in compliance with 37 CFR 1.213(a) is made in the application) or issuance of a patent. Furthermore, the record from an abandoned application may also be available to the public if the application is referenced in a published application or an issued patent (see 37 CFR 1.14). Checks and credit card authorization forms PTO-2038 submitted for payment purposes are not retained in the application file and therefore are not publicly available.

LEGAL NAME OF INVENTOR

Inventor: Shih-Yuan WANG Date (Optional):

Signature: Shih-Yuan Wang

Note: An application data sheet (PTO/AIA/14 or equivalent), including naming the entire inventive entity, must accompany this form. Use an additional PTO/SB/AIA01 form for each additional inventor.

This collection of information is required by 35 U.S.C. 115 and 37 CFR 1.63. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 1 minute to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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Electronic Acknowledgement Receipt

EFS ID:	27133744
Application Number:	14945003
International Application Number:	
Confirmation Number:	1200
Title of Invention:	MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES
First Named Inventor/Applicant Name:	Shih-Yuan WANG
Customer Number:	23432
Filer:	Ivan Kavrukov/Maria Arap
Filer Authorized By:	Ivan Kavrukov
Attorney Docket Number:	5176-88184-2
Receipt Date:	05-OCT-2016
Filing Date:	18-NOV-2015
Time Stamp:	17:30:44
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Application Data Sheet	88184-2_ADS_CORRECTED-.pdf	10745011 e1e4405505e0b5fc9dc07659e4d1ef05b10bd514	no	7

Warnings:

Information:					
This is not an USPTO supplied ADS fillable form					
2	Oath or Declaration filed	Decl_SY-Wang.pdf	354006 61f909ece253d804f6ad76657a15aac995f2b10c	no	1
Warnings:					
Information:					
3	Oath or Declaration filed	Decl__SP-Wang.pdf	362460 c76160bce4503829a0ea1c79a7dd2858101c1f4b	no	1
Warnings:					
Information:					
4	Power of Attorney	POA_SP-Wang.pdf	441626 b32f1c6840391934c526fc129704ee536c795c82	no	1
Warnings:					
Information:					
5	Assignee showing of ownership per 37 CFR 3.73	373Statement_Assign.pdf	973441 da4c73a8c77eb02dbbc4c547ccaebb38b0804d4d	no	5
Warnings:					
Information:					
		Total Files Size (in bytes):	12876544		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Doc Code: PA..
Document Description: Power of Attorney

PTO/AIA/82B (07-13)
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POWER OF ATTORNEY BY APPLICANT

I hereby revoke all previous powers of attorney given in the application identified in either the attached transmittal letter or the boxes below.

Application Number	Filing Date
14/945,003	November 18, 2015

(Note: The boxes above may be left blank if information is provided on form PTO/AIA/82A.)

☑ I hereby appoint the Patent Practitioner(s) associated with the following Customer Number as my/our attorney(s) or agent(s), and to transact all business in the United States Patent and Trademark Office connected therewith for the application referenced in the attached transmittal letter (form PTO/AIA/82A) or identified above: 23432

OR

☐ I hereby appoint Practitioner(s) named in the attached list (form PTO/AIA/82C) as my/our attorney(s) or agent(s), and to transact all business in the United States Patent and Trademark Office connected therewith for the patent application referenced in the attached transmittal letter (form PTO/AIA/82A) or identified above. (Note: Complete form PTO/AIA/82C.)

Please recognize or change the correspondence address for the application identified in the attached transmittal letter or the boxes above to:

☐ The address associated with the above-mentioned Customer Number

OR

☐ The address associated with Customer Number:

OR

Firm or Individual Name					
Address					
City		State		Zip	
Country					
Telephone		Email			

I am the Applicant (if the Applicant is a juristic entity, list the Applicant name in the box):

W&Wsens Devices, Inc.

☐ Inventor or Joint Inventor (title not required below)

☐ Legal Representative of a Deceased or Legally Incapacitated Inventor (title not required below)

☑ Assignee or Person to Whom the Inventor is Under an Obligation to Assign (provide signer's title if applicant is a juristic entity)

☐ Person Who Otherwise Shows Sufficient Proprietary Interest (e.g., a petition under 37 CFR 1.46(b)(2) was granted in the application or is concurrently being filed with this document) (provide signer's title if applicant is a juristic entity)

SIGNATURE of Applicant for Patent

The undersigned (whose title is supplied below) is authorized to act on behalf of the applicant (e.g., where the applicant is a juristic entity).

Signature		Date (Optional)	
Name	Shih-Ping WANG		
Title	President and CEO		

NOTE: Signature - This form must be signed by the applicant in accordance with 37 CFR 1.33. See 37 CFR 1.4 for signature requirements and certifications. If more than one applicant, use multiple forms.

☐ Total of forms are submitted.

This collection of information is required by 37 CFR 1.131, 1.32, and 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/945,003	11/18/2015	Shih-Yuan WANG	5176-88184-2	1200

23432 7590 09/30/2016

COOPER & DUNHAM, LLP
30 Rockefeller Plaza
20th Floor
NEW YORK, NY 10112

EXAMINER
RODELA, EDUARDO A

ART UNIT	PAPER NUMBER
2893	

MAIL DATE	DELIVERY MODE
09/30/2016	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Applicant-Initiated Interview Summary	Application No.	Applicant(s)	
	14/945,003	WANG ET AL.	
	Examiner	Art Unit	
	Eduardo A. Rodela	2893	

All participants (applicant, applicant's representative, PTO personnel):

(1) *Eduardo A. Rodela, Examiner*. (3)_____.

(2) *Ivan Kavrukov, Appilcant's Representative*. (4)_____.

Date of Interview: *9/28/2016*.

Type: ☒ Telephonic ☐ Video Conference
☐ Personal [copy given to: ☐ applicant ☐ applicant's representative]

Exhibit shown or demonstration conducted: ☐ Yes ☒ No.
If Yes, brief description: _____.

Issues Discussed ☐101 ☐112 ☐102 ☐103 ☒Others
(For each of the checked box(es) above, please describe below the issue and detailed description of the discussion)

Claim(s) discussed: *1*.

Identification of prior art discussed: *copending application 14/943,898, US 2003/0127608, US 8604511*.

Substance of Interview
(For each issue discussed, provide a detailed description and indicate if agreement was reached. Some topics may include: identification or clarification of a reference or a portion thereof, claim interpretation, proposed amendments, arguments of any applied references etc...)

As per timeliness requirements, Examiner previously agreed to conduct a prior art search in preparation for discussion of the claims in today's interview. Several prior art were discovered that would aid in potentially crafting claim language that would lead to furthering prosecution. However, it was pointed out that the allowed copending application 14/943,898 would require a terminal disclaimer. Applicant's Representative indicated that he would consult Applicant's and return to communications once a decision was reached as to how to proceed.

Applicant recordation instructions: The formal written reply to the last Office action must include the substance of the interview. (See MPEP section 713.04). If a reply to the last Office action has already been filed, applicant is given a non-extendable period of the longer of one month or thirty days from this interview date, or the mailing date of this interview summary form, whichever is later, to file a statement of the substance of the interview

Examiner recordation instructions: Examiners must summarize the substance of any interview of record. A complete and proper recordation of the substance of an interview should include the items listed in MPEP 713.04 for complete and proper recordation including the identification of the general thrust of each argument or issue discussed, a general indication of any other pertinent matters discussed regarding patentability and the general results or outcome of the interview, to include an indication as to whether or not agreement was reached on the issues raised.

☐ Attachment

/Eduardo A. Rodela/ Primary Examiner, Art Unit 2893	

Summary of Record of Interview Requirements

Manual of Patent Examining Procedure (MPEP), Section 713.04, Substance of Interview Must be Made of Record
A complete written statement as to the substance of any face-to-face, video conference, or telephone interview with regard to an application must be made of record in the application whether or not an agreement with the examiner was reached at the interview.

Title 37 Code of Federal Regulations (CFR) § 1.133 Interviews
Paragraph (b)

In every instance where reconsideration is requested in view of an interview with an examiner, a complete written statement of the reasons presented at the interview as warranting favorable action must be filed by the applicant. An interview does not remove the necessity for reply to Office action as specified in §§ 1.111, 1.135. (35 U.S.C. 132)

37 CFR §1.2 Business to be transacted in writing.
All business with the Patent or Trademark Office should be transacted in writing. The personal attendance of applicants or their attorneys or agents at the Patent and Trademark Office is unnecessary. The action of the Patent and Trademark Office will be based exclusively on the written record in the Office. No attention will be paid to any alleged oral promise, stipulation, or understanding in relation to which there is disagreement or doubt.

———

The action of the Patent and Trademark Office cannot be based exclusively on the written record in the Office if that record is itself incomplete through the failure to record the substance of interviews.

It is the responsibility of the applicant or the attorney or agent to make the substance of an interview of record in the application file, unless the examiner indicates he or she will do so. It is the examiner's responsibility to see that such a record is made and to correct material inaccuracies which bear directly on the question of patentability.

Examiners must complete an Interview Summary Form for each interview held where a matter of substance has been discussed during the interview by checking the appropriate boxes and filling in the blanks. Discussions regarding only procedural matters, directed solely to restriction requirements for which interview recordation is otherwise provided for in Section 812.01 of the Manual of Patent Examining Procedure, or pointing out typographical errors or unreadable script in Office actions or the like, are excluded from the interview recordation procedures below. Where the substance of an interview is completely recorded in an Examiners Amendment, no separate Interview Summary Record is required.

The Interview Summary Form shall be given an appropriate Paper No., placed in the right hand portion of the file, and listed on the "Contents" section of the file wrapper. In a personal interview, a duplicate of the Form is given to the applicant (or attorney or agent) at the conclusion of the interview. In the case of a telephone or video-conference interview, the copy is mailed to the applicant's correspondence address either with or prior to the next official communication. If additional correspondence from the examiner is not likely before an allowance or if other circumstances dictate, the Form should be mailed promptly after the interview rather than with the next official communication.

The Form provides for recordation of the following information:
- Application Number (Series Code and Serial Number)
- Name of applicant
- Name of examiner
- Date of interview
- Type of interview (telephonic, video-conference, or personal)
- Name of participant(s) (applicant, attorney or agent, examiner, other PTO personnel, etc.)
- An indication whether or not an exhibit was shown or a demonstration conducted
- An identification of the specific prior art discussed
- An indication whether an agreement was reached and if so, a description of the general nature of the agreement (may be by attachment of a copy of amendments or claims agreed as being allowable). Note: Agreement as to allowability is tentative and does not restrict further action by the examiner to the contrary.
- The signature of the examiner who conducted the interview (if Form is not an attachment to a signed Office action)

It is desirable that the examiner orally remind the applicant of his or her obligation to record the substance of the interview of each case. It should be noted, however, that the Interview Summary Form will not normally be considered a complete and proper recordation of the interview unless it includes, or is supplemented by the applicant or the examiner to include, all of the applicable items required below concerning the substance of the interview.

A complete and proper recordation of the substance of any interview should include at least the following applicable items:
1) A brief description of the nature of any exhibit shown or any demonstration conducted,
2) an identification of the claims discussed,
3) an identification of the specific prior art discussed,
4) an identification of the principal proposed amendments of a substantive nature discussed, unless these are already described on the Interview Summary Form completed by the Examiner,
5) a brief identification of the general thrust of the principal arguments presented to the examiner,
   (The identification of arguments need not be lengthy or elaborate. A verbatim or highly detailed description of the arguments is not required. The identification of the arguments is sufficient if the general nature or thrust of the principal arguments made to the examiner can be understood in the context of the application file. Of course, the applicant may desire to emphasize and fully describe those arguments which he or she feels were or might be persuasive to the examiner.)
6) a general indication of any other pertinent matters discussed, and
7) if appropriate, the general results or outcome of the interview unless already described in the Interview Summary Form completed by the examiner.

Examiners are expected to carefully review the applicant's record of the substance of an interview. If the record is not complete and accurate, the examiner will give the applicant an extendable one month time period to correct the record.

Examiner to Check for Accuracy

If the claims are allowable for other reasons of record, the examiner should send a letter setting forth the examiner's version of the statement attributed to him or her. If the record is complete and accurate, the examiner should place the indication, "Interview Record OK" on the paper recording the substance of the interview along with the date and the examiner's initials.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application of: Shih-Yuan WANG

Application No.: 14/945,003

Date Filed: November 18, 2015

For: MICROSTRUCTURE ENHANCED ABSORPTIO00N PHOTOSENSITIVE DEVICES

Conf. No.: 1200

This correspondence is being filed electronically with the U.S. Patent and Trademark Office via EFS-Web.

/erin finnegan/ September 29, 2016
Erin Finnegan

30 Rockefeller Plaza, 20th Floor
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Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

:

FOURTH PRELIMINARY AMENDMENT

Prior to examination of the above-identified patent application, please enter this Amendment.

Amendments to the claims are reflected in the **Listing of Claims** section which begins on page 2.

Remarks begin on page 10 of this paper.

Listing of Claims

The following listing of claims will replace all prior versions, and listings, of claims in the subject application:

1. (Currently Amended) An integrated detector/processor circuit for data communication comprising both a photodetector with microstructure-enhanced photoabsorption and an electronic processor formed into a single semiconductor chip, comprising:

a photodetector formed on a semiconductor substrate and comprising a photon absorbing region configured to absorb photons from an optical source signal modulated for data communication and provide an output electrical signal corresponding thereto;

said photon absorbing region comprising an I-region that is between an N-region and a P-region and comprises a plurality of holes ~~therein~~ extending in said I-region toward said substrate and configured to concurrently receive the same source signal at a plural number of the holes;

an electronic processor also formed on said semiconductor substrate and operatively associated with said photon absorbing region to receive therefrom and process said output electrical signal into a processed output, thereby forming a single semiconductor chip that receives the optical source signal and outputs the processed output;

wherein said photon absorbing region and said electronic processor have respective thicknesses that are of the same order of magnitude; and

a cathode region and an anode region operatively associated with said photon absorbing region and reverse biasing circuitry configured to apply a voltage between said cathode and anode regions such that said cathode region is driven to a more positive voltage than said anode region.

2. (Original) The integrated detector/processing circuit of claim 1, wherein the thickness of the photon absorbing region is in the range of 0.5 to 5 micrometers.

3. (Original) The integrated detector/processing circuit of claim 1, wherein the electronic

processor comprises an application specific integrated circuit (ASIC) comprising at least one of complementary metal oxide semiconductor (CMOS) devices, bipolar (Bi) devices, and BiCMOS devices.

4.(Original) The integrated detector/processing circuit of claim 1, wherein the photon absorbing region is configured to absorb in excess of 60% of the incident source signal at wavelengths from 800 nm to 900 nm and provide an output electrical signal corresponding thereto.

5. (Original) The integrated detector/processing circuit of claim 1, wherein the photon absorbing region is configured to absorb the incident source signal at an absorption percentage that varies by less than 20% over selected wavelength spans of at least 20 nm of source signal wavelengths from 800 nm to 900 nm.

6. (Canceled) The integrated detector/processing circuit of claim 1, wherein the photon absorbing region is configured to absorb the incident source signal at an absorption percentage that varies by less than 20% over selected wavelength spans of at least 20 nm of source signal wavelengths from 800 nm to 900 nm.

7. (Original) The integrated detector/processing circuit of claim 1, wherein the photon absorbing region is configured to absorb in excess of 60% of the incident source signal at wavelengths from 800 nm to 900 nm and provide an output electrical signal corresponding thereto

8. (Previously Submitted) The integrated detector/processing circuit of claim 1, further including one or more additional photodetectors formed on said semiconductor substrate and having respective photon absorbing regions receiving respective additional source signals and providing respective output electrical signals corresponding thereto, and one or more additional electronic processors also formed on said semiconductor substrate and operatively associated with the respective photon absorbing regions of said additional

photodetectors to receive therefrom and [procces] process said respective output electrical signals therefrom.

9. (Previously Submitted) The integrated detector/processing circuit of claim 1, wherein the plurality of holes enhances absorption of photons compared to a hole-free but otherwise same photodetector at a range of wavelengths that includes a wavelength of said source signal.

10. (Original) The integrated detector/processing circuit of claim 1, wherein the electronic processor includes one or more types selected from a group consisting of: transimpedance amplifier, signal processing electronics, and routing electronics.

11. (Original) The integrated detector/processing circuit of claim 1, wherein a capacitance associated with the photodetector is decreased compared to an otherwise same photodetector having its anode and cathode regions operatively connected to a conventional bond pad.

12. (Currently Amended) A photodetector with microstructure-enhanced photoabsorption comprising:

a photon absorbing region that comprises an I-region between an N-region and a P-region, said I-region having a thickness between 0.5 and 5 micrometers and configured to absorb photons from a source signal modulated for data communication and provide an output electrical signal corresponding thereto;

said photon absorbing region comprising silicon with a plurality of holes extending through at least a portion of the thickness of the ~~photon absorbing~~ I-region and configured to concurrently receive the same source signal at a plural number of the holes; and

said photon absorbing region being configured to absorb in excess of 40% of the incident source signal at wavelengths in at least one of the ranges from 800 nm to 900 nm and from 1400 nm to 1700 nm and provide an output electrical signal

corresponding thereto.

13. (Original) The photodetector of claim 12, wherein the photon absorbing region is configured to absorb in excess of 40% of the incident source signal at wavelengths from 800 nm to 900 nm and provide an output electrical signal corresponding thereto.

14. (Original) The photodetector of claim 12, wherein the photon absorbing region is configured to absorb in excess of 50% of the incident source signal at wavelengths from 800 nm to 900 nm and provide an output electrical signal corresponding thereto.

15. (Original) The photodetector of claim 12, wherein the photon absorbing region is configured to absorb the incident source signal at an absorption percentage that varies by less than 20% over wavelength spans of at least 20 nm of source signal wavelengths from 800 nm to 900 nm.

16. (Original) The photodetector of claim 12, wherein each hole has a cross-section parallel to the upper surface of the substrate and has a maximum dimension of between 400 nm and 2500 nm, and each hole has a center that is spaced apart by less than 3500 nm from a center of a nearest adjacent hole of the plurality of holes.

17. (Previously Submitted) The photodetector of claim 12, wherein the photodetector comprises a reflecting structure configured to cause multiple reflections of the source signal thereby traversing the photon absorbing region with said source signal multiple times.

18. (Currently Amended) A photodetector with microstructure-enhanced photoabsorption comprising:

a cathode region;

an anode region;

reverse biasing circuitry configured to apply a voltage between said cathode and anode regions such that said cathode region is driven to a more positive voltage than said

anode region;

a substrate material having an upper surface; and

a photon absorbing I-region comprising silicon, operatively associated with the cathode and anode regions, and configured to absorb photons from a source signal, said photon absorbing I-region including a plurality of holes each having a cross section parallel to the upper substrate surface having a maximum dimension of between 400 nm and 2500 nm, and each hole having a center that is spaced apart by less than 3500 nm from a center of a nearest adjacent hole of the plurality of holes, said I-region being configured to absorb photons from a source signal that has a substantially continuous profile illuminating an area that includes plural holes in the I-region.

19. (Original) The photodetector of claim 18 wherein the source signal has a wavelength that is greater than 800 nm and less than 1000 nm.

20. (Canceled) The photodetector according to claim 18 wherein the plurality of holes are arranged into a periodically-spaced array.

21. (Canceled) The photodetector according to claim 20 wherein the periodically-spaced array has a hexagonal or square lattice pattern.

22. (Previously Submitted) The photodetector according to claim 18 wherein the plurality of holes enhances absorption of photons compared to a hole-free but otherwise same photodetector at a range of wavelengths that includes a wavelength of said source signal.

23. (Previously Submitted) The photodetector according to claim 18 wherein each of the holes has a predominately circular cross-section parallel to the upper substrate surface.

24. (Original) The photodetector according to claim 18 wherein the cathode and anode regions

are operatively connected to integrated circuit electronics and the photodetector and integrated circuit electronics are integrated into a single silicon chip.

25. (Canceled) The photodetector according to claim 24 wherein the integrated circuit electronics includes one or more types selected from a group consisting of: transimpedance amplifier, signal processing electronics and routing electronics.

26. (Canceled) The photodetector according to claim 18 wherein said photodetector is configured to detect said source signal at a data bandwidth of greater than 2.5 gigabits per second at source signal wavelengths of 850 nanometers with a quantum efficiency of at least 30%.

27. (Canceled) The photodetector according to claim 18 wherein said photodetector is configured to detect said source signal at a data bandwidth of greater than 2.5 gigabits per second at source signal wavelengths of 850 nanometers with a quantum efficiency of at least 50%.

28. (Original) The photodetector according to claim 18 wherein said photodetector is configured to detect said source signal at a data bandwidth of greater than or equal to 5 gigabits per second, at source signal wavelengths of 850 nanometers with a quantum efficiency of at least 30%.

29. (Original) The photodetector according to claim 18 wherein said photodetector is configured to detect said source signal at a data bandwidth of greater than or equal to 5 Gb/s, at source signal wavelengths of 850 nanometers with a quantum efficiency of at least 50%.

30. (Original) The photodetector according to claim 18 further including a substrate and wherein the cathode, absorbing and anode regions are formed above the substrate and the photodetector is configured to receive the source signal from directions facing a side of the photodetector opposite of the substrate.

31. (Currently Amended) A single silicon substrate on which are fabricated and integrated a photodetector, an active electronic circuit, and electrical interconnects that operatively couple the photodetector and the active electronic circuit to each other and provide an output for use by other circuits, comprising:

a photodetector fabricated on the single silicon substrate and comprising a P-doped region, an N-doped region, and an I-region that is between the P-doped region and the N-doped region and is not intentionally doped or is doped to a lower dopant concentration than the P-doped region and the N-doped region, wherein:

said I-region:

comprises at least one of silicon and germanium;

is no more than 5000 nanometers thick in a direction from one toward the other of said P-doped region and said N-doped region;

comprises intentionally formed pillars or holes, said pillars or holes being spaced from each other and extending in said direction from one toward the other of said P-doped region and N-doped region;

said photodetector is configured to receive an optical beam that:

is modulated at 10 Gigabits per second or more;

is substantially continuous in cross-section; and

impinges on plural ones of said pillars or holes at the same time;

said photodetector is further configured to provide, in response to impingement thereon of said optical beam, a photodetector electrical output that:

represents the modulation of said optical beam; and

has a bandwidth of 10 Gigabits per second or more;

said photodetector has quantum efficiency of at least 30% (i) when the optical beam wavelength in 850-1000 nm and the I-region comprises silicon, and (ii) when the optical beam wavelength is 1550-1600 ~~1660~~ nm and the I-region comprises germanium; and

an active electronic circuit that:

is fabricated on the substrate on which the photodetector is fabricated;

comprises at least one of CMOS and BiCMOS integrated circuit fabricated with at least one of silicon and germanium; and

is configured to:

receive the photodetector electrical output from the photodetector; and

process the received photodetector electrical output to thereby produce a processed electrical output that has at least some different characteristics compared with the photodetector electrical output; and

electrical interconnects that:

also are fabricated on the same silicon substrate;

are configured to operatively couple said photodetector and said active electronic circuit to each other, including by transferring said photodetector electrical output from said photodetector to said active electronic circuit; and

are further configured to output the processed electrical output from the active electronic circuit for use by other circuits.

32. (Previously Submitted) The single silicon substrate of claim 31 in which the I-region comprises said holes.

33. (Previously Submitted) The single substrate of claim 32 in which the holes are arranged in an aperiodic array.

34. (Previously Submitted) The single silicon substrate of claim 31 in which the I-region comprises said pillars.

35. (Previously Submitted) The single silicon substrate of claim 31 in which said pillars are arranged in an aperiodic array.

36. (New) The single silicon substrate of claim 31 in which said pillars or holes are tapered.

REMARKS

This Fourth Preliminary Amendment clarifies independent claims 1, 12, and 18 based on the disclosure that holes exist at least in the I-region of PIN or NIP devices. In addition, this paper corrects a typing error in claim 31 (correcting a wavelength range from 1550-1660 nm to 1550-1600 nm), and cancels claim 6 that is a duplicate of claim 5 and adds in its place a dependent claim 36. The total number of claims remains 30, of which 4 are independent.

Applicants believe that the permissible number of claims for this application is 30 total of which 4 are independent. Their petition to make special based on age was granted on January 21, 2016 under 37 CFR 1.102(c)(1). The Rule is reproduced below, with pertinent parts underlined:

37 CFR 1.102 Advancement of examination.

- (a) Applications will not be advanced out of turn for examination or for further action except as provided by this part, or upon order of the Director to expedite the business of the Office, or upon filing of a request under paragraph (b) or (e) of this section or upon filing a petition or request under paragraph (c) or (d) of this section with a showing which, in the opinion of the Director, will justify so advancing it.
- (b) Applications wherein the inventions are deemed of peculiar importance to some branch of the public service and the head of some department of the Government requests immediate action for that reason, may be advanced for examination.
- (c) A petition to make an application special may be filed without a fee if the basis for the petition is:
  - (1) The applicant's age or health; or
  - (2) That the invention will materially:
    - (i) Enhance the quality of the environment;
    - (ii) Contribute to the development or conservation of energy resources; or
    - (iii) Contribute to countering terrorism.
- (d) A petition to make an application special on grounds other than those referred to in paragraph (c) of this section must be accompanied by the fee set forth in § 1.17(h).
- (e) A request for prioritized examination under this paragraph must comply with the requirements of this paragraph and be accompanied by the prioritized examination fee set forth in § 1.17(c), the processing fee set forth in § 1.17(i), and if not already paid, the publication fee set forth in § 1.18(d). An application for which prioritized examination has been requested may not contain or be amended to contain more than four independent claims, more than thirty total claims, or any multiple dependent claim.

The limitation to 20 claims does not apply to applications that are made special based on age of an inventor, as explained in the portion of MPEP reproduced below with added

underlining of pertinent portions:

708.02(a) Accelerated Examination [R-07.2015]

All petitions to make special, except those based on applicant's health or age or participation in the Patent Prosecution Highway (PPH) pilot program must meet the requirements set forth in subsection I below. See MPEP § 708.02 subsection I or II (where appropriate) for the requirements for filing a petition to make special based on applicant's health or age. For prioritized examination under 37 CFR 1.102(e), see MPEP § 708.02(b). For participation in the Patent Prosecution Highway program, see MPEP § 708.02(c).

I.REQUIREMENTS FOR PETITIONS TO MAKE SPECIAL UNDER ACCELERATED EXAMINATION

A new application may be granted accelerated examination status under the following conditions:

- (A) The application must be filed with a petition to make special under the accelerated examination program accompanied by either the fee set forth in 37 CFR 1.17(h) or a statement that the claimed subject matter is directed to environmental quality, the development or conservation of energy resources, or countering terrorism. See 37 CFR 1.102(c)(2). Applicant should use form PTO/SB/28 for filing the petition.
- (B) The application must be a non-reissue utility or design application filed under 35 U.S.C. 111(a).
- (C) The application, petition, and required fees must be filed electronically using the USPTO's electronic filing system (EFS), or EFS-Web. If the USPTO's EFS and EFS-Web are not available to the public during the normal business hours for these systems at the time of filing the application, applicant may file the application, other papers and fees by mail accompanied by a statement that EFS and EFS-Web were not available during the normal business hours, but the final disposition of the application may occur later than twelve months from the filing of the application. See subsection VIII.F. below for more information.
- (D) At the time of filing, the application must be complete under 37 CFR 1.51 and in condition for examination. For example, the application must be filed together with the basic filing fee, search fee, examination fee, and application size fee (if applicable), and an executed inventor's oath or declaration (under 37 CFR 1.63 or 1.64) for each inventor. See subsection VIII.C. below for more information.
- (E) The application must contain three or fewer independent claims and twenty or fewer total claims. The application must also not contain any multiple dependent claims.

The Patent Office is hereby authorized to charge any fees that are required in connection with this amendment and to credit any overpayment to our Deposit Account No. 03-3125.

Respectfully submitted,

/Ivan S. Kavrukov/

Ivan S. Kavrukov, Reg. No. 25,161
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Electronic Acknowledgement Receipt

EFS ID:	27076666
Application Number:	14945003
International Application Number:	
Confirmation Number:	1200
Title of Invention:	MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES
First Named Inventor/Applicant Name:	Shih-Yuan WANG
Customer Number:	23432
Filer:	Ivan Kavrukov/Erin Finnegan
Filer Authorized By:	Ivan Kavrukov
Attorney Docket Number:	5176-88184-2
Receipt Date:	29-SEP-2016
Filing Date:	18-NOV-2015
Time Stamp:	16:17:42
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Preliminary Amendment	4thPreliminaryAmendment_14_945003_Sept2016.pdf	168521 bfa9cee910e89c2c7caf7523e0aeec8e77d28b7d	no	12

Warnings:

Information:	
Total Files Size (in bytes):	168521

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Dkt. 5176/88184-2

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application of: Shih-Yuan WANG et al.

Application No.: 14/945,003

Confirmation No.: 1200

GAU: 2893

Filed: November 18, 2015

Examiner: Rodela, Eduardo A.

For: MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES

This correspondence is being filed electronically with the U.S. Patent and Trademark Office via EFS-Web.

/erin finnegan/ **September 27, 2016**

Erin Finnegan Date

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New York, New York 10112
Tel.: (212) 278-0400

INFORMATION DISCLOSURE STATEMENT

It is respectfully requested that the information cited in annexed form be considered by the Examiner in connection with the above-identified patent application, To the best of Applicant's knowledge, this Information Disclosure Statement is being filed before the date of mailing of a first Office Action on the merits in connection with this application.

The citation of the listed items is not a representation that they constitute a complete or exhaustive listing of the relevant art or that these items are prior art. The items listed are submitted in good faith, but are not intended to substitute for the Examiner's search. It is hoped, however, that in addition to apprising the Examiner of the particular items, they will assist in identifying fields of search and in making as full and complete a search as possible.

The filing of this Information Disclosure Statement is not an admission that the information cited herein is, or is considered to be, material to patentability as defined in 37 C.F.R. §1.56(b).

According to the August 5, 2003 OG Notice published by the Patent and Trademark Office, the Office has waived the requirement under 37 C.F.R. §1.98(a)(2)(i) for submitting a copy of each cited U.S. patent and each cited U.S. patent application publication for all U.S. national patent applications filed after June 30, 2003 and for all international application that have entered the national stage under 35 U.S.C. §371 after June 30, 2003.

Accordingly, copies are submitted herewith for only references listed on the annexed form that are not a U.S. patent or U.S. patent application publication.

The Patent Office is hereby authorized to charge any fees that are required for consideration of this Information Disclosure Statement and to credit any overpayment during prosecution of this application to our Deposit Account No. 03-3125.

Respectfully submitted,

/ivan s. kavrukov/

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PATENT COOPERATION TREATY

PCT

INTERNATIONAL SEARCH REPORT

(PCT Article 18 and Rules 43 and 44)

Applicant's or agent's file reference SYR 2001/66514-PCT	FOR FURTHER ACTION	see Form PCT/ISA/220 as well as, where applicable, item 5 below.
International application No. PCT/US14/39208	International filing date *(day/month/year)* 22 May 2014 (22.05.2014)	(Earliest) Priority Date *(day/month/year)* 22 May 2013 (22.05.2013)
Applicant Shih-Yuan Wang		

This international search report has been prepared by this International Searching Authority and is transmitted to the applicant according to Article 18. A copy is being transmitted to the International Bureau.

This international search report consists of a total of 5 sheets.

☐ It is also accompanied by a copy of each prior art document cited in this report.

1. **Basis of the report**

a. With regard to the **language**, the international search was carried out on the basis of:

☒ the international application in the language in which it was filed.

☐ a translation of the international application into _____ which is the language of a translation furnished for the purposes of international search (Rules 12.3(a) and 23.1(b)).

b. ☐ This international search report has been established taking into account the **rectification of an obvious mistake** authorized by or notified to this Authority under Rule 91 (Rule 43.6*bis*(a)).

c. ☐ With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, see Box No. I.

2. ☐ **Certain claims were found unsearchable** (see Box No. II).

3. ☒ **Unity of invention is lacking** (see Box No. III).

4. With regard to the **title**,

☒ the text is approved as submitted by the applicant.

☐ the text has been established by this Authority to read as follows:

5. With regard to the **abstract**,

☒ the text is approved as submitted by the applicant.

☐ the text has been established, according to Rule 38.2, by this Authority as it appears in Box No. IV. The applicant may, within one month from the date of mailing of this international search report, submit comments to this Authority.

6. With regard to the **drawings**,

a. the figure of the **drawings** to be published with the abstract is Figure No. 10B

☐ as suggested by the applicant.

☒ as selected by this Authority, because the applicant failed to suggest a figure.

☐ as selected by this Authority, because this figure better characterizes the invention.

b. ☐ none of the figures is to be published with the abstract.

Form PCT/ISA/210 (first sheet) (July 2009)

International application No.
PCT/US14/39208

Box No. II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. ☐ Claims Nos.:
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:

3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box No. III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:
See Extra Sheet.

1. ☐ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.

2. ☐ As all searchable claims could be searched without effort justifying additional fees, this Authority did not invite payment of additional fees.

3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:

4. ☒ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:
1-49

Remark on Protest

☐ The additional search fees were accompanied by the applicant's protest and, where applicable, the payment of a protest fee.

☐ The additional search fees were accompanied by the applicant's protest but the applicable protest fee was not paid within the time limit specified in the invitation.

☐ No protest accompanied the payment of additional search fees.

International application No.
PCT/US14/39208

A. CLASSIFICATION OF SUBJECT MATTER
IPC(8) - H01L 31/02, 31/0352, 31/107 (2014.01)
CPC - H01L 29/0603, 29/0626, 31/107
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC(8) Classification(s): H01L 31/00, 31/02, 31/0236, 31/0352, 31/036, 31/072, 31/0224, 31/107 (2014.01)
CPC Classification(s): H01L 29/02, 29/04, 29/06, 29/0603, 29/0626, 29/66113, 29/0665, 31/107; B82Y 20/00

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
MicroPatent (US Granted, US Applications, EP-A, EP-B, WO, JP, DE-G, DE-A, DE-T, DE-U, GB-A, FR-A); ProQuest (Derwent, INSPEC, NTIS, PASCAL, Current Contents Search, Dissertation Abstracts Online, Inside Conferences); IP.com; Google Scholar; KEYWORDS: microstructure*, photoabsorption, nano*, photovoltaic*, cathode*, anode*, silicon, germanium, III-V, photodiode*, reverse*, bias*

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X — Y	US 2008/0218740 A1 (WILLIAMS, R et al.) September 11, 2008; abstract; figures 1-2D, 4, and 15; paragraphs [0037, 0060, 0067, 0070]	1-6, 8-10, 16, 17, 21, 28, 30, 31, 33-36, 40, 41, 43 — 7, 11-15, 18-20, 22, 25-27, 29, 32, 37-39, 42, 44-49
Y	US 2005/0184354 A1 (CHU, J et al.) August 25, 2005; figure 1A; paragraphs [0023, 0024, 0050, 0051, 0053]	7, 29, 39
Y	WO 2012/149441 A2 (CHANG-HASNAIN, C et al.) November 1, 2012; abstract; figure 22, paragraph [0089]	11-15
Y	US 2007/0092192 A1 (ACHOUCHE, M et al.) April 26, 2007; abstract; paragraph [0045]	18-20, 22, 25, 26, 38
Y	US 2005/0092925 A1 (ZENTAI, G et al.) May 5, 2005; figure 2A; paragraphs [0016, 0017, and 0020]	27, 44-49
Y	US 7,397,101 B1 (MASINI, G et al.) July 8, 2008; figure 7A; column 7, lines 50-55; column 8, lines 5-20	32, 37

☒ Further documents are listed in the continuation of Box C. ☐

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
27 August 2014 (27.08.2014)	28 NOV 2014
Name and mailing address of the ISA/US Mail Stop PCT, Attn: ISA/US, Commissioner for Patents P.O. Box 1450, Alexandria, Virginia 22313-1450 Facsimile No. 571-273-3201	Authorized officer: Shane Thomas PCT Helpdesk: 571-272-4300 PCT OSP: 571-272-7774

International application No.
PCT/US14/39208

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 4,637,129 A (DERKITS, G, JR et al.) January 20, 1987; abstract; figures 1-7; column 2, lines 24-40	42
A	US 5,457,327 A (TAGUCHI, K) October 10, 1995; abstract; figure 1; column 5, lines 29-35	23, 24
A	US 7,795,064 B2 (PAN, Z et al.) September 14, 2010; abstract; figure 3; column 4, lines 60-66; column 5, lines 1-5	23, 24

International application No.
PCT/US14/39208

-***-Continued from Box III-***-

This application contains the following inventions or groups of inventions which are not so linked as to form a single general inventive concept under PCT Rule 13.1. In order for all inventions to be examined, the appropriate additional examination fee must be paid.

Group I: Claims 1-49 are directed toward a photodetector comprising a cathode, an anode, reverse biasing circuitry, microstructure-enhanced photon absorbing semiconductor material, and a plurality of micro structures.

Group II: Claims 50-53 are directed toward a photovoltaic device comprising a semiconductor material, a plurality of voids within said semiconductor material, and converting solar radiation into direct current electricity.

Group III: Claims 54-58 are directed toward a glass material comprising a plurality of buried voids, said voids dimensioned between 0.01 microns and 1000 microns.

Group IV: Claims 59-62 are directed toward a microwave transmission line structure comprising a semiconductor substrate, a plurality of high-density dielectric-filled voids, reduced dielectric constant, and plurality of metallic microwave transmission lines.

Group V: Claims 63-67 are directed toward an optical wave guide structure comprising an optical mode region, a supporting material, a plurality of microstructured voids in the supporting material, and altering an effective index of refraction.

Group VI: Claims 68-69 are directed toward a heat generating device, a heat sink, a surrounding medium, an intermediate material, a plurality of voids in said intermediate material, and altering the thermal conductivity of said intermediate material.

The inventions listed as Groups I-VI do not relate to a single general inventive concept under PCT Rule 13.1 because, under PCT Rule 13.2, they lack the same or corresponding special technical features. Group I has at least a cathode region, anode region, reverse biasing circuitry, source signal, and a source wavelength that Groups II-VI do not have. Group II has at least converting solar radiation into direct current electricity that Groups I and III-VI do not have. Group III has at least a glass material and dimensioned voided between 0.01 microns and 1000 microns that Groups I, II, and IV-VI do not have. Group IV has at least a dielectric filling, a reduced dielectric constant, and a plurality of metallic microwave transmission lines that Groups I-III, V, and VI do not have. Group V has at least an optical waveguide and an optical mode region that Groups I-IV and VI do not have. Group VI has at least a heat exchanger, a heat generating device, a heat sink, a surrounding medium, an intermediate material, and an altered thermal conductivity that Groups I-V do not have.

The common technical feature of Groups I-VI is at least a plurality of voids. This common feature is disclosed by US 2005/0092925 A1 to Zentai et al. (hereinafter "Zentai"). Zentai discloses a plurality of voids (a photodetector conversion layer includes a plurality of microscopic voids; abstract; figure 2A; paragraph [0016]).

Since the common technical feature is previously disclosed by the Zentai reference, this common feature is not special and so Groups I-VI lack unity.

PTO/SB/08a (01-10)
Approved for use through 07/31/2012. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	14945003
Filing Date	2015-11-18
First Named Inventor	Shih-Yuan WANG et al.
Art Unit	
Examiner Name	RODELA, EDUARDO A
Attorney Docket Number	5176/88184-2

U.S.PATENTS Remove

Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	4637129		1987-01-20	DERKITS G. JR et al.	
	2	5457327A		1995-10-10	TAGUCHI, K	
	3	7397101		2008-08-07	MASINI, G. et al.	
	4	7795064		2010-09-14	PAN, Z. et al.	
	5	7893348		2011-02-22	Korevan, B	
	6	8129710		2012-03-06	Cho, et al.	
	7	7601597		2009-10-13	Takei, M.	
	8	7115971		2006-10-03	Stumbo	

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	14945003
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	First Named Inventor	Shih-Yuan WANG et al.
	Art Unit	
	Examiner Name	RODELA, EDUARDO A
	Attorney Docket Number	5176/88184-2

	9	7674563		2010-03-09	Suda	
	10	8436370		2013-05-07	Park	
	11	5451767		1995-09-19	Amano	
	12	4716449		1987-12-29	Miller	
	13	8114695		2012-02-14	Masuoka	
	14	7772615		2010-08-10	Ledentsov	
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	18	6027956		2000-02-22	Isissou	
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	Examiner Name	RODELA, EDUARDO A
	Attorney Docket Number	5176/88184-2

	20	7495306		2009-02-24	Langguth	
	21	7972934		2011-07-05	Wilson	
	22	4571559		1986-02-18	Henry	
	23	6667528		2003-12-23	Cohen	
	24	6177289		2001-01-23	Crow	

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U.S.PATENT APPLICATION PUBLICATIONS Remove

Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	20050092925		2005-05-05	ZENTAI, G et al.	
	2	20050184354		2005-08-25	CHU, J et al.	
	3	20070092192		2007-04-26	ACHOUCHE, M et al	
	4	20080218740		2008-09-11	WILLIAMS, R. et al.	

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	Attorney Docket Number	5176/88184-2

	5	20100193768		2010-08-05	Habib	
	6	20100197068		2010-08-05	Poon	
	7	20100126548		2010-05-27	JANG, ET AL.	
	8	20080265449		2008-10-30	Meinders et al.	
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	13	20081012582		2008-01-05	Takei	
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	Examiner Name	RODELA, EDUARDO A
	Attorney Docket Number	5176/88184-2

	16	20100029067	2010-02-01	Vijh	
	17	20100221866	2010-09-01	Graham	
	18	20120193676	2012-08-02	Bobde	
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	23	20120292676	2012-11-22	Pan	
	24	20080248608	2008-10-09	Wilson	

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Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2] i	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	14945003
	Filing Date	2015-11-18
	First Named Inventor	Shih-Yuan WANG et al.
	Art Unit	
	Examiner Name	RODELA, EDUARDO A
	Attorney Docket Number	5176/88184-2

	1	WO2012149441A2	wo		2012-11-01	CHANG-HASNAIN, Connie et al.		
	2	PCT/JP2014/39208	JP		2014-11-28	International Search Report		
	3	PCT/US1561120	US		2015-11-17	WANG, S		
	4	PCT/US1439208	US		2014-05-22	WANG, S		
	5	PCT/US15/61120	US		2015-11-17	WANG, S		
	6	PCT/US11/51091	US		2011-09-09	WANG, S		
	7	WO2012034078	WO		2015-03-05	Wang, S		
	8	WO2014190189	WO		2014-11-27	Wang, S		

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NON-PATENT LITERATURE DOCUMENTS Remove

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T5
	1	M. K. Emsley, O. Dosunmu, and M. S. Unlu, "High-speed resonant-cavity-enhanced silicon photodetectors on reflecting silicon-on-insulator substrates," Ieee Photonics Technology Letters, vol. 14, pp. 519-521, Apr 2002.	

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	First Named Inventor	Shih-Yuan WANG et al.
	Art Unit	
	Examiner Name	RODELA, EDUARDO A
	Attorney Docket Number	5176/88184-2

	2	E. Ozbay, M. S. Islam, B. Onat, M. Gokkavas, O. Aytur, G. Tuttle, et al., "Fabrication of high-speed resonant cavity enhanced Schottky photodiodes," Ieee Photonics Technology Letters, vol. 9, pp. 672-674, May 1997.
	3	T. Knodl, H. K. H. Choy, J. L. Pan, R. King, R. Jager, G. Lullo, et al., "RCE photodetectors based on VCSEL structures," Ieee Photonics Technology Letters, vol. 11, pp. 1289-1291, Oct 1999.
	4	K. Kato, "Ultrawide-band/high-frequency photodetectors," Ieee Transactions on Microwave Theory and Techniques, vol. 47, pp. 1265-1281, Jul 1999.
	5	M. Amani, D. H. Lien, D. Kiriya, J. Xiao, A. Azcatl, J. Noh, et al., "Near-unity photoluminescence quantum yield in MoS2," Science, vol. 350, pp. 1065-1068, Nov 27 2015.
	6	T. Mueller, F. N. A. Xia, and P. Avouris, "Graphene photodetectors for high-speed optical communications," Nature Photonics, vol. 4, pp. 297-301, May 2010.
	7	L. Chen and M. Lipson, "Ultra-low capacitance and high speed germanium photodetectors on silicon," Optics Express, vol. 17, pp. 7901-7906, May 11 2009.
	8	P. Kuang, S. Eyderman, M. L. Hsieh, A. Post, S. John, and S. Y. Lin, "Achieving an Accurate Surface Profile of a Photonic Crystal for Near-Unity Solar Absorption in a Super Thin-Film Architecture," Acs Nano, vol. 10, pp. 6116-6124, Jun 2016.
	9	A. Mavrokefalos, S. E. Han, S. Yerci, M. S. Branham, and G. Chen, "Efficient Light Trapping in Inverted Nanopyramid Thin Crystalline Silicon Membranes for Solar Cell Applications," Nano Letters, vol. 12, pp. 2792-2796, Jun 2012.
	10	K. X. Z. Wang, Z. F. Yu, V. Liu, A. Raman, Y. Cui, and S. H. Fan, "Light trapping in photonic crystals," Energy & Environmental Science, vol. 7, pp. 2725-2738, Aug 2014.
	11	S. E. Han and G. Chen, "Optical Absorption Enhancement in Silicon Nanohole Arrays for Solar Photovoltaics," Nano Letters, vol. 10, pp. 1012-1015, Mar 2010.
	12	Y. Park, E. Drouard, O. El Daif, X. Letartre, P. Viktorovitch, A. Fave, et al., "Absorption enhancement using photonic crystals for silicon thin film solar cells," Optics Express, vol. 17, pp. 14312-14321, Aug 3 2009.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	14945003
	Filing Date	2015-11-18
	First Named Inventor	Shih-Yuan WANG et al.
	Art Unit	
	Examiner Name	RODELA, EDUARDO A
	Attorney Docket Number	5176/88184-2

	13	C. Yeh and F. I. Shimabukuro, The essence of dielectric waveguides. New York ; London: Springer, 2008.
	14	Y. G. Wang, Y. X. Kang, W. J. Zhao, S. Yan, P. J. Zhai, and X. W. Tang, "Studies on surface damageinduced by ion bombardment," Journal of Applied Physics, vol. 83, pp. 1341-1344, Feb 1 1998.
	15	Liu AY et al., High performance continuous wave 1.3 μm quantum dot lasers on silicon, Appl. Phys. Letters, 104, 041104 (2014)

If you wish to add additional non-patent literature document citation information please click the Add button Add

EXAMINER SIGNATURE

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	14945003
Filing Date	2015-11-18
First Named Inventor	Shih-Yuan WANG et al.
Art Unit	
Examiner Name	RODELA, EDUARDO A
Attorney Docket Number	5176/88184-2

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

See attached certification statement.

The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/ivan s. kavrukov/	Date (YYYY-MM-DD)	2016-09-27
Name/Print	Ivan S. Kavrukov	Registration Number	25161

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these record s.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Acknowledgement Receipt

EFS ID:	27048662
Application Number:	14945003
International Application Number:	
Confirmation Number:	1200
Title of Invention:	MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES
First Named Inventor/Applicant Name:	Shih-Yuan WANG
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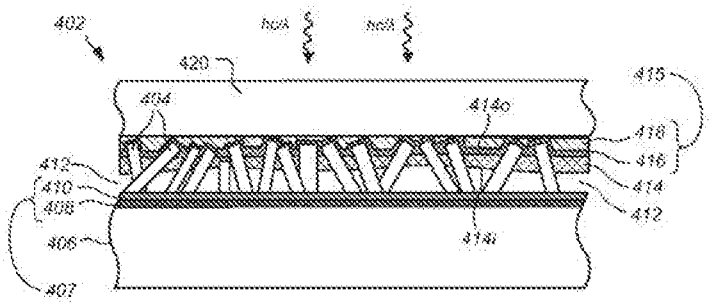

FIG. 4

(57) Abstract: Nanowire-based photovoltaic energy conversion devices and related fabrication methods therefor are described. A plurality of photovoltaic (PV) nanowires extend outwardly from a surface layer of a substrate, each PV nanowire having a root end near the substrate surface layer and a tip end opposite the root end. For some embodiments, a collar material is formed that laterally surrounds and is in contact with the PV nanowires along a portion of one or more of their ends. According to some embodiments, the PV nanowires are formed on a crystalline silicon substrate. According to some other embodiments, the PV nanowires are formed on a roll-sourced continuous substrate.

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PHOTOVOLTAIC NANOWIRE STRUCTURES AND RELATED FABRICATION METHODS

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application is related to, and claims the benefit of, each of the following U.S. Provisional Patent Applications: U.S. Prov. Ser. No. 61/381,930, filed September 10, 2010; U.S. Prov. Ser. No. 61/390,732, filed October 7, 2010; U.S. Prov. Ser. No. 61/415,943, filed November 22, 2010; U.S. Prov. Ser. No. 61/450,107, filed March 7, 2011; and U.S. Prov. Ser. No. 61/526,629, filed 23 August 2011. This application is related to the subject matter of the following applications: U.S. Prov. Ser. No. 61/236,144, filed August 24, 2009; U.S. Prov. Ser. No. 61/263,315, filed November 20, 2009; U.S. Prov. Ser. No. 61/264,194, filed November 24, 2009; U.S. Prov. Ser. No. 61/295,500, filed January 15, 2010; U.S. Prov. Ser. No. 61/295,579, filed January 15, 2010; U.S. Prov. Ser. No. 61/295,606, filed January 15, 2010; U.S. Prov. Ser. No. 61/309,414, filed March 1, 2010; International Application No. PCT/US10/46334 filed August 23, 2010; and U.S. Prov. Ser. No. 61/376,358, filed August 24, 2010. Each of the above-referenced applications is incorporated by reference herein in its entirety.

FIELD

[0002] This patent specification relates to photovoltaic energy conversion devices, such as may be used in photovoltaic solar cells and solar panels. More particularly, this patent specification relates to nanowire-based photovoltaic energy conversion devices, as well as systems and methods for fabricating such devices.

BACKGROUND

[0003] Solar electric power generation systems, particularly those based on photovoltaic solar panels, continue to gain popularity in efforts to shift away from supply-limited, greenhouse-gas producing fossil fuels to more environmentally friendly and sustainable forms of energy. Most of today's conventional rooftop photovoltaic solar panels comprise side-by-side arrangements of relatively large (*e.g.*, 5 cm x 5 cm, 10 cm x 10 cm) bulk monocrystalline or bulk multicrystalline silicon wafers processed to form depthwise p-n junctions. Manufacture of the bulk

crystalline silicon wafers is highly energy-intensive and expensive, and the power conversion efficiency of the resultant devices is typically only in the range of 15% to 20%. A chronic shortage in the supply of bulk crystalline silicon wafers has plagued the industry in recent years, a shortage that is expected by some forecasters to reach crisis proportions in coming years. Although thin-film photovoltaic cells fabricated from amorphous silicon or chalcogenide compounds require less semiconductor material than those based on bulk crystalline silicon wafers and are less energy-intensive and less costly to produce, their power conversion efficiencies are even lower, usually in the 6% to 10% range.

[0004] Proposals have been set forth for using semiconducting nanowires as a basis for photovoltaic solar energy conversion. Nanowires are small self-assembled structures having lengths typically in the range of 0.5 μm – 5 μm and diameters typically in the range of 10 nm – 1000 nm. One method of fabricating nanowires uses a vapor-liquid-solid ("VLS") synthesis process, sometimes termed a catalytic growth process. A catalyst material such as gold or titanium is deposited on a substrate at a large number of spots thereacross, each spot being a location at which a nanowire will be grown. The substrate with the catalyst is then placed in a reaction chamber and heated to high temperatures (*e.g.*, 250° C - 1000° C). Precursor gases, including the elements or compounds that will form the nanowires, are introduced into the chamber. Under the influence of the catalyst, the precursor gases at least partially decompose into their respective elements, some of which are transported on or through the catalyst in liquified phase to the immediately underlying solid surface provided by the substrate. At each spot, a nanowire epitaxially grows outwardly from the substrate as the process proceeds, the catalyst at each spot remaining at the tip of the nanowire and rising away from surface of the substrate as the nanowire grows. The resultant nanowires exhibit a long-range atomic order (i.e., single-crystal) that can potentially be exploited for a variety of different useful applications. So-called self-catalytic growth of nanowires has also been reported in the literature.

[0005] During nanowire formation, the elements or compounds used to form the nanowires can be varied, such that the material composition and/or semiconductor doping level of each nanowire is variable along the longitudinal length of that nanowire. In one known scenario relevant to the preferred

embodiments herein, the longitudinally varying material and/or doping profile can be designed such that each nanowire exhibits a photovoltaic property, *i.e.*, is capable of absorbing incident photons and providing an associated photocurrent to an external load (if properly electrically connected to that load). As used herein, PV nanowire refers to any of a variety of nanowires themselves or related structures that employ nanowires and are capable of exhibiting photovoltaic properties, such photovoltaic properties arising from any of a variety of different material selections, material compositional and spatial chemical profiles, and/or doping profiles thereof. By way of non-limiting example, PV nanowires can comprise one or more longitudinal homojunctions (e.g., p-n, p-i-n, p-n-p, n-p-n homojunctions), one or more longitudinal heterojunctions (e.g., materials containing various chemical elements and/or various chemical compositions and various bandgaps), and/or portions of such homojunctions or heterojunctions that are completed by virtue of the materials and/or doping profiles immediately opposite the longitudinal end(s) of the nanowire. One example of a PV nanowire-based solar cell is described in US 2007/0267625 A1, which is incorporated by reference herein in its entirety.

[0006] Advantageously, PV nanowire-based solar cells can provide power conversion efficiencies that are as great, or even greater, than solar cells based on bulk crystalline wafers made of a same material. For example, it is believed at least theoretically possible to achieve PV nanowire-based solar cells composed of III-V semiconductor material having 35 percent, and perhaps even 40 percent, energy conversion efficiency, which is as high or better than photovoltaic cells made with bulk crystalline semiconductor wafers. At the same time, because they can be built upon low-cost substrates with low material utilization and comparatively low energy requirements, PV nanowire-based solar cells can be fabricated at a fraction of the cost of comparable solar cells based on bulk crystalline wafers.

[0007] One or more issues may arise in the design and/or fabrication of PV nanowire-based solar cells that is at least partially resolved by one or more of the preferred embodiments described herein. One issue that may arise in PV nanowire-based solar cells relates to the need for an electrode to be provided on each side of the PV nanowire array, including a root-side electrode corresponding

to the roots of the PV nanowires and a tip-side electrode corresponding to the tips of the PV nanowires. The need to provide good electrical contact and conductivity at these electrodes can present substantial limitations on the type, complexity, and orientation of the overall PV nanowire-based solar cells, because structures providing the good electrical contact and conductivity can often prove to be light-absorbing or light-reflecting, thereby reducing the percentage of photons able to reach the PV nanowire junctions. For PV nanowire-based solar cells that are based on longitudinal p-i-n junctions, another issue that may arise relates to the quality of p-type, intrinsic-type, and n-type semiconductor material that physically forms the PV nanowire for achieving optimum photovoltaic performance.

[0008] One issue that can affect the performance of PV nanowire-based solar cells is carrier loss due to charge recombination occurring along the surface of the PV nanowires. Charge recombination is a loss process in which an electron, which has been photo-excited from the valence band to the conduction band of a semiconductor, falls back into an empty state (hole) in the valence band. Charges that recombine do not produce any photocurrent and, hence, do not contribute toward solar cell efficiency. Charge recombination losses can be particularly strong along the surface of a semiconductor material, where dangling bonds give rise to certain surface states that greatly facilitate the electron-hole recombination process. Because the recombination losses associated with surfaces scale with total surface area, the problem becomes particularly amplified for nanowires having high surface-to-volume ratio. Generally speaking, the recombination losses at surfaces tend to be more problematic for III-V compound semiconductor PV nanowires than for silicon PV nanowires for which stable natural oxide (i.e., SiO_2) that can be easily formed on Si surfaces can greatly reduce the density of surface states. Other issues may arise as would be apparent to one skilled in the art upon reading the present disclosure.

SUMMARY

[0009] According to some embodiments, a method for fabricating a photovoltaic energy conversion device is described. The method includes providing a substrate including a substrate surface layer doped in a first dopant type (e.g. n-type or p-type); growing a plurality of photovoltaic (PV) nanowires outwardly from the substrate surface layer, each PV nanowire having a root end

near the substrate surface layer and a tip end opposite the root end; forming a layer of collar material that laterally surrounds and is in contact with the PV nanowires along at least a rootward portion of their lengths, the collar material doped in the first dopant type; and forming a tip-side doped material doped in a second dopant type, the tip-side doped material in contact with the tip ends of the PV nanowires.

[0010] According to some embodiments the layer of collar material is grown in a lateral direction from the PV nanowires, and a layer of optically transparent, electrically insulating solid filler material is provided that laterally surrounds the PV nanowires along an outward portion of their lengths. A longitudinal p-i-n junction is preferably associated with each PV nanowire. According to some embodiments, the growing of PV nanowires is partially carried out before the forming of the collar material and partially carried out after the forming of the collar material, such that a gap between 0.2 microns and 5 microns is formed between an outward-most portion of the collar material a rootward most portion of the tip-side material. The PV nanowires are not intentionally doped, according to some embodiments. In such cases the PV nanowires preferably have impurity levels less than 10^{17} per cubic centimeter.

[0011] According to some embodiments, a method for fabricating a photovoltaic energy conversion device it described that includes: providing a substrate including an n-doped substrate surface layer; growing a plurality of n-doped photovoltaic (PV) nanowires outwardly from the substrate surface layer, each PV nanowire having a root end near the substrate surface layer and a tip end opposite the root end; forming a layer of optically transparent, electrically insulating solid filler material that laterally surrounds the PV nanowires along a portion of their lengths; and forming a tip-side p-doped material in contact with the tip ends of the PV nanowires. According to some embodiments, the tip-side p-doped material is p+ or p++ type doped.

[0012] According to some embodiments, a method for fabricating a photovoltaic energy conversion device is described that includes: providing a 6" by 6" square substrate including a substrate surface layer on which the PV nanowires and other structures are formed.

[0013] According to some embodiments, a method for fabricating a photovoltaic energy conversion device is described, that includes forming a mask layer on the substrate surface layer, the mask having a plurality of spaced apart voids such that portions of the substrate surface layer are exposed at the locations of the voids. The photovoltaic (PV) nanowires are grown outwardly from the exposed portions of the substrate surface layer.

[0014] According to some embodiments, a method for fabricating a photovoltaic energy conversion device is described that includes providing a substrate including a long range atomic order (LRAO) substrate surface layer (such as a highly n-type doped <111> crystallographic plane of the silicon wafer); and growing a plurality of n-doped photovoltaic (PV) nanowires outwardly from the LRAO substrate surface layer.

[0015] According to some embodiments, a method for fabricating a photovoltaic energy conversion device is described that includes providing a roller-based substrate material including a substrate surface layer with short range atomic order (SRAO) such as polysilicon or amorphous silicon, on which the PV nanowires and other structures are formed.

[0016] According to some embodiments, a photovoltaic energy conversion device is provided that is fabricated according to the methods described herein.

BRIEF DESCRIPTION OF THE DRAWINGS

[0017] Fig. 1 illustrates fabricating a PV nanowire structure according to some preferred embodiments;

[0018] Fig. 2A illustrates a simplified cross-sectional view of one of the PV nanowire structures formed according to the method of Fig. 1;

[0019] Fig. 2B illustrates a simplified perspective view thereof;

[0020] Figs. 3A-C illustrate an alternative method of manufacture using a thin mask structure, according to some embodiments;

[0021] Fig. 4 illustrates a cross-sectional view of a PV nanowire-based solar cell, according to some embodiments;

[0022] Fig. 5 illustrates some fabrication steps of the device of Fig. 4 according to some embodiments;

[0023] Fig. 6 illustrates fabrication of a PV nanowire-based solar cell according to some embodiments;

[0024] Fig. 7 is a block diagram showing stations of a continuous substrate roll manufacturing process for fabricating PV nanowire-based solar cells, according to some embodiments;

[0025] Figs. 8A-B schematically illustrate roll-based continuous substrate manufacturing processes for PV nanowire-based solar cells, according to some embodiments;

[0026] Fig. 9 is diagram schematically illustrating a heating and/or cooling station, according to some embodiments;

[0027] Figs. 10A-B show cross sections of a processing chamber having a moveable lid, according to some embodiments;

[0028] Fig. 11 is a cross section of a processing chamber having high impedance wall section, according to some embodiments;

[0029] Fig. 12 is a cross section of a processing chamber having double rollers, according to some embodiments;

[0030] Fig. 13 is a plan view of a processing station used to spray on nanowire catalyst material, according to some embodiments;

[0031] Fig. 14 schematically illustrates a large area discrete substrate manufacturing process for PV nanowire-based solar cells, according to some embodiments; and

[0032] Fig. 15 illustrate a structure that includes an n-doped PV nanowire and a heavily doped p-type tip-side electrode material, according to some embodiments.

DESCRIPTION

[0033] One or more aspects of the preferred embodiments hereinbelow may be further understood in view of selected background references from the non-patent literature identified in the list that follows. The listed references, each of which is incorporated by reference herein in its entirety, are referenced further hereinbelow by their respective identifying numerals.

[0034] {1} Kobayashi, et. al., "Metal Organic Chemical Vapor Deposition of Indium Phosphide Nanoneedles on Non-Single Crystal Silicon Surfaces," Proc. SPIE, Vol. 6370, 63700S-1-8 (2006);

[0035] {2} Kobayashi, et. al., "Growth and Characterization of Indium Phosphide Single-Crystal Nanoneedles on Microcrystalline Surfaces," Appl. Phys. A, Vol. 85, 1-6 (2006);

[0036] {3} Kobayashi, et. al., "Ensembles of Indium Phosphide Nanowires: Physical Properties And Functional Devices Integrated On Non-Single Crystal Platforms," Appl. Phys. A, Vol. 95, 1005-1013 (2009);

[0037] {4} Goto, et. al., "Growth of Core-Shell InP Nanowires for Photovoltaic Application by Selective-Area Metal Organic Vapor Phase Epitaxy," Applied Physics Express 2, 035004-1-3 (2009);

[0038] {5} Singh, et. al., "Reduction in Surface Charge Density By New GaAs Passivation Method," J. Phys. D: Appl. Phys., Vol. 8, L42-43 (1975);

[0039] {6} Kalhor, et. al., "Annealing Effects on Opto-electronic Properties of Thermally-Evaporated ITO/Ag/ITO Multilayered Films for Use in Color Filter Electrodes," World Applied Sciences Journal 6 (1): 83-87 (2009);

[0040] {7} Perkins, et. al., "Combinatorial Optimization of Transparent Conducting Oxides (TCOs) for PV," 31st IEEE Photovoltaics Specialists Conference and Exhibition, Lake Buena Vista, Florida, Jan. 3-7, 2005, NREL/CP 520-37420 (2005);

[0041] {8} Pern, et. al., "Accelerated Exposure Tests of Encapsulated Si Solar Cells and Encapsulation Materials," National Center for Photovoltaics Program Review Meeting, Denver, Colorado, Sept. 8-11, 1998, NREL/CP-520-25361 (1998);

[0042] {9} Guillen, et. al., "ITO/Metal/ITO Multilayer Structures Based On Ag and Cu Metal Films for High Performance Transparent Electrodes," Solar Energy Materials and Solar Cells, Vol. 92, Issue 8, pp. 938-941 (2008);

[0043] {10} Iyer, R., "Sulfur as a Surface Passivation for InP," Appl. Phys. Lett. 53 (2) (1988);

[0044] {11} Voyles, et. al., "Absence of an Abrupt Phase Change from Polycrystalline to Amorphous in Silicon with Deposition Temperature," Phys. Rev. Lett. 86 (24), pp. 5514-5517 (2001); and

[0045] {12} Gao, L., et. al., "Self-Catalyzed Epitaxial Growth of Vertical Indium Phosphide Nanowires on Silicon," Nano Lett. 9 (6), pp 2223–2228 (2009).

[0046] PV nanowires can be formed (*e.g.*, catalytically grown or otherwise generated) upon substrates having different types of surface characteristics. PV nanowires can, of course, be formed upon substrates that exhibit long-range crystallographic order along their surfaces, including cost-intensive bulk crystalline wafer substrates. However, as described in {2}-{3}, *supra*, PV nanowires can also be formed upon substrates that do not exhibit long-range crystallographic order along their surfaces, but that do exhibit short-range crystallographic order along their surfaces at the locations of the nanowires to be formed. For purposes of the present description, the term short range atomic order (SRAO) is used interchangeably with the term short range crystallographic order. The material providing the short-range atomic order, termed herein SRAO material, can be different or the same as the underlying material that forms the bulk of the substrate. When different from the underlying substrate material, the SRAO material can be formed as a very thin layer thereupon, which can be termed a template layer. Advantageously, the substrate material underlying the SRAO template layer can be any material suitable to provide mechanical and/or electrical support for the SRAO template layer regardless of the presence or absence of crystalline character, provided only that its properties are otherwise consistent with the purpose of the apparatus to be built. By way of example, the bulk of the substrate can comprise amorphous silicon dioxide, quartz, stainless steel, or chromium. By way of example, the SRAO template layer can be a 100-nm thick film of hydrogenated amorphous silicon or hydrogenated microcrystalline silicon.

[0047] If the PV nanowires are formed upon a substrate whose surface exhibits long range atomic order, it is more likely that a high percentage of the nanowires will be in geometric alignment with each other and that their tips will rise to similar heights above the substrate surface. If the PV nanowires are formed upon a substrate having an short range atomic order (SRAO) material surface, the population of PV nanowires will be more likely to have a lesser degree of alignment due to the multiple different crystallographic directions imposed upon the population of PV nanowires, and there will be greater variation in the heights of their tips above the substrate surface. The preferred PV nanowire-coupling fabrication methods described hereinbelow are presented in the context of PV nanowires formed upon substrates having SRAO material surfaces. In addition to

representing the more difficult (and more general) case due to greater variation in PV nanowire tip heights, the latter also represents a more commercially desirable case due to the availability of lower-cost fabrication processes, such as roll-based manufacturing processes, associated with the wide flexibility in bulk substrate material choices. It is nevertheless to be appreciated, however, that the described methods are readily applicable in the context of PV nanowires formed upon substrates whose surfaces exhibit long range atomic order, such as bulk crystalline wafer substrates.

[0048] In relation to the description that follows, it is to be readily understood that the "positive" and "negative" electrical polarities can of course be reversed depending on the material structures and doping profiles of the PV nanowires. For one or more of the examples presented herein, the "top" direction corresponds to an outward direction relative to a surface of the substrate from which the PV nanowires are grown. However, it is to be appreciated that the terms "top" and "bottom" are used for convenience of description and do not imply any particular orientation relative to gravity, nor do they imply any particular direction of solar radiation entry into the PV nanowire array.

[0049] Fig. 1 illustrates fabricating a PV nanowire structure according to some preferred embodiments. Fig. 2A illustrates a simplified cross-sectional view of one of the PV nanowire structures formed according to the method of Fig. 1, while Fig. 2B illustrates a simplified perspective view thereof. At step 102, a bottom electrode layer 154 is formed upon a substrate 152, and a layer 156 of n-type amorphous hydrogenated silicon (n-type a-Si:H) is formed on the bottom electrode layer 154. The bulk of the substrate 152 substrate can comprise, for example, amorphous silicon dioxide, quartz, stainless steel, chromium, or an optically transparent glass. The bottom electrode layer can comprise, for example, a metal such as molybdenum or aluminum.

[0050] At step 104 a nanoparticle catalyst island 158, comprising for example gold or platinum, is formed on the n-type a-Si:H layer 156 at each location where a nanowire is to be grown. The catalyst island 158 will be shaped and dimensioned according to the desired profile of the nanowire to be grown. In one example, the catalyst island 158 can be generally circular with a diameter in the range of 50 nm – 500 nm.

[0051] At step 106, catalytic nanowire growth is commenced, for example at a temperature of 430 degrees Celsius for InP nanowires, in conjunction with the introduction of appropriate precursor gases into the growth chamber. However, according to a preferred embodiment, the nanowire growth process proceeds only to a time when the nanowire tips are at a predetermined intermediate height, such as 500 nm, above the surface of the n-type a-Si:H layer. At this point, as illustrated in Fig. 1, only a root section 160a of a nanowire has been formed.

[0052] At step 108, the temperature is then raised to 500-600 degrees, and the precursor gases used in step 106 are kept the same except that n-type dopants are also introduced into the reaction chamber. Due to the raised temperature, the upward nanowire growth, as catalyzed by the nanoparticle catalyst island 158, stops occurring. Instead a more standard (non-catalytic) crystallographic growth of the InP material occurs, with the lateral sides of the root section 160a serving as a "substrate" for that growth. Accordingly, at step 108 the growth proceeds laterally, rather than upwardly, to form what is essentially a cylindrical shell 162 of InP material around the root section 160a, and because n-type dopants are introduced, the InP shell 162 is an n+ type shell. The lateral growth of the n+ type shell 162 proceeds until its thickness (*i.e.*, the amount that it extends laterally outward from the root section 160a) is comparable to the diameter of the root section 160a, *e.g.*, about 500 nm. Suitable n-type dopants for step 108 include, for example, Te, Sn, and Si for the case of InP nanowires. Notably, it is acceptable and can indeed be advantageous if some n-doping of the nanowire root section 160a occurs during the step 108.

[0053] At step 110, subsequent to the formation of the n+ type shell 162, the temperature is again lowered to the previous catalytic nanowire growth temperature, such as 430 degrees Celsius for InP nanowires, and the upward catalytic nanowire growth process is resumed to form upper nanowire portions 160b, proceeding until completed nanowires 160 at their full ultimate intended height (such as between 2 μm to 5 μm, although the scope of the present teachings is not so limited) are formed. Optionally, after nanowire growth, a thin passivation layer can be applied on the surface of the nanowires to chemically and physically protect the nanowires and stabilize the surface of the nanowires to reduce the density of unfavorable surface states. Such thin passivation layer can

be made by a technique such as atomic layer deposition that relies upon self-limiting surface chemical reaction of precursors containing desired chemical elements such that the voids among the nanowires will not be filled.

[0054] At step 112 an optically transparent, electrically insulating solid filler material layer 164 is applied, such as by spinning, such that the tips of the nanowires 160 are covered. For one preferred embodiment, the filler layer 164 comprises a spin-coating material, such as spin-on glass (SOG) or cyclotene, that is applied to the top of the nanowire array and then spun on. Notably, a variety of different materials for the solid filler layer 164 and methods for achieving the result of step 112 are within the scope of the preferred embodiments. For example, the solid filler layer 164 can alternatively comprise one or more of Si oxides, Si nitrides, Al oxide, Al nitride, or other materials that are optically transparent and electrically insulating, and methods of application other than spinning such as spraying and injecting via inkjet could be used.

[0055] At step 114, the solid filler layer 164 is subject to a dry etch, such as with O2 plasma, so that most of the nanowires 160 jut outwardly from an outward surface of the solid filler layer 164 and are available to make good physical and electrical contact with a tip-side electrode layer. Since the nanowires 160 are less affected by the etching, their tip ends will look much like stubble or whiskers sticking out of the solid filler layer 164. The solid filler layer 164 may advantageously provide at least some degree of passivation of the nanowire surfaces.

[0056] At step 116, the temperature is again raised to 500-600 degrees Celsius and the InP precursor gases introduced into the chamber, this time in the presence of p-type dopants, to form a p+ type shell 166 around the tip ends of the nanowires 160 in a lateral non-catalytic growth process similar to that described above for step 108. Suitable dopants for step 116 include, for example, Zn and Mg for the case of InP nanowires. Notably, it is acceptable and can indeed be advantageous if some p-doping of the nanowire tip sections occurs during the lateral growth process of step 116. Moreover, it is also acceptable and can be advantageous, as shown in the progress drawing adjacent to box 116 of Fig. 1, for the p+ type shells 166 of adjacent nanowires 160 to merge together. Alternatively, there can be formed a p+ type layer using any of a variety of materials having a bandgap greater

than the 1.35 eV bandgap of InP, such as InGaP which has a bandgap of 1.82 eV. With reference back to step 108 and as illustrated by the dotted line in the progress drawing adjacent to box 116 of Fig. 1, it is also acceptable and can indeed be advantageous for the n+ type shells 162 to merge together during step 108. Note that although the shells 166 are shown as connected in Fig. 1-2, there may be a gap between them, as shown by the dotted lines 199.

[0057] Finally, at step 118, a transparent conductive oxide layer (TCL) 168 is formed upon and around the p+ type shells 166, and grid-style metal electrode 170 is formed to complete a tip-side electrode for the overall PV nanowire structure. As illustrated in Figs. 2A-2B, each PV nanowire structure takes on an overall shape similar to that of a dumbbell, by virtue of the p+ type shells 166 near the nanowire tip and the n+ type shell 162 near the nanowire root. The resultant PV nanowire-based device provides an advantageously optimized combination of good p-i-n photovoltaic properties, good root-side and tip-side electrode connectivity and conductivity, mechanical and electrical stability, and amenability to roll-based fabrication methods.

[0058] Figs. 3A-C illustrate an alternative method of manufacture using a thin mask structure, according to some embodiments. One or more aspects of such embodiments may be further understood in view of selected background references from the non-patent literature identified in the list that follows. The listed references, each of which is incorporated by reference herein in its entirety, are referenced further hereinbelow by their respective identifying numerals.

[0059] {13} Li, RR and Dapkus, D., et. al., "Dense arrays of ordered GaAs nanostructures by selective area growth on substrates patterned by block copolymer lithography," App. Phys. Lett. 76(13), pp. 1689-1691 (27 March 2000);

[0060] {14} Zhang, Y., et. al., "Patterned growth and field emission of ZnO nanowires," Materials Letters 60, pp. 522-526 (2006);

[0061] {15} Ho, S.T., et. al., "Catalyst-free selective-area growth of vertically aligned zinc oxide nanowires," Chemical Physics Letters 463, pp. 141--144 (2008);

[0062] {16} Zhang, Y., et. al., "Selective-area growth and field emission properties of Zinc oxide nanowire micropattern arrays," Physica B 382, pp. 76-80 (2006);

[0063] {17} Bauer, J., et. al., "GaAs nanowires grown by MOVPE," Phys. Status Solidi B 247, No. 6, 1294–1309 (2010); and

[0064] {18} Dalacu, et. al., "Selective-area vapour–liquid–solid growth of InP nanowires," Nanotechnology 20, 395602 (6 pp.) (2009).

[0065] Provided according to a preferred embodiment are methods for forming photovoltaic (PV) nanowire-based solar cells, along with the resultant solar cells themselves, based on the methods of the incorporated patent references, together with the selective area growth strategies of the references {13} - {18} above, but with certain key differences as set forth hereinbelow. As illustrated in Fig. 3A, there is provided a short-range atomic order (SRAO) substrate 310, such as n-Si:H. In Fig. 3B, there is then provided a very thin mask layer of SiO2 (or other suitable oxide) 312 above the SRAO layer, a mask layer 312 is preferably so thin (for example, 2-5 nm) that it intrinsically contains a series of randomly and irregularly distributed, sized and shaped openings therethrough. The openings can alternatively be called "holes" or "voids," and the mask layer can be called a "holey film." The SRAO layer is exposed through those openings, and is not exposed elsewhere. In Fig. 3C, the PV nanowire precursor gases are introduced into the chamber at a relatively high temperature as needed for non-catalytic growth (in comparison to catalytic growth), and the PV nanowires grow non-catalytically through the random, irregular openings in the mask layer. The PV nanowires do not grow through the remaining mask areas, but rather only through the openings. The result is photovoltaic nanowires formed in spatially random clusters over the surface, as shown in Fig. 3C.

[0066] Stated differently, there is provided what it believed to potentially be a better alternative to the patterned selective area growth (SAG) method of growing nanowires without using catalyst. In contrast to the Dapkus idea in which a dielectric pattern is provided over a crystalline surface, the nanowires growing through areas not covered by the dielectric, according to some embodiments, a very thin dielectric film with lots of "holes," such as SiO2 (say 3 to 10 nm thick or so), is deposited to serve as a random pattern over crystalline or amorphous Si surface, and the nanowires will grow in areas not covered by the "holey" film.

[0067] Notably, the PV nanowires grown in this fashion could also be encouraged to grow laterally, by changing the growth temperature and other

conditions, so that all the nanowires could become fat. It is also possible that the fat nanowires could simply grow together to form a quasi-continuous layer or film. Again, the nanowires could be made of InP, GaAs, GaN and other III-V materials. Notably, according to some embodiments, the lateral growth techniques described herein can be added to the ideas of the incorporated patent references above. There would be no need to deposit a larger catalyst grain. The nanowires could grow fat by changing the growth conditions and still have a tiny catalyst cap. The fat nanowires could again grow together to form a quasi-continuous film as described above.

[0068] A method of making III-V microwire solar cell modules compatible to silicon crystal modules will now be described, according to some embodiments. The modules can use minimally modified silicon crystal module manufacturing and handling equipment as well as fitting into the standard panels for silicon crystal modules. This is particularly important for cost and manufacturing yield considerations.

[0069] Since approximately 80% of the solar cell modules are made of silicon crystal and the costs of such manufacturing and handling equipment are well designed and proven at a much lower cost than specialized equipment for typical thin-film solar cell modules. This cost advantage also applies to the standard panels and mounting fixtures.

[0070] A typical silicon solar cell module is six-inch square (6"x6"), made from an eight-inch (8") silicon wafer. It takes approx. 43 of these modules to add up to a square meter. Thus, each silicon crystal module typically delivers 3.5W or less. Whereas, each such size (6"x6") III-V microwire solar cell module should deliver 7W. For a silicon crystal solar cell manufacturing plant of GW/year (one billion watt/year) capacity, it would have to produce 800,000 such 6"x6" modules per day x 360 days/year. If yield were 80%, then the daily run rate would be over one million modules per day.

[0071] According to one preferred embodiment, III-V microwire solar cells are fabricated according to one or more of the methods described in the above-referenced applications that are incorporated by reference herein, with the additional constraint that they are made in discrete, individually manipulable plates or sections having unit sizes that correspond to the sizes of conventional silicon

crystal wafers. The III-V microwire solar cell units or plates are formed such that they can be "substituted" in place of the conventional silicon crystal wafers in a conventional solar cell module-making process, with only relatively minor modifications to that process. The result is solar panel modules that have the general look, feel, and applicability of conventional solar panels, except that they are advantageously based on III-V microwire-based solar cell technology instead of conventional silicon crystal wafers.

[0072] Thus, for example, according to one preferred embodiment, the III-V microwire solar cell module is made on (A) 6"x6" (or similar size as crystal silicon standards change) glass or other transparent substrate, or on (B) 6"x6" non-glass opaque or metal substrate. A manufacturing process has been disclosed in the above-referenced prior disclosures. A key is to be able to use standard multi-wafer silicon crystal module manufacturing and handling equipment with minimal modifications. This would substantially reduce the equipment costs for III-V microwire solar cell modules.

[0073] An additional benefit is the yield rate will be much higher than making a much larger module than 6"x6", which most current thin-film solar cell manufacturers do. For example, Applied Material's thin-film module was recently increased from 1.4 square meters to 5.7 square meters, which is respective equivalent to 60 to 245 times the size of 6"x6" modules. For example, if the yield of a 6"x6" module is 95%, then 1.4 and 5.7 square meter modules would have respective yield of (0.95)60 = 4.6% and (0.95)245 = 0.0003%. The yield is a very important cost factor, especially during the early years of the manufacturing ramp up period.

[0074] A method of forming solar energy conversion devices with III-V photo voltaic nanowires formed on <111> crystalline silicon substrates will now be described, according to some embodiments. The embodiments are related to the teachings of WO2011/025733A1, which is incorporated by reference herein in its entirety, and is more particularly directed to III-V photovoltaic (PV) nanowire-based solar energy conversion devices. Generally speaking, the many examples set forth in WO2011/025733A1 for the growth of PV nanowires and the formation of operable photovoltaic solar panels therefrom, including methods for PV nanowire stabilization and forming operable electrode structures suitable for field use, are

applicable for contexts in which the III-V PV nanowires are formed upon substrates whose surfaces exhibit long range atomic order, such as bulk crystalline wafer substrates. According to one embodiment, it is desirable to leverage the many teachings set forth in WO2011/025733A1 for PV nanowire-based solar cell formation for a particular context in which III-V PV nanowires are grown on a highly n-type (or p-type) doped <111> crystallographic plane of a silicon wafer.

[0075] One way is to grow the PV nanowires using gold catalyst on a highly n-type doped silicon's <111> crystallographic plane of the silicon wafer. The surface could optionally buffed, reactive etched, or slightly mechanically roughened to promote the initiation of growth. Since the growth is on same crystallographic plane, the nanowires will grow more parallel to each another, which is different from the more random orientation on growing on non-crystalline surfaces covered with a layer of amorphous silicon. The growth process could still be similar to that we disclosed for growing on non-crystalline surfaces, using MOCVD for example. After growth, we can do the same atomic layer deposition passivation, fill and etch back, and deposition of p-type Si, TCL, etc. at taught in WO2011/025733A1. Alternatively, we could also dope both ends of the nanowires, p-type and n-type, as we have disclosed before in the commonly assigned U.S. 61/381,930, *supra*.

[0076] Each of the following references discusses one or more aspects of growing III-V nanowires on crystalline silicon <111> substrates, and each of the following references is incorporated by reference herein in its entirety: Bao, X., et. al., "Heteroepitaxial Growth of Vertical GaAs Nanowires on Si (111) Substrates by Metal Organic Chemical Vapor Deposition," Nano Lett. 8 (11), 3755-3760 (2008); and Mi, Z., et. al., "III-V Compound Semiconductor Nanostructures On Silicon: Epitaxial Growth, Properties, And Applications In Light Emitting Diodes And Lasers," J. Nanophotonics, Vol. 3, 031602 (23 January 2009). According to one preferred embodiment, it is desirable to form the PV nanowires such that the i-region of each nanowire is at least 0.2 μm in length.

[0077] Certain cost advantages associated with using SRAO substrates (*e.g.*, compatibility with roll-based processes, etc.) are not shared for the currently disclosed embodiment of using silicon wafers as substrates for growing the III-V PV nanowires, and therefore the costs may be higher in comparison to growing on non-crystalline surfaces. However, since the III-V nanowire PV cell described

herein inherently has much higher conversion efficiency than crystalline silicon, the resultant cost per watt will still be lower than conventional photovoltaic cells made of crystalline silicon.

[0078] Methods for fabricating nanowire-based photovoltaic solar cells on roller-based substrate material will now be described, according to some embodiments. According to some embodiments, high-efficiency solar cells are fabricated on a continuous substrate, such as a roll-to-roll based substrate. According to some embodiments crystallized III-V based solar cells are fabricated on a flexible substrate, such as roll-to-roll based substrates. According to some embodiments, PV nanowire-based solar cells are fabricated on a continuous substrate, such as a roll-to-roll based substrate. According to some embodiments, single crystalline nanostructure-based solar cells are fabricated on a continuous substrate, such as a roll-to-roll based substrate.

[0079] Aspects of the currently disclosed embodiments may be more thoroughly understood in view of the following references, each of which is incorporated by reference herein in its entirety: {19} Goto, et. al., "Growth of Core-Shell InP Nanowires for Photovoltaic Application by Selective-Area Metal Organic Vapor Phase Epitaxy," Applied Physics Express 2, 035004-1-3 (2009); {20} U.S. Patent No. 7,608,530; {21} PCT International Patent Application No. PCT/US10/46334; {22} U.S. Patent No. 7,608,530, issued October 27, 2009 to Kobayashi and Wang, entitled "Hetero-Crystalline Structure and Method of Making Same"; {23} Singh and Hartnagel, "Reduction in Surface Charge Density By New GaAs Passivation Method," J. Phys. D: Appl. Phys., Vol. 8, pp. L42-L43 (1975); and {24} Pern and Glick, "Accelerated Exposure Tests of Encapsulated Si Solar Cells and Encapsulation Materials," National Center for Photovoltaics Program Review Meeting, Denver, Colorado, Sept. 8-11, 1998, NREL/CP-520-25361 (October 1998).

[0080] Fig. 4 illustrates a cross-sectional view of a PV nanowire-based solar cell, according to some embodiments. PV nanowire-based solar cell 402 (PV nanowire-based photovoltaic energy conversion device) includes an array of PV nanowires 404. More specifically, for a preferred embodiment of Fig. 4, the array of PV nanowires 404 is sandwiched between a root-side electrode 407 and a tip-side electrode 415. The root-side electrode 407 includes an SRAO layer 410 (for

example, n-type amorphous hydrogenated silicon or a-Si:H) and a metallic layer 408 (for example, molybdenum or aluminum). The root-side electrode 407 is disposed upon a continuous substrate 406, which according to some embodiment is stainless steel. According to some embodiments, substrate 406 is taken from a roll and cell 402 is manufactured on substrate 406 as part of a roll manufacturing process. According to some embodiments, the substrate 406 is electrically conductive, and can be considered as part of the root-side electrode. Tip-side electrode 415 comprises a layer 416 of an optically transparent electrically conductive material, such as an optically transparent electrically conductive semiconductor material including p-type a-Si:H, and a transparent conductive layer (TCL) 418. Although the PV nanowires 404 are shown as having rectangular cross-sections, they can likewise have a nanoneedle character, without departing from the scope of the preferred embodiments. According to some embodiments, a solid layer 414 of transparent insulating filler material is disposed in the space between the root-side electrode 407 and tip-side electrode 415, but it does not fill all of the air space among the PV nanowires 404, whereby there is an air gap layer 412 disposed between an inwardly facing surface 414i of the solid filler layer 414 and the root-side electrode 407. The tip ends of the PV nanowires 404 jut outwardly beyond an outwardly facing surface 414o of the solid filler layer 414 into physical and electrical contact with the tip-side electrode layer 415.

[0081] The design of Fig. 4 can be advantageous in reducing the adverse effects, such as absorption, heating, and darkening over time, that would be brought about by an insulator material that fully extends over the lengths of the PV nanowires, while at the same time providing good lateral stabilization of the PV nanowires and providing a stable platform upon which to fabricate the tip-side electrode layers of the device. Additionally, by the juttable extension of the tip ends of the PV nanowires 404 beyond the outwardly facing surface 414o of the solid filler layer 414 and well into the material of the tip-side electrode layer 415, superior electrical contact with the tip-side electrode layer 415 is achieved for promoting superior overall performance.

[0082] According to some embodiments, the air gap 412 occupies at least twenty-five percent of the vertical space between the solid filler layer 414 and the root-side electrode 407. For another preferred embodiment, the air gap 412

occupies at least fifty percent of the vertical space between the solid filler layer 414 and the root-side electrode 407. For another preferred embodiment, the air gap 412 occupies at least seventy-five percent of the vertical space between the solid filler layer 414 and the root-side electrode 407. Notably, in view of the material characteristics of the solid filler layer 414 (optically transparent, electrically insulating), it is not required that the air gap 412 be provided over one hundred percent of the lateral extent of the root-side electrode 407, because the device would still be substantially operable in the event there is contact between portions of the solid filler layer 414, although the advantages of the air gap would not be enjoyed at those contact locations. Accordingly, some drooping or sagging of the solid filler layer 414 toward the root-side electrode 407 as may occur during device fabrication, including some areas of contact therebetween that are not statistically overwhelming relative to the overall lateral extent of the device, may be acceptable.

[0083] According to some embodiments, each of the PV nanowires 404 is intrinsically doped along all or substantially all of its length between the root-side electrode 407 and tip-side electrode 415, with a photovoltaic cell being formed by virtue of the p-doped layer 416 at the tip end and the n-doped layer 410 at the root end. For this preferred embodiment the nanowire array 404 acts as the i-region, that is, each PV nanowire 404 is an i-region along its entire length. As used herein, i-region refers to a semiconductor region that is an intrinsically doped semiconductor region, or a semiconductor region that is not intentionally doped, as contrasted with p-region or p-doped region (intentionally p-doped) and n-region or n-doped region (intentionally n-doped). According to some other embodiments, the tips of the PV nanowires 404 can be doped of a similar type as the corresponding electrode. For embodiments having an opaque substrate 406 such as in Figs. 4-5, the light photons enter the device from the top (tip-side) through the transparent conductive layer (TCL) 418, then through the thin (10 to 20 nm) transparent p-type electrode layer 416, and then to the array of PV nanowires 404. TCL 418 can comprise a transparent conductive oxide, such as ITO (indium tin oxide), or alternatively any of a variety of different materials known to be both conductive and transparent, preferably with more than 80% light transmission. It is to be appreciated that it is within the scope of the preferred embodiments for the described doping configurations to be reversed, for example, for the p-type

electrode layer (and p-type nanowire tips) to be at the root side of the device of Fig. 4 and n-type electrode layer (and n-type nanowire tips) to be near the tip side of the device. According to some embodiments, the cell 402 includes a protective glass layer 420 on top (*i.e.*, on the tip-side of the PV nanowire-based solar cell device).

[0084] Fig. 5 illustrates some fabrication steps of the device of Fig. 4 according to some embodiments. According to these embodiments stainless steel substrate 506 in a continuous form such as a roll is used. At step 552, the stainless steel surface can be textured or roughened, which will increase light trapping by allowing the incident light photons to back-reflect. When the PV nanowires to be grown will have high aspect ratios (greater than 20:1, for example), they will generally be naturally light trapping and so the texturing of the substrate may be less beneficial. However, when the PV nanowires to be grown will be short and stubby according to some embodiments (less than 20:1, for example), they may be less naturally light-trapping and therefore it will be more beneficial to texturize the stainless steel surface as in step 552.

[0085] At step 554, the stainless steel surface is sputtered or evaporation coated with a layer of metal 408 such as molybdenum or aluminum or other metals, the layer 408 thus also facilitates bottom electrode (root-side electrode) functionality in conjunction with the n-type electrode layer 410. The metal layer 408, on the textured substrate surface, could also reflect back into the nanowire array any transmitted photons. Also at step 554, the electrode layer 410 of n-type a-Si:H is deposited, for example by PECVD (plasma enhanced chemical vapor deposition). Also at step 554, the PV nanowires 404 are grown, such as by MOCVD (metal organic chemical vapor deposition) or CVD (chemical vapor deposition) outwardly from the electrode layer 410 with or without the need of catalysts, using for example one or more techniques discussed in U.S. Patent No. 7,608,530. The nanowires grown by such technique could allow for the design of PV nanowire arrays with better geometry. According to some embodiments, the PV nanowires 404 should have a diameter in the range of 100 to 500 nm. Broader ranges, such as 20 to 1000 nm are also usable. One particularly important feature is the cross-sectional aspect ratio of the PV nanowires 404 (ratio of length to root cross-sectional dimension). For better performance, lower aspect ratios are more

desirable, preferably in the range of 1:1 to 20:1, which is in contrast to known prior art PV nanowire aspect ratios that are much larger than 20:1.

[0086] At steps 556-558, the layer 414 of optically transparent, electrically insulating solid filler material is formed that laterally surrounds the PV nanowires 404 along a portion of their lengths, wherein the forming is carried out such that (i) the air gap 412 remains between the root-side electrode 407 and an inwardly facing surface 414i of the solid filler layer 414, and (ii) the tip ends of the PV nanowires 104 are juttedly exposed beyond an outwardly facing surface 414o of the solid filler layer 414. At step 556, the optically transparent, electrically insulating solid filler material is applied, such as by spaying or injecting via inkjet. For one preferred embodiment, the filler material comprises a spray-coating material, such as spray-on glass, that is applied to the top of the PV nanowire array via one or more sprayer heads. Note that according to some preferred embodiments, the filler material is sprayed on such that the air gap 412 remains. At step 558, the solid filler layer 414 is subject to a dry etch, such as with O_2 plasma, so that most of the PV nanowires 404 jut outwardly from the outward surface 414o of the solid filler layer 414 and are available to make good physical and electrical contact with the tip-side electrode layer 415. Since the PV nanowires 404 are less affected by the etching, their tip ends look much like stubble or whiskers sticking out of the solid filler layer 414.

[0087] Notably, a variety of different materials for the solid filler layer 414 and methods for achieving the result of steps 556-558 are within the scope of the preferred embodiments. For example, the solid filler layer 414 can alternatively comprise one or more of Si oxides, Si nitrides, Al oxide, Al nitride, or other materials that are optically transparent and electrically insulating. According to some embodiments, the depth space between the PV nanowires is left partially unfilled, thereby leaving the air gap 412. In this way, the filler material will not absorb substantial amounts of the incident photons before reaching the i-region of the PV nanowires. An optically transparent, electrically insulating filler material that is somewhat phobic to the PV nanowires so that it does not "wet" well to the nanowires may be preferred. Advantageously, upon completion of step 558, the outwardly facing surface 414o of the solid filler layer 414 is available as a stable platform for the formation of the tip-side electrode layers 416 and 418. As used

herein, the term "layer" should not be construed as limiting such item to a single material, but rather a layer recited herein such as the solid filler layer 414, the passivation layer 656 (in Fig. 6), root-side electrode layer 407, or tip-side electrode layer 415 can comprise multiple sublayers of different materials.

[0088] At step 560, for this preferred embodiment, a p-type layer 416 of amorphous Si:H is deposited on the outwardly facing surface 414o of the solid filler layer 414 by a PECVD process. Finally, at step 562, the TCL 418 (transparent conductive layer) is deposited. There are a number of well-known materials that can be used for the TCL 418 that are suitable in photovoltaic cells, such as SnO (tin oxide), indium-tin oxides (ITO), ZnO, etc., as well as non-oxide materials that are substantially conductive and substantially transparent.

[0089] In another preferred embodiment as will be discussed further *infra*, before forming the solid filler layer 414, an atomic layer of Si oxide or Al oxide is deposited onto the nanowires to coat the PV nanowires using atomic layer deposition method for passivating the surfaces of the PV nanowires and increasing overall efficiency.

[0090] Presented by way of example, and not by way of limitation, are typical dimensions and materials for the various layers of the PV nanowire-based solar cell 402 of Fig. 4. The metal layer 408 will typically be greater than 100 nm thick and comprise a metal and/or metallic alloy such as Mo, Cr, NiSi, etc. The n-electrode layer 410 will typically be n-type a-Si:H (B doped a-Si-H, etc.) having a thickness greater than 50 nm. The PV nanowires 404, which have the preferred dimensions and aspect ratios described *supra*, can comprise Group IV, II-VI, or III-V semiconductors and related alloys. For one preferred embodiment, the nanowires 404 will have lengths and diameters of about 10 nm or greater, again so as preferably to keep their aspect ratios low to make their surface area to volume ratios low. The p-electrode layer 416 will typically have a thickness greater than 10 nm and may comprise wide bandgap non-single-crystal semiconductors such as p-type a-Si:H, p-type mc-Si:H, p-type SiC, etc. The TCL 418 will typically have a thickness greater than about 500 nm and will preferably comprise a wide bandgap transparent semiconductor (ITO, ZNO, etc.). The PV nanowire-based solar cell 402 will also comprise a mesh-style electrode layer (not shown in Fig. 4) atop the TCL 418, the mesh-style electrode layer being optimally designed to provide

electrical connectivity to the various areas of TCL 418, while at the same time not covering too much lateral area so as to allow most of the incident light to pass through to the TCL 418 and the underlying layers.

[0091] Fig. 6 illustrates fabrication of a PV nanowire-based solar cell according to some embodiments. At step 602, PV nanowires 652 are formed upon a continuous substrate 654, such as stainless steel from a roll source. The substrate 654 includes a root-side electrode structure (not shown) including an SRAO surface (not shown) similar to those described above from which the PV nanowires 652 are grown, these elements being omitted from the present description for clarity of disclosure. PV nanowires amenable to passivation methods according to one or more of the preferred embodiments can be formed upon substrates that exhibit long-range atomic order, substrates having SRAO material surfaces, or other suitable substrates.

[0092] At step 604, the PV nanowires 652 are passivated by forming a passivation layer 656 (which may itself comprise multiple individual passivation layers) on each individual PV nanowire 652. The passivation layer 656 can be formed using methods including, but not limited to, atomic layer deposition. Atomic layer deposition can be particularly advantageous for randomly oriented ensembles of nanowires with high aspect ratio for which conventional chemical vapor deposition may not be sufficiently functional. Atomic layer deposition will provide conformal deposition that uniformly covers complicated geometrical surfaces resulting from randomly oriented ensembles of nanowires. Suitable materials for the passivation layer 656 include, but are not limited to, aluminum oxide, tin oxide, titanium oxide, silicon oxide and certain nitrides. In one preferred embodiment for which the PV nanowires 652 are formed from InP material, the passivation process comprises depositing a thin layer of SiO_2 on the PV nanowires 652 by placing the assembly in an atomic layer deposition reactor and introducing two precursors containing silicon and oxygen that react spontaneously even at room temperature. Prior to the deposition of a passivation layer, the surfaces of the PV nanowires 652 could be chemically pretreated to saturate dangling bonds on the surface. For instance, a process that employs chemicals that contain sulfur using ammonium sulfide was found very effective way to reduce adverse surface effects as described in Iyer, R., "Sulfur as a Surface Passivation for InP," Appl. Phys. Lett. 53

(2) (1988), which is incorporated by reference herein in its entirety. However, an ensemble of nanowires is inherently hydrophobic, thus a surface treatment based on solution will not work as uniformly on all nanowires within an ensemble. Instead, it is more preferable to place a small amount of solid sulfur in atomic layer deposition reaction chamber during the deposition of a passivation layer. The sulfur pretreatment process serves to protect, or at least stabilize, the surface of the PV nanowires 652 against thermal degradation during the deposition of a passivation layer.

[0093] Subsequent to the passivation of the PV nanowires 552 at step 604, the remainder of the solar cell fabrication process can proceed according to one or more methods described above with respect to Fig. 5. The remainder of steps of Fig. 6 are similar to the latter steps of the fabrication method of Fig. 5 that results in the device of Fig. 4. At step 606, a layer of substantially transparent insulating filler material 658 is applied, preferably in a manner that leaves an air gap 660. At step 608, the filler layer 658 is subject to a dry etch, such as with O_2 plasma. Since the PV nanowires 652 are less affected by the dry etch, the appearance is much like whiskers sticking out of the transparent insulating filler 658. Advantageously, a significant longitudinal portion of the PV nanowires 652 are now available to make electrical contact with the top layers, rather than just the top tips of the PV nanowires. In addition to etching back the filler material 658, the dry etch step 608 should also serve to etch back the passivation layer 656 above the surface of the filler material 658 so to expose the tips and upper sidewalls of the PV nanowires 652, to facilitate electrical contact with the subsequently applied p-type layer of amorphous Si:H. At step 612, the p-type layer 662 of amorphous Si:H is deposited on the filler layer by PECVD process. Advantageously, by virtue of the etching step 608, a better ohmic contact is established between each PV nanowire 652 and the a-Si:H layer 662, since the a-Si:H layer 662 now can make substantial contact with the upper side walls of the PV nanowires 652 rather than just the very tips of the PV nanowires 652. Finally, at step 614, a transparent conductive layer 664 *(e.g.*, comprising tin oxide, indium-tin oxides, zinc oxide, or other substantially conductive and substantially transparent material) is formed above the Si:H layer 662.

[0094] Conventional uses of a passivation layer on a semiconductor surface is rather passive in the sense that electronic states associated with the presence of a surface are inactivated so that they do not contribute to the electrical transport properties of bulk semiconductor underneath the surface. In contrast, within our frame work of passivation of PV nanowires, we explicitly control the electrical transport properties of PV nanowires by tuning the electronic structures established between a passivation layer and a semiconductor surface.

[0095] Explicit control of the electronic structures can be established between a passivation layer and a semiconductor surface by controlling, for instance, bandgap of a passivation layer or the density of built-in ionized impurities in a passivation layer, which can be very advantageous for PV nanowires. Unlike a semiconductor surface that exists on a bulk semiconductor that has infinite thickness, the diameter of a nanowire is very small, thus an electronic band that deforms at the surface of a nanowire can be interacted inside of a nanowire. As a result, photo-generated excess electron and holes can be confined either near the center of a nanowire or near the surface of a nanowire. The band bending at the surface of a nanowire can be intentionally controlled by, for instance, having a passivation layer contain either negatively or positively charged ions.

[0096] In the PV structure that employs PV nanowires described hereinabove, all nanowires in an ensemble of nanowires have a built-in electric field parallel to the long axis of nanowires, thus, charged carriers confined near the center of a nanowire can be swept away by drift without getting scattered at the surface of a nanowire while charged carriers confined near the surface of a nanowire will be swept away by drift in quasi-two dimensional channel (i.e., two-dimensional electron or hole gas), which improves overall PV properties.

[0097] The term "micro-wires" or "microwires" can be used to refer to the PV nanowires 652 where their root dimensions approach the order of hundreds of nanometers.

[0098] Fig. 7 is a block diagram showing stations of a continuous substrate roll manufacturing process for fabricating PV nanowire-based solar cells, according to some embodiments. According to some embodiments, each station has the same length and the process is carried out at each station while the substrate is stationary. Following a set amount of time, for example 5 minutes, the processes

at each station are complete and the substrate is advanced and stopped such that the portion of substrate that was processed by the previous station is aligned for processing at the following station. Through this start-stop process of indexed advancements, the PV nanowire based solar cells are fabricated on a continuous substrate such as rolled stainless steel.

[0099] At station 710, the root side electrode is deposited. Station 710 corresponds to part of step 554 in Fig. 5 in which a layer of metal such as molybdenum or aluminum or other metals form a part or all of the root side electrode. According to some embodiments, the processing temperature is about 250°C. Prior to station 710, a pre-heating station may be used to raise the temperature from room temperature to close to 250°C. At station 712 an amorphous silicon, for example n-type, is formed via a PECVD process at approximately 250°C, which also corresponds to part of step 554 in Fig. 5.

[00100] At station 714, the substrate is actively cooled in preparation for the application of micro-particles used as a catalyst for nanowire growth. The active cooling can be, for example, by convection with a gas such as helium gas and/or conduction such as with cooling rollers as will be described in further detail herein. At station 716, a catalyst material such as gold or titanium is deposited at a large number of spots, with each spot being a location at which a nanowire will be grown. According to some embodiments, gold suspended in a suitable organic solvent is sprayed on the substrate so as to uniformly distribute the nano particles of gold. According to some embodiments, the spray on catalyst can be performed at about 150°C. At station 718, the substrate is heated in preparation for the nanowire growth process. Heating can be carried out, for example using convection, conduction via heated rollers as is described in further detail herein and/or radiation such as with IR lamps as is known in rapid thermal annealing processes.

[00101] At station 720, the nanowires are grown at temperatures of about 450°C. Station 720 corresponds with part of step 554 in Fig. 5 and with step 602 in Fig. 6. Precursor gases, including the elements or compounds that will form the nanowires, are introduced into a chamber. Under the influence of the catalyst, the precursor gases at least partially decompose into their respective elements, some of which are transported on or through the catalyst in liquified phase to the immediately underlying solid surface provided by the substrate. At each spot, a

nanowire epitaxially grows outwardly from the substrate as the process proceeds, the catalyst at each spot remaining at the tip of the nanowire and rising away from surface of the substrate as the nanowire grows. The resultant nanowires exhibit a long-range atomic order (i.e., single-crystal) that can potentially be exploited for a variety of different useful applications.

[00102] By way of example, the VLS synthesis process can be carried out in a metalorganic chemical vapor deposition (MOCVD) process, which is sometimes alternatively termed a metalorganic vapor phase epitaxy (MOVPE) process, an organometallic vapor phase epitaxy (OMVPE) process, or an organometallic chemical vapor deposition (OMCVD) process. Exemplary precursors for InP nanowires can be trimethylindium ($(CH_3)_3In$) and phosphine (PH_3). During a first phase of nanowire growth corresponding to the root region, n-type doping can be achieved during the MOCVD process by introducing an Si-containing gas, such as silane (SiH_4), or other suitable n-dopant. During a second phase of nanowire growth corresponding to the intrinsic region, no dopants would be introduced. During a third root region phase of nanowire growth corresponding to the tip region, p-type doping can be achieved during the MOCVD process by introducing a metalorganic vapor containing Zn, or other p-type dopants such as Be in a Be-containing metalorganic vapor. In other preferred embodiments, the PV nanowires can comprise another III-V material such as GaAs, together with suitable associated complementary dopants for the root and tip ends.

[00103] A variety of different material systems and doping schemes for the PV nanowires are generally within the scope of the preferred embodiments. According to some embodiments, the root ends of the PV nanowires correspond to the n-doped side of the device, while the tip ends correspond to the p-doped side of the device.

[00104] It has been found particularly advantageous for the PV nanowires to comprise high-purity intrinsic InP along most or all of their vertical height (length). Thus, according to some embodiments, in which these InP nanowires have root diameters in the range of 400 nm – 750 nm, aspect ratios in the range of 2.0 – 5.0, and therefore nanowire lengths in the range of 0.8 μm – 3.75 μm, high-purity intrinsic InP extends along most or all of the 0.8 μm – 3.75 μm length of the nanowire. The photovoltaic character of the overall device is provided by virtue of

the tip-side p-i junctions formed with the p-doped a-Si:H layer at the tip end, and the root-side i-n junctions formed with the n-doped a-Si:H layer at the root end.

[00105] At station 722, the substrate is actively cooled in preparation for the application of the passivation layer. The active cooling can be, for example, by convection with a gas such as helium gas and/or conduction such as with cooling rollers as will be described in further detail herein. At station 724, a passivation layer of a material such as aluminum oxide, tin oxide, titanium oxide, silicon oxide or other nitride is applied via atomic layer deposition. The passivation layer can be deposited, using atomic layer deposition at range of temperatures from about room temperature to about 400°C. According to some embodiments a temperature of about 250°C so as to minimize the need to heat and/or cool the substrate in subsequent processing steps. Station 724 corresponds with step 604 in Fig. 6.

[00106] At station 728, the substrate is heated or cooled in preparation for the application of the filler layer. At station 730, the filler material is applied preferably using a spray-coating material, such as spray-on glass. The filler material is uniformly applied to the top of the PV nanowire array via one or more sprayer heads in station 730. Station 730 corresponds to step 556 in Fig. 5 and to step 606 in Fig. 6. The liquid used in station 730 can be similar or identical to known spin-on glass formulations. However, due to the highly viscous nature of many such liquids, a higher application temperature is preferred when spraying on rather than spinning on the glass. According to some embodiments, filler material may be applied at a temperature of about 250°C so as to lower the viscosity of the filler material and also to minimize the need to heat and/or cool the substrate in subsequent processing steps. At station 732, the substrate is heated or cooled in preparation for the etching step. Note that in the case where stations 724, 730 and 734 are all carried out at close to 250°C, the additional heating/cooling stations 728 and 732 can be eliminated. At station 734, the filler layer is subject to a dry etch, such as with O2 plasma, at approximately 250°C. Station 734 corresponds to step 558 in Fig. 5 and to step 608 in Fig. 6.

[00107] At station 736, a p-type layer of amorphous Si:H is deposited on the solid filler layer by a PECVD process at approximately 250°C. Station 736 corresponds to step 560 in Fig. 5 and to step 612 in Fig. 6. At station 738, the TCL (transparent conductive layer) is deposited at approximately 250°C. There are a

number of well-known materials that can be used for the TCL that are suitable in photovoltaic cells, such as SnO (tin oxide), indium-tin oxides (ITO), ZnO, etc., as well as non-oxide materials that are substantially conductive and substantially transparent. Station 738 corresponds to step 562 in Fig. 5 and to step 614 in Fig. 6. At station 740, a metal layer is sputter deposited to create one or more metal electrodes on the tip side. Since the metal electrode will block light from entering the cell, the shape of the metal should be designed, such as a grid-pattern, so as to minimize the amount of surface area covered.

[00108] Figs. 8A-B schematically illustrate roll-based continuous substrate manufacturing processes for PV nanowire-based solar cells, according to some embodiments. In Fig. 8A, the roll-based fabrication line 800 is shown that includes a large continuous substrate 842 that passes through a number of processing stations such as those described with respect to Fig. 7. According to some embodiments, substrate 842 is thin stainless steel that is sourced from source roll 850. According to some embodiments substrate 842 is 1 meter wide and about 5 km long. According to some embodiments, each processing station processes about 1 square meter of substrate material in a stop-start fashion. The processing stations, such as stations 810, 812, 814, 838 and 840 are housed within respective housings to provide the environment (e.g. pressure, temperature and gasses) used for the particular process carried out at the station. For example, station 810, which corresponds to station 710 in Fig. 7, is used to sputter deposit the root side electrode layer at about 250°C; station 812, which corresponds to station 712 in Fig. 7 is used to form an amorphous silicon layer via a PECVD process at approximately 250°C; station 814, which corresponds to station 714 in Fig. 7 is used to actively cool the substrate 842 in preparation for the application of micro-particles used as a catalyst for the nanowire growth; station 538, which corresponds to station 738 in Fig. 7, is used deposit the TCL (transparent conductive layer) at approximately 250°C; and in station 840, which corresponds to station 740 in Fig. 7, a metal layer is sputter deposited to create one or more metal electrodes.

[00109] In Fig. 8A, the fabricated solar cells are collected on a roll 870. In the case of Fig. 8B, the fabricated solar cells are cut using cutter 880 into sheets corresponding to the size of the processing stations. In the example of each

processing station covering a 1m x 1m are of the substrate 842, for example, the cut size of sheets 882 is also 1m x 1m.

[00110] According to some embodiments, one or more buffer chambers 860 are used to collect any gases that may have leaked from the individual processing stations. The buffer chambers, such as buffer chamber 860, can be used to (1) recycle escaped gasses for subsequent use; and/or (2) collect gases for subsequent treatment to decrease the likelihood of a hazardous gas escaping into the environment. A number of rollers are provided at the entrances and exits of each processing station and to the buffer chamber(s) so as to provide sufficient impedance for gas leakage, and to prevent cross-contamination as will be described in further detail herein. The upper rollers are preferably made from a soft elastic material having low hardness so as not to damage the formed structures (e.g. the nanowires) during the fabrication process, and appropriate temperature resistance for the processes being carried out.

[00111] When operating in a start-stop processing arrangement, the stationary time allowed for processing at each station should be set according to the most time consuming process. In one example, the MOCVD nanowire growth station, such as station 720 in Fig. 7, is the most time consuming station and uses about 5 minutes. In this example, the substrate is advanced by 1 meter plus the distance between the stations and then stopped for 5 minutes, then advanced and then stopped for 5 minutes, and so on. In the case where fabrication line 800 uses a 1 meter wide substrate and 1 meter long processing stations, the throughput is approximately:

$$\frac{1\ \text{meter}^2}{5\ \text{min}} \times 60\frac{\text{min}}{\text{hr}} \times 24\frac{\text{hr}}{\text{day}} \times 365\frac{\text{days}}{\text{year}} \cong 100{,}000\ \text{m}^2/\text{year}$$

Assuming in this example, 1 square meter generates about 200 watts for 20% efficiency at 1000 watts/square meter, such a line would produce about 20 Megawatts / Year. According to some embodiments, a wider substrate media could be used, such as 2 meters wide, and the processing stations could be 2 meters long, which would produce 4 square meters per 5 minutes equaling about 80MW per year.

[00112] According to some embodiments, a continuous process could be used instead of a start-stop process.

[00113] Fig. 9 is diagram schematically illustrating a heating and/or cooling station, according to some embodiments. In Fig. 9, a heating station 918 is used to raise the temperature of the substrate 942 from the liquid spray catalyst stage 916 to the MOCVD nanowire growth stage 920. According to these embodiments, heated rollers such as rollers 910 are used to heat the substrate using conduction. the rollers can be heated for example via electric resistance coils and/or by passing heated liquid through portions of the rollers. According to some embodiments, the same type of arrangement of rollers could be used for cooling the substrate 942 via conduction in which case the rollers are cooled for example by passing a cool liquid through portions thereof.

[00114] Figs. 10A-B show cross sections of a processing chamber having a moveable lid, according to some embodiments. Processing station 1000 has an upper lid 1010 and a lower housing 1012. A start-stop process is used to fabricate PV nanowire-based solar cells on a continuous substrate 1042. The substrate 1042 is held flat in part by rollers within the chamber such as roller 1030. The portion of the substrate 1050 is where the solar cells are being fabricated. In between processing stages, when the substrate is being advanced, the moveable lid 1010 is raised by a distance d, as shown in Fig. 10A. During processing at station 1000, the lid 1010 is lowered to contact the substrate 1042 such that the processing chamber is relatively air tight between the walls of the lid 1010 and lower rollers 1020 and 1022. In this way, very little gas will escape from the chamber during processing. Prior to raising the lid 1010, the chamber can be flushed such that contaminating gases can be removed. Note that in a start-stop fabrication method, fabrication only takes place in some locations on the substrate, such as location 1050, so that contact by the wall portions of the lid 1010 will not damage any structures being fabricated.

[00115] Fig. 11 is a cross section of a processing chamber having high impedance wall section, according to some embodiments. Processing station 1100 has a wall 1110 that forms a processing chamber 1102 with slots on the left and right sides for entry and exit of a continuous substrate 1142 on which solar cells are fabricated. The substrate 1142 is held flat in part by rollers within the chamber such as roller 1130. Gas communication between the chamber 1102 and the outside 1104, which could be still within a buffer chamber, is controlled by contact

rollers 1120 and 1122 and wall sections 1112 and 1114. Wall sections 1112 and 1114 have a width w and a distance d from the surface of the substrate 1142 such that there is sufficient impedance for gas communication between the chamber 1102 and the outside 1104. According to some embodiments, station 1100 is used in a start-stop fabrication process. However, according to some embodiments, station 1100 is used in a continuous processing method in which the substrate 1142 is continuously advanced without stopping.

[00116] Fig. 12 is a cross section of a processing chamber having double rollers, according to some embodiments. Processing station 1200 has a wall 1210 that forms a processing chamber 1202 with slots on the left and right sides for entry and exit of a continuous substrate 1242 on which solar cells are fabricated. The substrate 1242 is held flat in part by rollers within the chamber such as roller 1230. Gas communication between the chamber 1202 and the outside 1204, which could be still within a buffer chamber, is controlled by contact rollers 1220, 1222, 1260 and 1262. The upper rollers 1260 and 1262 are preferably made from a soft elastic material having low hardness so as not to damage the formed structures (e.g. such as the nanowires) during the fabrication process, and appropriate temperature resistance for the processes being carried out. According to some embodiments, station 1200 is used in a start-stop fabrication process. However, according to some embodiments, station 1200 is used in a continuous processing method in which the substrate 1242 is continuously advanced without stopping.

[00117] Fig. 13 is a plan view of a processing station used to spray on nanowire catalyst material, according to some embodiments. The processing station 1300 corresponds, for example, to station 716 in Fig. 7 and is used for uniformly depositing a catalyst material such as gold or titanium is at a large number of spots on substrate 1342, with each spot being a location at which a nanowire will be grown. Processing chamber 1302 is defined by chamber wall 1310 and gas communication between the chamber 1302 and the outside, which could be a buffer chamber, is controlled by rollers such as rollers 1320 and 1322. The area 1344 on continuous substrate 1342 is where the PV solar cells are being fabricated. A spray assembly 1330 includes a wide spray head 1332 that is made up of a large number of nozzles. According to some embodiments, the nozzles are similar to inkjet nozzles used in inkjet technology. During operation, the spray

assembly 1330 is translated across fabrication area 1344 (as denoted by the arrows and small dotted lines in Fig. 13) such that the liquid spray, and therefore the suspended nano particles of catalyst material, is uniformly deposited across the area 1344.

[00118] According to some embodiments, a processing station similar to that shown in Fig. 13 is used for depositing spray on glass. In such embodiments, the nozzles 1332 in head 1330 are dimensioned and spaced according to the viscosity of the liquid being deposited.

[00119] Fig. 14 schematically illustrates a large area discrete substrate manufacturing process for PV nanowire-based solar cells, according to some embodiments. Fabrication line 1400 is similar to line 800 shown in Figs. 8A and 8B except that prior to processing, the substrate is cut into discrete pieces corresponding to the size of the processing stations. For example, according to some embodiments, the processing stations 1410, 1412, 1414, 1438 and 1440 are all 1meter x 1meter format, and the discrete substrate pieces, such as piece 1442, 1444, and 1446 are also 1m x 1m.

[00120] Fig. 15 illustrates a structure that includes a lightly n-doped PV nanowire and a more heavily doped p-type tip-side electrode material, according to some embodiments. Instead of an intrinsic PV nanowire, as described herein according to some other embodiments, the PV nanowire 1510 is intentionally lightly doped n-type (e.g. n^- type) on an n-type substrate 1520. For example, the n-type doping of PV nanowire 1510 can be intentionally doped to an impurity level in the range of 10^{14} to 10^{16} per cubic centimeter. A heavily p+ type cap 1530 is formed, which can be p+ or p++ type doping. Due to heavily doped p-type cap 1530, the tip region 1512 of the nanowire becomes p-type. Furthermore, a depletion region 1514 is caused in the lightly doped PV nanowire due to field strength and the relative doping levels. The depletion region 1514, can range in size, for example, from 0.2 microns to 3 microns. According to some embodiments, a depletion region of about 1 micron in height can result from an PV nanowire intentionally doped to an impurity level of about 10^{16} per cubic centimeter. According to some embodiments, lightly-doped PV nanowires such as the one shown in Fig. 15 can be combined with the other teachings and techniques as described herein.

[00121] Although the description herein is directed primarily to PV nanowires made of III-V compound semiconductors such as InP, the scope of the present teachings is not necessarily so limited. More generally, the PV nanowires can be composed of various combinations of elemental and compound semiconductors optimized for different spectrum ranges in the solar spectrum. The elemental semiconductors include silicon ("Si") and germanium ("Ge"), and compound semiconductors include group III-V and II-VI materials (the Roman numerals III and V representing elements in the group IIIa and Va on the periodic table). Compound semiconductors can be composed of group IIIa elements, such as Aluminum ("Al"), Gallium ("Ga"), and Indium ("In"), in combination with group Va elements, such as Nitrogen ("N"), Phosphorus ("P"), Arsenic ("As"), and Antimony ("Sb"). Compound semiconductors can be classified according the relative quantities of III and V elements. By way of example, binary compound semiconductors include GaAs, InP, InAs, GaN, and GaP; ternary compound semiconductors include $GaAs_yP_{1-y}$, where y ranges between 0 and 1; and quaternary compound semiconductors include $In_xGa_{1-x}As_yP_{1-y}$, where both x and y independently range between 0 and 1. Other types of suitable compound semiconductors include II-VI materials, the Roman numerals II and VI representing elements in group IIb and VIa on the periodic table. By way of example, CdSe, ZnSe, ZnS, and ZnO are examples of binary II-VI compound semiconductors.

[00122] In the case of using a stainless steel substrate or other non-transparent substrate, it is beneficial to optimize the filler layer, the dry etch to expose a large percentage of the micro-wires, the deposition of the a-Si layer to provide a p-type (or n-type) junction, and finally the TCL layer to optimize conductivity and optical transmissivity.

[00123] According to some embodiments, a protective encapsulation on the light incident side is provided, which consists of a sun-resistant transparent overcoat of polymer. See, for example, Pern and Glick, "Accelerated Exposure Tests of Encapsulated Si Solar Cells and Encapsulation Materials," National Center for Photovoltaics Program Review Meeting, Denver, Colorado, Sept. 8-11, 1998, NREL/CP-520-25361 (October 1998), which is incorporated by reference herein in its entirety.

[00124] Whereas many alterations and modifications of the present invention will no doubt become apparent to a person of ordinary skill in the art after having read the foregoing description, it is to be understood that the particular embodiments shown and described by way of illustration are in no way intended to be considered limiting. By way of example, in another preferred embodiment, the i-region portion of each nanowire can be made very short, and the device can be operable as a light-emitting diode (LED) rather than a photovoltaic energy generation device. Therefore, reference to the details of the preferred embodiments is not intended to limit their scope.

What is claimed is:

1. A method for fabricating a photovoltaic energy conversion device, comprising:

providing a substrate including a substrate surface layer doped in a first dopant type;

growing a plurality of photovoltaic (PV) nanowires outwardly from the substrate surface layer, each PV nanowire having a root end near said substrate surface layer and a tip end opposite said root end;

forming a layer of collar material that laterally surrounds and is in contact with the PV nanowires along at least a rootward portion of their lengths, the collar material doped in the first dopant type; and

forming a tip-side doped material doped in a second dopant type, the tip-side doped material in contact with said tip ends of the PV nanowires.

2. A method according to claim 1 wherein the layer of collar material is grown in a lateral direction from the PV nanowires.

3. A method according to claim 1 further comprising forming a layer of optically transparent, electrically insulating solid filler material that laterally surrounds the PV nanowires along an outward portion of their lengths.

4. A method according to claim 1 wherein the first dopant type is n-type and second dopant type is p-type.

5. A method according to claim 1 wherein the first dopant type is p-type and second dopant type is n-type.

6. A method according to claim 1 wherein the collar material is in contact with the substrate surface layer.

7. A method according to claim 1 wherein a longitudinal p-i-n junction is associated with each PV nanowire.

8. A method according to claim 1 wherein said growing of PV nanowires is partially carried out before said forming of the collar material and partially carried out after said forming of the collar material.

9. A method according to claim 8 wherein a gap between 0.2 microns and 5 microns is formed between an outward-most portion of the collar material a rootward most portion of the tip-side material.

10. A method according to claim 9 wherein said gap is between 0.2 microns and 2 microns.

11. A method according to claim 1 wherein the PV nanowires are not intentionally doped.

12. A method according to claim 1 wherein the PV nanowires have impurity levels less than 10^{17} per cubic centimeter.

13. A photovoltaic energy conversion device fabricated according to the method of claim A1.

14. A photovoltaic energy conversion device comprising:

a substrate including an electrically conductive substrate surface layer doped in a first dopant type;

a plurality of photovoltaic (PV) nanowires extending outwardly from the substrate surface layer, each PV nanowire having a root end near said substrate surface layer and a tip end opposite said root end, said substrate surface layer forming at least a portion of a root-side electrode layer of the device;

a collar material laterally surrounding the PV nanowires along at least a rootward portion of their lengths, the collar material doped in the first dopant type; and

a tip-side electrode material doped in a second dopant type, the tip-side electrode material being in contact with said tip ends of the PV nanowires.

15. A device according to claim 14 further comprising a layer of optically transparent, electrically insulating solid filler material laterally surrounding the PV nanowires along an outward portion of their lengths.

16. A device according to claim 14 wherein a longitudinal p-i-n junction is associated with each PV nanowire.

17. A device according to claim 14 wherein a gap between 0.2 microns and 5 microns is formed between an outward-most portion of the collar material a rootward most portion of the tip-side material.

18. A device according to claim 14 wherein the PV nanowires are not intentionally doped.

19. A method for fabricating a photovoltaic energy conversion device, comprising:

providing a substrate including an n-doped substrate surface layer;

growing a plurality of n-doped photovoltaic (PV) nanowires outwardly from the substrate surface layer, each PV nanowire having a root end near said substrate surface layer and a tip end opposite said root end;

forming a layer of optically transparent, electrically insulating solid filler material that laterally surrounds the PV nanowires along a portion of their lengths; and

forming a tip-side p-doped material in contact with said tip ends of the PV nanowires.

20. A method according to claim 19 wherein said tip-side p-doped material is p+ type doped.

21. A method according to claim 19 wherein said tip-side p-doped material is p++ type doped.

22. A method according to claim 19 wherein said n-doped PV nanowires and said tip-side p-doped material form radial and longitudinal p-n junctions.

23. A method according to claim 19 wherein said n-doped PV nanowires are intentionally lightly doped n- type to an impurity level of between 10^{14} to 10^{16} per cubic centimeter.

24. A method according to claim 19 wherein a depletion region within each n-doped PV nanowire is formed of between 0.2 and 3.0 microns in longitudinal distance.

25. A photovoltaic energy conversion device fabricated according to the method of claim C9.

26. A method for fabricating a photovoltaic energy conversion device, comprising:

providing a 6" by 6" square substrate including a substrate surface layer;

growing a plurality of photovoltaic (PV) nanowires outwardly from the square substrate surface layer, each PV nanowire having a root end near said substrate surface layer and a tip end opposite said root end;

forming a layer of optically transparent, electrically insulating solid filler material that laterally surrounds the PV nanowires along a portion of their lengths; and

forming a tip-side electrode upon said outwardly facing surface of the solid filler layer in contact with said tip ends of the PV nanowires.

27. A method according to claim 26 wherein said forming the layer of optically transparent material is carried out such that an air gap remains between the substrate surface layer and an inwardly facing surface of the solid filler layer.

28. A method according to claim 26 wherein said forming the layer of optically transparent material is carried out such that the tip ends of the PV nanowires are juttedly exposed beyond an outwardly facing surface of the solid filler layer.

29. A photovoltaic energy conversion device fabricated according to claim 26.

30. A method for fabricating a photovoltaic energy conversion device, comprising:

providing a substrate including a substrate surface layer;

forming a mask layer on the substrate surface layer, the mask having a plurality of spaced apart voids such that portions of the substrate surface layer are exposed at the locations of the voids;

growing a plurality of photovoltaic (PV) nanowires outwardly from said exposed portions of the substrate surface layer, each PV nanowire having a root end near said substrate surface layer and a tip end opposite said root end;

forming a layer of optically transparent, electrically insulating solid filler material that laterally surrounds the PV nanowires along a portion of their lengths; and

forming a tip-side electrode upon said outwardly facing surface of the solid filler layer in contact with said tip ends of the PV nanowires.

31. A method according to claim 30 wherein the voids are located randomly within the mask layer.

32. A method according to claim 30 wherein the mask layer is within a thickness range of 3 to 10 nm.

33. A photovoltaic energy conversion device fabricated according to claim 30.

34. A method for fabricating a photovoltaic energy conversion device, comprising:

providing a substrate including a long range atomic order (LRAO) substrate surface layer;

growing a plurality of n-doped photovoltaic (PV) nanowires outwardly from the LRAO substrate surface layer, each PV nanowire having a root end near said substrate surface layer and a tip end opposite said root end;

forming a layer of optically transparent, electrically insulating solid filler material that laterally surrounds the PV nanowires along a portion of their lengths; and

forming a tip-side electrode upon said outwardly facing surface of the solid filler layer in contact with said tip ends of the PV nanowires.

35. A method according to claim 34 wherein the substrate is a bulk crystalline wafer substrate.

36. A method according to claim 34 wherein the PV nanowires are III-V PV nanowires, and the LRAO substrate surface layer is a highly n-type doped <111> crystallographic plane of a silicon wafer.

37. A method according to claim 36 wherein a gold catalyst is formed upon said a highly n-type doped <111> crystallographic plane of the silicon wafer.

38. A photovoltaic energy conversion device fabricated according to claim 34.

39. A method for fabricating a photovoltaic energy conversion device, comprising:

providing a roller-based substrate material including a substrate surface layer;

growing a plurality of photovoltaic (PV) nanowires outwardly from the square substrate surface layer, each PV nanowire having a root end near said substrate surface layer and a tip end opposite said root end;

forming a layer of optically transparent, electrically insulating solid filler material that laterally surrounds the PV nanowires along a portion of their lengths; and

forming a tip-side electrode upon said outwardly facing surface of the solid filler layer in contact with said tip ends of the PV nanowires.

40. A method according to claim 39 wherein a plurality of fabrication stations are used, each station being adapted to completing a process upon a fixed length of the roller-based substrate material within a predetermined amount of time.

41. A method according to claim 39 wherein the method includes actively cooling the substrate material using rollers.

42. A method according to claim 39 wherein the method includes actively heating the substrate material using rollers.

43. A method according to claim 39 wherein the filler material is applied using a spray-coating process.

44. A method according to claim 39 wherein the roller based substrate material is at least about 1 meter wide.

45. A photovoltaic energy conversion device fabricated according to claim 39.

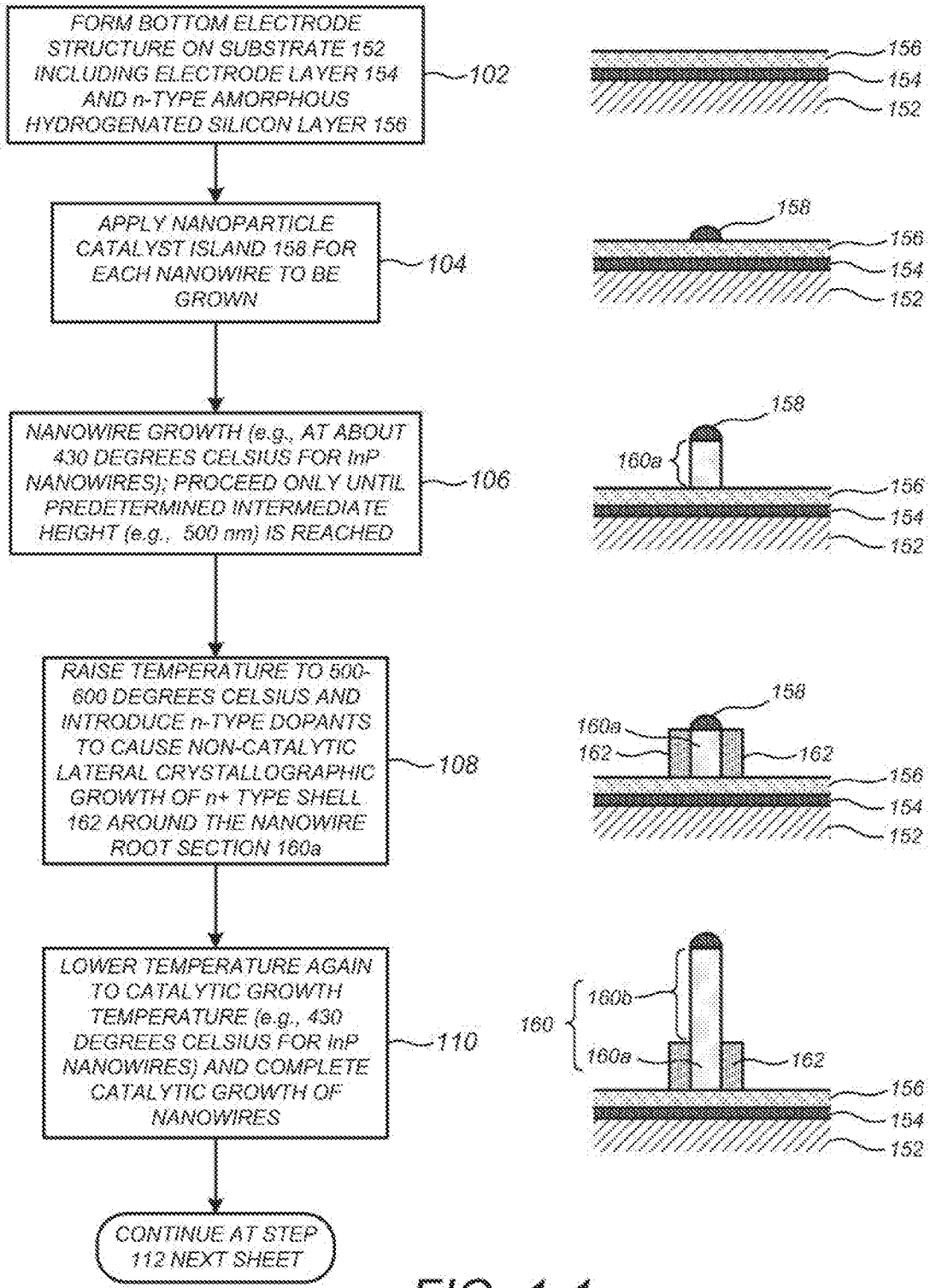
FORM BOTTOM ELECTRODE STRUCTURE ON SUBSTRATE 152 INCLUDING ELECTRODE LAYER 154 AND n-TYPE AMORPHOUS HYDROGENATED SILICON LAYER 156
102
156
154
152
APPLY NANOPARTICLE CATALYST ISLAND 158 FOR EACH NANOWIRE TO BE GROWN
104
158
156
154
152
NANOWIRE GROWTH (e.g., AT ABOUT 430 DEGREES CELSIUS FOR InP NANOWIRES); PROCEED ONLY UNTIL PREDETERMINED INTERMEDIATE HEIGHT (e.g., 500 nm) IS REACHED
106
158
160a
156
154
152
RAISE TEMPERATURE TO 500-600 DEGREES CELSIUS AND INTRODUCE n-TYPE DOPANTS TO CAUSE NON-CATALYTIC LATERAL CRYSTALLOGRAPHIC GROWTH OF n+ TYPE SHELL 162 AROUND THE NANOWIRE ROOT SECTION 160a
108
158
160a
162
162
156
154
152
LOWER TEMPERATURE AGAIN TO CATALYTIC GROWTH TEMPERATURE (e.g., 430 DEGREES CELSIUS FOR InP NANOWIRES) AND COMPLETE CATALYTIC GROWTH OF NANOWIRES
110
160
160b
160a
162
156
154
152
CONTINUE AT STEP 112 NEXT SHEET

FIG. 1-1

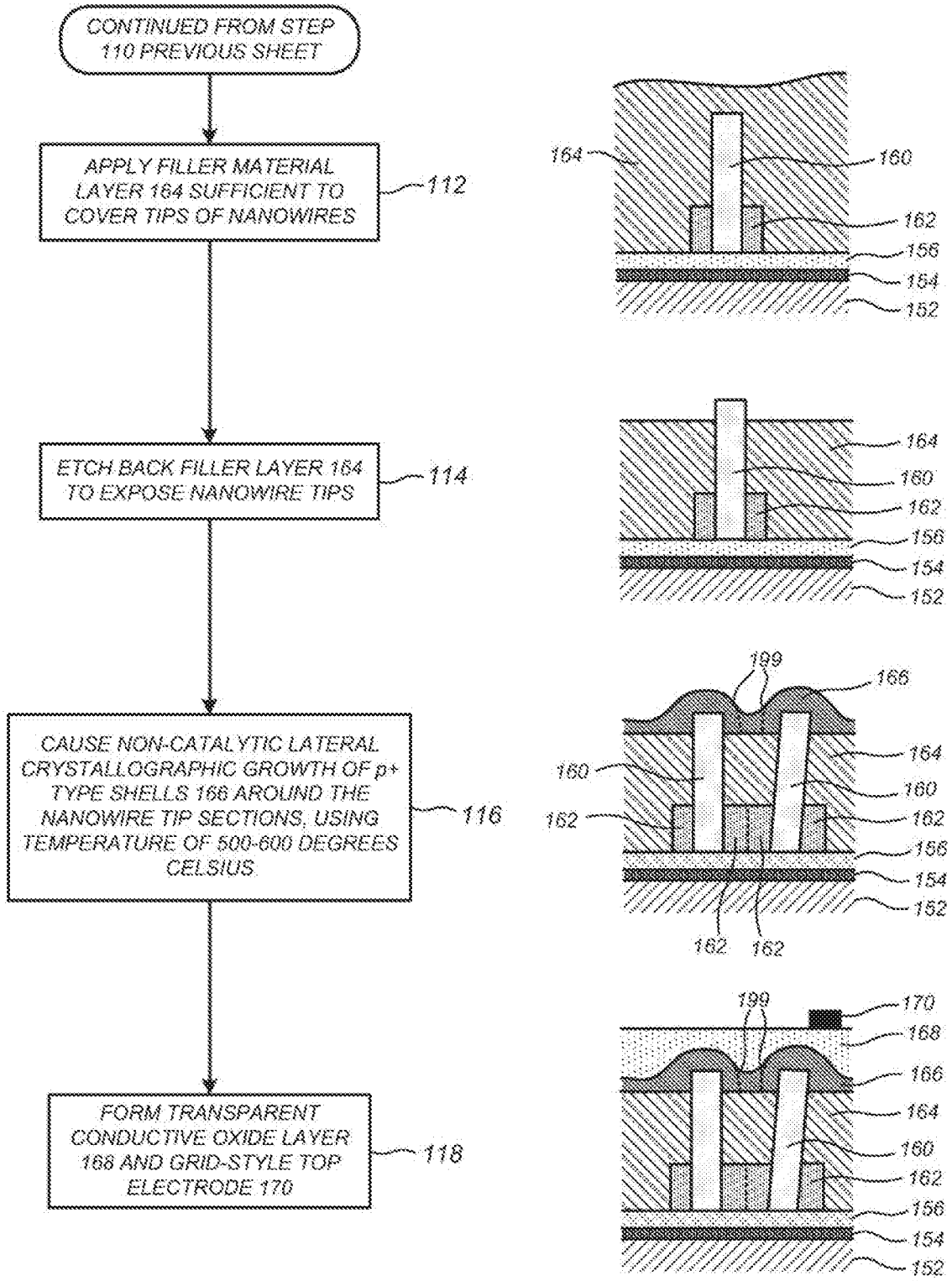
CONTINUED FROM STEP 110 PREVIOUS SHEET
APPLY FILLER MATERIAL LAYER 164 SUFFICIENT TO COVER TIPS OF NANOWIRES
112
ETCH BACK FILLER LAYER 164 TO EXPOSE NANOWIRE TIPS
114
CAUSE NON-CATALYTIC LATERAL CRYSTALLOGRAPHIC GROWTH OF p+ TYPE SHELLS 166 AROUND THE NANOWIRE TIP SECTIONS, USING TEMPERATURE OF 500-600 DEGREES CELSIUS
116
FORM TRANSPARENT CONDUCTIVE OXIDE LAYER 168 AND GRID-STYLE TOP ELECTRODE 170
118
164
160
162
156
154
152
199
166
170
168

FIG. 1-2

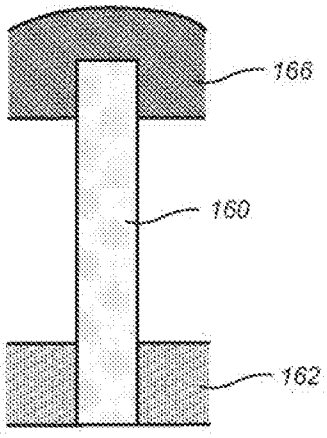

FIG. 2A

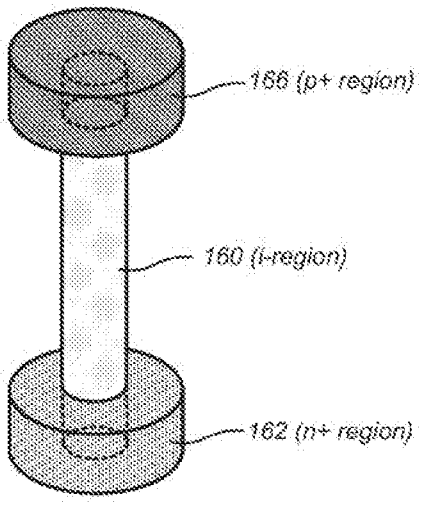

FIG. 2B

STEP 1: FORM LAYER OF n-TYPE AMORPHOUS Si

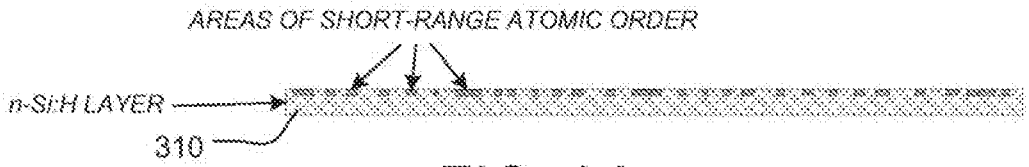

FIG. 3A

STEP 2: FORM VERY THIN MASK LAYER OF SiO2 (OR OTHER OXIDE)

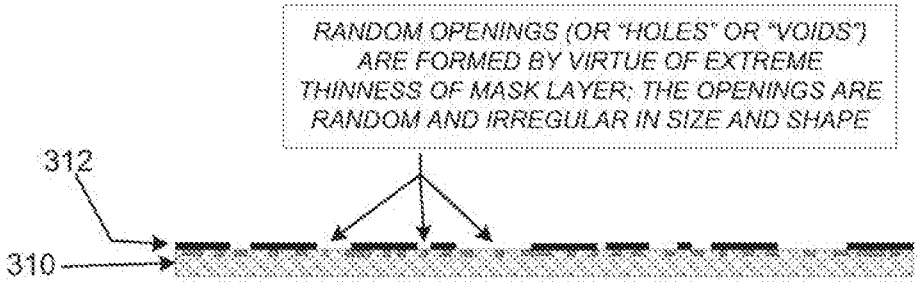

FIG. 3B

STEP 3: INTRODUCE NANOWIRE PRECURSOR GASES AT HIGH TEMPERATURE TO GROW NANOWIRES THROUGH THE RANDOM, IRREGULARLY SHAPED MASK LAYER OPENINGS

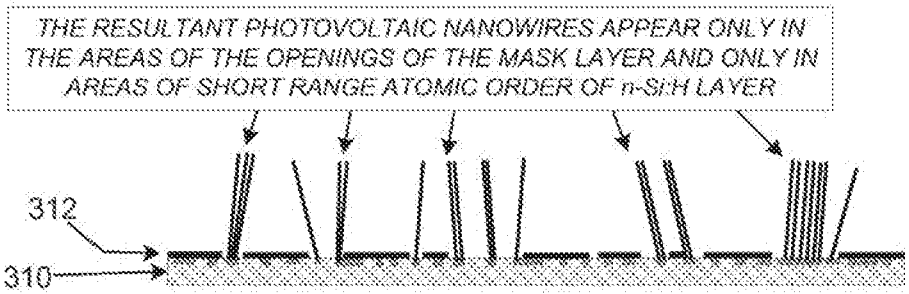

FIG. 3A

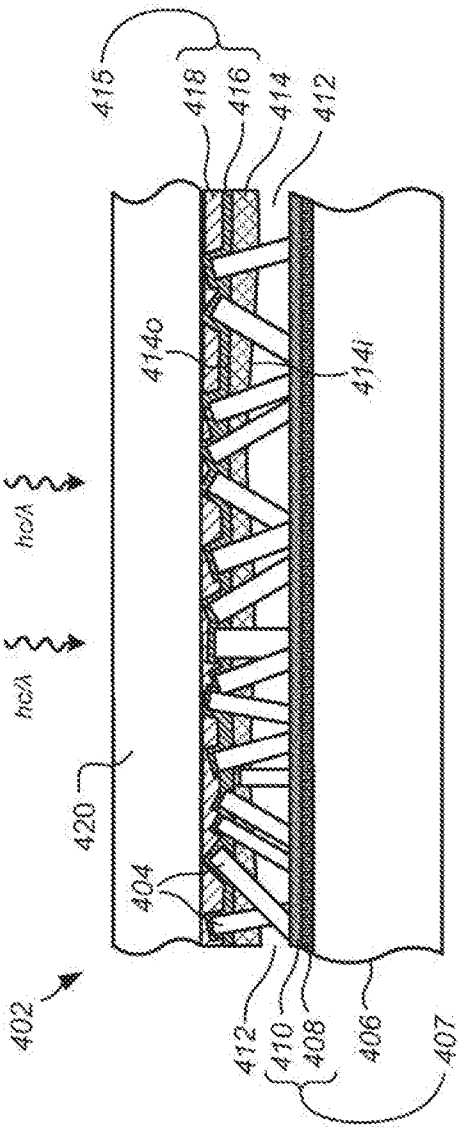
415
418
416
414
412
414o
414i
hc/λ
hc/λ
420
404
402
412
410
408
406
407

FIG. 4

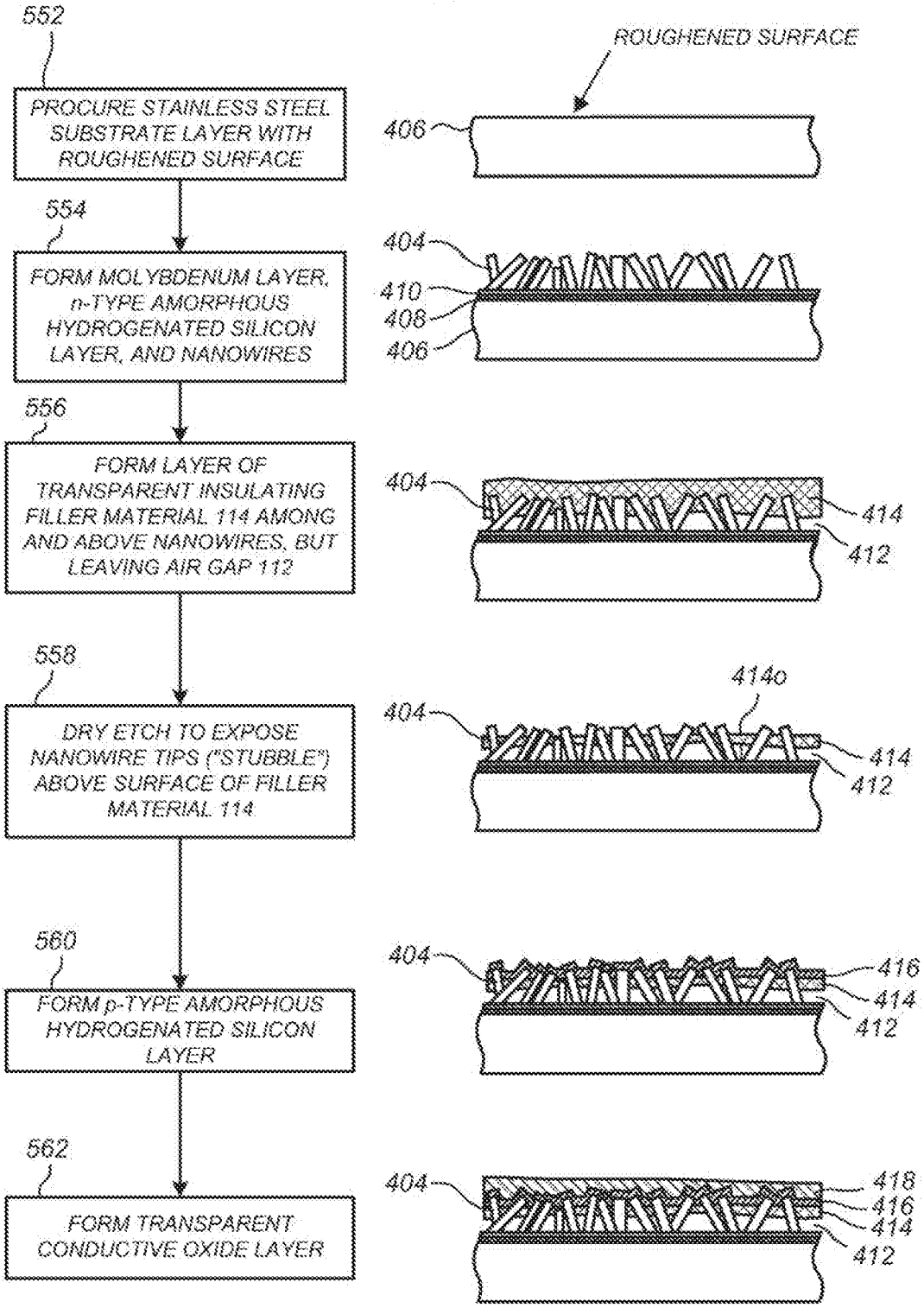
552
PROCURE STAINLESS STEEL SUBSTRATE LAYER WITH ROUGHENED SURFACE
554
FORM MOLYBDENUM LAYER, n-TYPE AMORPHOUS HYDROGENATED SILICON LAYER, AND NANOWIRES
556
FORM LAYER OF TRANSPARENT INSULATING FILLER MATERIAL 114 AMONG AND ABOVE NANOWIRES, BUT LEAVING AIR GAP 112
558
DRY ETCH TO EXPOSE NANOWIRE TIPS ("STUBBLE") ABOVE SURFACE OF FILLER MATERIAL 114
560
FORM p-TYPE AMORPHOUS HYDROGENATED SILICON LAYER
562
FORM TRANSPARENT CONDUCTIVE OXIDE LAYER
ROUGHENED SURFACE
406
404
410
408
406
404
414
412
414o
404
414
412
404
416
414
412
404
418
416
414
412

FIG. 5

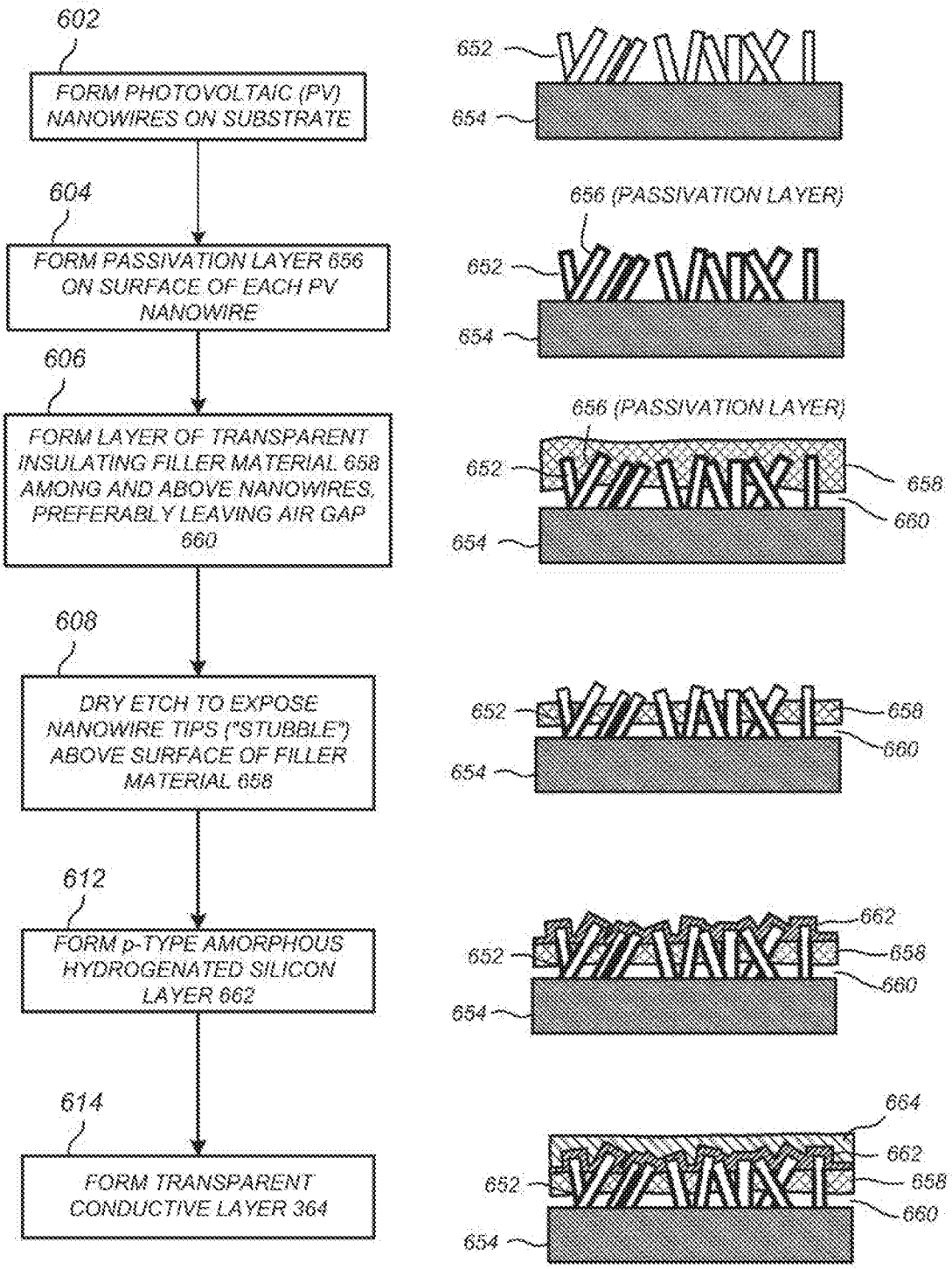
602
FORM PHOTOVOLTAIC (PV) NANOWIRES ON SUBSTRATE
604
FORM PASSIVATION LAYER 656 ON SURFACE OF EACH PV NANOWIRE
606
FORM LAYER OF TRANSPARENT INSULATING FILLER MATERIAL 658 AMONG AND ABOVE NANOWIRES, PREFERABLY LEAVING AIR GAP 660
608
DRY ETCH TO EXPOSE NANOWIRE TIPS ("STUBBLE") ABOVE SURFACE OF FILLER MATERIAL 658
612
FORM p-TYPE AMORPHOUS HYDROGENATED SILICON LAYER 662
614
FORM TRANSPARENT CONDUCTIVE LAYER 364
652
654
656 (PASSIVATION LAYER)
658
660
662
664

FIG. 6

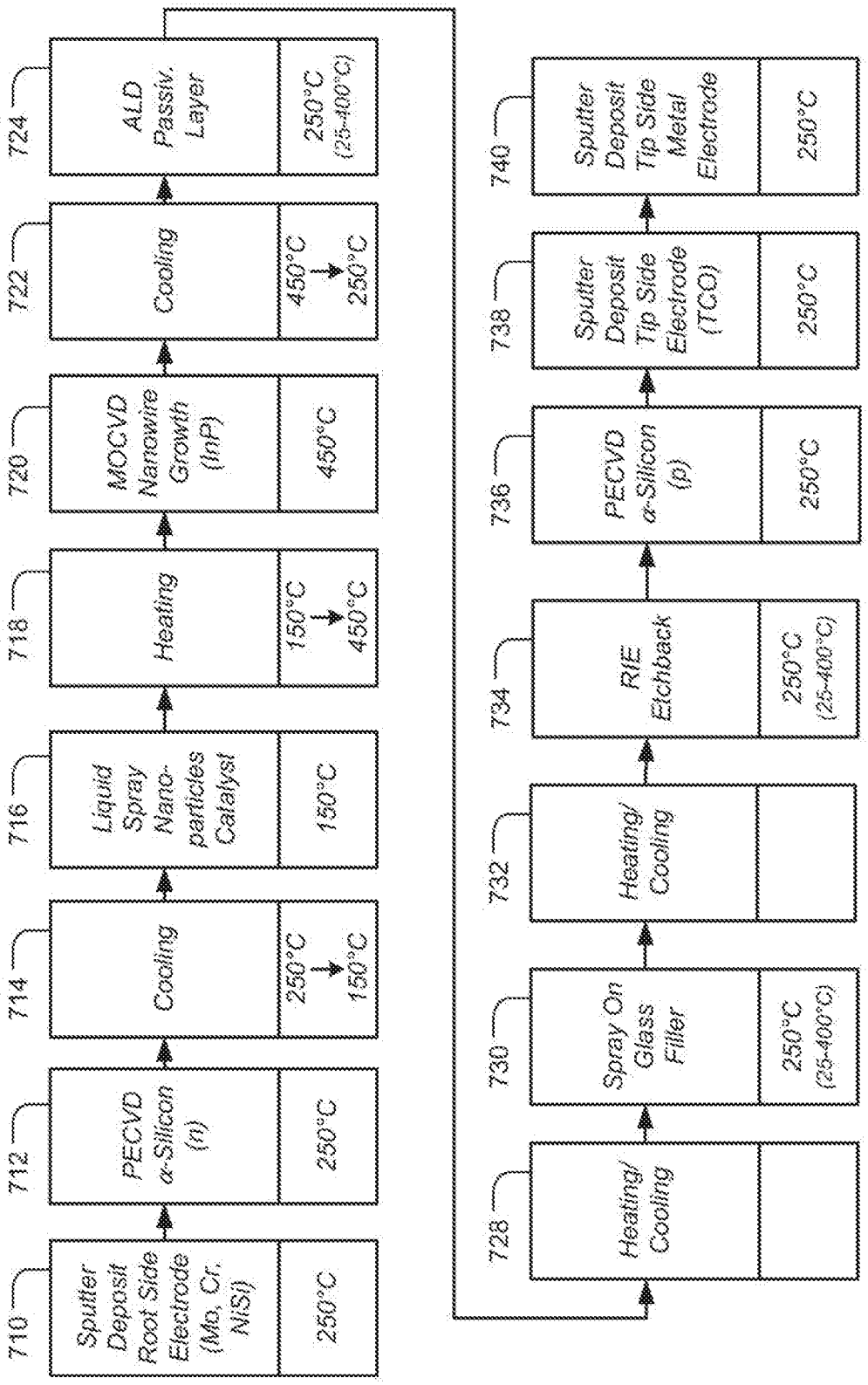
710
Sputter Deposit Root Side Electrode (Mo, Cr, NiSi)
250°C
712
PECVD α-Silicon (n)
250°C
714
Cooling
250°C → 150°C
716
Liquid Spray Nano-particles Catalyst
150°C
718
Heating
150°C → 450°C
720
MOCVD Nanowire Growth (InP)
450°C
722
Cooling
450°C → 250°C
724
ALD Passiv. Layer
250°C (25-400°C)
728
Heating/ Cooling
730
Spray On Glass Filler
250°C (25-400°C)
732
Heating/ Cooling
734
RIE Etchback
250°C (25-400°C)
736
PECVD α-Silicon (p)
250°C
738
Sputter Deposit Tip Side Electrode (TCO)
250°C
740
Sputter Deposit Tip Side Metal Electrode
250°C

FIG. 7

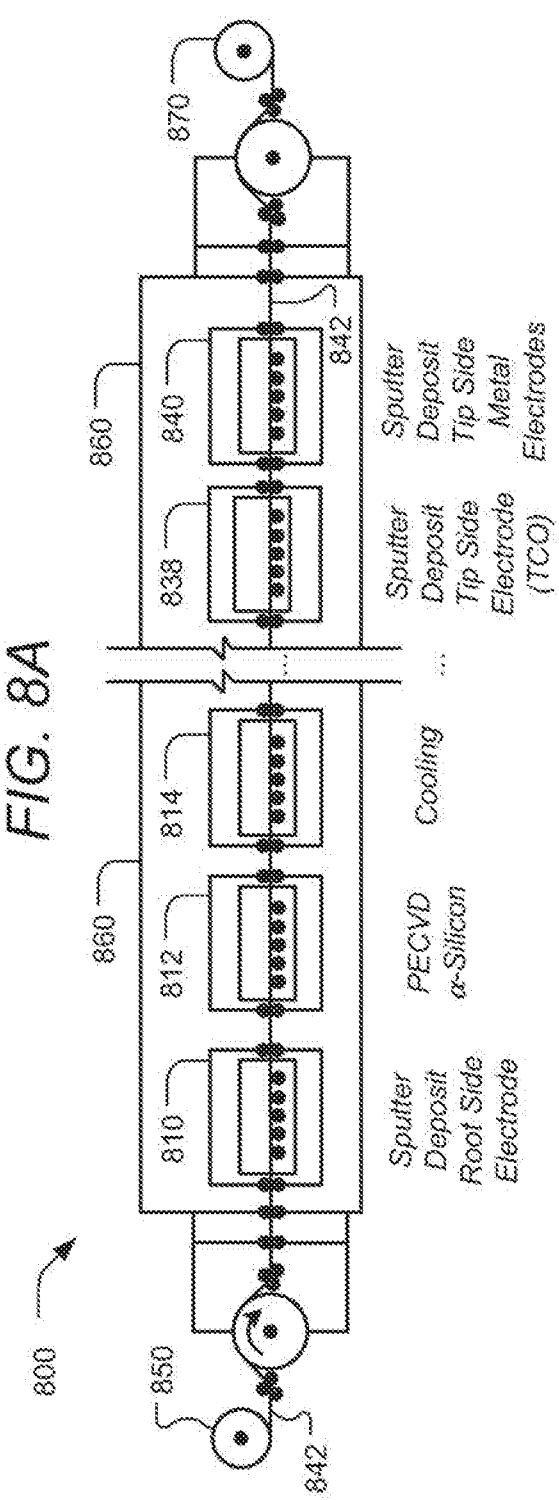

FIG. 8A

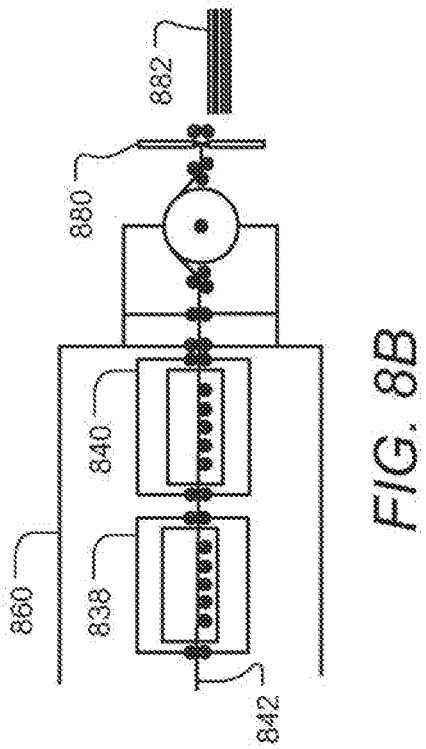

FIG. 8B

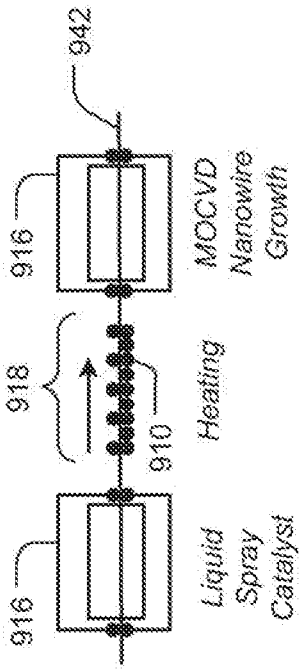

FIG. 9

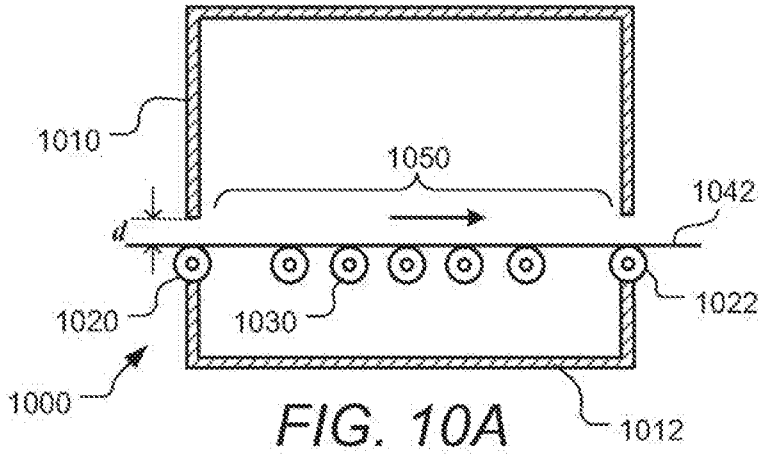

FIG. 10A

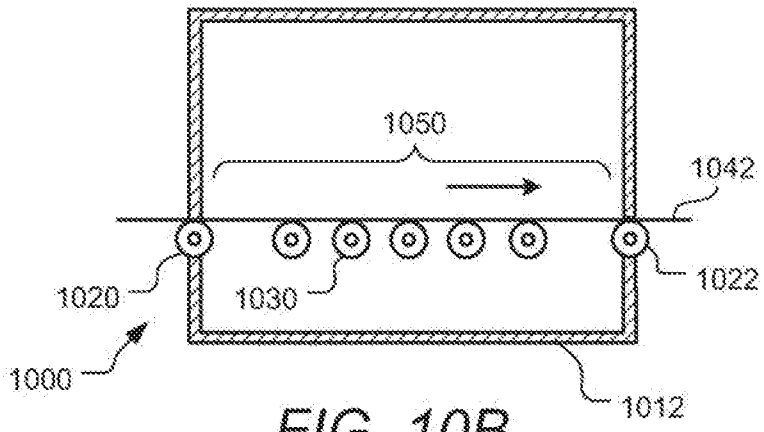

FIG. 10B

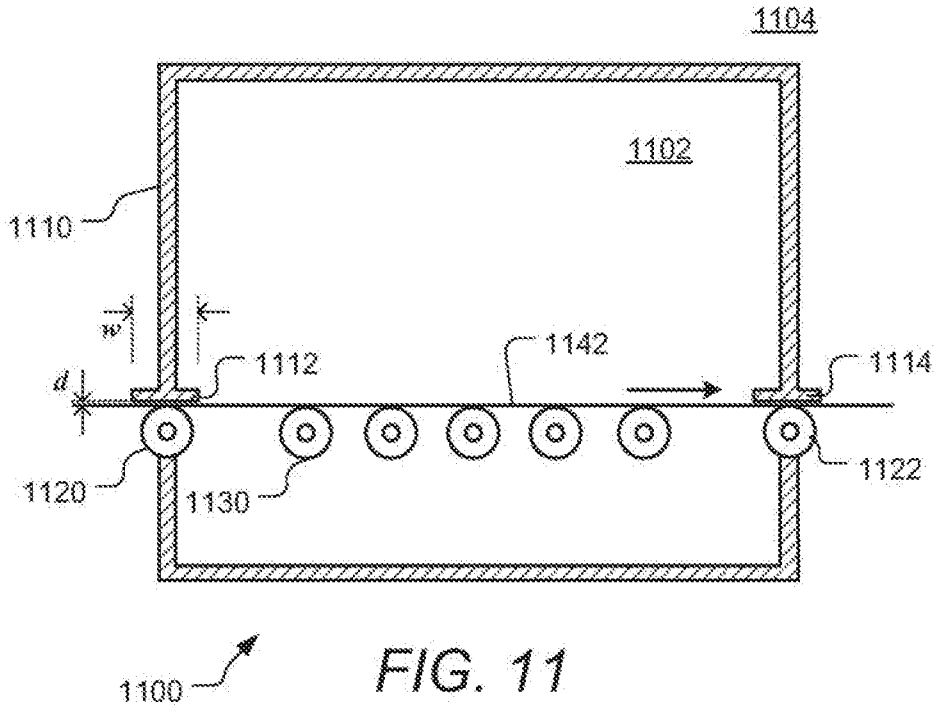
1104
1102
1110
w
d
1112
1142
1114
1120
1130
1122
1100

FIG. 11

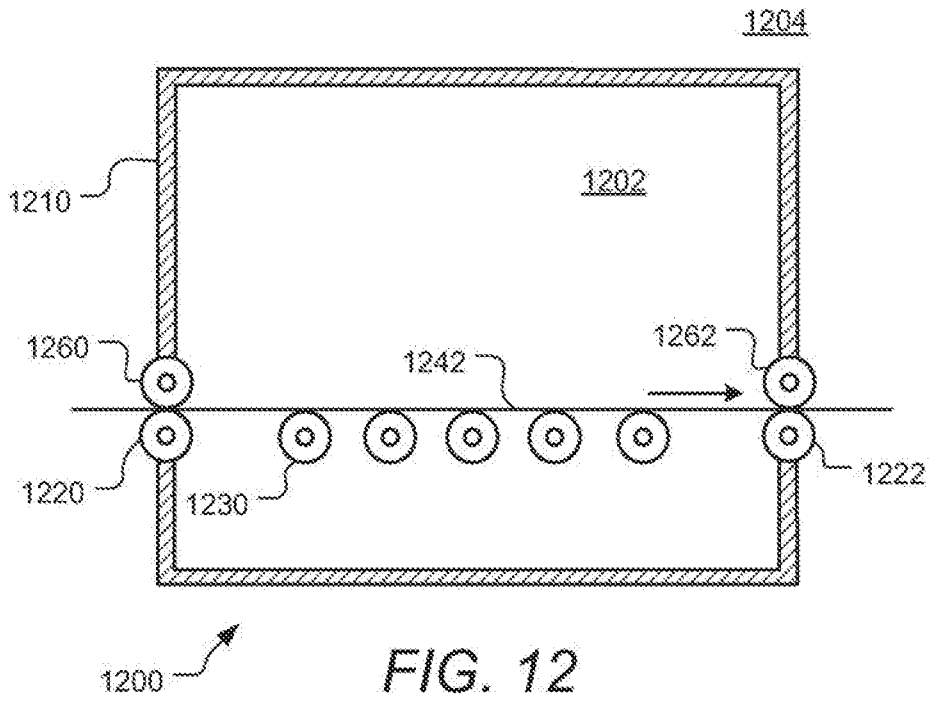
1204
1202
1210
1260
1242
1262
1220
1230
1222
1200

FIG. 12

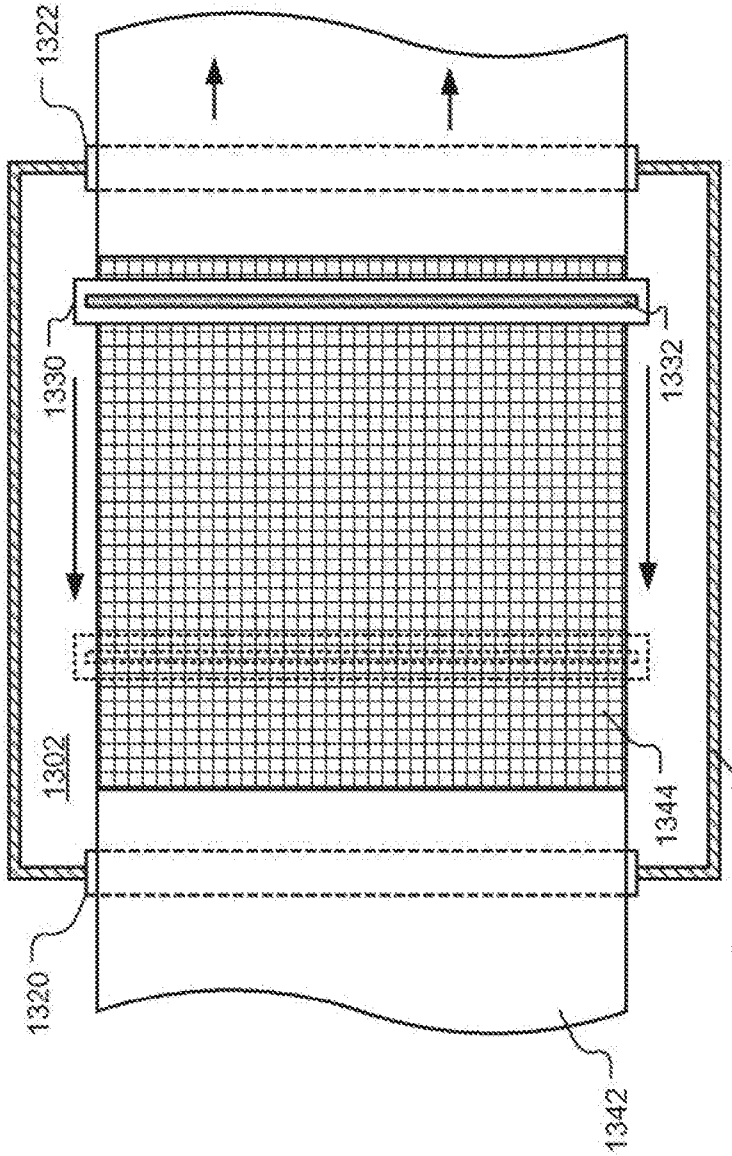

FIG. 13

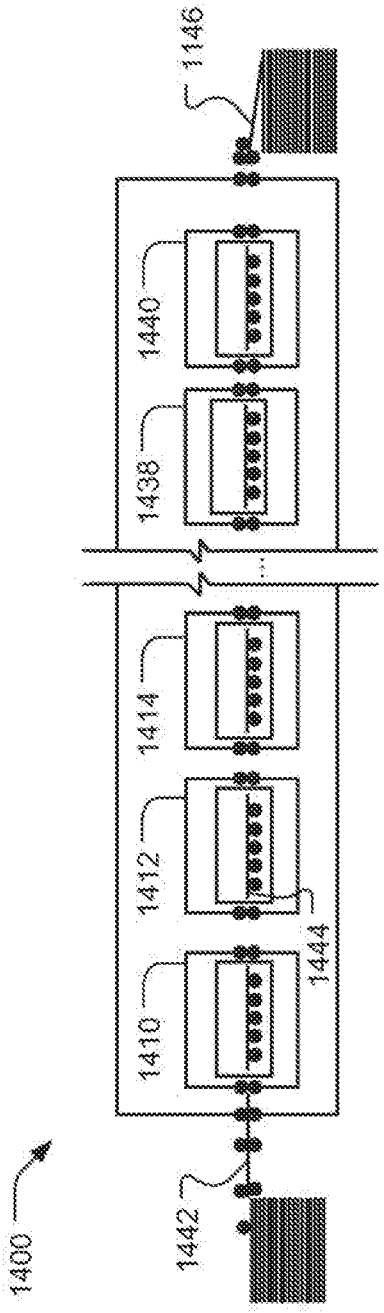

FIG. 14

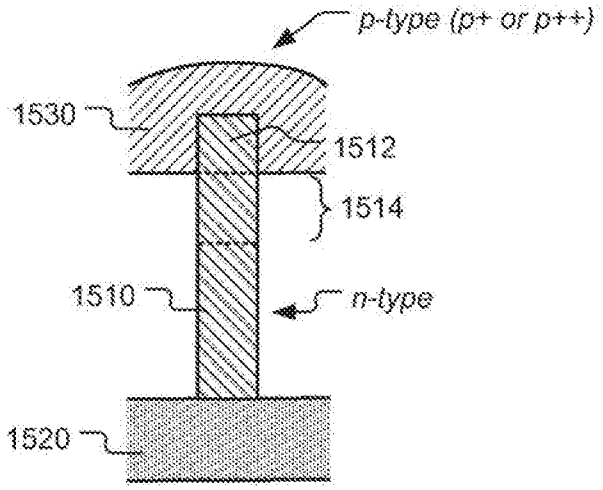

FIG. 15

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2011/061091

A. CLASSIFICATION OF SUBJECT MATTER
IPC(8) - H01L 31/00 (2011.01)
USPC - 136/255
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC(8) - H01L 31/00, H01L 31/042, and H02N 6/00 (2011.01)
USPC - 136/244, 136/251, and 136/255

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
MicroPatent, Google Patent, and ACM

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 2008/0047604 A1 (KOREVAAR et al) 28 February 2008 (28.02.2008) entire document	1-45
Y	US 2010/0193768 A1 (HABIB) 05 August 2010 (05.08.2010) entire document	1-45
Y	US 2010/0197088 A1 (POON et al) 05 August 2010 (05.08.2010) entire document	9-10 and 17
Y	US 2009/0267049 A1 (CHO et al) 29 October 2009 (29.10.2009) entire document	11, 18, 20-21
Y	US 2010/0126548 A1 (JANG et al) 27 May 2010 (27.05.2010) entire document	12
Y	US 2008/0102582 A1 (TAKEI) 01 May 2008 (01.05.2008) entire document	23, 30-33
Y	US 7,115,971 B2 (STUMBO et al) 03 October 2006 (03.10.2006) entire document	24
Y	US 2008/0265449 A1 (MEINDERS et al) 30 October 2008 (30.10.2008) entire document	32
Y	US 2007/0190434 A1 (SUDA) 16 August 2007 (16.08.2007) entire document	26-29
Y	US 2009/0188557 A1 (WANG et al) 30 July 2009 (30.07.2009) entire document	34-38
Y	US 2008/0265449 A1 (HEIDARI) 25 September 2008 (25.09.2008) entire document	39-45

☐ Further documents are listed in the continuation of Box C. ☐

* Special categories of cited documents:
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"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
09 December 2011	23 DEC 2011
Name and mailing address of the ISA/US Mail Stop PCT, Attn: ISA/US, Commissioner for Patents P.O. Box 1450, Alexandria, Virginia 22313-1450 Facsimile No. 571-273-3201	Authorized officer: Blaine R. Copenheaver PCT Helpdesk: 571-272-4300 PCT OSP: 571-272-7774

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61/843,021	4 July 2013 (04.07.2013)	US
61/905,109	15 November 2013 (15.11.2013)	US

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(74) Agent: **KAVRUKOV, Ivan, S.**; Cooper & Dunham LLP, 30 Rockefeller Plaza, 20th Floor, New York, NY 10112 (US).

(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, JP, KE, KG, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Published:

— *without international search report and to be republished upon receipt of that report (Rule 48.2(g))*

WO 2014/190189 A2

(54) **Title**: MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES

(57) **Abstract**: Techniques for enhancing the absorption of photons in semiconductors with the use of microstructures are described. The microstructures, such as pillars and/or holes, effectively increase the effective absorption length resulting in a greater absorption of the photons. Using microstructures for absorption enhancement for silicon photodiodes and silicon avalanche photodiodes can result in bandwidths in excess of 10 Gb/s at photons with wavelengths of 850 nm, and with quantum efficiencies of approximately 90% or more.

MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES

REFERENCE TO RELATED APPLICATIONS

[0001] This patent application claims the priority of and incorporates by reference each of the following applications:

U.S. Prov. Ser. No. 61/826,446 filed May 22, 2013;

U.S. Prov. Ser. No. 61/834,873 filed June 13, 2013;

U.S. Prov. Ser. No. 61/843,021 filed July 4, 2013; and

U.S. Prov. Ser. No. 61/905,109 filed November 15, 2013;

The above-referenced provisional patent applications are collectively referenced herein as "the commonly assigned incorporated applications."

FIELD

[0002] The present invention generally relates mainly to photosensitive devices. More particularly, some embodiments relate to photosensitive devices having microstructure enhanced absorption characteristics.

BACKGROUND

[0003] Fiber-optic communication is widely used in applications such as telecommunications and communication within large data centers. Because of attenuation losses associated with using shorter optical wavelengths most fiber-optic communication uses optical wavelengths of 800 nm and longer. Commonly used transmission windows exist between 1260 nm and 1675 nm. A main component of optical receivers used in fiber-optic communication system is the photo detector, usually in the form of a photodiode (PD) or avalanche photodiode (APD).

[0004] High-quality low-noise APDs can be made from silicon. However, while silicon will absorb light in the visible and near infrared range, it becomes more transparent at longer optical wavelengths. Silicon PDs and APDs can be made for optical wavelengths of 800 nm and longer by increasing the thickness of the absorption "I" region of the device. FIG. 2 is a cross section of a conventional PIN photodiode 200, where "d" is the length of the absorption "I" region 220. FIGs. 3A and 3B show bandwidth and quantum efficiency a conventional silicon photodiode

with a 30-micron diameter at 850 nm optical wavelength. As can be seen, in order to obtain a quantum efficiency of 90% the thickness "d" of the "I" region is over 30 microns. This leads to a maximum bandwidth of less than 2.5 Gb/s, which is too low for many current and future telecom and data center applications.

[0005] To avoid the inherent problem that silicon PDs and APDs have with longer wavelengths and higher bandwidths, other materials are used. Germanium (Ge) detects infrared out to a wavelength of 1700 nm, but has relatively high multiplication noise. InGaAs can detect out to longer than 1600 nm, and has less multiplication noise than Ge but still has far greater noise than silicon. InGaAs is known to be used as the absorption region of a heterostructure diode, most typically involving InP as a substrate and as a multiplication layer. This material system is compatible with an absorption window of roughly 900 to 1700 nm. However both InGaAs and Ge devices are relatively expensive and have relatively high multiplication noise when compared with silicon.

[0006] The subject matter claimed herein is not limited to embodiments that solve any specific disadvantages or that operate only in environments such as those described above. Rather, this background is only provided to illustrate one exemplary technology area where some embodiments described herein may be practiced.

SUMMARY

[0007] According to some embodiments, a photodetector with microstructure-enhanced photoabsorption is described. The photodetector (e.g. photodiode or avalanche photodiode) includes: a cathode region; an anode region; reverse biasing circuitry configured to apply a voltage between the cathode and anode regions such that the cathode region is driven to a more positive voltage than the anode region; and a microstructure-enhanced photon absorbing semiconductor region configured to absorb photons from a source signal. The absorbing region includes a plurality of microstructures that are dimensioned and positioned to increase absorption of photons at a range of wavelengths that includes a wavelength of the source signal. According to some embodiments the microstructures have at least one dimension that is equal to or shorter than a longest signal wavelength. According to some embodiments the microstructures

are pillars, holes and/or voids. The microstructures can be arranged into a periodically-spaced array, a non-periodically-spaced array, a randomly-spaced array or a multiperiodically-spaced array. According to some embodiments the microstructures have a major longitudinal axis that is normal to the upper surface of the underlying substrate material. According to some other embodiments, the microstructures have major longitudinal axes that are not parallel to one another. According to some embodiments, the microstructures are oriented so as to reduce sensitivity to any single direction of the source signal.

[0008] According to some embodiments, the microstructures increase absorption at least in part by forming an absorbing mode high contrast grating that makes use of resonance effects, scattering effects, near field effects, sub-wavelength effects, and/or interference effects.

[0009] According to some embodiments, the absorbing region and the microstructures are formed of silicon. According to some embodiments, a silicon photodiode is provided that can detect source signals at a data bandwidth of greater than 5 gigabits per second, at wavelengths of 850 nanometers with a quantum efficiency of at least 60%. According to some embodiments, a silicon photodiode is provided that can detect source signals at a data bandwidth of greater than 10 gigabits per second, at signal wavelengths of 850 nanometers with a quantum efficiency of at least 60%. According to some embodiments a silicon avalanche photodiode is provided that can detect source signals at a data bandwidth of greater than 5 gigabits per second, at wavelengths of 850 nanometers, while having a gain of greater than 2. According to some embodiments a silicon APD has a multiplication region with microstructures that extend into the P multiplication layer, N multiplication layer and/or charge layer. According to some embodiments a silicon photodiode is provided that can detect source signals at a data bandwidth of greater than 1 gigabit per second, at wavelengths of 980 nanometers with a quantum efficiency of at least 40%. According to some embodiments a silicon photodiode is provided that can detect source signals at a data bandwidth of greater than 0.5 gigabits per second, at wavelengths of 1000 nanometers with a quantum efficiency of at least 30%. According to some embodiments, the microstructures effectively reduce

capacitance of the photodetector when compared to a microstructure-free device having a similar photon absorbing length.

[0010] According to some embodiments, the absorbing semiconductor region and the microstructures are formed of silicon and germanium. According to some embodiments, the microstructures are formed by etching away portions of silicon and using a selective area growth process to grow germanium in the etched away portions. According to some embodiments, the absorbing semiconductor region and the microstructures are formed of germanium. According to some embodiments, the photo detector is configured to receive the source signal from the substrate-side. The anode region can include a germanium P layer formed by an epitaxial lateral overgrowth process. The device can be configured such that the source signal to passes through the absorbing region a first time, reflects from a surface and thereafter passes through the absorbing region a second time. The device can also be configured to receive the source signal the top-side and the anode region can be made of a silicon P layer. According to some embodiments, a avalanche photodiode is provided that detects source signals at a data bandwidth of greater than 1 gigabit per second, at source signal wavelengths of 1750 nanometers or shorter, and having a gain of greater than 2. According to some embodiments, the absorbing semiconductor region and the microstructures are formed of III-V family material(s) such as InP, GaAs, InGaAs, GaN, InGaN, InGaAsP, AlGaAs, AlGaN, GaP, InSb or InAs.

[0011] According to some embodiments, the microstructures include voids buried within the absorbing semiconductor region. According to some embodiments, voids are buried in a layer of material so as to effectively lower the refractive index at the signal wavelength(s) and as well as lower the capacitance of the layer of material.

[0012] According to some embodiments, a photovoltaic device is described that includes a semiconductor material having a plurality of voids buried therein. The semiconductor material being configured to convert solar radiation into direct current electricity. According to some embodiments, the voids are microstructured voids and are configured to enhance absorption of the semiconductor material thereby increasing conversion efficiency of the device. According to some embodiments, the voids are sized and/or spaced apart by less than 3 microns, and

are configured to alter an effective refractive index of the semiconductor material near a surface, for example to reduce reflection of incident sunlight from the device and/or increase internal reflections within the semiconductor material.

[0013] According to some embodiments a glass material is described in which the glass has a plurality of buried voids dimensioned between 0.01 microns to 1000 microns. In some examples the glass forms a part of a photovoltaic device. According to some embodiments, the buried voids are filled with a material gel, polymer and gas. The buried voids can provide flexibility of the glass material, and/or increased resistance of the glass material to physical damage and/or damage propagation.

[0014] According to some embodiments, a microwave transmission line structure is described that includes: a semiconductor substrate material having a plurality of high-density dielectric-filled voids configured to reduce a dielectric constant of the semiconductor substrate material; and a plurality of metallic microwave transmission lines, least one of which is positioned above the semiconductor substrate material. According to some embodiments, the dielectric-filled voids are filled a material such as: nitrogen, argon, vacuum, air, helium, polymer, metal oxides, silicon dioxide, silicon nitride, calcium fluoride, or zinc oxide. According to some embodiments, the voids are further configured to reduce dispersion and reduce loss associated with the microwave transmission lines at least in part by reducing current loop flow and/or eddy currents.

[0015] According to some embodiments, an optical waveguide structure is described that includes: an optical mode region; and a supporting semiconductor material adjacent to the optical mode region. The supporting material includes a plurality of microstructured voids that are configured to alter an effective index of refraction of the supporting material based on the size, shape, density, etc. of the microstructured voids.

[0016] According to some embodiments, a heat exchanger system is described that includes: a heat generating device; a heat sink configured to dissipate heat to a surrounding medium; and an intermediate material mounted between the heat generating device and the heat sink. The intermediate material includes a plurality of buried voids configured to effect thermal conductivity of the intermediate material. According to some embodiments, some of the buried voids are filled with

thermally conductive material and others are filled with a thermally isolating material. The two types of voids being positioned to conduct heat from the heat generating device to the heat sink and to reduce thermal cross talk with other heat sensitive devices mounted on the intermediate material.

BRIEF DESCRIPTION OF THE DRAWINGS

[0017] To further clarify the above and other advantages and features of the subject matter of this patent specification, specific examples of embodiments thereof are illustrated in the appended drawings. It should be appreciated that these drawings depict only illustrative embodiments and are therefore not to be considered limiting of the scope of this patent specification or the appended claims. The subject matter hereof will be described and explained with additional specificity and detail through the use of the accompanying drawings in which:

[0018] FIG. 1 is schematic side cross section of three dimensional micro structures that enhance bulk absorption coefficient in photo sensitive devices, according to some embodiments;

[0019] FIG. 2 is a cross section diagram showing aspects of a typical structure of a conventional PIN photodiode;

[0020] FIGs. 3A and 3B a plots showing bandwidth and quantum efficiency (QE), respectively, of a bulk conventional silicon photodiode versus "d" in microns;

[0021] FIGs. 4A-4D are graphs showing the enhancement of bulk absorption coefficient vs bandwidth and QE for a microstructured Si photodetector, according to some embodiments;

[0022] FIGs. 5A and 5B are cross sections showing aspects of a top illuminated microstructered PIN silicon photodiode, according to some embodiments;

[0023] FIGs. 6A and 6B are cross sections showing aspects of a bottom illuminated microstructered NIP silicon photodiode, according to some embodiments;

[0024] FIGs. 7A and 7B are cross sections showing aspects of a microstructered avalanche photodiode, according to some embodiments;

[0025] FIG. 8 is a cross section showing a silicon epitaxial structure for a high-speed high-efficiency microstructured APD, according to some embodiments;

[0026] FIGs. 9A-9E are a series of cross sections showing some basic microstructure processing steps, for a high-speed APD, according to some embodiments;

[0027] FIGs. 10A-10B are cross sections showing aspects of a top illuminated microstructered photo diodes, avalanche photo diodes and/or photovoltaics (PV) with microstructured voids in N-Si, according to some embodiments;

[0028] FIGs. 11A and 11B are cross sections showing aspects of an heteroepitaxial APD structure of Ge on Si, according to some embodiments;

[0029] FIG. 12 is a cross section illustrating aspects of a passivation method for Ge surfaces on microstructures, according to some embodiments;

[0030] FIGs. 13A and 13B are graphs showing the effects of mictrostructure enhancement of Ge bulk absorption coefficient for photodiodes and/or avalanche photodiodes based on Ge on Si, according to some embodiments;

[0031] FIGs. 14A-14B are cross sections showing aspects of a top-illuminated Ge on Si avalanche photodiode having microstructured pillars/holes, according to some embodiments;

[0032] FIGs. 15A-15D are cross sections illustrating aspects of bottom-illuminated Ge on Si avalanche photodiodes having microstructured pillars/holes, according to some embodiments;

[0033] FIGs. 16A and 16B are graphs comparing single pass and double pass photodiodes and/or avalanche photodiodes based on Ge on Si, according to some embodiments;

[0034] FIGs. 17A-17B are cross sections showing aspects of a top-illuminated Ge on Si photodiode structure having microstructured pillars/holes for applications with signal wavelengths ranging from 700 to 1800 nm, according to some embodiments;

[0035] FIGs. 18A-18B are cross sections showing aspects of a bottom-illuminated Ge on Si photodiode structure having microstructured pillars/holes for applications with signal wavelengths ranging from 1200 to 1800 nm, according to some embodiments;

[0036] FIGs. 19A-19C are diagrams illustrating how mictrostructures can reduce capacitance of a photodiode such that a larger area photo diode can be fabricated with the same bandwidth and QE, according to some embodiments;

[0037] FIGs. 19D-19E are cross sections showing aspects of fabricating an APD device having a III-V absorbing layer grown on a P-I-N silicon multiplication layer, according to some embodiments;

[0038] FIG. 20 shows bulk layers without a final P-Si layer for devices having microstructured Ge buried or embedded in an Si microstructure, according to some embodiments;

[0039] FIG. 21 is a cross section showing etching of microstructured pillars and/or holes for devices having microstructured Ge buried or embedded in an Si microstructure, according to some embodiments;

[0040] FIG. 22 is a cross section showing a device having microstructured Ge buried or embedded in an Si microstructure, after the Ge "I" layer is grown in the etched region and planarized, according to some embodiments;

[0041] FIG. 23 is a cross section showing a device having microstructured Ge buried or embedded in an Si microstructure, after I-Ge regrowth and planarization, and a cap layer of P-Si, according to some embodiments;

[0042] FIGs. 24A - 24B are cross sections showing aspects of a microstructured APD with buried/embedded I-Ge absorbing microstructures in I-Si microstructures, according to some embodiments;

[0043] FIGS. 25A - 25C are cross sections showing aspects of a photodiode having buried/embedded Ge microstructures in a Si microstuctured pillar and/or hole array, according to some embodiments;

[0044] FIGs. 25D - 25E are cross sections showing aspects of a forward biased device such as a vertical cavity surface emitting laser (VCSEL), according to some embodiments;

[0045] FIG. 26 is a cross section showing starting epitaxial layers in which mictrostructured voids are fabricated, according to some embodiments;

[0046] FIG. 27 is a cross section showing microstructured holes/pillars etched into the I-Si layer, according to some embodiments;

[0047] FIG. 28 is a cross section showing microstructured voids buried or embedded in Si with a Si capping P^+ anode layer 2826, according to some embodiments;

[0048] FIG. 29 is a cross section showing Bragg reflectors formed on the P-Si surface to provide a highly reflective mirror, according to some embodiments;

[0049] FIG. 30 shows an example of a PIN PD/PV structure with microstructured voids to enhance absorption, reduce bulk refractive index, reduce capacitance and increase mechanical flexibility of large sheets of PV on semiconductor material, according to some embodiments;

[0050] Fig. 31 is a cross section showing regrown I-Ge with a buried/embedded voids, according to some embodiments;

[0051] Fig. 32 is a cross section showing a device having buried microstructured voids in I-Si with regrown I-Ge and capped by a epitaxial layer, according to some embodiments;

[0052] FIG. 33 is a top view showing distribution of microstructured pillars, holes and/or buried voids in an PD/APD, according to some embodiments;

[0053] FIG. 34 is a top view showing distribution of microstructured pillars, holes and/or buried voids in an PD/APD, according to some other embodiments;

[0054] Fig. 35 shows the basic epitaxial structure for a conventional Si PV/PD diode on N Si substrate;

[0055] FIG. 36 shows microstructured voids incorporated into an N-Si layer, according to some embodiments;

[0056] FIG. 37 is a cross section showing etched Si microstructured pillars/holes with regrown Ge covering the Si, according to some embodiments;

[0057] FIG. 38 is a cross section showing microstructured Si pillars/holes with Ge regrowth on an N-Si layer having embedded microstructured voids, according to some embodiments;

[0058] FIG. 39 is a cross section showing partial coverage I-Ge on microstructured Si pillars/holes, according to some embodiments;

[0059] FIG. 40 is a cross section sowing the basic components for the a microstructured Si-Ge pillar hole array PD/PV and/or APD, according to some embodiments;

[0060] FIGs. 41A-41B are cross sections showing aspects of a microstructured pillar/hole array device above a N-Si layer having buried microstructured voids, according to some embodiments;

[0061] FIGs. 42A-42D are cross sections showing aspects of an APD with microstructured pillar/hole arrays above an N-Si layer having buried microstructured voids, according to some embodiments;

[0062] FIGs. 43-46 are top views illustrating various dimensions, spacings and shapes for microstructured elements, according to some embodiments;

[0063] FIGs. 47-48 are cross sections showing microstructured pillar and hole arrays having varying lengths and depths, according to some embodiments;

[0064] FIG. 49 shows shows a microstructured surface having a combination of both pillars and holes, according to some embodiments;

[0065] FIG. 50 is a cross section of an optical ridge waveguide, according to some embodiments;

[0066] FIG. 51 is a cross section of a buried optical waveguide in silicon using voids, according to some embodiments;

[0067] FIGs. 52 and 53 are a cross section and top view, respectively, of a ridge waveguide integrated with a microstructured PD/APD, according to some embodiments;

[0068] FIGs. 54A and 54B show a microwave transmission line on Si with voids, according to some embodiments;

[0069] FIG. 55 is a cross section of voids for thermal conduction and thermal isolation of heat producing ICs and light emitters, according to some embodiments; and

[0070] FIG. 56 is a cross section showing a distribution of voids to increase lateral path length for increasing lateral electrical resistivity and decrease lateral thermal conduction, according to some embodiments.

DETAILED DESCRIPTION

[0071] A detailed description of examples of preferred embodiments is provided below. While several embodiments are described, it should be understood that the new subject matter described in this patent specification is not limited to any one embodiment or combination of embodiments described herein, but instead encompasses numerous alternatives, modifications, and equivalents. In addition, while numerous specific details are set forth in the following description in order to provide a thorough understanding, some embodiments can be practiced without some or all of these details. Moreover, for the purpose of clarity, certain technical material that is known in the related art has not been described in detail

in order to avoid unnecessarily obscuring the new subject matter described herein. It should be clear that individual features of one or several of the specific embodiments described herein can be used in combination with features or other described embodiments. Further, like reference numbers and designations in the various drawings indicate like elements.

[0072] According to some embodiments, microstructures are used to enhance the bulk absorption constant (also referred to as absorption coefficient) to achieve high quantum efficiency (QE) while maintaining an absorption length suitable for high data rate applications. As used herein, "QE" refers to internal quantum efficiency (IQE). IQE is equal to external quantum efficiency (EQE) in cases where reflection and transmission are negligible.

[0073] According to some embodiments, microstructures are used to improve bulk absorption constant at wavelengths in the proximity of the semiconductor material's band gap. This allows for extending the operating optical wavelengths and/or operating spectrum of the photosensor. The enhanced bulk absorption constant (or coefficient) is called the effective absorption constant (or coefficient). The term "effective" is used since absorption constant or coefficient is an inherent material property. However, with resonance effects, plasmonic effects, field enhancement effects, scattering effects, near field and sub wavelength effects, the effective absorption constant or coefficient can be greater than the bulk or material absorption constant or coefficient. As used herein, the following terms are used interchangeably: enhanced absorption constant, enhanced absorption coefficient; enhanced effective absorption constant; enhanced effective absorption coefficient; enhanced absorption; enhanced effective absorption; and effective absorption constant; and effective absorption coefficient.

[0074] According to some embodiments, enhanced absorption can also have drastic effects on path length. In one bulk absorption example, the path length for the photons to be absorbed to 1/e of its original amplitude is, for example 100 micrometers (μm), whereas under enhanced absorption according to some embodiments, the path length is 1 micrometer for the optical amplitude to decay to 1/e of its original amplitude. Equivalently, if path length is kept constant to one micrometer then the enhanced absorption coefficient is 100 times greater than the bulk absorption coefficient.

[0075] This is seen by the relationship $A= A_0 e^{-\alpha L}$ where A is the decaying amplitude of the incident photon flux A_0 and α is the absorption coefficient and L the path length for absorption to take place. So, rather than have L be 100 times longer, an effective α can be defined such that it is 100 times greater than a non enhanced absorption coefficient such as the bulk absorption coefficient. The resonance/scattering/near field effects of microstructures for example gives the equivalence of the path length that is 100 times longer where the resonant/scattering/near field microstructure is just one micron long. To put it another way, in a very simplistic view, the photons in the resonant structures make 50 round trips before reaching the 1/e value of its original amplitude, so the equivalent linear length is 100 times the length of the resonant structure. For simplicity, resonance/scattering/near field effects will collectively be referred to herein as "resonant" which can include, resonant, scattering, near field, plasmonic, nonlinear and linear optical effects.

[0076] As used herein the terms "microstructures" and "microstructured" refer to: pillars, voids, holes and mesas, of various shapes and sizes having at least one dimension in the micrometer scale, submicrometer scale, and/or sub-wavelength scale.

[0077] According to some embodiments, properties of the microstructures can also be explained as the absorption mode of high contrast grating (HCG) being used to enhance the effective absorption constant/coefficient or enhanced absorption. Conventionally, HCG uses material that is transparent at the optical wavelength of interest. In contrast, according to some embodiments, at least one of the microstructures is absorbing or weakly absorbing at the optical wavelength of interest. According to some embodiments a low-Q absorbing mode HCG enhances absorption (e.g. Q values in the range of 2-200).

[0078] According to some embodiments, a low index material is used such as buried oxide (BOX), silicon on insulator (SOI), silicon on sapphire (SOS), low-density semiconductors such as amorphous semiconductor, nanowire semiconductors, voids and holes to lower the effective refractive index. Refractive index is an inherent property of a material. However, according to some embodiments, when structures such as voids, air gaps, and/or holes (which can be filled with low index material, and/or regrowth) have dimensions on the order of the

optical wavelength, the optical electromagnetic field will see an average refractive index consisting of the material refractive index and the structures (which can be filled by a low refractive index material). This average is referred to herein as the effective refractive index. According to some embodiments, a low index or effective low index material need not be used in the microstructures.

[0079] According to some embodiments, the techniques for enhancing effective absorption can be applied to various materials including: silicon, germanium, III-V material such as InP, GaAs, GaN, InGaAs, and any combination of the III-V material family. As used herein, the term "material family" of a III-V material is defined as any material that is lattice matched or approximately lattice matched (within a few percent) to GaAs, InP, GaN, InSb semiconductors. For example, the InP material family can include InGaAs, InGaAsP, InAlAs. According to some embodiments, in the case of microstructures, regrowth such as selective area growth (SAG) of Ge, InGaAs, or other III-V material in silicon microstructures can be carried out without the detrimental effects of lattice mismatch since the dimension of the footprint of the lattice mismatched material on silicon is small (approximately a few micrometers to sub-micrometers). This allows Ge and other III-V materials to be integrated with silicon without the use of a conventional buffer layer (such as amorphous Ge in the case of Ge on Si growth). The heterogeneous integration of materials can be homo or hetero structures, combination of crystalline and microcrystalline and amorphous semiconductor, conductor such as carbon, graphene, insulator, dielectrics, solid, gaseous, liquid such as glass or polymer that can be semiconducting.

[0080] Due to the microstructures, the capacitance can also be represented by an effective capacitance which is a parallel capacitance of (1) the dielectric constant of one semiconductor, and (2) the dielectric constant of another material, which can be a semiconductor, dielectric, gas, vacuum, partial vacuum, liquid such as glass or polymer (polyimide, mylar, or other organic compound). The effective capacitance of the device is the combination of the capacitance of the parallel capacitors, which can be two or more. An advantage of the use of microstructure according to some embodiments, is that the effective capacitance can be significantly lower than the capacitance of a homogeneous material such as a semiconductor. The lower capacitance allows a device to have a larger area while

still maintaining suitably high data rate bandwidth, and/or increase the data rate bandwidth by reducing the thickness of the device to reduce the transit time.

[0081] According to some embodiments, the photosensor can be a photodiode (PD), avalanche photodiode (APD), photovoltaic (PV) or solar cell, or any optoelectronic device that converts photons to electrons. According to some embodiments, emitters such as lasers and light emitting diodes that convert electrons/holes to photons can also be implemented using microstructures.

[0082] According to some embodiments, the enhanced absorption allows the APD/PD to: (1) extend the sensitivity of the APD/PD to photons with energies (or wavelength) closer to the material band gap with QE greater than 60% and data bandwidth greater than 3 Gb/s; (2) operate at a high data rate bandwidth (e.g. >10 Gb/s), due to shorter absorption length therefore shorter transit time; (3) increase quantum efficiency with enhanced absorption; (4) be manufactured of silicon which has superior APD properties with low excess noise; (5) be compatible with Si Photonics and CMOS processes. According to some embodiments, the PD/APD can be integrated with ASIC (application specific integrated circuits) such as signal processing, signal amplification, memory, cpu, electrical transmitter, optical waveguides, integrated optics, and other ICs for specific applications. This is advantageous for mass production using CMOS foundries.

[0083] According to some embodiments, microstructures such as voids are used to reduce effective refractive index to create resonant structures to enhance the absorption. In microstructures where selective area growth are used to integrate Ge or III-V material with silicon, voids can be made in the silicon microstructure such that the absorbing region is a resonant structure to enhance the effective absorption coefficient by 2 to over 100 times.

[0084] According to some embodiments, silicon is used for avalanche gain. Silicon has the lowest excess noise for an avalanche photodiode. By integrating Ge and/or III-V material with silicon, the absorption takes place in Ge and/or III-V material and the electronic gain occurs in silicon. Depending on the optical wavelengths, for example shorter than 1100 nm, silicon may be used for both absorption and electronic gain with the use of microstructures.

[0085] According to some embodiments, microstructures such as buried voids can reduce lateral electrical and thermal conductivity. In situations where

directional conductivity of electrical or thermal (phonons) is preferred, voids can be used to confine the flow of electrical current and/or heat.

[0086] According to some embodiments, the absorption of photons in semiconductors is enhanced with the use of microstructures. The microstructures can have effects such as resonance, field enhancement, near field and sub wavelength effects, scattering, plasmonics, photonic crystal, absorption mode in high contrast grating at the near field regime, which are both linear and non linear effects that can effectively increase the effective absorption length resulting in a greater absorption of the photons for a given length.

[0087] According to some embodiments, microstructures used for absorption enhancement for silicon photodiodes and silicon avalanche photodiodes can result in silicon PD and APD with bandwidths in excess of 10 Gb/s (or equivalently 6.75 GHz approximately depending of the digital coding format) at photons with wavelengths of 850 nm approximately (which is the current datacom preferred wavelength) with quantum efficiencies of approximately 90% or more.

[0088] Silicon optical detectors are very robust due to the maturity of the material and processing techniques, the surfaces can be easily passivated to eliminate dangling bonds that can cause surface states and carrier recombination centers, they have excellent carrier lifetimes due to low defects and high material purity, and for APD applications, the noise is low due to the small ionization ratio between holes and electrons (k factor, silicon have the lowest k factor than any III-V material) and such detectors are CMOS compatible for integration with electronics for signal processing and with Si photonics.

[0089] According to some embodiments, other material such as germanium, III-V, a-Si (amorphous silicon) may also be used singly or together with other materials such that a multiple bandgap in parallel can be fabricated with enhanced absorption.

[0090] According to some embodiments, microstructures and voids are used to reduce the effective refractive index and capacitance to achieve the absorption mode high contrast grating effect and to reduce the effective capacitance of the device for lower RC time constants.

[0091] In addition, according to some embodiments, microstructures buried in the semiconductor can reduce lateral electrical and thermal conduction. Microwave

transmission lines are possible for example where high-density voids are buried in Si to reduce the dielectric constant and also eddy currents in the semiconductor resulting in low loss and dispersion. Voids can also be used for thermal isolation and to improve thermal conductivity by filling the voids with thermal conductors. This is useful in thermal management of components on a silicon substrate.

[0092] The enhancement using nanowires (Garnett et al, Light trapping in silicon nanowire solar cells, Nano Letters, 2010, 10, 1082-1087; Kelzenberg et al, Enhanced absorption and carrier collection in Si wire arrays for photovoltaic applications, Nature Materials, vol. 9, March 2010, 239-244) and nanoholes (Lin et al, Optical absorption enhancement in silicon nanowire and nanohole arrays for photovoltaic applications, Proceeding of SPIE, Vol. 7772, 77721G-1, 2010) have been reported. Nanowire is known to be used for light trapping in photovoltaic applications where the photogenerated carriers diffuse to the anode or cathode of a P-N junction with zero external bias operating at DC (direct current).

[0093] According to some embodiments, the photogenerated carriers are swept out with an external reverse bias in the absorbing "i" region of a P-I-N diode (PD) or P-I-P-I-N diode (APD) for high modulation bandwidth (greater than or equal to 10 Gb/s bandwidth) and high quantum efficiency and for APD for high current gain, with gain greater than 3 dB.

[0094] The cause or causes of the enhancement of the absorption coefficient are believed to include one or more of the following: an increase in optical field concentration, resonance effects, constructive and destructive optical interferences (amplitude and phase) effects, scattering, and high contrast grating (HCG) effects. See, e.g. Chang-Hasnain et al, High contrast gratings for integrated optoelectronics, Advances in Optics and Photonics 4, 379–440 (2012), hereinafter "Chang-Hasnain." The HCG effects are at the near-wavelength regime (See, Chang-Hasnain) where the optical wavelength in the material of the grating and the optical wavelength in the surrounding material of the grating is the range of the period of the grating.

[0095] FIG. 1 is schematic side cross section of three dimensional micro structures that enhance bulk absorption coefficient in photo sensitive devices, according to some embodiments. Microstructured pillars 110 and/or holes 120 are etched into the "I" Si layer 100. The optical wavelength in material M_1 is λ/n_1 where

n_1 is the refractive index of M_1 and the optical wavelength in material M_2 is given by λ/n_2 where n_2 is the refractive index of material M_2. The center to center distance L of the structures 110 can be between λ/n_1 and λ/n_2 or approximately 100-2000 nm, which is referred to as the near-wavelength regime. The diffraction regime is where L (one cycle) is greater than the wavelength, while the subwavelength regime is where L is less than the wavelength. The cross section of FIG. 1 shows the 3D (dimension) microstructured pillar/hole array, which enhances the bulk film absorption coefficient by factors of 1.5 to over 100. The period of the 3D pillar/hole microstructured array can be seen as a 3D high contrast grating, whose period of the grating Λ can lie between λ/n_1 where n_1 is the optical refractive index of material M_1 and λ/n_2 where n_2 is the optical refractive index of material M_2. If $n_1 > n_2$ then $\lambda/n_1 < \Lambda < \lambda/n_2$ where λ is the optical wavelength of the light to be absorbed by the microstructured pillar/hole array typically in the "I" region of a P-I-N PD or for APD, the absorbing "I" region P-I-P-I-N where the second "I" region is the multiplication region, or the wavelength of the optical signal to be detected by the PD and APD. At this near-wavelength regime of the 3D HCG microstructured pillar/hole array, the resonance Q (quality factor, or proportional to the ratio of the energy stored in the resonator/energy losses per cycle; where it is the optical cycle, the optical frequency impinging on the resonator or in the resonator) can be as high as 10^7 (see, Chang-Hasnain) if the HCG has minimal absorption loss as is known. In addition, in most cases the ratio of the index of the HCG to the surrounding material index need only be approximately 1.1 to observe the effects of the HCG.

[0096] The HCG effect that may explain the high enhancement of the absorption coefficient of the bulk material is that a single or multiple HCG layer (or a single microstructured pillar/hole array layer) due to its resonance effects and/or due to a varying of the microstructured pillar/hole period spacing, the optical signal resonating in the HCG/microstructured pillar-hole array can be directed to propagate in the plane of the HCG/microstructured pillar-hole array rather than normal to the surface. Together with resonance and in-plane propagation this can greatly increase the absorption path length in the HCG/microstructured pillar-hole array. According to some embodiments, the absorbing HCG mode is operated with a reverse voltage bias for PD/APD and a built-in bias (zero applied bias) in photovoltaic devices.

[0097] Using the phenomenon of near-wavelength and also deep-wavelength where the HCG period is much less than the optical wavelength, and the diffraction regime where the HCG period is greater than the optical wavelength (See, Chang-Hasnain) the microstructured pillar-hole-void array can have enhanced absorption coefficient over the bulk absorption coefficient by a factor of 1.1 to over 100.

[0098] According to some embodiments, the HCG effect is also used in the absorbing mode or lossy mode or low Q of 1-10000 (compared with known HCG that are in the non-absorbing mode or non-lossy mode to achieve high Q of greater than 1,000,000 and high reflectivity), in both buried/embedded (not fully buried) Ge microstructures in Si and buried/embedded void microstructures in either Ge or Si to improve the quantum efficiency (QE) and operating wavelength range of Si (400-1100 nm) and Ge (400 to 1800 nm) and Ge on Si photodiodes and avalanche photodiodes operated in a reverse bias mode of the pn, pin, pinip junctions (p and n can be switched for certain device configurations) that can be homo or heterojuction, crystalline or amorphous or any combinations thereof. In addition, the substrate can be on SOI or BOX or voids to reduce the index of refraction or effective index of refraction and the dielectric constant or effective dielectric constant (a dielectric with many voids can be represented as an effective dielectric constant, or equivalently effective capacitance).

[0099] Known silicon photodetectors have been limited to wavelength ranges of 200 to 1000 nm due to indirect bandgap of 1.1 eV. In particular, near the band gap wavelengths of 800-1000 nm, the frequency response of the silicon photodetector to a modulated optical signal at Gb/s rate is limited to 1.5 Gb/s approximately or less due to the weak absorption constant of Si at those wavelengths which are approximately 760 cm^{-1} at 850 nm and 67 cm^{-1} and 63 cm^{-1} at 980 and 1000 nm respectively, resulting in long absorption lengths of material, 30 microns or more, which results in low frequency response for the PD/APD. The wavelengths 850 nm is of interest since this is the standard wavelength for short distance (few meters to a few kilometers) multimode fiber optical datacommunication.

[00100] The amount of incident photons absorbed is approximately given by $\eta=1-e^{-\alpha L}$ where η (also the quantum efficiency if reflection off the surface of the PD is negligible) is the amount absorbed and "α" is α the absorption constant and "L" is the length length of the absorber. Using this equation and the absorption constant

of Si at 850 nm, 90% of the incident photons are absorbed at a depth of approximately 30 μm. Known high speed photodetectors typically have an absorption region of approximately 2 μm in length. The reason for this is that transit time and RC time of the photodiode need to be considered to have a bandwidth of 20 GHz (or approximately 30 Gb/s) or more and still have an external quantum efficiency of 80-90% or better.

[00101] Efficiency and bandwidth (transit and RC time): At a field strength of $6 \cdot 10^4$ V/cm the electron drift velocity is $1 \cdot 10^7$ cm/s at a temperature of 300 K. The 3 dB bandwidth of the photodetector due to transit time is given by: f(3dB)=0.45/t(transit) where t(transit) is the transit time for the carriers to cross the depleted high field region. FIG. 2 is a cross section diagram showing aspects of a typical structure of a PIN photodiode structure. Assuming negligible photocarriers generated in the P region 210 of the PIN 200 and mostly generated in the "i" region 220, the transit time is determined by the electron drift velocity and "d" (the high field "i" region). The PIN 200 is reversed biased (e.g. between -4 and -25 V). The "i" region 220 is fully depleted in this case. The RC time of the PIN structure 200 is determined by the capacitance, which is the ratio of the area ($\pi w^2/4$) of the PIN 220 to d.

[00102] According to conventional techniques, a 30 μm thick absorption layer ('i") to achieve 90% absorption for Si at 850 nm wavelength will give a transit time limited 3dB bandwidth of 1.5 GHz (approximately 2.2 Gb/s) which is too low for many current applications. Many current applications are in the 10-20 Gb/s range and in the near future 40 Gb/s. A d of 2 μm or less is desirable for current high-speed photodiodes in optical datacom applications to give over 30 Gb/s bandwidth.

[00103] RC time is another time to consider in photodiodes (applies to both APD and PD). The 3 dB bandwidth due to RC time is given by $f(RC)= 1/(2\pi RC)$; where C is the capacitance of the photodiode and R is the load resistance which is typically 50 ohms (and occasionally 25 ohms). Capacitance in the case of a conventional PIN structure photodiode with the "i" region fully depleted by the reverse bias, is just a parallel plate capacitance given by $\varepsilon A/d$ where ε is the dielectric constant of the material (multiplied by vacuum permittivity of $8.854 \cdot 10^{-14}$ farads/cm) which is 11.9 for Si, A is the area of the capacitor ($\pi(w/2)^2$), and d is the depleted "i" (i and I are used herein interchangeably). The f(RC) becomes larger

as d increases since the capacitance is decreasing with increasing d and a fixed area, where the diode diameter for example is 30 μm (diameters of high frequency PD/APD range from 5 to 60 μm). Diameter of diode for calculating the RC time is the total capacitive area of the diode that includes the photosensitive area and any metallization that may contribute to the overall capacitance.

[00104] The overall frequency bandwidth of the photodiode is a sum of the squares of the transit time and the RC time. This is given by the equation:

$$f=1/(2\pi(RC)^2+(\tau/2.4)^2)^{1/2}).$$

[00105] FIGs. 3A and 3B are plots showing bandwidth and QE, respectively, of a bulk conventional Silicon photodiode versus "d" in microns. From plots 310 and 312 in FIGs. 3A and 3B, for the combined f(3dB) of the transit time and RC time and the quantum efficiency η (assuming negligible reflection losses) we see that for bulk silicon to reach 10 Gb/s, the quantum efficiency (QE) is less than 40%, for a 30 μm diameter PD, which is too low for most datacom applications.

[00106] According to some embodiments, to overcome the relatively weak absorption of semiconductors with radiation energies near the bandgap and indirect bandgap semiconductors, for example Si at 850-1100 nm, a microstructured array is used that is etched into silicon that is grown by conventional methods epitaxially such as chemical vapor deposition (CVD) or metal organic chemical vapor deposition (MOCVD), atomic layer deposition (ALD), molecular beam epitaxy (MBE). Note that according to some embodiments, non semiconductors can be used: such as polymers, glass, ceramics, hybrid material such as transition metal oxides, hydrides, chlorides, sulfides embedded with semiconductor, metal, carbon nanoparticles and or atoms, which may or may not have a bandgap. The microstructured array of silicon consists of pillars of Si and/or holes in Si. See, Garnett and Yang, *Light Trapping in Silicon Nanowire Solar Cells, Nano Lett. 2010, 10, 1082–1087* (hereinafter "Garnett et al.") that experimentally demonstrates that an ordered array of silicon nanowires increased the optical path length of the incident optical radiation by 73 times greater than that of bulk silicon.

[00107] According to some embodiments, as described earlier, the concept of effective absorption coefficient is introduced. The effective absorption coefficient of the ordered array of Si nanowires is 73X that of bulk silicon; bulk α for Si is 760 /cm

and nanowire Si α is $5.548x10^4$ /cm at 850 nm which is higher than direct bandgap III-V material.

[00108] It should be noted that the microstructures can also be epitaxially grown using methods such as VLS (vapor liquid solid epitaxial grown) nanowires or microwires (some nanowires have the largest dimension, such as the diameter, in the micron range, so that it can be called a microwire) with or without catalysts, or using a dielectric mask for selective area growth (SAG) epitaxy.

[00109] The nanowire array described in Garnett et al. has a diameter of the nanowire of approximately 390 nm using an array of beads of 530 nm as a dry etch mask. Roughly 1/2 of the Si material is etched away; the effective capacitance for the nanowire array is less than that of the bulk. The effective capacitance can be estimated as two parallel capacitors, one with Si and another with polyimide (filler) whose dielectric constants are 11.9 and 3.4 respectively. The area of each capacitor will be 1/2 that of a 30 μm diameter parallel plate.

[00110] With the effective capacitance lower, the overall 3dB bandwidth for a 30 μm diameter device is significantly higher. FIGs. 4A-4D are graphs showing the enhancement of bulk absorption coefficient vs bandwidth and QE for a microstructured Si photodetector, according to some embodiments. FIGs. 4A and 4B shows the bandwidth (plot 410) and quantum efficiency (plot 420) of a microstructured Si photodiode (PD) or avalanche photodiode (APD) at 850 nm wavelength photons impinging on the PD/APD either single or double pass. With an effective absorption coefficient (EAC) of 73X (412), 30X (414) or 15X (416) over bulk absorption coefficient (BAC), the bandwidth and QE are 54 Gb/s, 98%; 49 Gb/s 90%, 28 Gb/s 90% respectively for a 30 micrometer diameter PD/APD for example. At 1100nm, shown in plots 430 and 440 of FIGs. 4C and 4D, with enhancement, for example, of 172X QE of 90% and bandwidths of 26 Gb/s can be attained using Si microstructured PD/APD. Both PD and APD operate at a reverse bias of -2 to -50 volts range. APDs in general will have less bandwidth than PDs for the same geometry due to the added multiplication layer of the APD. In addition, APDs have a gain-bandwidth product. For simplicity, APD and PD are shown to be approximately the same.

[00111] According to some embodiments, a combination of low capacitance due to the gaps between the microstructured pillars and the enhanced absorption

allows the silicon photodiode and avalanche photodiode to operate at bandwidths greater than 10 Gb/s with high quantum efficiencies (> 90%) at 850 nm wavelength. This has not been demonstrated by conventional silicon PD/APD at these wavelengths. 850 nm is chosen as the nominal wavelength, but according to some embodiments, wavelengths can have values from 700 to 1100 nm.

[00112] According to some embodiments, the weak absorption in the bulk can be taken advantage of for photodetector applications since this will allow light at 850 nm and longer to pass through Si substrate and epitaxial layers toward the microstructured silicon with minimal optical loss and minimal photocurrent outside of the high field region, which can diffuse to the i-region and can cause the photodetector to have a degradation in frequency response.

[00113] According to some embodiments, the techniques described herein are applied to other semiconductors, polymers, organic films, glass, dielectrics, hybrid material such as glass, dielectrics, polymers embedded with nanoparticles of metal, semiconductors. According to some embodiments, one or more of the following are used: Ge, III-V material family such as InP, GaAs, GaN, InGaN; II-VI material family such as ZnSe, and also heterostucture material such as III-V grown on Si, Ge grown on Si. For example, for Ge on Si, microstructures are fabricated on the Ge to increase absorption which allows a shorter length of Ge to be used resulting in higher speed due to lower effective capacitance and shorter transit time for the carriers.

[00114] FIGs. 5A and 5B are cross sections showing aspects of a top illuminated microstructered PIN silicon photodiode, according to some embodiments. FIG. 5A shows the starting basic material structure 500. In FIG. 5B, silicon epitaxial structure is shown for a high-speed high efficiency microstructured photodiode 520. The photophoto diode 520 in FIG. 5B is designed for top illumination. According to some embodiments, BOX/SOI layer 504 may not be used. FIGs. 6A-B, *infra* show an example for bottom illumination. Note that with minor modifications the n and p doping can be switched and the direction of illumination may also be affected. Acccording to some embodiments, the illumination can be either perpendicular to the surface of the PD/APD or at an angle off perpendicular to the surface. According to some embodiments, in integrated structures where the optical signal is guided in an optical waveguide, the

microstructured absorption region can also be illuminated edge wise, directly into the microstructures or evanescently coupled to the microstructured i region.

[00115] FIG. 5B shows a microstructured pillar and or hole PD 520 in silicon with the starting material 500 consisting of a P-I-N Si layer grown on an Si substrate 502 that can be N doped or low doped in which case an extra N^+ layer is first grown on the substrate to minimize series resistance. The dimensions and doping of the layers can range as follows; N^+ cathode contact layer 506 (or a thin layer on top of 506, between 506 and 508) with N doping of greater than 5. $10^{17}/cm^3$, and thickness ranging approximately from 0.1 to 10 micrometers or more; N layer 506 with N doping greater than 5. $10^{17}/cm^3$, and thickness ranging approximately from 0.1 to 10 micrometers or more; I high field absorption region 508 with background doping of less than $5x10^{16}/cm^3$ and thickness ranging approximately from 0.1 to 5 micrometers depending on applications; and P^+ anode layer 510 with P doping greater than 5. $10^{18}/cm^3$ and thickness ranging approximately from 0.1 to 5 micrometers or more. The PD (and APD) photosensitive area (defined by the P-I-N or P-I-P-I-N junction area) is nominally 30 micrometers (10-80 micrometers in diameter are possible ranges) in diameter for 20 Gb/s or more bandwidth operation. According to some embodiments, the area can be larger for lower bandwidth or smaller for higher bandwidth operation. The Si microstructures of arrays of holes 522 and/or pillars 524 shown in FIG. 5B, which can be random, patterned or pseudo-random, are for enhancing the bulk absorption coefficient of Si to detect photons with wavelengths from 300-1100 nm. In the case of datacom applications, according to some embodiments, the optical signal wavelengths range from 750-1100 nm. A transparent conducting oxide and P-ohmic layer 526 is also provided.

[00116] The PD 520 is operated in a reverse bias mode, with negative voltage on the anode (P^+ layer 510 via P-ohmic and bond contact metal 528) and positive voltage on the cathode (N^+ layer 506 with N-ohmic bond contact metal 530) ranging from -1 to -20 volts. According to some embodiments, the PD structure 520 shown in Fig. 5B (and PD structure 620 in FIG. 6B, *infra*) can also be used for photovoltaic (PV) operation without any external bias.

[00117] As shown in FIG. 5B, the optical signal can impinge normal to the surface or at an angle off normal. In certain cases, optical signal coming in at an

angle off normal can have a higher QE and can also be at a certain rotation about the axis normal to the surface. This is to avoid the bald spot effect where some photons travelling normal to the surface can "see" bald spots whereas for photons illuminating at an angle off normal to the surface, the bald spots are hidden by other microstructures. This is not the case in near field optics where the spacing of the microstructures are of the order of the optical wavelength or subwavelength, the bald spots are not a significant issue.

[00118] FIGs. 6A and 6B are cross sections showing aspects of a bottom illuminated microstructered NIP silicon photodiode, according to some embodiments. The optical signal impinges on the photodiode 620 from the substrate side or bottom. The substrate 602 can be thinned to 10 microns or less by etching for example a via and stopping at the P layer or the photodiode can be fabricated on a BOX (buried oxide) or silicon on insulator (SOI) silicon wafer and the etch via can stop at the BOX layer 604 which can also be selectively etched to the silicon layer 606, the via 630 is as wide or wider as the photosensitive area of the photodiode 620. An antireflection layer (not shown) is applied to the silicon remaining layer 606 or the BOX layer 604 (the BOX layer 604 can be designed as a part of the antireflection layer for example) to minimize reflection (the BOX layer 604 can also be selectively etched off such that antireflection layer can be applied to the silicon P layer 606 to minimize multiple reflections). The back illuminated photodiode 620 has the advantage that a reflector 626 can be applied on the N layer 610 to reflect any light not absorbed on the first pass, in effect doubling the length of the "I" layer 608. The QE can be increased due to the extra length. In addition the reflector 626 on the N layer 610 can be smooth of textured to scatter (non-specular or diffused reflection) the light (optical signal) to optimize absorption by the microstructures (arrays of pillars 624 or holes 622). Since the length of the "I" region is effectively doubled, the transit time can effectively be reduce since only half of "I" is needed.

[00119] Bottom illuminated PDs such as PD 620 in FIG. 6B are also sometimes referred to back/substrate illuminated PDs, and top illuminated PDs such as PD 520 in FIG. 5B are also sometimes referred to front/surface illuminated PDs.

[00120] According to some embodiments, the basic structure of a microstructured Si photodiode such as shown in in FIGs. 5A, 5B, 6A and 6B, is

fabricated from a bulk thin film epitaxially grown silicon with a P-I-N structure on a silicon wafer which can be doped N type or not intentionally doped or low doped N type Si substrate with (100) orientation or other orientation such as (111).

[00121] According to some embodiments, the basic layer structures (such as layers 502, 504, 506, 508 and 510 of structure 500 of FIG. 5A, and layers 602, 604, 606, 608 and 610 in structure 600 of FIG. 6A) are all grown epitaxially using one or more of the following methods: chemical vapor deposition (CVD), metal organic chemical vapor deposition (MOCVD), plasma enhanced chemical vapor deposition (PECVD), molecular beam epitaxy (MBE), atomic layer deposition (ALD), pulsed laser deposition (PLD) on Si substrate of either P or N or low doped or undoped) or BOX/SOI substrates.

[00122] Processing details have been left out for simplicity. According to some embodiments the following basic steps are carried out: first (for pillars, not necessary for holes), depositing the p ohmic contact metal layer using e-beam, thermal or sputtering deposition; second, photolithographically (or imprint lithography) defining the microstructure pattern either pillars or holes and forming the etch mask for either dry or wet etching; third, etching of microstructure patterns on the P and I layers partially or fully and can extend into the N layer; fourth, passivating the sidewalls of the microstructure patterns (pillars or holes) with thermal oxide to minimize surface recombination of the photogenerated carriers via surface states due to dangling bonds and other surface imperfections (other passivation techniques may also be applied such as ALD (atomic layer deposition) of Si oxides and Si nitrides); fifth, planarization (filler step) using either spin on glass, polyimide, or plasma enhanced chemical vapor deposition (PECVD) of dielectrics such as Si oxides and Si nitrides; sixth, etch back to expose the P layer or P ohmic metal layer (polyimide or spin-on glass may partially fill the holes or space between the pillars/microstructures); and seventh, ohmic and/or bond contacts formed on the P and N layers. In the case of top illuminated photodetectors, where the optical signal enters on the epitaxial surface where the microstructure patterns are fabricated, a transparent conducting oxide is deposited to connect all the P ohmic metal layers (for pillars). In the case where the microstructures are holes or voids the transparent conducting oxide layer is not used, according to some embodiments. A voltage bias is applied between the P

layer (anode) and the N layer (cathode) of -1 to -20 V, and the photodiode is operated in a reverse bias mode to deplete as much as possible the "I" layer, preferably the entire I layer.

[00123] FIGs. 7A and 7B are cross sections showing aspects of a microstructered avalanche photodiode, according to some embodiments. As in the Si microstructured photodiodes shown in FIGs. 5A, 5B, 6A and 6B, the epitaxial layers 700 for the APD 720 are grown first followed by microstructure processing. The microstructured avalanche photodiode 720 can be illuminated (e.g. with 300-1100 nm) from the top with transparent metal oxide P ohmic contact 726, or the P ohmic contact 726 can be a mirror to reflect the photons illuminating from the bottom (e.g. with 950-1100 nm) to have a double pass absorption. The double pass absorption greatly improves the RC time and the Transit time of the APD for a higher frequency response.

[00124] FIG. 8 is a cross section showing a silicon epitaxial structure for a high-speed high-efficiency microstructured APD, according to some embodiments. Layers 800 are shown prior to microstructure processing. With minor modifications, the n and p doping can be switched and the direction of illumination may also be affected. Starting with a N silicon substrate 802 (or low doped or silicon on sapphire or a BOX /SOI wafer depending on the application and packaging considerations), an N^+ layer 804 (N ohmic contact layer) is formed with doping concentration of greater than 10^{18} cm^{-3} (typically phosphorous) with layer thickness ranging approximately from 0.1 to 10 µm. A non-intentionally doped layer "i" 806 or a P^- (very low doping level P layer) has a doping concentration less than $5x10^{16}$ cm^{-3} (this is the multiplication or electronic gain layer of the APD) with thickness ranging approximately from 0.1 to 2.0 µm depending on gain and bandwidth of the APD. A P charge layer 808 is grown with an approximate thickness 0.05-0.2 µm and doping concentration of greater than $2x10^{17}$ cm^{-3}. An absorption layer 810 is grown (P^- or "i") ("I" and "i" are used interchangeably herein) with doping less than $5x10^{16}$ cm^{-3} with thickness ranging approximately from 0.1 to 5 µm. Finally a P^+ contact layer 812 is grown with doping greater than $5x10^{19}$ cm^{-3} with layer thickness ranging approximately from 0.1 to 1.0 µm. According to some embodiments, all layers 800 are grown epitaxially using CVD or MOCVD reactors.

Doping and thickness are approximate and are adjusted depending on applications.

[00125] For best noise performance of the Si APD, photogenerated electrons should dominate in the multiplication process; i.e. holes diffuse/drift toward p (anode) and electrons diffuse/drift toward the n (cathode) with reverse bias. The Si layers 800 are grown epitaxially using chemical vapor deposition, plasma enhanced chemical vapor deposition, molecular beam epitaxy, atomic layer deposition (can be a combination of these methods to generate the optimal layer structure in doping and interface quality) on doped or undoped substrates. The total length for the electrons to transit range from approximately 0.25 to 7.2 microns. This can be, for example, 0.5 μm for absorption, 0.1 μm for charge, 0.5 μm for multiplication, with a total of 1.1 μm for the APD layer structure 800 shown. According to some embodiments, for higher QE, the absorption region can be lengthened to one μm for a total transit length of 1.6 μm for example. Other layer thickness and doping concentrations can be adjusted to optimize device characteristics for different wavelength, integration with CMOS, application requirements, operating conditions such as bias voltage, gain and noise.

[00126] Also, the APD can be illuminated with modulated optical signal from the bottom, where using BOX or SOI, the bulk of the substrate can be removed to minimize optical losses and thus can use the double pass of the photons in the enhanced absorbing microstructured layer.

[00127] FIGs. 9A-9E are a series of cross sections showing some basic microstructure processing steps, for a high-speed APD, according to some embodiments. FIG. 9A shows the high speed APD epi structure 800 as described with respect to FIG. 8. In FIG. 9B, as in the PD process, a P-ohmic metallization or dielectric mask 910 can be deposited first on the P layer 812 for the microstructured pillars. In the case of holes and/or voids this step may not be carried out. Dry etch mask 910 is deposited on the surface using photolithography, metal/dielectric deposition techniques and wet/dry etching. In FIG. 9C, according to some embodiments, reactive ion etching (RIE) or deep reactive ion etching (DRIE), wet etching using chemicals and oxidation of the Si are used to generate the microstructured pillars 914. Native silicon oxide for surface passivation can be provided by thermal oxidation (which is preferred in some cases), electrochemical

anodization, and/or plasma enhanced chemical vapor deposition. According to some embodiments, the thermal oxidation of the pillars 914 can also be used to fine tune the diameter of the pillar since the oxide is created from the Si material. Thermal oxidation also smooths the surface which is favorable for electrical properties. In FIG. 9D a filler 916 is used to fill or partially fill the space between the Si pillars 914 to support subsequent contact layers to be deposited. The filler 916 can be spin on glass, polyimide, dielectric such as silicon nitride, or silicon oxide, that can be deposited for example using plasma enhanced chemical vapor deposition. Once the contacts are made the fillers can be left in place or removed by dissolving the filler with an etchant or solvent. Removing the filler has an advantage of further reducing the capacitance of the device since air has a dielectric constant of 1. The reduction of the capacitance allows the device to operate at higher bandwidth due to reduction of the RC time. In FIG. 9E, the anode and cathode ohmic contact metallizations 922, 924 and 926 are made. Depending on the direction of illumination, transparent conducting oxide TCO 932 (such as indium tin oxide ITO) can be used. In the case of top illumination, a dry etch can be used to expose the pillars if they are buried in the filler. The TCO 932 can then be used to contact the P^+ silicon pillars at the tip or the P ohmic metallization 922. Ohmic contact metallization is then applied to the cathode (N^+) layer either on the surface (924) or bottom (926) depending on integration topology.

[00128] In the case of the optical signal coming from the substrate side (the bottom), the wafer is thinned. If the thinning is carried out by etching it can include a buried silicon dioxide layer such as silicon on insulator, SOI/BOX, such that the oxide layer can act as an etch stop layer. The wafer can be thinned first by chemical mechanical polishing to 100 μm followed by a via etch to the oxide layer which can be selectively etched off, such that the optical signal only need to traverse a few micrometers of Si bulk material. Anti-reflection coating 930 is applied to the Si surface to minimize reflection loss. Ohmic metallization is applied to the N^+ layer followed by bond metal 924. On the microstructured pillars, ohmic metallization is applied to the P^+ tips (if its not applied already in the preliminary steps), followed by bond metal 922. According to some embodiments, an advantage of the optical signal entering from the substrate surface (i.e. the bottom)

is that the light will bounce and travel twice within the pillar structures, thus increasing the quantum efficiency. According to some other embodiments, the pillars can be made shorter to improve the transit time.

[00129] According to some embodiments, the optical signal can also enter from the edge as shown FIG. 52, *infra*, either in a guided mode or in free space. In the edge application, TCO 932 and solid anode ohmic contacts may not be used and wafer thinning may not be carried out. Cathode ohmic contacts can instead complete the structure. According to some embodiments, in edge approach, the pillars are arranged such that their density is not uniform to optimize the capture of the optical radiation. It can be arranged in a V pattern for example to reduce optical reflection.

[00130] Not shown in FIGS. 9A-9D are mesa etching steps used to define the diameter of the APD 920. According to some embodiments, other methods such as ion implantation may also be used. Note that the microstructures themselves provide good confinement of current in the vertical direction and not in the lateral direction. Other known processing steps that are not shown for sake of simplicity include: thermal oxidation passivation of exposed surfaces; adding guard rings; thinning of the wafer; adding anti-reflection coatings; annealing of ohmic contacts; and creating via holes for removal of filler.

[00131] Taking advantage of low absorption constant of bulk Si. High speed photodiodes made with III-V material often are constructed such than the photocarriers are generated only in the i layer of a PiN structure to minimize the photogenerated carriers outside of the high field region that can cause degradation to the frequency response of the device. This can be done easily in III-V material since there are many ternary and quaternary material such as InGaAsP, InGaAs, InAs, that are lattice matched to InP and the bandgap of these alloys can be changed by altering the composition such that the P+ anode 812 and P charge 808 layers are mostly transparent and the i layer is absorbing. However it is not easy for silicon since there are no materials that are lattice matched to silicon. Germanium can be grown on silicon but with the addition of a buffer layer to accommodate for the lattice mismatch.

[00132] According to some embodiments, a method to overcome this issue in silicon is to take advantage of the low absorption constant of silicon at radiation

near the bandgap of silicon. According to some embodiments, the wafer can be thinned to the insulator of an SOI structure and the 850 nm optical signal will only traverse 1-2 μm of bulk silicon losing approximately 10% or less of the incident radiation. The rest of the radiation continues to the microstructured pillar silicon where the absorption is stronger possibly due to resonance effects. According to some embodiments, the shape of the pillars can be circular, oval, rectangle, chevron, hexagon, double-circle, crescent, star, or any shape to optimize absorption and collection efficiency. The pillar diameter range from 50-1200 nm (smallest dimension can be 50 and largest dimension 1200 nm) and can be spaced uniformly or non-uniformly, periodic or aperiodic, chirped, or a pattern either locally or globally to optimize APD/PD performance and applications. The spacing of the pillars can be 20-2000 nm. The microstructured pillars can be 100 to 10000 nm in length that is optimized for bandwidth and efficiency for a particular wavelength near the silicon bandgap for example 850, 880, 980, 1000 nm.

[00133] According to some embodiments, multiple dimensions (both structure and spacing) of the microstructures within a single PD/APD can broaden the resonance bandwidth of the microstructures such that the enhanced absorption coefficient is over a broader optical spectrum.

[00134] The substrate becomes less absorbing as the wavelength approaches 1100 nm (1.1 eV Si indirect bandgap).

[00135] According to some embodiments, the microstructured pillars/holes/voids can have orientations that are not perpendicular to the surface of the silicon substrate. Other orientations off perpendicular or with multiple orientations or even random or pseudo-random are possible to optimize the QE with respect to the directivity of the optical signal. In multiple and/or random or pseudo random orientations of the microstructures, the device become less sensitive to the direction of light illumination which is beneficial in PV applications. In certain applications, antenna like high directivity of the PD/APD may be desirable to avoid cross talk for example from other optical signal sources or to further improve its QE.

[00136] According to some embodiments, microstructured hole arrays, instead of pillar arrays, are used as light traps in silicon. Microstructure hole arrays have similar properties as microstructured pillars. See e.g. Lin et al, Optical absorption

enhancement in silicon nanowire and nanohole arrays for photovoltaic applications, Next Generation (Nano) Photonic and Cell Technologies for Solar Energy Conversion, edited by Loucas Tsakalakos, Proc. of SPIE Vol. 7772, 77721G (2010). According to some embodiments, instead of etching microstructured pillar arrays as described herein, microstructured hole arrays are etched using RIE/DRIE and similar processing for the pillars, including thermal oxidation for surface passivation, deep ion implantation for electrical isolation, confinement of optical fields and reduction of capacitance. In the case of the hole arrays, it is possible that the filler need not extend the entire length of the hole. For example, if the surface tension of the filler is high, only partial filling of the holes with filler will be possible and provide support for subsequent layers of TCO, metal, oxide, silicide, alloys to name a few that may be necessary to complete the device structure. According to some embodiments, in the case of microstructured holes, fillers are not used in the PD/APD/PV devices since the surface is contiguous rather than consisting of islands as in the case of microstructured pillars.

[00137] According to some embodiments, the microstructured holes can have diameters of 50-3000 nm and can be a square, hexagon, oval, rectangle, chevron, double-hole, with the smallest dimension at 50 nm to the largest dimension of 3000 nm approximately. The spacing between holes (adjacent edges) can be regular or irregular or a pattern at 20-2000 nm. The depth (or length) of the hole can be 100 to 10000 nm and can be uniform depth or non-uniform depth. Dimensions are chosen for optimal absorption, quantum efficiency, bandwidth and radiation collection efficiency for a particular wavelength and application.

[00138] As discussed earlier, to optimize High Contrast Grating in the Absorption regime of this invention, it may be desirable to have the microstructured enhanced absorption structures on materials of a lower refractive index such as BOX or SOI where the silicon dioxide refractive index is lower than that of Si, Ge or III-V/II-VI material. According to some embodiments, the effective refractive index can be made lower than the refractive index of the microstructures with the inclusion of voids in the substrate. FIGs. 10A-10B are cross sections showing aspects of a top illuminated microstructered photo diodes, avalanche photo diodes and/or photovoltaics (PV) with microstructured voids in N-Si, according to some embodiments. Voids can be included in the substrate or as a microstructure for

enhancing absorption coefficient as will be discussed *infra*. Refractive index in the optical spectrum of Si, Ge, III-V material typically range from 3-3.6, by using silicon dioxide such as SOI and voids that are 50% of the material in volume, the refractive index or effective refractive index can be reduced to approximately 0.5 that of the bulk semiconductors. By adjusting the ratio of the volume of the voids to the material (Si for example) the effective refractive index can also be adjusted from a few percent to more than 90% that of the bulk material. The voids can be filled with other material such that it is not just air, gas or vacuum, but a dielectric such as glass, polymer, dielectric, oxide, or amorphous semiconductor that can be optically and/or electrically passive and or active with optical and/or electrical gain for example.

[00139] FIG. 10A shows the layers 1000 including N-Si layer 1006 which contains microstructured voids 1008 that effectively reduce the refractive index of the N-Si layer 1006 as described. FIG. 10B shows a top illuminated PD/APD/PV 1020 that includes microstructured pillars 1024 and/or holes 1022, as well as transparent conducting oxide layer 1026. Microstructered voids 1008 can be random or patterned. The microstructered voids 1008 can be used reflect photons back to the absorbing "I" region if the voids 1008 are patterned to have HCG effects at wavelenghs where loss is low such as 950-1100 nm. According to some embodiments, BOX or SOI substrates can also be used together with voids or without voids or without BOX/SOI.

[00140] According to some embodiments, the microstructuring techniques described herein are also applied to heteroepitaxial material (III-V on Si, Ge on Si, or II-VI on Si). Ge (bandgap 0.66 eV at 300K) having much smaller bandgap than Si, can be used for detecting optical signals at 850 and 1300 nm. Using the techniques described herein, Ge devices can also be made to detect optical signal with wavelength at 1550-1600 nm which can than replace III-V material based photodetectors. According to some embodiments, microstructures are grown such as nano/microwires or etched from bulk material with or without lithographic masking.

[00141] Ge thin film can be grown epitaxially on Si. See, e.g. Kang et al, Epitaxially-grown Ge/Si avalanche photodiodes for 1.3μm light detection, 23 June 2008 / Vol. 16, No. 13 / OPTICS EXPRESS 9365 (hereinafter "Kang et al."), where

an APD was fabricated for 1310 nm wavelength operation for a 30 μm diameter device. The QE of the device with a 1 μm Ge absorption length is only 56% whereas by using microstructured pillars/holes/voids according to embodiments described herein, QE of approximately 90% or greater can be achieved at 1300-1600 nm wavelength with bandwidths of approximately 30 Gb/s or greater for a 30 micrometer diameter PD/APD. Such devices can find useful applications in datacenters, local area networks, and in metro and long distance optical data/telecommunications. According to some embodiments, integration on silicon is used which results in significant cost reduction in manufacturing and packaging. In comparison, in Kang et al. a 30 μm diameter APD was only able to reach approximately 15 Gb/s bandwidth at 1310 nm and cannot extend the wavelength due to low absorption of the bulk material without sacrificing a significant reduction in bandwidth.

[00142] FIGs. 11A and 11B are cross sections showing aspects of an heteroepitaxial APD structure of Ge on Si, according to some embodiments. Layers 1100 and APD device 1120 show a possible heteroepitaxial APD structure of Ge on Si (as opposed to descriptions, *supra*, of homoepitaxial APD/PD structure where only silicon is used with different doping concentrations). Similar processing methods as in the homoepitaxial Si APD are used to fabricate microstructured pillar/hole arrays. According to some embodiments, the absorption constant of bulk Ge is enhanced by greater than 70X, for example 73-172X. According to some embodiments, APDs and PDs with bandwidths in excess of 30 Gb/s can be achieved in devices with an active diameter of 30 μm or less at wavelengths to 1750 nm and QE of approximately 90% or greater. This is a significant improvement over existing Ge on Si APD with illumination normal or off normal to the surface of the substrates.

[00143] According to some embodiments, the microstructured pillar and hole (and variations thereof) arrays can be fabricated in Si, Ge, Ge on Si, SiGe on Si, SiGe on Ge; it can be any combination of Si,Ge and SiGe.

[00144] At longer wavelengths 1200-1800 nm, Ge (germanium) photodiodes are often used since Ge has a bandgap of 0.66 eV (whereas Si has a bandgap of 1.1 eV). However, for high bandwidth applications (greater or equal to 20 Gb/s) Ge photodiodes are only good to 1350 nm due to the fact that for transit times to be

approximately 30 picosec (electron saturated drift velocity is $6x10^6$ cm/s at $1x10^4$ V/cm in order to have a bandwidth of approximately 20 Gb/s ($f(3dB)=0.44/\tau$ where τ is the transit time through the "I" region) the length of the absorption region or the "I" region is limited to approximately 2 microns. At this length, the QE at 1550 and 1600 nm is less than 10%, which is not generally acceptable for optical receivers for datacom and telecom applications. In a waveguide configuration, the length of the absorption region can be 50-100 microns and still achieve 20 Gb/s or higher with QE equal or greater than 90%. The waveguide Ge on Si photodiode structure have been reported by other research groups however such waveguide photodiodes have excess optical losses due to waveguide losses and coupling loss (coupling of optical signal to the optical waveguide) which can be as high as 3 dB or half of the optical signal is lost. The "free-space" coupling (where the optical signal is directed to the PD/APD using elements such as lens, diffraction elements, light pipes, optical waveguides to name a few) of optical signal to the microstructured photodiode and avalanche photodiode have much less optical losses, typically a few percent or less. One of the reason is the large area of the microstructured PD/APD which is 30 microns in diameter as compared to waveguide photodiodes its dimensions are a few microns, typically 1-2 microns. Not only is coupling loss high in waveguide PD/APD, it often uses active alignment which requires that the waveguide PD/APD is turned on to monitor the coupling of the optical signal into the waveguide PD/APD. This active alignment is slow and time consuming which adds cost to the packaging of the waveguide PD/APD in any optical receiver module. In contrast, the large area microstructured PD/APD, according to some embodiments, uses only passive alignment where it is aligned without turning on the microstructured PD/APD. Such alignment is much faster and easier which reduces the cost of a microstructured PD/APD in any optical receiver module. It should be noted that with the effective capacitance of the microstructured PD/APD significantly lower than bulk PD/APD by 10 to 80% or more, the area of the microstructured PD/APD can be correspondingly larger by 10 to 80% or more.

[00145] In FIG. 11B, a microstructured Ge on Si pillars/holes APD structure 1120 with bottom illumination is shown. Epitaxial layers for an APD Ge on Si are used where the optical absorption to generate electron-hole pairs takes place in Ge

and the gain/multiplication of the electrical charged carriers takes place in Si. The epitaxially grown layers are similar to Ge on Si bulk (thin film) APD with the following layer compositions ranges (shown in FIG. 11A). N is undoped, or low doped (20 ohms-cm) Si substrate 1102, which can also be SOI or BOX, to allow removal of the Si substrate for bottom illumination and/or to reduce the refractive index. If SOI or BOX substrates are used, the N ohmic contact and bond metal will be on the N^+ -Si surface adjacent to the multiplication I region. N^+ contact layer 1104 which can be 2-8 microns, $N^+ > 5.10^{18}\,cm^{-3}$. I multiplication layer (or gain layer) 1106 which can be undoped (not intentionally doped), 0.2-1.0 microns thick and $I < 1.10^{16}\,cm^{-3}$. P charge layer 1108 having a thickness of 0.05-0.2 microns and $P \sim 1\text{-}6.\ 10^{17}\,cm^{-3}$. P^- low temp Ge buffer layer 1110 having a thickness of ~ 0.01-0.04 microns and $P^- \sim < 1.\ 10^{16}\,cm^{-3}$. I or P^- absorption layer 1112 having a thickness of 0.2- 2.0 microns, and I (or P^-) $<1.\ 10^{16}\,cm^{-3}$. Finally, P^+ contact layer 1114 has a thickness of 0.05- 0.2 microns, and $P^+ > 2.\ 10^{20}\,cm^{-3}$, approximately.

[00146] Starting with a wafer with all the layers 1100 grown for APD operation, the processing details are left out for simplicity. The basic steps involve first, depositing the p ohmic contact metal layer 1126 using e-beam, thermal or sputtering deposition. The microstructure pattern of either pillars or holes is photolithographically, using positive or negative or image reversal photoresist methods depending on pillars or holes, defined to form the etch mask for either dry or wet etching. According to some embodiments imprint lithography can be used. The microstructure patterns are etched on the P^+ and I (or P^-) and P Ge layers 1114, 1112 and 1110, respectively, partially or fully to the P Si layer 1108 (e.g. using fluorine, chlorine, bromine based gases such as SF_6, CF_4, BCl_2, Cl_2, for selective dry etching using RIE and DRIE). The selectivity of the etch between Ge and Si can be as high as 70, so as to etch Ge 70 times faster than Si by adjusting gases mixtures, pressure, temperature and bias, and power. The sidewalls of the microstructure patterns (pillars or holes) are passivated with dielectric or SiGe and gradually reducing the Ge content such that Si remains on the surface (using for example atomic layer deposition ALD) and subsequently using thermal oxidation to minimize surface recombination of the photogenerated carriers via surface states due to dangling bonds and other surface imperfections. According to some embodiments, other passivation techniques may also be applied such as ALD of

Si oxides and Si nitrides. Planarization is performed using either spin on glass, polyimide, or PECVD deposition of dielectrics such as Si oxides and Si nitrides. An etch back is performed to expose the P layer. For microstructured holes and pillars, it may not be necessary to planarize completely, by using polyimide or spin-on glass to partially fill the holes and spaces between pillars. Ohmic and/or bond contacts are formed on the P and N layers. For top illuminated photodetectors, where the optical signal enters on the epitaxial surface where the microstructure patterns are fabricated, a transparent conducting oxide 1126 (the transparent conducting oxide may not be used in the case of microstructured holes) is deposited to connect all the P ohmic metal layers (for pillars). A voltage bias is applied between the P^+ Ge layer 1114 (anode) and the N^+ Si layer 1104 (cathode) of -2 to -45 V. The APD 1120 is operated in a reverse bias mode to deplete as much as possible both of the "I" layers. Many detailed processing steps are left out such as annealing, surface preparations, deposition of ohmic contacts, bond metal, RIE, DRIE, wet etching, masks for etching, mask removal, antireflection coatings, mirrors such as Bragg reflectors on the microstructured layers, to name a few. Ohmic contact metallization to P and N semiconductors and bond metallizations are well known in the art and details are not mentioned here. Also, holes are used in electron-hole pairs as charged electrical carriers and holes as in a physical void such as the microstructured holes. From context it should be understood if "hole" refers to a charged electrical particle or a physical void.

[00147] According to some embodiments, Ge surfaces of the microstructured pillars or holes and any Ge surfaces exposed to an electric field, where electric current can flow and/or where electric charges are formed are passivated to reduce current leakage, minimize surface states that can be a potential sink or recombination centers for carriers, especially photogenerated carriers of electrons and holes (as in Si, thermal oxide or rapid thermal exidation, to create SiO_2 and SiO_x used to passivate any silicon surfaces that can cause excessive leakage current or recombination centers for photogenerated carriers, or a carrier sink) and GeO_xN_y which is a native Ge oxynitride that is formed in two stages, where the Ge microstructured pillars and/or holes are first exposed to oxygen and then to ammonia ambient in a rapid thermal annealer to form the Ge oxynitride passivation layer. These passivation methods are well known in the art.

[00148] FIG. 12 is a cross section illustrating aspects of a passivation method for Ge surfaces on microstructures, according to some embodiments. Shown are microstructured Ge pillars 1202 (or holes) for a PD and/or APD. On the Ge surfaces is conformally epitaxially grown SiGe layer 1210. Gradually, the Ge content is reduced within layer 1210 until only Si is exposed on the surface. Thermal oxidation of Si is then used to passivate the exposed Si surfaces, forming SiO2 layer 1212, to minimize leakage current and surface states that can be a potential sink for carriers, especially photogenerated carriers (electrons and holes) that can degrade QE.

[00149] FIGs. 13A and 13B are graphs showing the effects of mictrostructure enhancement of Ge bulk absorption coefficient for photodiodes and/or avalanche photodiodes based on Ge on Si, according to some embodiments. According to some embodiments, a 73x enhancement of bulk absorption coefficient is gained in PD/APD devices having microstructured pillars/holes at 1550 and 1600 nm. FIG. 13A shows the bandwidth verses "d" or the length of the "I" layer for 1550 nm (point 1310) and for 1600 nm (point 1312) Note that APDs have both a Ge "I" layer and an Si "I" layer; whereas for PDs have just a Ge "I" layer. FIG. 13B shows QE verses "d" or "I" layer length for 1550 nm (point 1320) and 1600 nm (point 1322). It can be seen that for a 30 micron diameter active region PD/APD bandwidths of 40 and 31 Gb/s can be attained at 1550 nm and 1600 nm optical wavelength respectively with 90% QE. This result was not achievable with bulk Ge photodiodes and avalanche photodiodes of conventional design.

[00150] The separation of using Ge microstructures to absorb the light generating e-h (electron-hole) pairs and using Si for the avalanche multiplication of the carriers, preferably electrons, results in an APD with very low noise due to the fact that the ionization ratio (defined as hole ionization rate/electron ionization rate) for electrons injected into the multiplication region (gain region which is a function of applied reversed bias voltage) is lower than in III-V material family. This result in a low excess noise factor leads advantageously to a high signal to noise ratio (S/N).

[00151] FIGs. 14A-14B are cross sections showing aspects of a top-illuminated Ge on Si avalanche photodiode having microstructured pillars/holes, according to some embodiments. FIG. 14A shows the bulk layers 1400. In FIG. 14B, top

illuminated microstructured Ge on Si APD 1420 is shown with a semitransparent conductive oxide 1426 connecting the P-ohmics on the Ge microsturctured pillars 1424 (holes 1422) as described *supra*. Both top and bottom illuminated microstructured Ge on Si share similar epitaxial structures. The processing steps for top and bottom illuminated microstructured APDs are similar. The main differences are that the transparent conductive oxide for top illuminated APD (or PD) is replaced with an opaque ohmic/bond metallization that can act as a mirror to reflect the optical signal back toward the absorption I layer. According to some embodiments, the mirror can also consist of Bragg reflectors either wafer bond to the microstructure or epitaxially or vacuum deposited such as dielectric or conductive metal dielectrics to enhance the reflectivity to greater than 90% of the optical signal. In addition, bottom illuminated PD/APD may require a window or via where most of the Si substrate is removed to reduce optical losses depending on the wavelength of the optical signal.

[00152] FIGs. 15A-15C are cross sections illustrating aspects of bottom-illuminated Ge on Si avalanche photodiodes having microstructured pillars/holes, according to some embodiments. FIG. 15A shows the bulk layers 1500 prior to forming the microstructures (pillars and/or holes). FIG. 15B shows a Ge on Si microstructured APD 1520 with the optical signal illuminating from the bottom (substrate side) for wavelengths from 1200-1800 nm. Note that Si is basically transparent at these wavelengths. According to some embodiments, to further reduce optical losses, the Si wafer can be thinned just at the area of illumination, for example through a via of 50-500 microns in diameter and thinned to the N^+ layer of the Si; or the Si substrate 1502 can include a BOX or SOI layer 1502. The Si substrate 1502 can then be thinned selectively to the BOX or insulator layer 1502 which can be etched away selectively. According to some embodiments, an anti reflection layer (not shown) can be added to minimize reflection. The advantage of this arrangement is that the optical signal will have a double bounce, reflecting off the metallization 1526 on the Ge P^+ layer 1514 and traversing the Ge "I" absorber region 1512 once again. For example, as shown in FIGs. 13A and 13B, keeping the same absorption length, Ge "I" length, the QE for both 1550 and 1600 nm would be approximately 90% or higher for a Si substrate side (bottom) illumination by the optical signal assuming negligible reflection loss. According to some

embodiments, the Ge "I" absorption length can be further shortened to increase the bandwidth and still maintain acceptable QE.

[00153] For Ge epitaxially grown on Si, it is known that the bulk absorption coefficient is greater than that of Ge bulk by itself (not grown on Si); at 1750 nm the Ge on Si absorption coefficient is approximately 100 cm^{-1}. According to some embodiments, this can be enhanced by the microstructured pillars and/or holes by 172 times. The resulting enhanced Ge on Si microstructured pillar and/or holes absorption coefficient can be about 1.72. 10^4 cm^{-1}.

[00154] FIG. 15C shows an APD 1540 in which the microstructure extends all the way to the N cathode layer 1506 to further reduce capacitance and refractive index. In this case, the absorbing i layer 1512 is microstructured as is the charge layer 1510 and the i multiplication layer 1508. According to some embodiments, the microstructures can also be formed partially into the charge and multiplication layers 1510 and 1508. Additionally, according to some embodiments, the microstructures in the absorbing layer 1512 and the multiplication layer 1508 need not be the same. In FIG. 15D, photons may generate electron hole pairs in the multiplication region which may contribute to added gain but also may contribute to excess noise. According to some embodiments, the absorption and multiplication region using the microstructure APD is combined in one region without the use of the charge layer. This is possible due to enhanced absorption: the length of absorption and multiplication can be of the order of one micron or less allowing reasonable avalanche voltage.

[00155] FIG. 15D shows a microstructered APD 1560 where the absorption and multiplication region are a single region 1566, pillars or holes, according to some embodiments. This is enabled by the microstructure enhancing the absorption coefficient so that less than one micron of the absorbing microstructure length is needed to achieve QE of approximately 90% or more and avalanche multiplication can also occur in this length of material. For example, if 0.5 μm of microstructured Si shown in Fig.15D is the thickness of layer 1566, a back illuminated APD 1560 allows a double bounce of the optical signal reflecting off the N ohmic contact and bond metallization resulting in an effective length of one micron of absorption length. The Si APD 1560 can operate at 0.5 μm multiplication length resulting in gain of 3 dB or more with a reverse bias ranging from -5 to -50 volts. According to

some embodiments, the structure shown in FIG. 15D can be applied to other material systems such as Ge, Ge on Si, III-V, and III-V on Si or not on Si.

[00156] FIGs. 16A and 16B are graphs comparing single pass and double pass photodiodes and/or avalanche photodiodes based on Ge on Si, according to some embodiments. Points 1610 and 1620 show the bandwidth and QE values for single pass with d of approximately 1.4 microns and points 1612 and 1622 show the bandwidth and QE values for a thinner d of approximately 0.7 microns single pass. For double pass the device will have points 1612 for bandwidth and point 1622 for QE. At 1750 nm optical signal wavelength, using absorption coefficient data of 100/cm for Ge on Si and with, for example, 172 times (172X) enhancement factor due to the microstructured Ge on Si photodiode/avalanche photodiode structures, a bandwidth of 27 Gb/s and a QE of approximately as high as 90% can be attained with an "I" (also "d") length of approximately 1.4 microns for a single pass (top illuminated - where the optical signal illuminates the top Ge microstructured side). As mentioned earlier, for photodiodes the "I" or "d" is the absorption length, whereas for avalanche photodiodes the "I" is the combined absorption length and the multiplication length. For example, for an APD to achieve 27 Gb/s the total "I" length needs to be limited to 1.4 microns. A double pass arrangement can be used such that for example the absorption length is 0.9 microns and the multiplication is 0.5 microns, making the absorption length effectively 1.8 microns to achieve QE above 90%. However, if we instead have the optical signal illuminate from the bottom Si substrate side, the Si substrate and Si layers are basically transparent and have minimal optical losses (approximately 1-3 dB/cm) at optical radiation energies that are below the bandgap of Si (1.1 eV or 1127 nm wavelength at 300K) for example for radiation from 1200-1800 nm wavelengths. The advantage of illuminating from the Si substrate side (bottom) is that the optical signal can have a double pass at the Ge "I" absorbing region if the metallization on the P^+ contact layer is reflective which it should be since it is metallic composing of Au, Al, Ag, Cr, Zn, Ti, Ta, Ge, or a combination of these metals and semiconductors. Bragg reflectors consisting of material with alternating refractive indices from oxides, nitrides, chlorides, semiconductors, either wafer bonded to the microstructures or deposited on the microstructures can also be incorporated. Reflectivity can be greater than 90%. With double pass, as shown in

FIGs. 16A and 16B, a bandwidth of 40 Gb/s can be attained with a QE approximately as high as 90% or more.

[00157] FIGs. 17A-17B are cross sections showing aspects of a top-illuminated Ge on Si photodiode structure having microstructured pillars/holes for applications with signal wavelengths ranging from 700 to 1800 nm, according to some embodiments. FIG. 17A shows the bulk layers 1700. In FIG. 17B, Ge on Si microstructured pillars 1724 and/or holes 1722 are in a configuration for photodiode 1720. This is essentially a P-I-N structure where the "P" and "I" are Ge with microstructured pillars 1724 and/or holes 1722 to enhance the bulk absorption coefficient of Ge grown on Si. The increase in the absorption coefficient of Ge grown on Si (Ge on Si) could be due to the stress build in the Ge epitaxial layer due to lattice mismatch with the Si host substrate that it is grown on. Optical signal as in the case for Ge on Si APD can be illuminated from either the microstructured side (as in FIG. 17B) or the substrate side (as in FIG. 18B).

[00158] FIGs. 18A-18B are cross sections showing aspects of a bottom-illuminated Ge on Si photodiode structure having microstructured pillars/holes for applications with signal wavelengths ranging from 1200 to 1800 nm, according to some embodiments. FIG. 18A shows the bulk layers 1800. FIG. 18B shows photo diode 1820 configured for signal illumination from the Si substrate side (bottom illumination) with photo energies that are less than the Si bandgap of 1.1 eV at 300K. The corresponding wavelength range is 1200 to 1800 nm. Ohmic contact 1826 can also act as a mirror such that the light makes a double pass of the Ge absorbing microstructures where the metal contact layer on the P Ge can reflect the optical signal back toward the Ge "I" absorbing layer.

[00159] It should be noted that in all the discussions of the P-I-N structures, according to some embodiments the P and N are interchanged such as with an N-I-P structure formed on a P substrate or on a low doped P substrate or undoped substrate. According to some embodiments, the N and P for the APD structures are also interchanged and the substrate can be P, low doped P or undoped. However, in an Si multiplication layer, to achieve the lowest noise and the best S/N, electrons are injected into the multiplication region as dominantly as possible since the ionization rate of electrons is higher than the ionization rate of holes in Si; the ionization ratio for Si can range from 0.06 to 0.002 where as compared to Ge

and InGaAs it is 0.9 and 0.45 respectively. This is why in many of the embodiments described herein the enhanced absorption is in Ge microstructures and the gain or multiplication which is dependent on the field strength and therefore on the applied reverse bias voltage which for the described devices can range from -10 to -60 V, is in Si.

[00160] According to some embodiments, the microstructured pillars and or holes for Si and Ge on Si photodiodes (PD) and avalanche photodiodes (APD) are used to replace relatively expensive III-V photodiodes. The Si microstructured pillars and holes PD/APD can operate from 500 to 1100 nm at bandwidths of 20 Gb/s or higher and QE of 90% or higher. In particular, the datacom wavelengths of 730-980 nm. The microstructured pillars and or holes on Ge epitaxially grown on Si PD and APD can operate from 500-1800 nm with bandwidths of 20 Gb/s or more and QE of 90% or more. In particular, the telecom wavelengths of 1250-1600 nm and possibly to 1750 nm. The techniques described herein thus extends the wavelengths, bandwidth and QE of conventional Si and Ge on Si free space coupled photodiodes and avalanche photodiodes.

[00161] According to some embodiments, the microstructured pillars can also be fabricated using VLS (vapor-liquid-solid epitaxy) growth of Ge nanowires on an Si substrate. Others have demonstrated the growth of vertical Ge nanowires on Si (111) orientation for example, with Au nanoparticles as catalysts for the VLS epitaxial growth using chemical vapor deposition (CVD) or metal organic chemical vapor deposition (MOCVD). Crystal orientations other than (111), or with materials with multiple orientations such as in polycrystalline may be used. Materials such as Si, Ge, III-V, glass, quartz, metal, to name a few can also be used as substrates. According to some embodiments, a thin Ge buffer layer of approximately 2nm on Si (111) substrate is formed together with Au nanoparticles as catalysts for VLS growth in a CVD reactor. The Au catalyst can be deposited using a lithography mask to expose photoresist that is coated on the Si substrate. The Au is evaporated onto the Si substrate with patterned photoresist. Using standard processing methods such as lift-off, the Au pattern is left behind on the Si substrate which is then the catalyst for Ge VLS growth on Si substrates. According to some embodiments, it can also be grown using selective area growth where a dielectric

mask is deposited on the Si substrate with a pattern of voids that allow Ge to grow in the void using CVD.

[00162] The microstructure of pillars and holes on the surface of a bulk photodiode not only enhance the absorption coefficient by factors ranging from 10-200 over the absorption coefficient of bulk material (material without any microstructured features and grown on lattice matched substrates so that stress due to lattice mismatch is minimal) but also significantly reduce the capacitance of devices such as PDs and APDs. The reduction in capacitance allows the PD or APD to have a shorter absorption length, which in turns result in a faster transit time for the photogenerated carriers to be swept out of the high field region. The absorption region typically is depleted as much as possible by the reverse bias voltage that is applied externally with an electric field strength approaching 10,000 V/cm or higher. If the microstructured pillars or holes can result in removing half or more of the semiconductor material, which for silicon has a dielectric constant of 11.9 and germanium have a dielectric constant of 16, replacing the removed material with either air (dielectric constant of 1) or polyimide (dielectric constant of 3.5) or other dielectrics with low dielectric constants, then the overall capacitance can be estimated to be the sum of the capacitance due to the total area occupied by the semiconductor and the capacitance due to the area occupied by air or polyimide. C(total)=C(semiconductor)+C(air or polyimide) where $C= \varepsilon A/d$ where ε is the dielectric constant times the free space permittivity ($8.854\ 10^{-14}$ farads/cm), A is the area occuped by the semiconductor or air/polyimide and d is the length of the "I" region which can be the absorbing region or the absorbing and multiplication region as in the case for APD. From the equation for C(total), the more semiconductor material which has a high dielectric constant removed and replaced by low dielectric material such as air/polyimide/ SiOx/spin on glass the lower the overall capacitance and the faster the RC time. This reduction of capacitance for PD and APD invention can be extended to other PD and APD such as those of III-V material, microstructures can be fabricated on its surfaces and extend into and pass the optical signal absorbing regions to remove half or more of the semiconductor material to reduce its capacitance and can effectively make a larger area PD/APD and have the same bandwidth as before etching microstructures on the device. The larger area allows for easier coupling of the optical signal to the

photodetector. A simple formula for the increase in radius for example by replacing semiconductor material with low dielectric material is: $r=(\varepsilon_1/((\varepsilon_1-\varepsilon_2)x+\varepsilon_2)))^{1/2} r_o$ where x is the fraction of semiconductor area left, ε_1 is the dielectric constant of the semiconductor, ε_2 is the low dielectric material such as air or polyimide or spin on glass, and r_o is the radius of the active area of the PD/APD before etching microstructured pillars and or holes. As an example, for a 20 micron diameter Ge photodiode with $\varepsilon_1=16$ and for simplicity $\varepsilon_2=1$ (air) and x=.5 (half of the semiconductor material is removed in the microstructured pillar or holes), the increase in the new radius with the same capacitance as the non-microstructured Ge PD is 13 microns or a diameter of 26 microns which is significantly larger than 20 microns and can significantly reduce the cost of coupling the optical signal into the microstructured large area photodetector. This reduces the cost of passive packaging of the optical receiver module and increase the yield.

[00163] FIGs. 19A, 19B and 19C are diagrams illustrating how mictrostructures can reduce capacitance of a photodiode such that a larger area photo diode can be fabricated with the same bandwidth and QE, according to some embodiments. FIG. 19A shows the bulk layers 1900 in an InP-InGaAs-InP structure. In FIG. 19B, the InP-InGaAs-InP layers with microstructured holes 1922 effectively reduce the capacitance of the photodiode 1920 to allow a larger area photodiode to be fabricated with the same bandwidth and QE. FIG. 19C is a top view showing PD 1920. The microstructured holes 1922 can be 100-1000 nm in diameter with depth of 0.1 to 3 microns. Also visible in FIG. 19C is contact ring 1930 and bond pad 1932. According to some embodiments, a complementary microstructured pillars can also be fabricated. According to some embodiments, the sidewalls of InP and InGaAs can be passivated with SiOx, SiNx (silicon oxide and silicon nitride via ALD or PECVD), polyimide or spin-on-glass that can be spun on using standard processing methods. The absorption coefficient of the bulk material can be enhanced by up to two orders of magnitude or more.

[00164] According to some embodiments, III-V material such as InP, InGaAs, InGaAsP, InAs, InSb, GaSb, InGaSb on Si, Ge on Si, is epitaxially grown in a sub micrometer selective area growth (SAG) or vapor liquid solid (VLS) (See, e.g. Sarkar et al, Heteroepitaxial growth dynamics of InP nanowires on silicon, Journal of Nanophotonics, Vol. 2, 021775 (12 February 2008); Roest, et al, Position-

controlled epitaxial III–V nanowires on silicon, Nanotechnology 17 (2006) S271–S275) heteroepitaxy using metal organic vapor epitaxy with or without catalyst which can consists of Au, Cu, Al, Ti, W, Fe, Cr to name a few. Also for vertical oriented microwires grown on silicon, wafers with surface orientation (111) are selected. It is not necessary that the microwires be normal to the surface, it can be off normal and even have a mixture of orientations.

[00165] In VLS growth, the silicon wafer that has the layer structure for APD or PD just prior to heteroepitaxial growth is photolithographically (or e-beam or nanoimprint lithographically) patterned with aperture ranging from 10-5000 nm, and spaced between 10-3000 nm. An Au deposition (e-beam, or thermal evaporation) follows with thickness of 0.1-10 nm, followed by a lift-off, VLS epitaxial growth in a MOCVD reactor.

[00166] For SAG growth (See, e.g. Chu et al, Wurtzite InP nanowire arrays grown by selective area MOCVD, Phys. Status Solidi C 7, No. 10, 2494 – 2497 (2010)), a 50 nm SiN_x is PECVD (or sputtered or ALD) deposited on a (111) oriented Si wafer with the necessary APD or PD epitaxial layers grown on it ready for heteroepitaxial growth. Using lithography (photo, e-beam or nanoimprint) apertures are defined with dimensions ranging from 10-5000 nm and spaced between 10-10000 nm followed by dry etching (RIE) to open a via to the silicon surface. The wafer is then ready for SAG of Ge, III-V microwires in a MOCVD reactor.

[00167] Detailed processes such as surface treatments, surface preparations, annealing, plasma etching, are not described for simplicity. These processes can be found in the literature.

[00168] FIGs. 19D and 19E are cross sections showing aspects of fabricating an APD device having a III-V absorbing layer grown on a P-I-N silicon multiplication layer, according to some embodiments. In FIG. 19D, a Si APD structure 1940 is etched as shown for v epitaxial growth of the III-V material. In FIG. 19E a III-V absorbing layer is grown on P-I-N silicon multiplication layer for APD device 1960. As in the III-V on Si for a PD device, the III-V nanowires or microwires can be grown on Si using VLS process with or without catalyst. Since the footprint of the nano/microwires on Si is of the order of a micron, defects due to stress from lattice mismatch are not a significant issue and high quality III-V nano/microwires can be

grown on Si. According to some embodiments, SAG is used for fabricating III-V microstructures on Si electronic gain layers.

[00169] From FIGs. 19D and 19E it can be seen that the InGaAs on Si APD 1960 starts with a Si APD structure 1940 where microstructures of holes or pillars are etched to the charge layer 1944 or just before the charge layer 1944. According to some embodiments, the microstructure holes and/or pillars can be etched into the multiplication layer 1942. Then using a process, for example SAG, with or without silicon oxide on the Si microstructure's sidewalls, I-InGaAs is grown, ending with P-InGaAs at the surface. Surface growth can use a process such as epitaxial lateral overgrowth (ELOG) to form a continuous P-InGaAs film of high quality. P ohmic alloy and bond metal 1966 are formed and annealed on the P-InGaAs. The back side processing consist of thinning the Si wafer using for example a BOX layer for selective etch stop and removing the BOX layer. Anti reflection can be coated on the backside silicon to reduce reflection. N ohmic 1968 is fabricated on the N Si layer. The optical signal is illuminated from the bottom. A reverse bias of -5 to -50 volts is applied to the cathode and anode. As mentioned earlier, the small footprint of the InGaAs on Si microstructure of the order of 10 square microns allows for high quality InGaAs material to be grown where lattice mismatch causing crystal defects are not significant.

[00170] According to some embodiments, the integration of Ge, III-V with Si PDs, PVs (See, FIG. 25C, *infra*.) and APDs allow the absorption spectrum of Ge and III-V material on a mature Si electronic platform. It allows integration of III-V with Si CMOS ICs for example for photodetector, optical light source such as light emitting diodes (LED) and laser diodes (LD) and III-V electronics such as transistors.

[00171] Multiple absorbing material and voids as microstructures. According to some embodiments, the microstructured pilllars and/or holes are regrown with Ge such that both Si and Ge are microstructured to enhance the bulk absorption coefficient. According to some embodiments, voids can also be buried or embedded to generate a buried/embedded microstructure such that the surface is more planar. The microstructured voids can also enhance the absorption coefficient, by being patterned so as to enhance reflection and also to reduce the effective refractive index of a material (e.g. Si), reduce the weight of the device,

and increase mechanical flexibility. The microstructured voids can be random, pseudo-random or patterned typically with dimension and spacing that are approximately the order of a wavelength or subwavelength. According to some embodiments, instead of combining Ge with Si, others combinations can be used for example III-V with Si or other semiconductor material, polymers, or other non semiconductor absorbers, which can significantly broaden the absorption spectrum over that of a single absorber.

[00172] The enhancement using nanowires (See, e.g. Garnett et al, Light trapping in silicon nanowire solar cells, Nano Letters, 2010, 10, 1082-1087; Kelzenberg et al, Enhanced absorption and carrier collection in Si wire arrays for photovoltaic applications, Nature Materials, vol. 9, March 2010, 239-244) and nanoholes (See, e.g. Lin et al, Optical absorption enhancement in silicon nanowire and nanohole arrays for photovoltaic applications, Proceeding of SPIE, Vol. 7772, 77721G-1, 2010) have been reported by various groups. The known use of nanowire for light trapping are for photovoltaic applications where the photogenerated carriers diffuse to the anode or cathode of a P-N junction with zero external bias, operating at DC (direct current). According to many of the embodiments described herein, the photogenerated carriers are swept out with an external reverse bias in the absorbing "i" region of a P-I-N diode (PD) or P-I-P-I-N diode (APD) for high modulation bandwidth (e.g. greater than or equal to 10 Gb/s bandwidth) and high quantum efficiency and for APD for high current gain (e.g. gain greater than 3 dB). In addition, according to some embodiments, multiple absorbing materials can be used to broaden the absorption spectrum. The multiple absorbing materials are connected in parallel as current sources whereas in known technology the absorbing materials are connected in series. In addition, the use of voids as microstructures to enhance the absorption of the material according to many embodiments described herein allows the surface to be more planar and simplify processing since fillers may be avoided. Also, the more planar surface allows the epitaxial growth of semiconductor Bragg reflectors to enhance reflection for double or multiple pass absorption in the I absorption layer of the PD/APD. According to some embodiments, Dielectric Bragg reflectors can also be used in a more planar surface since the surface can be highly N or P doped and the ohmic contact can be made on the periphery such as a ring ohmic contact and the

dielectric Bragg reflectors deposited on the photosensitive area such as shown in FIG. 29, *infra*. Chemical mechanical polishing (CMP) can be used to smooth the surface of the epitaxial layer with buried voids.

[00173] Further aspects of fabricating devices having microstructured Ge that is buried or embedded in Si microstructure will now be described. FIG. 20 shows bulk layers without a final P-Si layer for devices having microstructured Ge buried or embedded in an Si microstructure, according to some embodiments. The final P-Si layer, according to some embodiment will be the last layer grown in the epitaxial structure where the first layer grown is the layer adjacent to the substrate, followed by the second layer that is adjacent to the first layer, and so forth to the last layer grown. Shown in FIG. 20 is P-I-N PD structure 2000 and a P-I-P-I-N APD structure 2020 both without the final P-Si layer. In many of the embodiments described herein, N can refer to N (mid N type doping of 5. 10^{16} cm^{-3} to 8. 10^{17} cm^{-3}, low N doping less than 1. 10^{17} cm^{-3}, and high N doping greater than 5. 10^{17} cm^{-3}, with the same for P doping. I (or i) doping is commonly defined as intrinsic, or not intentionally doped or low doping back ground doping of less than 5. 10^{16} cm^{-3}. The "I" region is configured such that the field of a P-I-N junction is developed across the "I" region usually with an external reverse bias. In PD and APD applications, the absorbing material is in the "I" region so that the photogenerated carriers can be quickly sweep to anode (P) and cathode (N) layers. For APDs, the carriers (electrons in most cases shown here, since this gives the lowest noise APD) are swept to the second "I" region for multiplication (current gain) before transiting to the cathode layer). In the Figures herein, P-I-N, P-I-P-I-N structures are shown and the top P layer(s) that are in contact to external circuits are referred to as the anode and the N layer(s) that are in contact to external circuits are referred tp as the cathode; the layers can be interchanged from P to N and N to P with P or low dope substrates to also fabricate PD's and APD's.

[00174] FIG. 21 is a cross section showing etching of microstructured pillars and/or holes for devices having microstructured Ge buried or embedded in an Si microstructure, according to some embodiments. The microstructure pillars 2104 and/or holes 2102 are etched into the I-Si layer, partially or entirely or to/into the N (PD structure) or P (APD structure) Si layer. The etching process can be one of the following: wet chemical etching, dry etching using reactive ion etching (RIE), a

deep reactive ion etching (DRIE), ion milling, and/or focused ion beam milling. The etching can be isotropic or anisotropic or a combination of isotropic and anisotropic. As shown in FIGs. 22 and 23, *infra*, Ge is then regrown in the etched region (i.e. the area around the pillars and on the sidewalls of the pillars in the case of pillars, or area in the holes, sidewalls of the holes in the case of holes) isotropically, anisotropically, or by selective area growth (SAG) where a dielectric layer such as SiOx, SiNx, cover area where regrowth of Ge is not desired which in some embodiments can include the sidewalls. During etching if a dielectric mask material such as SiOx, SiNx, SiCx is used and left in place during epitaxial growth, the epitaxy layers may not grow on the dielectric mask in a crystalline film and may be amorphous in nature or may not grow on the dielectric layer other than some dendrites. Note that the isotropic or anisotropic growth rate often depends on the crystal plane it is growing on and any etched structures may expose multiple crystal planes resulting in different growth rates at those planes that can lead to anisotropic growth in the etched regions with 3D microstructures.

[00175] Growth of Ge on Si is well documented in the literature where a thin buffer Ge layer is first epitaxially grown at a lower temperature followed by a higher temperature Ge epitaxial growth using chemical vapor deposition (CVD), molecular beam epitaxy (MBE), atomc layer deposition (ALD), low pressure -CVD, and or a combination of growth techniques, for example the thin Ge buffer layer can be grown by MBE and the high quality thicker Ge film grown by CVD. The thin Ge buffer layer is to allow lattice mismatch stress to be accommodated between Si and Ge, (see, e.g. Feng et al, High-speed Ge photodetector monolithically integrated with large cross-section silicon-on-insulator waveguide, APPLIED PHYSICS LETTERS 95, 261105 ,2009).

[00176] The Ge regrowth may have voids or non-planarities and, where useful, the surface can be planarized using polishing such as chemical mechanical polishing (CMP) or etching. FIG. 22 is a cross section showing a device having microstructured Ge buried or embedded in an Si microstructure, after the Ge "I" layer is grown in the etched region and planarized, according to some embodiments. Note that according to some embodiments, planarization is not needed and is omitted. After the Ge "I" layer 2202 is grown and planarized, a P^+ Ge capping layer 2204 is grown to complete the P-I-N structure of a PD or P-I-P-I-

N structure of an APD. Optical signal or photons with wavelengths ranging from 400 to 1800 nm can illuminate the PD/APD 2220 from the anode (top) side (P^+ side) 2202 and optical signal or photons with wavelength ranges 950-1800 from the substrate side (bottom) since Si is mostly non-absorbing at these wavelengths. According to some embodiments, it is advantageous to configure the device 2220 for illumination from the substrate side since this will allow a double bounce of the optical signal or photons within the absorbing Ge microstructures embedded in Si. Shown in these figures are only the basic epitaxial layer structures. Structures and layers not shown for simplicity include: anti-reflection coatings, passivations, ohmic metals, bond metallization, any metal interconnect to CMOS, via's for electrical connectivity, arrays of PD/APD for multichannel optical interconnects, to name a few. Optical signal/photons can illuminate either normal to the surface or at any angle off normal, including rotation angles for optimal PD/APD performances; optimizing QE and bandwidth of the PD/APD.

[00177] FIG. 23 is a cross section showing a device having microstructured Ge buried or embedded in an Si microstructure, after I-Ge regrowth and planarization, and a cap layer of P-Si, according to some embodiments. In the case of FIG. 23, the buried Ge microstructures 2302 are capped with a P^+ Si layer 2304. The Si P^+ cap layer (anode) 2304 has low optical loss at optical wavelengths of 950-1800 nm and therefore generates minimal photocarriers that are not in the high field "I" region of the PD/APD 2320 and contribute minimal diffusion photocurrent which can lead to a degradation of the frequency response of the PD/APD 2320 and the QE of the PD/APD.

[00178] Some dimension doping ranges for the buried or embedded Ge and capping layers shown in FIGs. 20-23 will now be provided in greater detail, according to some embodiments. The dimension of the microstructured Ge (e.g. 2202 and/or 2302) can range in depth from 0.1 to 5 micrometers, have a lateral dimension range from 10-5000 nm, and a spacing between adjacent microstructure structures (the structures can be identical or non-identical) in contact (overlapping) to 5000 nm. The "I" doping for both Ge (2202 and/or 2302) and Si (2104) is less than or equal to 5. $10^{16}/cm^3$. "I" is often called intrinsic or not intentionally doped and can have either a p or n background doping, the doping level is low enough that a reverse bias voltage of -2 to -45 volts can fully deplete the "I" region of

mobile holes or electrons (carriers). The capping layer, Si (2304) or Ge(2204) thickness can range from 0.1 to 5 μm with doping level greater than or equal to 6. $10^{17}/cm^3$. These parameters can be adjusted to other values, but the goals are to increase or optimize the QE and bandwidth of the PD/APD for a given application. Series resistance, photogenerated diffusion current, ohmic contacts, capacitance, transit time, depletion of the "I" absorption region all contribute to the performance of the PD/APD. In addition for double/multiple bounce within the "I" region for optical signal illuminating from the bottom substrate side, a reflective metal or dielectric stack such as a Bragg refelctor/mirror consisting of alternating dielectric layers of different refractive indices or HCG can be used to reflect the optical signal back into the microstructured absorbing region at the top anode side. With the Si cap layer as in FIG. 23, the optical signal can illuminate the Si P^+ cap layer (anode) 2304 and, since Si has minimal losses at 1100-1800 nm (below bandgap radiation), it can also have double bounce of the optical signal within the microstructured buried/embedded Ge 2302 by providing a reflector such as a Bragg reflector epitaxially grown at the Si N^+ layer or at the Si substrate to reflect the light back into the absorption region.

[00179] According to some embodiments, all the discussions of microstructured layers herein, light can additionally impinge from top and bottom surfaces, as well as on the sides of the microstructures, either directly or from scattering, near field effects, interferences, or resonance, which can vastly improve the QE of the microstructured photosensors since photogenerated carriers are generated directly in the high field absorbing "I" ("I") layer(s).

[00180] According to some embodiments, dopant choices for Si and Ge (group 4 elements) include the following: (1) for donors (n-type) from group 5 elements - antimony, phosphorus, and arsenic; and (2) for acceptors (p-type) from group 3 elements - boron, aluminum, and gallium.

[00181] It is also noted that in the structure shown in FIG. 23, the I-Ge microstructures 2302 buried in Si 2104 are completely surrounded by Si which has a lower refractive index than Ge. At 1000-2000 nm wavelength range, the refractive index of Si is approximately 3.49 and for Ge is 4.1. The index ratio of Ge/Si is 1.17 so according to Chang-Hasnain reference, HCG effects will exist. The resonance and field concentration in the absorbing Ge microstructures can further enhance

the absorption coefficient from that of the bulk absorption coefficient value anywhere from greater than 1X to several orders of magnitude. The index difference also causes light to be confined and concentrated in the high index material, in this example, Ge; further improving QE.

[00182] The silicon (Si) microstructure can detect photons with wavelength ranging from 300-1100 nm and the germanium (Ge) microstructure can detect photons with wavelengths ranging from 300-1800 nm. According to some embodiments, for high bandwidth and high QE, the shorter wavelengths, 300-600 nm, may generate photocarriers outside the "I" region resulting in a diffusion current that can result in non-optimal bandwidth and or QE. Where bandwidth is not an issue, the degradations may not be very significant.

[00183] FIGs. 24A and 24B are cross sections showing aspects of a microstructured APD with buried/embedded I-Ge absorbing microstructures in I-Si microstructures, according to some embodiments. FIG. 24A shows the bulk layers 2400. In FIG. 24B, the etched pillars 2424 and/or holes 2422 are filled with I-Ge (intrinsic-Ge, non-intentionally doped or undoped or low doped Ge) and finished with a capping layer 2426 of P^+ Ge or Si to complete the anode of the APD 2420. The microstructured Ge 2422 is buried/embedded in Si 2412. Optical signal of wavelength 950-1800 nm (or photons from 300-1800nm where the shorter wavelengths, 300-900 nm, may not have as high a bandwidth) can illuminate the APD 2420 from either top or bottom at various angles to the normal and/or normal to the surface. According to some embodiments, the starting layers prior to the I-Ge regrowth into the etched regions can also include the P^+ Si layer 2426, such as shown in FIG. 7 with layer 726, *supra*. In the case shown in FIG. 24B, the starting layer was removed to minimize P dopant diffusion during I-Ge regrowth. The buried or embedded Ge microstructure in Si microstructure allows the APD (or PD) 2420 to operate in two regimes. A first regime is at wavelengths where Si is low loss and Ge is absorbing or high loss (950-1800 nm). In this Si low loss regime, the Ge microstructures 2422 with a Si P^+ anode cap layer 2426 is completely buried in Si which has a lower refractive index than Ge. The Ge microstructure arrays can have HCG low Q with Q ranging from 1 to 3000 approximately (or other resonant, scattering, near field, linear and non-linear optical effects) or high enhancement of the absorption coefficient. A second regime is where both Si and

Ge are absorbing, 300-945 nm, and both Si microstructures 2424 and Ge microstructures 2422 work in parallel (parallel current generators) absorbing the photons with enhancement of the absorption coefficients of both Si and Ge. This is particularly advantageous for examples in photovoltaic applications.

[00184] FIGS. 25A - 25C are cross sections showing aspects of a photodiode having buried/embedded Ge microstructures in a Si microstuctured pillar and/or hole array, according to some embodiments. Starting with a Si PD epitaxial layer structure 2500 with or without the P layer 2526, microstructures of holes 2522 and/or pillars 2524 are etched into the Si P layer 2526 and I layer 2512 and can extend into the N layer 2510. Regrowth of Ge 2522 (or III-V material such as InGaAs, InAs, InSb, GaN, InGaN to name a few) using a process such as SAG with our without silicon oxide on the sidewalls of the Si microstructure 2524 or using a process such as VLS with or without catalysts, the I-Ge layer 2522 is grown followed by P Ge 2526 (or a P-Si layer which may be more suitable for top illuminated devices) at the surface where a process such as ELOG can be used to form a contiunous P-Ge film. P ohmic alloy, annealed, followed by bond metallization completes the contact 2528 for the anode. The back side processing as discussed earlier is deposited on the silicon surface to reduce reflection. See, e.g. FIGs. 19A-19C, *supra*, where the silicon is thinned and etched to the BOX layer selectively. The BOX layer is etched selectively and an anti reflection N ohmic alloy is formed on the N-Si layer, annealed and followed by bond metallization, which completes the cathode contact. Reverse bias of -2 to - 10 volts is applied between the anode and cathode for high bandwidth PD applications. In PV applications, 0 bias is applied.

[00185] According to some embodiments, the dimensions and doping are similar to the Si microstructured PD shown in FIGs. 5A-5B, *supra*, with the I-Ge doping level less than 5. 10^{16} cm^{-3}, and dimensions ranging in thickness of 0.1 to 5 micrometers, and lateral dimension of the microstructure ranging from 10 to 5000 nm with adjacent structures that can touch/overlap to 5000 nm separation. Optical signal/photons can either illuminate from the anode top side or cathode bottom side with wavelength range of 300-1800 nm and normal to the surface or at an angle to normal which can also include rotation. For bottom side illumination, the Si is thinned down to a few micrometers thickness for illumination at wavelength

ranges of 300-900 nm. Only the basic layers are shown for simplicity. For example, the following structures are not shown: isolation mesa or diffusion or ion implantation, passivation, anti-reflection, ohmic metal, guard rings (e.g. for an APD). Both Si microstructures and Ge microstructures can detect the optical signal/photons in parallel for wavelengths where both are absorbing, 300-1100 nm, and only the Ge microstructure at wavelength ranges 900-1800 nm. The cap layer 2526 and 2546 in FIGs. 25B and 25C respectively can be either P^+ Si or P^+ Ge. For broad modulation bandwidth (sometimes just referred to as bandwidth) of greater than 10 Gb/s (gigabits per second), P^+ Si cap layer is preferred for wavelengths ranges from 950 to 1800 nm, since at these wavelengths Si has low optical losses (also referred to low loss). According to some embodiments, the structure shown in FIGs. 25B and 25C can also be use for photovoltaic applications where no external bias is purposely applied in the reverse direction.

[00186] According to some embodiments, for all the structures shown, the P and N can be interchanged to form for example N-I-P structures for the PD and PV (photovoltaic) and N-I-N-I-P structures for the APD.

[00187] The regrowth of Ge microstructures in Si also have applications in photovoltaic devices where the device is operated without external reverse bias. The P-I-N PD structure for example with Ge microstructures embedded or buried in Si microstructures effectively have two bandgaps, Si bandgap and Ge bandgap that is exposed to the solar radiation. The combination of two bandgaps widen the absorption spectrum of the photovoltaic device and therefore can collect a broader spectrum of the solar energy. The two bandgaps can have a higher QE and or short circuit current over that of single bandgap photovoltaic devices or multiple devices connected in series. The microstructures also have enhanced absorption that can further improve the QE and or short circuit current of the photovoltaic device. The solar spectrum at AM 0 and AM 1.0, with a photovoltaic device with a spectrum width of 300-1800 nm, at least approximately 90% of the solar spectrum is captured. In addition, in the PV device with Ge and Si microstructures are adjacent laterally to each other (i.e. in parallel) rather than being vertically adjacent (i.e. in series) as in prior art PVs. This allows the Si and Ge to be exposed to solar photons equally and are parallel current generators that are additive; $I_{Si} + I_{Ge} = I_{total}$

where I_S is the photocurrent generated by the Si microstructures and I_{Ge} is the photocurrent generated by the Ge microstructure and I_{total} is the total photocurrent.

[00188] Although according to some embodiments the use of Si and Ge are described, according to some other embodiments, other materials are used. According to some embodiments, Si is used with an InP microstructure embedded or buried. According to some embodiments, more than two materials are used such as Si, Ge, InGaAs, InP, GaAS, GaN, InGaN, InSb, to name a few. The microstructures, in addition to pillars and holes, can be embedded and or buried to use the effects of HCG to enhance the absorption coefficient over that of bulk absorption coefficient to further improve QE and minimize the use of material in order to reduce cost of manufacturing.

[00189] FIG. 25C is a cross section showing grown Ge, InP, InGaAs to name a few, within silicon microstructures. SAG can be used where the sidewalls of the microstructures are oxidized or coated with a conformal dielectric and where the oxide/dielectric is removed at the bottom of the microstructure surface where it is approximately parallel to the silicon substrate where it can provide crystalline information for the growth of Ge, InP, InGaAs microstructures. The area where the Ge, InP, InGaAs will epitaxially grow with or without catalysts using various growth methods such as VLS, MOCVD, CVD to name a few, is approximately 100 square microns or less; more typically around 0.3-3 square microns. Because of the small area, crystalline defects due to lattice mismatch are not significant. The sidewalls with the silicon dioxide that can be thermally grown or deposited using ALD, provide an electrical insulation between the Si and the Ge, InP, InGaAs SAG grown layer. It should be noted that SAG growth can continue until the Ge or InP or InGaAs (to name a few) can merge above the silicon microstructure and with lateral over growth (LOG) epitaxial process, the microstructures of Ge or InP or InGaAs can form a continuous epitaxial thin film layer that can be doped P type for the anode layer.

[00190] FIGs. 25D and 25E are cross sections showing aspects of a forward biased device such as a vertical cavity surface emitting laser (VCSEL), according to some embodiments. VCSEL 2562 can also be fabricated using similar processing as described *supra* for the PDs, PVs and/or APDs. Starting with a SI PIN structure 2562, Si microstructure hole(s) 2564 are etched through I-Si layer

2566 to the N-Si layer 2568. According to some embodiments, the etching of hole 2564 can extend into the N-Si layer 2568. An SAG process is followed with or without silicon oxide on the Si microstructure sidewalls (oxide 2570 is shown). First, a GaAs/AlGaAs distributed Bragg reflector 2572 (DBR) all N type is grown, follow by N-GaAs 2574, The active layer 2576 is undoped InGaAs/GaAs multiple quantum well (MQW) of 1-5 wells, followed by P-GaAs 2578 to the surface and using ELOG which can form a continuous film at the surface of the I-Si 2566. Dielectric DBR 2582 on the P-GaAs 2580 completes the optical cavity. P ohmic alloy with anneal and bond metal 2584 on P-GaAs 2580 completes the anode contact and N ohmic alloy with anneal and bond metal 2582 on N-Si 2568 completes the cathode contact. Forward bias of 1 to 20 volts to the anode and cathode will result 1200-1300 nm light to be emitted from the VCSEL 2560.

[00191] The design and growth of VCSELs at 1200-1300 nm and other wavelengths are known. See, e.g. "High-performance 1200-nm InGaAs and 1300-nm InGaAsN quantum-well lasers by metalorganic chemical vapor deposition", Tansu et el; Selected Topics in Quantum Electronics, IEEE Journal of (Volume: 9, Issue: 5), 2003.

[00192] According to some embodiments, longer wavelength are selected when embedding InGaAs, InGaAsN and other III-V material, because at wavelengths greater than 1000 nm silicon is mostly transparent and does not introduce excess additional optical losses. Accordingly, Si is a good heat sink for the VCSEL 2560. According to some embodiments, the GaAs/AlGaAs DBR 2572 is replaced with a silicon/air or a dielectric DBR on the bottom by thinning the Si wafer and etching to the BOX layer, removing the BOX layer and depositing a dielectric DBR. Design of DBR, dielectric and semiconductors are well known. The silicon/air DBR will require further processing, using sacrificial layers such as Ge that can later be selectively etched away via etch trenches.

[00193] According to some embodiments, an LED is fabricated by applying minor variations, including removing the DBRs and adding multiple Si microstructures. The LED can use MQW or just a simple heterojunction of P-GaAs/I-InGaAs/N-GaAs for example. Other semiconductors can also be used such as InGaAsN, InGaAsP, GaAsN, to name a few. The substrate can be another material such as sapphire, SOI, insulator on Si (IOS), ceramic, glass, quartz, GaN,

crystalline or non-crystalline. Addtionally, other material for blue/UV LEDs such as GaN, AlGaN, GaInN, AlN, can be grown using epitaxial reactors and methods of fabrication described above.

[00194] According to some embodiments, voids are formed, that are buried or embedded in Si or Ge on Si or Ge. As used herein "buried" refers to cases when the void is beneath the surface, and "embedded" refers to cases when the void can intersect or be slightly above the surface. As described *supra*, during regrowth of Ge on a microstructured Si with pillar and/or hole arrays, voids can develop due to the fact that growth rate during epitaxial growth often depends on the crystal orientation of the surface. Since etching microstructured pillars and/or holes in Si can expose different surface orientation of the side walls, asymmetric growth rate of Ge on these different Si surface orientation can result in void formation. According to some embodiments, the void formation is exploited to generate a buried and/or embedded microstructured void arrays that can behave as HCG and or light trapping structures that concentrate the optical field and/or resonance through interference of the optical field (amplitude and phase), scattering, near field, linear and non-linear optical effects to enhance the bulk film absorption coefficient by one to several orders of magnitude. In addition, the voids can be used to reduce the effective refractive index of a material (e.g. Si with voids) since the optical field sees an average or effective refractive index. At dimensions on the order of a wavelength or less, the refractive index of voids and Si, for example, can be approximated with an effective refractive index which is the average of the volume occupied by Si and the volume occupied by the void. For example, if Si occupies 1/2 the volume and voids occupy 1/2 volume, the Si index is 3.49 and the void is 1.0 (for air), then the average effective index is approximately 2.25.

[00195] The voids also reduce capacitance of the device if the voids are generated in the "I" region, as discussed *supra*; where the space between microstructured pillars or the microstructured holes can reduce the capacitance of the P-I-N PD diode or the P-I-P-I-N APD diode. The voids according to some embodiments are either buried (buried holes) or embedded (space between pillars) and the total capacitance is approximately the capacitance of the total area occupied by the voids plus the capacitance of the total area occupied by the semiconductor. In the case where the voids do not occupy the full thickness of the

"I" layer (i.e. only occupy part of the thickness), then the effective dielectric constant can be estimated by taking into account a volume that contains both the void and the semiconductor extending through the thickness of the "I" layer, the volume of the void and the volume of the semiconductor in a given volume; for example if the voids occupy 1/2 of a given volume of the thickness of the "I" layer and the semiconductor material occupies 1/2, and if the semiconductor material is Si with dielectric constant of 11.9, then the average effective dielectric constant is approximately 6.5, where the void is assumed to be air with dielectric constant of 1 for that given volume. The total area occupied by this effective dielectric constant, consisting of both voids and semiconductor material, is used in the capacitance calculation plus the area occupied only by semiconductor in the "I" region to give the total capacitance of the P-I-N or P-I-P-I-N diode. Reduction of capacitance leads to a reduction in RC time constant for the diode which improves the bandwidth of the PD and APD.

[00196] Although buried voids in semiconductor material are known, such voids are conventionally regarded as detrimental and as such are to be avoided. According to some embodiments, such voids are intentionally created and form useful features in the semiconductor material.

[00197] FIG. 26 is a cross section showing starting epitaxial layers in which mictrostructured voids are fabricated, according to some embodiments. To generate voids in PD, PV and APD structures start with a structure 2600. The starting material can be a Si PD or APD structure with or without the Si P^+ anode layer. Details of the layers are not shown for simplicity.

[00198] FIG. 27 is a cross section showing microstructured holes/pillars etched into the I-Si layer, according to some embodiments. The microsctured holes 2722 (or space around pillars) are etched into the Si "I" layer and can extend pass the "I" layer or can be partially into the "I" layer. Wet and/or dry etching can be used or a combination of wet chemical and dry etching (RIE, DRIE for example) where the wet etching can be used to remove damage due to dry etching or wet etching in combination with dry etching and oxidation to form a certain shape or surface smoothness. As shown in FIG. 27, the etch can be isotropic or anisotropic, the sidewall can have negative or positive slope (slope defined with respect to the plane of the substrate). For anisotropic etching both negative and positive slope

can exist at the same time for an etched feature such as a pillar or hole. Anisotropic epitaxial growth can result in void formation, with the shape of the void being determined by many factors including: side wall slope, crystal orientations of the side wall, growth conditions, pressure, temperature, flow rate, growth technique (CVD, MBE, ALD or a combination of growth methods), surface preparation, and surface oxidation. According to some embodiments, surface oxide, partial oxide or other dielectric 2726 can be intentionally deposited on the side walls, which can also influence the regrowth of Si or Ge (or any other semiconductor such as InP, GaAs, InGaAs, GaN, InGaN, to name a few) and can be used to form voids.

[00199] FIG. 28 is a cross section showing microstructured voids buried or embedded in Si with a Si capping P^+ anode layer 2826, according to some embodiments. The buried voids 2800 can be uniformly spaced, or with chirped spacing, or any complex patterns with a combination of periodic and aperiodic spacing or it can be random or pseudo-random. The buried voids 2800 can have a length ranging approximately from 0.1 to 10 micrometers and lateral dimension ranging from 10-5000 nm. The voids can also be overlapping one another. Although FIG. 28 shows buried voids in Si, according to some embodiments buried voids can be formed in Ge. For example, in a Ge epitaxial layer on Si, or any other semiconductors, such as InP, GaAs, InGaAs, GaN, InGaN, InGaAsP, and other semiconductors in the III-V material family. The voids can be non-uniform is size and shape within the void and adjacent voids. The voids may also have non-uniform spacing and/or orientation. However, with proper process control uniformity in size and shape, patterning, random and pseudo-random placements of the voids can be attained. For simplicity the voids are shown to be uniform.

[00200] FIG. 29 is a cross section showing Bragg reflectors formed on the P-Si surface to provide a highly reflective mirror, according to some embodiments. With a more planar surface, high reflectivity Bragg reflectors 2900 may be deposited or grown using dielectrics or semiconductors on the P silicon layer 2826 surface. The ohmic contact and the bond metallization 2902 can be on the peripheral in a ring configuration as shown in FIG. 29. Optical signal illuminating from the bottom will have a double/multiple pass through the absorbing I region thereby improving QE and the bandwidth of the PD/APD. In PV where bandwidth is not an issue, then the QE will be improved. According to some embodiments,

Bragg reflectors 2900 can be configured for wavelength selectivity so as to reflect the optical signal back into the absorbing I region.

[00201] According to some embodiments, voids are not only in the I region but are also formed in the P and/or N region of a PIN PD or PV, in the P charge region, in the I multiplication region and/or the P anode and N cathode region of an APD. According to some embodiments, voids can also be formed in the substrate. The density, shape and material (voids can be filled with different material from vacuum, gas, helium to dielectrics with or without doping with rare earth elements for optical gain for example, carbon/graphene/diamond,copper, ceramics for thermal conductivity for example) of the voids in each layer can be different or the same, or different/same within the same layer.

[00202] According to some embodiments, voids are also used to make the material more mechanically flexible and bend and or conform to different surface contours. For example, in PV applications where large sheets of the device are fabricated, the sheets can conform to contours in for example the roof, or the sheets of semiconductor PV can be rolled for compactness in storage prior to deployment. According to some embodiments, voids sized between 0.01 microns and 1000 microns are introduced into semiconductor and/or glass material for use with photo voltaics for purposes of increasing flexibility and/or resistance to physical damage and/or damage propagation.

[00203] High-density voids in semiconductors are also resistant to crack propagation since the crack will terminate at a boundary, in this case the boundary of the void. This is advantageous for large devices such as solar cells where if an object such as hail or stone strikes the solar cell, only the point of contact will be damaged and perhaps a small adjacent area (5-50% of the diameter of impact for example) where the damages are localized to area of impact and cracks will not propagate across the entire cell. A device may survive such small damage events with minimal degraded performance without taking the entire solar panel down.

[00204] According to some embodiments, the voids are also formed in other materials also such as glass, ceramics, polymers, metal, plastics, to name a few, to avoid crack propagation in case of foreign object impacts since cracks will terminate at a boundary, in this case the boundary at the void.

[00205] FIG. 30 shows an example of a PIN PD/PV structure 3000 with microstructured voids to enhance absorption, reduce bulk refractive index, reduce capacitance and increase mechanical flexibility of large sheets of PV on semiconductor material, according to some embodiments. The Si substrate is removed leaving only the BOX/SOI layers together with the PIN epitaxially grown layers. Ohmic contacts, bond metallizations, antireflection coatings, passivations, are not shown for simplicity. In addition to PV, the techniques are also applicable to PD, APD, light emitters such as light emitting diodes and diode lasers, and to electronic integrated circuits such as CMOS and ASIC (application specific integrated circuits) where voids can not only make the material more flexible and lighter but also as mentioned earlier more resistant to cracking. The voids, according to some embodiments can be filled with a gel that can repair impact damage and seal exposed cracked edges to prevent further deterioration due to moisture for example to the semiconducting surfaces. The gel can be spin on glass for example. According to some embodiments, the voids can be filled with material to enhance thermal conductivity for example, reduction of optical or microwave losses by removing the silicon and replacing with material that is not lossy such as Ar, He, Xe, N_2, Ne gas, or vacuum for example. The voids can have different sizes and shapes and densities and can be random, pseudo random, aperiodic, periodic, chirped, single or multiple patterns. The voids can also be in a single layer or in multiple layers of the device. Fig. 30, for example, shows the voids in P-Si layer 3002, I-Si layer 3004, and N-Si layers 3006 and 3008. According to some embodiments the index of refraction near the uppermost surface can be altered to more effectively index "match" with surrounding air so as to reduce reflections of incident light. For example, in PV applications near surface voids can be used to index match such that less incident sunlight is reflected from the PV surface. According to some embodiments, the index of refraction at lower surfaces can be altered so as to increase internal reflections that may, for examples, increase the number of passes light makes through an absorbing region.

[00206] According to some embodiments, random voids can also be generated by dry etching/electrochemical etching the surface of the semiconductor without any mask. Generating semiconductor nanowires followed by epitaxial regowth on these random nanowires will result in buried voids. As discussed in Frajtag et al,

Growing thin films that contain embedded voids, 23 June 2011, SPIE Newsroom; DOI: 10.1117/2.1201105.003750, this method can be used in GaN light emitting diodes to minimize defect formation due to lattice mismatch of the GaN epitaxial layer with the substrate which can be sapphire, Si, SOI, IOS to name a few. The random formation of semiconductor nanowires by dry etching of the surface of the semiconductor (which can be Si, Ge, III-V material family such as InP, GaAs, InGaAs, InGaAsP, GaN, InGaN, InSb, to name a few) without any mask and subsequently regrowing on the nanowires epitaxially using CVD for example, to form random buried voids can also be used to reduce the effective refractive index of the semiconductor and reduce the effective capacitance of the P-I-N, P-I-P-I-N diodes if the voids are formed in the "I" absorption layer and/or P, N layers, and/or charge, multiplication layers of the PD, APD, in any combination to optimize the performance of the device in bandwidth, QE, and energy consumption.

[00207] Fig. 31 is a cross section showing regrown I-Ge with a buried/embedded voids, according to some embodiments. The regrowth of Ge 3104 epitaxially on Si microstructured pillars and/or holes results in voids 3102 in the Ge layer that can be intrinsic or non-intentionally doped or low doped using the method shown in FIGs. 27-28, *supra*. In addition, selective masking with dielectric such as SiOx, SiNx for example can be used to generate nanowires only in the selected areas such as the Ge regrowth, for example, and with additional regrowth of Ge, random voids can be buried only in the selected Ge areas. The random voids can be combined with patterned voids to optimize a device performance in terms of bandwidths, quantum efficiencies and power consumption. The microstructures shown in FIG. 31 combine the Ge microstructure and void microstructure to enhance to bulk absorption coefficient and reduce the effective capacitance of the diode.

[00208] Fig. 32 is a cross section showing a device having buried microstructured voids in I-Si with regrown I-Ge and capped by an epitaxial layer, according to some embodiments. As can be seen in FIG. 32, the buried/embedded microstructure voids 3202 can be in I-Si layer 3200 while the Ge microstructure 3104 is also buried/embedded in Si layer 3200 using a few additional processing steps. First the voids 3202 are buried/embedded as in FIG. 28 with or without the P-Si anode layer 3226. Microstructures are then again

etched into the I-Si layer 3200 with the voids and then Ge 3104 is regrown resulting in a microstructure with voids 3202 in the Si layer 3200 and a Ge microstructure 3104 to enhance the bulk absorption coefficient and reduce the capacitance of the diode. Not shown is that the microstructured voids can also be buried/embedded entirely in Ge for Ge on Si layers, such that in Fig. 28, if the I-Si layer 3200 is replaced with I-Ge followed by a P^+ Ge capping anode layer 3226.

[00209] The buried/embedded microstructure voids is an inverse HCG structure with absorption, or a lossy HCG structure, and can have resonance, constructive and destructive optical interference effects of both phase and amplitude that can result in the enhancement of the bulk absorption coefficient. The period of the microstructure pillar, hole, void, buried/embedded Ge arrays can fall in the near-wavelength regime of the HCG effect or it can fall in the subwavelength regime where the grating period is much less than a wavelength and the diffraction regime where the period is greater than a wavelength. The HCG characteristics of the microstructure array and the input optical signal can be coupled to in-plane optical modes. The microstructured arrays can also behave as a lens to mode match the incoming optical signal. Good coupling efficiency also improves the overall QE of the PD/APD. According to some embodiments, a lossy HCG is provided where the absorbing region is a part of or included in the HCG structure (other effects such as scattering, near field, plasmonic, resonance, linear and non-linear optical effects to name a few, can also play a significant role in absorption enhancements), and where Si can be the HCG for photon energies that are below the Si bandgap and the Ge microstructures are buried or embedded within the Si that is absorbing to the photons with wavelength ranging from 950-1800 nm (where Si has relatively low optical losses).

[00210] According to some embodiments, the microstructures of holes, pillars, and voids can be arranged in any pattern or no pattern in the active area, including any parts of the P-I-N structure of a PD or P-I-P-I-N structure of an APD; the active area includes the absorbing "I" region and the P and N regions. According to some embodiments, to simplify manufacturing and to improve yield, the microstructures can extend outside the active areas of a PD/APD if it does not interfere with the PD/APD operations and performance. FIG. 33 is a top view showing distribution of microstructured pillars, holes and/or buried voids in an PD/APD, according to some

embodiments. The microstructure array 3300 consists of pillars, holes, and/or voids, and buried/embedded Ge in Si or Si in Ge or any combination of multiple semiconductors, can be distributed over the entire active area 3302 of the photodiode or avalanche photodiode or just partially for example in the center where the optical intensity is the highest. The active area can be defined as any area that contributes to the generation of electrical signal upon illumination with optical signal, or in the case of a PV, the generation of electricity upon illumination with photons. In FIG. 33, the active area 3302 is commonly the area within the metal ohmic contact/bond metal ring 3304. The distribution of the array 3300 can be non uniform, non periodic, non uniform is size of the microstructure, or in shape.

[00211] FIG. 34 is a top view showing distribution of microstructured pillars, holes and/or buried voids in an PD/APD, according to some other embodiments. In FIG. 34, the QE is optimized at the center of the active area where the optical intensity is the highest and away from the center, more semiconductor material is removed in the microstructure pattern to reduce the capacitance of the active area in order to decrease the RC (resistance, capacitance) time constant to achieve higher bandwidth for the PD/APD and or to increase the active area to allow passive alignment of the optical signal to the PD/APD thereby reducing the cost of packaging and assembly. Microstructured pillars/holes/buried voids 3400 near the center of the PD/APD optimize QE while the microstructured pillars/holes/buried voids 3410 at the periphery of active area 3402 minimize capacitance while still maintaining good QE.

[00212] Buried voids in the N (or P if P and N are switched) part of the P-I-N or P-I-P-I-N diode structure can reduce the effective refractive index of the semiconductor in the N layer. This is useful in increasing the refractive index contrast for HCG structures (to include other possible optical effects that may be significant in absorption enhancements such as scattering, plasmonic, near field, linear and non-linear optical effects to name a few), for example in Si the refractive index is approximately 3.5 (for wavelengths 950-1800 nm) and if half of the volume of the material is air, then the effective refractive index (1/2 air and 1/2 Si) would be approximately 1.8 for the air-Si composite material. Any semiconductor microstructures of pillars or holes fabricated on top of this composite air-Si material will have a index contrast of, for example Si pillars on the composite air-Si layer,

approximately 2. The high index contrast would enhance the performance of the HCG. According to some embodiments, this is used to enhance the lossy HCG performance (where loss can be as high or higher than - 1 dB/cm) and enhance the absorption coefficient with its resonance, light concentration and in-plane light coupling effects to name a few. There is an advantage in having the voids in the N and or N^+ layers since it will have a minimal effect on the electrical properties and characteristics of the diode since once electrons are swept into the N and or N^+ layer, they are majority carriers.

[00213] The microstructured voids in the N and or N^+ layer can be patterned, non-patterned or random or pseudo-random, and can be defined using lithography, masking and etching or just etching followed by a regrowth of Si, or Ge or any other material. The voids can range in length approximately from 0.01 to 10 micrometers and lateral dimensions can range approximately from 10-5000 nm with spacing between adjacent voids ranging approximately from overlapping to 5000 nm.

[00214] Fig. 35 shows the basic epitaxial structure 3500 for a conventional Si PV/PD diode on N Si substrate. FIG. 36 shows the structure of FIG. 35 with microstructured voids incorporated into the N-Si layer, according to some embodiments. The doping and thickness of the layers are dependent of the applications. For high bandwidth PD applications the "I" Si thickness ranges from 0.1 to 3 micrometers whereas for PV applications the "I" Si thickness ranges from 1 to 20 micrometers with doping range of intrinsic or not intentionally doped, background doping of $< 5. 10^{16}$ cm^{-3}. Device size to define the area of the capacitance for high bandwidth PD (for circular apertures) ranges from 5 to 100 micrometer diameter whereas for PV, the lateral dimension can range from 0.1 to > 50 cm (centimeters) limited only by the size of the wafer or substrate. The doping ranges and layer thicknesses for non "I" layers are similar for PV, PD and APD; P or P^+ layer thickness ranges 0.1 to 3 micrometers P doping $> 5. 10^{18}$ cm^{-3}, N or N^+ layer(s) thickness ranges of 0.1 to 10 micrometers N doping $> 1. 10^{17}$ cm^{-3}. The Si substrate can be N doped, low N doped or undoped.

[00215] After growing the N/N^+ layer(s) on the Si substrate, microstructures of pillars and or holes and or nanowires are etched into the N/N^+ layer(s) 3604 and followed by a N/N^+ layer(s) regrowth resulting in buried voids 3622 as shown in Fig.

36. The regrowth surface may or may not need further planarization such as using chemical mechanical polishing (CMP). Some applications may have more optimal performance with a non-planar surface, for example PV that can couple sun light in multiple angles with minimal reflections (a rough surface reflect less light).

Subsequent "I" Si layer 3606 and P/P^+ layer 3608 are grown on the N/N^+ layer(s) 3604 with the buried voids 3622. In addition to reducing the effective refractive index, at wavelengths where Si has low loss (approximately ~1 dB/cm or less), 950-1800 nm, the buried voids 3622 can be patterned into a reversed HCG and behave as a very reflective (close to 100% reflectivity) broad spectrum mirror for any photons illuminating from the top (P side) and not absorbed in the "I" microstructured pillar/hole region on the first pass, the photons can be reflected back toward the absorbing "I" region. In addition, with the voids, the substrate may be more flexible and lightweight such that it can be more adaptable to contoured surfaces and/or for use where weight is an issue such as a solar panel, or for mobility.

[00216] FIG. 37 is a cross section showing etched Si microstructured pillars/holes with regrown Ge covering the Si, according to some embodiments. The starting structure is the same as layers 3500 in FIG. 35. The Si microstructure pillar and/or hole arrays are etched with a depth ranging from 0.1 to 10 micrometers and subsequently regrown with a I-Ge layer 3702 of thickness 0.01 to 4 micrometers including according to some embodiments a 1-10 nm low temperature buffer Ge layer to account for lattice mismatch between the Si and Ge. Note that the Ge buffer may not be included for pillar hole lateral dimensions of approximately 1000 nm or less since the lattice mismatch strain at that small area may not be significant to cause extensive defects to form. The lateral dimensions of the microstructured pillars 3704 and holes 3706 range from 10 to 5000 nm and spacing of adjacent elements from overlapping to 5000 nm. The P/P^+ Si layer 3708 is left on in FIG. 37 as it may be useful in making good P ohmic contact with the ohmic metals of Ti, W, Al silicide that are 1-50 nm thick to be semitransparent or transparent transition metal silicide.

[00217] FIG. 38 is a cross section showing microstructured Si pillars/holes with Ge regrowth on an N-Si layer having embedded microstructured voids, according to some embodiments. The structure shown in FIG. 38 is similar in starting

material as shown in FIG. 36. The buried voids 3822 in the N/N^+ layer 3804 act to reduce the effective refractive index of layer 3804. The voids spacing and lateral dimensions can be subwavelength (< λ) or even deep subwavelength (<< λ) to minimize optical scattering loss such as Rayleigh scattering which is proportional to λ^{-4} where λ is the wavelength. The wavelength of interest range from 300 to 1800 nm.

[00218] FIG. 39 is a cross section showing partial coverage I-Ge on microstructured Si pillars/holes, according to some embodiments. In the variation of the microstructure shown in FIG. 39, instead of regrowing I-Ge over the entire Si microstructured pillars and holes, it is only grown on part of the Si microstructures. Part of the Si microstructure is without I-Ge and the other part has regrown I-Ge. The partial regrowth of Ge can be accomplished by partially covering the Si microstructure with a dielectric such as SiOx or SiNx by directional deposition such as electron beam evaporation deposition, or directional laser ablation deposition or other directional methods such as ion milling to remove native oxide of Si selectively or ALD thin layer of oxides/nitrides and removing selectively and directionally with ion beam milling. Once the Si microstructure is partially coated with an oxide or nitride (or other dielectric such as CaFx, TaOx, TiOx, to name a few) Ge epitaxial regrowth will predominantly occur where there is lattice information such as a Si surface. The I-Ge regrowth 3902 thickness can range from 0.1 to 4 micrometers or more. The Si microstructure of pillars 3904 or holes 3906 can have a depth of 0.1 to 10 micrometers and a lateral dimension of 10 to 5000 nm and spacing between adjacent microstructures of overlapping to 5000 nm. Both Si and Ge microstructures are exposed to photons with wavelengths ranging from 300-1800 nm from photons impinging from the anode surface and impinging on the sidewalls of the microstructure directly, scattered, near field, resonance, HCG effect, linear and non-linear optical effects, and with enhanced absorption coefficient. Both Si and Ge will generate photocurrent due to the incident photons. The Si current generator and Ge current generator are in parallel and the total photocurrent generated by this PD/PV is the sum of the Si and Ge photocurrent generators. The buried voids 3922 reduce the refractive index of the N/N^+ layer 3914 and improve the index contrast of the microstructure and the substrate thus improving the performance of the lossy HCG for enhancing the absorption

coefficient. The voids 3922 in the Si 3914 can also behave as a good reflector to reflect photons back toward the "I" absorbing layer for a double pass (for photons illuminating from the top side). BOX or SOI 3912 can also be used in addition with the buried voids or without the buried voids, as the refractive index of SiO_2 is approximately 1.54, roughly half that of silicon at infrared and near infrared wavelengths.

[00219] FIG. 40 is a cross section showing the basic components for a microstructured Si-Ge pillar hole array PD/PV and/or APD, according to some embodiments. Note that the APD multiplication layers are not shown for simplicity. Only the very basic parts of the device is shown. After processing steps shown in FIG. 39 are completed, surface passivation is carried out using thermal oxide or ALD or PECVD or CVD deposition of oxide or nitride to passivate or SiGe as a passivation layer on Ge. A filler 4002 is spun on or deposited such as spin-on-glass, or SiOx, SiNx by PECVD or CVD. Using RIE to etch back to expose either the Ge or P/P^+ Si (during i-Ge epitaxial growth, the P dopant in the P/P^+ Si may diffuse into the Ge layer to also result in a P/P^+ Ge layer). Ge and or Si P- ohmic material may be Al, W, AuGe, Au, Au/Ti and Al, TiN, Pt, transition metal-silicide respectively; ohmic contacts to P and N semiconductors are well known in the literature and art and these are only a few examples of possible ohmic contacts. A transparent conducting oxide (TCO) 4004 such as indium tin oxide (ITO) may be used to further reduce the series resistance of the anode. For microstructured holes, since the P/P^+ layers are contiguous, TCO 4004 may not be used and only a perimeter (ring for circular apertured PD/APD/PV) border ohmic contact and metallization 4006 may be used instead to reduce series resistance of the ohmic contact, such as Al, Au/Ti. Cu, to name a few. Anti-reflection layers are not shown for simplicity. N ohmic material can be used on the substrate or on the N/N^+ layer together with metallization. Al, Pt, transition metal silicide, followed with Al or Au deposition (e-beam, sputter, thermal evaporation) on the ohmic contacts reduce series resistance. Ohmic contacts normally use an annealing process that is well known in the art. Bond and/or connecting metallization 4006 is deposited (using standard processing methods) to complete the PD/APD/PV device. Sunlight/optical signal is illuminated from the top (anode) of the device normal to the surface or at any angle off normal and may be rotated to optimize the QE. At wavelengths where

Si is low loss (950-1800 nm or more) the buried voids can both reduce the effective refractive index of Si and act as a reflector to reflect photons that are not absorbed back toward the absorbing region. The surface of the N/N^+ layer 3914 can be non-planar to help diffuse the reflected photons to optimize its absorption in the microstructured Si and Ge array. A contact pad 4008 can be provided, for example, on the side of layer 3914 as shown. Although many of the embodiments show the microstructures of Si and Ge, Si, Ge are normal to the surface (vertically aligned) and straight, according to some other embodiments if the N/N^+ surface is non-planar, subsequent layers may also be non-planar. Etching (wet chemical or dry RIE, DRIE) may result in microstructures that are off normal and not straight (with bends) which may further improve the absorption of photons. Due to the non-planar topology of the surface, the microstructures may have various orientations depending on the orientation of the crystal within the same device. The different orientations of the microstructures are advantageous to capturing photons that may be illuminating the surface of the device at different angles, for example for PV as the sun changes position in the sky and for PD/APD for applications where multiple optical signal may illuminate the PD/APD from different angles/directions.

[00220] Microstructured Si pillar and/or hole arrays/pattern/random PD shown in FIG. 5, *supra*, can also have buried voids in the N/N^+ layers as shown in FIG. 10 to both reduce the refractive index of Si so that the microstuctures of Si pillars/holes are more optimized as lossy HCG by increasing the refractive index contrast and also as a HCG reflector in Si for wavelengths where Si has low loss, 950-1100 nm for this application as a wide bandwidth (> 5 Gb/s) PD or as a PV.

[00221] The Si substrate in all the embodiments described herein can be either Si with doping, not intentionally doped, low doping, or buried oxide (BOX) or silicon on insulator (SOI) where the silicon layers again can be doped, heavily doped, lightly doped or not intentionally doped. The BOX and SOI layers allow the removal of the all or almost all of the Si substrate to reduce optical losses, increase mechanical flexibility and also the refractive index of SiO_2 in BOX and SOI have refractive index of approximately 1.54 in the infrared and near infrared wavelengths which is roughly half of silicon refractive index. The low index of SiO_2 also improves the performance of HCG, or the silicon dioxide layer can be removed for bottom illuminated PD/APD/PV.

[00222] FIGs. 41A-41B are cross sections showing aspects of a microstructured pillar/hole array device above a N-Si layer having buried microstructured voids, according to some embodiments. The bulk layers 4100 shown in FIG. 41A include I-Si layer 4112 and N-Si layer 4110. Microstructured voids 4102 are formed in the N-Si layer 4110 using techniques such as described herein *supra*. The structures in FIGs. 41A and 41B are a version of the PDs/PVs shown in FIGs. 25A-B but with buried voids 4102 in the N/N$^+$ layer 4110 to improve the refractive index contrast for lossy HCG (microstructures of Si and Ge) and to provide a reflector low loss HCG for photons. Pillars 4124 and/or holes 4122 arrays are formed in I-Si layer 4112. I-Ge is regrown in the etch region 4122 resulting in a buried/embedded Ge "I" layer with microstructure voids 4102 in the N Si layer 4110 to reduce the effective refractive index of Si and/or to reflect photons entering from the anode surface at wavelength where Si is low loss (950-1800 nm). Cap layer 4126 can be P-GE or P-Si regrowth. In the case of bottom illumination, an anti-reflection coating 4130 may be provided.

[00223] FIGs. 42A-42D are cross sections showing aspects of an APD with microstructured pillar/hole arrays above an N-Si layer having buried microstructured voids, according to some embodiments. The APDs shown in FIGs. 42A-42D are versions of the APD shown in FIGs. 24A and 24B, *supra*, except that buried voids 4202 are included in the N/N$^+$ layer 4210 to improve the refractive index contrast for lossy HCG (microstructures of Si and Ge) and to provide a reflector low loss HCG for photons. According to some embodiments, BOX/SOI Si wafers can also be used with or without buried voids to improve refractive index contrast for optimal HCG lossy operation. Only the basic structures are shown for simplicity. Electrical isolation, passivations, ohmic metallization, anneal, anti reflections, bond/interconnect metallization, guard rings, to name a few are not shown. FIG. 42A shows the bulk layers 4200, which include N-Si layer 4206, I-Si layers 4208 and 4212 and P-Si layer 4210. Microstructured voids 4202 are formed in the N-Si layer 4206 using techniques such as described herein *supra*. As in the case of FIG. 41B, I-Ge is regrowth in the etched area 4222. The voids 4202 are to reduce the effective index of the N-Si since the optical field will be an average effective refractive index composing of air and Si. If the voids 4202 are patterned for HCG effect, photons can be reflected that are not absorbed in the first pass

through the "I" absorbing region 4212 for photons illuminating the APD 4220 from the top or anode surface. The APD can also be illuminated from the bottom or cathode side.

[00224] FIGs. 42C and 42D show another variation of an APD 4230 in which voids 4204 are formed in the I-Si multiplication layer 4208 as well as in N^+ layer 4206 to reduce the effective refractive index and capacitance of those layers. Note that the elongated nature of the microstructured voids will have a minimal effect on charged carrier transport in the semiconductor materials. According to some embodiments, voids of various shapes and densities can be formed in the P anode, N cathode, P charge, and/or I multiplication layers of the APD in addition to the absorbing I layer. The addition of voids in the I multiplication layer 4208 and the I absorption layer 4212 can reduce the effective capacitance resulting in a short RC time constant for the device. The voids 4204 in the multiplication I Si layer 4208 also reduce the effective refractive index, which is helpful in enhancing the absorption coefficient in a HCG absorbing mode.

[00225] Epitaxial growth/regrowth/overgrowth/selective area growth/epitaxial lateral over growth of Si, Ge, SiGe, III-V such as InP, GaAs, GaN, InGaN, InGaAs, InGaAsP, InSb, heteroepitaxy, homoepitaxy, heterogeneous epitaxy to name a few, using chemical vapor deposition (CVD), metallic organic chemical vapor deposition (MOCVD), atomic layer deposition (ALD), molecular beam epitaxy (MBE), gas source molecular beam epitaxy (GSMBE) plasma enhanced chemical vapor deposition (PECVD), laser ablation deposition (LAD) to name a few, are well known in the art.

[00226] According to some embodiments, material other than Si and Ge on Si are used. For example, the techniques described herein can be applied to all combinations of Si, Ge, III-V and II-VI material families and substrates.

[00227] FIGs. 43-46 are top views illustrating various dimensions, spacings and shapes for microstructured elements, according to some embodiments. FIG. 43 shows a microstructured pillar and/or hole array 4300 (also applicable to embedded or buried voids) that is uniformly spaced with a fixed diameter ranging from 100-5000 nm and a spacing ranging from 100-10000 nm. The pillars and or holes can be formed in or using: Si, Ge, SiGe, or other materials such as III-V or II-VI material family. Examples includes: GaAs, InP, InGaAs, InGaAsN, InGaAsP,

InAs, GaN, InGaN, ZnTe, CdS, ZnSe, and HgTe. According to some embodiments, the microstructures can also be formed in or using absorbing polymers, glass, and/or ceramics.

[00228] FIG. 44 shows a microstructured pillar and/or hole array 4400 having a fixed diameter but with non-uniform spacing such as aperiodic or a mixture of periodic and aperiodic or random/pseudo random spacing or a mixture of random/pseudo random, periodic and aperiodic. According to some embodiments, the arrays can also be uniformly spaced periodic but with varying diameter. FIG. 45 shows a microstructured pillar and/or hole array 4500 having both variable diameters (ranging from 100 nm to 5000 nm) and variable spacing (ranging from 100 nm to 10000 nm). According to some embodiments, the variations can be random/pseudo random, or a pattern or a mixture of patterns or any combinations thereof. FIG. 46 shows a microstructured pillar and/or hole array 4600 having various shapes such as oval, circular, rectangle, doublets, triplets, and stars. In general, any shape that can be generated using a photolithographic mask, or e-beam direct write or that can be generated with a mold for imprint lithography, can be used. The pillar/hole arrays can also have a combination of different shapes and spacings, as well as variations in the depth of the microstructured holes or lengths of the microstructured pillars/mesas. The variations can be periodic, aperiodic, or random (or a mixture of periodic, aperiodic and random) within a single array.

[00229] According to some embodiments, for some applications an array dimension of Si or Ge or III-V microstructured pillars or holes of length 2 μm approximately (or depth of 2 μm approximately) with diameter of pillar/hole of 390 nm approximately and center to center spacing of 1060 nm approximately has been found to be suitable for enhancement of the absorption coefficient of greater than 50X.

[00230] According to some embodiments, the material can be Si, Ge, SiGe, Ge on Si, III-V, II-VI, III-V on Si, polymer, glass, ceramic and any combination thereof. Examples of III-VI and II-VI are InP, GaAs, AlGaAs, AlAs, AlInAs, InGaAs, InGaAsP, InAs, InGaAsN, InN, GaN, InSb, ZnSe, ZnTe, HgTe, and CdS. Also III-V, II-VI and group IV material such as Ge can be embedded in Si microstructures using SAG, VLS, ELOG growth methods in MOCVD, CVD, MBE, reactors.

[00231] FIGs. 47-48 are cross sections showing microstructured pillar and hole arrays having varying lengths and depths, according to some embodiments. FIG. 47 shows a microstructured pillar array 4700 having different lengths, diameters and spacing. According to some embodiments, the pillar diameters range from 10 nm to 5000 nm and the pillar heights range from 0.1 to 10 microns. FIG. 48 shows a microstructured hole array 4800 having different depths, diameters and spacings. According to some embodiments, the holes have diameters ranging from 10 nm to 5000 nm and depths ranging from 0.1 to 10 microns. The variation in lengths and etched depths can be accomplished by additional lithographic masking steps where regions are masked for longer etch or shorter etch to vary the length of the pillars and the depth of the holes. The lengths and depths can be gradually or sharply varied. A patterned grating effect can be used to further optimize the optical path lengths and increase the enhancement factor for absorption coefficient. Other uses include forming a light trap by using constructive and destructive optical interference, generating a fresnel lens, matching the mode of the optical signal, forming a filter in wavelength selectivity in wavelength division multiplexing for example, or as a wavelength selector for spectroscopy and sensor applications. It should be noted that by varying the dimensions and spacing of the microstructured pillars and holes in an array can also result in constructive and destructive optical interferences that can also increase the enhancement factor of the absorption coefficient, improve light trapping, create fresnel lens, mode matching of radiation patterns of the optical signal.

[00232] FIG. 49 shows shows a microstructured surface having a combination of both pillars and holes, according to some embodiments. Microstructure array 4900 includes pillars and holes co-existing on the same microstructured surface either globally or locally. Both pillars and holes can exist in a single array (such as shown in FIG. 49) for the microstructured photodetector, or holes and pillars can exist on separate arrays for different microstructured photodetectors. In addition, hole(s) can exist in a pillar and pillar(s) can exist within a hole and these also can be global or local. The pillars, holes, hole(s) in pillar and pillar(s) in holes can have any shape, for example a rectangular pillar within a round hole, can have any mixture thereof to optimize enhancement of the absorption coefficient, light trapping, constructive and destructive optical interference, scattering, near field effects,

linear and non-linear optical effects, subwavelengths effects, fresnel lens, wavelength selection, optical mode matching, diffraction, high contrast grating, blazed grating, high Q resonator, highly reflective mirrors using high contrast grating.

[00233] The microstructured pillar and hole (and variations thereof) arrays can be fabricated in Si, Ge, Ge on Si, SiGe on Si, SiGe on Ge. The array structure can be any combination of Si, Ge and SiGe. The array can be entirely Si or Ge or SiGe, or Ge on Si, or Si on Ge, or Ge on Si with SiGe on both. The structure can also include III-V and II-VI material systems together with Si, Ge and SiGe and any combination of Si, Ge, and III-V, II-VI material systems. According to some embodiments, the array structure can also include polymer, glass, oxides, nitrides, sulfides and chlorides of transition metals, ceramics, quartz, SOI, IOS, organic conducting and non conducting polymers, carbon based material such as graphene to name a few.

[00234] The microstructures pillars, holes, voids, and any other shapes such as pyramids, microwires, nanowires, multiple materials, SAG microstructures, can have orientations that are not perpendicular to the surface of the substrate. They can have a single or multiple orientations that can be perpendicular and or off perpendicular to the surface. They can be random or pseudo random, single pattern or multiple pattern orientations at any angle where angle can range from 0 to 90 degrees with respect to the normal to the silicon substrate, and they can be on sidewalls and on all three dimensions. With the microstructures at certain orientations, the photosensor can have a higher sensitivity to certain direction of illumination. Conversely, with multiple orientations and or random or pseudo random orientations the photosensor can be mostly insensitive to direction of illumination.

[00235] Reducing the effective refractive index with buried voids in semiconductor has applications beyond PD/APD and PV devices. It also, for example, has applications in optical waveguides. FIG. 50 is a cross section of an optical ridge waveguide, according to some embodiments. Waveguide 5000 uses the density of voids to alter the effective refractive index of Si. According to some embodiments materials other than Si are used, for example other semiconductors such as Ge, SiGe, any of the III-V semiconductor family, or other material such as

ceramics, glass, polymer. In Si photonic optical waveguide 5000, the ridge 5002 and slab 5004 are made of Si on a BOX (buried oxide) Si substrate 5006. Due to the high refractive index of Si. 3.49 at 1100-1800 nm wavelengths, the dimensional tolerance of the solid Si waveguide is very critical. Known Si photonic components are difficult to manufacture and have low yield and are temperature sensitive. According to some embodiments, voids are buried in the Si layers. By varying the density of the voids, the refractive index of the composite Si-voids can be adjusted. In the schematic diagram of FIG. 50, a ridge waveguide 5000 has voids 5014 on slab 5004, as well as voids 5012 on ridge 5002. The density of voids 5012 in the ridge 5002 is less than the density of voids 5014 in the slab 5004. The refractive index in the ridge 5002 is therefore higher than the refractive index in the slab 5004 resulting in a ridge optical waveguide. The optical mode of the waveguide 5000 is indicated by the dotted oval 5022. The lower refractive index helps in reducing the dimensional tolerance and the optical waveguide can have a larger dimension. Thus, according to some embodiments, the refractive index can be varied by varying the void density making other components such as couplers easier to manufacture. The dimensions of the voids can be subwavelength ranging from 10nm to 1000nm depending on optical wavelengths.

[00236] According to some embodiments, voids are also buried in a silicon wafer (including BOX/SOI silicon wafers) to adjust the effective refractive index of the Si wafer. The Si wafer with buried voids can then be the starting platform for silicon photonic circuits. It can also be the platform for large area PV cells that allow mechanical flexibility but still retain the high quality of silicon and its electrical characteristics. This can also be the platform for flexible displays and other electronics that require mechanical flexibility and or light weight. According to some embodiments, burying or embedding voids is not limited to just Si, but can include Ge, GeSi, amorphous semiconductors, III-V, II-VI material families, polymers, glass, quartz, metal, alloys, ceramics and any other material that requires flexibility. In some embodiments, the voids can be filled with gas, liquid or solid for specific applications. Gel such as spin on glass that does not require anneal for example can be used for impact/crack situations where the integrity of the device is compromised such as a crack due to impact, to seal surfaces such as semiconductors or any surfaces sensitive to environment such as moisture, water,

oxygen to name a few to prevent further deterioration. Voids are also excellent in preventing crack propagation.

[00237] FIG. 51 is a cross section of a buried optical waveguide in silicon using voids, according to some embodiments. A composite waveguide 5100 is formed in Si substrate 5106 using Si-voids to selectively alter the effective refractive index in certain locations. The effective refractive index of Si can be adjusted precisely by adjusting the total volume of the voids in a given volume of Si. In the example shown in FIG. 51, the higher density voids 5114 surround a central region of lower density voids 5112. The optical mode of the waveguide 5100 is indicated by the dotted oval 5122.

[00238] According to some embodiments, the dimension and spacing of the voids are optimized to reduce scattering losses and to provide ease of manufacturing. Also, the void dimensions and spacing can be adjusted for certain applications. For example, in HCG the dimensions and spacings are selected to satisfy the near field regime where the dimensions and spacing lie approximately between the wavelength in the high refractive index material and the wavelength in the low refractive index material. In most cases, in the applications to reduce the effective refractive index, the void and the surrounding material dimensions and spacing are in the subwavelength regime where the microstructures containing the voids are less or much less than the wavelength in either the high or low index material. For coupling applications, the diffraction regime may be the microstructure (voids and material) dimensions and spacing. It can also be a mixture of two or more regimes to optimize a device performance.

[00239] Array patterns can include microstructure ensembles whose distribution of individual microstructures can be periodic, aperiodic, chirped, random, pseudo-random, uniform, or non-uniform in all three dimensions, orientations and spacings, (including overlapping). According to some embodiments, the patterns can include microstructures within microstructures. The terms "array" and "pattern" are used herein interchangeably.

[00240] The PD/APD are biased between the anode and cathode, to extract a broadband modulation signal greater than a gigabit per second (Gb/s) at a typical transmission line impedance is 25-50 ohms. According to some embodiments, the external bias is provided with a bias-tee connected to the transmission line to block

the RF signal from reaching the DC power supply and to block the DC from biasing the transmission line away from the PD/APD. The bias-tee basically consists of an inductor and capacitor, the inductor to block the RF and the capacitor to block the DC away from the PD/APD. External bias of -2 to -30 volts is applied depending on the application, PD or APD and performance desired.

[00241] In PV mode, no external bias is applied and the PV is basically a current generator. All the electrical connections are for DC current from the PV which then connects to a converter that converts the DC current/voltage to AC current/voltage.

[00242] PV devices are in DC mode whereas PD/APD for data and tele communication are all RF with modulation bandwidth ranging from 1 to 100 Gb/s. Transit time of carriers and capacitance are critical in PD and APD but not so much for PV.

[00243] The terms "modulation bandwidth" and "bandwidth" are interchangeable as used herein. Both terms refer to the modulation (e.g. of a laser or LED) where an RF signal is impressed on the light. When this modulated light (also referred to as "optical signal") illuminates the PD/APD, the RF modulated signal is extracted and converted from light to electrical signal. For example, a bandwidth or modulation bandwidth of a PD/APD of 20 Gb/s means that an RF signal impressed on the laser light beam at a data rate at 20 Gb/s can be converted by the PD/APD from optical to electrical with good signal integrity or signal replication. The laser/LED is the transmitter and the PD/APD is the receiver where the electrical signal can be further processed by an amplifier such as a transimpedance amplifier and the signal sent for further analysis and processing in application specific integrated circuits (ASIC) computers (CPU central processing unit), routers, memories, to name a few.

[00244] According to some embodiments the applications for the microstructured pillars and or holes in Si and Ge and Si regrowth with Ge, Ge on Si, with and or without buried or embedded voids photodiodes and avalanche photodiodes, are in data and tele communications. According to some embodiments, these applications include: fiber to home, local area network, data center optical interconnects board to board, on the board, rack to rack, and chip to chip, between data centers, metro area network, and optical communication for distances from less than a centimeter to over 10 kilometers or more. The

applications in consumer space also includes: game box, personal computers, tablets, mobile devices such as smart phones, animations studios, and anywhere that benefits from a bandwidth of more than one gigabit per second. Other applications of the microstructured PDs and APDs, according to some embodiments, are in sensors where broadband communication is important, such as sensors for infrastructures, health, environment, oil exploration, where the sensors communicate with a remote receiver that is connected to data centers for data analysis.

[00245] Other applications of the microstructured PD and APD, according to some embodiments, are in analytical instruments and optical tests and measurement instruments where high sensitivity and bandwidth are important.

[00246] According to some embodiments, the microstructured PV have applications in energy harvesting for power generation all the way from gigawatts to watts, to power cities and homes to powering sensors. Since the microstructured PV is lightweight and high efficiency it can be used in mobile applications, space, solar transportation, recycling of photons in home, offices and factories. The PV can also be used on windows and can be semi-transparent.

[00247] The described microstructures in Si, Ge, Si regrowth with Ge, Ge on Si, pillars, holes, and voids can be any shape and form, and are not limited to the schematics shown. According to some embodiments, the dimensions range from 10-10000 nm (nanometers). The microstructures can be within each other such as pillar(s) in hole(s), hole(s) in pillar(s) and void(s) can be in the pillar, and buried and or embedded in any layer of the semiconductor heterogeneous or homogeneous. The material used includes semiconductors such as Si, Ge, GeSi, Ge on Si, and the III-V group material family of InP, GaN, InGaAsP, GaAs, and other semiconductors such as ZnO, CdTe, CuInGaSe (CIGS), amorphous Si, or any amorphous semiconductor and or microcrystalline and crystalline semiconductor. The material can be a combination of amorphous, microcrystalline, crystalline heterogeneous and or homogeneous. The material used is also not limited to semiconductors, but also include polymers, electrically conducting, semiconducting, non conducting polymers, organic and or inorganic polymers, glass, conducting, semiconducting, non conducting glass. Nanoparticles of semiconductors and or metal can also be buried in the polymer and glass.

Semiconductors, polymer and glass can exist within the same microstructure, separately or in any combination.

[00248] According to some embodiments, in silicon photonic circuit applications, optical waveguides such as shown in FIG. 50, *supra*, can be integrated with optical sources and optical detectors such as photodiodes, avalanche photodiodes and photoconductors. FIG. 52 is a cross section of a ridge waveguide integrated with a microstructured PD/APD, according to some embodiments. Device 5200 includes a ridge waveguide that is edge coupled to a microstructered Ge on Si photodiode or avalanche photodiode (with multiplication layers added). In the ridge wave guide portion, as shown in FIG. 50, a ridge 5202 has lower density voids 5212 and slab 5204 had higher density voids 5214. Ion implantation is used to increase the N doping (region 5224) for the PD and a coplanar transmission line is fabricated on the photodiode to extract the electrical signal as shown in FIG. 53, *infra*. Anode contact 5226 is made of P-Ge, according to some embodiments. The cathode contact is made to layer 5224 (cathode contact not shown for simplicity and clarity of drawing.)

[00249] FIG. 53 is a top view the integrated ridge waveguide and microstructured PD/APD shown in FIG. 52, according to some embodiments. The device 5200 is in a coplanar transmission line configuration. Ridge portion 5202 is 0.5 to 10 μm wide and 0.1 to 10 μm deep, according to some embodiments. Slab portion 5204 has higher density voids, as shown in FIG. 52, to vary the refractive index as a platform for silicon photonic circuits. Coplaner cathodes 5228 and 5230 are in contact with the N-Si ion implanted region 5224 shown in FIG. 52. According to some embodiments, the optical field can also be coupled evanescently by placing the PD/APD above the optical waveguide such that the optical field overlaps the absorbing I microstructures.

[00250] FIGs. 54A and 54B show a microwave transmission line on Si with voids, according to some embodiments. High bit rate transmission lines on silicon suffers from a multitude of effects, from slow wave to dispersion to loss. However by removing most of the silicon material with the addition of high-density voids according to some embodiments, the dispersion and loss can be alleviated and signal integrity restored. An advantage is that silicon can be the substrate for both microwave transmission line and for ICs without the use of intermediate ceramic

such as alumina for transmission line to connect various IC chips. FIG. 54A is a cross section showing high density voids 5314 buried in silicon 5304 which reduce the effective dielectric constant of the silicon, and disrupt lateral electrical conductivity which in turn can result in lower microwave loss and dispersion which are important as bit rate increases into the multi Gb/s range (e.g. 40-60 Gb/s). Coplanar microwave metallic transmission lines 5310 are provided as means to move the electrical signal to/from electronic devices (e.g. processors, storage devices, input-output devices, ASICs, CPUs, and memories) on the same substrate. FIG. 54B is a top view. Conventional techniques use multi chip carriers that need additional packaging. According to some embodiments, having many devices all on the same silicon substrate greatly reduces the cost since it can be all fabricated at once and requires no additional packaging for each chip. According to some embodiments, the voids 5314 are arranged in a fashion where the path length in silicon laterally is significantly increased in order to increase lateral resistivity. According to some embodiments, Ion implantation of protons and or oxygen can be used to further increase electrical resistivity. Although FIGs. 54A and 54B show a co-planar arrangement, according to some embodiments other microwave transmission line arrangements (e.g. microstrip, slotline, and stripline) are used with a semiconductor substrate having high-density buried voids. According to some embodiments, the positioning and/or other properties (e.g. size, shape, and filling material) of the high-density voids can be selected such that the slow wave effect can be manipulated or "tuned" in a way that is suitable for the application at hand.

[00251] FIG. 55 is a cross section of voids for thermal conduction and thermal isolation of heat producing ICs and light emitters, according to some embodiments. The buried voids in silicon 5404 can be filled with thermal conductors such as helium gas, metal such as copper, aluminum, tungsten, or ceramic such as boron nitride, or carbon, graphene, diamond like carbon, or heterogeneous material/ceramic doped with metal nanoparticles, carbon nanotubes. The voids 5414 underneath the heat producing elements such as ICs and CPUs 5422, and light emitters 5420 such as laser diodes and bipolar drivers, can be filled with enhanced thermal conductors to extract the heat from the hot components and direct it to a heat sink 5402. Voids 5412 between hot elements are kept at a low

thermal conducting state that are either in partial vacuum or filled with a gas such as nitrogen, argon, carbon dioxide, for example to prevent thermal cross talk between the hot components or to any other components where heat is not desirable. According to some embodiments, the voids are arranged in a fashion such that the path length in silicon is vastly increased to maintain low thermal crosstalk. According to some embodiments, the techniques of FIG. 55 are used to keep PVs cool when exposed to the sun. According to some embodiments, thermoelectric devices can be integrated together with the voids to generate electricity from the excess heat.

[00252] FIG. 56 is a cross section showing a distribution of voids to increase lateral path length for increasing lateral electrical resistivity and decrease lateral thermal conduction, according to some embodiments. The buried voids 5602 configured for microwave transmission lines and/or for thermal management can be arranged in a randomly, pseudo randomly, or in a pattern in areas where lateral electrical and thermal conductance is significantly reduced and vertical electrical and thermal conductance is significantly enhanced. There may be areas where lateral electrical and thermal conductance enhancement is desired, in which case the voids can overlap to form a conducting channel.

[00253] This patent application refers to certain theories in explaining the nature and operation of devices, but it should be clear that such theories are based on current understanding and do not affect the actual operation of the disclosed devices even if future developments prove the theories incorrect. This patent specification also refers to numerical ranges of paramaters, and it should be understood that insubstantial departures from such ranges are still within the spirit of the disclosed advancements.

[00254] Although the foregoing has been described in some detail for purposes of clarity, it will be apparent that certain changes and modifications may be made without departing from the principles thereof. It should be noted that there are many alternative ways of implementing both the processes and apparatuses described herein. Accordingly, the present embodiments are to be considered as illustrative and not restrictive, and the body of work described herein is not to be limited to the details given herein, which may be modified within the scope and equivalents of the appended claims.

CLAIMS

What it claimed is:

1. A photodetector with microstructure-enhanced photoabsorption comprising:
a cathode region;
an anode region;
reverse biasing circuitry configured to apply a voltage between said cathode and anode regions such that said cathode region is driven to a more positive voltage than said anode region; and
a microstructure-enhanced photon absorbing semiconductor region operatively associated with the cathode and anode regions and configured to absorb photons from a source signal, said absorbing region including a plurality of microstructures configured to increase absorption of photons at a range of wavelengths that includes a wavelength of said source signal relative to an absorbing region that is not intentionally microstructure-enhanced.

2. A photodetector according to claim 1 wherein said microstructures are configured to increase absorption of photons at the range of wavelengths by being dimensioned and positioned to facilitate said increase of absorption.

3. A photodetector according to claim 2 wherein said microstructures have at least one dimension that is equal to or shorter than a longest wavelength in the range of wavelengths.

4. A photodetector according to claim 1 wherein said microstructures have one or more shapes selected from a group consisting of pillars, holes and voids.

5. A photodetector according to claim 1 wherein said microstructures are arranged into a periodically-spaced array.

6. A photodetector according to claim 1 wherein said microstructures are arranged into a non-periodically-spaced, randomly-spaced or multiperiodically-spaced array.

7. A photodetector according to claim 1 further including a substrate material and wherein said microstructures have a major longitudinal axis normal to an upper surface of the substrate material.

8. A photodetector according to claim 1 wherein said microstructures have major longitudinal axes that are not parallel to one another.

9. A photodetector according to claim 1 wherein said microstructures are oriented to reduce cross-talk in an application selected from a group consisting of: free space applications and coupling to multiple sources in an array, compared to an otherwise same photodetector.

10. A photodetector according to claim 1 wherein said microstructures are oriented to reduce sensitivity to any single direction of said source signal compared to an otherwise same photodetector.

11. A photodetector according to claim 1 wherein the microstructures increase absorption compared to an otherwise same photodetector at least in part by forming an absorbing mode high contrast grating.

12. A photodetector according to claim 11 wherein the microstructures increase absorption compared to an otherwise same photodetector at least in part due to one or more of the following effects: resonance effects, scattering effects, near field effects, sub-wavelength effects, and interference effects.

13. A photodetector according to claim 11 wherein said high contrast grating is in 2-dimensions or 3-dimensions.

14. A photodetector according to claim 11 wherein said high contrast grating is of one or more types selected from a group consisting of: periodic, aperodic, chirped, random, pseudo random.

15. A photodetector according to claim 11 wherein contrast for said high contrast grating is increased using a plurality of voids in one or more materials compared to an otherwise same photodetector.

16. A photodetector according to claim 1 wherein said microstructure-enhanced photon absorbing semiconductor region and said microstructures are formed of silicon.

17. A photodetector according to claim 16 wherein said photodetector is a silicon photodiode.

18. A photodetector according to claim 17 wherein said photodetector is configured to detect said source signal at a data bandwidth of greater than 5 gigabits per second, at source signal wavelengths of 850 nanometers with a quantum efficiency of at least 60%.

19. A photodetector according to claim 18 wherein said photodetector is configured to detect said source signal at a data bandwidth of greater than 10 gigabits per second, at source signal wavelengths of 850 nanometers with a quantum efficiency of at least 60%.

20. A photodetector according to claim 17 wherein said photodetector is configured for quantum efficiency of greater than 60%.

21. A photodetector according to claim 16 wherein said photodetector is an avalanche photodiode.

22. A photodetector according to claim 21 wherein said avalanche photodiode is configured to detect said source signal at a data bandwidth of greater than 5 gigabits per second, at source signal wavelengths of 850 nanometers, and having a gain of greater than 2.

23. A photodetector according to claim 21 further comprising a multiplication region that includes a second plurality of microstructures.

24. A photodetector according to claim 23 wherein said second plurality of microstructures extends into one or more multiplication layers selected from a group consisting of: P multiplication layer, N multiplication layer and charge layer.

25. A photodetector according to claim 16 wherein said photodetector is configured to detect said source signal at a data bandwidth of greater than 1 gigabit per second, at source signal wavelengths of 980 nanometers with a quantum efficiency of at least 40%.

26. A photodetector according to claim 16 wherein said photodetector is configured to detect said source signal at a data bandwidth of greater than 0.5 gigabits per second, at source signal wavelengths of 1000 nanometers with a quantum efficiency of at least 30%.

27. A photodetector according to claim 1 wherein said plurality of microstructures effectively reduces capacitance of the photodetector when compared to a microstructure-free device having a similar photon absorbing length.

28. A photodetector according to claim 1 wherein said microstructure-enhanced photon absorbing semiconductor region and said microstructures are formed of silicon and germanium.

29. A photodetector according to claim 28 wherein said microstructures are formed by etching away portions of silicon and using a selective area growth process to grow germanium in the etched away portions.

30. A photodetector according to claim 1 wherein said microstructure-enhanced photon absorbing semiconductor region and said microstructures are formed of germanium.

31. A photodetector according to claim 30 further including a substrate and wherein said cathode, absorbing and anode regions are formed above the substrate and said photodetector is configured to receive said source signal from a substrate-side of the photodetector.

32. A photodetector according to claim 31 wherein said anode region comprises a germanium P layer formed by an epitaxial lateral overgrowth process.

33. A photodetector according to claim 31 wherein the photodetector is configured for a portion of the source signal to pass through the absorbing region a first time, reflect from a surface and thereafter pass through the absorbing region a second time.

34. A photodetector according to claim 30 further including a substrate and wherein said cathode, absorbing and anode regions are formed above the substrate and said photodetector is configured to receive said source signal from directions facing a side of the photodetector opposite of said substrate.

35. A photodetector according to claim 34 wherein said anode region comprises a silicon P layer.

36. A photodetector according to claim 30 wherein said photodector is an avalanche photodiode and further comprises a multiplication region formed of silicon.

37. A photodetector according to claim 36 wherein said anode region comprises a germanium P layer formed by an epitaxial lateral overgrowth process.

38. A photodetector according to claim 36 wherein said avalanche photodiode is configured to detect said source signal at a data bandwidth of greater than 1 gigabit per second, at source signal wavelengths of 1750 nanometers or shorter, and having a gain of greater than 2.

39. A photodetector according to claim 36 wherein at least one germanium layer is grown epitaxiallly on a silicon layer.

40. A photodetector according to claim 1 wherein said microstructure-enhanced photon absorbing semiconductor region and said microstructures are at least partially formed of a III-V family material.

41. A photodetector according to claim 40 wherein said III-V family material is selected from a group consisting of: InP, GaAs, InGaAs, GaN, InGaN, InGaAsP, AlGaAs, AlGaN, GaP, InSb and InAs.

42. A photodetector according to claim 40 wherein said III-V family material is formed using a selective area growth process.

43. A photodetector according to claim 40 wherein said photodector is an avalanche photodiode and further comprises a multiplication region formed of silicon.

44. A photodetector according to claim 1 wherein said plurality of microstructures include voids buried within the absorbing semiconductor region.

45. A photodetector according to claim 44 wherein the absorbing semiconductor region is made of a material selected from a group consisting of silicon and germanium.

46. A photodetector according to claim 1 further comprising a plurality of voids buried in a layer of material effectively lowering a refractive index at said

range of wavelengths and lowering capacitance of said layer of material compared to the material when free of intentional voids.

47. A photodetector according to claim 46 wherein said layer of material is an N layer formed on a substrate material.

48. A photodetector according to claim 46 wherein said photodetector is an avalanche photodiode and said layer of material forms a multiplication layer of the avalanche photo diode.

49. A photodetector according to claim 46 wherein said plurality of voids are filed with a material selected from a group consisting: nitrogen, argon, polymer, amorphous semiconductor material, and glass.

50. A photovoltaic device comprising a semiconductor material having a plurality of voids buried therein, the semiconductor material configured to convert solar radiation into direct current electricity.

51. A device according to claim 50 wherein said plurality of voids are microstructured voids configured to enhance absorption of said semiconductor material to thereby increase conversion efficiency of the device compared with the material when free of intentional microstructured voids.

52. A device according to claim 50 wherein said plurality of voids are sized and/or spaced apart by less than 3 microns, and are configured to alter an effective refractive index of the semiconductor material near a surface of the semiconductor material to reduce reflection of incident sunlight from the device compared with an otherwise same device.

53. A device according to claim 50 wherein said plurality of microstructured voids are sized and/or spaced apart by less than 3 microns, and are configured to alter an effective refractive index of the semiconductor material

near a surface of the semiconductor material to increase internal reflection within the semiconductor material compared to an otherwise same device.

54. A glass material comprising a glass having a plurality of buried voids dimensioned between 0.01 microns to 1000 microns.

55. A glass material according to claim 54 wherein the material forms a part of a photovoltaic device.

56. A glass material according to claim 54 wherein said buried voids are filled with a material selected from a group consisting of: gel, polymer and gas.

57. A device according to claim 54 wherein said plurality of buried voids are configured to provide flexibility of the glass material.

58. A device according to claim 54 wherein said plurality of buried voids are configured to provide increased resistance of the glass material to physical damage and/or damage propagation compared to an otherwise same device.

59. A microwave transmission line structure comprising:
a semiconductor substrate material including a plurality of high-density dielectric-filled voids configured to reduce a dielectric constant of the semiconductor substrate material; and
a plurality of metallic microwave transmission lines, at least one of which is positioned above said semiconductor substrate material and is operatively associated therewith.

60. A structure according to claim 59 wherein said dielectric-filled voids are filled with one or more dielectric materials selected from a group consisting of: nitrogen, argon, vacuum, air, helium, polymer, metal oxides, silicon dioxide, silicon nitride, calcium fluoride, and zinc oxide.

61. A structure according to claim 59 wherein said voids are further configured to reduce dispersion and reduce loss associated with said microwave transmission lines at least in part by reducing current loop flow and/or eddy currents compared to an otherwise same structure.

62. A structure according to claim 59 wherein said plurality of metallic microwave transmission lines are arranged in a manner selected from a group consisting of: coplanar, microstrip, slotline, and stripline.

63. An optical waveguide structure comprising:
an optical mode region; and
a supporting semiconductor material adjacent to said optical mode region, wherein said supporting material includes a plurality of microstructured voids formed therein that are configured to alter an effective index of refraction of said supporting material.

64. An optical waveguide structure according to claim 63 wherein said effective index of refraction depends on a density of the plurality of microstructured voids.

65. An optical waveguide structure according to claim 63 wherein said optical mode region is formed into a ridge supported by said supporting semiconductor material.

66. An optical waveguide structure according to claim 63 wherein said optical mode region is surrounded by said supporting semiconductor material.

67. An optical waveguide structure according to claim 63 wherein said optical mode region includes a second plurality of microstructured voids formed therein that are configured to alter an effective index of refraction of said optical mode region.

68. A heat exchanger system comprising:

a heat generating device;
a heat sink configured to dissipate heat to a surrounding medium; and
an intermediate material mounted between said heat generating device and said heat sink, the intermediate material including a plurality of buried voids configured to alter thermal conductivity of said intermediate material.

69. A heat exchanger according to claim 68 wherein a first portion of said buried voids are filled with thermally conductive material and a second portion of said buried voids are filled with a thermally isolating material, the first and second portions being positioned to conduct heat from said heat generating device to said heat sink and to reduce thermal cross talk with other heat sensitive devices mounted on said intermediate material.

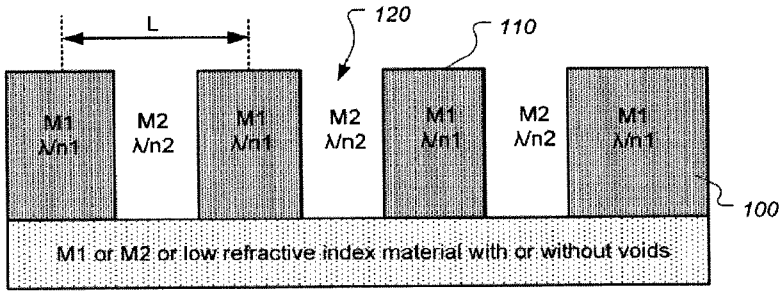

FIG. 1

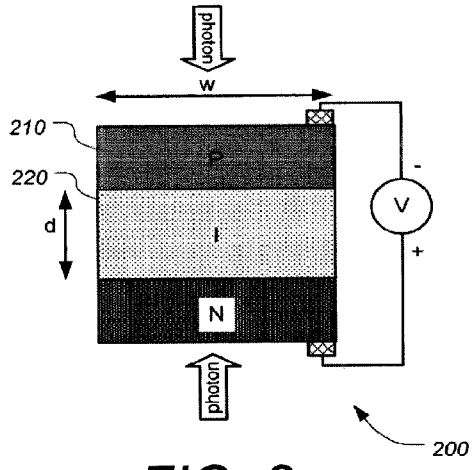

FIG. 2
(prior art)

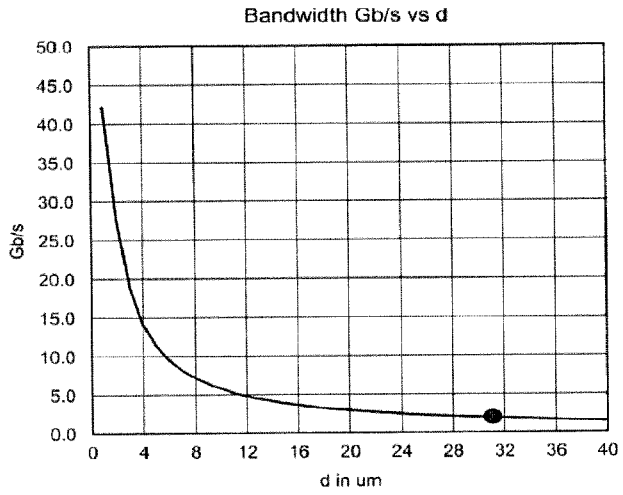

FIG. 3A
(prior art)

310

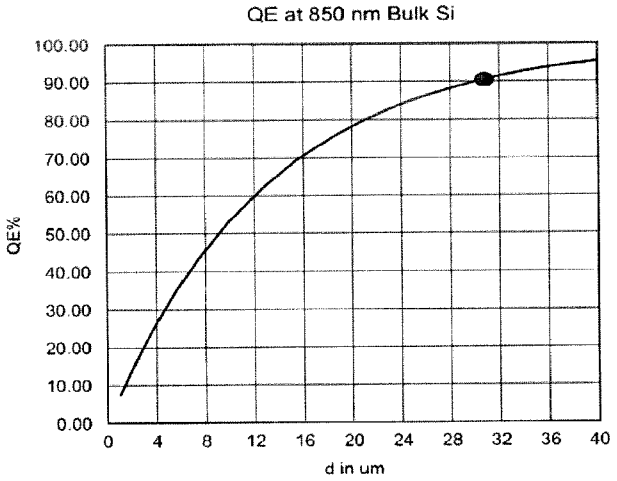

FIG. 3B
(prior art)

312

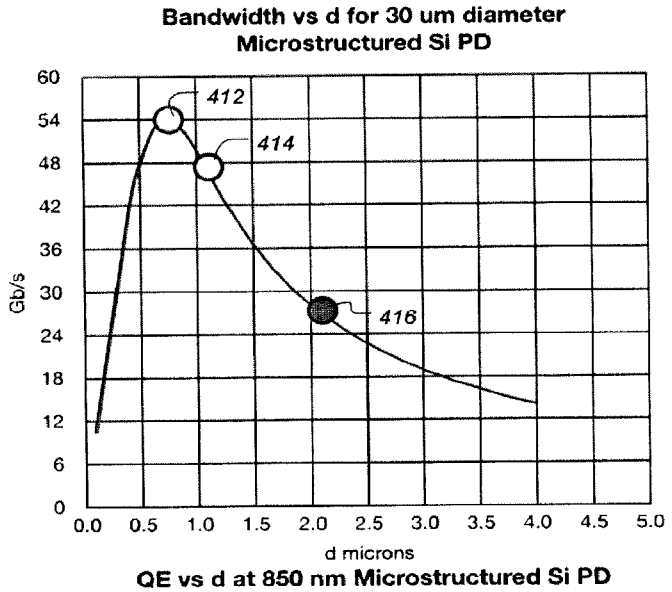

FIG. 4A

410

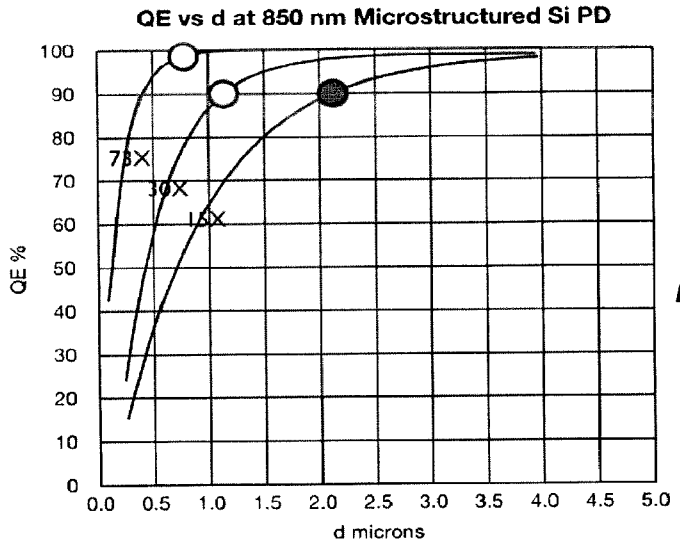

FIG. 4B

420

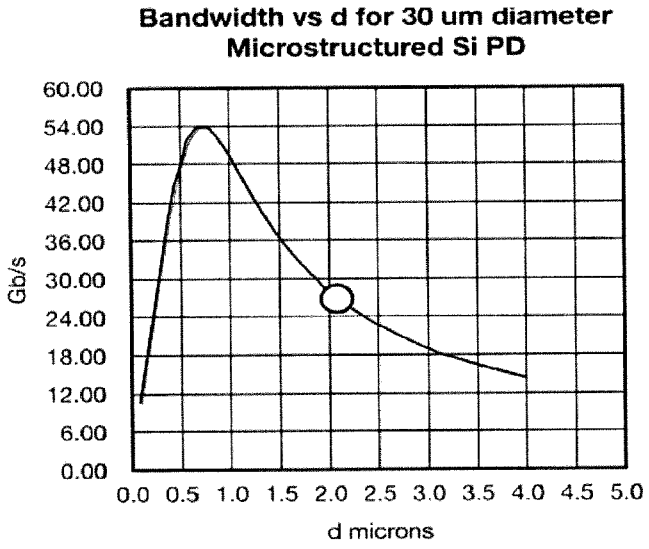

FIG. 4C

430

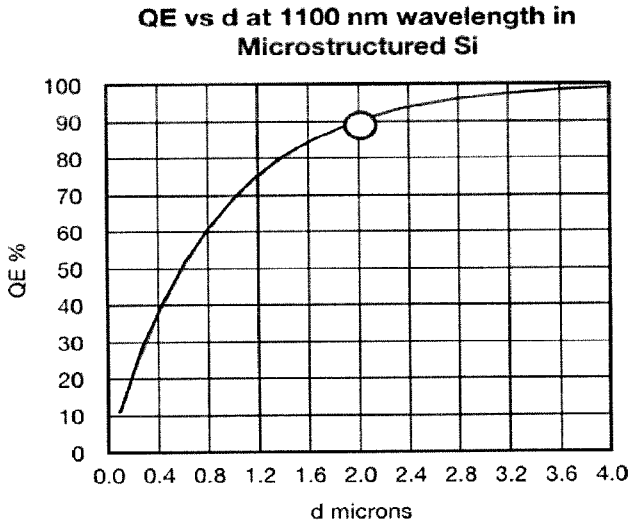

FIG. 4D

440

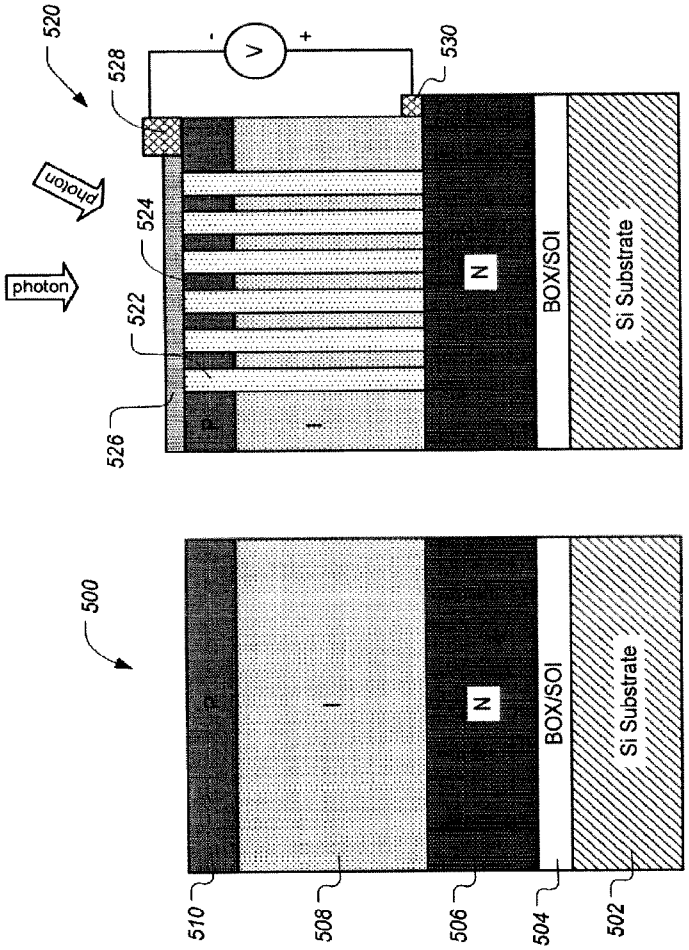
520
528
530
V
-
+
photon
photon
524
522
526
P
I
N
BOX/SOI
Si Substrate

FIG. 5B

500
P
I
N
BOX/SOI
Si Substrate
510
508
506
504
502

FIG. 5A

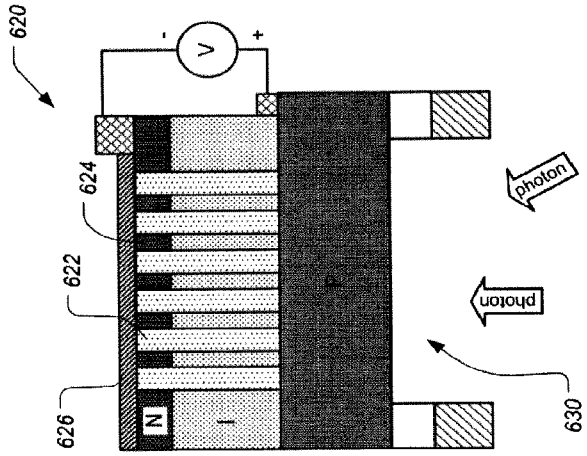
620
-
V
+
624
622
626
N
I
P
photon
photon
630

FIG. 6B

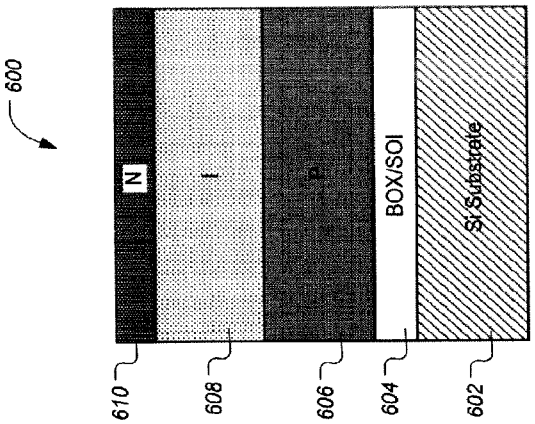
600
N
I
P
BOX/SOI
Si Substrate
610
608
606
604
602

FIG. 6A

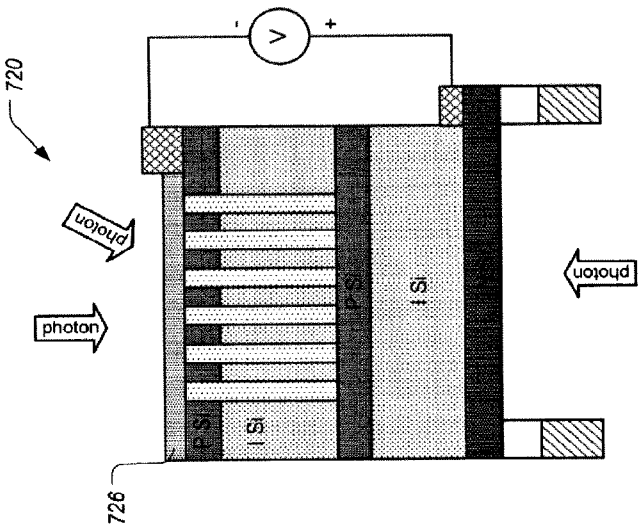
720
-
+
photon
photon
photon
P Si
I Si
P Si
I Si
726

FIG. 7B

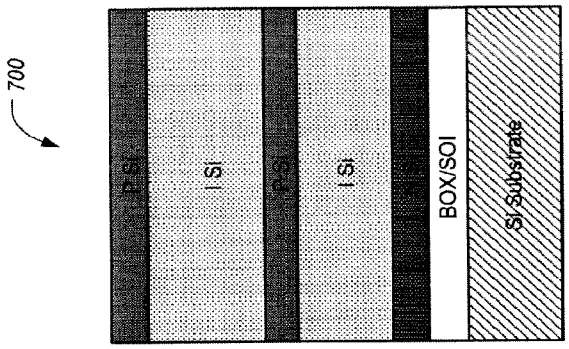
700
P Si
I Si
P Si
I Si
BOX/SOI
Si Substrate

FIG. 7A

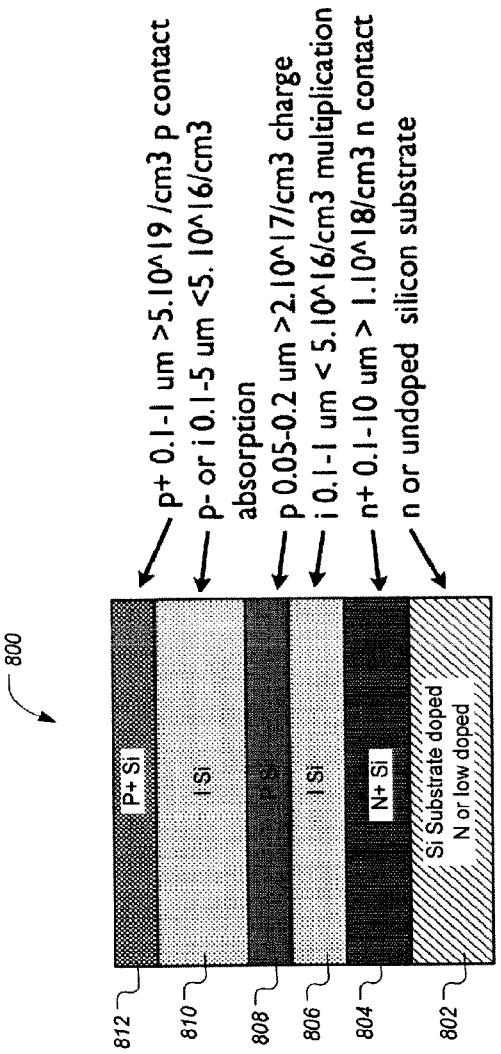
800
P+ Si
I Si
P Si
I Si
N+ Si
Si Substrate doped
N or low doped
812
810
808
806
804
802
p+ 0.1-1 um >5.10^19 /cm3 p contact
p- or i 0.1-5 um <5. 10^16/cm3
absorption
p 0.05-0.2 um >2.10^17/cm3 charge
i 0.1-1 um < 5.10^16/cm3 multiplication
n+ 0.1-10 um > 1.10^18/cm3 n contact
n or undoped silicon substrate

FIG. 8

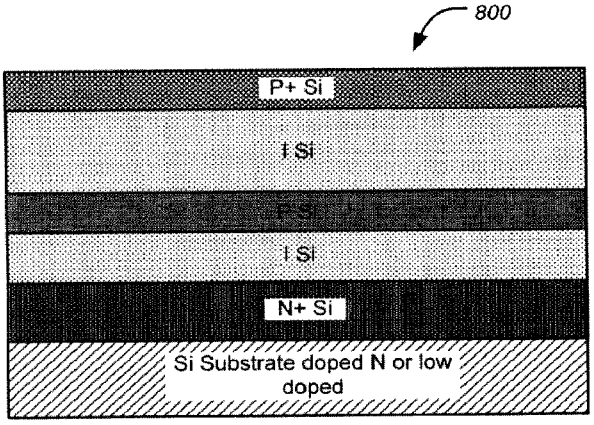
800
P+ Si
I Si
P Si
I Si
N+ Si
Si Substrate doped N or low doped

FIG. 9A

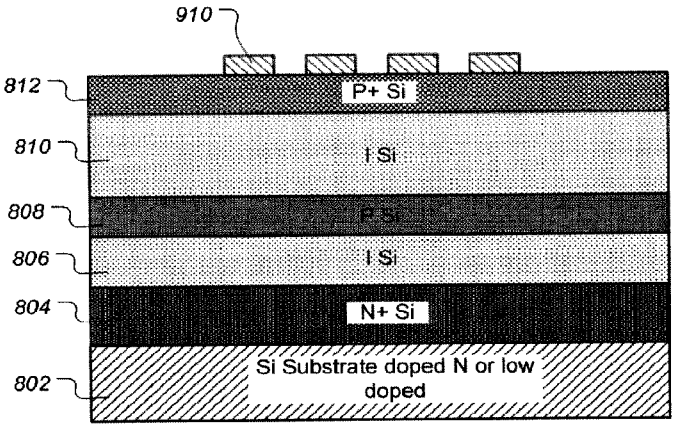
910
812
810
808
806
804
802
P+ Si
I Si
P Si
I Si
N+ Si
Si Substrate doped N or low doped

FIG. 9B

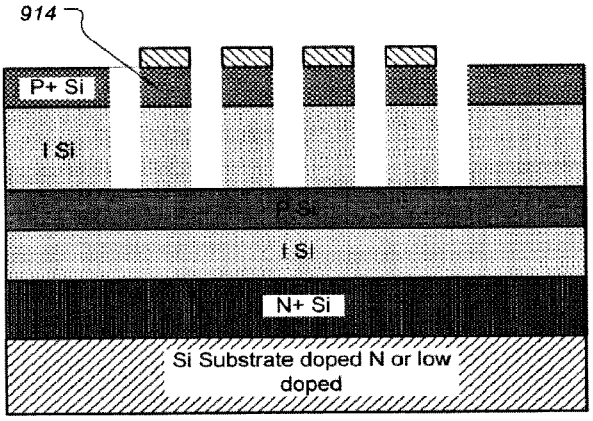
914
P+ Si
I Si
P Si
I Si
N+ Si
Si Substrate doped N or low doped

FIG. 9C

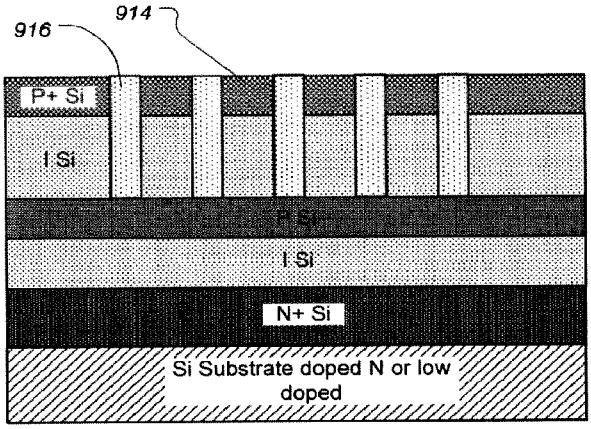
916
914
P+ Si
I Si
P Si
I Si
N+ Si
Si Substrate doped N or low doped

FIG. 9D

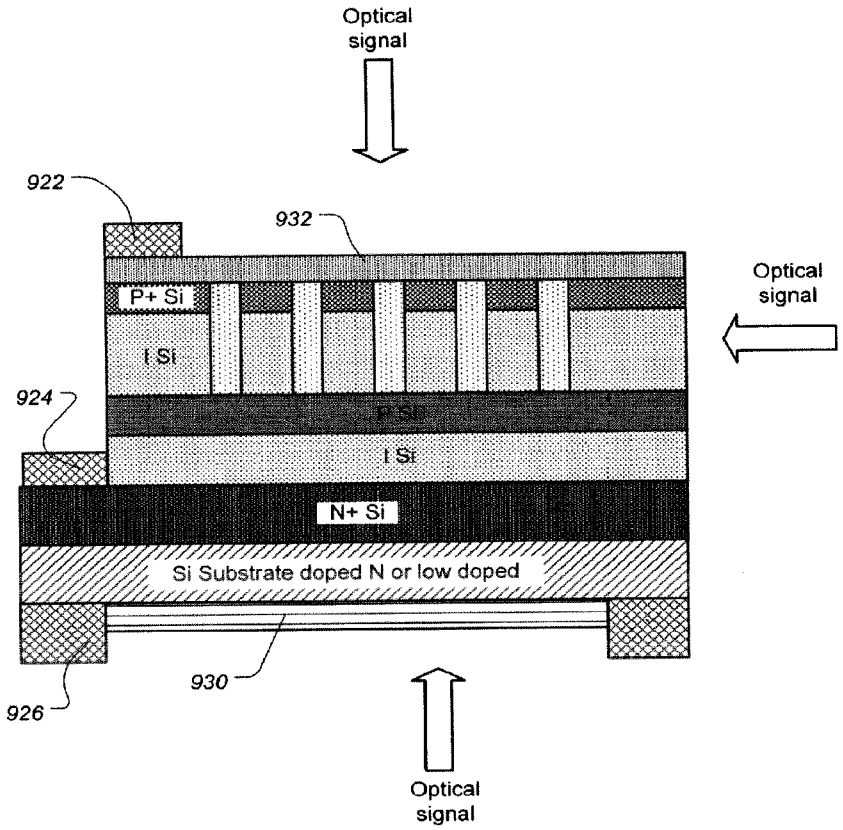
Optical signal
922
932
Optical signal
P+ Si
I Si
924
P Si
I Si
N+ Si
Si Substrate doped N or low doped
930
926
Optical signal

FIG. 9E

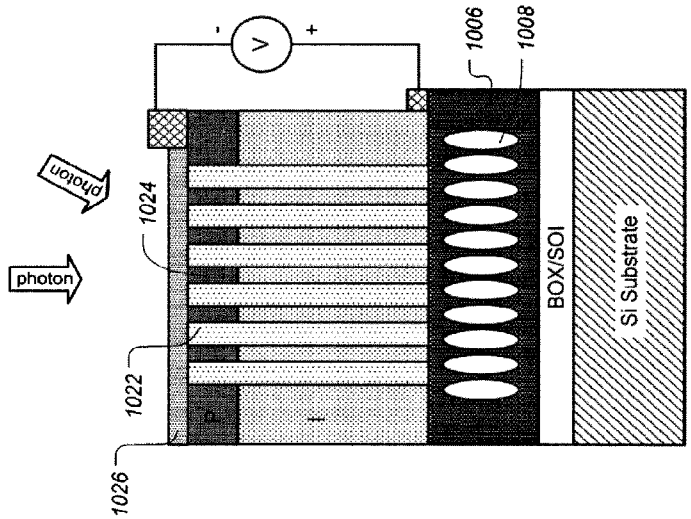

FIG. 10B

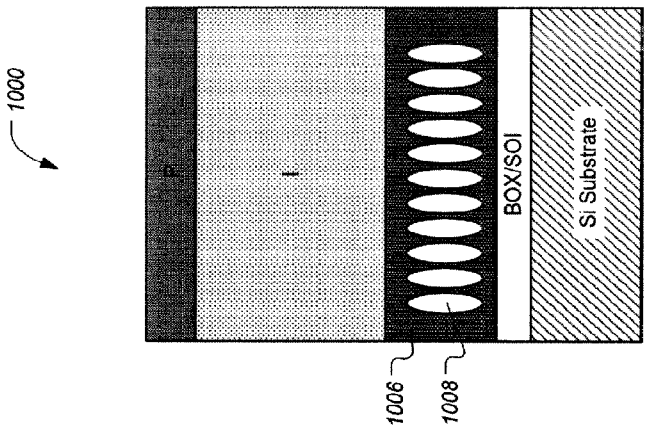

FIG. 10A

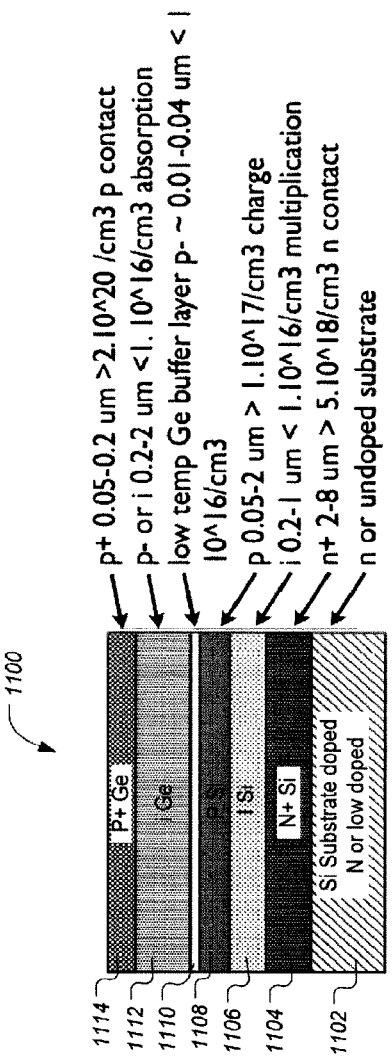
1100
P+ Ge
Ge
P Si
I Si
N+ Si
Si Substrate doped
N or low doped
1114
1112
1110
1108
1106
1104
1102
p+ 0.05-0.2 um >2.10^20 /cm3 p contact
p- or i 0.2-2 um <1. 10^16/cm3 absorption
low temp Ge buffer layer p- ~ 0.01-0.04 um < 1
10^16/cm3
p 0.05-2 um > 1.10^17/cm3 charge
i 0.2-1 um < 1.10^16/cm3 multiplication
n+ 2-8 um > 5.10^18/cm3 n contact
n or undoped substrate

FIG. 11A

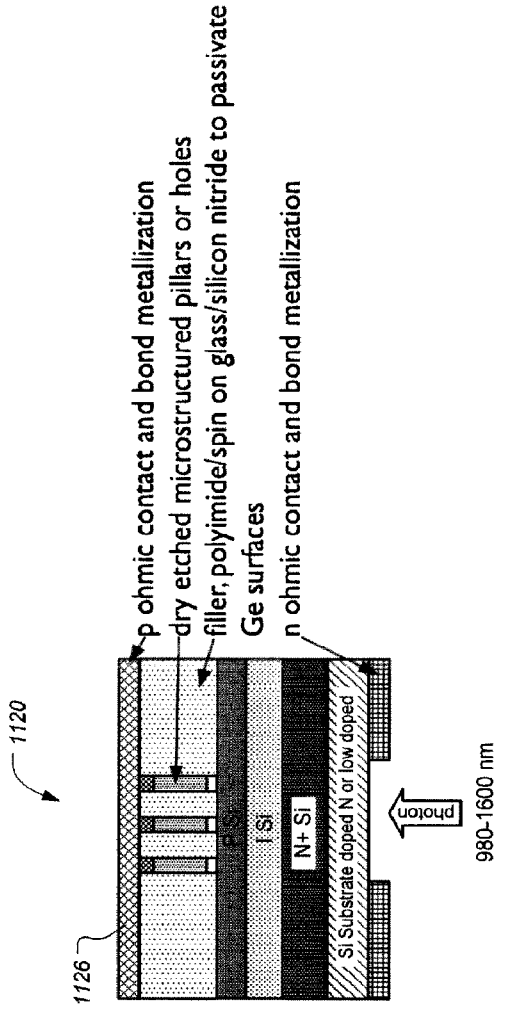
1120
1126
p ohmic contact and bond metallization
dry etched microstructured pillars or holes
filler, polyimide/spin on glass/silicon nitride to passivate
Ge surfaces
n ohmic contact and bond metallization
P+ Si
I Si
N+ Si
Si Substrate doped N or low doped
photon
980-1600 nm

FIG. 11B

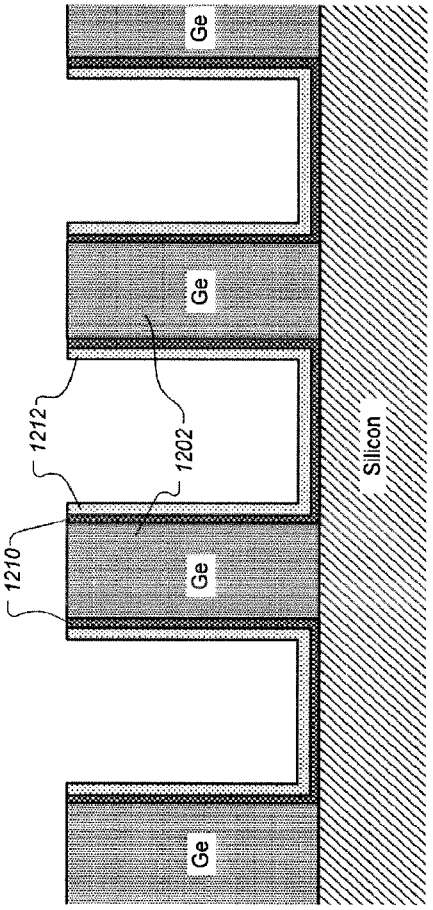

FIG. 12

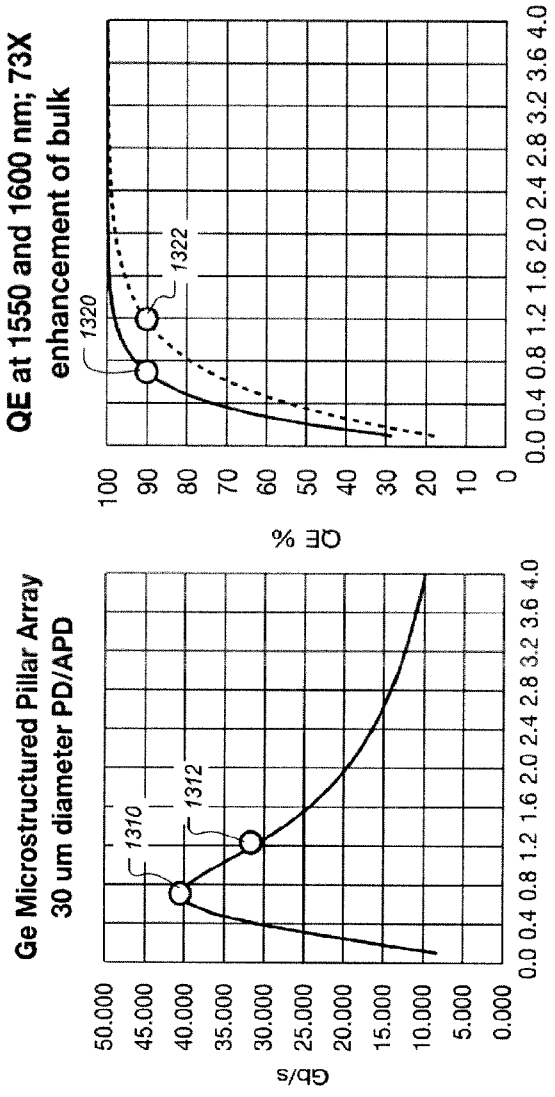

FIG. 13A

FIG. 13B

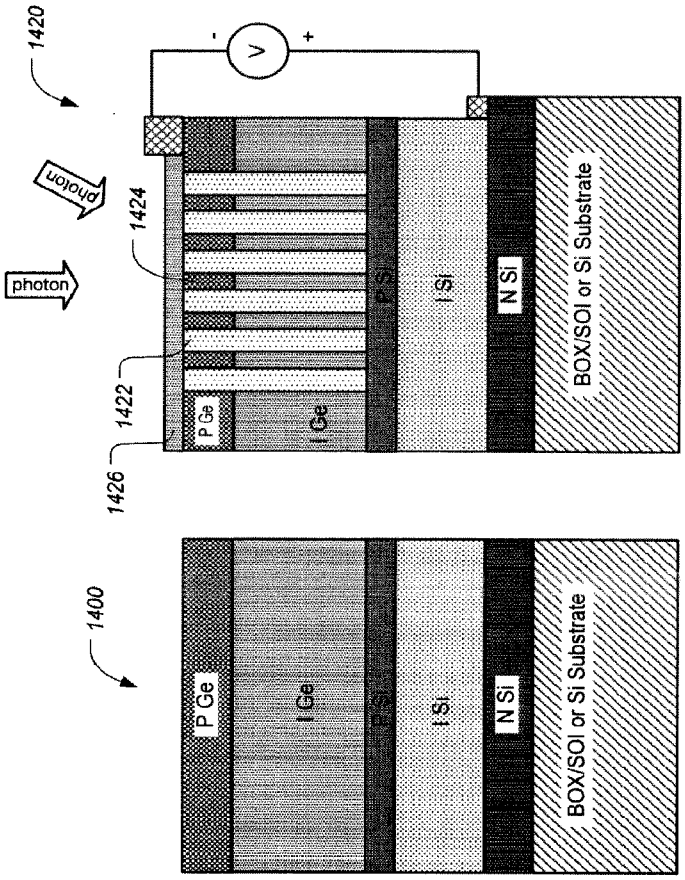

FIG. 14B

FIG. 14A

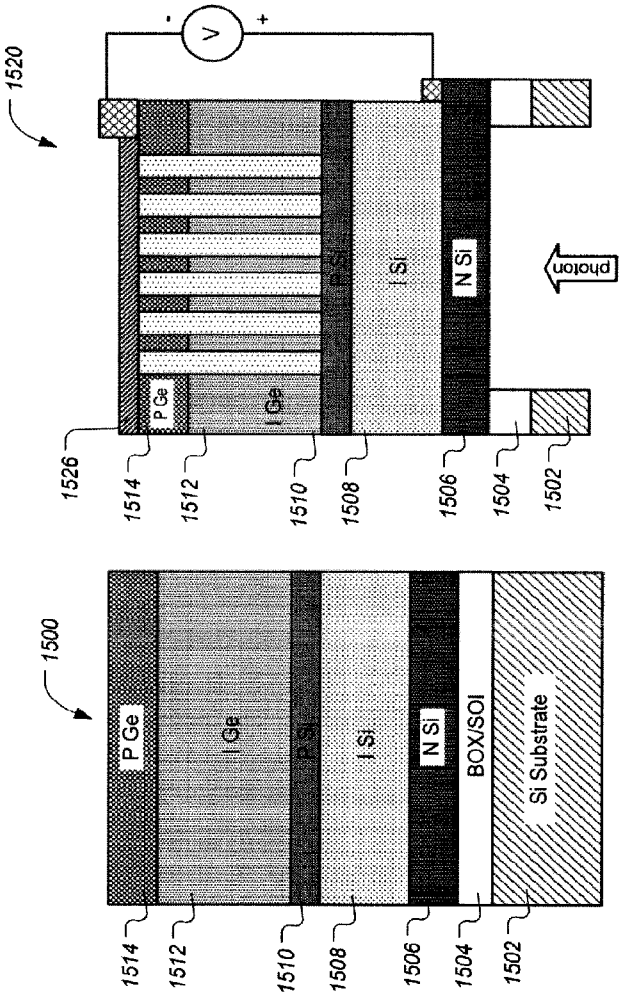

FIG. 15B

FIG. 15A

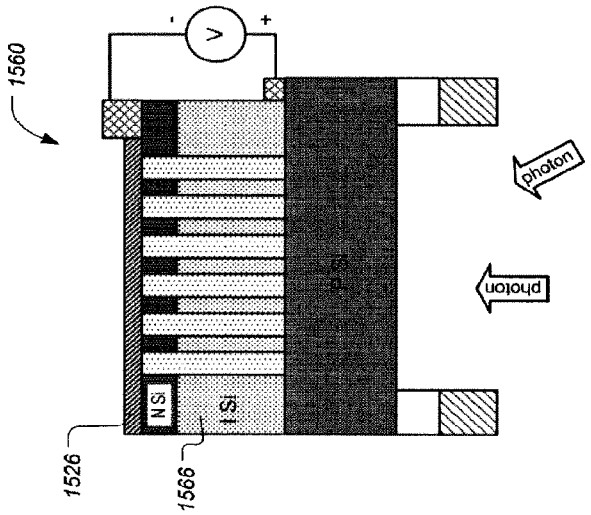

FIG. 15D

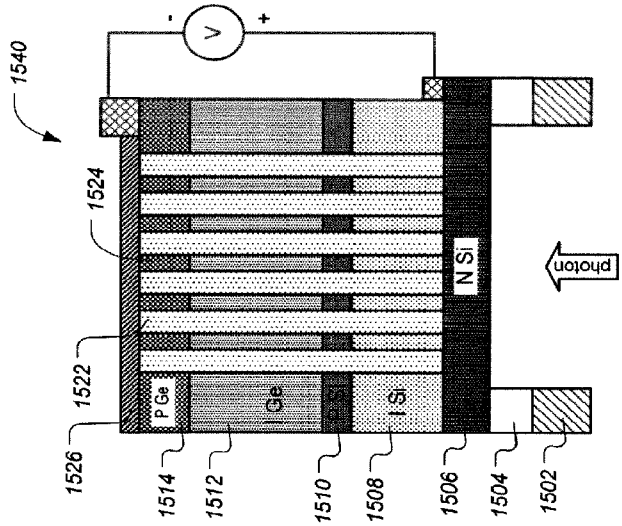

FIG. 15C

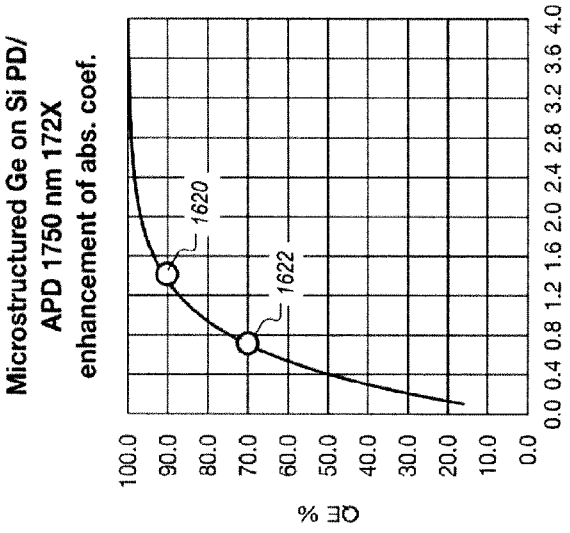

FIG. 16B

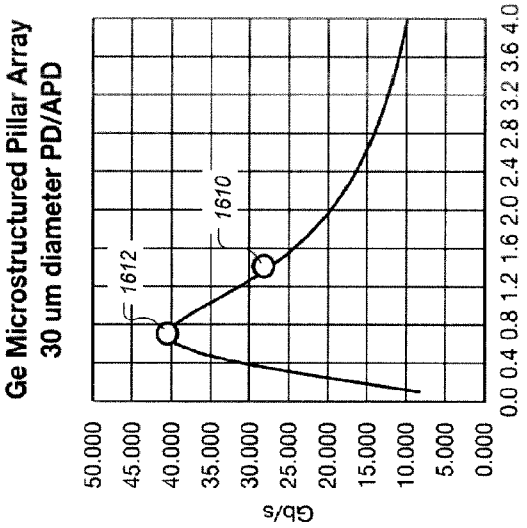

FIG. 16A

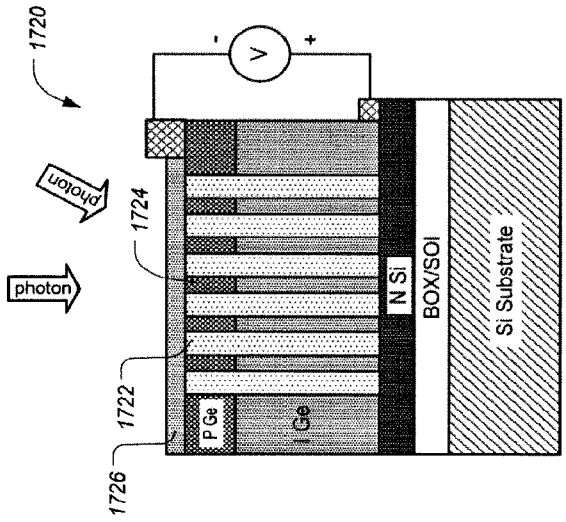

FIG. 17B

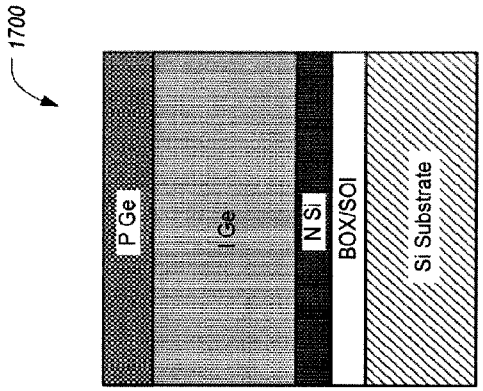

FIG. 17A

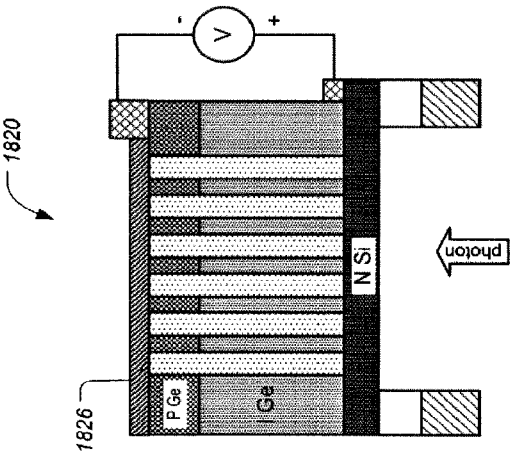

FIG. 18B

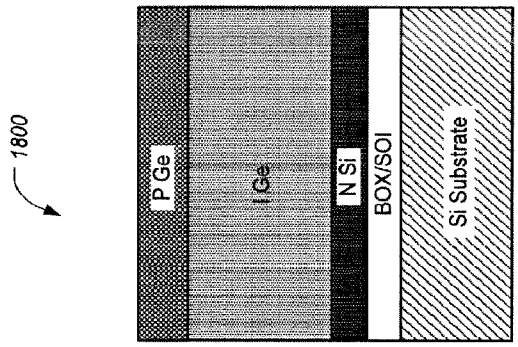

FIG. 18A

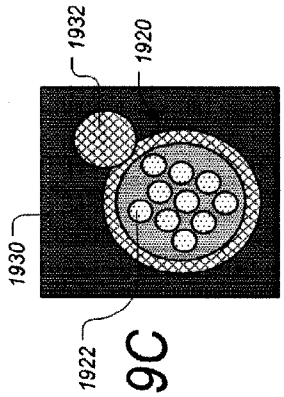

FIG. 19C

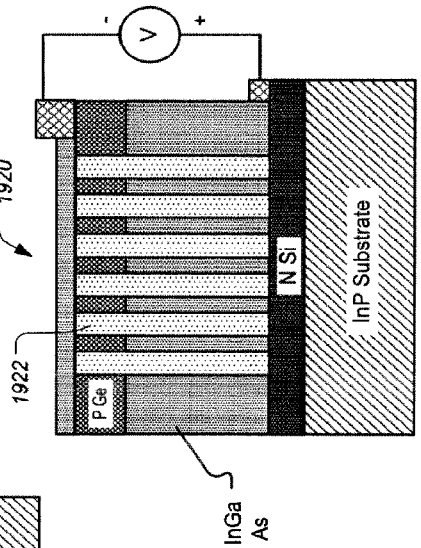

FIG. 19B

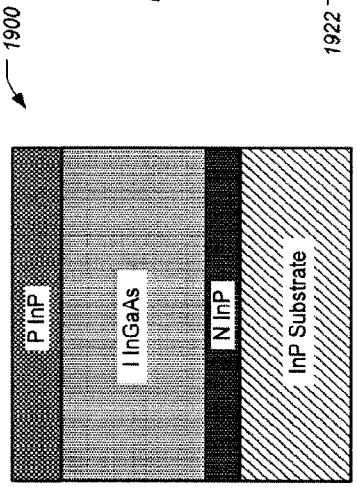

FIG. 19A

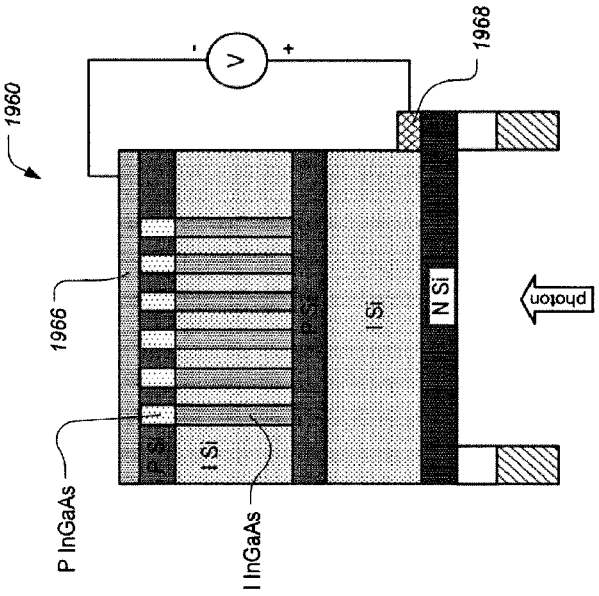

FIG. 19E

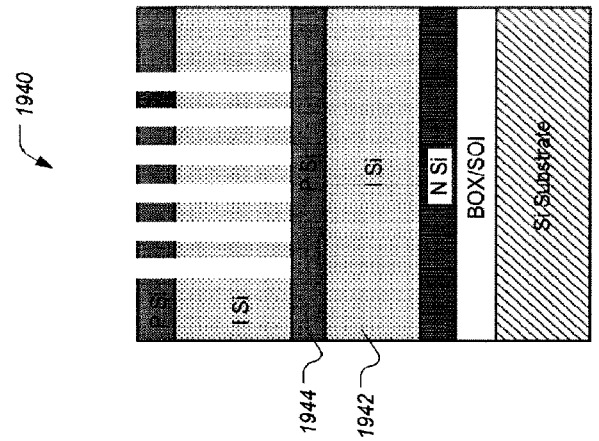

FIG. 19D

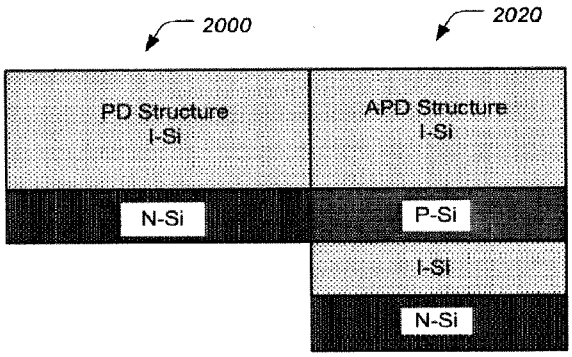
2000
2020
PD Structure
I-Si
APD Structure
I-Si
N-Si
P-Si
I-Si
N-Si

FIG. 20

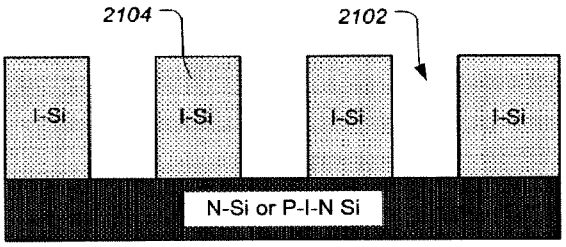
2104
2102
I-Si
I-Si
I-Si
I-Si
N-Si or P-I-N Si

FIG. 21

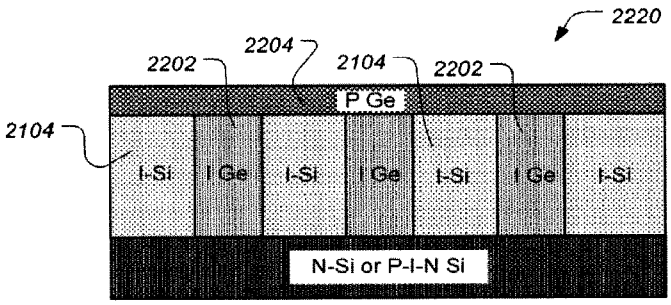
2220
2202
2204
2104
2202
P Ge
2104
I-Si
I Ge
I-Si
I Ge
I-Si
I Ge
I-Si
N-Si or P-I-N Si

FIG. 22

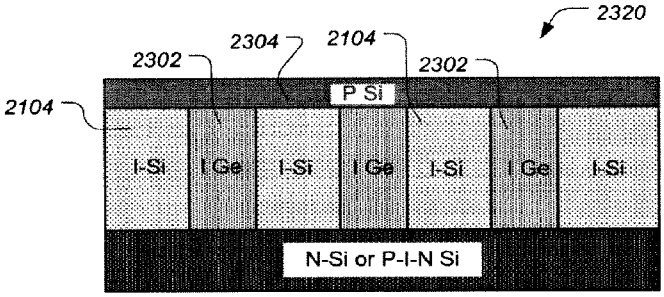
2320
2302
2304
2104
2302
P Si
2104
I-Si
I Ge
I-Si
I Ge
I-Si
I Ge
I-Si
N-Si or P-I-N Si

FIG. 23

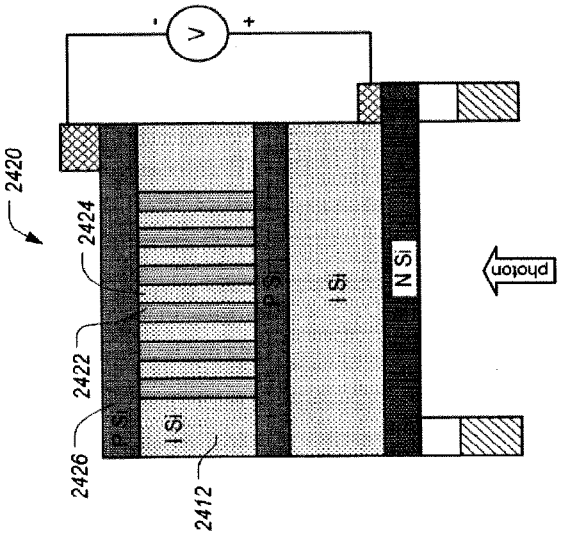

FIG. 24B

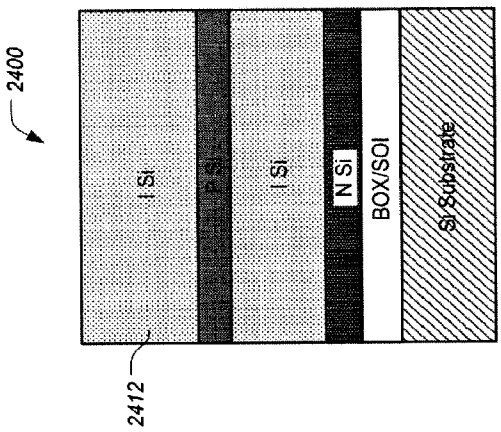

FIG. 24A