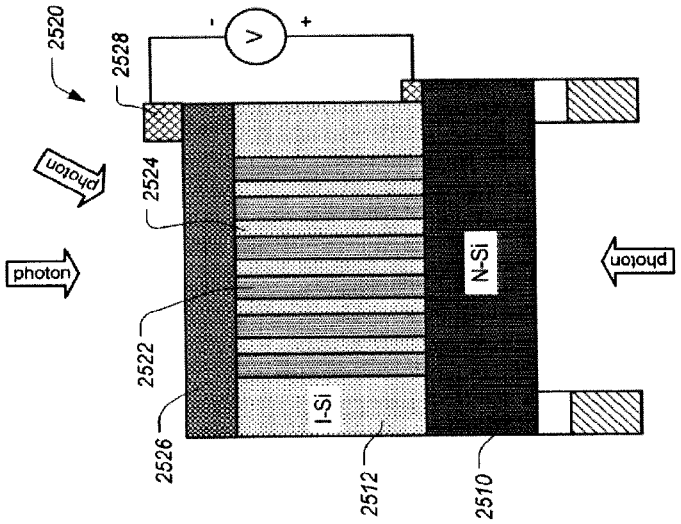


FIG. 25B

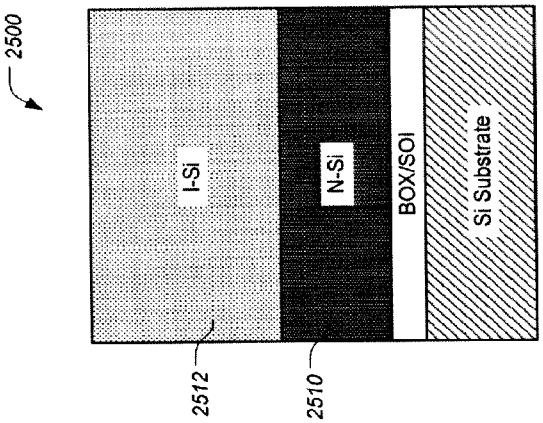


FIG. 25A

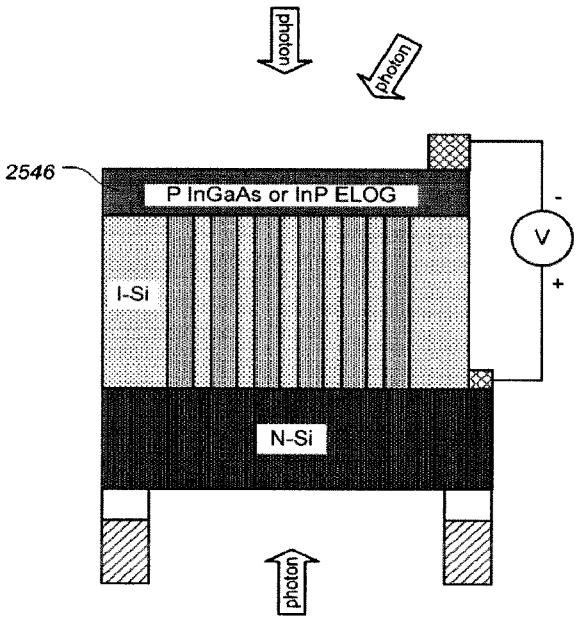


FIG. 25C

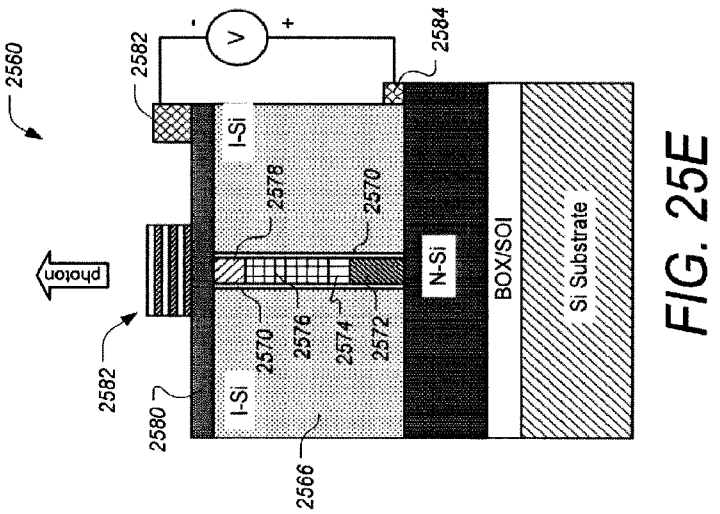


FIG. 25E

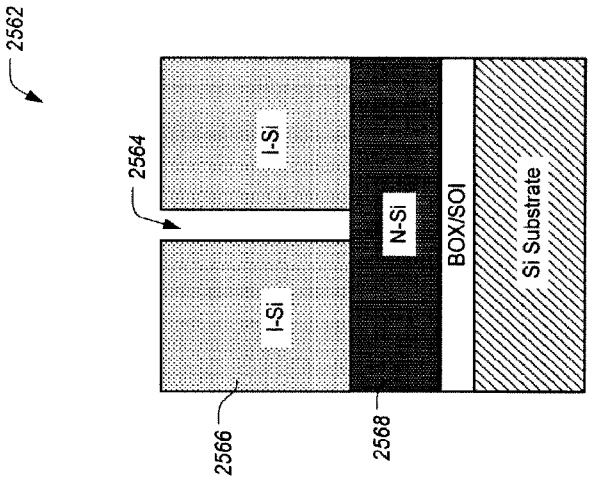


FIG. 25D

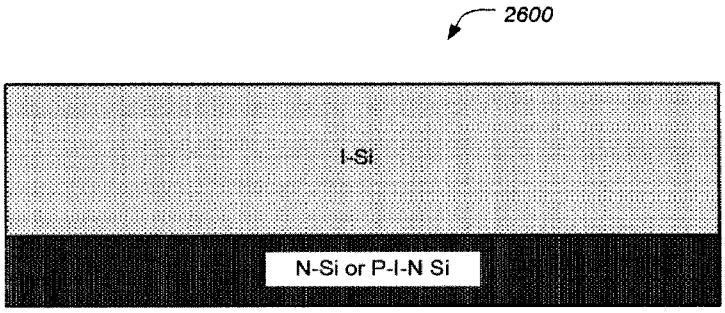


FIG. 26

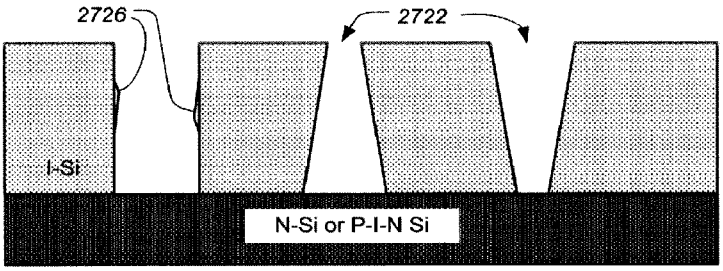


FIG. 27

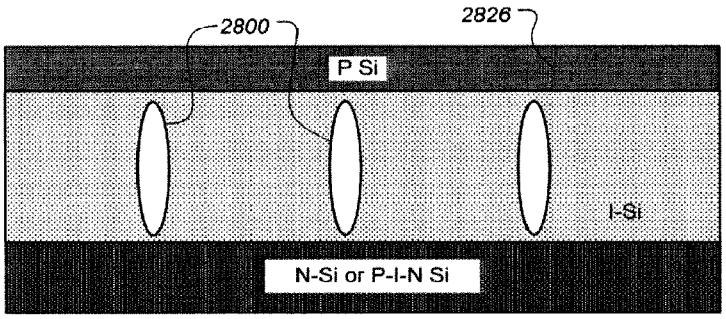

2800
2826
P Si
I-Si
N-Si or P-I-N Si

FIG. 28

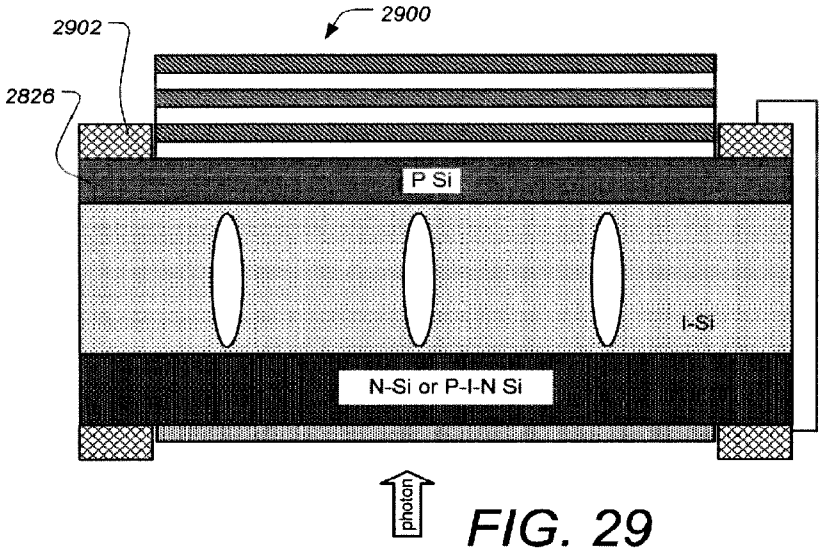

2902
2900
2826
P Si
I-Si
N-Si or P-I-N Si
photon

FIG. 29

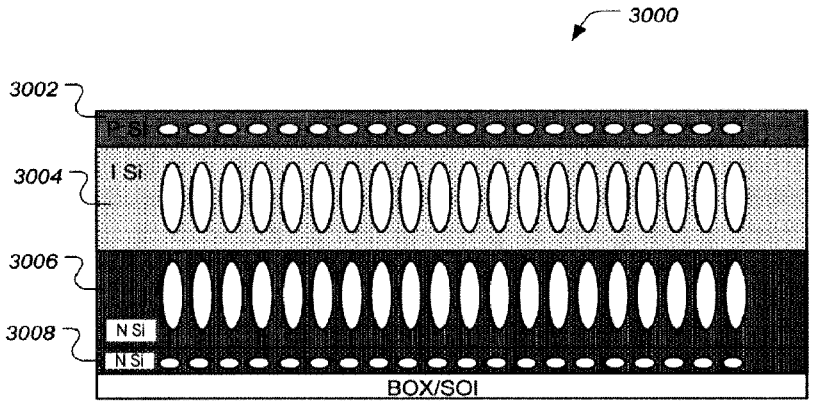

3000
3002
P Si
3004
I Si
3006
3008
N Si
N Si
BOX/SOI

FIG. 30

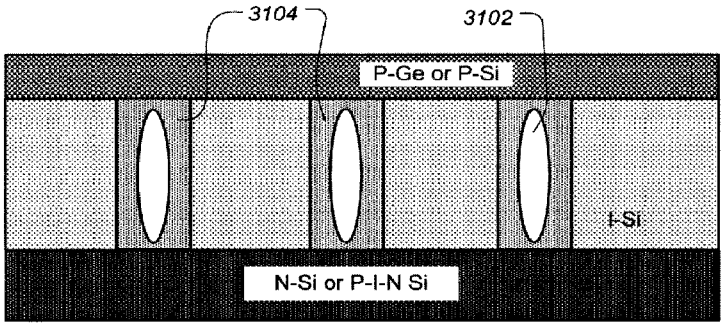

3104
3102
P-Ge or P-Si
I-Si
N-Si or P-I-N Si

FIG. 31

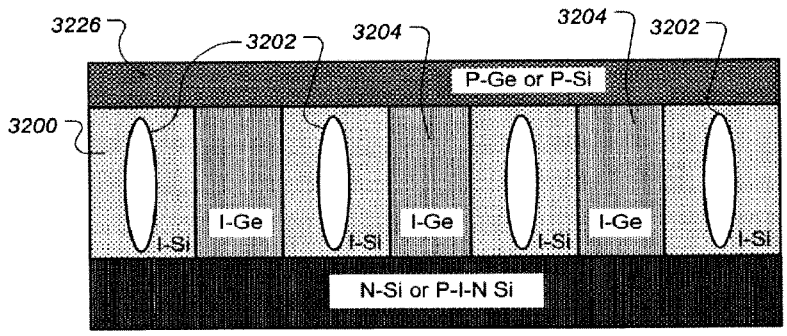

3226
3202
3204
3204
3202
P-Ge or P-Si
3200
I-Si
I-Ge
I-Si
I-Ge
I-Si
I-Ge
I-Si
N-Si or P-I-N Si

FIG. 32

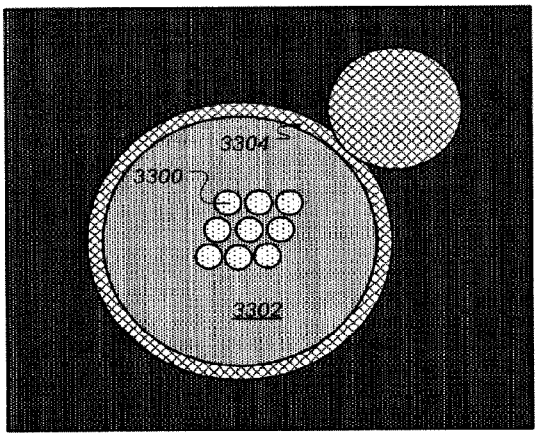

3304
3300
3302

FIG. 33

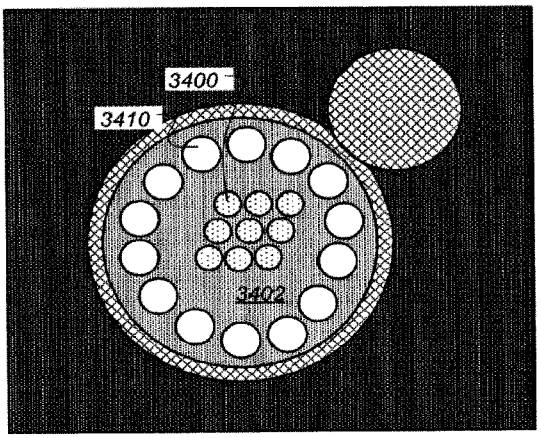


FIG. 34

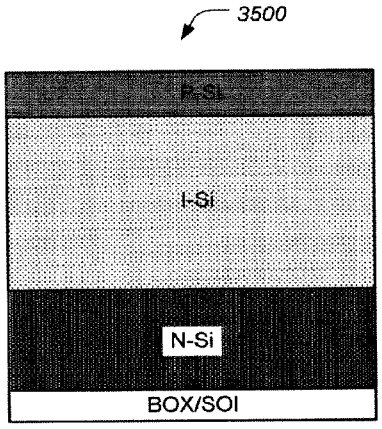


FIG. 35
(prior art)

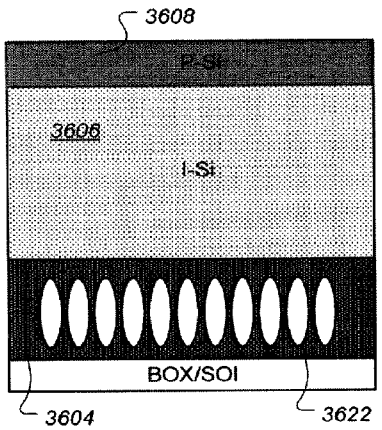


FIG. 36

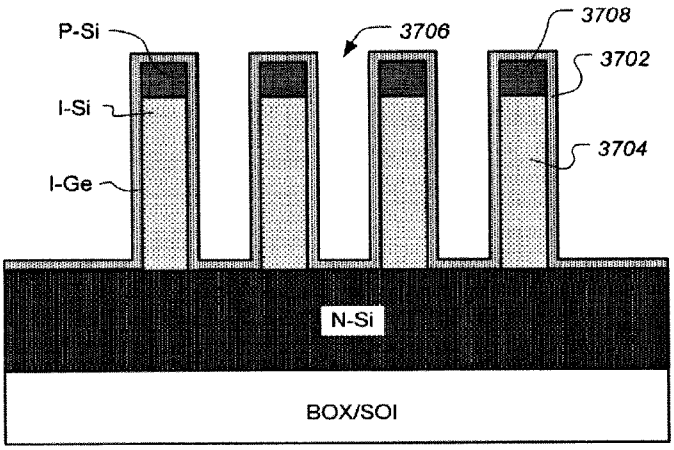

P-Si
3706
3708
3702
I-Si
3704
I-Ge
N-Si
BOX/SOI

FIG. 37

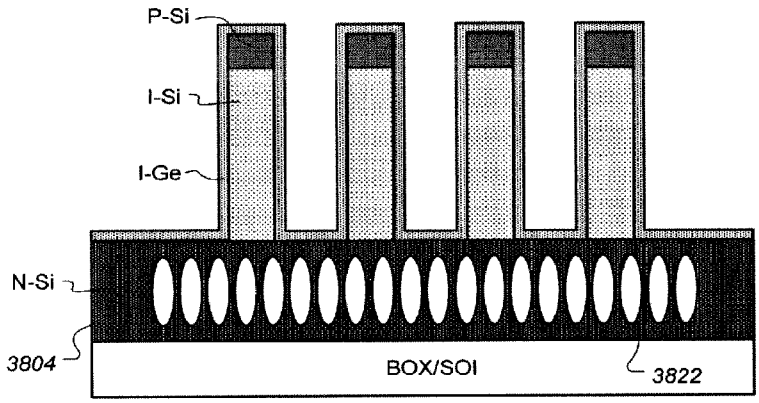

P-Si
I-Si
I-Ge
N-Si
3804
BOX/SOI
3822

FIG. 38

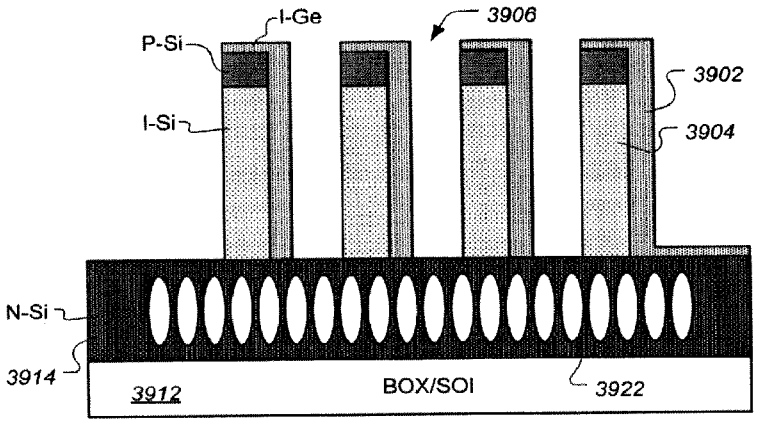

I-Ge
3906
P-Si
3902
I-Si
3904
N-Si
3914
3912
BOX/SOI
3922

FIG. 39

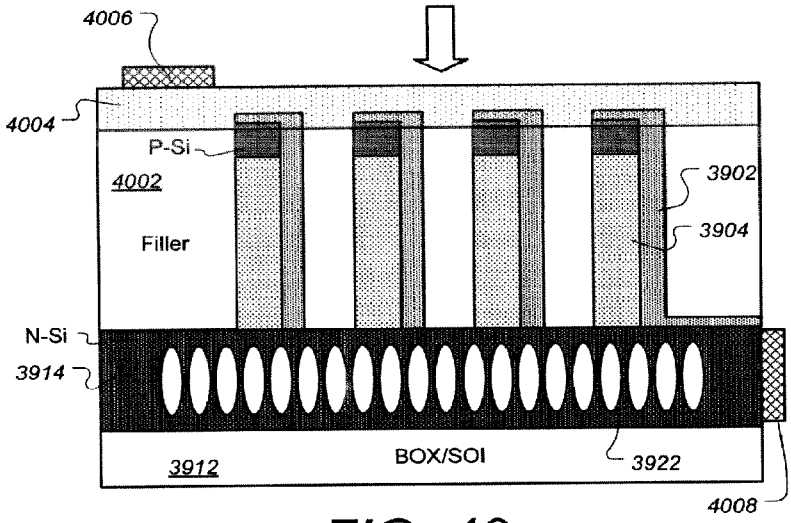

4006
4004
P-Si
4002
Filler
3902
3904
N-Si
3914
3912
BOX/SOI
3922
4008

FIG. 40

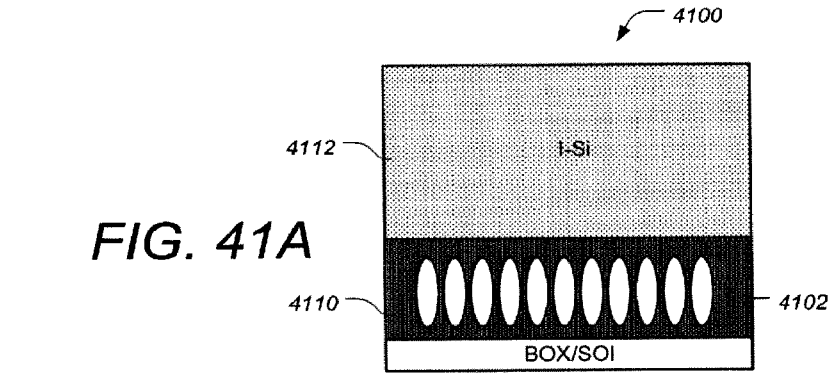


FIG. 41A

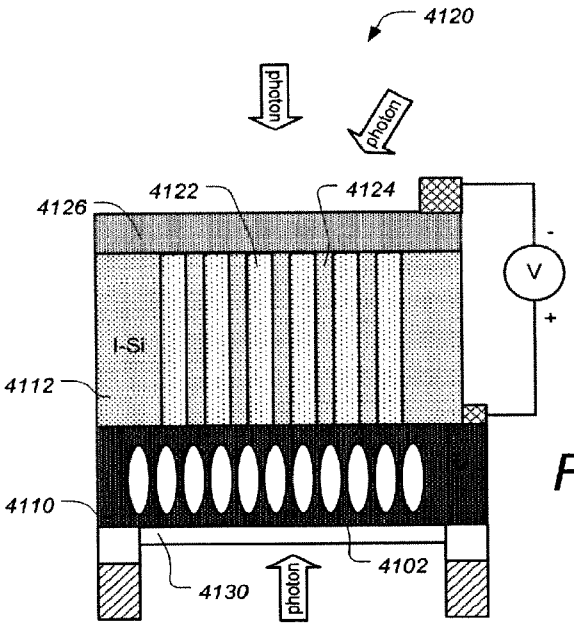
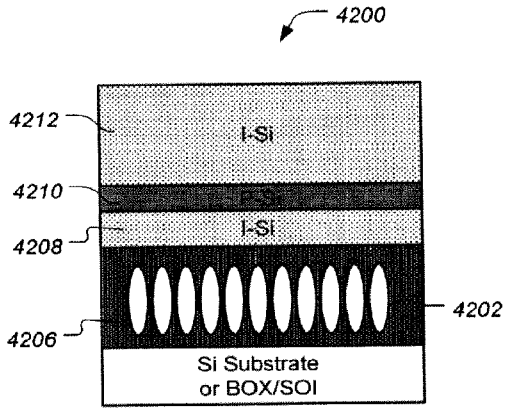


FIG. 41B

FIG. 42A



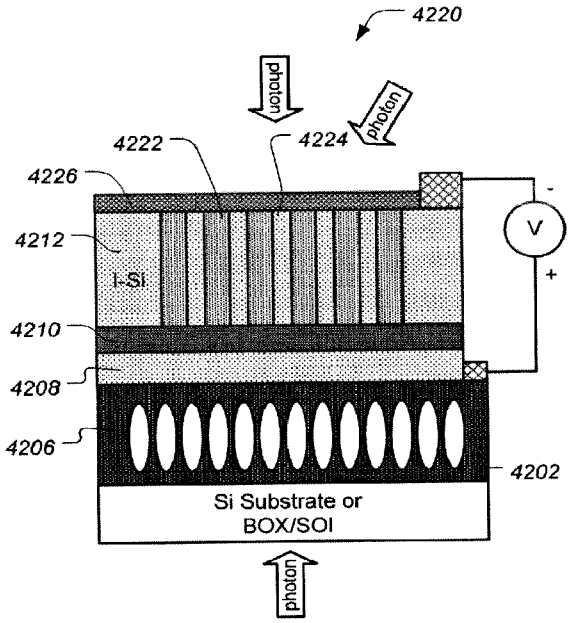


FIG. 42B

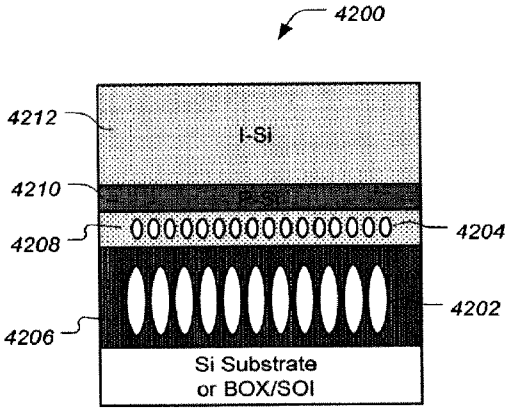


FIG. 42C

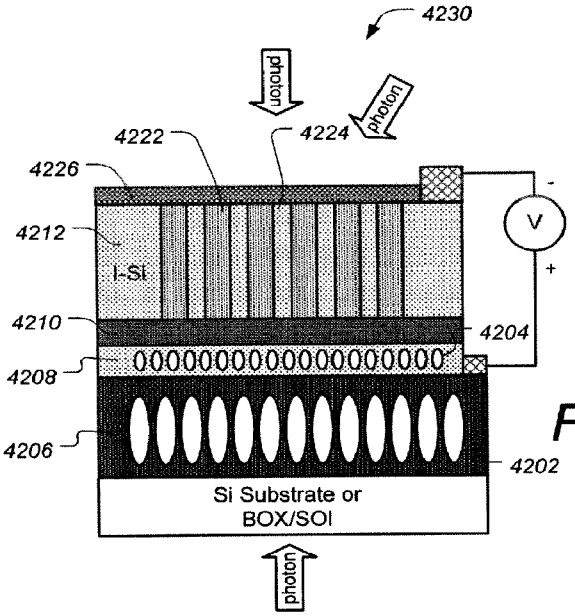


FIG. 42D

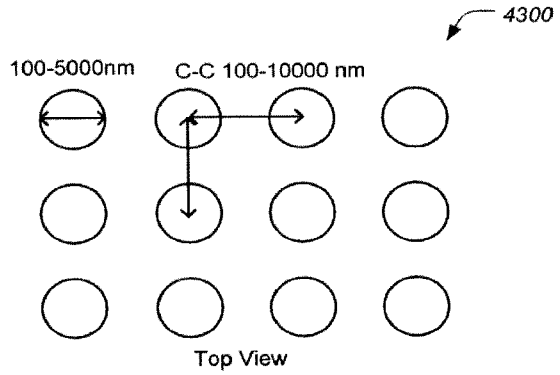

4300
100-5000nm
C-C 100-10000 nm
Top View

FIG. 43

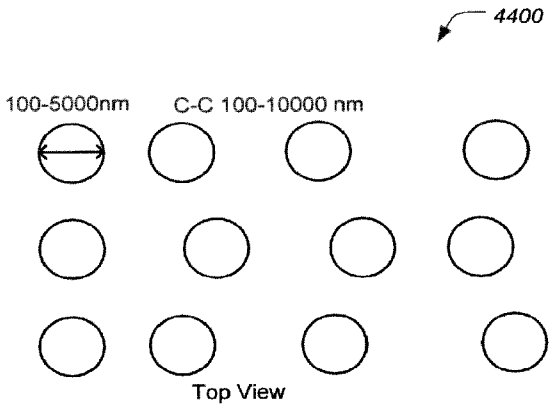

4400
100-5000nm
C-C 100-10000 nm
Top View

FIG. 44

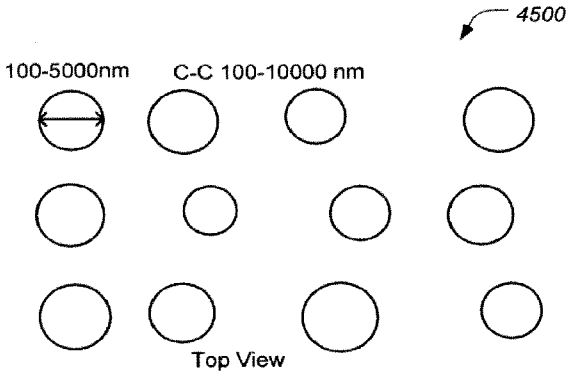

4500
100-5000nm
C-C 100-10000 nm
Top View

FIG. 45

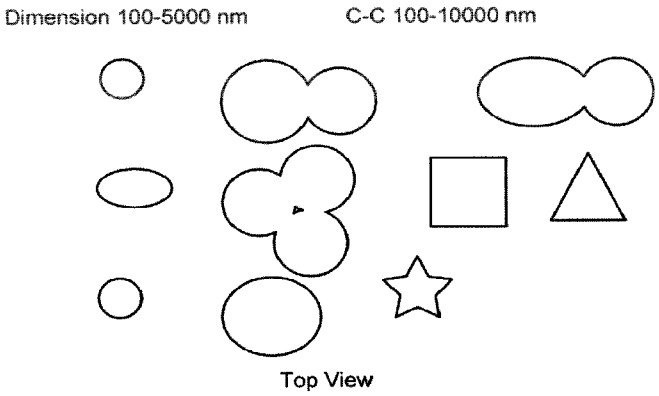

Dimension 100-5000 nm
C-C 100-10000 nm
Top View

FIG. 46

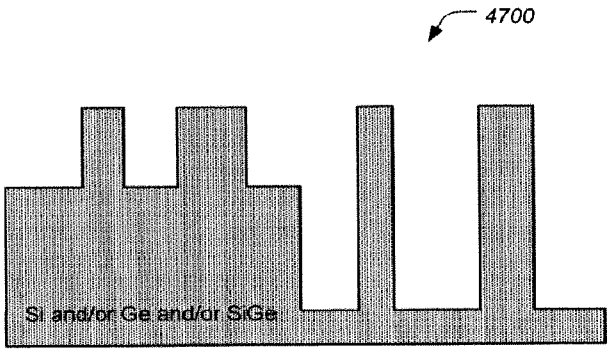


FIG. 47

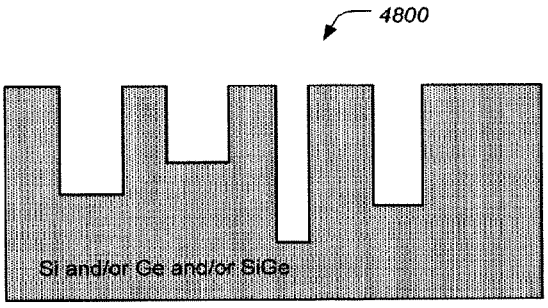


FIG. 48

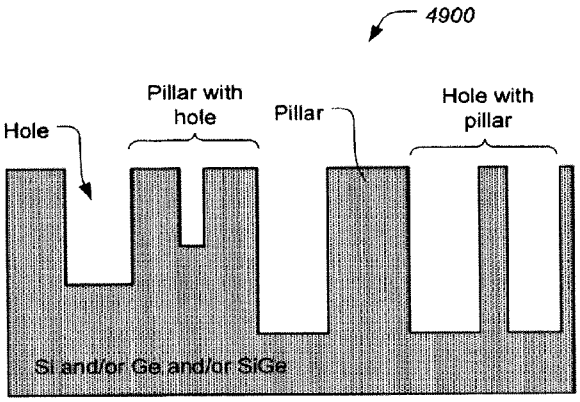

4900
Pillar with hole
Pillar
Hole with pillar
Hole
Si and/or Ge and/or SiGe

FIG. 49

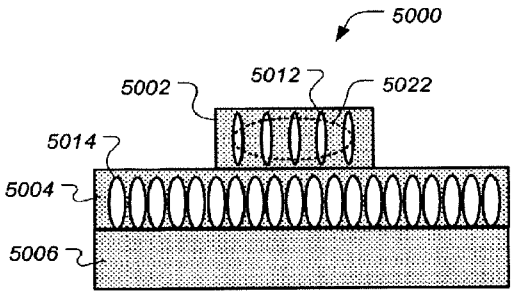

5000
5002
5012
5022
5014
5004
5006

FIG. 50

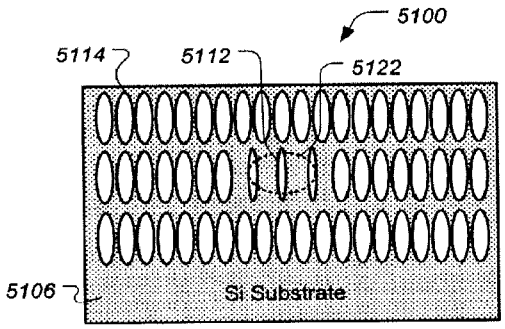

5100
5114
5112
5122
5106
Si Substrate

FIG. 51

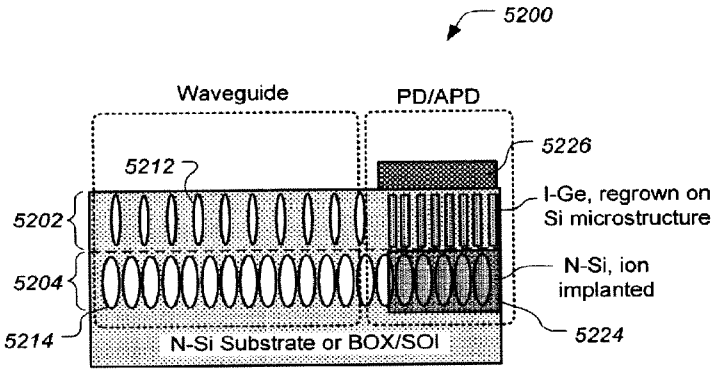

5200
Waveguide
PD/APD
5212
5226
I-Ge, regrown on
Si microstructure
5202
5204
N-Si, ion
implanted
5214
5224
N-Si Substrate or BOX/SOI

FIG. 52

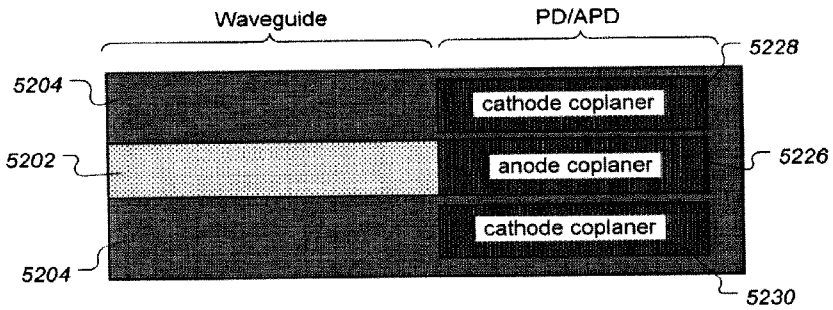


FIG. 53

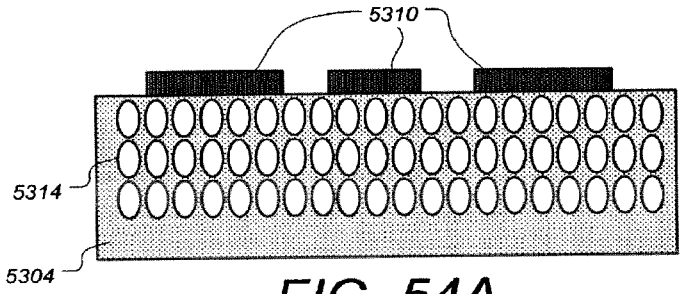


FIG. 54A

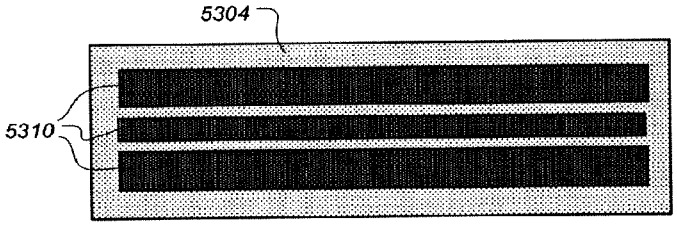


FIG. 54B

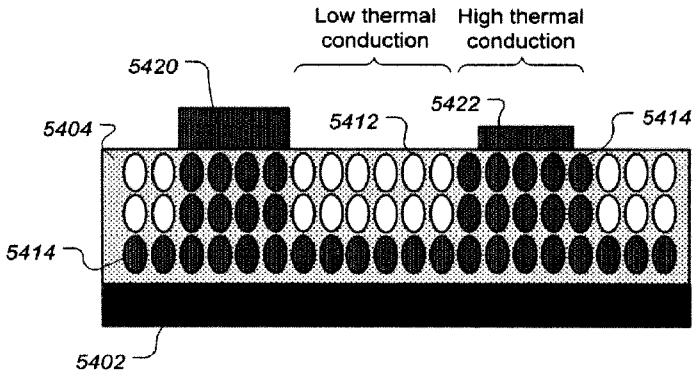

Low thermal conduction
High thermal conduction
5420
5422
5404
5412
5414
5414
5402

FIG. 55

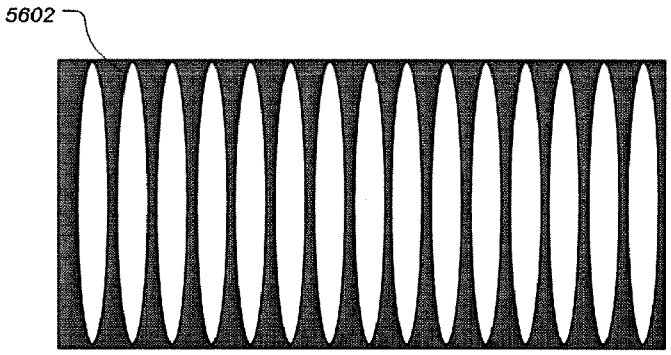

5602

FIG. 56

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(30) Priority Data:
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(75) Inventors/Applicants *(for US only)*: **CHANG-HASNAIN, Connie** [US/US]; 2925 Greer Road, Palo Alto, California 94720 (US). **ZHU, Li** [CN/US]; 1608 Delaware St., #D, Berkeley, California 94703 (US). **KARAGODSKY, Vadim** [IL/US]; 2100 Channing Way, Apt. 304, Berkeley, California 94704 (US). **YANG, Weijian** [CN/US]; 2556 Le Conte Avenue, Berkeley, California 94709 (US).

(74) Agent: **O'BANION, John**; O'BANION & RITCHEY LLP, 400 Capitol Mall, Suite 1550, Sacramento, California 95814 (US).

(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Declarations under Rule 4.17:

— *as to the applicant's entitlement to claim the priority of the earlier application (Rule 4.17(iii))*

Published:

— *without international search report and to be republished upon receipt of that report (Rule 48.2(g))*

(54) **Title**: HIGH EFFICIENCY VERTICAL OPTICAL COUPLER USING SUB-WAVELENGTH HIGH CONTRAST GRATING

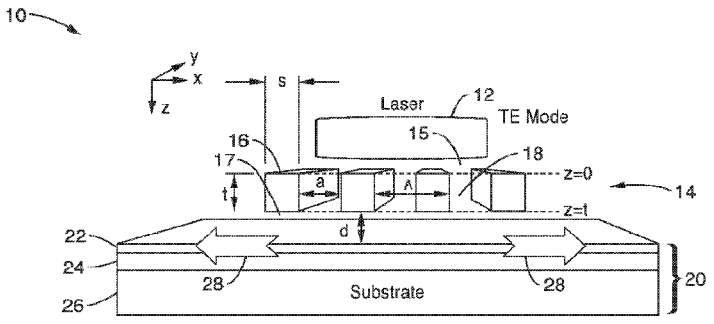


FIG. 1

(57) **Abstract**: A vertical optical coupler which redirects light transmission in response to the interaction between a sub-wavelength high contrast grating (HCG) having a plurality of spaced apart segments of grating material which is optically coupled to a wave-guide. For a selected set of material, grating geometry, gaps and spacing, the light directed at a normal incidence into the optical coupler is angularly displaced in traveling in the optical waveguide, while light directed along the optical waveguide is angularly displaced in being output at normal incidence from the optical coupler. The coupler is integrated into a number of device embodiments, including: a coupler between angularly displaced waveguides, lasers, light emitting diodes (LEDs) and solar cells.

WO 2012/149441 A2

HIGH EFFICIENCY VERTICAL OPTICAL COUPLER USING SUB-WAVELENGTH HIGH CONTRAST GRATING

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application claims priority from U.S. provisional patent application serial number 61/480,467 filed on April 29, 2011, incorporated herein by reference in its entirety.

STATEMENT REGARDING FEDERALLY SPONSORED RESEARCH OR DEVELOPMENT

[0002] This invention was made with Government support under Grant Number N00244-09-1-013 awarded by the Department of Defense (DOD) under the National Security Science and Engineering Faculty Fellowship (NSSEFF) Program. The Government has certain rights in the invention.

INCORPORATION-BY-REFERENCE OF MATERIAL SUBMITTED ON A COMPACT DISC

[0003] Not Applicable

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BACKGROUND OF THE INVENTION

[0005] 1. Field of the Invention

[0006] This invention pertains generally to optical transmission, and more particularly to an optical coupler for changing the direction of light transmission.

[0007] 2. Description of Related Art

[0008] High-density photonic integrated circuits (PICs) are important to integrate various optical functionalities in one single chip for many applications, ranging from communications, sensing, display, to system-on-a-chip and lab-on-a-chip applications. These devices, by and large, utilize light guided by waveguides in the direction parallel to the wafer surface, known as the in-plane direction. Devices are cascaded longitudinally (in the direction of light propagation) or laterally (orthogonal to light propagation) to achieve higher levels of functionalities. Various material platforms have been reported, including InP-based material, silicon and silicon-on-insulator (SOI), various organic materials, and so forth. Efficient coupling of a surface-normal propagating light beam, such as from an output of an optical fiber or free-space optics, or a device, (e.g. lasers such as vertical cavity surface emitting lasers (VCSEL)), with PICs is especially desirable.

[0009] However, conventional second order gratings have limited efficiency, often significantly below 25% in each in-plane direction. Some approaches propose adding reflection DBRs or by using slanted gratings. However, those approaches can make fabrication complicated, and perhaps too complicated for practical manufacture.

[0010] Accordingly, a need exists for an optical coupling means which can couple and redirect light at high efficiencies. The present invention fulfills that need and overcomes shortcomings of prior coupling technologies.

BRIEF SUMMARY OF THE INVENTION

[0011] A vertical optical coupler with high coupling efficiency using a sub-wavelength high contrast grating (HCG), and a number of novel device

designs into which the vertical optical coupler is integrated, are desc HCG is a single-layer sub-wavelength grating in which the grating high-index bars are completely surrounded by a low-index material. It has been demonstrated that high-Q resonances and high reflectivity can be beneficially achieved under proper design of grating dimensions. For regular grating couplers, when the period Λ is equal to wavelength, the surface normal incident light couples into the in-plane waveguide. By utilizing the resonance nature of HCG, the coupling efficiency from vertical incidence to in-plane waveguide can be increased to a total of at least 92% in both in-plane propagation directions (combined). The inventive coupler can be used in the reverse direction, with input received from an in-plane waveguide and directed to the vertical direction as well. Efficiencies of greater than 90% are achieved for both single-side incidence and double-side incidence. Various inventive devices incorporating the vertical optical coupler are presented.

[0012] Further aspects of the invention will be brought out in the following portions of the specification, wherein the detailed description is for the purpose of fully disclosing preferred embodiments of the invention without placing limitations thereon.

BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWING(S)

[0013] The invention will be more fully understood by reference to the following drawings which are for illustrative purposes only:

[0014] FIG. 1 is a schematic of a "vertical to in-plane" coupler according to an embodiment of the present invention.

[0015] FIG. 2 is a schematic of an "in-plane to vertical" coupler with symmetrical incidence according to an embodiment of the present invention.

[0016] FIG. 3 is a schematic of a single-side "in-plane to vertical" coupler according to an embodiment of the present invention.

[0017] FIG. 4A and FIG. 4B are graphs of operating modes utilized according to an embodiment of the present invention, showing first through third modes

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in FIG. 4A, and an overall mode profile at the output plane $z = t$ in FI

[0018] FIG. 5 is a graph of HCG surface normal reflectivity utilized according to an embodiment of the present invention.

[0019] FIG. 6 is a graph of a mode dispersion relationship utilized according to an embodiment of the present invention.

[0020] FIG. 7A and FIG. 7B are graphs of vertical to in-plane coupling, utilized according to an embodiment of the present invention, showing field distribution in FIG. 7A, and coupling efficiency in FIG. 7B.

[0021] FIG. 8A and FIG. 8B are graphs of coupling utilized according to an embodiment of the present invention, showing symmetrical in-plane incidence to vertical coupling field distribution in FIG. 8A, and coupling efficiency in FIG. 8B.

[0022] FIG. 9A and FIG. 9B are graphs of in-plane characteristics utilized according to an embodiment of the present invention, showing waveguide field distribution for the case of in-plane reflection in FIG. 9A, and in-plane reflectivity in FIG. 9B.

[0023] FIG. 10A through FIG. 10C are graphs of efficiency spectrum in response to different HCG thickness utilized according to an embodiment of the present invention, showing in-plane reflection (-x direction) in FIG. 10A, vertical coupling (+z direction) in FIG. 10B, and in-plane transmission (+x direction) in FIG. 10C.

[0024] FIG. 11A and FIG. 11B are graphs of single side in-plane incidence to vertical coupling field distribution in FIG. 11A, and coupling efficiency in FIG. 11B utilized according to an embodiment of the present invention.

[0025] FIG. 12 is a schematic of light being turned in a hollow-core waveguide (HW) utilizing vertical couplers according to an embodiment of the present invention.

[0026] FIG. 13 is a schematic of light being turned in a hollow-core waveguide (HW) utilizing side-coupling according to an embodiment of the present invention.

[0027] FIG. 14 is a schematic of connecting two HCG hollow core waveguide

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couplers according to an embodiment of the present invention to turr

[0028] FIG. 15 is a schematic of an HCG multiplexer according to an embodiment of the present invention.

[0029] FIG. 16 is a schematic of an HCG demultiplexer according to an embodiment of the present invention.

[0030] FIG. 17 is a schematic of vertical incidence to single side in-plane waveguide coupling according to an embodiment of the present invention.

[0031] FIG. 18 is a schematic of parallel waveguide coupling according to an embodiment of the present invention.

[0032] FIG. 19 is a schematic of an HCG vertical coupler and reflector for surface-emitting quantum cascade laser according to an embodiment of the present invention.

[0033] FIG. 20 is a schematic of an HCG reflector as cavity mirror in GaN laser diode according to an embodiment of the present invention.

[0034] FIG. 21 is a schematic of HCG light extraction for GaN light emitter diode according to an embodiment of the present invention.

[0035] FIG. 22 is a schematic of an HCG light collector for a solar cell according to an embodiment of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

[0036] **1. High Contrast Grating Vertical Coupler Structure**

[0037] FIG. 1 through FIG. 3 illustrate different operations of the inventive vertical coupler which can couple light from a vertical light source into both directions of a horizontal waveguide (FIG. 1), or from both directions of the horizontal waveguide to the vertical direction (FIG. 2), or utilize a single side operation of the vertical coupler in which light is preferentially coupled to or from one direction of the waveguide (FIG. 3). The optical coupler thus angularly displaces light transmission passing either way through the coupler. These operations of the vertical optical coupling are described in greater detail in the following sections. In one embodiment, the vertical coupler comprises a sub-wavelength high contrast grating (HCG) configured with proper grating

dimensions and spacing for interoperation with a waveguide whose characteristics match the HCG. The period of the HCG preferably should be close to, or the same as, periodicity of the field profile for a specific waveguide mode in the propagation direction (i.e., propagation constant).

[0038] In the embodiment illustrated in FIG. 1, a laser light source 12, comprising a laser (which, for example, can be a VCSEL or edge emitting laser), is shown coupled to a HCG 14, having periodic spaced apart segments of grating material 16 of width (s) and thickness (t), with a spacing 18 of distance (a) between segments and period Λ. Although the embodiments address the use of a VCSEL, it should be appreciated that a laser or edge emitting laser can be generally substituted. The HCG is positioned with a gap 15 beneath the VCSEL, and a gap 17 above the waveguide 20.

[0039] The gap size is a design parameter which can influence power coupling efficiency and its spectral width from laser into waveguide. The gap size design can be optimized by finite-difference time-domain (FDTD) simulations or numerical analysis. A typical value is in the range from 10 nm to about 1,500 nm, depending on the refractive indices of the material used for the gap and the HCG, as well as the wavelength of interest. In the range given above, there exists an optimum value range with which a high coupling efficiency and broad spectral width is achieved. As the gap increases and reduces from the optimum range, both coupling efficiency and spectral width are reduced.

[0040] In this example embodiment, waveguide 20 is shown comprising an in-plane silicon-on-insulator (SOI) waveguide having a waveguide layer 22 and buried oxide layer 24. The buried oxide layer should be sufficiently thick that the light is guided by the waveguide 22 and does not experience significant leakage into the silicon substrate. A plane wave with the E-field polarized in the y-direction (hereinafter TE polarization) propagates in the z-direction (downward) from VCSEL 12 towards HCG 14. The three physical parameters that select the characteristics of the HCG are period (Λ), thickness (t) and duty cycle (η). The period (Λ) of sub-wavelength high contrast grating should be smaller than the working wavelength while the thickness can be

larger. The duty cycle (η) is defined herein as the ratio of grating ba period (s/Λ). In this example, an in-plane SOI waveguide is utilized and placed beneath the HCG, separated by a gap 17 denoted by (d). In this example, the silicon waveguide thickness is 0.1 μm, SiO_2 layer thickness is 1.35 μm. Based on such structure, the light incidence from +z direction is coupled into the waveguide in both +x and –x directions 28 symmetrically. It is also seen in the figure that the top surface of the HCG waveguide is designated as z=0, while the bottom is at z= t.

[0041] In FIG. 2, operation of the vertical coupler is illustrated in example embodiment 30 with light symmetrically incident along the waveguide being output vertically. The sub-wavelength HCG 32 can have the same parameters as described for FIG. 1 with grating segments 32, and spacing 34, and gap 37 over the waveguide 38, such as having a waveguide layer 40 and buried oxide layer 42 and a substrate layer 44. Light 46 is shown traversing the waveguide 38 and coupled through the vertical optical coupler 32, with its interaction with the waveguide to direct the light in direction 48.

[0042] In FIG. 3, operation of the vertical coupler is illustrated in example embodiment 50 with light transmission through waveguide 64 being blocked from vertical coupler 52 for vertical output 74, by an in-plane reflector 58. The vertical coupler 52 can be configured with the same parameters as described for FIG. 1 with regard to spaced art segments of grating material 54, spacing 56, and gap 57 over the waveguide 64. The waveguide 64 is illustrates by way of example and not limitation with a waveguide layer 66, buried oxide layer 68 and a substrate layer 70. In the figure, arrow 72a depicts light input to the waveguide, with arrow 72b depicting transmission light that cannot be coupled vertically in a single pass. Arrow 72c represents the reflected light of 72b through in-plane reflector 58. The large vertical arrow 74 represents the total vertically out-coupling light. The reflector 58 also comprises segments of grating material 60, spaces 62, and is positioned with a gap 63 separating it from waveguide 64. HCG parameters for reflector 58 differ from that of the vertical optical coupler to provide efficient and broadband reflection.

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[0043] The coupler design procedure is as follows. The first step is t determine the HCG period Λ. The goal is to couple a down-propagating plane wave, with the E-field polarized in y-direction into the fundamental TE mode of the Si waveguide (E-field in the same direction). It will be appreciated that an HCG can be considered as a (short) slab waveguide array supporting modes propagating in the z-direction

[0044] FIG. 4A and FIG. 4B depict mode characteristics of a high contrast grating utilized in the vertical optical coupler. In FIG. 4A, in-plane lateral mode profiles for the first three modes of propagation are seen. Due to the large index contrast, there exists a wide wavelength range where the HCG supports exactly two propagating modes, while the third and higher modes are evanescent in z and are bound to input and output surfaces of HCG (surface modes). These first two modes propagate in the z-direction with different propagation constants, β_1 and β_2. At the input and output planes, z = 0 and z = t, respectively, the two modes are reflected not only back to themselves, but also couple into each other's reflections, resulting in a mixing of the two modes. The propagation wave-numbers adjusted for the mode cross-coupling are denoted herein as β'_1 and β'_2. Most importantly, due to the sub-wavelength period, the two modes do not couple into any diffraction order other than the fundamental one, which is a surface normal propagating plane wave.

[0045] In FIG. 4B, the net field profile at the existing planes is seen having a periodic spatial variation equal to the HCG period. The high coupling can be anticipated when this periodicity is matched to the propagation constant of the Si/SiO_2 waveguide mode, denoted as β_x since it propagates in x-direction. The first step for the vertical coupler is therefore calculating the effective index η_{eff} of Si/SiO_2 waveguide, where η_{eff} is $\beta_x\lambda_0/2\pi$ and λ_0 is the free space wavelength. This leads to the determination of the period of HCG, $\Lambda = 2\pi/\beta_x = \lambda_0/\eta_{eff}$.

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[0046] Next, HCG thickness is determined by finding the condition wl and $\beta'_2 t$ are a multiple of 2π, which is the condition in which the two modes are in resonance, whereby the field inside the grating under this condition is accordingly enhanced.

[0047] FIG. 5 depicts HCG surface normal reflectivity, indicating that for a given λ_0 and Λ, there are multiple sets of t and η pairs that satisfy this condition.

[0048] FIG. 6 depicts the dispersion relationship of one such resonance mode, in which the four sets of dotted lines represent HCG resonance modes, while the solid lines represent coupled waveguide modes. The flat solid line and lower dotted line depict the mode without coupling. The other lines illustrate the use of an air gap (d) of 0.25 μm, 0.30 μm and 0.35 μm, respectively. Toward the middle of the graph the dotted line curves are seen in order of air gap spacing, with 0.35 μm seen as the lowest dotted line, and 0.25 μm as the uppermost dotted line. On the other hand, the Si waveguide mode propagating in the x direction can be represented by a straight horizontal line in the dispersion curve. By changing the gap between HCG and Si waveguide, d, the HCG resonance mode couples with the waveguide mode, causing the crossed dispersion lines to repel against each other. The stronger the coupling is, the wider the bandgap of the forbidden zone. At the center of the forbidden zone, there is no longer allowed real values for k_z, indicating the wave is forbidden to propagate in the vertical direction and all energy is transferred to in-plane propagation.

[0049] **2. Coupler Performance**

[0050] **2.1 Vertical to In-Plane Coupler**

[0051] At the wavelength of 1.55 μm for this example embodiment, the waveguide effective index is 2.13. The HCG perturbs the effective index of the waveguide underneath to 2.14. Based on the design principle described above, the following parameters were chosen: period Λ = 0.724 μm, HCG

thickness t = 0.96 μm, duty cycle η = 0.61 and air gap thickness d μm.

[0052] FIG. 7A and FIG. 7B depict results of a finite difference time domain (FDTD) simulation performed to test the design. In FIG. 7A, the intensity distribution shows the coupling effect, in which it can be clearly seen that the field inside the waveguide under the HCG is enhanced and the surface normal incident light is coupled into the waveguide. In FIG. 7B, coupling efficiency is seen for each propagation direction as a function of wavelength. The highest coupling efficiency for this example is 46% and the coupling wavelength is 1.552 μm. Therefore, in the combination of both +x and –x directions, 92% of incident energy was coupled into the waveguide. The remaining 8% was leakage due to the limited HCG width. The 1 dB and 3dB coupling bandwidths were found to be 30 nm and 50 nm, respectfully, which is substantially wide and readily makes this device useful for WDM application. The bandwidth is determined by the band gap of the forbidden zone, which can be tuned by the spacing between the HCG and the waveguide, as was shown previously in regard to FIG. 6. Therefore, wider or narrower bandwidth can be achieved by tuning the air gap and the corresponding HCG dimension.

[0053] **2.2 Coupler from Symmetrical In-Plane Incidence to Vertical Output**

[0054] Based on reciprocity, it can be expected that the symmetrical light incidence from two sides of the waveguide can be coupled into the vertical direction with high efficiency as well, as shown in the schematic of FIG. 2.

[0055] FIG. 8A through FIG. 8D depict FDTD simulation results for coupling light from two sides of the waveguide into the vertical direction. The dimensions in this configuration are the same as the vertical to in-plane coupler. In this simulation, two mode matched light sources are positioned at the waveguide symmetrically to HCG. In FIG. 8A the field distribution is plotted in a log scale, while FIG. 8B shows the coupling efficiency with plots for –z leakage (bottom line) +x, -x leakage (trough-shaped curve), upward coupling (peaked curve), and the combination (summation). At the

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wavelength of 1.551 μm, the highest coupling efficiency is found to

The 1 dB and 3 dB bandwidths are 38 nm and 70 nm, respectively.

[0056] **2.3 Coupler from Single Side In-Plane Incidence to Vertical Output**

[0057] For the single side in-plane incidence case, previously described in FIG. 3, to prevent optical transmission passing through the waveguide, an in-plane reflector is integrated into the device. By changing the HCG thickness t with the other dimensions fixed as in the previous designs, a broad band high efficiency in-plane reflector can be designed.

[0058] FIG. 9A and FIG. 9B depict simulated waveguide field distribution and in-plane reflectivity, respectively. The field distribution of in-plane reflectivity in FIG. 9A is shown in a log scale, for a device with HCG thickness t at 0.495 μm, a period λ of 0.724 μm, and duty cycle η at 0.61. FIG. 9B depicts the reflectivity spectrum, with the highest reflectivity in this test being 97% with a bandwidth of 30 nm. It will be noted that by varying the HCG thickness in the simulation, the HCG expresses different behaviors.

[0059] FIG. 10A through FIG. 10C, respectively, depict that the light can be reflected backward in the –x direction shown in FIG. 10A, coupled upwardly in the +z direction shown in FIG. 10B, or transmitted through in the +x direction shown in FIG. 10C across a range of different HCG thicknesses, with these transformations observed with respect to grating period.

[0060] In the above example, the HCG coupler and in-plane reflector grating were selected with the same thickness, but having different periods and duty cycles. By increasing the duty cycle, the anti-crossing behavior seen in FIG. 5 can be shifted to smaller HCG thicknesses. In FIG. 5, sharp reflectivity changes indicate the resonance conditions of specific modes. At the center, two modes which are supposed to intersect with each other repel at the crossing point, and is referred to as the anti-crossing behavior. The coupler HCG of the example embodiment has a thickness of 0.495 μm, period 0.715 μm, and a duty cycle of 0.69.

[0061] FIG. 11A and FIG. 11B depict, respectively, coupling field distribution and the coupling efficiency spectrum for this configuration. The highest

coupling efficiency observed in this example embodiment was 91.7% wavelength of 1.554 μm, with the 1 dB bandwidth at 70 nm.

[0062] **3. Applications**

[0063] **3.1. Integration of Vertical Coupler with Hollow Core Waveguides**

[0064] Notwithstanding the numerous beneficial configurations described in the preceding sections, the inventive vertical optical coupler also provides wide applicability in the context of hollow-core waveguides (HWs). It will be appreciated that a wide range of applications exist for these hollow-core waveguides (HWs), including applications in gas sensing and gas-based nonlinear optics. With the elimination of core material, the problems with nonlinearity, dispersion effects and scattering losses in traditional SiO_2, Si or III-V waveguides can be drastically reduced. Utilizing chip-scale HWs opens up a new range of on-chip applications, such as optical buffers, optical signal processors, and RF filtering. Although integrated HWs can achieve a low propagation loss for the straight session, there is usually a relatively large light leakage when the waveguide bends. At the bending region, the sidewall reflection reduces, and thus large radiation losses can arise, in particular with integrated HWs. The small footprint of integrated optics requires unavoidably tight packing of the waveguides and sharp turns. This would introduce high loss as the bending loss increases exponentially with the decrease of the radius of curvature. These losses have imposed significant limitations on the application of integrated HWs. Use of the inventive vertical coupler can solve this problem by bridging two adjacent HWs without the need of a sharp bend.

[0065] FIG. 12 through FIG. 14 illustrate example embodiments utilizing vertical couplers with waveguides. The hollow core waveguides can be of any desired types, such as metal HWs, distributed Bragg reflection type HWs, anti-resonant HWs, HCG HWs, or other form of HW. These examples illustrate coupling so that the light is turned a full 180 degrees, although the teachings are applicable to turning light through other angular displacements. Because the coupler can be designed to have coupling with any angle, the stripe

waveguide 98 and HCG HWs 92 and 94 can be configured to any re angle and work with the corresponding couplers.

[0066] In the embodiment 90 of FIG. 12, two HWs are seen 92, 94 having exterior 102 surrounding an interior hollow light guide region 104. At the end of each of these HWs are vertical couplers 96a, 96b, in a butt-coupling arrangement, that are in turn interconnected with each other by a strip waveguide 98. An HCG 100a, 100b are seen in each vertical coupler upon which light has normal incidence from HWs 92, 94 to the vertical coupler. Through the vertical coupler, light can be transformed from the HWs to the stripe waveguide. The propagation direction of the light thus changes 90 degrees at each vertical coupler. The first vertical coupler 96a directs light from a first waveguide 92 into a stripe waveguide 98, while a second vertical coupler 96b transforms the light back onto the adjacent HW 94. In this case, a virtually sharp turn is made without any sharp bends. With the high efficiency of the vertical coupler, the loss for the whole transformation can be small, on the order of 10% or less.

[0067] FIG 13 illustrates an alternative HW light bending technique to the above, utilizing the vertical coupler configured in a side-coupling embodiment 110. A first waveguide 112 and second waveguide 114 are shown having an exterior 102 with hollow waveguide interior 104. The grating 118a, 118b of the vertical couplers 116a, 116b are placed on top of the waveguides 112, 114 with a stripe waveguide 120 connecting the vertical couplers. This and other embodiments of the invention may also be equally realized by replacing the stripe waveguide with other forms of waveguides, such as HCG waveguide, or hollow waveguides. With a proper design, light can be coupled upwards to the stripe waveguide, and then downwards to the adjacent HW. It should be appreciated that this configuration may be particularly well-suited to simplified fabrication processing.

[0068] FIG. 14 illustrates an embodiment 130 in which the vertical coupler is utilized with HCG HWs 132, 134, to which it may be even more beneficially coupled. It will be appreciated that HCG HWs represent another class of

hollow-core waveguide, with the HCG configured as high reflection n and light is thus confined between opposing layers 136, 137 of HCGs. This form of waveguide has an extremely low propagation loss, and lateral confinement can be achieved by choosing different periods and duty cycles for the core and cladding region. A first vertical coupler 138a with its HCG 140a is shown integrated with first HCG HW 132, with light coupled through a stripe waveguide 142 to a second vertical coupler 138b, with its HCG 140b, coupled to a second HCG waveguide 134. It will be appreciated that the HCGs at the end of the waveguide can be designed as a vertical coupler to transform the light upwards to the stripe waveguide, or downwards from the stripe waveguide. The transition between the waveguide and the coupler can be designed to be smooth, and this ensures a minimum loss. It would appear that this arrangement can provide a most beneficial combination to replace traditional lossy light bending arrangements.

[0069] **3.2. WDM Multiplexer and Demultiplexer**

[0070] FIG. 15 and FIG. 16 illustrate utilizing the inventive HCG vertical coupler for multiplexing and demultiplexing in a WDM system. In the multiplexer embodiment 150 of FIG. 15, outputs from a plurality of VCSELs 152a, 152b and 152c with different wavelengths (λ_1, λ_2, λ_3) are coupled through the inventive vertical optical coupling into a waveguide 162. It will be appreciated that the multiplexor and the demultiplexer of these figures are shown having three inputs / outputs, for the sake of simplicity of illustration, however, the technique can be utilized with any desired number of inputs / outputs, respectively. It should also be appreciated that each vertical coupler is configured for its particular working wavelength, and that by optimizing HCG parameters, the crosstalk arising between different wavelengths can be essentially eliminated.

[0071] It will be seen from the figure that inputs 152a, 152b, 152c are directed through gap 154a, 154b, 154c to an HCG 156a, 156b, 156c, containing segments 158a, 158b, and 158c along with spaces 159a, 159b, 159c. Vertical coupling between HCG 156a, 156b, 156c is through gap 160a, 160b, 160c

with a waveguide 162 having a waveguide layer 164, a buried oxide and a substrate layer 168. It should be appreciated that waveguide 162, and other waveguides within the optical coupler, may comprise any desired forms of waveguides. It can be seen from the figure that the light received at λ_1 is dispersed in both directions 170a of the waveguide 162, while similarly light received at λ_2 is dispersed in both directions 170b, and light received at λ_3 is also dispersed in both directions 170c.

[0072] FIG. 16 illustrates a demultiplexer embodiment 190 configured for demultiplexing a plurality of wavelengths from a common waveguide. It will be noted that because of the reciprocity principle, the demultiplexer can have the same dimensions as the multiplexer described in FIG. 15. Based on the simulation results, the phase difference of the input light at each side of the coupler is optimally an integer multiple of 2π, which can be readily satisfied in response to tuning the distance between the couplers. By way of example and not limitation, a set of typical dimensions for multiplexing of a 1.55 μm and 1.3 μm wavelength input. For a 1.55 μm coupler, HCG thickness is 0.7 μm, duty cycle η is 0.6, period λ is 0.744 μm; while for a 1.3 μm coupler, thickness is 0.84 μm, duty cycle η is 0.635, period λ is 0.581 μm.

[0073] In the demultiplexer embodiment 190, wavelengths 206a, 206b, and 206c of light along waveguide 198 having a waveguide layer 200, an insulating layer 202 and a substrate layer 204, are vertically coupled to HCG 192a, 192b, 192c having segments of grating material 194a, 194b, 194c and spaces 195a, 195b, 195c, over gap 196a, 196b, 196c, whereby in response to vertical optical coupling operation the three wavelengths (λ_1, λ_2, λ_3) are output vertically. It will be noted that the HCG elements are configured to be frequency selective and thus perform demultiplexing of signals from the waveguide.

[0074] It should be appreciated that the waveguide can be coupled to any desired optical elements, such as optical fiber ports or other optical devices without limitation. In particular, in the case of a multiplexer, the various

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wavelengths coupled into the waveguide can be passed to an optica wherein they are coupled for communication over an optical fiber.

[0075] 3.3. Vertical to Single Side Coupler

[0076] The phases of HCG modes are significantly influenced by high index material width. By chirping the grating, that is by changing the periodicity of the grating, the coupling from surface normal incidence can have a directional preference to the in-plane waveguide.

[0077] FIG. 17 illustrates a vertical to single side coupling embodiment 210 utilizing a chirped grating. Light can be directed from a laser light source 212, depicted as VCSEL, through gap 218 to an HCG 214, having segments of grating material 216 of different widths and / or spacing 217, and coupled through gap 220 to a waveguide 222 having a waveguide layer 224, an insulating layer 226 and a substrate layer 228. It can be seen in the figure that the light 230 from the light source, VCSEL 212, is shown traversing the waveguide in a single direction 230 in response to the chirp of the HCG whose grating bar width (s) and gap width (a) are chirped in the x direction to give a phase preference in that direction, thus providing a selection of coupling direction.

[0078] 3.4. Parallel Waveguide Coupler

[0079] FIG. 18 illustrates an embodiment 250 of utilizing an HCG coupler to couple the light wave between two parallel waveguides. The HCG coupler 256 is located between two parallel waveguides 252, 264. Light from the input waveguide 252 along a first direction 254 is coupled through HCG 256 through gaps 260, 262 to waveguide 264 wherefrom light continues traveling along in a second direction 266 parallel to said first direction 254.

[0080] 3.5. Reflector and Coupler for Surface-Emitting Lasers with In-Plane Waveguide and Active Region

[0081] An HCG vertical coupler and reflector can also be utilized in fabricating in-plane lasers emitting in the surface-normal direction. This is particularly useful for devices where mirrors are hard to construct (e.g., such as due to lack of suitable material or processing techniques) and / or surface emission is

desirable for two-dimensional integration and on-wafer testing. One is quantum cascade lasers (QCL) and a second example may be GaN or ZnO2 based devices.

[0082] FIG. 19 illustrates an example surface-emitting QCL structure embodiment 270. HCG reflectors are shown 272a, 272c, having segments of grating material 274a, 274c, and spaces 276a, 276c, and located at two ends of waveguide 280 comprising a waveguide layer 282, insulating layer 284 and substrate layer 286, act as cavity mirrors with spacing 278a, 278c over waveguide 280. An HCG vertical coupler 272b having segments of grating material 274b and spaces 276b disposed over gap 278b from waveguide 280, is upon the active waveguide region to provide the vertical emitting 289 from the combination of light waves 288a, 288b. Similar to the structure in previous sections, the reflector and coupler can have identical thickness. In this case, a monolayer HCG can solve both vertical emitting and cavity reflection issues.

[0083] FIG. 20 illustrates the utilization of the HCG reflector within a GaN laser, exemplified by a GaN laser embodiment 290. GaN material system based laser diodes are of particular interest in recent times because of their short wavelength outputs. However, the etching of GaN facets always poses a difficulty. The implementation of the HCG reflector in a GaN laser structure provide a beneficial alternative to fabrication of the facets. The GaN laser is exemplified as having an n-electrode 292 beneath substrate 294, such as of sapphire or GaN material. Over the substrate is an n-GaN layer 296, an n-AlGaN layer 298, another n-GaN layer 300, an In-GaN layer 302, a quantum structure layer 304, such as comprising a multiple quantum well (MQW) layer, of InGaN/AlGaN within an active region, another In-GaN layer 306, a p-AlGaN layer 308 and a p-GaN layer 310. It should be appreciated that the active region may comprise quantum wells, quantum wires, quantum dots, either separately or in combination, or even a bulk region.

[0084] At the upper portion of the device there is stopper layers (SLs) 312 of AlGaN/p-GaN. Shoulders of SiO_2 in layer 314 flank a vertical portion of layer 312 of AlGaN/p-GaN, which is capped with a layer of p-GaN 316. An HCG

318 is integrated on the flanks of the vertical portions of layer 312 wi segments 320 within a p-electrode layer 322. It will be appreciated that HCGs 318 are sitting at two edges of the laser diode acting as the reflector of the GaN laser cavity, while SiO_2 layer 314 is the low index gap between HCG and the semiconductor in the cavity. The HCG reflectors 318 are incorporated within the laser heterostructure to confine the light mode in the active region between the two HCG reflectors, so that device edges do not require special treatments, such as etching and reflective coating. If surface-normal emission is desirable, a vertical output coupler can also be made on the laser, similar to that of FIG. 18.

[0085] **3.6. LED Coupling**

[0086] FIG. 21 illustrates an example embodiment 330 of a GaN light emitting diode incorporating an HCG vertical coupler on the active region. The light extraction efficiency for GaN based light emitting diodes has been an ongoing obstacle to the advance of LED efficiency, which without special treatment is only around 4%. One method to improving this light extraction efficiency is to roughen the emitting surface. However, utilizing the present invention optical coupling light extraction efficiency is dramatically increased.

[0087] The example LED embodiment 330 is shown fabricated with a metal base 332, upon which is an n-electrode layer 334, a layer of n-GaN 336, above which is an active region of InGaN 338 followed by a layer of p-GaN 340, a layer of SiO_2 342, above which is an HCG layer 344 having grating segments 346 and spaces 347, and a p-electrode 348 disposed centrally. It is preferable that the central p-electrode be of a heavily doped material to inject the current. It goes through SiO_2 layer 342 and connect to p-GaN layer 340. It should also be noted that the shape depicted in the top plane view of FIG. 21 is not necessarily constricted, but is dependent on how the LED is designed. Typically, the shape of the p-electrode is as a circle or a ring. It will be appreciated that the above describes an improvement to conventional GaN diodes, whose operating principles need not be discussed in detail as they are well known in the art.

[0088] **3.7. Solar Cells**

[0089] FIG. 22 illustrates an example solar cell embodiment 350, incorporating an HCG vertical coupler 352 with respect to a solar cell instead of a waveguide. The HCG 352 comprises segments of grating material 354 and spaces 355, positioned with a gap 356 over a solar cell 358 acting as a light collector, and shown comprising a p-n junction layers 360, 362 on a substrate 364. The incorporation of the HCG vertical coupler increases solar cell efficiency by reducing light reflection, because of the resonant nature of HCG in this configuration the light can be confined in the active region and therefore help to enhance efficiency

[0090] **3.9. Use of Different Materials**

[0091] The material requirement for an HCG coupler and reflector are readily achieved using a wide range of materials, as any material combinations can be utilized in which the refractive index of the grating materials have a high contrast with refractive index of the surrounding materials. The larger the contrast, the better the performance (bandwidth, coupling efficiency, and so forth) of the HCG coupler and reflector. Some possible materials include Si, Ge, GaAs, InAs, AlSb, InP, AlGaInP, InGaAs, AlGaAs, AlAs, CaSe, ZnSe, GaSb, AlSb, GaN, and similar dielectric materials.

[0092] From the discussion above it will be appreciated that the invention can be embodied in various ways, including the following:

[0093] 1. An apparatus for optical coupling, comprising: a sub-wavelength high contrast grating (HCG) having a plurality of separate spaced apart segments of material with a gap between adjacent segments; and an optical waveguide proximally coupled through a selected gap to said sub-wavelength high contrast grating (HCG); wherein light is coupled between normal incidence on said sub-wavelength high contrast grating (HCG) and transmission through said optical waveguide.

[0094] 2. The embodiment of claim 1, wherein said spaced apart segments of material of said high contrast grating (HCG) comprise a high refractive index material surrounded by low index material.

[0095] 3. The embodiment of claim 1, wherein the index of refractior high index material and the index of refraction of said low index material have a differential that is greater than one unit.

[0096] 4. The embodiment of claim 1, wherein said spaced apart segments of material comprising said high contrast grating have a width (s), thickness (t), a spacing (a) between segments, and a period Λ.

[0097] 5. The embodiment of claim 1, wherein said optical waveguide comprises a slab waveguide, HCG, or hollow-core waveguides (HW).

[0098] 6. The embodiment of claim 1, wherein said sub-wavelength high contrast grating (HCG) can be chirped to support asymmetrical waveguide transmission.

[0099] 7. The embodiment of claim 1, further comprising an in-plane reflector for preventing transmission along selected directions of angular displacement of said light.

[00100] 8. The embodiment of claim 1, wherein said optical coupler comprises a multiplexer or demultiplexer for coupling, through an angular displacement, a number of wavelengths of light between a normal incident direction to said HCG and transmission through said waveguide.

[00101] 9. The embodiment of claim 1, wherein said apparatus comprises materials selected from the group of materials consisting of Si, Ge, GaAs, InAs, InAlGaAs, AlAs, AlSb, GaSb, GaAlSb, InP, AlGaInP, InGaAlAs, CdSe, ZnSe, CdSSe, InAlGaN, InN, AlN, GaN, ZnO2, and SiN.

[00102] 10. The embodiment of claim 1, wherein said optical coupling is integrated within the surface of a light emitting diode to transfer light reaching the waveguide along the surface to a vertical output.

[00103] 11. The embodiment of claim 1, wherein said optical coupling is integrated within the surface of a solar cell to transfer light impinging on the surface into the p-n junction taking the place of a waveguide along said surface.

[00104] 12. An apparatus for optical coupling, comprising: a sub-wavelength high contrast grating (HCG) having a plurality of separate spaced apart

segments of material with a gap between adjacent segments; where spaced apart segments of material comprise a high refractive index material surrounded by low index material;wherein the index of refraction of said high index material and the index of refraction of said low index material have a differential that is greater than one unit; and an optical waveguide proximally coupled through a selected gap to said sub-wavelength high contrast grating (HCG); wherein light is coupled between normal incidence on said sub-wavelength high contrast grating (HCG) and transmission through said optical waveguide

[00105] 13. The embodiment of claim 12, wherein said waveguide comprises a slab waveguide, HCG, or hollow-core waveguides (HW).

[00106] 14. The embodiment of claim 12, wherein said sub-wavelength high contrast grating (HCG) of said optical coupler can be chirped to support asymmetrical waveguide transmission.

[00107] 15. The embodiment of claim 12, further comprising an in-plane reflector for preventing transmission along selected directions of angular displacement of said light.

[00108] 16. The embodiment of claim 12, wherein said apparatus comprises materials selected from the group of materials consisting of Si, Ge, GaAs, InAs, InAlGaAs, AlAs, AlSb, GaSb, GaAlSb, InP, AlGaInP, InGaAlAs, CdSe, ZnSe, CdSSe, InAlGaN, InN, AlN, GaN, ZnO2, and SiN.

[00109] 17. An apparatus for multiplexing or demultiplexing optical signals, comprising: a plurality of sub-wavelength high contrast gratings (HCGs), each having a plurality of separate spaced apart segments of material with a gap between adjacent segments; and an optical waveguide proximally coupled through a selected gap to said plurality of sub-wavelength high contrast gratings (HCGs); wherein light received by each of said sub-wavelength high contrast gratings (HCGs) is multiplexed onto said optical waveguide; and wherein light received by said optical waveguide is demultiplexed through said plurality of sub-wavelength high contrast gratings (HCGs) which contain sub-wavelength high contrast gratings (HCGs) that are adapted to pass different

wavelengths of said light.

[00110] 18. A surface-emitting quantum cascade laser apparatus, comprising: an active region having quantum wells; a reflector on either side of said active region; and at least two reflective sub-wavelength high contrast gratings (HCGs) near an output the surface-emitting laser to confine the light mode in an active region of the laser between two HCG reflectors.

[00111] 19. A light emitting diode apparatus, comprising: an n-electrode region; a p-electrode region; an active region disposed between said n-electrode region and said p-electrode region; and an optical coupler disposed on an output of said light emitting diode and comprising a waveguide layer for collecting light in a horizontal plane and coupled with a sub-wavelength high-contrast grating for redirecting collected light for output in a vertical direction.

[00112] 20. A solar cell apparatus, comprising: a sub-wavelength high contrast grating (HCG) having a plurality of separate spaced apart segments of material; and a solar cell having layers of a p-n junction upon which light from said HCG is directed and converted to electrical energy.

[00113] Although the description above contains many details, these should not be construed as limiting the scope of the invention but as merely providing illustrations of some of the presently preferred embodiments of this invention. Therefore, it will be appreciated that the scope of the present invention fully encompasses other embodiments which may become obvious to those skilled in the art, and that the scope of the present invention is accordingly to be limited by nothing other than the appended claims, in which reference to an element in the singular is not intended to mean "one and only one" unless explicitly so stated, but rather "one or more." All structural, chemical, and functional equivalents to the elements of the above-described preferred embodiment that are known to those of ordinary skill in the art are expressly incorporated herein by reference and are intended to be encompassed by the present claims. Moreover, it is not necessary for a device or method to address each and every problem sought to be solved by the present invention, for it to be encompassed by the present claims. Furthermore, no element,

component, or method step in the present disclosure is intended to b dedicated to the public regardless of whether the element, component, or method step is explicitly recited in the claims. No claim element herein is to be construed under the provisions of 35 U.S.C. 112, sixth paragraph, unless the element is expressly recited using the phrase "means for."

CLAIMS

What is claimed is:

1. An apparatus for optical coupling, comprising:

a sub-wavelength high contrast grating (HCG) having a plurality of separate spaced apart segments of material with a gap between adjacent segments; and

an optical waveguide proximally coupled through a selected gap to said sub-wavelength high contrast grating (HCG);

wherein light is coupled between normal incidence on said sub-wavelength high contrast grating (HCG) and transmission through said optical waveguide.

2. The apparatus recited in claim 1, wherein said spaced apart segments of material of said high contrast grating (HCG) comprise a high refractive index material surrounded by low index material.

3. The apparatus recited in claim 1, wherein the index of refraction of said high index material and the index of refraction of said low index material have a differential that is greater than one unit.

4. The apparatus recited in claim 1, wherein said spaced apart segments of material comprising said high contrast grating have a width (s), thickness (t), a spacing (a) between segments, and a period Λ.

5. The apparatus recited in claim 1, wherein said optical waveguide comprises a slab waveguide, HCG, or hollow-core waveguides (HW).

6. The apparatus recited in claim 1, wherein said sub-wavelength high contrast grating (HCG) can be chirped to support asymmetrical waveguide transmission.

7. The apparatus recited in claim 1, further comprising an in-plar reflector for preventing transmission along selected directions of angular displacement of said light.

8. The apparatus recited in claim 1, wherein said optical coupler comprises a multiplexer or demultiplexer for coupling, through an angular displacement, a number of wavelengths of light between a normal incident direction to said HCG and transmission through said waveguide.

9. The apparatus recited in claim 1, wherein said apparatus comprises materials selected from the group of materials consisting of Si, Ge, GaAs, InAs, InAlGaAs, AlAs, AlSb, GaSb, GaAlSb, InP, AlGaInP, InGaAlAs, CdSe, ZnSe, CdSSe, InAlGaN, InN, AlN, GaN, ZnO2, and SiN.

10. The apparatus recited in claim 1, wherein said optical coupling is integrated within the surface of a light emitting diode to transfer light reaching the waveguide along the surface to a vertical output.

11. The apparatus recited in claim 1, wherein said optical coupling is integrated within the surface of a solar cell to transfer light impinging on the surface into the p-n junction taking the place of a waveguide along said surface.

12. An apparatus for optical coupling, comprising:

a sub-wavelength high contrast grating (HCG) having a plurality of separate spaced apart segments of material with a gap between adjacent segments;

wherein said spaced apart segments of material comprise a high refractive index material surrounded by low index material;

wherein the index of refraction of said high index material and the index of refraction of said low index material have a differential that is greater than one unit; and

an optical waveguide proximally coupled through a selected gap to said sub-

wavelength high contrast grating (HCG);

wherein light is coupled between normal incidence on said sub-wavelength high contrast grating (HCG) and transmission through said optical waveguide

13. The apparatus recited in claim 12, wherein said waveguide comprises a slab waveguide, HCG, or hollow-core waveguides (HW).

14. The apparatus recited in claim 12, wherein said sub-wavelength high contrast grating (HCG) of said optical coupler can be chirped to support asymmetrical waveguide transmission.

15. The apparatus recited in claim 12, further comprising an in-plane reflector for preventing transmission along selected directions of angular displacement of said light.

16. The apparatus recited in claim 12, wherein said apparatus comprises materials selected from the group of materials consisting of Si, Ge, GaAs, InAs, InAlGaAs, AlAs, AlSb, GaSb, GaAlSb, InP, AlGaInP, InGaAlAs, CdSe, ZnSe, CdSSe, InAlGaN, InN, AlN, GaN, ZnO2, and SiN.

17. An apparatus for multiplexing or demultiplexing optical signals, comprising:

a plurality of sub-wavelength high contrast gratings (HCGs), each having a plurality of separate spaced apart segments of material with a gap between adjacent segments; and

an optical waveguide proximally coupled through a selected gap to said plurality of sub-wavelength high contrast gratings (HCGs);

wherein light received by each of said sub-wavelength high contrast gratings (HCGs) is multiplexed onto said optical waveguide; and

wherein light received by said optical waveguide is demultiplexed through said plurality of sub-wavelength high contrast gratings (HCGs) which contain sub-

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wavelength high contrast gratings (HCGs) that are adapted to pass differen wavelengths of said light.

18. A surface-emitting quantum cascade laser apparatus, comprising:

an active region having quantum wells;

a reflector on either side of said active region; and

at least two reflective sub-wavelength high contrast gratings (HCGs) near an output the surface-emitting laser to confine the light mode in an active region of the laser between two HCG reflectors.

19. A light emitting diode apparatus, comprising:

an n-electrode region;

a p-electrode region;

an active region disposed between said n-electrode region and said p-electrode region; and

an optical coupler disposed on an output of said light emitting diode and comprising a waveguide layer for collecting light in a horizontal plane and coupled with a sub-wavelength high-contrast grating for redirecting collected light for output in a vertical direction.

20. A solar cell apparatus, comprising:

a sub-wavelength high contrast grating (HCG) having a plurality of separate spaced apart segments of material; and

a solar cell having layers of a p-n junction upon which light from said HCG is directed and converted to electrical energy.

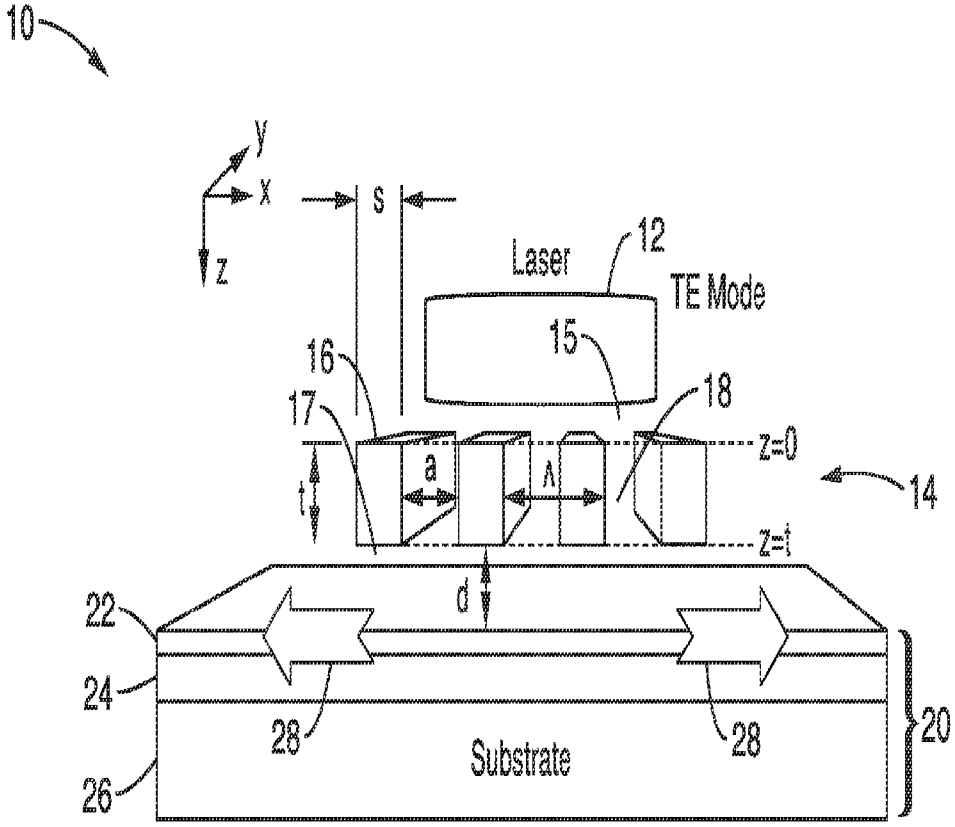

10
y
x
z
s
Laser
12
TE Mode
15
16
17
18
z=0
14
a
Λ
t
z=t
d
22
24
26
28
28
Substrate
20

FIG. 1

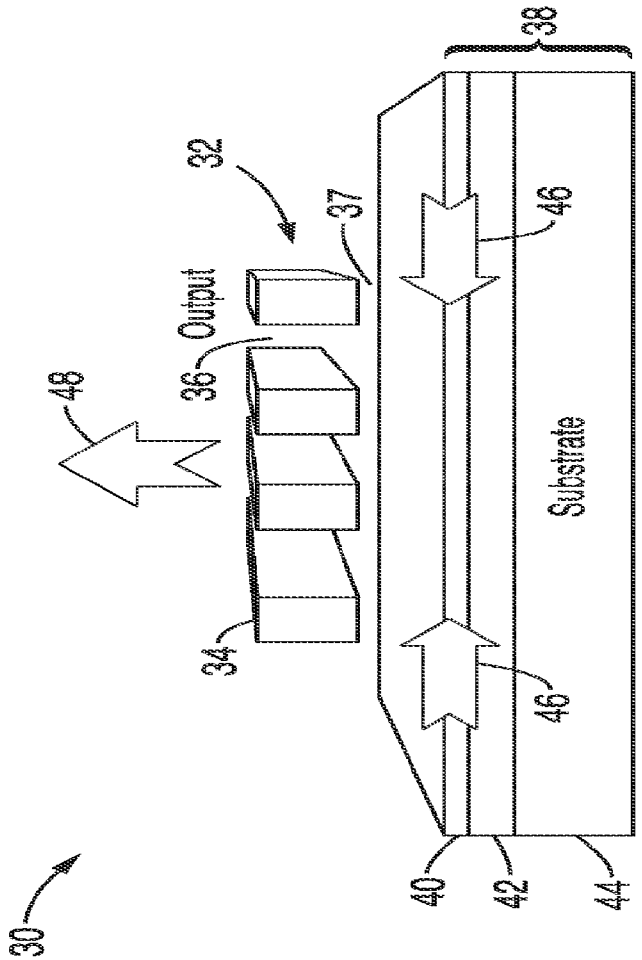


FIG. 2

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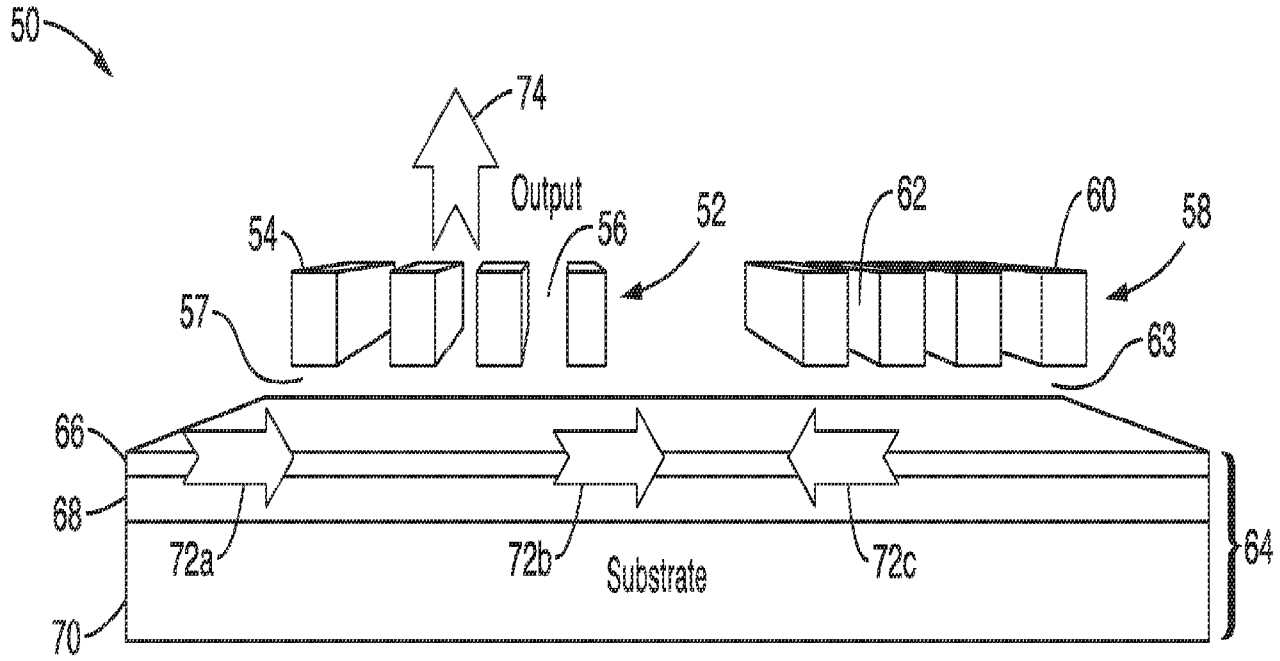

50
74
Output
54
56
52
62
60
58
57
63
66
68
72a
72b
Substrate
72c
64
70

FIG. 3

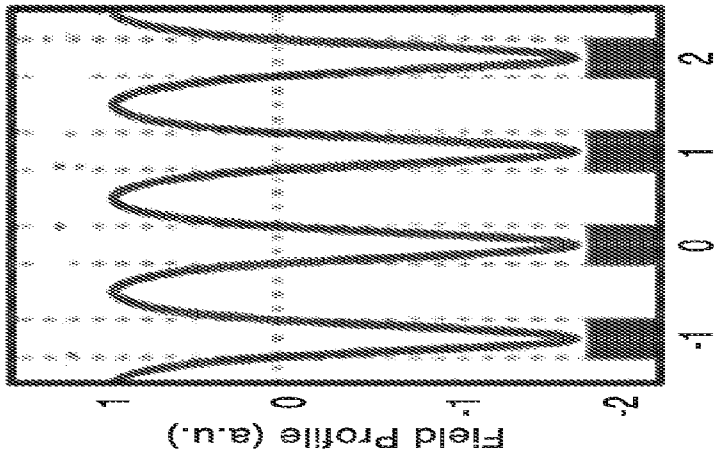


FIG. 4B

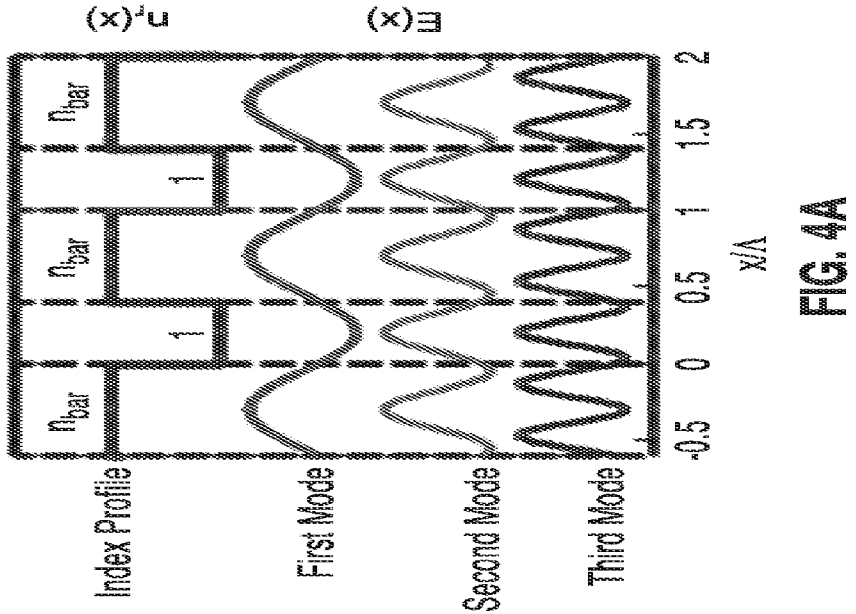


FIG. 4A

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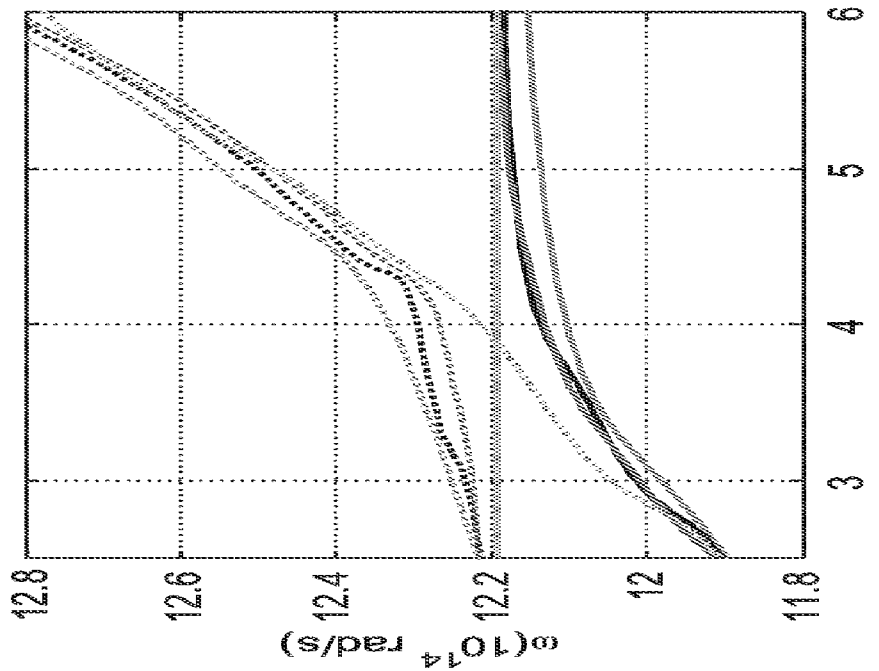


FIG. 6

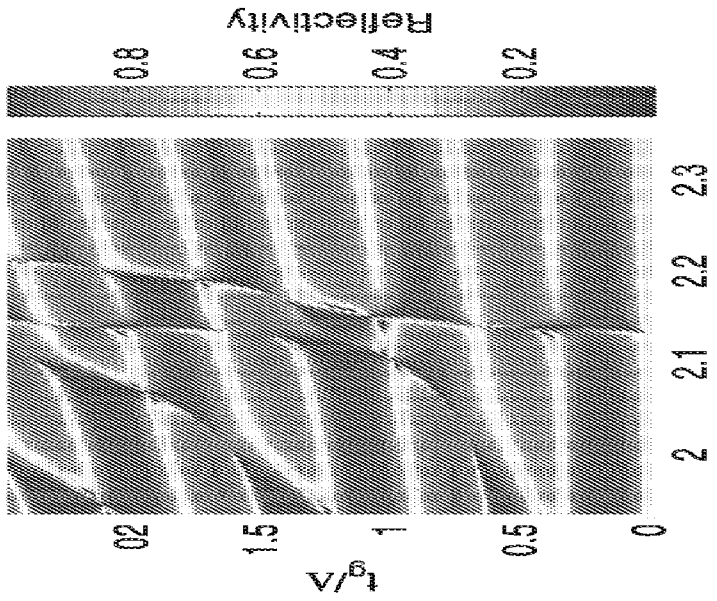


FIG. 5

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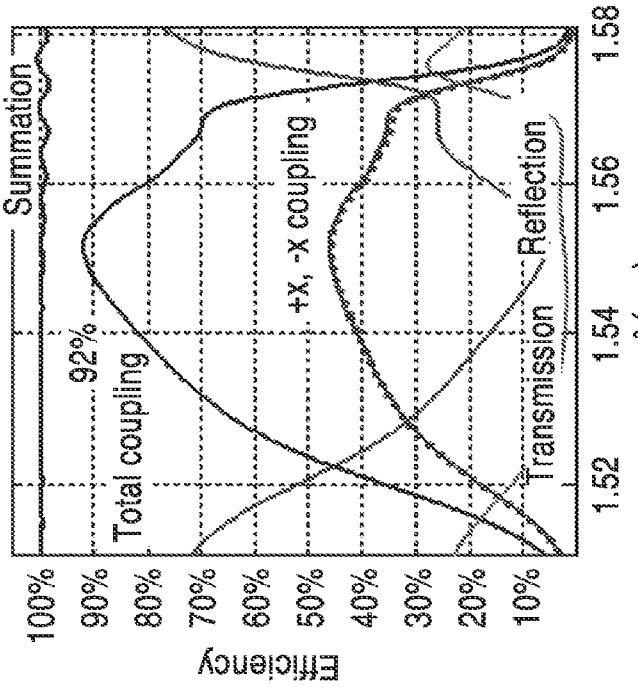

Summation
92%
Total coupling
+x, -x coupling
Reflection
Transmission
Efficiency
100%
90%
80%
70%
60%
50%
40%
30%
20%
10%
1.52
1.54
1.56
1.58
λ(μm)

FIG. 7B

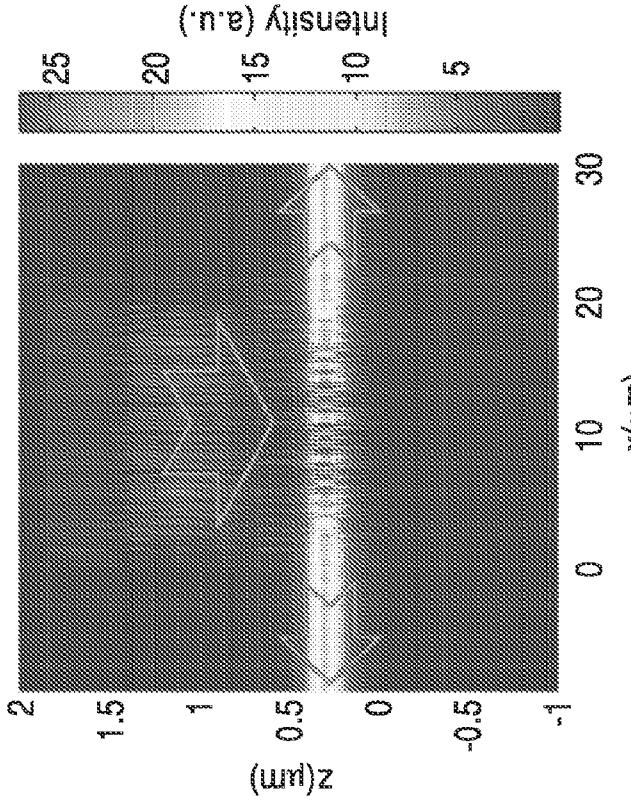

Intensity (a.u.)
25
20
15
10
5
z(μm)
2
1.5
1
0.5
0
-0.5
-1
0
10
20
30
x(μm)

FIG. 7A

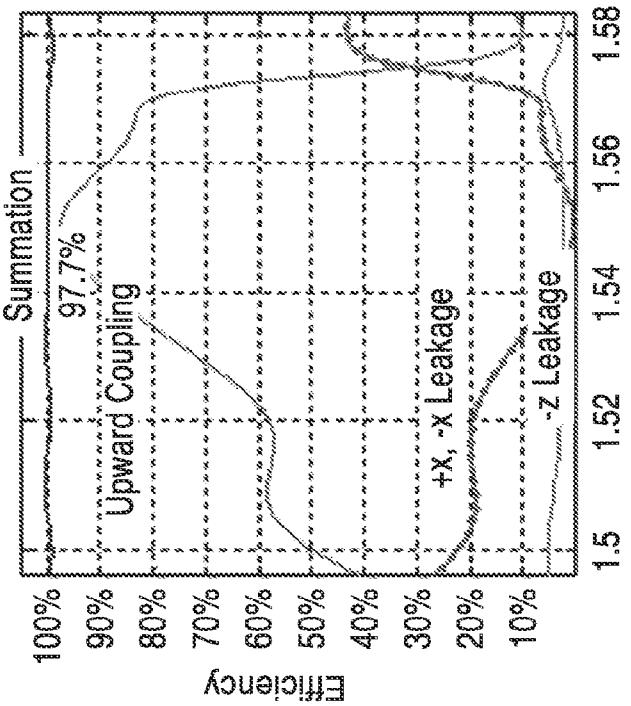

Summation
97.7%
Upward Coupling
+x, -x Leakage
-z Leakage
Efficiency
100%
90%
80%
70%
60%
50%
40%
30%
20%
10%
1.5
1.52
1.54
1.56
1.58
λ(μm)

FIG. 8B

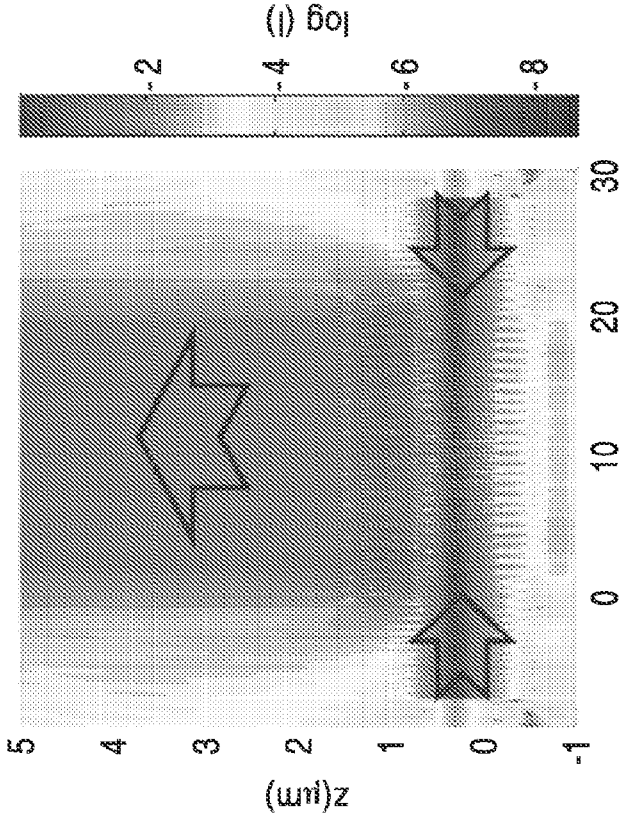

log (I)
-2
-4
-6
-8
z(μm)
5
4
3
2
1
0
-1
0
10
20
30
x(μm)

FIG. 8A

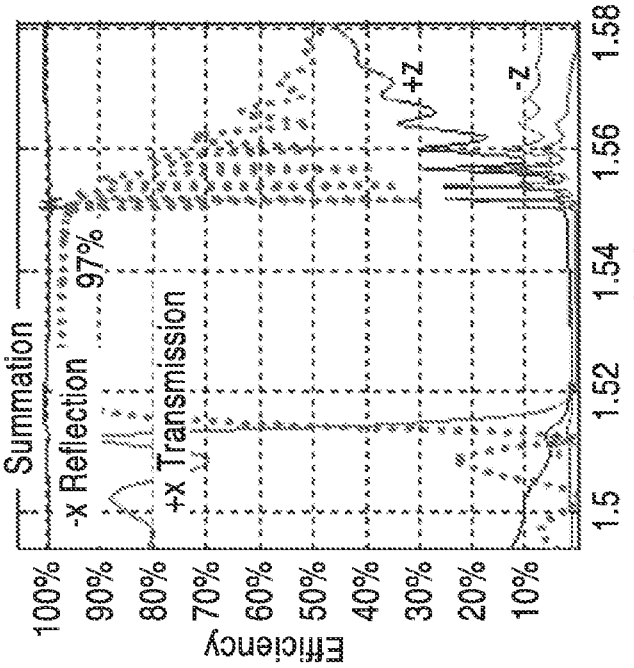

Summation
-x Reflection
97%
+x Transmission
+z
-z
Efficiency
100%
90%
80%
70%
60%
50%
40%
30%
20%
10%
1.5
1.52
1.54
1.56
1.58
λ(μm)

FIG. 9B

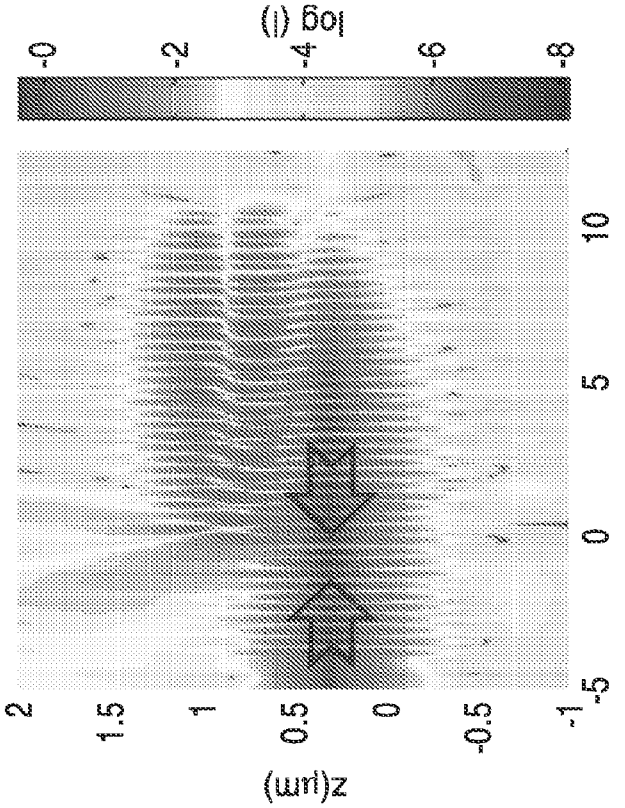

log (I)
-0
-2
-4
-6
-8
x(μm)
-5
0
5
10
z(μm)
2
1.5
1
0.5
0
-0.5
-1

FIG. 9A

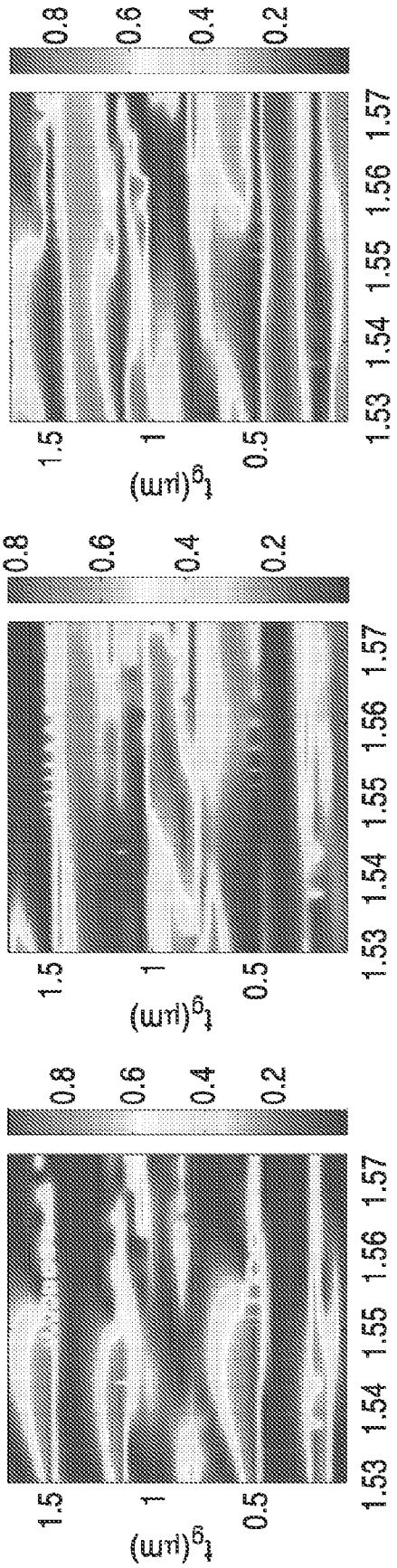


FIG. 10C

FIG. 10B

FIG. 10A

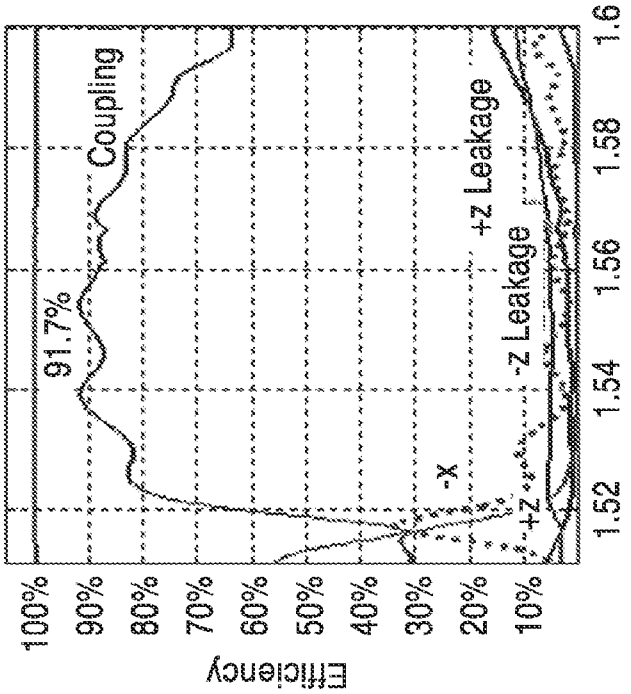


FIG. 11B

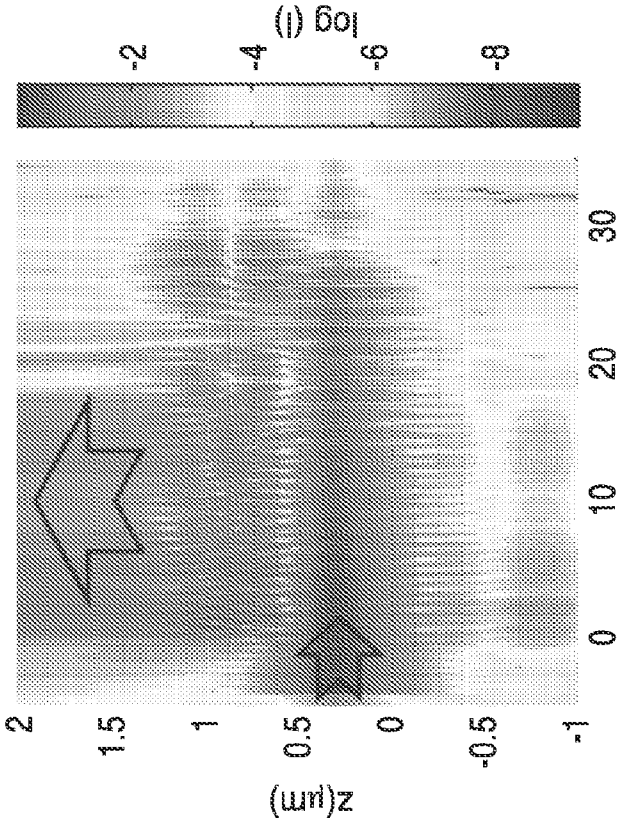


FIG. 11A

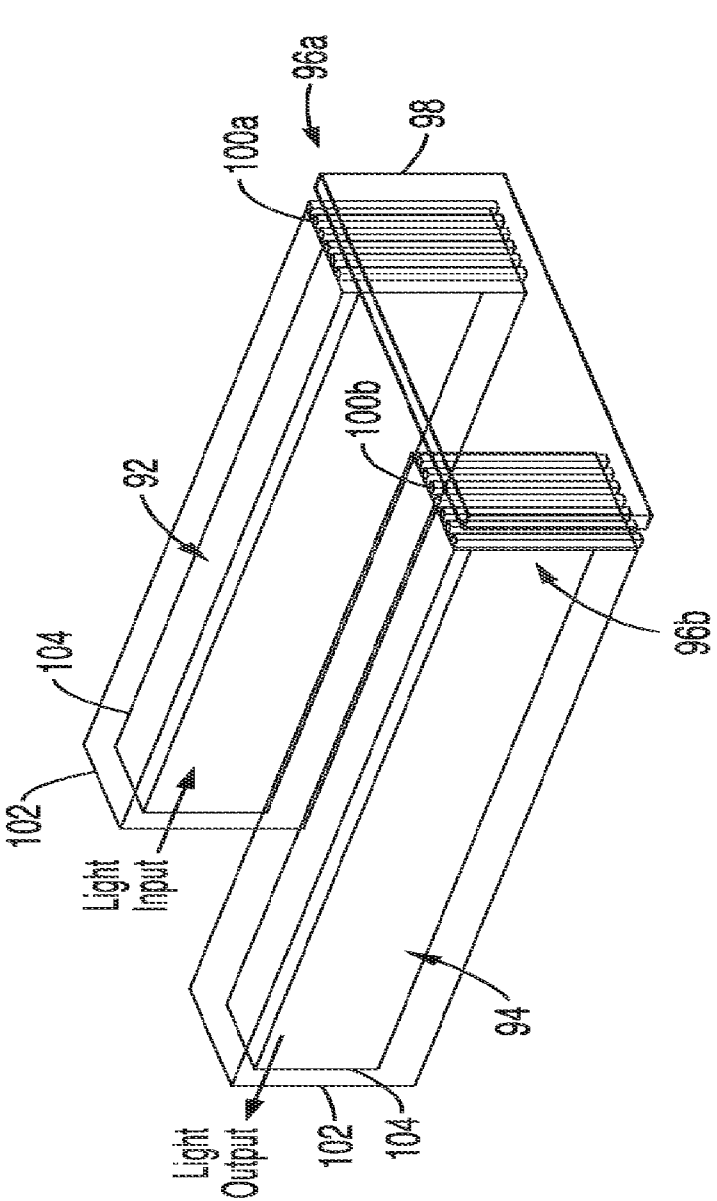


FIG. 12

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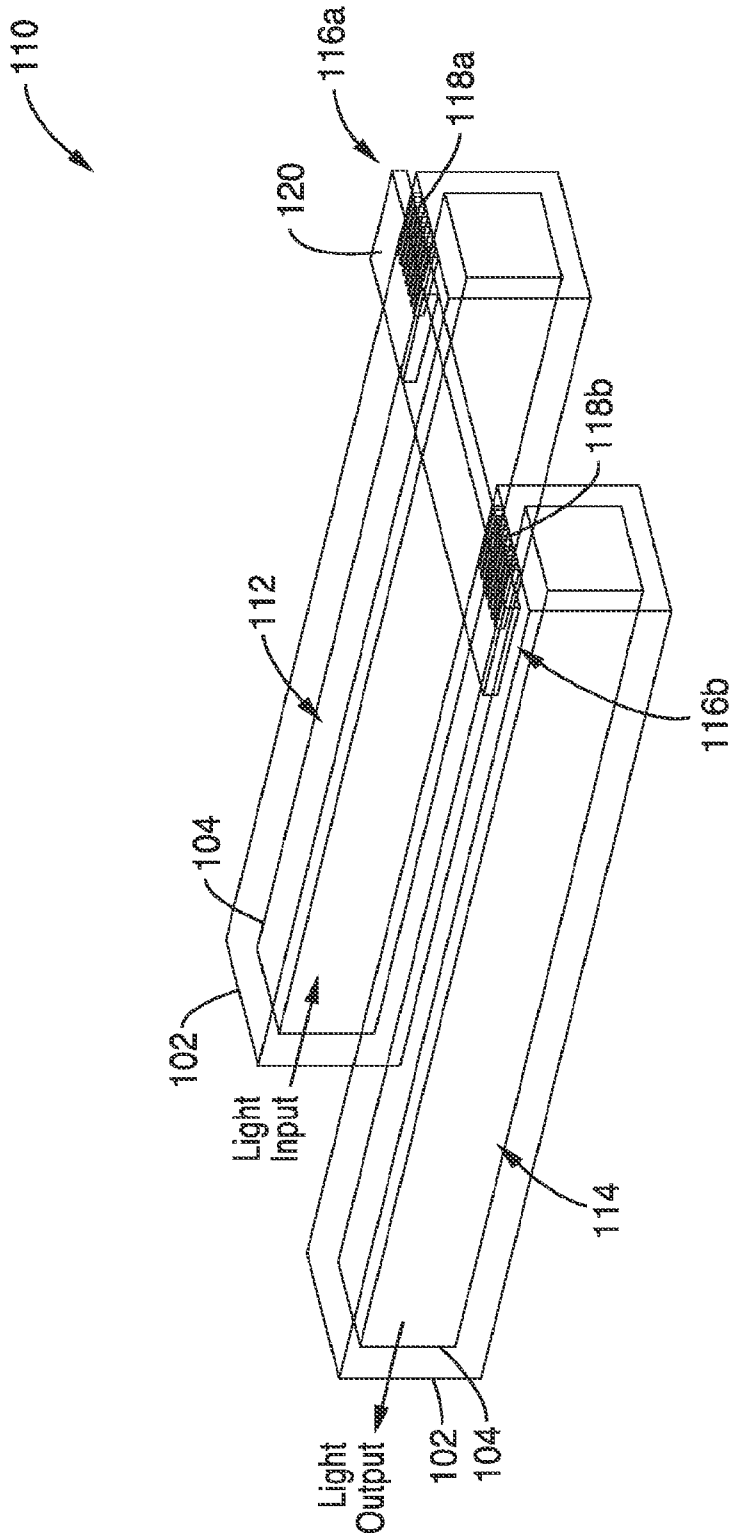

110
116a
118a
120
118b
112
116b
104
102
Light Input
114
Light Output
102
104

FIG.13

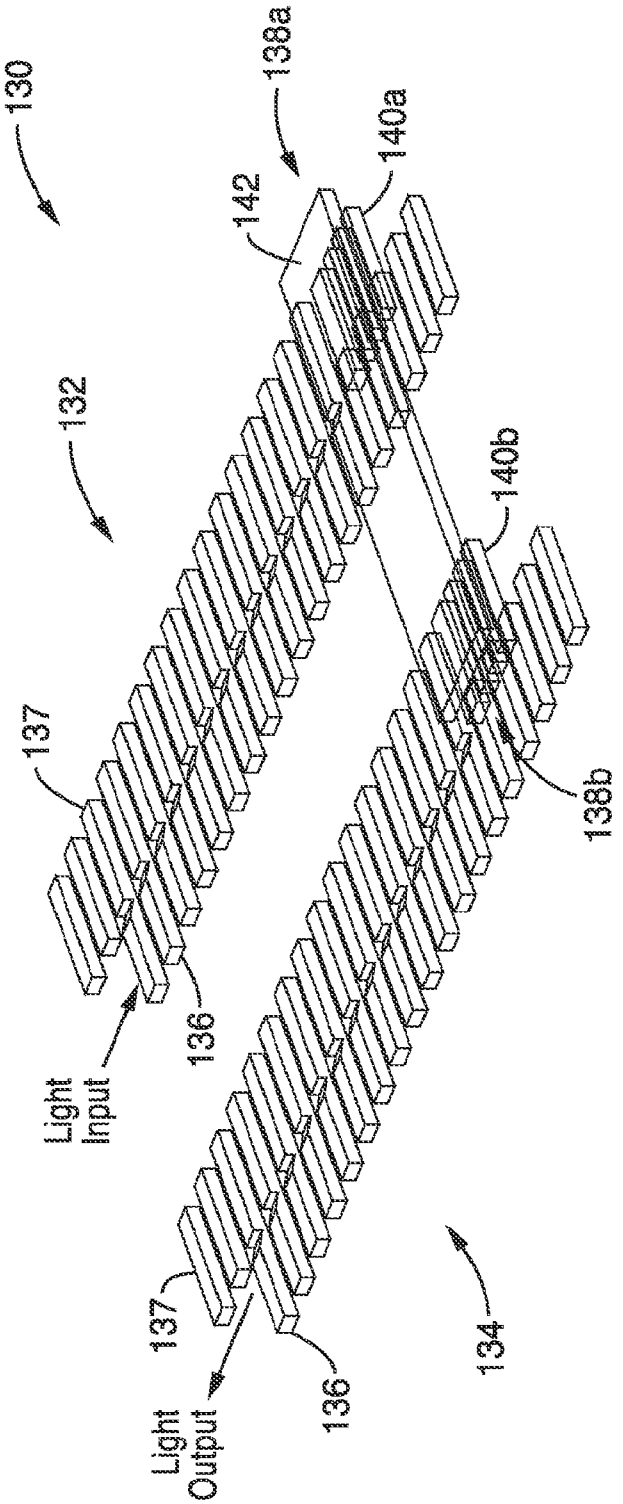

130
138a
140a
142
132
140b
137
138b
Light Input
136
137
Light Output
136
134

FIG. 14

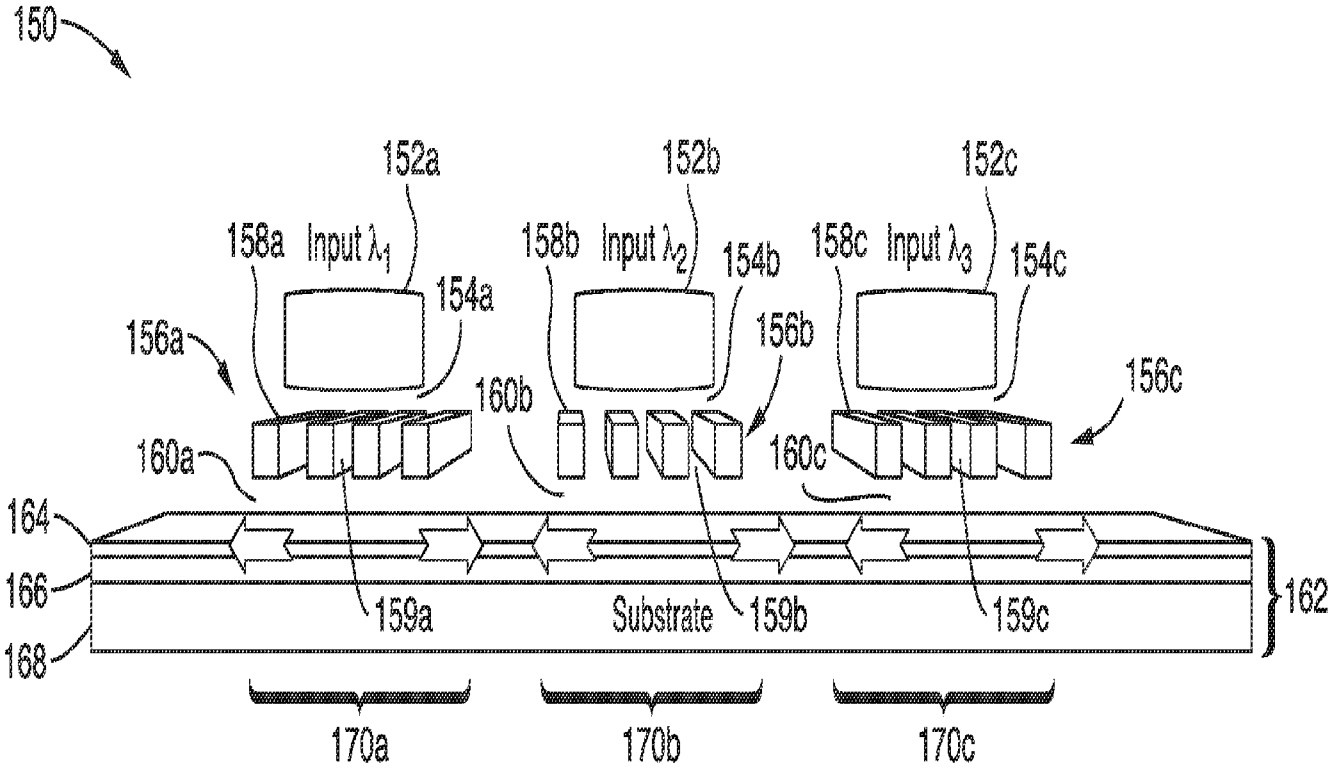

150
152a
152b
152c
158a
Input λ_1
158b
Input λ_2
158c
Input λ_3
154a
154b
154c
156a
156b
156c
160a
160b
160c
164
166
168
159a
Substrate
159b
159c
162
170a
170b
170c

FIG. 15

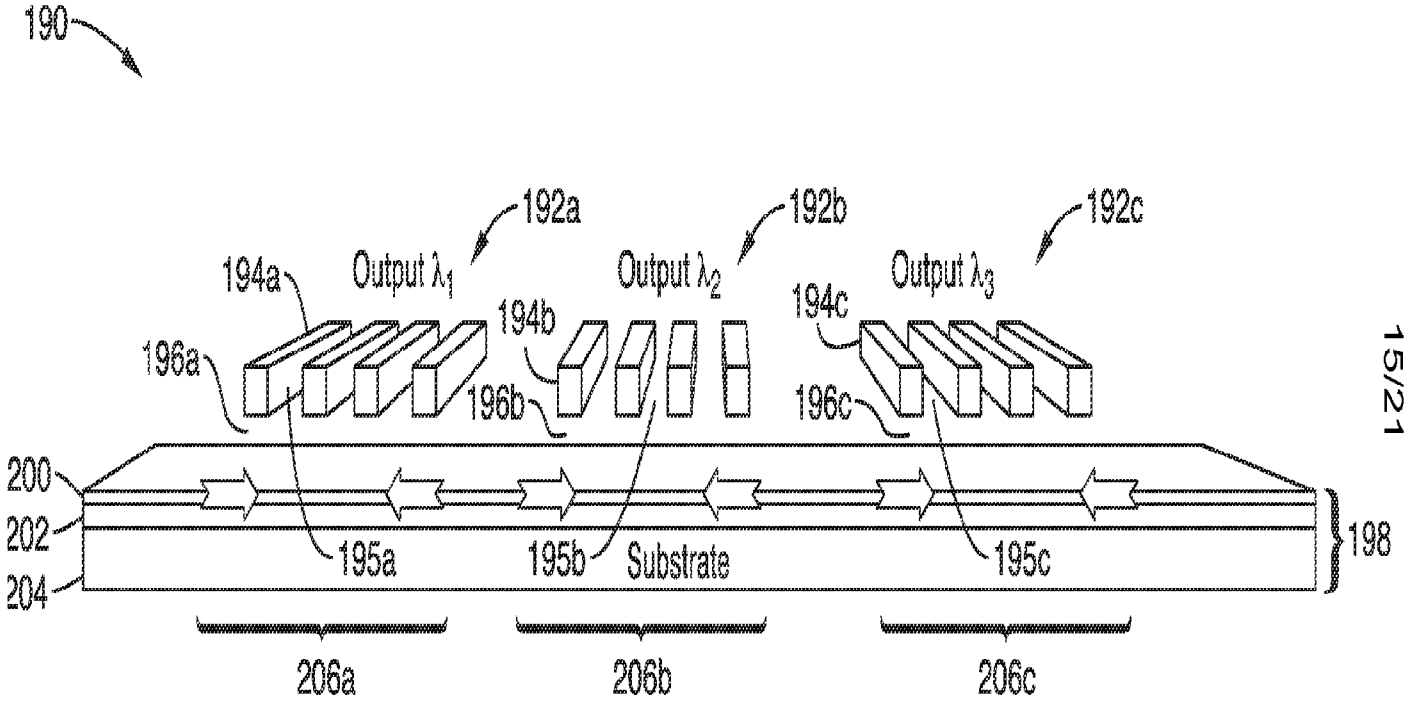

190
192a
192b
192c
194a
Output λ_1
Output λ_2
Output λ_3
194b
194c
196a
196b
196c
200
202
204
195a
195b
Substrate
195c
198
206a
206b
206c

FIG. 16

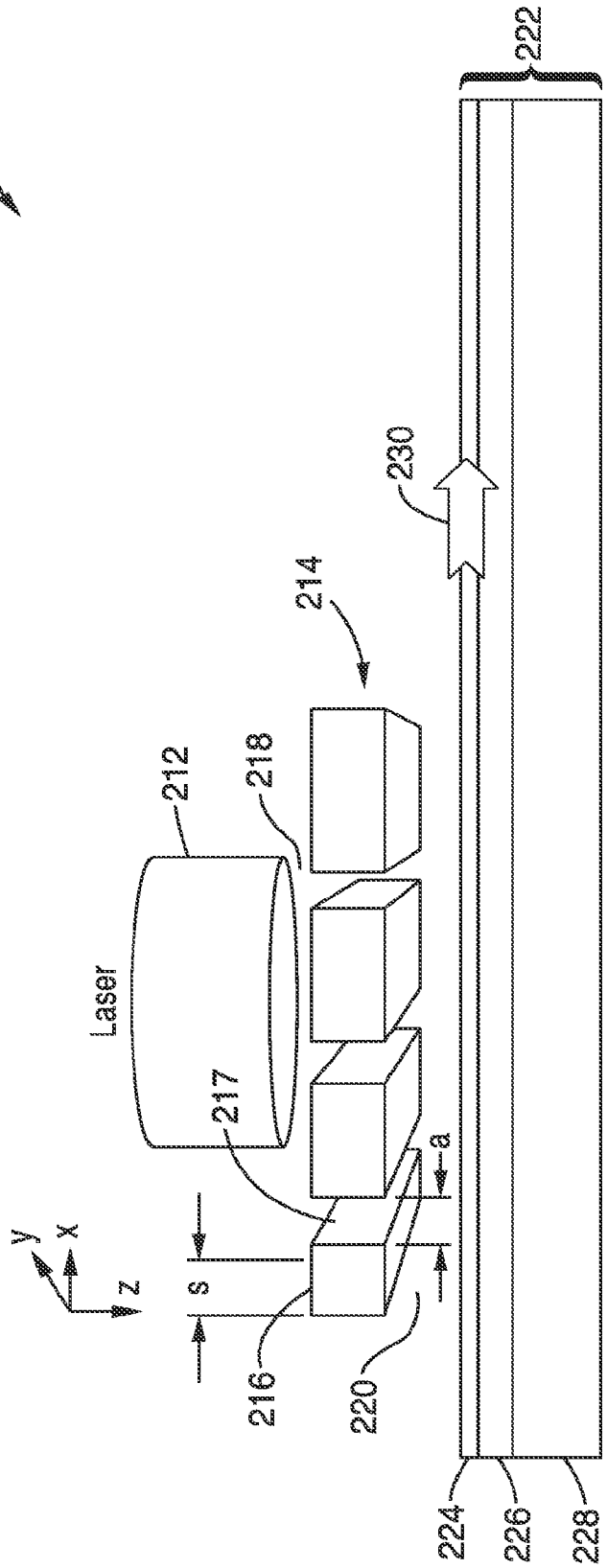


FIG. 17

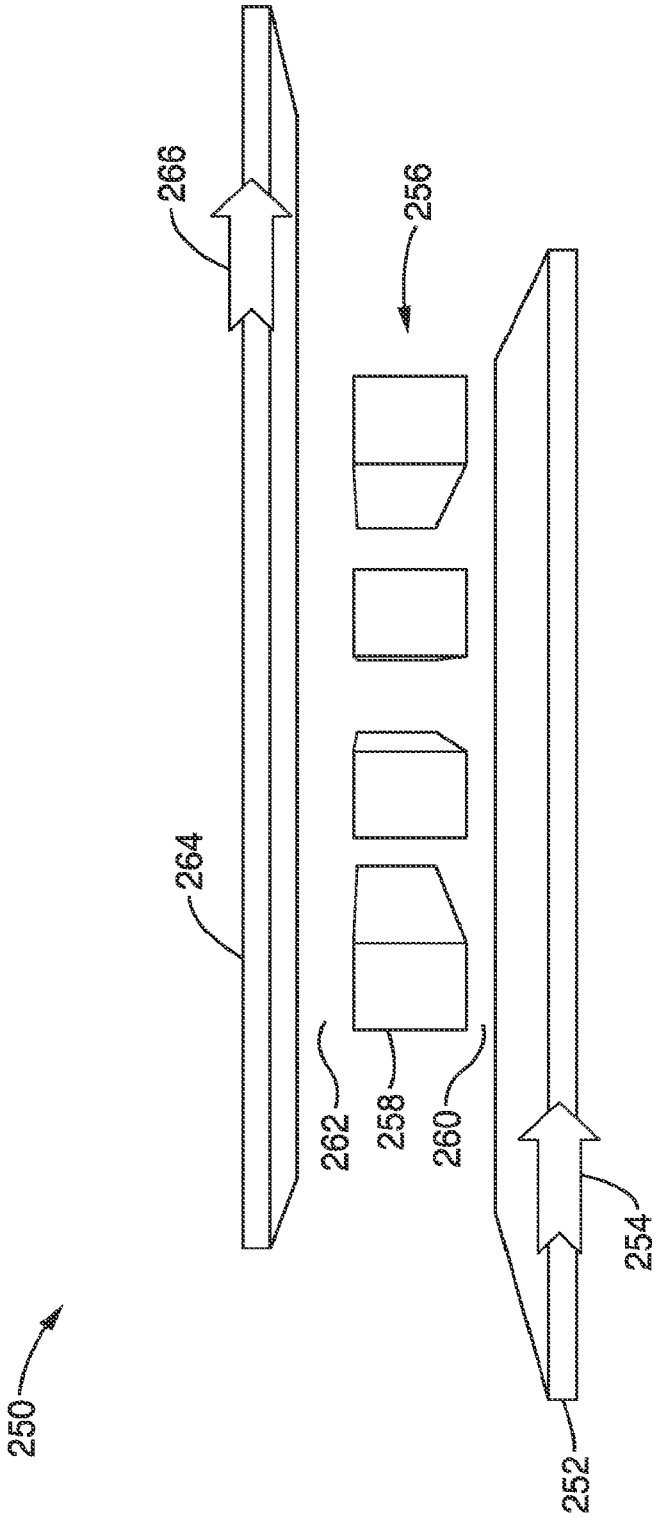


FIG. 18

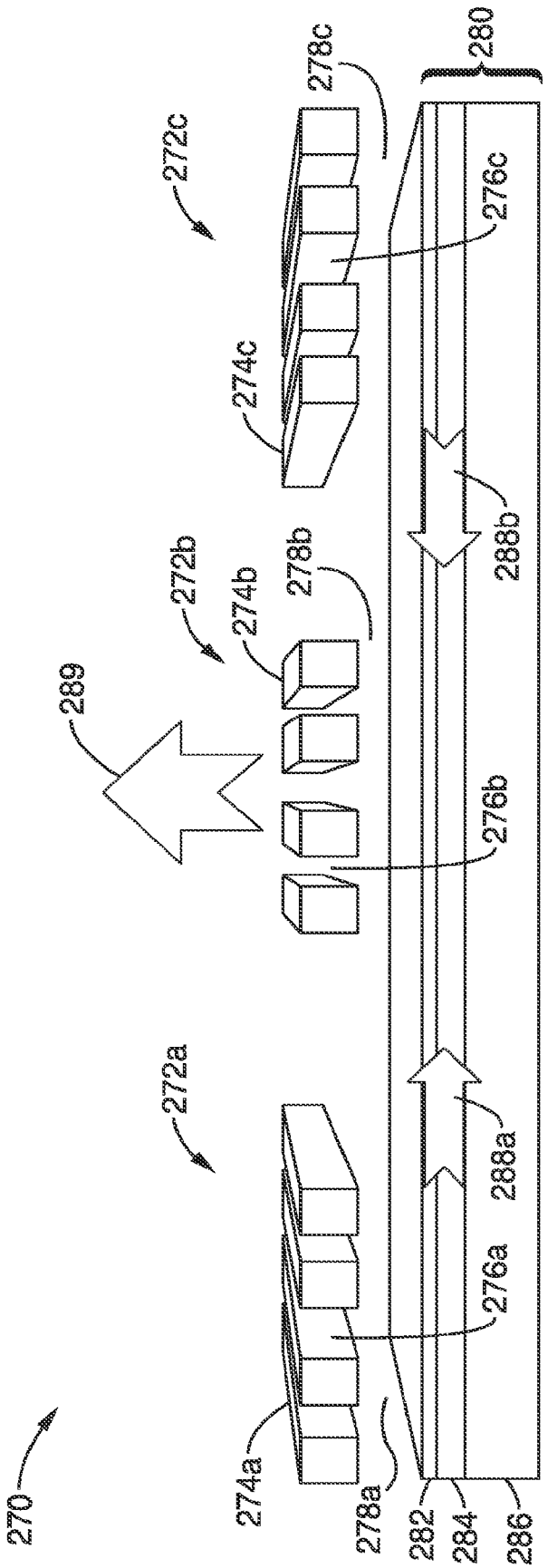

270
272a
272b
272c
274a
274b
274c
276a
276b
276c
278a
278b
278c
280
282
284
286
288a
288b
289

FIG. 19

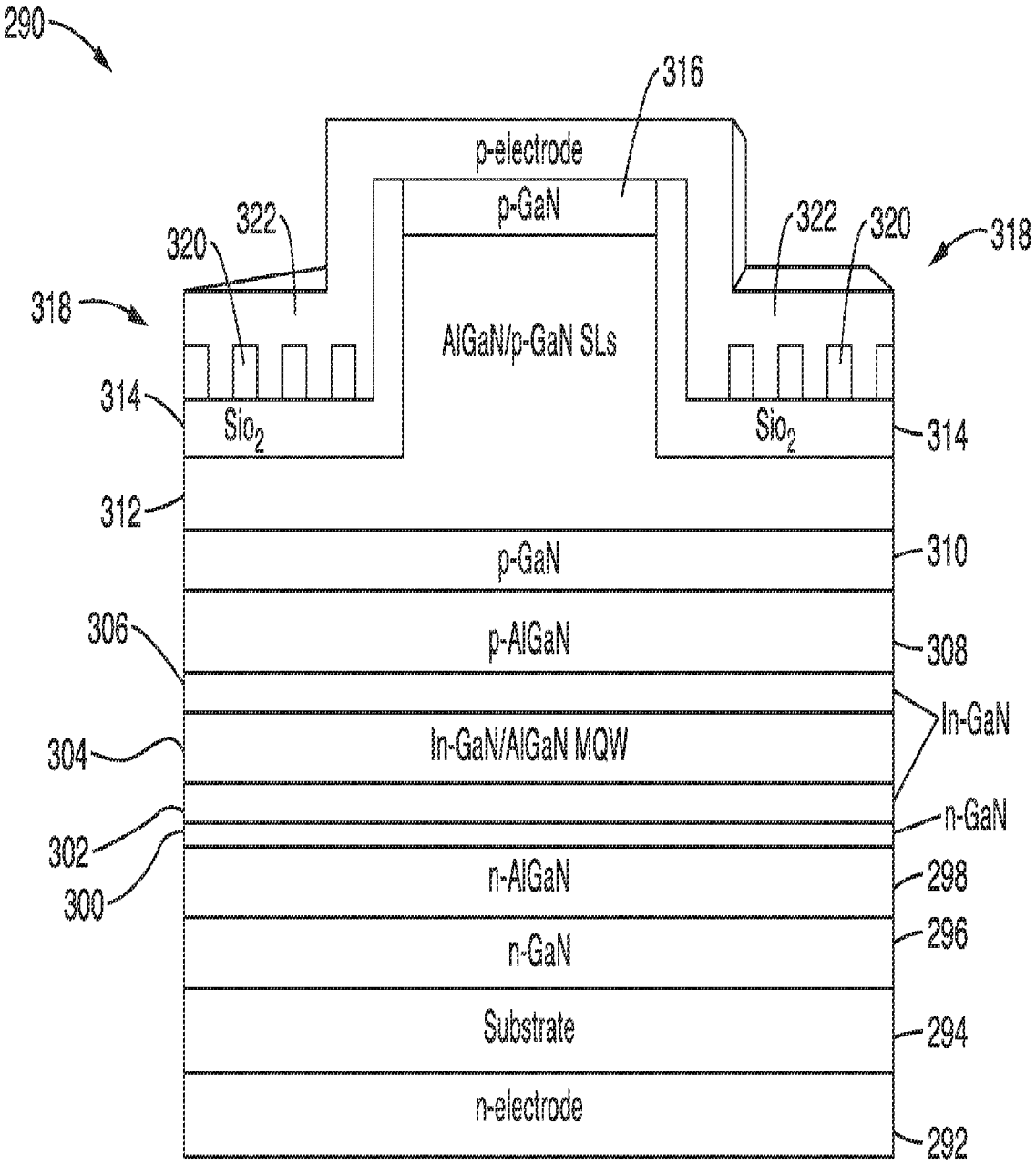

290
316
p-electrode
p-GaN
322
320
322
320
318
318
AlGaN/p-GaN SLs
314
SiO_2
SiO_2
314
312
p-GaN
310
306
p-AlGaN
308
In-GaN
304
In-GaN/AlGaN MQW
n-GaN
302
n-AlGaN
298
300
n-GaN
296
Substrate
294
n-electrode
292

FIG. 20

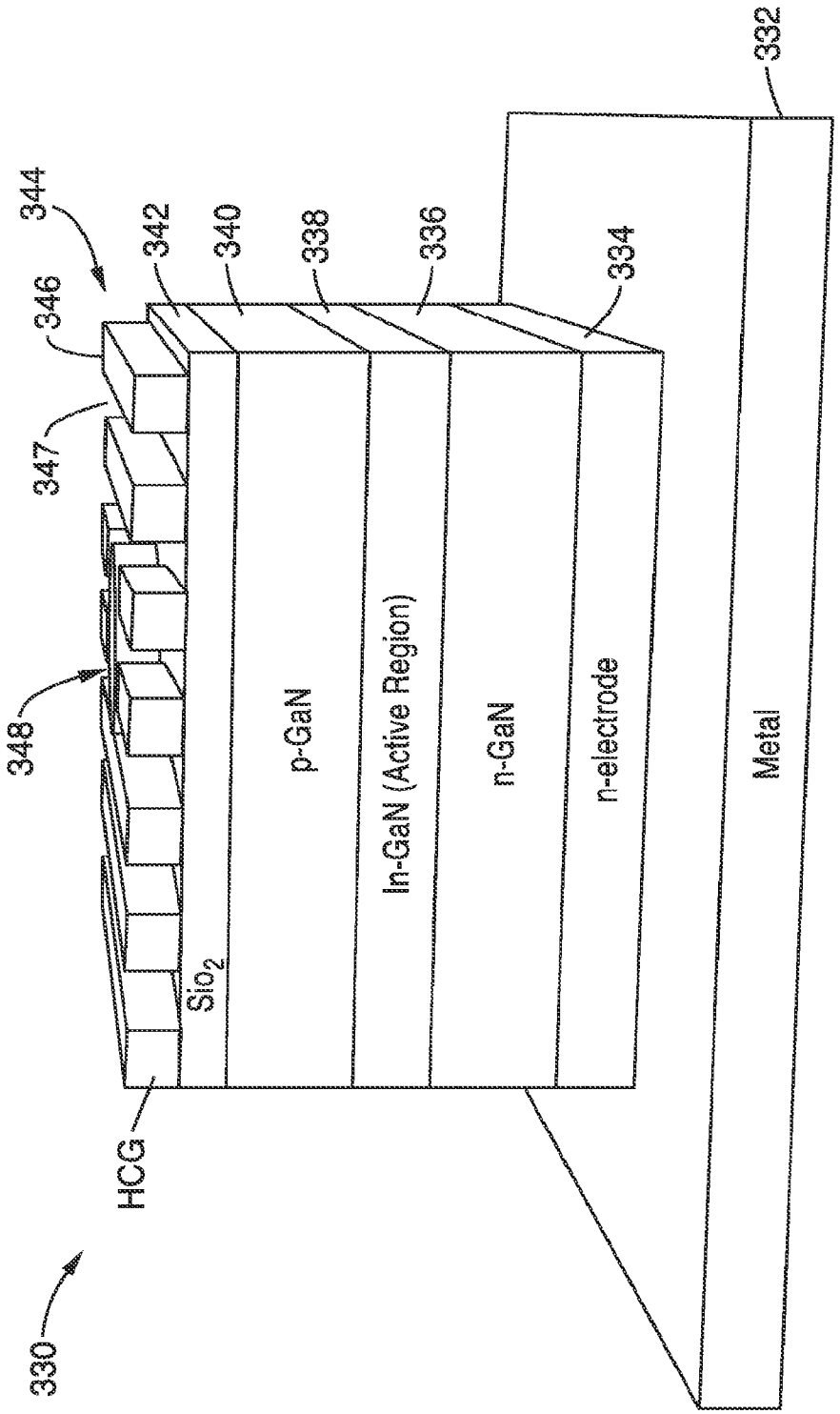

332
344
342
340
338
336
334
346
347
348
330
HCG
Sio_2
p-GaN
In-GaN (Active Region)
n-GaN
n-electrode
Metal

FIG. 21

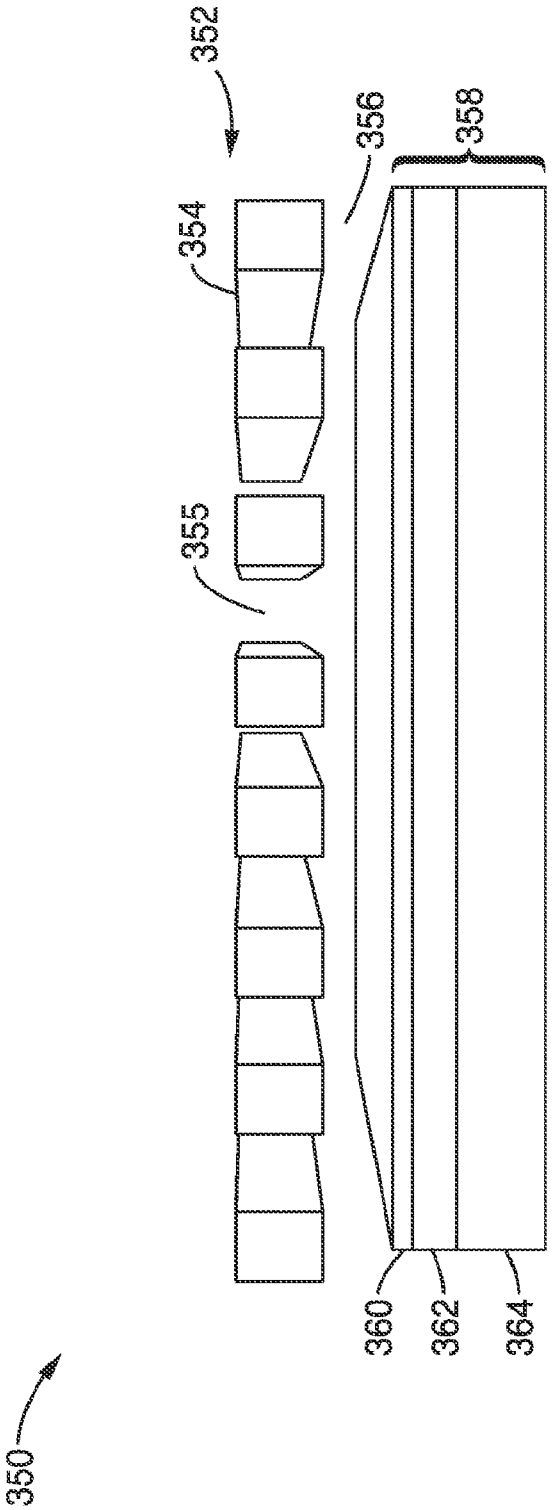


FIG. 22

REMARKS

This Third Preliminary Amendment cancels dependent claims 7, 20, 21, and 25-27 without prejudice or disclaimer, and submits in their place independent claim 31 and dependent claims 32-36. The total number of claims remains 30 but the number of independent claims is increased from 3 to 4, which complies with the limitations regarding number of claims in applications made special based on applicant's age as set forth in MPEP § 708.02.

Examples of structures integrating a photodetector and an active electronic circuit on the same silicon are illustrated in Figs. 44-52 and 86, and discussed in paragraphs 196-205 and 247 of the subject application, and elsewhere. Examples of photodetectors and their performance are illustrated in Figs. 2-43D, 53-85, and 87-117.

Applicants thank the Examiner for scheduling a telephone interview with their undersigned representative for Wednesday, September 28, 2016, 1 PM.

The Patent Office is hereby authorized to charge any fees that are required in connection with this amendment and to credit any overpayment to our Deposit Account No. 03-3125.

Respectfully submitted,

/Ivan S. Kavrukov/
Ivan S. Kavrukov, Reg. No. 25,161
Attorney for Applicant
COOPER & DUNHAM LLP
30 Rockefeller Plaza, 20th Floor
New York, NY 10112
Tel.: (212) 278-0400

Electronic Acknowledgement Receipt

EFS ID:	27042662
Application Number:	14945003
International Application Number:	
Confirmation Number:	1200
Title of Invention:	MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES
First Named Inventor/Applicant Name:	Shih-Yuan WANG
Customer Number:	23432
Filer:	Ivan Kavrukov/Mary Ellen Finnegan
Filer Authorized By:	Ivan Kavrukov
Attorney Docket Number:	5176-88184-2
Receipt Date:	27-SEP-2016
Filing Date:	18-NOV-2015
Time Stamp:	12:30:14
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	DA
Payment was successfully received in RAM	$210
RAM confirmation Number	092716INTEFSW00012761033125
Deposit Account	033125
Authorized User	Mary Ellen Finnegan

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

37 CFR 1.21 (Miscellaneous fees and charges)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Preliminary Amendment	ThirdPreliminaryAmendment.pdf	87293 655364c96e3f61a70a1c0c1ca201673c9039be5d	no	10
Warnings:					
Information:					
2	Fee Worksheet (SB06)	fee-info.pdf	30772 37075cbfafafc75ef3db01d7f3a55b34461e19e3	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	118065		

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New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application of: Shih-Yuan WANG

Application No.: 14/945,003

Date Filed: November 17, 2015

For: MICROSTRUCTURE ENHANCED ABSORPTIO00N PHOTOSENSITIVE DEVICES

Conf. No.: 1200

This correspondence is being filed electronically with the U.S. Patent and Trademark Office via EFS-Web. /Ivan S. Kavrukov/ September 27, 2016 Ivan S. Kavrukov	30 Rockefeller Plaza, 20th Floor New York, New York 10112 Tel.: (212) 278-0400

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

THIRD PRELIMINARY AMENDMENT

Prior to examination of the above-identified patent application, please enter this Amendment.

Amendments to the claims are reflected in the **Listing of Claims** section which begins on page 2.

Remarks begin on page 8 of this paper.

Electronic Patent Application Fee Transmittal

Application Number:	14945003
Filing Date:	18-Nov-2015
Title of Invention:	MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES
First Named Inventor/Applicant Name:	Shih-Yuan WANG
Filer:	Ivan Kavrukov/Mary Ellen Finnegan
Attorney Docket Number:	5176-88184-2

Filed as Small Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
INDEPENDENT CLAIMS IN EXCESS OF 3	2201	1	210	210
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Extension-of-Time:				
Miscellaneous:				
			Total in USD ($)	**210**

Listing of Claims

The following listing of claims will replace all prior versions, and listings, of claims in the subject application:

1. (Previously Submitted) An integrated detector/processor circuit for data communication comprising both a photodetector with microstructure-enhanced photoabsorption and an electronic processor formed into a single semiconductor chip, comprising:

a photodetector formed on a semiconductor substrate and comprising a photon absorbing region configured to absorb photons from an optical source signal modulated for data communication and provide an output electrical signal corresponding thereto;

said photon absorbing region comprising a plurality of holes therein extending toward said substrate and configured to concurrently receive the same source signal at a plural number of the holes;

an electronic processor also formed on said semiconductor substrate and operatively associated with said photon absorbing region to receive therefrom and process said output electrical signal into a processed output, thereby forming a single semiconductor chip that receives the optical source signal and outputs the processed output;

wherein said photon absorbing region and said electronic processor have respective thicknesses that are of the same order of magnitude; and

a cathode region and an anode region operatively associated with said photon absorbing region and reverse biasing circuitry configured to apply a voltage between said cathode and anode regions such that said cathode region is driven to a more positive voltage than said anode region.

2. (Original) The integrated detector/processing circuit of claim 1, wherein the thickness of the photon absorbing region is in the range of 0.5 to 5 micrometers.

3. (Original) The integrated detector/processing circuit of claim 1, wherein the electronic processor comprises an application specific integrated circuit (ASIC) comprising at least

one of complementary metal oxide semiconductor (CMOS) devices, bipolar (Bi) devices, and BiCMOS devices.

4.(Original) The integrated detector/processing circuit of claim 1, wherein the photon absorbing region is configured to absorb in excess of 60% of the incident source signal at wavelengths from 800 nm to 900 nm and provide an output electrical signal corresponding thereto.

5. (Original) The integrated detector/processing circuit of claim 1, wherein the photon absorbing region is configured to absorb the incident source signal at an absorption percentage that varies by less than 20% over selected wavelength spans of at least 20 nm of source signal wavelengths from 800 nm to 900 nm.

6. (Original) The integrated detector/processing circuit of claim 1, wherein the photon absorbing region is configured to absorb the incident source signal at an absorption percentage that varies by less than 20% over selected wavelength spans of at least 20 nm of source signal wavelengths from 800 nm to 900 nm.

7. (Canceled) The integrated detector/processing circuit of claim 1, wherein the photon absorbing region is configured to absorb in excess of 60% of the incident source signal at wavelengths from 800 nm to 900 nm and provide an output electrical signal corresponding thereto

8. (Previously Submitted) The integrated detector/processing circuit of claim 1, further including one or more additional photodetectors formed on said semiconductor substrate and having respective photon absorbing regions receiving respective additional source signals and providing respective output electrical signals corresponding thereto, and one or more additional electronic processors also formed on said semiconductor substrate and operatively associated with the respective photon absorbing regions of said additional photodetectors to receive therefrom and [procces] process said respective output

electrical signals therefrom.

9. (Previously Submitted) The integrated detector/processing circuit of claim 1, wherein the plurality of holes enhances absorption of photons compared to a hole-free but otherwise same photodetector at a range of wavelengths that includes a wavelength of said source signal.

10. (Original) The integrated detector/processing circuit of claim 1, wherein the electronic processor includes one or more types selected from a group consisting of: transimpedance amplifier, signal processing electronics, and routing electronics.

11. (Original) The integrated detector/processing circuit of claim 1, wherein a capacitance associated with the photodetector is decreased compared to an otherwise same photodetector having its anode and cathode regions operatively connected to a conventional bond pad.

12. (Previously Submitted) A photodetector with microstructure-enhanced photoabsorption comprising:

a photon absorbing region having a thickness between 0.5 and 5 micrometers and configured to absorb photons from a source signal modulated for data communication and provide an output electrical signal corresponding thereto;

said photon absorbing region comprising silicon with a plurality of holes extending through at least a portion of the thickness of the photon absorbing region and configured to concurrently receive the same source signal at a plural number of the holes; and

said photon absorbing region being configured to absorb in excess of 40% of the incident source signal at wavelengths in at least one of the ranges from 800 nm to 900 nm and from 1400 nm to 1700 nm and provide an output electrical signal corresponding thereto.

13. (Original) The photodetector of claim 12, wherein the photon absorbing region is configured to absorb in excess of 40% of the incident source signal at wavelengths from 800 nm to 900 nm and provide an output electrical signal corresponding thereto.

14. (Original) The photodetector of claim 12, wherein the photon absorbing region is configured to absorb in excess of 50% of the incident source signal at wavelengths from 800 nm to 900 nm and provide an output electrical signal corresponding thereto.

15. (Original) The photodetector of claim 12, wherein the photon absorbing region is configured to absorb the incident source signal at an absorption percentage that varies by less than 20% over wavelength spans of at least 20 nm of source signal wavelengths from 800 nm to 900 nm.

16. (Original) The photodetector of claim 12, wherein each hole has a cross-section parallel to the upper surface of the substrate and has a maximum dimension of between 400 nm and 2500 nm, and each hole has a center that is spaced apart by less than 3500 nm from a center of a nearest adjacent hole of the plurality of holes.

17. (Previously Submitted) The photodetector of claim 12, wherein the photodetector comprises a reflecting structure configured to cause multiple reflections of the source signal thereby traversing the photon absorbing region with said source signal multiple times.

18. (Previously Submitted) A photodetector with microstructure-enhanced photoabsorption comprising:

a cathode region;

an anode region;

reverse biasing circuitry configured to apply a voltage between said cathode and anode regions such that said cathode region is driven to a more positive voltage than said anode region;

a substrate material having an upper surface; and

a photon absorbing region comprising silicon, operatively associated with the cathode and anode regions, and configured to absorb photons from a source signal, said absorbing region including a plurality of holes each having a cross section parallel to the upper substrate surface having a maximum dimension of between 400 nm and 2500 nm, and each hole having a center that is spaced apart by less than 3500 nm from a center of a nearest adjacent hole of the plurality of holes.

19. (Original) The photodetector of claim 18 wherein the source signal has a wavelength that is greater than 800 nm and less than 1000 nm.

20. (Canceled) The photodetector according to claim 18 wherein the plurality of holes are arranged into a periodically-spaced array.

21. (Canceled) The photodetector according to claim 20 wherein the periodically-spaced array has a hexagonal or square lattice pattern.

22. (Previously Submitted) The photodetector according to claim 18 wherein the plurality of holes enhances absorption of photons compared to a hole-free but otherwise same photodetector at a range of wavelengths that includes a wavelength of said source signal.

23. (Previously Submitted) The photodetector according to claim 18 wherein each of the holes has a predominately circular cross-section parallel to the upper substrate surface.

24. (Original) The photodetector according to claim 18 wherein the cathode and anode regions are operatively connected to integrated circuit electronics and the photodetector and integrated circuit electronics are integrated into a single silicon chip.

25. (Canceled) The photodetector according to claim 24 wherein the integrated circuit electronics includes one or more types selected from a group consisting of:

transimpedance amplifier, signal processing electronics and routing electronics.

26. (Canceled) The photodetector according to claim 18 wherein said photodetector is configured to detect said source signal at a data bandwidth of greater than 2.5 gigabits per second at source signal wavelengths of 850 nanometers with a quantum efficiency of at least 30%.

27. (Canceled) The photodetector according to claim 18 wherein said photodetector is configured to detect said source signal at a data bandwidth of greater than 2.5 gigabits per second at source signal wavelengths of 850 nanometers with a quantum efficiency of at least 50%.

28. (Original) The photodetector according to claim 18 wherein said photodetector is configured to detect said source signal at a data bandwidth of greater than or equal to 5 gigabits per second, at source signal wavelengths of 850 nanometers with a quantum efficiency of at least 30%.

29. (Original) The photodetector according to claim 18 wherein said photodetector is configured to detect said source signal at a data bandwidth of greater than or equal to 5 Gb/s, at source signal wavelengths of 850 nanometers with a quantum efficiency of at least 50%.

30. (Original) The photodetector according to claim 18 further including a substrate and wherein the cathode, absorbing and anode regions are formed above the substrate and the photodetector is configured to receive the source signal from directions facing a side of the photodetector opposite of the substrate.

31. (New) A single silicon substrate on which are fabricated and integrated a photodetector, an active electronic circuit, and electrical interconnects that operatively couple the photodetector and the active electronic circuit to each other and provide an output for use by other circuits, comprising:

a photodetector fabricated on the single silicon substrate and comprising a P-doped region, an N-doped region, and an I-region that is between the P-doped region and the N-doped region and is not intentionally doped or is doped to a lower dopant concentration than the P-doped region and the N-doped region, wherein:

said I-region:

comprises at least one of silicon and germanium;

is no more than 5000 nanometers thick in a direction from one toward the other of said P-doped region and said N-doped region;

comprises intentionally formed pillars or holes, said pillars or holes being spaced from each other and extending in said direction from one toward the other of said P-doped region and N-doped region;

said photodetector is configured to receive an optical beam that:

is modulated at 10 Gigabits per second or more;

is substantially continuous in cross-section; and

impinges on plural ones of said pillars or holes at the same time;

said photodetector is further configured to provide, in response to impingement thereon of said optical beam, a photodetector electrical output that:

represents the modulation of said optical beam; and

has a bandwidth of 10 Gigabits per second or more;

said photodetector has quantum efficiency of at least 30% (i) when the optical beam wavelength in 850-1000 nm and the I-region comprises silicon, and (ii) when the optical beam wavelength is 1550-1660 nm and the I-region comprises germanium; and

an active electronic circuit that:

is fabricated on the substrate on which the photodetector is fabricated;

comprises at least one of CMOS and BiCMOS integrated circuit fabricated with at least one of silicon and germanium; and

is configured to:

receive the photodetector electrical output from the photodetector; and

process the received photodetector electrical output to thereby produce a processed electrical output that has at least some different characteristics compared with the photodetector electrical output; and

electrical interconnects that:

also are fabricated on the same silicon substrate;

are configured to operatively couple said photodetector and said active electronic circuit to each other, including by transferring said photodetector electrical output from said photodetector to said active electronic circuit; and

are further configured to output the processed electrical output from the active electronic circuit for use by other circuits.

32. (New) The single silicon substrate of claim 31 in which the I-region comprises said holes.

33. (New) The single substrate of claim 32 in which the holes are arranged in an aperiodic array.

34. (New) The single silicon substrate of claim 31 in which the I-region comprises said pillars.

35. (New) The single silicon substrate of claim 31 in which said pillars are arranged in an aperiodic array.

36. (New) The single silicon substrate of claim 31 further comprising a layer of oxide between the silicon substrate and the photodetector.

PTO/SB/06 (09-11)
Approved for use through 1/31/2014. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 14/945,003	Filing Date 11/18/2015	☐ To be Mailed

ENTITY: ☐ LARGE ☒ SMALL ☐ MICRO

APPLICATION AS FILED – PART I

	(Column 1)	(Column 2)		
FOR	NUMBER FILED	NUMBER EXTRA	RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).			
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))				
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL	

APPLICATION AS AMENDED – PART II

		(Column 1)		(Column 2)	(Column 3)		
AMENDMENT	09/27/2016	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	* 30	Minus	** 30	= 0	X $40 =	0
	Independent (37 CFR 1.16(h))	* 4	Minus	***3	= 1	X $210 =	210
	☐ Application Size Fee (37 CFR 1.16(s))						
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
						TOTAL ADD'L FEE	**210**

		(Column 1)		(Column 2)	(Column 3)		
AMENDMENT		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =	
	☐ Application Size Fee (37 CFR 1.16(s))						
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
						TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

LIE
GLORIA ANTHONY

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**
If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Dkt. 5176/88184-2

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application of: Shih-Yuan WANG et al.

Application No.: 14/945,003

Confirmation No.: 1200

GAU: 2893

Filed: November 18, 2015

Examiner: Rodela, Eduardo A.

For: MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES

This correspondence is being filed electronically with the U.S. Patent and Trademark Office via EFS-Web.

/erin finnegan/ **September 27, 2016**

Erin Finnegan Date

30 Rockefeller Plaza, 20th Floor
New York, New York 10112
Tel.: (212) 278-0400

INFORMATION DISCLOSURE STATEMENT

Applicants hereby advise the Examiner of the following co-pending applications with related subject matter:

1. Ser. No. 14/943,898 filed November 17, 2015;
2. PCT/US15/61120, filed November 17, 2015;
3. Ser. No.14/892,821, filed November 20, 2015 (allowed September 14, 2016);
4. Ser. No. 14/947,718, filed November 20, 2015;
5. PCT/US14/190189, filed May 22, 2014;
6. Ser. No. 13/821,963, filed October 22, 2013 (allowed September 13, 2016); and
7. PCT/US11/51091, filed September 9, 2011.

No fees are believed to be required in connection with this filing. Nevertheless, the Patent Office is hereby authorized to charge any fees that are required for consideration of this Information Disclosure Statement, and to credit any overpayment during prosecution of this application, to our Deposit Account No. 03-3125.

Respectfully submitted,

/ivan s. kavrukov/

Ivan Kavrukov, Reg. No. 25,161
Attorney for Applicant
COOPER & DUNHAM LLP
30 Rockefeller Plaza, 20th Floor
New York, New York 10112
Tel.: (212) 278-0400

Electronic Acknowledgement Receipt

EFS ID:	27048760
Application Number:	14945003
International Application Number:	
Confirmation Number:	1200
Title of Invention:	MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES
First Named Inventor/Applicant Name:	Shih-Yuan WANG
Customer Number:	23432
Filer:	Ivan Kavrukov/Erin Finnegan
Filer Authorized By:	Ivan Kavrukov
Attorney Docket Number:	5176-88184-2
Receipt Date:	27-SEP-2016
Filing Date:	18-NOV-2015
Time Stamp:	16:27:45
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Transmittal Letter	IDS_2_communication.pdf	87756 959296a88ee754863478da05b8fa4fe8fdc4bf4b	no	2

Warnings:

Information:	
Total Files Size (in bytes):	87756

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National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application of: Shih-Yuan WANG

Application No.: 14/945,003

Date Filed: November 17, 2015

For: MICROSTRUCTURE ENHANCED ABSORPTIO00N PHOTOSENSITIVE DEVICES

Conf. No.: 1200

This correspondence is being filed electronically with the U.S. Patent and Trademark Office via EFS-Web. /Ivan S. Kavrukov/ September 23, 2016 Ivan S. Kavrukov	30 Rockefeller Plaza, 20th Floor New York, New York 10112 Tel.: (212) 278-0400

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

SECOND PRELIMINARY AMENDMENT

Prior to examination of the above-identified patent application, please enter this Amendment.

Amendments to the claims are reflected in the **Listing of Claims** section which begins on page 2.

Remarks begin on page 8 of this paper.

Listing of Claims

The following listing of claims will replace all prior versions, and listings, of claims in the subject application:

1. (Previously Submitted) An integrated detector/processor circuit for data communication comprising both a photodetector with microstructure-enhanced photoabsorption and an electronic processor formed into a single semiconductor chip, comprising:

a photodetector formed on a semiconductor substrate and comprising a photon absorbing region configured to absorb photons from an optical source signal modulated for data communication and provide an output electrical signal corresponding thereto;

said photon absorbing region comprising a plurality of holes therein extending toward said substrate and configured to concurrently receive the same source signal at a plural number of the holes;

an electronic processor also formed on said semiconductor substrate and operatively associated with said photon absorbing region to receive therefrom and process said output electrical signal into a processed output, thereby forming a single semiconductor chip that receives the optical source signal and outputs the processed output;

wherein said photon absorbing region and said electronic processor have respective thicknesses that are of the same order of magnitude; and

a cathode region and an anode region operatively associated with said photon absorbing region and reverse biasing circuitry configured to apply a voltage between said cathode and anode regions such that said cathode region is driven to a more positive voltage than said anode region.

2. (Original) The integrated detector/processing circuit of claim 1, wherein the thickness of the photon absorbing region is in the range of 0.5 to 5 micrometers.

3. (Original) The integrated detector/processing circuit of claim 1, wherein the electronic processor comprises an application specific integrated circuit (ASIC) comprising at least one of complementary metal oxide semiconductor (CMOS) devices, bipolar (Bi) devices, and BiCMOS devices.

4.(Original) The integrated detector/processing circuit of claim 1, wherein the photon absorbing region is configured to absorb in excess of 60% of the incident source signal at wavelengths from 800 nm to 900 nm and provide an output electrical signal corresponding thereto.

5. (Original) The integrated detector/processing circuit of claim 1, wherein the photon absorbing region is configured to absorb the incident source signal at an absorption percentage that varies by less than 20% over selected wavelength spans of at least 20 nm of source signal wavelengths from 800 nm to 900 nm.

6. (Original) The integrated detector/processing circuit of claim 1, wherein the photon absorbing region is configured to absorb the incident source signal at an absorption percentage that varies by less than 20% over selected wavelength spans of at least 20 nm of source signal wavelengths from 800 nm to 900 nm.

7. (Original) The integrated detector/processing circuit of claim 1, wherein the photon absorbing region is configured to absorb in excess of 60% of the incident source signal at wavelengths from 800 nm to 900 nm and provide an output electrical signal corresponding thereto

8. (Previously Submitted) The integrated detector/processing circuit of claim 1, further including one or more additional photodetectors formed on said semiconductor substrate and having respective photon absorbing regions receiving respective additional source signals and providing respective output electrical signals corresponding thereto, and one or more additional electronic processors also formed on said semiconductor substrate and

operatively associated with the respective photon absorbing regions of said additional photodetectors to receive therefrom and [procces] process said respective output electrical signals therefrom.

9. (Previously Submitted) The integrated detector/processing circuit of claim 1, wherein the plurality of holes enhances absorption of photons compared to a hole-free but otherwise same photodetector at a range of wavelengths that includes a wavelength of said source signal.

10. (Original) The integrated detector/processing circuit of claim 1, wherein the electronic processor includes one or more types selected from a group consisting of: transimpedance amplifier, signal processing electronics, and routing electronics.

11. (Original) The integrated detector/processing circuit of claim 1, wherein a capacitance associated with the photodetector is decreased compared to an otherwise same photodetector having its anode and cathode regions operatively connected to a conventional bond pad.

12. (Previously Submitted) A photodetector with microstructure-enhanced photoabsorption comprising:

a photon absorbing region having a thickness between 0.5 and 5 micrometers and configured to absorb photons from a source signal modulated for data communication and provide an output electrical signal corresponding thereto;

said photon absorbing region comprising silicon with a plurality of holes extending through at least a portion of the thickness of the photon absorbing region and configured to concurrently receive the same source signal at a plural number of the holes; and

said photon absorbing region being configured to absorb in excess of 40% of the incident source signal at wavelengths in at least one of the ranges from 800 nm to 900 nm and from 1400 nm to 1700 nm and provide an output electrical signal

corresponding thereto.

13. (Original) The photodetector of claim 12, wherein the photon absorbing region is configured to absorb in excess of 40% of the incident source signal at wavelengths from 800 nm to 900 nm and provide an output electrical signal corresponding thereto.

14. (Original) The photodetector of claim 12, wherein the photon absorbing region is configured to absorb in excess of 50% of the incident source signal at wavelengths from 800 nm to 900 nm and provide an output electrical signal corresponding thereto.

15. (Original) The photodetector of claim 12, wherein the photon absorbing region is configured to absorb the incident source signal at an absorption percentage that varies by less than 20% over wavelength spans of at least 20 nm of source signal wavelengths from 800 nm to 900 nm.

16. (Original) The photodetector of claim 12, wherein each hole has a cross-section parallel to the upper surface of the substrate and has a [maxium] maximum dimension of between 400 nm and 2500 nm, and each hole has a center that is spaced apart by less than 3500 nm from a center of a nearest adjacent hole of the plurality of holes.

17. (Previously Submitted) The photodetector of claim 12, wherein the photodetector comprises a reflecting structure configured to cause multiple reflections of the source signal thereby traversing the photon absorbing region with said source signal multiple times.

18. (Previously Submitted) A photodetector with microstructure-enhanced photoabsorption comprising:

a cathode region;

an anode region;

reverse biasing circuitry configured to apply a voltage between said cathode and anode regions such that said cathode region is driven to a more positive voltage than said anode region;

a substrate material having an upper surface; and

a photon absorbing region comprising silicon, operatively associated with the cathode and anode regions, and configured to absorb photons from a source signal, said absorbing region including a plurality of holes each having a cross section parallel to the upper substrate surface having a maximum dimension of between 400 nm and 2500 nm, and each hole having a center that is spaced apart by less than 3500 nm from a center of a nearest adjacent hole of the plurality of holes.

19. (Original) The photodetector of claim 18 wherein the source signal has a wavelength that is greater than 800 nm and less than 1000 nm.

20. (Original) The photodetector according to claim 18 wherein the plurality of holes are arranged into a periodically-spaced array.

21. (Original) The photodetector according to claim 20 wherein the periodically-spaced array has a hexagonal or square lattice pattern.

22. (Previously Submitted) The photodetector according to claim 18 wherein the plurality of holes enhances absorption of photons compared to a hole-free but otherwise same photodetector at a range of wavelengths that includes a wavelength of said source signal.

23. (Previously Submitted) The photodetector according to claim 18 wherein each of the holes has a predominately circular cross-section parallel to the upper substrate surface.

24. (Original) The photodetector according to claim 18 wherein the cathode and anode regions are operatively connected to integrated circuit electronics and the photodetector and integrated circuit electronics are integrated into a single silicon chip.

25. (Original) The photodetector according to claim 24 wherein the integrated circuit electronics includes one or more types selected from a group consisting of: transimpedance amplifier, signal processing electronics and routing electronics.

26. (Original) The photodetector according to claim 18 wherein said photodetector is configured to detect said source signal at a data bandwidth of greater than 2.5 gigabits per second at source signal wavelengths of 850 nanometers with a quantum efficiency of at least 30%.

27. (Original) The photodetector according to claim 18 wherein said photodetector is configured to detect said source signal at a data bandwidth of greater than 2.5 gigabits per second at source signal wavelengths of 850 nanometers with a quantum efficiency of at least 50%.

28. (Original) The photodetector according to claim 18 wherein said photodetector is configured to detect said source signal at a data bandwidth of greater than or equal to 5 gigabits per second, at source signal wavelengths of 850 nanometers with a quantum efficiency of at least 30%.

29. (Original) The photodetector according to claim 18 wherein said photodetector is configured to detect said source signal at a data bandwidth of greater than or equal to 5 Gb/s, at source signal wavelengths of 850 nanometers with a quantum efficiency of at least 50%.

30. (Original) The photodetector according to claim 18 further including a substrate and wherein the cathode, absorbing and anode regions are formed above the

substrate and the photodetector is configured to receive the source signal from directions facing a side of the photodetector opposite of the substrate.

REMARKS

This Second Preliminary Amendment submits the claims that were filed on November 20, 2015. The intent is to remove any uncertainty as to what claims are pending that may have arisen because of the filing of a substitute specification on July 1, 2016.

Applicants thank the Examiner for scheduling a telephone interview with their undersigned representative for Wednesday, September 28, 2016, 1 PM.

The Patent Office is hereby authorized to charge any fees that are required in connection with this amendment and to credit any overpayment to our Deposit Account No. 03-3125.

Respectfully submitted,

/Ivan S. Kavrukov/
Ivan S. Kavrukov, Reg. No. 25,161
Attorney for Applicant
COOPER & DUNHAM LLP
30 Rockefeller Plaza, 20th Floor
New York, NY 10112
Tel.: (212) 278-0400

Electronic Acknowledgement Receipt

EFS ID:	27017070
Application Number:	14945003
International Application Number:	
Confirmation Number:	1200
Title of Invention:	MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES
First Named Inventor/Applicant Name:	Shih-Yuan WANG
Customer Number:	23432
Filer:	Ivan Kavrukov/Mary Ellen Finnegan
Filer Authorized By:	Ivan Kavrukov
Attorney Docket Number:	5176-88184-2
Receipt Date:	23-SEP-2016
Filing Date:	18-NOV-2015
Time Stamp:	14:07:51
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Preliminary Amendment	PreliminaryAmendment.pdf	144960 4d7dfee81904d12b1966f0950158f42a4c190e11	no	8
Warnings:					

Information:	
Total Files Size (in bytes):	144960

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New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

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New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/945,003	11/18/2015	Shih-Yuan WANG	5176-88184-2	1200

23432 7590 09/14/2016

COOPER & DUNHAM, LLP
30 Rockefeller Plaza
20th Floor
NEW YORK, NY 10112

EXAMINER	
RODELA, EDUARDO A	

ART UNIT	PAPER NUMBER
2893	

MAIL DATE	DELIVERY MODE
09/14/2016	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of Non-Compliant Amendment (37 CFR 1.121)	Application No.	Applicant(s)
	14/945,003	WANG ET AL.
	Examiner	Art Unit
	Eduardo A. Rodela	2893

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

The amendment document filed on *01 July 2016* is considered non-compliant because it has failed to meet the requirements of 37 CFR 1.121 or 1.4. In order for the amendment document to be compliant, correction of the following item(s) is required.

THE FOLLOWING MARKED (X) ITEM(S) CAUSE THE AMENDMENT DOCUMENT TO BE NON-COMPLIANT:

- ☐ 1. Amendments to the specification:
  - ☐ A. Amended paragraph(s) do not include markings.
  - ☐ B. New paragraph(s) should not be underlined.
  - ☐ C. Other _____.
- ☐ 2. Abstract:
  - ☐ A. Not presented on a separate sheet. 37 CFR 1.72.
  - ☐ B. Other _____.
- ☐ 3. Amendments to the drawings:
  - ☐ A. The drawings are not properly identified in the top margin as "Replacement Sheet," "New Sheet," or "Annotated Sheet" as required by 37 CFR 1.121(d).
  - ☐ B. The practice of submitting proposed drawing correction has been eliminated. Replacement drawings showing amended figures, without markings, in compliance with 37 CFR 1.84 are required.
  - ☐ C. Other _____.
- ☒ 4. Amendments to the claims:
  - ☐ A. A complete listing of all of the claims is not present.
  - ☐ B. The listing of claims does not include the text of all pending claims (including withdrawn claims)
  - ☒ C. Each claim has not been provided with the proper status identifier, and as such, the individual status of each claim cannot be identified. Note: the status of every claim must be indicated after its claim number by using one of the following status identifiers: (Original), (Currently amended), (Canceled), (Previously presented), (New), (Not entered), (Withdrawn) and (Withdrawn-currently amended).
  - ☐ D. The claims of this amendment paper have not been presented in ascending numerical order.
  - ☐ E. Other: _____.
- ☐ 5. Other (e.g., the amendment is unsigned or not signed in accordance with 37 CFR 1.4):

  _____

For further explanation of the amendment format required by 37 CFR 1.121, see MPEP § 714.

TIME PERIODS FOR FILING A REPLY TO THIS NOTICE:

1. Applicant is given **no new time period** if the non-compliant amendment is an after-final amendment or an amendment filed after allowance. If applicant wishes to resubmit the non-compliant after-final amendment with corrections, the **entire corrected amendment** must be resubmitted.
2. Applicant is given **two months** from the mail date of this notice to supply the correction, if the non-compliant amendment is one of the following: a preliminary amendment, a non-final amendment (including a submission for a request for continued examination (RCE) under 37 CFR 1.114), a supplemental amendment filed within a suspension period under 37 CFR 1.103(a) or (c), and an amendment filed in response to a *Quayle* action. If any of above boxes 1. to 4. are checked, the correction required is only the **corrected section** of the non-compliant amendment in compliance with 37 CFR 1.121.

   Extensions of time are available under 37 CFR 1.136(a) only if the non-compliant amendment is a non-final amendment or an amendment filed in response to a *Quayle* action.

   Failure to timely respond to this notice will result in:
   Abandonment of the application if the non-compliant amendment is a non-final amendment or an amendment filed in response to a *Quayle* action; or
   Non-entry of the amendment if the non-compliant amendment is a preliminary amendment or supplemental amendment.

/Eduardo A. Rodela/ Primary Examiner, Art Unit 2893	

Electronic Acknowledgement Receipt

EFS ID:	26605520
Application Number:	14945003
International Application Number:	
Confirmation Number:	1200
Title of Invention:	MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES
First Named Inventor/Applicant Name:	Shih-Yuan WANG
Customer Number:	23432
Filer:	Ivan Kavrukov/maria arap
Filer Authorized By:	Ivan Kavrukov
Attorney Docket Number:	5176-88184-2
Receipt Date:	10-AUG-2016
Filing Date:	18-NOV-2015
Time Stamp:	16:20:54
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Transmittal Letter	IDS_88184-2.pdf	175325 831bc9e31ad790f73ff7b0d8b6e966cebdfe0713	no	1
Warnings:					

Information:	
Total Files Size (in bytes):	175325

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National Stage of an International Application under 35 U.S.C. 371

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New International Application Filed with the USPTO as a Receiving Office

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Dkt. 5176/88184-2

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application of: Shin-Yann WANG et al.

Application No.: 14/945,003 Date Filed: November 18, 2015

For: MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES

This correspondence is being filed electronically with the U.S. Patent and Trademark Office via EFS-Web.

Maria Arap August 10, 2016

Maria Arap Date

30 Rockefeller Plaza, 20th Floor
New York, New York 10112
Tel.: (212) 278-0400

INFORMATION DISCLOSURE STATEMENT

Applicants hereby advise the Examiner of several co-pending applications with related subject matter:

1. Ser. No. 14/947,718, filed November 20, 2015 as a continuation of PCT/US14/39208 (of which the subject application is a national stage filing);
2. Ser. No. 14/943,898 filed November 17, 2015;
3. Ser. No.14/892,821, filed November 20, 2015; and
4. International Application Number PCT/US15/61120 filed November 17, 2015.

No fees are believed to be required in connection with this filing. Nevertheless, the Patent Office is hereby authorized to charge any fees that are required for consideration of this Information Disclosure Statement, and to credit any overpayment during prosecution of this application, to our Deposit Account No. 03-3125.

Respectfully submitted,

Ivan Kavrukov, Reg. No. 25,161
Attorney for Applicant
COOPER & DUNHAM LLP
30 Rockefeller Plaza, 20th Floor
New York, New York 10112
Tel.: (212) 278-0400

Electronic Acknowledgement Receipt

EFS ID:	26394588
Application Number:	14945003
International Application Number:	
Confirmation Number:	1200
Title of Invention:	MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES
First Named Inventor/Applicant Name:	Shih-Yuan WANG
Customer Number:	23432
Filer:	Ivan Kavrukov/MARIA arap
Filer Authorized By:	Ivan Kavrukov
Attorney Docket Number:	2901/88184-2
Receipt Date:	19-JUL-2016
Filing Date:	18-NOV-2015
Time Stamp:	17:41:45
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		88184-2-IDS_1449.pdf	1779515 e9c9f4cc8a98f12dfe7ab8dbca1c79b5b9cd041d	yes	9

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Transmittal Letter	1	2
	Information Disclosure Statement (IDS) Form (SB08)	3	9

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2	Foreign Reference	WO2014190189.pdf	9332029 8df0276e95cd403bd24f11921ba312a16069d3a5	no	139
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3	Foreign Reference	WO2012149441A2.pdf	2328184 6937c323f3253ad600dac44c1be665f3a4afe489	no	49
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4	Foreign Reference	InternationalSearchReportUS1439208.pdf	1047270 1126922de63971c15e73e25d0a7d4c8858048900	no	5
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5	Foreign Reference	2011_12_23_InternationalSearchReportpctus1151091.pdf	457642 f74167be31f4552148a111796026d1c9863de421	no	2
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7	Non Patent Literature	2.pdf	587054 2b37e4a6d454d075829ddf70b8666c268d615b06	no	7
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Information:					
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10	Non Patent Literature	5.pdf	2781147 ac19c8f4dddc8ca2eb021f1621211b5e73c5048b	no	21
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Information:					
11	Non Patent Literature	6.pdf	877250 ef2cafded9fe92eed6183ff255d7e0318ed356c8	no	6
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12	Non Patent Literature	7.pdf	831002 518a53c13d89a326740ee3996a130086fce439cb	no	6
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Information:					
13	Non Patent Literature	8.pdf	392746 f23b46b30fe27cd834c2ec1157e5197615199960	no	5
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Information:					
14	Non Patent Literature	9.pdf	952915 68596fd4137fbab315c39961f1d1011b1ce596fc	no	9
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Information:					
15	Non Patent Literature	10_.pdf	1043986 31c6ddb3e240bd509b6e6a7e29b43d2f14e11528	no	7
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16	Non Patent Literature	11.pdf	301035 530b98ec2763484dad7a927e83d6687f01f0297e	no	3
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17	Non Patent Literature	12.pdf	1303800 dc6cc96fefbb8aeb68287cfb1aa73ba02723f3af	no	2
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18	Non Patent Literature	13.pdf	1225956 cff7eaf39c4fdd3e1ae4824475aef51c2c548181	no	5
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19	Non Patent Literature	14.pdf	292402 ea47e29dd8f49e184ab391285e668306cad0ff81	no	4
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20	Non Patent Literature	15.pdf	1363635 5f44028baa68f4fccf266a49732e777fe73cfe85	no	12
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Information:					
21	Non Patent Literature	16.pdf	698820 46987906877a338b3e5effc520632a25b9ff1067	no	3
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Information:					

22	Non Patent Literature	17.pdf	948471 2d9224f576aee1769d4d32750af1b999d7dee029	no	7
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23	Non Patent Literature	18.pdf	2718429 cf56f3bf186613523ada9f78eb6814631fd9d5d6	no	11
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24	Non Patent Literature	19.pdf	313161 247bd869b79b0958c3d9d34d8f34f018ef9ba340	no	8
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25	Non Patent Literature	20.pdf	214450 54c17565e137d38eaf6b04ab0d7928a8382ae172	no	3
Warnings:					
Information:					
26	Non Patent Literature	21.pdf	1057182 9bcb59e7f21b1ab62bc2d331452c86721c2129ed	no	4
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Information:					
27	Non Patent Literature	22.pdf	1094119 30a825f8365189839607f4535f46e5f222903 9d0a	no	25
Warnings:					
Information:					
28	Non Patent Literature	23.pdf	3165299 77679e25b2a45dbff241680c1597b8ea454e4bad	no	13
Warnings:					
Information:					

29	Non Patent Literature	24.pdf	368732 be9bdd979026ecbfec9913cbf7eac8c0b44f5793	no	8
Warnings:					
Information:					
30	Non Patent Literature	25.pdf	10429125 4dd2c5894fe89311f13ab28515a1dcf9a28d5e04	no	7
Warnings:					
Information:					
31	Non Patent Literature	26.pdf	1652816 5f12b624394b3fc5977f67b1e598f9ae7a8d6c17	no	11
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32	Non Patent Literature	27.pdf	4111503 845b64d5c4d113b79870e20a75791976ddaa958b	no	62
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33	Non Patent Literature	28.pdf	395642 d4c399a50a983a43d35ab650f2ffd7e931f5ce53	no	4
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Information:					
34	Non Patent Literature	29.pdf	426007 f949397b0736269cf4884016456a06c923d4b2dd	no	7
Warnings:					
Information:					
		Total Files Size (in bytes):	58111502		

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PATENT COOPERATION TREATY

PCT

INTERNATIONAL SEARCH REPORT

(PCT Article 18 and Rules 43 and 44)

Applicant's or agent's file reference SYR 2001/66514-PCT	FOR FURTHER ACTION	see Form PCT/ISA/220 as well as, where applicable, item 5 below.
International application No. PCT/US14/39208	International filing date *(day/month/year)* 22 May 2014 (22.05.2014)	(Earliest) Priority Date *(day/month/year)* 22 May 2013 (22.05.2013)
Applicant Shih-Yuan Wang		

This international search report has been prepared by this International Searching Authority and is transmitted to the applicant according to Article 18. A copy is being transmitted to the International Bureau.

This international search report consists of a total of 5 sheets.

☐ It is also accompanied by a copy of each prior art document cited in this report.

1. **Basis of the report**

a. With regard to the **language**, the international search was carried out on the basis of:

☒ the international application in the language in which it was filed.

☐ a translation of the international application into _____ which is the language of a translation furnished for the purposes of international search (Rules 12.3(a) and 23.1(b)).

b. ☐ This international search report has been established taking into account the **rectification of an obvious mistake** authorized by or notified to this Authority under Rule 91 (Rule 43.6*bis*(a)).

c. ☐ With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, see Box No. I.

2. ☐ **Certain claims were found unsearchable** (see Box No. II).

3. ☒ **Unity of invention is lacking** (see Box No. III).

4. With regard to the **title**,

☒ the text is approved as submitted by the applicant.

☐ the text has been established by this Authority to read as follows:

5. With regard to the **abstract**,

☒ the text is approved as submitted by the applicant.

☐ the text has been established, according to Rule 38.2, by this Authority as it appears in Box No. IV. The applicant may, within one month from the date of mailing of this international search report, submit comments to this Authority.

6. With regard to the **drawings**,

a. the figure of the **drawings** to be published with the abstract is Figure No. 10B

☐ as suggested by the applicant.

☒ as selected by this Authority, because the applicant failed to suggest a figure.

☐ as selected by this Authority, because this figure better characterizes the invention.

b. ☐ none of the figures is to be published with the abstract.

International application No.
PCT/US14/39208

Box No. II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. ☐ Claims Nos.:
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:

3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box No. III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:
See Extra Sheet.

1. ☐ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.

2. ☐ As all searchable claims could be searched without effort justifying additional fees, this Authority did not invite payment of additional fees.

3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:

4. ☒ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:
1-49

Remark on Protest

☐ The additional search fees were accompanied by the applicant's protest and, where applicable, the payment of a protest fee.

☐ The additional search fees were accompanied by the applicant's protest but the applicable protest fee was not paid within the time limit specified in the invitation.

☐ No protest accompanied the payment of additional search fees.

International application No.
PCT/US14/39208

A. CLASSIFICATION OF SUBJECT MATTER
IPC(8) - H01L 31/02, 31/0352, 31/107 (2014.01)
CPC - H01L 29/0603, 29/0626, 31/107
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC(8) Classification(s): H01L 31/00, 31/02, 31/0236, 31/0352, 31/036, 31/072, 31/0224, 31/107 (2014.01)
CPC Classification(s): H01L 29/02, 29/04, 29/06, 29/0603, 29/0626, 29/66113, 29/0665, 31/107; B82Y 20/00

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
MicroPatent (US Granted, US Applications, EP-A, EP-B, WO, JP, DE-G, DE-A, DE-T, DE-U, GB-A, FR-A); ProQuest (Derwent, INSPEC, NTIS, PASCAL, Current Contents Search, Dissertation Abstracts Online, Inside Conferences); IP.com; Google Scholar; KEYWORDS: microstructure*, photoabsorption, nano*, photovoltaic*, cathode*, anode*, silicon, germanium, III-V, photodiode*, reverse*, bias*

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X — Y	US 2008/0218740 A1 (WILLIAMS, R et al.) September 11, 2008; abstract; figures 1-2D, 4, and 15; paragraphs [0037, 0060, 0067, 0070]	1-6, 8-10, 16, 17, 21, 28, 30, 31, 33-36, 40, 41, 43 — 7, 11-15, 18-20, 22, 25-27, 29, 32, 37-39, 42, 44-49
Y	US 2005/0184354 A1 (CHU, J et al.) August 25, 2005; figure 1A; paragraphs [0023, 0024, 0050, 0051, 0053]	7, 29, 39
Y	WO 2012/149441 A2 (CHANG-HASNAIN, C et al.) November 1, 2012; abstract; figure 22, paragraph [0088]	11-15
Y	US 2007/0092192 A1 (ACHOUCHE, M et al.) April 26, 2007; abstract; paragraph [0045]	18-20, 22, 25, 26, 38
Y	US 2005/0092925 A1 (ZENTAI, G et al.) May 5, 2005; figure 2A; paragraphs [0016, 0017, and 0020]	27, 44-49
Y	US 7,397,101 B1 (MASINI, G et al.) July 8, 2008; figure 7A; column 7, lines 50-55; column 8, lines 5-20	32, 37

☒ Further documents are listed in the continuation of Box C. ☐

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
27 August 2014 (27.08.2014)	28 NOV 2014
Name and mailing address of the ISA/US Mail Stop PCT, Attn: ISA/US, Commissioner for Patents P.O. Box 1450, Alexandria, Virginia 22313-1450 Facsimile No. 571-273-3201	Authorized officer: Shane Thomas PCT Helpdesk: 571-272-4300 PCT OSP: 571-272-7774

International application No.
PCT/US14/39208

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 4,637,129 A (DERKITS, G, JR et al.) January 20, 1987; abstract; figures 1-7; column 2, lines 24-40	42
A	US 5,457,327 A (TAGUCHI, K) October 10, 1995; abstract; figure 1; column 5, lines 29-35	23, 24
A	US 7,795,064 B2 (PAN, Z et al.) September 14, 2010; abstract; figure 3; column 4, lines 60-66; column 5, lines 1-5	23, 24

International application No.
PCT/US14/39208

-***-Continued from Box III-***-

This application contains the following inventions or groups of inventions which are not so linked as to form a single general inventive concept under PCT Rule 13.1. In order for all inventions to be examined, the appropriate additional examination fee must be paid.

Group I: Claims 1-49 are directed toward a photodetector comprising a cathode, an anode, reverse biasing circuitry, microstructure-enhanced photon absorbing semiconductor material, and a plurality of micro structures.

Group II: Claims 50-53 are directed toward a photovoltaic device comprising a semiconductor material, a plurality of voids within said semiconductor material, and converting solar radiation into direct current electricity.

Group III: Claims 54-58 are directed toward a glass material comprising a plurality of buried voids, said voids dimensioned between 0.01 microns and 1000 microns.

Group IV: Claims 59-62 are directed toward a microwave transmission line structure comprising a semiconductor substrate, a plurality of high-density dielectric-filled voids, reduced dielectric constant, and plurality of metallic microwave transmission lines.

Group V: Claims 63-67 are directed toward an optical wave guide structure comprising an optical mode region, a supporting material, a plurality of microstructured voids in the supporting material, and altering an effective index of refraction.

Group VI: Claims 68-69 are directed toward a heat generating device, a heat sink, a surrounding medium, an intermediate material, a plurality of voids in said intermediate material, and altering the thermal conductivity of said intermediate material.

The inventions listed as Groups I-VI do not relate to a single general inventive concept under PCT Rule 13.1 because, under PCT Rule 13.2, they lack the same or corresponding special technical features. Group I has at least a cathode region, anode region, reverse biasing circuitry, source signal, and a source wavelength that Groups II-VI do not have. Group II has at least converting solar radiation into direct current electricity that Groups I and III-VI do not have. Group III has at least a glass material and dimensioned voided between 0.01 microns and 1000 microns that Groups I, II, and IV-VI do not have. Group IV has at least a dielectric filling, a reduced dielectric constant, and a plurality of metallic microwave transmission lines that Groups I-III, V, and VI do not have. Group V has at least an optical waveguide and an optical mode region that Groups I-IV and VI do not have. Group VI has at least a heat exchanger, a heat generating device, a heat sink, a surrounding medium, an intermediate material, and an altered thermal conductivity that Groups I-V do not have.

The common technical feature of Groups I-VI is at least a plurality of voids. This common feature is disclosed by US 2005/0092925 A1 to Zentai et al. (hereinafter "Zentai"). Zentai discloses a plurality of voids (a photodetector conversion layer includes a plurality of microscopic voids; abstract; figure 2A; paragraph [0016]).

Since the common technical feature is previously disclosed by the Zentai reference, this common feature is not special and so Groups I-VI lack unity.

PTO/SB/08a (01-10)
Approved for use through 07/31/2012. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	14945003
Filing Date	2015-11-18
First Named Inventor	Shih-Yuan WANG et al.
Art Unit	
Examiner Name	not yet assigned
Attorney Docket Number	5176/88184-2

U.S.PATENTS						
Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	4637129		1987-01-20	DERKITS G. JR et al.	
	2	5457327A		1995-10-10	TAGUCHI, K	
	3	7397101		2008-08-07	MASINI, G. et al.	
	4	7795084		2010-09-14	PAN, Z. et al.	
	5	7893348		2011-02-22	Korevan, B	
	6	8129710		2012-03-06	Cho, et al.	
	7	7601597		2009-10-13	Takei, M	
	8	7115971		2006-10-03	Stumbo	

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	14945003
	Filing Date	2015-11-18
	First Named Inventor	Shih-Yuan WANG et al.
	Art Unit	
	Examiner Name	not yet assigned
	Attorney Docket Number	5176/88184-2

	9	7674663		2010-03-09	Suda	

If you wish to add additional U.S. Patent citation information please click the Add button.

U.S.PATENT APPLICATION PUBLICATIONS

Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	20050092925		2005-05-05	ZENTAI, G et al.	
	2	20050184354		2005-08-25	CHU, J et al.	
	3	20070092192		2007-04-26	ACHOUCHE, M et al	
	4	20080216740		2008-09-11	WILLIAMS, R. et al.	
	5	20100193788		2010-08-05	Habib	
	6	20100197068		2010-08-05	Poon	
	7	20100126548		2010-05-27	JANG, ET AL.	
	8	20080265449		2008-10-30	Meinders et al.	

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	14945003
	Filing Date	2015-11-18
	First Named Inventor	Shih-Yuan WANG et al.
	Art Unit	
	Examiner Name	not yet assigned
	Attorney Docket Number	5176/88184-2

	9	20090188557		2009-07-30	Wang, et al.	
	10	20080265449		2008-09-25	Heidari	

If you wish to add additional U.S. Published Application citation information please click the Add button.

FOREIGN PATENT DOCUMENTS

Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2] i	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]
	1	WO2012149441A2	wo		2012-11-01	CHANG-HASNAIN, Connie et al.		☐
	2	PCT/JP2014/39208	JP		2014-11-28	International Search Report		☐
	3	PCT/US1561120	US		2015-11-17	WANG, S		☐
	4	PCT/US1439208	US		2014-05-22	WANG, S		☐
	5	PCT/US15/61120	US		2015-11-17	WANG, S		☐
	6	PCT/US11/51091	US		2011-09-09	WANG, S		☐
	7	WO2012034078	WO		2015-03-05	Wang, S		☐

EFS Web 2.1.17

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	14945003
	Filing Date	2015-11-18
	First Named Inventor	Shih-Yuan WANG et al.
	Art Unit	
	Examiner Name	not yet assigned
	Attorney Docket Number	5176/88184-2

	8	WO2014190189	WO		2014-11-27	Wang, S		☐

If you wish to add additional Foreign Patent Document citation information please click the Add button

NON-PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T§
	1	Ren, R., et al., "Enhanced absorption in elliptical silicon nanowire arrays for solar energy harvesting", Optical Engineering, Vol 53(2), 027102, February, (2014), http://opticalengineering.spiedigitallibrary.org/article.aspx?articleid=1828860	☐
	2	Dayal, G., et al, "Broadband infrared metamaterial absorber with visible transparency using ITO as ground plane", OPTICS EXPRESS 15104 June (2014).	☐
	3	Donnelly, J. L., et al., "Mode-based analysis of silicon nanohole arrays for photovoltaic applications," Vol. 22, No. S5, OPTICS EXPRESS, A1343 25, August (2014).	☐
	4	Gasca, L., "From O to L: The Future of Optical-Wavelength Bands," BROADBAND PROPERTIES," June, (2008) www.broadbandproperties.com	☐
	5	Finisar, "World's Largest Supplier of Optical Solutions for the Communications Industry," http://files.shareholder.com/downloads/FNSR/0x0x382377/0b3893ee-fb06-417d-ac71-84f2f9084b0d/Finisar_Investor_Presentation.pdf.)	☐
	6	Silvaco., "Investigation of the SiGe Waveguide Phototides Using FDTD Method for High Speed Optical Communication," Simulation Standard, http://www.silvaco.com/tech_lib_TCAD/simulationstandard/2010/apr_may_jun/a1/a1.html)	☐
	7	Kolodzey, J., et al, "Optical and electronic properties of SiGeC alloys grown on Si substrates," Journal of Crystal Growth 157, 386-391, (1995).	☐
	8	Kraus, T.F., "Slow light in photonic crystal waveguides," Journal of Physics D: Applied Physics, Vol. 40, (2007).	☐

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	14945003
	Filing Date	2015-11-18
	First Named Inventor	Shih-Yuan WANG et al.
	Art Unit	
	Examiner Name	not yet assigned
	Attorney Docket Number	5176/88184-2

	9	Liu, A., et al., "Quantum dot lasers for silicon photonics [invited]," Photonics Research, Vol. 3, No. 5, October, (2015).	☐
	10	Liu, N., et al, "Infrared Perfect Absorber and Its Application As Plasmonic Sensor," Nano Lett. 10, 2342–2348, (2010).	☐
	11	Kang, Y., "Monolithic Ge/Si Avalnache Photodiodes," 978-1-4244-4403, IEEE, (2009).	☐
	12	Liu, A.Y., et al., Quantum Dot Lasers on Silicon," aUCSB Materials Department, Santa Barbara, California, USA, bUCSB Department of Electrical and Computer Engineering, Santa Barbara, California, USA	☐
	13	Logeeswaran, V.J., "A 14-ps full width at half maximum high-speed photoconductor fabricated with intersecting InP nanowires on an amorphous surface," Applied Physics A, Vol. 91, 1-5., (2008).	☐
	14	Hu, L., et al. "Analysis of Optical Absorption in Silicon Nanowire Arrays for Photovoltaic Applications," NANO LETT. Vol. 7, No. 11, 2007.	☐
	15	Meng, L., et al. "Polarization-sensitive perfect absorbers at near-infrared wavelengths," OPTICS EXPRESS, A111, December, (2012).	☐
	16	Molin, D., "850-950nm WideBand OM4 Multimode Fiber for Next-Generation WDM Systems," OFC (2015).	☐
	17	Piels, et al., "40 GHz Si/Ge uni-traveling carrier waveguide phototiode", Journal of Lightwave Technology, 15908, (2014).	☐
	18	Fountaine, K., et al., "Near-unity broadband absorption designs for semiconducting nanowire arrays via localized radial mode excitation", Vol. 22, No. OPTICS EXPRESS A930, 5 May (2014).	☐
	19	Feng, D., et al, "High-speed Ge photodetector monolithically integrated with large cross-section silicon-on-insulator waveguide," Applied Physics Letters 95, 261105 (2009).	☐

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	14945003
	Filing Date	2015-11-18
	First Named Inventor	Shih-Yuan WANG et al.
	Art Unit	
	Examiner Name	not yet assigned
	Attorney Docket Number	5176/88184-2

	20	Schaub, J.D., et al. "Resonant-Cavity-Enhanced High-Speed Si Photodiode Grown by Epitaxial Lateral Overgrowth," IIEE Photonics Technology Letters, Vol. 11, No. 12, December, 1999.	☐
	21	Seyedi, M.A., et al., "Efficient Schottky-like junction GaAs nanowire photodetector with 9 GHz modulation bandwidth with large active area," APPLIED PHYSICS LETTERS 105, 041105 (2014).	☐
	22	Piatek, S., "Physics and Operation of an MPPC," Tutorials, Hamamatsu Phototonics, November 16, (2015); http://www.hamamatsu.com/us/en/community/optical_sensors/tutorials/physics_of_mppc/index.html?utm_source=googleplus&utm_medium=social&utm_campaign=hc-social	☐
	23	Garnett, E., "Light Trapping in Silicon Nanowire Solar Cells", Nano Letters, (2010) pg. 10, 1082–1087.	☐
	24	Tanus et al.: "High-performance 1200-nm InGaAs and 1300- nm InGaAsN quantum-well lasers by metalorganic chemical vapor deposition," Selected Topics in Quantum Electronics, IEEE Journal of SELECTED TOPICS IN QUANTUM ELECTRONICS, Vol. 9, Issue: 5 (2003).	☐
	25	Kelzenberg, et al., "Enhanced absorption and carrier collection in Si wire arrays for photovoltaic applications. Nature Materials, Vol. 9, March (2010), pg. 239-244. http://authors.library.caltech.edu/17988/	☐
	26	Lin, et al., "Optical absorption enhancement in silicon nanowire and nanohole arrays for photovoltaic applications," Proceeding of SPIE, Vol. 772, 77721G-1, (2010).	☐
	27	Chang-Hasnain, C., et al., "High contrast gratings for integrated optoelectronics, Advances in Optics and Photonics Vol. 4, (2012), pg. 379-440. http://www.eecs.berkeley.edu/Pubs/TechRpts/2014/EECS-2014-197.html	☐
	28	Chu, H-J ,et al , "Wurtzite InP nanowire arrays grown by selective area MOCVD," Phys. Status Solidi Vol. C 7, No. 10, (2010), pg. 2494 – 2497.	☐
	29	Kang et al., "Epitaxially-grown Ge/Si avalanche photodiodes for 1.3μm light detection," OPTICS EXPRESS 9365, Vol. 16, No. 13, June 23, 2008.	☐
	30	International Search Report dated November 28, 2014 in PCT/US2014/59208.	☐

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	14945003
	Filing Date	2015-11-18
	First Named Inventor	Shih-Yuan WANG et al.
	Art Unit	
	Examiner Name	not yet assigned
	Attorney Docket Number	5178/88184-2

	31	International Search Report dated December 23, 2011 in PCT/US2011/051091.	☐

If you wish to add additional non-patent literature document citation information please click the Add button

EXAMINER SIGNATURE

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

PATENT COOPERATION TREATY

PCT

INTERNATIONAL SEARCH REPORT

(PCT Article 18 and Rules 43 and 44)

Applicant's or agent's file reference [illegible]/83310-PCT	FOR FURTHER ACTION	see Form PCT/ISA/220 as well as, where applicable, item 5 below.
International application No. PCT/US2011/051091	International filing date *(day/month/year)* 09 September 2011	(Earliest) Priority Date *(day/month/year)* 10 September 2010
Applicant [illegible] WANG, SHIH-PING		

This international search report has been prepared by this International Searching Authority and is transmitted to the applicant according to Article 18. A copy is being transmitted to the International Bureau.

This international search report consists of a total of 9 sheets.

☐ It is also accompanied by a copy of each prior art document cited in this report.

1. **Basis of the report**

   a. With regard to the **language**, the international search was carried out on the basis of:

   ☒ the international application in the language in which it was filed.

   ☐ a translation of the international application into _____ which is the language of a translation furnished for the purposes of international search (Rules 12.3(a) and 23.1(b)).

   b. ☐ This international search report has been established taking into account the **rectification of an obvious mistake** authorized by or notified to this Authority under Rule 91 (Rule 43.6*bis*(a)).

   c. ☐ With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, see Box No. I.

2. ☐ **Certain claims were found unsearchable** (see Box No. II).

3. ☐ **Unity of invention is lacking** (see Box No. III).

4. With regard to the **title**,

   ☒ the text is approved as submitted by the applicant.

   ☐ the text has been established by this Authority to read as follows:

5. With regard to the **abstract**,

   ☒ the text is approved as submitted by the applicant.

   ☐ the text has been established, according to Rule 38.2, by this Authority as it appears in Box No. IV. The applicant may, within one month from the date of mailing of this international search report, submit comments to this Authority.

6. With regard to the **drawings**,

   a. the figure of the drawings to be published with the abstract is Figure No. 4

   ☒ as suggested by the applicant.

   ☐ as selected by this Authority, because the applicant failed to suggest a figure.

   ☐ as selected by this Authority, because this figure better characterizes the invention.

   b. ☐ none of the figures is to be published with the abstract.

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2011/051091

A. CLASSIFICATION OF SUBJECT MATTER
IPC(8) - H01L 31/00 (2011.01)
USPC - 136/255
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC(8) - H01L 31/00, H01L 31/042, and H02N 6/00 (2011.01)
USPC - 136/244, 136/251, and 136/255

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
MicroPatent, Google Patent, and ACM

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 2008/0047604 A1 (KOREVAAR et al) 28 February 2008 (28.02.2008) entire document	1-45
Y	US 2010/0193768 A1 (HABIB) 05 August 2010 (05.08.2010) entire document	1-45
Y	US 2010/0197068 A1 (POON et al) 05 August 2010 (05.08.2010) entire document	9-10 and 17
Y	US 2009/0267049 A1 (CHO et al) 29 October 2009 (29.10.2009) entire document	11, 18, 20-21
Y	US 2010/0126548 A1 (JANG et al) 27 May 2010 (27.05.2010) entire document	12
Y	US 2008/0102582 A1 (TAKEI) 01 May 2008 (01.05.2008) entire document	23, 30-33
Y	US 7,115,971 B2 (STUMBO et al) 03 October 2006 (03.10.2006) entire document	24
Y	US 2008/0265449 A1 (MEINDERS et al) 30 October 2008 (30.10.2008) entire document	32
Y	US 2007/0190434 A1 (SUDA) 16 August 2007 (16.08.2007) entire document	26-29
Y	US 2009/0188557 A1 (WANG et al) 30 July 2009 (30.07.2009) entire document	34-38
Y	US 2008/0265449 A1 (HEIDARI) 25 September 2008 (25.09.2008) entire document	39-45

☐ Further documents are listed in the continuation of Box C. ☐

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
09 December 2011	23 DEC 2011
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Application of: Shih-Yuan WANG et al.

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For: MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES

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Maria Arap — July 19, 2016

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INFORMATION DISCLOSURE STATEMENT

Pursuant to 37 C.F.R. 1.97(b)(3), this Information Disclosure Statement is being filed before the mailing of a first Office action on the merits. It is respectfully requested that the information cited in annexed Form PTO-SB/08a be considered by the Examiner in connection with the above-identified patent application, and be made of record in said application.

The above-identified application is a continuation of International Application PCT/US14/39208. One or more of the items listed on the annexed Form PTO-SB/08a was cited in the International Search Report (copy enclosed herewith) in connection with International Applications No. PCT/US14/39208 and PCT/US2011/51091 or U.S. Application SN 13/821,963.

The following co-pending U.S. patent applications are also brought to the attention of the examiner:

(a) U.S. Application Ser. No. 13/821,963 filed October 22, 2013;

(b) U.S. Application Ser. No. 14/943,898 filed November 17, 2015;

(c) U.S. Application Ser. No. 14/947,718 filed November 20, 2015;

(d) U.S. Application Ser. No. 14/892,821 filed November 20, 2015;

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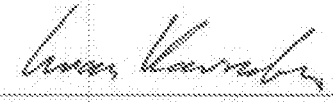
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The citation of the listed items is not a representation that they constitute a complete or exhaustive listing of the relevant art or that these items are prior art. The filing of this Information Disclosure Statement is not an admission that the information cited herein is, or is considered to be, material to patentability as defined in 37 C.F.R. §1.56(b).

Pursuant to 37 C.F.R. §1.98, copies are submitted herewith for only references listed on the annexed Form PTO-1449 that are not a U.S. patent or U.S. patent application publication.

No fees are believed to be required in connection with this filing. Nevertheless, the Patent Office is hereby authorized to charge any fees that are required for consideration of this Information Disclosure Statement, and to credit any overpayment during prosecution of this application, to our Deposit Account No. 03-3125.

Respectfully submitted,



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(54) **Title**: MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES

(57) **Abstract**: Techniques for enhancing the absorption of photons in semiconductors with the use of microstructures are described. The microstructures, such as pillars and/or holes, effectively increase the effective absorption length resulting in a greater absorption of the photons. Using microstructures for absorption enhancement for silicon photodiodes and silicon avalanche photodiodes can result in bandwidths in excess of 10 Gb/s at photons with wavelengths of 850 nm, and with quantum efficiencies of approximately 90% or more.

MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES

REFERENCE TO RELATED APPLICATIONS

[0001] This patent application claims the priority of and incorporates by reference each of the following applications:

U.S. Prov. Ser. No. 61/826,446 filed May 22, 2013;

U.S. Prov. Ser. No. 61/834,873 filed June 13, 2013;

U.S. Prov. Ser. No. 61/843,021 filed July 4, 2013; and

U.S. Prov. Ser. No. 61/905,109 filed November 15, 2013;

The above-referenced provisional patent applications are collectively referenced herein as "the commonly assigned incorporated applications."

FIELD

[0002] The present invention generally relates mainly to photosensitive devices. More particularly, some embodiments relate to photosensitive devices having microstructure enhanced absorption characteristics.

BACKGROUND

[0003] Fiber-optic communication is widely used in applications such as telecommunications and communication within large data centers. Because of attenuation losses associated with using shorter optical wavelengths most fiber-optic communication uses optical wavelengths of 800 nm and longer. Commonly used transmission windows exist between 1260 nm and 1675 nm. A main component of optical receivers used in fiber-optic communication system is the photo detector, usually in the form of a photodiode (PD) or avalanche photodiode (APD).

[0004] High-quality low-noise APDs can be made from silicon. However, while silicon will absorb light in the visible and near infrared range, it becomes more transparent at longer optical wavelengths. Silicon PDs and APDs can be made for optical wavelengths of 800 nm and longer by increasing the thickness of the absorption "I" region of the device. FIG. 2 is a cross section of a conventional PIN photodiode 200, where "d" is the length of the absorption "I" region 220. FIGs. 3A and 3B show bandwidth and quantum efficiency a conventional silicon photodiode

with a 30-micron diameter at 850 nm optical wavelength. As can be seen, in order to obtain a quantum efficiency of 90% the thickness "d" of the "I" region is over 30 microns. This leads to a maximum bandwidth of less than 2.5 Gb/s, which is too low for many current and future telecom and data center applications.

[0005] To avoid the inherent problem that silicon PDs and APDs have with longer wavelengths and higher bandwidths, other materials are used. Germanium (Ge) detects infrared out to a wavelength of 1700 nm, but has relatively high multiplication noise. InGaAs can detect out to longer than 1600 nm, and has less multiplication noise than Ge but still has far greater noise than silicon. InGaAs is known to be used as the absorption region of a heterostructure diode, most typically involving InP as a substrate and as a multiplication layer. This material system is compatible with an absorption window of roughly 900 to 1700 nm. However both InGaAs and Ge devices are relatively expensive and have relatively high multiplication noise when compared with silicon.

[0006] The subject matter claimed herein is not limited to embodiments that solve any specific disadvantages or that operate only in environments such as those described above. Rather, this background is only provided to illustrate one exemplary technology area where some embodiments described herein may be practiced.

SUMMARY

[0007] According to some embodiments, a photodetector with microstructure-enhanced photoabsorption is described. The photodetector (e.g. photodiode or avalanche photodiode) includes: a cathode region; an anode region; reverse biasing circuitry configured to apply a voltage between the cathode and anode regions such that the cathode region is driven to a more positive voltage than the anode region; and a microstructure-enhanced photon absorbing semiconductor region configured to absorb photons from a source signal. The absorbing region includes a plurality of microstructures that are dimensioned and positioned to increase absorption of photons at a range of wavelengths that includes a wavelength of the source signal. According to some embodiments the microstructures have at least one dimension that is equal to or shorter than a longest signal wavelength. According to some embodiments the microstructures

are pillars, holes and/or voids. The microstructures can be arranged into a periodically-spaced array, a non-periodically-spaced array, a randomly-spaced array or a multiperiodically-spaced array. According to some embodiments the microstructures have a major longitudinal axis that is normal to the upper surface of the underlying substrate material. According to some other embodiments, the microstructures have major longitudinal axes that are not parallel to one another. According to some embodiments, the microstructures are oriented so as to reduce sensitivity to any single direction of the source signal.

[0008] According to some embodiments, the microstructures increase absorption at least in part by forming an absorbing mode high contrast grating that makes use of resonance effects, scattering effects, near field effects, sub-wavelength effects, and/or interference effects.

[0009] According to some embodiments, the absorbing region and the microstructures are formed of silicon. According to some embodiments, a silicon photodiode is provided that can detect source signals at a data bandwidth of greater than 5 gigabits per second, at wavelengths of 850 nanometers with a quantum efficiency of at least 60%. According to some embodiments, a silicon photodiode is provided that can detect source signals at a data bandwidth of greater than 10 gigabits per second, at signal wavelengths of 850 nanometers with a quantum efficiency of at least 60%. According to some embodiments a silicon avalanche photodiode is provided that can detect source signals at a data bandwidth of greater than 5 gigabits per second, at wavelengths of 850 nanometers, while having a gain of greater than 2. According to some embodiments a silicon APD has a multiplication region with microstructures that extend into the P multiplication layer, N multiplication layer and/or charge layer. According to some embodiments a silicon photodiode is provided that can detect source signals at a data bandwidth of greater than 1 gigabit per second, at wavelengths of 980 nanometers with a quantum efficiency of at least 40%. According to some embodiments a silicon photodiode is provided that can detect source signals at a data bandwidth of greater than 0.5 gigabits per second, at wavelengths of 1000 nanometers with a quantum efficiency of at least 30%. According to some embodiments, the microstructures effectively reduce

capacitance of the photodetector when compared to a microstructure-free device having a similar photon absorbing length.

[0010] According to some embodiments, the absorbing semiconductor region and the microstructures are formed of silicon and germanium. According to some embodiments, the microstructures are formed by etching away portions of silicon and using a selective area growth process to grow germanium in the etched away portions. According to some embodiments, the absorbing semiconductor region and the microstructures are formed of germanium. According to some embodiments, the photo detector is configured to receive the source signal from the substrate-side. The anode region can include a germanium P layer formed by an epitaxial lateral overgrowth process. The device can be configured such that the source signal to passes through the absorbing region a first time, reflects from a surface and thereafter passes through the absorbing region a second time. The device can also be configured to receive the source signal the top-side and the anode region can be made of a silicon P layer. According to some embodiments, a avalanche photodiode is provided that detects source signals at a data bandwidth of greater than 1 gigabit per second, at source signal wavelengths of 1750 nanometers or shorter, and having a gain of greater than 2. According to some embodiments, the absorbing semiconductor region and the microstructures are formed of III-V family material(s) such as InP, GaAs, InGaAs, GaN, InGaN, InGaAsP, AlGaAs, AlGaN, GaP, InSb or InAs.

[0011] According to some embodiments, the microstructures include voids buried within the absorbing semiconductor region. According to some embodiments, voids are buried in a layer of material so as to effectively lower the refractive index at the signal wavelength(s) and as well as lower the capacitance of the layer of material.

[0012] According to some embodiments, a photovoltaic device is described that includes a semiconductor material having a plurality of voids buried therein. The semiconductor material being configured to convert solar radiation into direct current electricity. According to some embodiments, the voids are microstructured voids and are configured to enhance absorption of the semiconductor material thereby increasing conversion efficiency of the device. According to some embodiments, the voids are sized and/or spaced apart by less than 3 microns, and

are configured to alter an effective refractive index of the semiconductor material near a surface, for example to reduce reflection of incident sunlight from the device and/or increase internal reflections within the semiconductor material.

[0013] According to some embodiments a glass material is described in which the glass has a plurality of buried voids dimensioned between 0.01 microns to 1000 microns. In some examples the glass forms a part of a photovoltaic device. According to some embodiments, the buried voids are filled with a material gel, polymer and gas. The buried voids can provide flexibility of the glass material, and/or increased resistance of the glass material to physical damage and/or damage propagation.

[0014] According to some embodiments, a microwave transmission line structure is described that includes: a semiconductor substrate material having a plurality of high-density dielectric-filled voids configured to reduce a dielectric constant of the semiconductor substrate material; and a plurality of metallic microwave transmission lines, least one of which is positioned above the semiconductor substrate material. According to some embodiments, the dielectric-filled voids are filled a material such as: nitrogen, argon, vacuum, air, helium, polymer, metal oxides, silicon dioxide, silicon nitride, calcium fluoride, or zinc oxide. According to some embodiments, the voids are further configured to reduce dispersion and reduce loss associated with the microwave transmission lines at least in part by reducing current loop flow and/or eddy currents.

[0015] According to some embodiments, an optical waveguide structure is described that includes: an optical mode region; and a supporting semiconductor material adjacent to the optical mode region. The supporting material includes a plurality of microstructured voids that are configured to alter an effective index of refraction of the supporting material based on the size, shape, density, etc. of the microstructured voids.

[0016] According to some embodiments, a heat exchanger system is described that includes: a heat generating device; a heat sink configured to dissipate heat to a surrounding medium; and an intermediate material mounted between the heat generating device and the heat sink. The intermediate material includes a plurality of buried voids configured to effect thermal conductivity of the intermediate material. According to some embodiments, some of the buried voids are filled with

thermally conductive material and others are filled with a thermally isolating material. The two types of voids being positioned to conduct heat from the heat generating device to the heat sink and to reduce thermal cross talk with other heat sensitive devices mounted on the intermediate material.

BRIEF DESCRIPTION OF THE DRAWINGS

[0017] To further clarify the above and other advantages and features of the subject matter of this patent specification, specific examples of embodiments thereof are illustrated in the appended drawings. It should be appreciated that these drawings depict only illustrative embodiments and are therefore not to be considered limiting of the scope of this patent specification or the appended claims. The subject matter hereof will be described and explained with additional specificity and detail through the use of the accompanying drawings in which:

[0018] FIG. 1 is schematic side cross section of three dimensional micro structures that enhance bulk absorption coefficient in photo sensitive devices, according to some embodiments;

[0019] FIG. 2 is a cross section diagram showing aspects of a typical structure of a conventional PIN photodiode;

[0020] FIGs. 3A and 3B a plots showing bandwidth and quantum efficiency (QE), respectively, of a bulk conventional silicon photodiode versus "d" in microns;

[0021] FIGs. 4A-4D are graphs showing the enhancement of bulk absorption coefficient vs bandwidth and QE for a microstructured Si photodetector, according to some embodiments;

[0022] FIGs. 5A and 5B are cross sections showing aspects of a top illuminated microstructered PIN silicon photodiode, according to some embodiments;

[0023] FIGs. 6A and 6B are cross sections showing aspects of a bottom illuminated microstructered NIP silicon photodiode, according to some embodiments;

[0024] FIGs. 7A and 7B are cross sections showing aspects of a microstructered avalanche photodiode, according to some embodiments;

[0025] FIG. 8 is a cross section showing a silicon epitaxial structure for a high-speed high-efficiency microstructured APD, according to some embodiments;

[0026] FIGs. 9A-9E are a series of cross sections showing some basic microstructure processing steps, for a high-speed APD, according to some embodiments;

[0027] FIGs. 10A-10B are cross sections showing aspects of a top illuminated microstructered photo diodes, avalanche photo diodes and/or photovoltaics (PV) with microstructured voids in N-Si, according to some embodiments;

[0028] FIGs. 11A and 11B are cross sections showing aspects of an heteroepitaxial APD structure of Ge on Si, according to some embodiments;

[0029] FIG. 12 is a cross section illustrating aspects of a passivation method for Ge surfaces on microstructures, according to some embodiments;

[0030] FIGs. 13A and 13B are graphs showing the effects of mictrostructure enhancement of Ge bulk absorption coefficient for photodiodes and/or avalanche photodiodes based on Ge on Si, according to some embodiments;

[0031] FIGs. 14A-14B are cross sections showing aspects of a top-illuminated Ge on Si avalanche photodiode having microstructured pillars/holes, according to some embodiments;

[0032] FIGs. 15A-15D are cross sections illustrating aspects of bottom-illuminated Ge on Si avalanche photodiodes having microstructured pillars/holes, according to some embodiments;

[0033] FIGs. 16A and 16B are graphs comparing single pass and double pass photodiodes and/or avalanche photodiodes based on Ge on Si, according to some embodiments;

[0034] FIGs. 17A-17B are cross sections showing aspects of a top-illuminated Ge on Si photodiode structure having microstructured pillars/holes for applications with signal wavelengths ranging from 700 to 1800 nm, according to some embodiments;

[0035] FIGs. 18A-18B are cross sections showing aspects of a bottom-illuminated Ge on Si photodiode structure having microstructured pillars/holes for applications with signal wavelengths ranging from 1200 to 1800 nm, according to some embodiments;

[0036] FIGs. 19A-19C are diagrams illustrating how mictrostructures can reduce capacitance of a photodiode such that a larger area photo diode can be fabricated with the same bandwidth and QE, according to some embodiments;

[0037] FIGs. 19D-19E are cross sections showing aspects of fabricating an APD device having a III-V absorbing layer grown on a P-I-N silicon multiplication layer, according to some embodiments;

[0038] FIG. 20 shows bulk layers without a final P-Si layer for devices having microstructured Ge buried or embedded in an Si microstructure, according to some embodiments;

[0039] FIG. 21 is a cross section showing etching of microstructured pillars and/or holes for devices having microstructured Ge buried or embedded in an Si microstructure, according to some embodiments;

[0040] FIG. 22 is a cross section showing a device having microstructured Ge buried or embedded in an Si microstructure, after the Ge "I" layer is grown in the etched region and planarized, according to some embodiments;

[0041] FIG. 23 is a cross section showing a device having microstructured Ge buried or embedded in an Si microstructure, after I-Ge regrowth and planarization, and a cap layer of P-Si, according to some embodiments;

[0042] FIGs. 24A - 24B are cross sections showing aspects of a microstructured APD with buried/embedded I-Ge absorbing microstructures in I-Si microstructures, according to some embodiments;

[0043] FIGS. 25A - 25C are cross sections showing aspects of a photodiode having buried/embedded Ge microstructures in a Si microstuctured pillar and/or hole array, according to some embodiments;

[0044] FIGs. 25D - 25E are cross sections showing aspects of a forward biased device such as a vertical cavity surface emitting laser (VCSEL), according to some embodiments;

[0045] FIG. 26 is a cross section showing starting epitaxial layers in which mictrostructured voids are fabricated, according to some embodiments;

[0046] FIG. 27 is a cross section showing microstructured holes/pillars etched into the I-Si layer, according to some embodiments;

[0047] FIG. 28 is a cross section showing microstructured voids buried or embedded in Si with a Si capping P^+ anode layer 2826, according to some embodiments;

[0048] FIG. 29 is a cross section showing Bragg reflectors formed on the P-Si surface to provide a highly reflective mirror, according to some embodiments;

[0049] FIG. 30 shows an example of a PIN PD/PV structure with microstructured voids to enhance absorption, reduce bulk refractive index, reduce capacitance and increase mechanical flexibility of large sheets of PV on semiconductor material, according to some embodiments;

[0050] Fig. 31 is a cross section showing regrown I-Ge with a buried/embedded voids, according to some embodiments;

[0051] Fig. 32 is a cross section showing a device having buried microstructured voids in I-Si with regrown I-Ge and capped by a epitaxial layer, according to some embodiments;

[0052] FIG. 33 is a top view showing distribution of microstructured pillars, holes and/or buried voids in an PD/APD, according to some embodiments;

[0053] FIG. 34 is a top view showing distribution of microstructured pillars, holes and/or buried voids in an PD/APD, according to some other embodiments;

[0054] Fig. 35 shows the basic epitaxial structure for a conventional Si PV/PD diode on N Si substrate;

[0055] FIG. 36 shows microstructured voids incorporated into an N-Si layer, according to some embodiments;

[0056] FIG. 37 is a cross section showing etched Si microstructured pillars/holes with regrown Ge covering the Si, according to some embodiments;

[0057] FIG. 38 is a cross section showing microstructured Si pillars/holes with Ge regrowth on an N-Si layer having embedded microstructured voids, according to some embodiments;

[0058] FIG. 39 is a cross section showing partial coverage I-Ge on microstructured Si pillars/holes, according to some embodiments;

[0059] FIG. 40 is a cross section sowing the basic components for the a microstructured Si-Ge pillar hole array PD/PV and/or APD, according to some embodiments;

[0060] FIGs. 41A-41B are cross sections showing aspects of a microstructured pillar/hole array device above a N-Si layer having buried microstructured voids, according to some embodiments;

[0061] FIGs. 42A-42D are cross sections showing aspects of an APD with microstructured pillar/hole arrays above an N-Si layer having buried microstructured voids, according to some embodiments;

[0062] FIGs. 43-46 are top views illustrating various dimensions, spacings and shapes for microstructured elements, according to some embodiments;

[0063] FIGs. 47-48 are cross sections showing microstructured pillar and hole arrays having varying lengths and depths, according to some embodiments;

[0064] FIG. 49 shows shows a microstructured surface having a combination of both pillars and holes, according to some embodiments;

[0065] FIG. 50 is a cross section of an optical ridge waveguide, according to some embodiments;

[0066] FIG. 51 is a cross section of a buried optical waveguide in silicon using voids, according to some embodiments;

[0067] FIGs. 52 and 53 are a cross section and top view, respectively, of a ridge waveguide integrated with a microstructured PD/APD, according to some embodiments;

[0068] FIGs. 54A and 54B show a microwave transmission line on Si with voids, according to some embodiments;

[0069] FIG. 55 is a cross section of voids for thermal conduction and thermal isolation of heat producing ICs and light emitters, according to some embodiments; and

[0070] FIG. 56 is a cross section showing a distribution of voids to increase lateral path length for increasing lateral electrical resistivity and decrease lateral thermal conduction, according to some embodiments.

DETAILED DESCRIPTION

[0071] A detailed description of examples of preferred embodiments is provided below. While several embodiments are described, it should be understood that the new subject matter described in this patent specification is not limited to any one embodiment or combination of embodiments described herein, but instead encompasses numerous alternatives, modifications, and equivalents. In addition, while numerous specific details are set forth in the following description in order to provide a thorough understanding, some embodiments can be practiced without some or all of these details. Moreover, for the purpose of clarity, certain technical material that is known in the related art has not been described in detail

in order to avoid unnecessarily obscuring the new subject matter described herein. It should be clear that individual features of one or several of the specific embodiments described herein can be used in combination with features or other described embodiments. Further, like reference numbers and designations in the various drawings indicate like elements.

[0072] According to some embodiments, microstructures are used to enhance the bulk absorption constant (also referred to as absorption coefficient) to achieve high quantum efficiency (QE) while maintaining an absorption length suitable for high data rate applications. As used herein, "QE" refers to internal quantum efficiency (IQE). IQE is equal to external quantum efficiency (EQE) in cases where reflection and transmission are negligible.

[0073] According to some embodiments, microstructures are used to improve bulk absorption constant at wavelengths in the proximity of the semiconductor material's band gap. This allows for extending the operating optical wavelengths and/or operating spectrum of the photosensor. The enhanced bulk absorption constant (or coefficient) is called the effective absorption constant (or coefficient). The term "effective" is used since absorption constant or coefficient is an inherent material property. However, with resonance effects, plasmonic effects, field enhancement effects, scattering effects, near field and sub wavelength effects, the effective absorption constant or coefficient can be greater than the bulk or material absorption constant or coefficient. As used herein, the following terms are used interchangeably: enhanced absorption constant, enhanced absorption coefficient; enhanced effective absorption constant; enhanced effective absorption coefficient; enhanced absorption; enhanced effective absorption; and effective absorption constant; and effective absorption coefficient.

[0074] According to some embodiments, enhanced absorption can also have drastic effects on path length. In one bulk absorption example, the path length for the photons to be absorbed to 1/e of its original amplitude is, for example 100 micrometers (μm), whereas under enhanced absorption according to some embodiments, the path length is 1 micrometer for the optical amplitude to decay to 1/e of its original amplitude. Equivalently, if path length is kept constant to one micrometer then the enhanced absorption coefficient is 100 times greater than the bulk absorption coefficient.

[0075] This is seen by the relationship $A= A_0 e^{-\alpha L}$ where A is the decaying amplitude of the incident photon flux A_0 and α is the absorption coefficient and L the path length for absorption to take place. So, rather than have L be 100 times longer, an effective α can be defined such that it is 100 times greater than a non enhanced absorption coefficient such as the bulk absorption coefficient. The resonance/scattering/near field effects of microstructures for example gives the equivalence of the path length that is 100 times longer where the resonant/scattering/near field microstructure is just one micron long. To put it another way, in a very simplistic view, the photons in the resonant structures make 50 round trips before reaching the 1/e value of its original amplitude, so the equivalent linear length is 100 times the length of the resonant structure. For simplicity, resonance/scattering/near field effects will collectively be referred to herein as "resonant" which can include, resonant, scattering, near field, plasmonic, nonlinear and linear optical effects.

[0076] As used herein the terms "microstructures" and "microstructured" refer to: pillars, voids, holes and mesas, of various shapes and sizes having at least one dimension in the micrometer scale, submicrometer scale, and/or sub-wavelength scale.

[0077] According to some embodiments, properties of the microstructures can also be explained as the absorption mode of high contrast grating (HCG) being used to enhance the effective absorption constant/coefficient or enhanced absorption. Conventionally, HCG uses material that is transparent at the optical wavelength of interest. In contrast, according to some embodiments, at least one of the microstructures is absorbing or weakly absorbing at the optical wavelength of interest. According to some embodiments a low-Q absorbing mode HCG enhances absorption (e.g. Q values in the range of 2-200).

[0078] According to some embodiments, a low index material is used such as buried oxide (BOX), silicon on insulator (SOI), silicon on sapphire (SOS), low-density semiconductors such as amorphous semiconductor, nanowire semiconductors, voids and holes to lower the effective refractive index. Refractive index is an inherent property of a material. However, according to some embodiments, when structures such as voids, air gaps, and/or holes (which can be filled with low index material, and/or regrowth) have dimensions on the order of the

optical wavelength, the optical electromagnetic field will see an average refractive index consisting of the material refractive index and the structures (which can be filled by a low refractive index material). This average is referred to herein as the effective refractive index. According to some embodiments, a low index or effective low index material need not be used in the microstructures.

[0079] According to some embodiments, the techniques for enhancing effective absorption can be applied to various materials including: silicon, germanium, III-V material such as InP, GaAs, GaN, InGaAs, and any combination of the III-V material family. As used herein, the term "material family" of a III-V material is defined as any material that is lattice matched or approximately lattice matched (within a few percent) to GaAs, InP, GaN, InSb semiconductors. For example, the InP material family can include InGaAs, InGaAsP, InAlAs. According to some embodiments, in the case of microstructures, regrowth such as selective area growth (SAG) of Ge, InGaAs, or other III-V material in silicon microstructures can be carried out without the detrimental effects of lattice mismatch since the dimension of the footprint of the lattice mismatched material on silicon is small (approximately a few micrometers to sub-micrometers). This allows Ge and other III-V materials to be integrated with silicon without the use of a conventional buffer layer (such as amorphous Ge in the case of Ge on Si growth). The heterogeneous integration of materials can be homo or hetero structures, combination of crystalline and microcrystalline and amorphous semiconductor, conductor such as carbon, graphene, insulator, dielectrics, solid, gaseous, liquid such as glass or polymer that can be semiconducting.

[0080] Due to the microstructures, the capacitance can also be represented by an effective capacitance which is a parallel capacitance of (1) the dielectric constant of one semiconductor, and (2) the dielectric constant of another material, which can be a semiconductor, dielectric, gas, vacuum, partial vacuum, liquid such as glass or polymer (polyimide, mylar, or other organic compound). The effective capacitance of the device is the combination of the capacitance of the parallel capacitors, which can be two or more. An advantage of the use of microstructure according to some embodiments, is that the effective capacitance can be significantly lower than the capacitance of a homogeneous material such as a semiconductor. The lower capacitance allows a device to have a larger area while

still maintaining suitably high data rate bandwidth, and/or increase the data rate bandwidth by reducing the thickness of the device to reduce the transit time.

[0081] According to some embodiments, the photosensor can be a photodiode (PD), avalanche photodiode (APD), photovoltaic (PV) or solar cell, or any optoelectronic device that converts photons to electrons. According to some embodiments, emitters such as lasers and light emitting diodes that convert electrons/holes to photons can also be implemented using microstructures.

[0082] According to some embodiments, the enhanced absorption allows the APD/PD to: (1) extend the sensitivity of the APD/PD to photons with energies (or wavelength) closer to the material band gap with QE greater than 60% and data bandwidth greater than 3 Gb/s; (2) operate at a high data rate bandwidth (e.g. >10 Gb/s), due to shorter absorption length therefore shorter transit time; (3) increase quantum efficiency with enhanced absorption; (4) be manufactured of silicon which has superior APD properties with low excess noise; (5) be compatible with Si Photonics and CMOS processes. According to some embodiments, the PD/APD can be integrated with ASIC (application specific integrated circuits) such as signal processing, signal amplification, memory, cpu, electrical transmitter, optical waveguides, integrated optics, and other ICs for specific applications. This is advantageous for mass production using CMOS foundries.

[0083] According to some embodiments, microstructures such as voids are used to reduce effective refractive index to create resonant structures to enhance the absorption. In microstructures where selective area growth are used to integrate Ge or III-V material with silicon, voids can be made in the silicon microstructure such that the absorbing region is a resonant structure to enhance the effective absorption coefficient by 2 to over 100 times.

[0084] According to some embodiments, silicon is used for avalanche gain. Silicon has the lowest excess noise for an avalanche photodiode. By integrating Ge and/or III-V material with silicon, the absorption takes place in Ge and/or III-V material and the electronic gain occurs in silicon. Depending on the optical wavelengths, for example shorter than 1100 nm, silicon may be used for both absorption and electronic gain with the use of microstructures.

[0085] According to some embodiments, microstructures such as buried voids can reduce lateral electrical and thermal conductivity. In situations where

directional conductivity of electrical or thermal (phonons) is preferred, voids can be used to confine the flow of electrical current and/or heat.

[0086] According to some embodiments, the absorption of photons in semiconductors is enhanced with the use of microstructures. The microstructures can have effects such as resonance, field enhancement, near field and sub wavelength effects, scattering, plasmonics, photonic crystal, absorption mode in high contrast grating at the near field regime, which are both linear and non linear effects that can effectively increase the effective absorption length resulting in a greater absorption of the photons for a given length.

[0087] According to some embodiments, microstructures used for absorption enhancement for silicon photodiodes and silicon avalanche photodiodes can result in silicon PD and APD with bandwidths in excess of 10 Gb/s (or equivalently 6.75 GHz approximately depending of the digital coding format) at photons with wavelengths of 850 nm approximately (which is the current datacom preferred wavelength) with quantum efficiencies of approximately 90% or more.

[0088] Silicon optical detectors are very robust due to the maturity of the material and processing techniques, the surfaces can be easily passivated to eliminate dangling bonds that can cause surface states and carrier recombination centers, they have excellent carrier lifetimes due to low defects and high material purity, and for APD applications, the noise is low due to the small ionization ratio between holes and electrons (k factor, silicon have the lowest k factor than any III-V material) and such detectors are CMOS compatible for integration with electronics for signal processing and with Si photonics.

[0089] According to some embodiments, other material such as germanium, III-V, a-Si (amorphous silicon) may also be used singly or together with other materials such that a multiple bandgap in parallel can be fabricated with enhanced absorption.

[0090] According to some embodiments, microstructures and voids are used to reduce the effective refractive index and capacitance to achieve the absorption mode high contrast grating effect and to reduce the effective capacitance of the device for lower RC time constants.

[0091] In addition, according to some embodiments, microstructures buried in the semiconductor can reduce lateral electrical and thermal conduction. Microwave

transmission lines are possible for example where high-density voids are buried in Si to reduce the dielectric constant and also eddy currents in the semiconductor resulting in low loss and dispersion. Voids can also be used for thermal isolation and to improve thermal conductivity by filling the voids with thermal conductors. This is useful in thermal management of components on a silicon substrate.

[0092] The enhancement using nanowires (Garnett et al, Light trapping in silicon nanowire solar cells, Nano Letters, 2010, 10, 1082-1087; Kelzenberg et al, Enhanced absorption and carrier collection in Si wire arrays for photovoltaic applications, Nature Materials, vol. 9, March 2010, 239-244) and nanoholes (Lin et al, Optical absorption enhancement in silicon nanowire and nanohole arrays for photovoltaic applications, Proceeding of SPIE, Vol. 7772, 77721G-1, 2010) have been reported. Nanowire is known to be used for light trapping in photovoltaic applications where the photogenerated carriers diffuse to the anode or cathode of a P-N junction with zero external bias operating at DC (direct current).

[0093] According to some embodiments, the photogenerated carriers are swept out with an external reverse bias in the absorbing "i" region of a P-I-N diode (PD) or P-I-P-I-N diode (APD) for high modulation bandwidth (greater than or equal to 10 Gb/s bandwidth) and high quantum efficiency and for APD for high current gain, with gain greater than 3 dB.

[0094] The cause or causes of the enhancement of the absorption coefficient are believed to include one or more of the following: an increase in optical field concentration, resonance effects, constructive and destructive optical interferences (amplitude and phase) effects, scattering, and high contrast grating (HCG) effects. See, e.g. Chang-Hasnain et al, High contrast gratings for integrated optoelectronics, Advances in Optics and Photonics 4, 379–440 (2012), hereinafter "Chang-Hasnain." The HCG effects are at the near-wavelength regime (See, Chang-Hasnain) where the optical wavelength in the material of the grating and the optical wavelength in the surrounding material of the grating is the range of the period of the grating.

[0095] FIG. 1 is schematic side cross section of three dimensional micro structures that enhance bulk absorption coefficient in photo sensitive devices, according to some embodiments. Microstructured pillars 110 and/or holes 120 are etched into the "I" Si layer 100. The optical wavelength in material M_1 is λ/n_1 where

n_1 is the refractive index of M_1 and the optical wavelength in material M_2 is given by λ/n_2 where n_2 is the refractive index of material M_2. The center to center distance L of the structures 110 can be between λ/n_1 and λ/n_2 or approximately 100-2000 nm, which is referred to as the near-wavelength regime. The diffraction regime is where L (one cycle) is greater than the wavelength, while the subwavelength regime is where L is less than the wavelength. The cross section of FIG. 1 shows the 3D (dimension) microstructured pillar/hole array, which enhances the bulk film absorption coefficient by factors of 1.5 to over 100. The period of the 3D pillar/hole microstructured array can be seen as a 3D high contrast grating, whose period of the grating Λ can lie between λ/n_1 where n_1 is the optical refractive index of material M_1 and λ/n_2 where n_2 is the optical refractive index of material M_2. If $n_1 > n_2$ then $\lambda/n_1 < \Lambda < \lambda/n_2$ where λ is the optical wavelength of the light to be absorbed by the microstructured pillar/hole array typically in the "I" region of a P-I-N PD or for APD, the absorbing "I" region P-I-P-I-N where the second "I" region is the multiplication region, or the wavelength of the optical signal to be detected by the PD and APD. At this near-wavelength regime of the 3D HCG microstructured pillar/hole array, the resonance Q (quality factor, or proportional to the ratio of the energy stored in the resonator/energy losses per cycle; where it is the optical cycle, the optical frequency impinging on the resonator or in the resonator) can be as high as 10^7 (see, Chang-Hasnain) if the HCG has minimal absorption loss as is known. In addition, in most cases the ratio of the index of the HCG to the surrounding material index need only be approximately 1.1 to observe the effects of the HCG.

[0096] The HCG effect that may explain the high enhancement of the absorption coefficient of the bulk material is that a single or multiple HCG layer (or a single microstructured pillar/hole array layer) due to its resonance effects and/or due to a varying of the microstructured pillar/hole period spacing, the optical signal resonating in the HCG/microstructured pillar-hole array can be directed to propagate in the plane of the HCG/microstructured pillar-hole array rather than normal to the surface. Together with resonance and in-plane propagation this can greatly increase the absorption path length in the HCG/microstructured pillar-hole array. According to some embodiments, the absorbing HCG mode is operated with a reverse voltage bias for PD/APD and a built-in bias (zero applied bias) in photovoltaic devices.

[0097] Using the phenomenon of near-wavelength and also deep-wavelength where the HCG period is much less than the optical wavelength, and the diffraction regime where the HCG period is greater than the optical wavelength (See, Chang-Hasnain) the microstructured pillar-hole-void array can have enhanced absorption coefficient over the bulk absorption coefficient by a factor of 1.1 to over 100.

[0098] According to some embodiments, the HCG effect is also used in the absorbing mode or lossy mode or low Q of 1-10000 (compared with known HCG that are in the non-absorbing mode or non-lossy mode to achieve high Q of greater than 1,000,000 and high reflectivity), in both buried/embedded (not fully buried) Ge microstructures in Si and buried/embedded void microstructures in either Ge or Si to improve the quantum efficiency (QE) and operating wavelength range of Si (400-1100 nm) and Ge (400 to 1800 nm) and Ge on Si photodiodes and avalanche photodiodes operated in a reverse bias mode of the pn, pin, pinip junctions (p and n can be switched for certain device configurations) that can be homo or heterojuction, crystalline or amorphous or any combinations thereof. In addition, the substrate can be on SOI or BOX or voids to reduce the index of refraction or effective index of refraction and the dielectric constant or effective dielectric constant (a dielectric with many voids can be represented as an effective dielectric constant, or equivalently effective capacitance).

[0099] Known silicon photodetectors have been limited to wavelength ranges of 200 to 1000 nm due to indirect bandgap of 1.1 eV. In particular, near the band gap wavelengths of 800-1000 nm, the frequency response of the silicon photodetector to a modulated optical signal at Gb/s rate is limited to 1.5 Gb/s approximately or less due to the weak absorption constant of Si at those wavelengths which are approximately 760 cm^{-1} at 850 nm and 67 cm^{-1} and 63 cm^{-1} at 980 and 1000 nm respectively, resulting in long absorption lengths of material, 30 microns or more, which results in low frequency response for the PD/APD. The wavelengths 850 nm is of interest since this is the standard wavelength for short distance (few meters to a few kilometers) multimode fiber optical datacommunication.

[00100] The amount of incident photons absorbed is approximately given by $\eta=1-e^{-\alpha L}$ where η (also the quantum efficiency if reflection off the surface of the PD is negligible) is the amount absorbed and "α" is α the absorption constant and "L" is the length length of the absorber. Using this equation and the absorption constant

of Si at 850 nm, 90% of the incident photons are absorbed at a depth of approximately 30 μm. Known high speed photodetectors typically have an absorption region of approximately 2 μm in length. The reason for this is that transit time and RC time of the photodiode need to be considered to have a bandwidth of 20 GHz (or approximately 30 Gb/s) or more and still have an external quantum efficiency of 80-90% or better.

[00101] Efficiency and bandwidth (transit and RC time): At a field strength of $6 \cdot 10^4$ V/cm the electron drift velocity is $1 \cdot 10^7$ cm/s at a temperature of 300 K. The 3 dB bandwidth of the photodetector due to transit time is given by: f(3dB)=0.45/t(transit) where t(transit) is the transit time for the carriers to cross the depleted high field region. FIG. 2 is a cross section diagram showing aspects of a typical structure of a PIN photodiode structure. Assuming negligible photocarriers generated in the P region 210 of the PIN 200 and mostly generated in the "i" region 220, the transit time is determined by the electron drift velocity and "d" (the high field "i" region). The PIN 200 is reversed biased (e.g. between -4 and -25 V). The "i" region 220 is fully depleted in this case. The RC time of the PIN structure 200 is determined by the capacitance, which is the ratio of the area ($\pi w^2/4$) of the PIN 220 to d.

[00102] According to conventional techniques, a 30 μm thick absorption layer ('i") to achieve 90% absorption for Si at 850 nm wavelength will give a transit time limited 3dB bandwidth of 1.5 GHz (approximately 2.2 Gb/s) which is too low for many current applications. Many current applications are in the 10-20 Gb/s range and in the near future 40 Gb/s. A d of 2 μm or less is desirable for current high-speed photodiodes in optical datacom applications to give over 30 Gb/s bandwidth.

[00103] RC time is another time to consider in photodiodes (applies to both APD and PD). The 3 dB bandwidth due to RC time is given by $f(RC)= 1/(2\pi RC)$; where C is the capacitance of the photodiode and R is the load resistance which is typically 50 ohms (and occasionally 25 ohms). Capacitance in the case of a conventional PIN structure photodiode with the "i" region fully depleted by the reverse bias, is just a parallel plate capacitance given by $\varepsilon A/d$ where ε is the dielectric constant of the material (multiplied by vacuum permittivity of $8.854 \cdot 10^{-14}$ farads/cm) which is 11.9 for Si, A is the area of the capacitor ($\pi(w/2)^2$), and d is the depleted "i" (i and I are used herein interchangeably). The f(RC) becomes larger

as d increases since the capacitance is decreasing with increasing d and a fixed area, where the diode diameter for example is 30 μm (diameters of high frequency PD/APD range from 5 to 60 μm). Diameter of diode for calculating the RC time is the total capacitive area of the diode that includes the photosensitive area and any metallization that may contribute to the overall capacitance.

[00104] The overall frequency bandwidth of the photodiode is a sum of the squares of the transit time and the RC time. This is given by the equation:

$$f=1/(2\pi(RC)^2+(\tau/2.4)^2)^{1/2}).$$

[00105] FIGs. 3A and 3B are plots showing bandwidth and QE, respectively, of a bulk conventional Silicon photodiode versus "d" in microns. From plots 310 and 312 in FIGs. 3A and 3B, for the combined f(3dB) of the transit time and RC time and the quantum efficiency η (assuming negligible reflection losses) we see that for bulk silicon to reach 10 Gb/s, the quantum efficiency (QE) is less than 40%, for a 30 μm diameter PD, which is too low for most datacom applications.

[00106] According to some embodiments, to overcome the relatively weak absorption of semiconductors with radiation energies near the bandgap and indirect bandgap semiconductors, for example Si at 850-1100 nm, a microstructured array is used that is etched into silicon that is grown by conventional methods epitaxially such as chemical vapor deposition (CVD) or metal organic chemical vapor deposition (MOCVD), atomic layer deposition (ALD), molecular beam epitaxy (MBE). Note that according to some embodiments, non semiconductors can be used: such as polymers, glass, ceramics, hybrid material such as transition metal oxides, hydrides, chlorides, sulfides embedded with semiconductor, metal, carbon nanoparticles and or atoms, which may or may not have a bandgap. The microstructured array of silicon consists of pillars of Si and/or holes in Si. See, Garnett and Yang, *Light Trapping in Silicon Nanowire Solar Cells, Nano Lett. 2010, 10, 1082–1087* (hereinafter "Garnett et al.") that experimentally demonstrates that an ordered array of silicon nanowires increased the optical path length of the incident optical radiation by 73 times greater than that of bulk silicon.

[00107] According to some embodiments, as described earlier, the concept of effective absorption coefficient is introduced. The effective absorption coefficient of the ordered array of Si nanowires is 73X that of bulk silicon; bulk α for Si is 760 /cm

and nanowire Si α is 5.548×10^4 /cm at 850 nm which is higher than direct bandgap III-V material.

[00108] It should be noted that the microstructures can also be epitaxially grown using methods such as VLS (vapor liquid solid epitaxial grown) nanowires or microwires (some nanowires have the largest dimension, such as the diameter, in the micron range, so that it can be called a microwire) with or without catalysts, or using a dielectric mask for selective area growth (SAG) epitaxy.

[00109] The nanowire array described in Garnett et al. has a diameter of the nanowire of approximately 390 nm using an array of beads of 530 nm as a dry etch mask. Roughly 1/2 of the Si material is etched away; the effective capacitance for the nanowire array is less than that of the bulk. The effective capacitance can be estimated as two parallel capacitors, one with Si and another with polyimide (filler) whose dielectric constants are 11.9 and 3.4 respectively. The area of each capacitor will be 1/2 that of a 30 μm diameter parallel plate.

[00110] With the effective capacitance lower, the overall 3dB bandwidth for a 30 μm diameter device is significantly higher. FIGs. 4A-4D are graphs showing the enhancement of bulk absorption coefficient vs bandwidth and QE for a microstructured Si photodetector, according to some embodiments. FIGs. 4A and 4B shows the bandwidth (plot 410) and quantum efficiency (plot 420) of a microstructured Si photodiode (PD) or avalanche photodiode (APD) at 850 nm wavelength photons impinging on the PD/APD either single or double pass. With an effective absorption coefficient (EAC) of 73X (412), 30X (414) or 15X (416) over bulk absorption coefficient (BAC), the bandwidth and QE are 54 Gb/s, 98%; 49 Gb/s 90%, 28 Gb/s 90% respectively for a 30 micrometer diameter PD/APD for example. At 1100nm, shown in plots 430 and 440 of FIGs. 4C and 4D, with enhancement, for example, of 172X QE of 90% and bandwidths of 26 Gb/s can be attained using Si microstructured PD/APD. Both PD and APD operate at a reverse bias of -2 to -50 volts range. APDs in general will have less bandwidth than PDs for the same geometry due to the added multiplication layer of the APD. In addition, APDs have a gain-bandwidth product. For simplicity, APD and PD are shown to be approximately the same.

[00111] According to some embodiments, a combination of low capacitance due to the gaps between the microstructured pillars and the enhanced absorption

allows the silicon photodiode and avalanche photodiode to operate at bandwidths greater than 10 Gb/s with high quantum efficiencies (> 90%) at 850 nm wavelength. This has not been demonstrated by conventional silicon PD/APD at these wavelengths. 850 nm is chosen as the nominal wavelength, but according to some embodiments, wavelengths can have values from 700 to 1100 nm.

[00112] According to some embodiments, the weak absorption in the bulk can be taken advantage of for photodetector applications since this will allow light at 850 nm and longer to pass through Si substrate and epitaxial layers toward the microstructured silicon with minimal optical loss and minimal photocurrent outside of the high field region, which can diffuse to the i-region and can cause the photodetector to have a degradation in frequency response.

[00113] According to some embodiments, the techniques described herein are applied to other semiconductors, polymers, organic films, glass, dielectrics, hybrid material such as glass, dielectrics, polymers embedded with nanoparticles of metal, semiconductors. According to some embodiments, one or more of the following are used: Ge, III-V material family such as InP, GaAs, GaN, InGaN; II-VI material family such as ZnSe, and also heterostucture material such as III-V grown on Si, Ge grown on Si. For example, for Ge on Si, microstructures are fabricated on the Ge to increase absorption which allows a shorter length of Ge to be used resulting in higher speed due to lower effective capacitance and shorter transit time for the carriers.

[00114] FIGs. 5A and 5B are cross sections showing aspects of a top illuminated microstructered PIN silicon photodiode, according to some embodiments. FIG. 5A shows the starting basic material structure 500. In FIG. 5B, silicon epitaxial structure is shown for a high-speed high efficiency microstructured photodiode 520. The photophoto diode 520 in FIG. 5B is designed for top illumination. According to some embodiments, BOX/SOI layer 504 may not be used. FIGs. 6A-B, *infra* show an example for bottom illumination. Note that with minor modifications the n and p doping can be switched and the direction of illumination may also be affected. Acccording to some embodiments, the illumination can be either perpendicular to the surface of the PD/APD or at an angle off perpendicular to the surface. According to some embodiments, in integrated structures where the optical signal is guided in an optical waveguide, the

microstructured absorption region can also be illuminated edge wise, directly into the microstructures or evanescently coupled to the microstructured i region.

[00115] FIG. 5B shows a microstructured pillar and or hole PD 520 in silicon with the starting material 500 consisting of a P-I-N Si layer grown on an Si substrate 502 that can be N doped or low doped in which case an extra N^+ layer is first grown on the substrate to minimize series resistance. The dimensions and doping of the layers can range as follows; N^+ cathode contact layer 506 (or a thin layer on top of 506, between 506 and 508) with N doping of greater than 5. $10^{17}/cm^3$, and thickness ranging approximately from 0.1 to 10 micrometers or more; N layer 506 with N doping greater than 5. $10^{17}/cm^3$, and thickness ranging approximately from 0.1 to 10 micrometers or more; I high field absorption region 508 with background doping of less than $5x10^{16}/cm^3$ and thickness ranging approximately from 0.1 to 5 micrometers depending on applications; and P^+ anode layer 510 with P doping greater than 5. $10^{18}/cm^3$ and thickness ranging approximately from 0.1 to 5 micrometers or more. The PD (and APD) photosensitive area (defined by the P-I-N or P-I-P-I-N junction area) is nominally 30 micrometers (10-80 micrometers in diameter are possible ranges) in diameter for 20 Gb/s or more bandwidth operation. According to some embodiments, the area can be larger for lower bandwidth or smaller for higher bandwidth operation. The Si microstructures of arrays of holes 522 and/or pillars 524 shown in FIG. 5B, which can be random, patterned or pseudo-random, are for enhancing the bulk absorption coefficient of Si to detect photons with wavelengths from 300-1100 nm. In the case of datacom applications, according to some embodiments, the optical signal wavelengths range from 750-1100 nm. A transparent conducting oxide and P-ohmic layer 526 is also provided.

[00116] The PD 520 is operated in a reverse bias mode, with negative voltage on the anode (P^+ layer 510 via P-ohmic and bond contact metal 528) and positive voltage on the cathode (N^+ layer 506 with N-ohmic bond contact metal 530) ranging from -1 to -20 volts. According to some embodiments, the PD structure 520 shown in Fig. 5B (and PD structure 620 in FIG. 6B, *infra*) can also be used for photovoltaic (PV) operation without any external bias.

[00117] As shown in FIG. 5B, the optical signal can impinge normal to the surface or at an angle off normal. In certain cases, optical signal coming in at an

angle off normal can have a higher QE and can also be at a certain rotation about the axis normal to the surface. This is to avoid the bald spot effect where some photons travelling normal to the surface can "see" bald spots whereas for photons illuminating at an angle off normal to the surface, the bald spots are hidden by other microstructures. This is not the case in near field optics where the spacing of the microstructures are of the order of the optical wavelength or subwavelength, the bald spots are not a significant issue.

[00118] FIGs. 6A and 6B are cross sections showing aspects of a bottom illuminated microstructered NIP silicon photodiode, according to some embodiments. The optical signal impinges on the photodiode 620 from the substrate side or bottom. The substrate 602 can be thinned to 10 microns or less by etching for example a via and stopping at the P layer or the photodiode can be fabricated on a BOX (buried oxide) or silicon on insulator (SOI) silicon wafer and the etch via can stop at the BOX layer 604 which can also be selectively etched to the silicon layer 606, the via 630 is as wide or wider as the photosensitive area of the photodiode 620. An antireflection layer (not shown) is applied to the silicon remaining layer 606 or the BOX layer 604 (the BOX layer 604 can be designed as a part of the antireflection layer for example) to minimize reflection (the BOX layer 604 can also be selectively etched off such that antireflection layer can be applied to the silicon P layer 606 to minimize multiple reflections). The back illuminated photodiode 620 has the advantage that a reflector 626 can be applied on the N layer 610 to reflect any light not absorbed on the first pass, in effect doubling the length of the "I" layer 608. The QE can be increased due to the extra length. In addition the reflector 626 on the N layer 610 can be smooth of textured to scatter (non-specular or diffused reflection) the light (optical signal) to optimize absorption by the microstructures (arrays of pillars 624 or holes 622). Since the length of the "I" region is effectively doubled, the transit time can effectively be reduce since only half of "I" is needed.

[00119] Bottom illuminated PDs such as PD 620 in FIG. 6B are also sometimes referred to back/substrate illuminated PDs, and top illuminated PDs such as PD 520 in FIG. 5B are also sometimes referred to front/surface illuminated PDs.

[00120] According to some embodiments, the basic structure of a microstructured Si photodiode such as shown in in FIGs. 5A, 5B, 6A and 6B, is

fabricated from a bulk thin film epitaxially grown silicon with a P-I-N structure on a silicon wafer which can be doped N type or not intentionally doped or low doped N type Si substrate with (100) orientation or other orientation such as (111).

[00121] According to some embodiments, the basic layer structures (such as layers 502, 504, 506, 508 and 510 of structure 500 of FIG. 5A, and layers 602, 604, 606, 608 and 610 in structure 600 of FIG. 6A) are all grown epitaxially using one or more of the following methods: chemical vapor deposition (CVD), metal organic chemical vapor deposition (MOCVD), plasma enhanced chemical vapor deposition (PECVD), molecular beam epitaxy (MBE), atomic layer deposition (ALD), pulsed laser deposition (PLD) on Si substrate of either P or N or low doped or undoped) or BOX/SOI substrates.

[00122] Processing details have been left out for simplicity. According to some embodiments the following basic steps are carried out: first (for pillars, not necessary for holes), depositing the p ohmic contact metal layer using e-beam, thermal or sputtering deposition; second, photolithographically (or imprint lithography) defining the microstructure pattern either pillars or holes and forming the etch mask for either dry or wet etching; third, etching of microstructure patterns on the P and I layers partially or fully and can extend into the N layer; fourth, passivating the sidewalls of the microstructure patterns (pillars or holes) with thermal oxide to minimize surface recombination of the photogenerated carriers via surface states due to dangling bonds and other surface imperfections (other passivation techniques may also be applied such as ALD (atomic layer deposition) of Si oxides and Si nitrides); fifth, planarization (filler step) using either spin on glass, polyimide, or plasma enhanced chemical vapor deposition (PECVD) of dielectrics such as Si oxides and Si nitrides; sixth, etch back to expose the P layer or P ohmic metal layer (polyimide or spin-on glass may partially fill the holes or space between the pillars/microstructures); and seventh, ohmic and/or bond contacts formed on the P and N layers. In the case of top illuminated photodetectors, where the optical signal enters on the epitaxial surface where the microstructure patterns are fabricated, a transparent conducting oxide is deposited to connect all the P ohmic metal layers (for pillars). In the case where the microstructures are holes or voids the transparent conducting oxide layer is not used, according to some embodiments. A voltage bias is applied between the P

layer (anode) and the N layer (cathode) of -1 to -20 V, and the photodiode is operated in a reverse bias mode to deplete as much as possible the "I" layer, preferably the entire I layer.

[00123] FIGs. 7A and 7B are cross sections showing aspects of a microstructered avalanche photodiode, according to some embodiments. As in the Si microstructured photodiodes shown in FIGs. 5A, 5B, 6A and 6B, the epitaxial layers 700 for the APD 720 are grown first followed by microstructure processing. The microstructured avalanche photodiode 720 can be illuminated (e.g. with 300-1100 nm) from the top with transparent metal oxide P ohmic contact 726, or the P ohmic contact 726 can be a mirror to reflect the photons illuminating from the bottom (e.g. with 950-1100 nm) to have a double pass absorption. The double pass absorption greatly improves the RC time and the Transit time of the APD for a higher frequency response.

[00124] FIG. 8 is a cross section showing a silicon epitaxial structure for a high-speed high-efficiency microstructured APD, according to some embodiments. Layers 800 are shown prior to microstructure processing. With minor modifications, the n and p doping can be switched and the direction of illumination may also be affected. Starting with a N silicon substrate 802 (or low doped or silicon on sapphire or a BOX /SOI wafer depending on the application and packaging considerations), an N^+ layer 804 (N ohmic contact layer) is formed with doping concentration of greater than 10^{18} cm^{-3} (typically phosphorous) with layer thickness ranging approximately from 0.1 to 10 µm. A non-intentionally doped layer "i" 806 or a P^- (very low doping level P layer) has a doping concentration less than $5x10^{16}$ cm^{-3} (this is the multiplication or electronic gain layer of the APD) with thickness ranging approximately from 0.1 to 2.0 µm depending on gain and bandwidth of the APD. A P charge layer 808 is grown with an approximate thickness 0.05-0.2 µm and doping concentration of greater than $2x10^{17}$ cm^{-3}. An absorption layer 810 is grown (P^- or "i") ("I" and "i" are used interchangeably herein) with doping less than $5x10^{16}$ cm^{-3} with thickness ranging approximately from 0.1 to 5 µm. Finally a P^+ contact layer 812 is grown with doping greater than $5x10^{19}$ cm^{-3} with layer thickness ranging approximately from 0.1 to 1.0 µm. According to some embodiments, all layers 800 are grown epitaxially using CVD or MOCVD reactors.

Doping and thickness are approximate and are adjusted depending on applications.

[00125] For best noise performance of the Si APD, photogenerated electrons should dominate in the multiplication process; i.e. holes diffuse/drift toward p (anode) and electrons diffuse/drift toward the n (cathode) with reverse bias. The Si layers 800 are grown epitaxially using chemical vapor deposition, plasma enhanced chemical vapor deposition, molecular beam epitaxy, atomic layer deposition (can be a combination of these methods to generate the optimal layer structure in doping and interface quality) on doped or undoped substrates. The total length for the electrons to transit range from approximately 0.25 to 7.2 microns. This can be, for example, 0.5 μm for absorption, 0.1 μm for charge, 0.5 μm for multiplication, with a total of 1.1 μm for the APD layer structure 800 shown. According to some embodiments, for higher QE, the absorption region can be lengthened to one μm for a total transit length of 1.6 μm for example. Other layer thickness and doping concentrations can be adjusted to optimize device characteristics for different wavelength, integration with CMOS, application requirements, operating conditions such as bias voltage, gain and noise.

[00126] Also, the APD can be illuminated with modulated optical signal from the bottom, where using BOX or SOI, the bulk of the substrate can be removed to minimize optical losses and thus can use the double pass of the photons in the enhanced absorbing microstructured layer.

[00127] FIGs. 9A-9E are a series of cross sections showing some basic microstructure processing steps, for a high-speed APD, according to some embodiments. FIG. 9A shows the high speed APD epi structure 800 as described with respect to FIG. 8. In FIG. 9B, as in the PD process, a P-ohmic metallization or dielectric mask 910 can be deposited first on the P layer 812 for the microstructured pillars. In the case of holes and/or voids this step may not be carried out. Dry etch mask 910 is deposited on the surface using photolithography, metal/dielectric deposition techniques and wet/dry etching. In FIG. 9C, according to some embodiments, reactive ion etching (RIE) or deep reactive ion etching (DRIE), wet etching using chemicals and oxidation of the Si are used to generate the microstructured pillars 914. Native silicon oxide for surface passivation can be provided by thermal oxidation (which is preferred in some cases), electrochemical

anodization, and/or plasma enhanced chemical vapor deposition. According to some embodiments, the thermal oxidation of the pillars 914 can also be used to fine tune the diameter of the pillar since the oxide is created from the Si material. Thermal oxidation also smooths the surface which is favorable for electrical properties. In FIG. 9D a filler 916 is used to fill or partially fill the space between the Si pillars 914 to support subsequent contact layers to be deposited. The filler 916 can be spin on glass, polyimide, dielectric such as silicon nitride, or silicon oxide, that can be deposited for example using plasma enhanced chemical vapor deposition. Once the contacts are made the fillers can be left in place or removed by dissolving the filler with an etchant or solvent. Removing the filler has an advantage of further reducing the capacitance of the device since air has a dielectric constant of 1. The reduction of the capacitance allows the device to operate at higher bandwidth due to reduction of the RC time. In FIG. 9E, the anode and cathode ohmic contact metallizations 922, 924 and 926 are made. Depending on the direction of illumination, transparent conducting oxide TCO 932 (such as indium tin oxide ITO) can be used. In the case of top illumination, a dry etch can be used to expose the pillars if they are buried in the filler. The TCO 932 can then be used to contact the P^+ silicon pillars at the tip or the P ohmic metallization 922. Ohmic contact metallization is then applied to the cathode (N^+) layer either on the surface (924) or bottom (926) depending on integration topology.

[00128] In the case of the optical signal coming from the substrate side (the bottom), the wafer is thinned. If the thinning is carried out by etching it can include a buried silicon dioxide layer such as silicon on insulator, SOI/BOX, such that the oxide layer can act as an etch stop layer. The wafer can be thinned first by chemical mechanical polishing to 100 μm followed by a via etch to the oxide layer which can be selectively etched off, such that the optical signal only need to traverse a few micrometers of Si bulk material. Anti-reflection coating 930 is applied to the Si surface to minimize reflection loss. Ohmic metallization is applied to the N^+ layer followed by bond metal 924. On the microstructured pillars, ohmic metallization is applied to the P^+ tips (if its not applied already in the preliminary steps), followed by bond metal 922. According to some embodiments, an advantage of the optical signal entering from the substrate surface (i.e. the bottom)

is that the light will bounce and travel twice within the pillar structures, thus increasing the quantum efficiency. According to some other embodiments, the pillars can be made shorter to improve the transit time.

[00129] According to some embodiments, the optical signal can also enter from the edge as shown FIG. 52, *infra*, either in a guided mode or in free space. In the edge application, TCO 932 and solid anode ohmic contacts may not be used and wafer thinning may not be carried out. Cathode ohmic contacts can instead complete the structure. According to some embodiments, in edge approach, the pillars are arranged such that their density is not uniform to optimize the capture of the optical radiation. It can be arranged in a V pattern for example to reduce optical reflection.

[00130] Not shown in FIGS. 9A-9D are mesa etching steps used to define the diameter of the APD 920. According to some embodiments, other methods such as ion implantation may also be used. Note that the microstructures themselves provide good confinement of current in the vertical direction and not in the lateral direction. Other known processing steps that are not shown for sake of simplicity include: thermal oxidation passivation of exposed surfaces; adding guard rings; thinning of the wafer; adding anti-reflection coatings; annealing of ohmic contacts; and creating via holes for removal of filler.

[00131] Taking advantage of low absorption constant of bulk Si. High speed photodiodes made with III-V material often are constructed such than the photocarriers are generated only in the i layer of a PiN structure to minimize the photogenerated carriers outside of the high field region that can cause degradation to the frequency response of the device. This can be done easily in III-V material since there are many ternary and quaternary material such as InGaAsP, InGaAs, InAs, that are lattice matched to InP and the bandgap of these alloys can be changed by altering the composition such that the P+ anode 812 and P charge 808 layers are mostly transparent and the i layer is absorbing. However it is not easy for silicon since there are no materials that are lattice matched to silicon. Germanium can be grown on silicon but with the addition of a buffer layer to accommodate for the lattice mismatch.

[00132] According to some embodiments, a method to overcome this issue in silicon is to take advantage of the low absorption constant of silicon at radiation

near the bandgap of silicon. According to some embodiments, the wafer can be thinned to the insulator of an SOI structure and the 850 nm optical signal will only traverse 1-2 μm of bulk silicon losing approximately 10% or less of the incident radiation. The rest of the radiation continues to the microstructured pillar silicon where the absorption is stronger possibly due to resonance effects. According to some embodiments, the shape of the pillars can be circular, oval, rectangle, chevron, hexagon, double-circle, crescent, star, or any shape to optimize absorption and collection efficiency. The pillar diameter range from 50-1200 nm (smallest dimension can be 50 and largest dimension 1200 nm) and can be spaced uniformly or non-uniformly, periodic or aperiodic, chirped, or a pattern either locally or globally to optimize APD/PD performance and applications. The spacing of the pillars can be 20-2000 nm. The microstructured pillars can be 100 to 10000 nm in length that is optimized for bandwidth and efficiency for a particular wavelength near the silicon bandgap for example 850, 880, 980, 1000 nm.

[00133] According to some embodiments, multiple dimensions (both structure and spacing) of the microstructures within a single PD/APD can broaden the resonance bandwidth of the microstructures such that the enhanced absorption coefficient is over a broader optical spectrum.

[00134] The substrate becomes less absorbing as the wavelength approaches 1100 nm (1.1 eV Si indirect bandgap).

[00135] According to some embodiments, the microstructured pillars/holes/voids can have orientations that are not perpendicular to the surface of the silicon substrate. Other orientations off perpendicular or with multiple orientations or even random or pseudo-random are possible to optimize the QE with respect to the directivity of the optical signal. In multiple and/or random or pseudo random orientations of the microstructures, the device become less sensitive to the direction of light illumination which is beneficial in PV applications. In certain applications, antenna like high directivity of the PD/APD may be desirable to avoid cross talk for example from other optical signal sources or to further improve its QE.

[00136] According to some embodiments, microstructured hole arrays, instead of pillar arrays, are used as light traps in silicon. Microstructure hole arrays have similar properties as microstructured pillars. See e.g. Lin et al, Optical absorption

enhancement in silicon nanowire and nanohole arrays for photovoltaic applications, Next Generation (Nano) Photonic and Cell Technologies for Solar Energy Conversion, edited by Loucas Tsakalakos, Proc. of SPIE Vol. 7772, 77721G (2010). According to some embodiments, instead of etching microstructured pillar arrays as described herein, microstructured hole arrays are etched using RIE/DRIE and similar processing for the pillars, including thermal oxidation for surface passivation, deep ion implantation for electrical isolation, confinement of optical fields and reduction of capacitance. In the case of the hole arrays, it is possible that the filler need not extend the entire length of the hole. For example, if the surface tension of the filler is high, only partial filling of the holes with filler will be possible and provide support for subsequent layers of TCO, metal, oxide, silicide, alloys to name a few that may be necessary to complete the device structure. According to some embodiments, in the case of microstructured holes, fillers are not used in the PD/APD/PV devices since the surface is contiguous rather than consisting of islands as in the case of microstructured pillars.

[00137] According to some embodiments, the microstructured holes can have diameters of 50-3000 nm and can be a square, hexagon, oval, rectangle, chevron, double-hole, with the smallest dimension at 50 nm to the largest dimension of 3000 nm approximately. The spacing between holes (adjacent edges) can be regular or irregular or a pattern at 20-2000 nm. The depth (or length) of the hole can be 100 to 10000 nm and can be uniform depth or non-uniform depth. Dimensions are chosen for optimal absorption, quantum efficiency, bandwidth and radiation collection efficiency for a particular wavelength and application.

[00138] As discussed earlier, to optimize High Contrast Grating in the Absorption regime of this invention, it may be desirable to have the microstructured enhanced absorption structures on materials of a lower refractive index such as BOX or SOI where the silicon dioxide refractive index is lower than that of Si, Ge or III-V/II-VI material. According to some embodiments, the effective refractive index can be made lower than the refractive index of the microstructures with the inclusion of voids in the substrate. FIGs. 10A-10B are cross sections showing aspects of a top illuminated microstructered photo diodes, avalanche photo diodes and/or photovoltaics (PV) with microstructured voids in N-Si, according to some embodiments. Voids can be included in the substrate or as a microstructure for

enhancing absorption coefficient as will be discussed *infra*. Refractive index in the optical spectrum of Si, Ge, III-V material typically range from 3-3.6, by using silicon dioxide such as SOI and voids that are 50% of the material in volume, the refractive index or effective refractive index can be reduced to approximately 0.5 that of the bulk semiconductors. By adjusting the ratio of the volume of the voids to the material (Si for example) the effective refractive index can also be adjusted from a few percent to more than 90% that of the bulk material. The voids can be filled with other material such that it is not just air, gas or vacuum, but a dielectric such as glass, polymer, dielectric, oxide, or amorphous semiconductor that can be optically and/or electrically passive and or active with optical and/or electrical gain for example.

[00139] FIG. 10A shows the layers 1000 including N-Si layer 1006 which contains microstructured voids 1008 that effectively reduce the refractive index of the N-Si layer 1006 as described. FIG. 10B shows a top illuminated PD/APD/PV 1020 that includes microstructured pillars 1024 and/or holes 1022, as well as transparent conducting oxide layer 1026. Microstructered voids 1008 can be random or patterned. The microstructered voids 1008 can be used reflect photons back to the absorbing "I" region if the voids 1008 are patterned to have HCG effects at wavelenghs where loss is low such as 950-1100 nm. According to some embodiments, BOX or SOI substrates can also be used together with voids or without voids or without BOX/SOI.

[00140] According to some embodiments, the microstructuring techniques described herein are also applied to heteroepitaxial material (III-V on Si, Ge on Si, or II-VI on Si). Ge (bandgap 0.66 eV at 300K) having much smaller bandgap than Si, can be used for detecting optical signals at 850 and 1300 nm. Using the techniques described herein, Ge devices can also be made to detect optical signal with wavelength at 1550-1600 nm which can than replace III-V material based photodetectors. According to some embodiments, microstructures are grown such as nano/microwires or etched from bulk material with or without lithographic masking.

[00141] Ge thin film can be grown epitaxially on Si. See, e.g. Kang et al, Epitaxially-grown Ge/Si avalanche photodiodes for 1.3μm light detection, 23 June 2008 / Vol. 16, No. 13 / OPTICS EXPRESS 9365 (hereinafter "Kang et al."), where

an APD was fabricated for 1310 nm wavelength operation for a 30 μm diameter device. The QE of the device with a 1 μm Ge absorption length is only 56% whereas by using microstructured pillars/holes/voids according to embodiments described herein, QE of approximately 90% or greater can be achieved at 1300-1600 nm wavelength with bandwidths of approximately 30 Gb/s or greater for a 30 micrometer diameter PD/APD. Such devices can find useful applications in datacenters, local area networks, and in metro and long distance optical data/telecommunications. According to some embodiments, integration on silicon is used which results in significant cost reduction in manufacturing and packaging. In comparison, in Kang et al. a 30 μm diameter APD was only able to reach approximately 15 Gb/s bandwidth at 1310 nm and cannot extend the wavelength due to low absorption of the bulk material without sacrificing a significant reduction in bandwidth.

[00142] FIGs. 11A and 11B are cross sections showing aspects of an heteroepitaxial APD structure of Ge on Si, according to some embodiments. Layers 1100 and APD device 1120 show a possible heteroepitaxial APD structure of Ge on Si (as opposed to descriptions, *supra*, of homoepitaxial APD/PD structure where only silicon is used with different doping concentrations). Similar processing methods as in the homoepitaxial Si APD are used to fabricate microstructured pillar/hole arrays. According to some embodiments, the absorption constant of bulk Ge is enhanced by greater than 70X, for example 73-172X. According to some embodiments, APDs and PDs with bandwidths in excess of 30 Gb/s can be achieved in devices with an active diameter of 30 μm or less at wavelengths to 1750 nm and QE of approximately 90% or greater. This is a significant improvement over existing Ge on Si APD with illumination normal or off normal to the surface of the substrates.

[00143] According to some embodiments, the microstructured pillar and hole (and variations thereof) arrays can be fabricated in Si, Ge, Ge on Si, SiGe on Si, SiGe on Ge; it can be any combination of Si,Ge and SiGe.

[00144] At longer wavelengths 1200-1800 nm, Ge (germanium) photodiodes are often used since Ge has a bandgap of 0.66 eV (whereas Si has a bandgap of 1.1 eV). However, for high bandwidth applications (greater or equal to 20 Gb/s) Ge photodiodes are only good to 1350 nm due to the fact that for transit times to be

approximately 30 picosec (electron saturated drift velocity is $6x10^6$ cm/s at $1x10^4$ V/cm in order to have a bandwidth of approximately 20 Gb/s ($f(3dB)=0.44/\tau$ where τ is the transit time through the "I" region) the length of the absorption region or the "I" region is limited to approximately 2 microns. At this length, the QE at 1550 and 1600 nm is less than 10%, which is not generally acceptable for optical receivers for datacom and telecom applications. In a waveguide configuration, the length of the absorption region can be 50-100 microns and still achieve 20 Gb/s or higher with QE equal or greater than 90%. The waveguide Ge on Si photodiode structure have been reported by other research groups however such waveguide photodiodes have excess optical losses due to waveguide losses and coupling loss (coupling of optical signal to the optical waveguide) which can be as high as 3 dB or half of the optical signal is lost. The "free-space" coupling (where the optical signal is directed to the PD/APD using elements such as lens, diffraction elements, light pipes, optical waveguides to name a few) of optical signal to the microstructured photodiode and avalanche photodiode have much less optical losses, typically a few percent or less. One of the reason is the large area of the microstructured PD/APD which is 30 microns in diameter as compared to waveguide photodiodes its dimensions are a few microns, typically 1-2 microns. Not only is coupling loss high in waveguide PD/APD, it often uses active alignment which requires that the waveguide PD/APD is turned on to monitor the coupling of the optical signal into the waveguide PD/APD. This active alignment is slow and time consuming which adds cost to the packaging of the waveguide PD/APD in any optical receiver module. In contrast, the large area microstructured PD/APD, according to some embodiments, uses only passive alignment where it is aligned without turning on the microstructured PD/APD. Such alignment is much faster and easier which reduces the cost of a microstructured PD/APD in any optical receiver module. It should be noted that with the effective capacitance of the microstructured PD/APD significantly lower than bulk PD/APD by 10 to 80% or more, the area of the microstructured PD/APD can be correspondingly larger by 10 to 80% or more.

[00145] In FIG. 11B, a microstructured Ge on Si pillars/holes APD structure 1120 with bottom illumination is shown. Epitaxial layers for an APD Ge on Si are used where the optical absorption to generate electron-hole pairs takes place in Ge

and the gain/multiplication of the electrical charged carriers takes place in Si. The epitaxially grown layers are similar to Ge on Si bulk (thin film) APD with the following layer compositions ranges (shown in FIG. 11A). N is undoped, or low doped (20 ohms-cm) Si substrate 1102, which can also be SOI or BOX, to allow removal of the Si substrate for bottom illumination and/or to reduce the refractive index. If SOI or BOX substrates are used, the N ohmic contact and bond metal will be on the N^+ -Si surface adjacent to the multiplication I region. N^+ contact layer 1104 which can be 2-8 microns, $N^+ > 5.10^{18}\ cm^{-3}$. I multiplication layer (or gain layer) 1106 which can be undoped (not intentionally doped), 0.2-1.0 microns thick and $I < 1.10^{16}\ cm^{-3}$. P charge layer 1108 having a thickness of 0.05-0.2 microns and $P \sim 1\text{-}6.\ 10^{17}\ cm^{-3}$. P^- low temp Ge buffer layer 1110 having a thickness of ~ 0.01-0.04 microns and $P^- \sim < 1.\ 10^{16}\ cm^{-3}$. I or P^- absorption layer 1112 having a thickness of 0.2- 2.0 microns, and I (or P^-) $<1.\ 10^{16}\ cm^{-3}$. Finally, P^+ contact layer 1114 has a thickness of 0.05- 0.2 microns, and $P^+ > 2.\ 10^{20}\ cm^{-3}$, approximately.

[00146] Starting with a wafer with all the layers 1100 grown for APD operation, the processing details are left out for simplicity. The basic steps involve first, depositing the p ohmic contact metal layer 1126 using e-beam, thermal or sputtering deposition. The microstructure pattern of either pillars or holes is photolithographically, using positive or negative or image reversal photoresist methods depending on pillars or holes, defined to form the etch mask for either dry or wet etching. According to some embodiments imprint lithography can be used. The microstructure patterns are etched on the P^+ and I (or P^-) and P Ge layers 1114, 1112 and 1110, respectively, partially or fully to the P Si layer 1108 (e.g. using fluorine, chlorine, bromine based gases such as SF_6, CF_4, BCl_2, Cl_2, for selective dry etching using RIE and DRIE). The selectivity of the etch between Ge and Si can be as high as 70, so as to etch Ge 70 times faster than Si by adjusting gases mixtures, pressure, temperature and bias, and power. The sidewalls of the microstructure patterns (pillars or holes) are passivated with dielectric or SiGe and gradually reducing the Ge content such that Si remains on the surface (using for example atomic layer deposition ALD) and subsequently using thermal oxidation to minimize surface recombination of the photogenerated carriers via surface states due to dangling bonds and other surface imperfections. According to some embodiments, other passivation techniques may also be applied such as ALD of

Si oxides and Si nitrides. Planarization is performed using either spin on glass, polyimide, or PECVD deposition of dielectrics such as Si oxides and Si nitrides. An etch back is performed to expose the P layer. For microstructured holes and pillars, it may not be necessary to planarize completely, by using polyimide or spin-on glass to partially fill the holes and spaces between pillars. Ohmic and/or bond contacts are formed on the P and N layers. For top illuminated photodetectors, where the optical signal enters on the epitaxial surface where the microstructure patterns are fabricated, a transparent conducting oxide 1126 (the transparent conducting oxide may not be used in the case of microstructured holes) is deposited to connect all the P ohmic metal layers (for pillars). A voltage bias is applied between the P^+ Ge layer 1114 (anode) and the N^+ Si layer 1104 (cathode) of -2 to -45 V. The APD 1120 is operated in a reverse bias mode to deplete as much as possible both of the "I" layers. Many detailed processing steps are left out such as annealing, surface preparations, deposition of ohmic contacts, bond metal, RIE, DRIE, wet etching, masks for etching, mask removal, antireflection coatings, mirrors such as Bragg reflectors on the microstructured layers, to name a few. Ohmic contact metallization to P and N semiconductors and bond metallizations are well known in the art and details are not mentioned here. Also, holes are used in electron-hole pairs as charged electrical carriers and holes as in a physical void such as the microstructured holes. From context it should be understood if "hole" refers to a charged electrical particle or a physical void.

[00147] According to some embodiments, Ge surfaces of the microstructured pillars or holes and any Ge surfaces exposed to an electric field, where electric current can flow and/or where electric charges are formed are passivated to reduce current leakage, minimize surface states that can be a potential sink or recombination centers for carriers, especially photogenerated carriers of electrons and holes (as in Si, thermal oxide or rapid thermal exidation, to create SiO_2 and SiO_x used to passivate any silicon surfaces that can cause excessive leakage current or recombination centers for photogenerated carriers, or a carrier sink) and GeO_xN_y which is a native Ge oxynitride that is formed in two stages, where the Ge microstructured pillars and/or holes are first exposed to oxygen and then to ammonia ambient in a rapid thermal annealer to form the Ge oxynitride passivation layer. These passivation methods are well known in the art.

[00148] FIG. 12 is a cross section illustrating aspects of a passivation method for Ge surfaces on microstructures, according to some embodiments. Shown are microstructured Ge pillars 1202 (or holes) for a PD and/or APD. On the Ge surfaces is conformally epitaxially grown SiGe layer 1210. Gradually, the Ge content is reduced within layer 1210 until only Si is exposed on the surface. Thermal oxidation of Si is then used to passivate the exposed Si surfaces, forming SiO2 layer 1212, to minimize leakage current and surface states that can be a potential sink for carriers, especially photogenerated carriers (electrons and holes) that can degrade QE.

[00149] FIGs. 13A and 13B are graphs showing the effects of mictrostructure enhancement of Ge bulk absorption coefficient for photodiodes and/or avalanche photodiodes based on Ge on Si, according to some embodiments. According to some embodiments, a 73x enhancement of bulk absorption coefficient is gained in PD/APD devices having microstructured pillars/holes at 1550 and 1600 nm. FIG. 13A shows the bandwidth verses "d" or the length of the "I" layer for 1550 nm (point 1310) and for 1600 nm (point 1312) Note that APDs have both a Ge "I" layer and an Si "I" layer; whereas for PDs have just a Ge "I" layer. FIG. 13B shows QE verses "d" or "I" layer length for 1550 nm (point 1320) and 1600 nm (point 1322). It can be seen that for a 30 micron diameter active region PD/APD bandwidths of 40 and 31 Gb/s can be attained at 1550 nm and 1600 nm optical wavelength respectively with 90% QE. This result was not achievable with bulk Ge photodiodes and avalanche photodiodes of conventional design.

[00150] The separation of using Ge microstructures to absorb the light generating e-h (electron-hole) pairs and using Si for the avalanche multiplication of the carriers, preferably electrons, results in an APD with very low noise due to the fact that the ionization ratio (defined as hole ionization rate/electron ionization rate) for electrons injected into the multiplication region (gain region which is a function of applied reversed bias voltage) is lower than in III-V material family. This result in a low excess noise factor leads advantageously to a high signal to noise ratio (S/N).

[00151] FIGs. 14A-14B are cross sections showing aspects of a top-illuminated Ge on Si avalanche photodiode having microstructured pillars/holes, according to some embodiments. FIG. 14A shows the bulk layers 1400. In FIG. 14B, top

illuminated microstructured Ge on Si APD 1420 is shown with a semitransparent conductive oxide 1426 connecting the P-ohmics on the Ge microsturctured pillars 1424 (holes 1422) as described *supra*. Both top and bottom illuminated microstructured Ge on Si share similar epitaxial structures. The processing steps for top and bottom illuminated microstructured APDs are similar. The main differences are that the transparent conductive oxide for top illuminated APD (or PD) is replaced with an opaque ohmic/bond metallization that can act as a mirror to reflect the optical signal back toward the absorption I layer. According to some embodiments, the mirror can also consist of Bragg reflectors either wafer bond to the microstructure or epitaxially or vacuum deposited such as dielectric or conductive metal dielectrics to enhance the reflectivity to greater than 90% of the optical signal. In addition, bottom illuminated PD/APD may require a window or via where most of the Si substrate is removed to reduce optical losses depending on the wavelength of the optical signal.

[00152] FIGs. 15A-15C are cross sections illustrating aspects of bottom-illuminated Ge on Si avalanche photodiodes having microstructured pillars/holes, according to some embodiments. FIG. 15A shows the bulk layers 1500 prior to forming the microstructures (pillars and/or holes). FIG. 15B shows a Ge on Si microstructured APD 1520 with the optical signal illuminating from the bottom (substrate side) for wavelengths from 1200-1800 nm. Note that Si is basically transparent at these wavelengths. According to some embodiments, to further reduce optical losses, the Si wafer can be thinned just at the area of illumination, for example through a via of 50-500 microns in diameter and thinned to the N^+ layer of the Si; or the Si substrate 1502 can include a BOX or SOI layer 1502. The Si substrate 1502 can then be thinned selectively to the BOX or insulator layer 1502 which can be etched away selectively. According to some embodiments, an anti reflection layer (not shown) can be added to minimize reflection. The advantage of this arrangement is that the optical signal will have a double bounce, reflecting off the metallization 1526 on the Ge P^+ layer 1514 and traversing the Ge "I" absorber region 1512 once again. For example, as shown in FIGs. 13A and 13B, keeping the same absorption length, Ge "I" length, the QE for both 1550 and 1600 nm would be approximately 90% or higher for a Si substrate side (bottom) illumination by the optical signal assuming negligible reflection loss. According to some

embodiments, the Ge "I" absorption length can be further shortened to increase the bandwidth and still maintain acceptable QE.

[00153] For Ge epitaxially grown on Si, it is known that the bulk absorption coefficient is greater than that of Ge bulk by itself (not grown on Si); at 1750 nm the Ge on Si absorption coefficient is approximately 100 cm^{-1}. According to some embodiments, this can be enhanced by the microstructured pillars and/or holes by 172 times. The resulting enhanced Ge on Si microstructured pillar and/or holes absorption coefficient can be about 1.72. 10^4 cm^{-1}.

[00154] FIG. 15C shows an APD 1540 in which the microstructure extends all the way to the N cathode layer 1506 to further reduce capacitance and refractive index. In this case, the absorbing i layer 1512 is microstructured as is the charge layer 1510 and the i multiplication layer 1508. According to some embodiments, the microstructures can also be formed partially into the charge and multiplication layers 1510 and 1508. Additionally, according to some embodiments, the microstructures in the absorbing layer 1512 and the multiplication layer 1508 need not be the same. In FIG. 15D, photons may generate electron hole pairs in the multiplication region which may contribute to added gain but also may contribute to excess noise. According to some embodiments, the absorption and multiplication region using the microstructure APD is combined in one region without the use of the charge layer. This is possible due to enhanced absorption: the length of absorption and multiplication can be of the order of one micron or less allowing reasonable avalanche voltage.

[00155] FIG. 15D shows a microstructered APD 1560 where the absorption and multiplication region are a single region 1566, pillars or holes, according to some embodiments. This is enabled by the microstructure enhancing the absorption coefficient so that less than one micron of the absorbing microstructure length is needed to achieve QE of approximately 90% or more and avalanche multiplication can also occur in this length of material. For example, if 0.5 μm of microstructured Si shown in Fig.15D is the thickness of layer 1566, a back illuminated APD 1560 allows a double bounce of the optical signal reflecting off the N ohmic contact and bond metallization resulting in an effective length of one micron of absorption length. The Si APD 1560 can operate at 0.5 μm multiplication length resulting in gain of 3 dB or more with a reverse bias ranging from -5 to -50 volts. According to

some embodiments, the structure shown in FIG. 15D can be applied to other material systems such as Ge, Ge on Si, III-V, and III-V on Si or not on Si.

[00156] FIGs. 16A and 16B are graphs comparing single pass and double pass photodiodes and/or avalanche photodiodes based on Ge on Si, according to some embodiments. Points 1610 and 1620 show the bandwidth and QE values for single pass with d of approximately 1.4 microns and points 1612 and 1622 show the bandwidth and QE values for a thinner d of approximately 0.7 microns single pass. For double pass the device will have points 1612 for bandwidth and point 1622 for QE. At 1750 nm optical signal wavelength, using absorption coefficient data of 100/cm for Ge on Si and with, for example, 172 times (172X) enhancement factor due to the microstructured Ge on Si photodiode/avalanche photodiode structures, a bandwidth of 27 Gb/s and a QE of approximately as high as 90% can be attained with an "I" (also "d") length of approximately 1.4 microns for a single pass (top illuminated - where the optical signal illuminates the top Ge microstructured side). As mentioned earlier, for photodiodes the "I" or "d" is the absorption length, whereas for avalanche photodiodes the "I" is the combined absorption length and the multiplication length. For example, for an APD to achieve 27 Gb/s the total "I" length needs to be limited to 1.4 microns. A double pass arrangement can be used such that for example the absorption length is 0.9 microns and the multiplication is 0.5 microns, making the absorption length effectively 1.8 microns to achieve QE above 90%. However, if we instead have the optical signal illuminate from the bottom Si substrate side, the Si substrate and Si layers are basically transparent and have minimal optical losses (approximately 1-3 dB/cm) at optical radiation energies that are below the bandgap of Si (1.1 eV or 1127 nm wavelength at 300K) for example for radiation from 1200-1800 nm wavelengths. The advantage of illuminating from the Si substrate side (bottom) is that the optical signal can have a double pass at the Ge "I" absorbing region if the metallization on the P^+ contact layer is reflective which it should be since it is metallic composing of Au, Al, Ag, Cr, Zn, Ti, Ta, Ge, or a combination of these metals and semiconductors. Bragg reflectors consisting of material with alternating refractive indices from oxides, nitrides, chlorides, semiconductors, either wafer bonded to the microstructures or deposited on the microstructures can also be incorporated. Reflectivity can be greater than 90%. With double pass, as shown in

FIGs. 16A and 16B, a bandwidth of 40 Gb/s can be attained with a QE approximately as high as 90% or more.

[00157] FIGs. 17A-17B are cross sections showing aspects of a top-illuminated Ge on Si photodiode structure having microstructured pillars/holes for applications with signal wavelengths ranging from 700 to 1800 nm, according to some embodiments. FIG. 17A shows the bulk layers 1700. In FIG. 17B, Ge on Si microstructured pillars 1724 and/or holes 1722 are in a configuration for photodiode 1720. This is essentially a P-I-N structure where the "P" and "I" are Ge with microstructured pillars 1724 and/or holes 1722 to enhance the bulk absorption coefficient of Ge grown on Si. The increase in the absorption coefficient of Ge grown on Si (Ge on Si) could be due to the stress build in the Ge epitaxial layer due to lattice mismatch with the Si host substrate that it is grown on. Optical signal as in the case for Ge on Si APD can be illuminated from either the microstructured side (as in FIG. 17B) or the substrate side (as in FIG. 18B).

[00158] FIGs. 18A-18B are cross sections showing aspects of a bottom-illuminated Ge on Si photodiode structure having microstructured pillars/holes for applications with signal wavelengths ranging from 1200 to 1800 nm, according to some embodiments. FIG. 18A shows the bulk layers 1800. FIG. 18B shows photo diode 1820 configured for signal illumination from the Si substrate side (bottom illumination) with photo energies that are less than the Si bandgap of 1.1 eV at 300K. The corresponding wavelength range is 1200 to 1800 nm. Ohmic contact 1826 can also act as a mirror such that the light makes a double pass of the Ge absorbing microstructures where the metal contact layer on the P Ge can reflect the optical signal back toward the Ge "I" absorbing layer.

[00159] It should be noted that in all the discussions of the P-I-N structures, according to some embodiments the P and N are interchanged such as with an N-I-P structure formed on a P substrate or on a low doped P substrate or undoped substrate. According to some embodiments, the N and P for the APD structures are also interchanged and the substrate can be P, low doped P or undoped. However, in an Si multiplication layer, to achieve the lowest noise and the best S/N, electrons are injected into the multiplication region as dominantly as possible since the ionization rate of electrons is higher than the ionization rate of holes in Si; the ionization ratio for Si can range from 0.06 to 0.002 where as compared to Ge

and InGaAs it is 0.9 and 0.45 respectively. This is why in many of the embodiments described herein the enhanced absorption is in Ge microstructures and the gain or multiplication which is dependent on the field strength and therefore on the applied reverse bias voltage which for the described devices can range from -10 to -60 V, is in Si.

[00160] According to some embodiments, the microstructured pillars and or holes for Si and Ge on Si photodiodes (PD) and avalanche photodiodes (APD) are used to replace relatively expensive III-V photodiodes. The Si microstructured pillars and holes PD/APD can operate from 500 to 1100 nm at bandwidths of 20 Gb/s or higher and QE of 90% or higher. In particular, the datacom wavelengths of 730-980 nm. The microstructured pillars and or holes on Ge epitaxially grown on Si PD and APD can operate from 500-1800 nm with bandwidths of 20 Gb/s or more and QE of 90% or more. In particular, the telecom wavelengths of 1250-1600 nm and possibly to 1750 nm. The techniques described herein thus extends the wavelengths, bandwidth and QE of conventional Si and Ge on Si free space coupled photodiodes and avalanche photodiodes.

[00161] According to some embodiments, the microstructured pillars can also be fabricated using VLS (vapor-liquid-solid epitaxy) growth of Ge nanowires on an Si substrate. Others have demonstrated the growth of vertical Ge nanowires on Si (111) orientation for example, with Au nanoparticles as catalysts for the VLS epitaxial growth using chemical vapor deposition (CVD) or metal organic chemical vapor deposition (MOCVD). Crystal orientations other than (111), or with materials with multiple orientations such as in polycrystalline may be used. Materials such as Si, Ge, III-V, glass, quartz, metal, to name a few can also be used as substrates. According to some embodiments, a thin Ge buffer layer of approximately 2nm on Si (111) substrate is formed together with Au nanoparticles as catalysts for VLS growth in a CVD reactor. The Au catalyst can be deposited using a lithography mask to expose photoresist that is coated on the Si substrate. The Au is evaporated onto the Si substrate with patterned photoresist. Using standard processing methods such as lift-off, the Au pattern is left behind on the Si substrate which is then the catalyst for Ge VLS growth on Si substrates. According to some embodiments, it can also be grown using selective area growth where a dielectric

mask is deposited on the Si substrate with a pattern of voids that allow Ge to grow in the void using CVD.

[00162] The microstructure of pillars and holes on the surface of a bulk photodiode not only enhance the absorption coefficient by factors ranging from 10-200 over the absorption coefficient of bulk material (material without any microstructured features and grown on lattice matched substrates so that stress due to lattice mismatch is minimal) but also significantly reduce the capacitance of devices such as PDs and APDs. The reduction in capacitance allows the PD or APD to have a shorter absorption length, which in turns result in a faster transit time for the photogenerated carriers to be swept out of the high field region. The absorption region typically is depleted as much as possible by the reverse bias voltage that is applied externally with an electric field strength approaching 10,000 V/cm or higher. If the microstructured pillars or holes can result in removing half or more of the semiconductor material, which for silicon has a dielectric constant of 11.9 and germanium have a dielectric constant of 16, replacing the removed material with either air (dielectric constant of 1) or polyimide (dielectric constant of 3.5) or other dielectrics with low dielectric constants, then the overall capacitance can be estimated to be the sum of the capacitance due to the total area occupied by the semiconductor and the capacitance due to the area occupied by air or polyimide. C(total)=C(semiconductor)+C(air or polyimide) where $C= \varepsilon A/d$ where ε is the dielectric constant times the free space permittivity ($8.854\ 10^{-14}$ farads/cm), A is the area occuped by the semiconductor or air/polyimide and d is the length of the "I" region which can be the absorbing region or the absorbing and multiplication region as in the case for APD. From the equation for C(total), the more semiconductor material which has a high dielectric constant removed and replaced by low dielectric material such as air/polyimide/ SiOx/spin on glass the lower the overall capacitance and the faster the RC time. This reduction of capacitance for PD and APD invention can be extended to other PD and APD such as those of III-V material, microstructures can be fabricated on its surfaces and extend into and pass the optical signal absorbing regions to remove half or more of the semiconductor material to reduce its capacitance and can effectively make a larger area PD/APD and have the same bandwidth as before etching microstructures on the device. The larger area allows for easier coupling of the optical signal to the

photodetector. A simple formula for the increase in radius for example by replacing semiconductor material with low dielectric material is: $r=(\varepsilon_1/((\varepsilon_1-\varepsilon_2)x+\varepsilon_2)))^{1/2} r_o$ where x is the fraction of semiconductor area left, ε_1 is the dielectric constant of the semiconductor, ε_2 is the low dielectric material such as air or polyimide or spin on glass, and r_o is the radius of the active area of the PD/APD before etching microstructured pillars and or holes. As an example, for a 20 micron diameter Ge photodiode with $\varepsilon_1=16$ and for simplicity $\varepsilon_2=1$ (air) and x=.5 (half of the semiconductor material is removed in the microstructured pillar or holes), the increase in the new radius with the same capacitance as the non-microstructured Ge PD is 13 microns or a diameter of 26 microns which is significantly larger than 20 microns and can significantly reduce the cost of coupling the optical signal into the microstructured large area photodetector. This reduces the cost of passive packaging of the optical receiver module and increase the yield.

[00163] FIGs. 19A, 19B and 19C are diagrams illustrating how mictrostructures can reduce capacitance of a photodiode such that a larger area photo diode can be fabricated with the same bandwidth and QE, according to some embodiments. FIG. 19A shows the bulk layers 1900 in an InP-InGaAs-InP structure. In FIG. 19B, the InP-InGaAs-InP layers with microstructured holes 1922 effectively reduce the capacitance of the photodiode 1920 to allow a larger area photodiode to be fabricated with the same bandwidth and QE. FIG. 19C is a top view showing PD 1920. The microstructured holes 1922 can be 100-1000 nm in diameter with depth of 0.1 to 3 microns. Also visible in FIG. 19C is contact ring 1930 and bond pad 1932. According to some embodiments, a complementary microstructured pillars can also be fabricated. According to some embodiments, the sidewalls of InP and InGaAs can be passivated with SiOx, SiNx (silicon oxide and silicon nitride via ALD or PECVD), polyimide or spin-on-glass that can be spun on using standard processing methods. The absorption coefficient of the bulk material can be enhanced by up to two orders of magnitude or more.

[00164] According to some embodiments, III-V material such as InP, InGaAs, InGaAsP, InAs, InSb, GaSb, InGaSb on Si, Ge on Si, is epitaxially grown in a sub micrometer selective area growth (SAG) or vapor liquid solid (VLS) (See, e.g. Sarkar et al, Heteroepitaxial growth dynamics of InP nanowires on silicon, Journal of Nanophotonics, Vol. 2, 021775 (12 February 2008); Roest, et al, Position-

controlled epitaxial III–V nanowires on silicon, Nanotechnology 17 (2006) S271–S275) heteroepitaxy using metal organic vapor epitaxy with or without catalyst which can consists of Au, Cu, Al, Ti, W, Fe, Cr to name a few. Also for vertical oriented microwires grown on silicon, wafers with surface orientation (111) are selected. It is not necessary that the microwires be normal to the surface, it can be off normal and even have a mixture of orientations.

[00165] In VLS growth, the silicon wafer that has the layer structure for APD or PD just prior to heteroepitaxial growth is photolithographically (or e-beam or nanoimprint lithographically) patterned with aperture ranging from 10-5000 nm, and spaced between 10-3000 nm. An Au deposition (e-beam, or thermal evaporation) follows with thickness of 0.1-10 nm, followed by a lift-off, VLS epitaxial growth in a MOCVD reactor.

[00166] For SAG growth (See, e.g. Chu et al, Wurtzite InP nanowire arrays grown by selective area MOCVD, Phys. Status Solidi C 7, No. 10, 2494 – 2497 (2010)), a 50 nm SiN_x is PECVD (or sputtered or ALD) deposited on a (111) oriented Si wafer with the necessary APD or PD epitaxial layers grown on it ready for heteroepitaxial growth. Using lithography (photo, e-beam or nanoimprint) apertures are defined with dimensions ranging from 10-5000 nm and spaced between 10-10000 nm followed by dry etching (RIE) to open a via to the silicon surface. The wafer is then ready for SAG of Ge, III-V microwires in a MOCVD reactor.

[00167] Detailed processes such as surface treatments, surface preparations, annealing, plasma etching, are not described for simplicity. These processes can be found in the literature.

[00168] FIGs. 19D and 19E are cross sections showing aspects of fabricating an APD device having a III-V absorbing layer grown on a P-I-N silicon multiplication layer, according to some embodiments. In FIG. 19D, a Si APD structure 1940 is etched as shown for v epitaxial growth of the III-V material. In FIG. 19E a III-V absorbing layer is grown on P-I-N silicon multiplication layer for APD device 1960. As in the III-V on Si for a PD device, the III-V nanowires or microwires can be grown on Si using VLS process with or without catalyst. Since the footprint of the nano/microwires on Si is of the order of a micron, defects due to stress from lattice mismatch are not a significant issue and high quality III-V nano/microwires can be

grown on Si. According to some embodiments, SAG is used for fabricating III-V microstructures on Si electronic gain layers.

[00169] From FIGs. 19D and 19E it can be seen that the InGaAs on Si APD 1960 starts with a Si APD structure 1940 where microstructures of holes or pillars are etched to the charge layer 1944 or just before the charge layer 1944. According to some embodiments, the microstructure holes and/or pillars can be etched into the multiplication layer 1942. Then using a process, for example SAG, with or without silicon oxide on the Si microstructure's sidewalls, I-InGaAs is grown, ending with P-InGaAs at the surface. Surface growth can use a process such as epitaxial lateral overgrowth (ELOG) to form a continuous P-InGaAs film of high quality. P ohmic alloy and bond metal 1966 are formed and annealed on the P-InGaAs. The back side processing consist of thinning the Si wafer using for example a BOX layer for selective etch stop and removing the BOX layer. Anti reflection can be coated on the backside silicon to reduce reflection. N ohmic 1968 is fabricated on the N Si layer. The optical signal is illuminated from the bottom. A reverse bias of -5 to -50 volts is applied to the cathode and anode. As mentioned earlier, the small footprint of the InGaAs on Si microstructure of the order of 10 square microns allows for high quality InGaAs material to be grown where lattice mismatch causing crystal defects are not significant.

[00170] According to some embodiments, the integration of Ge, III-V with Si PDs, PVs (See, FIG. 25C, *infra*.) and APDs allow the absorption spectrum of Ge and III-V material on a mature Si electronic platform. It allows integration of III-V with Si CMOS ICs for example for photodetector, optical light source such as light emitting diodes (LED) and laser diodes (LD) and III-V electronics such as transistors.

[00171] Multiple absorbing material and voids as microstructures. According to some embodiments, the microstructured pilllars and/or holes are regrown with Ge such that both Si and Ge are microstructured to enhance the bulk absorption coefficient. According to some embodiments, voids can also be buried or embedded to generate a buried/embedded microstructure such that the surface is more planar. The microstructured voids can also enhance the absorption coefficient, by being patterned so as to enhance reflection and also to reduce the effective refractive index of a material (e.g. Si), reduce the weight of the device,

and increase mechanical flexibility. The microstructured voids can be random, pseudo-random or patterned typically with dimension and spacing that are approximately the order of a wavelength or subwavelength. According to some embodiments, instead of combining Ge with Si, others combinations can be used for example III-V with Si or other semiconductor material, polymers, or other non semiconductor absorbers, which can significantly broaden the absorption spectrum over that of a single absorber.

[00172] The enhancement using nanowires (See, e.g. Garnett et al, Light trapping in silicon nanowire solar cells, Nano Letters, 2010, 10, 1082-1087; Kelzenberg et al, Enhanced absorption and carrier collection in Si wire arrays for photovoltaic applications, Nature Materials, vol. 9, March 2010, 239-244) and nanoholes (See, e.g. Lin et al, Optical absorption enhancement in silicon nanowire and nanohole arrays for photovoltaic applications, Proceeding of SPIE, Vol. 7772, 77721G-1, 2010) have been reported by various groups. The known use of nanowire for light trapping are for photovoltaic applications where the photogenerated carriers diffuse to the anode or cathode of a P-N junction with zero external bias, operating at DC (direct current). According to many of the embodiments described herein, the photogenerated carriers are swept out with an external reverse bias in the absorbing "i" region of a P-I-N diode (PD) or P-I-P-I-N diode (APD) for high modulation bandwidth (e.g. greater than or equal to 10 Gb/s bandwidth) and high quantum efficiency and for APD for high current gain (e.g. gain greater than 3 dB). In addition, according to some embodiments, multiple absorbing materials can be used to broaden the absorption spectrum. The multiple absorbing materials are connected in parallel as current sources whereas in known technology the absorbing materials are connected in series. In addition, the use of voids as microstructures to enhance the absorption of the material according to many embodiments described herein allows the surface to be more planar and simplify processing since fillers may be avoided. Also, the more planar surface allows the epitaxial growth of semiconductor Bragg reflectors to enhance reflection for double or multiple pass absorption in the I absorption layer of the PD/APD. According to some embodiments, Dielectric Bragg reflectors can also be used in a more planar surface since the surface can be highly N or P doped and the ohmic contact can be made on the periphery such as a ring ohmic contact and the

dielectric Bragg reflectors deposited on the photosensitive area such as shown in FIG. 29, *infra*. Chemical mechanical polishing (CMP) can be used to smooth the surface of the epitaxial layer with buried voids.

[00173] Further aspects of fabricating devices having microstructured Ge that is buried or embedded in Si microstructure will now be described. FIG. 20 shows bulk layers without a final P-Si layer for devices having microstructured Ge buried or embedded in an Si microstructure, according to some embodiments. The final P-Si layer, according to some embodiment will be the last layer grown in the epitaxial structure where the first layer grown is the layer adjacent to the substrate, followed by the second layer that is adjacent to the first layer, and so forth to the last layer grown. Shown in FIG. 20 is P-I-N PD structure 2000 and a P-I-P-I-N APD structure 2020 both without the final P-Si layer. In many of the embodiments described herein, N can refer to N (mid N type doping of 5. 10^{16} cm^{-3} to 8. 10^{17} cm^{-3}, low N doping less than 1. 10^{17} cm^{-3}, and high N doping greater than 5. 10^{17} cm^{-3}, with the same for P doping. I (or i) doping is commonly defined as intrinsic, or not intentionally doped or low doping back ground doping of less than 5. 10^{16} cm^{-3}. The "I" region is configured such that the field of a P-I-N junction is developed across the "I" region usually with an external reverse bias. In PD and APD applications, the absorbing material is in the "I" region so that the photogenerated carriers can be quickly sweep to anode (P) and cathode (N) layers. For APDs, the carriers (electrons in most cases shown here, since this gives the lowest noise APD) are swept to the second "I" region for multiplication (current gain) before transiting to the cathode layer). In the Figures herein, P-I-N, P-I-P-I-N structures are shown and the top P layer(s) that are in contact to external circuits are referred to as the anode and the N layer(s) that are in contact to external circuits are referred tp as the cathode; the layers can be interchanged from P to N and N to P with P or low dope substrates to also fabricate PD's and APD's.

[00174] FIG. 21 is a cross section showing etching of microstructured pillars and/or holes for devices having microstructured Ge buried or embedded in an Si microstructure, according to some embodiments. The microstructure pillars 2104 and/or holes 2102 are etched into the I-Si layer, partially or entirely or to/into the N (PD structure) or P (APD structure) Si layer. The etching process can be one of the following: wet chemical etching, dry etching using reactive ion etching (RIE), a

deep reactive ion etching (DRIE), ion milling, and/or focused ion beam milling. The etching can be isotropic or anisotropic or a combination of isotropic and anisotropic. As shown in FIGs. 22 and 23, *infra*, Ge is then regrown in the etched region (i.e. the area around the pillars and on the sidewalls of the pillars in the case of pillars, or area in the holes, sidewalls of the holes in the case of holes) isotropically, anisotropically, or by selective area growth (SAG) where a dielectric layer such as SiOx, SiNx, cover area where regrowth of Ge is not desired which in some embodiments can include the sidewalls. During etching if a dielectric mask material such as SiOx, SiNx, SiCx is used and left in place during epitaxial growth, the epitaxy layers may not grow on the dielectric mask in a crystalline film and may be amorphous in nature or may not grow on the dielectric layer other than some dendrites. Note that the isotropic or anisotropic growth rate often depends on the crystal plane it is growing on and any etched structures may expose multiple crystal planes resulting in different growth rates at those planes that can lead to anisotropic growth in the etched regions with 3D microstructures.

[00175] Growth of Ge on Si is well documented in the literature where a thin buffer Ge layer is first epitaxially grown at a lower temperature followed by a higher temperature Ge epitaxial growth using chemical vapor deposition (CVD), molecular beam epitaxy (MBE), atomc layer deposition (ALD), low pressure -CVD, and or a combination of growth techniques, for example the thin Ge buffer layer can be grown by MBE and the high quality thicker Ge film grown by CVD. The thin Ge buffer layer is to allow lattice mismatch stress to be accommodated between Si and Ge, (see, e.g. Feng et al, High-speed Ge photodetector monolithically integrated with large cross-section silicon-on-insulator waveguide, APPLIED PHYSICS LETTERS 95, 261105 ,2009).

[00176] The Ge regrowth may have voids or non-planarities and, where useful, the surface can be planarized using polishing such as chemical mechanical polishing (CMP) or etching. FIG. 22 is a cross section showing a device having microstructured Ge buried or embedded in an Si microstructure, after the Ge "I" layer is grown in the etched region and planarized, according to some embodiments. Note that according to some embodiments, planarization is not needed and is omitted. After the Ge "I" layer 2202 is grown and planarized, a P^+ Ge capping layer 2204 is grown to complete the P-I-N structure of a PD or P-I-P-I-

N structure of an APD. Optical signal or photons with wavelengths ranging from 400 to 1800 nm can illuminate the PD/APD 2220 from the anode (top) side (P^+ side) 2202 and optical signal or photons with wavelength ranges 950-1800 from the substrate side (bottom) since Si is mostly non-absorbing at these wavelengths. According to some embodiments, it is advantageous to configure the device 2220 for illumination from the substrate side since this will allow a double bounce of the optical signal or photons within the absorbing Ge microstructures embedded in Si. Shown in these figures are only the basic epitaxial layer structures. Structures and layers not shown for simplicity include: anti-reflection coatings, passivations, ohmic metals, bond metallization, any metal interconnect to CMOS, via's for electrical connectivity, arrays of PD/APD for multichannel optical interconnects, to name a few. Optical signal/photons can illuminate either normal to the surface or at any angle off normal, including rotation angles for optimal PD/APD performances; optimizing QE and bandwidth of the PD/APD.

[00177] FIG. 23 is a cross section showing a device having microstructured Ge buried or embedded in an Si microstructure, after I-Ge regrowth and planarization, and a cap layer of P-Si, according to some embodiments. In the case of FIG. 23, the buried Ge microstructures 2302 are capped with a P^+ Si layer 2304. The Si P^+ cap layer (anode) 2304 has low optical loss at optical wavelengths of 950-1800 nm and therefore generates minimal photocarriers that are not in the high field "I" region of the PD/APD 2320 and contribute minimal diffusion photocurrent which can lead to a degradation of the frequency response of the PD/APD 2320 and the QE of the PD/APD.

[00178] Some dimension doping ranges for the buried or embedded Ge and capping layers shown in FIGs. 20-23 will now be provided in greater detail, according to some embodiments. The dimension of the microstructured Ge (e.g. 2202 and/or 2302) can range in depth from 0.1 to 5 micrometers, have a lateral dimension range from 10-5000 nm, and a spacing between adjacent microstructure structures (the structures can be identical or non-identical) in contact (overlapping) to 5000 nm. The "I" doping for both Ge (2202 and/or 2302) and Si (2104) is less than or equal to 5. $10^{16}/cm^3$. "I" is often called intrinsic or not intentionally doped and can have either a p or n background doping, the doping level is low enough that a reverse bias voltage of -2 to -45 volts can fully deplete the "I" region of

mobile holes or electrons (carriers). The capping layer, Si (2304) or Ge(2204) thickness can range from 0.1 to 5 μm with doping level greater than or equal to 6. $10^{17}/cm^3$. These parameters can be adjusted to other values, but the goals are to increase or optimize the QE and bandwidth of the PD/APD for a given application. Series resistance, photogenerated diffusion current, ohmic contacts, capacitance, transit time, depletion of the "I" absorption region all contribute to the performance of the PD/APD. In addition for double/multiple bounce within the "I" region for optical signal illuminating from the bottom substrate side, a reflective metal or dielectric stack such as a Bragg refelctor/mirror consisting of alternating dielectric layers of different refractive indices or HCG can be used to reflect the optical signal back into the microstructured absorbing region at the top anode side. With the Si cap layer as in FIG. 23, the optical signal can illuminate the Si P^+ cap layer (anode) 2304 and, since Si has minimal losses at 1100-1800 nm (below bandgap radiation), it can also have double bounce of the optical signal within the microstructured buried/embedded Ge 2302 by providing a reflector such as a Bragg reflector epitaxially grown at the Si N^+ layer or at the Si substrate to reflect the light back into the absorption region.

[00179] According to some embodiments, all the discussions of microstructured layers herein, light can additionally impinge from top and bottom surfaces, as well as on the sides of the microstructures, either directly or from scattering, near field effects, interferences, or resonance, which can vastly improve the QE of the microstructured photosensors since photogenerated carriers are generated directly in the high field absorbing "I" ("I") layer(s).

[00180] According to some embodiments, dopant choices for Si and Ge (group 4 elements) include the following: (1) for donors (n-type) from group 5 elements - antimony, phosphorus, and arsenic; and (2) for acceptors (p-type) from group 3 elements - boron, aluminum, and gallium.

[00181] It is also noted that in the structure shown in FIG. 23, the I-Ge microstructures 2302 buried in Si 2104 are completely surrounded by Si which has a lower refractive index than Ge. At 1000-2000 nm wavelength range, the refractive index of Si is approximately 3.49 and for Ge is 4.1. The index ratio of Ge/Si is 1.17 so according to Chang-Hasnain reference, HCG effects will exist. The resonance and field concentration in the absorbing Ge microstructures can further enhance

the absorption coefficient from that of the bulk absorption coefficient value anywhere from greater than 1X to several orders of magnitude. The index difference also causes light to be confined and concentrated in the high index material, in this example, Ge; further improving QE.

[00182] The silicon (Si) microstructure can detect photons with wavelength ranging from 300-1100 nm and the germanium (Ge) microstructure can detect photons with wavelengths ranging from 300-1800 nm. According to some embodiments, for high bandwidth and high QE, the shorter wavelengths, 300-600 nm, may generate photocarriers outside the "I" region resulting in a diffusion current that can result in non-optimal bandwidth and or QE. Where bandwidth is not an issue, the degradations may not be very significant.

[00183] FIGs. 24A and 24B are cross sections showing aspects of a microstructured APD with buried/embedded I-Ge absorbing microstructures in I-Si microstructures, according to some embodiments. FIG. 24A shows the bulk layers 2400. In FIG. 24B, the etched pillars 2424 and/or holes 2422 are filled with I-Ge (intrinsic-Ge, non-intentionally doped or undoped or low doped Ge) and finished with a capping layer 2426 of P^+ Ge or Si to complete the anode of the APD 2420. The microstructured Ge 2422 is buried/embedded in Si 2412. Optical signal of wavelength 950-1800 nm (or photons from 300-1800nm where the shorter wavelengths, 300-900 nm, may not have as high a bandwidth) can illuminate the APD 2420 from either top or bottom at various angles to the normal and/or normal to the surface. According to some embodiments, the starting layers prior to the I-Ge regrowth into the etched regions can also include the P^+ Si layer 2426, such as shown in FIG. 7 with layer 726, *supra*. In the case shown in FIG. 24B, the starting layer was removed to minimize P dopant diffusion during I-Ge regrowth. The buried or embedded Ge microstructure in Si microstructure allows the APD (or PD) 2420 to operate in two regimes. A first regime is at wavelengths where Si is low loss and Ge is absorbing or high loss (950-1800 nm). In this Si low loss regime, the Ge microstructures 2422 with a Si P^+ anode cap layer 2426 is completely buried in Si which has a lower refractive index than Ge. The Ge microstructure arrays can have HCG low Q with Q ranging from 1 to 3000 approximately (or other resonant, scattering, near field, linear and non-linear optical effects) or high enhancement of the absorption coefficient. A second regime is where both Si and

Ge are absorbing, 300-945 nm, and both Si microstructures 2424 and Ge microstructures 2422 work in parallel (parallel current generators) absorbing the photons with enhancement of the absorption coefficients of both Si and Ge. This is particularly advantageous for examples in photovoltaic applications.

[00184] FIGS. 25A - 25C are cross sections showing aspects of a photodiode having buried/embedded Ge microstructures in a Si microstuctured pillar and/or hole array, according to some embodiments. Starting with a Si PD epitaxial layer structure 2500 with or without the P layer 2526, microstructures of holes 2522 and/or pillars 2524 are etched into the Si P layer 2526 and I layer 2512 and can extend into the N layer 2510. Regrowth of Ge 2522 (or III-V material such as InGaAs, InAs, InSb, GaN, InGaN to name a few) using a process such as SAG with our without silicon oxide on the sidewalls of the Si microstructure 2524 or using a process such as VLS with or without catalysts, the I-Ge layer 2522 is grown followed by P Ge 2526 (or a P-Si layer which may be more suitable for top illuminated devices) at the surface where a process such as ELOG can be used to form a contiunous P-Ge film. P ohmic alloy, annealed, followed by bond metallization completes the contact 2528 for the anode. The back side processing as discussed earlier is deposited on the silicon surface to reduce reflection. See, e.g. FIGs. 19A-19C, *supra*, where the silicon is thinned and etched to the BOX layer selectively. The BOX layer is etched selectively and an anti reflection N ohmic alloy is formed on the N-Si layer, annealed and followed by bond metallization, which completes the cathode contact. Reverse bias of -2 to - 10 volts is applied between the anode and cathode for high bandwidth PD applications. In PV applications, 0 bias is applied.

[00185] According to some embodiments, the dimensions and doping are similar to the Si microstructured PD shown in FIGs. 5A-5B, *supra*, with the I-Ge doping level less than 5. 10^{16} cm^{-3}, and dimensions ranging in thickness of 0.1 to 5 micrometers, and lateral dimension of the microstructure ranging from 10 to 5000 nm with adjacent structures that can touch/overlap to 5000 nm separation. Optical signal/photons can either illuminate from the anode top side or cathode bottom side with wavelength range of 300-1800 nm and normal to the surface or at an angle to normal which can also include rotation. For bottom side illumination, the Si is thinned down to a few micrometers thickness for illumination at wavelength

ranges of 300-900 nm. Only the basic layers are shown for simplicity. For example, the following structures are not shown: isolation mesa or diffusion or ion implantation, passivation, anti-reflection, ohmic metal, guard rings (e.g. for an APD). Both Si microstructures and Ge microstructures can detect the optical signal/photons in parallel for wavelengths where both are absorbing, 300-1100 nm, and only the Ge microstructure at wavelength ranges 900-1800 nm. The cap layer 2526 and 2546 in FIGs. 25B and 25C respectively can be either P^+ Si or P^+ Ge. For broad modulation bandwidth (sometimes just referred to as bandwidth) of greater than 10 Gb/s (gigabits per second), P^+ Si cap layer is preferred for wavelengths ranges from 950 to 1800 nm, since at these wavelengths Si has low optical losses (also referred to low loss). According to some embodiments, the structure shown in FIGs. 25B and 25C can also be use for photovoltaic applications where no external bias is purposely applied in the reverse direction.

[00186] According to some embodiments, for all the structures shown, the P and N can be interchanged to form for example N-I-P structures for the PD and PV (photovoltaic) and N-I-N-I-P structures for the APD.

[00187] The regrowth of Ge microstructures in Si also have applications in photovoltaic devices where the device is operated without external reverse bias. The P-I-N PD structure for example with Ge microstructures embedded or buried in Si microstructures effectively have two bandgaps, Si bandgap and Ge bandgap that is exposed to the solar radiation. The combination of two bandgaps widen the absorption spectrum of the photovoltaic device and therefore can collect a broader spectrum of the solar energy. The two bandgaps can have a higher QE and or short circuit current over that of single bandgap photovoltaic devices or multiple devices connected in series. The microstructures also have enhanced absorption that can further improve the QE and or short circuit current of the photovoltaic device. The solar spectrum at AM 0 and AM 1.0, with a photovoltaic device with a spectrum width of 300-1800 nm, at least approximately 90% of the solar spectrum is captured. In addition, in the PV device with Ge and Si microstructures are adjacent laterally to each other (i.e. in parallel) rather than being vertically adjacent (i.e. in series) as in prior art PVs. This allows the Si and Ge to be exposed to solar photons equally and are parallel current generators that are additive; $I_{Si} + I_{Ge} = I_{total}$

where I_S is the photocurrent generated by the Si microstructures and I_{Ge} is the photocurrent generated by the Ge microstructure and I_{total} is the total photocurrent.

[00188] Although according to some embodiments the use of Si and Ge are described, according to some other embodiments, other materials are used. According to some embodiments, Si is used with an InP microstructure embedded or buried. According to some embodiments, more than two materials are used such as Si, Ge, InGaAs, InP, GaAS, GaN, InGaN, InSb, to name a few. The microstructures, in addition to pillars and holes, can be embedded and or buried to use the effects of HCG to enhance the absorption coefficient over that of bulk absorption coefficient to further improve QE and minimize the use of material in order to reduce cost of manufacturing.

[00189] FIG. 25C is a cross section showing grown Ge, InP, InGaAs to name a few, within silicon microstructures. SAG can be used where the sidewalls of the microstructures are oxidized or coated with a conformal dielectric and where the oxide/dielectric is removed at the bottom of the microstructure surface where it is approximately parallel to the silicon substrate where it can provide crystalline information for the growth of Ge, InP, InGaAs microstructures. The area where the Ge, InP, InGaAs will epitaxially grow with or without catalysts using various growth methods such as VLS, MOCVD, CVD to name a few, is approximately 100 square microns or less; more typically around 0.3-3 square microns. Because of the small area, crystalline defects due to lattice mismatch are not significant. The sidewalls with the silicon dioxide that can be thermally grown or deposited using ALD, provide an electrical insulation between the Si and the Ge, InP, InGaAs SAG grown layer. It should be noted that SAG growth can continue until the Ge or InP or InGaAs (to name a few) can merge above the silicon microstructure and with lateral over growth (LOG) epitaxial process, the microstructures of Ge or InP or InGaAs can form a continuous epitaxial thin film layer that can be doped P type for the anode layer.

[00190] FIGs. 25D and 25E are cross sections showing aspects of a forward biased device such as a vertical cavity surface emitting laser (VCSEL), according to some embodiments. VCSEL 2562 can also be fabricated using similar processing as described *supra* for the PDs, PVs and/or APDs. Starting with a Si PIN structure 2562, Si microstructure hole(s) 2564 are etched through I-Si layer

2566 to the N-Si layer 2568. According to some embodiments, the etching of hole 2564 can extend into the N-Si layer 2568. An SAG process is followed with or without silicon oxide on the Si microstructure sidewalls (oxide 2570 is shown). First, a GaAs/AlGaAs distributed Bragg reflector 2572 (DBR) all N type is grown, follow by N-GaAs 2574, The active layer 2576 is undoped InGaAs/GaAs multiple quantum well (MQW) of 1-5 wells, followed by P-GaAs 2578 to the surface and using ELOG which can form a continuous film at the surface of the I-Si 2566. Dielectric DBR 2582 on the P-GaAs 2580 completes the optical cavity. P ohmic alloy with anneal and bond metal 2584 on P-GaAs 2580 completes the anode contact and N ohmic alloy with anneal and bond metal 2582 on N-Si 2568 completes the cathode contact. Forward bias of 1 to 20 volts to the anode and cathode will result 1200-1300 nm light to be emitted from the VCSEL 2560.

[00191] The design and growth of VCSELs at 1200-1300 nm and other wavelengths are known. See, e.g. "High-performance 1200-nm InGaAs and 1300-nm InGaAsN quantum-well lasers by metalorganic chemical vapor deposition", Tansu et el; Selected Topics in Quantum Electronics, IEEE Journal of (Volume: 9, Issue: 5), 2003.

[00192] According to some embodiments, longer wavelength are selected when embedding InGaAs, InGaAsN and other III-V material, because at wavelengths greater than 1000 nm silicon is mostly transparent and does not introduce excess additional optical losses. Accordingly, Si is a good heat sink for the VCSEL 2560. According to some embodiments, the GaAs/AlGaAs DBR 2572 is replaced with a silicon/air or a dielectric DBR on the bottom by thinning the Si wafer and etching to the BOX layer, removing the BOX layer and depositing a dielectric DBR. Design of DBR, dielectric and semiconductors are well known. The silicon/air DBR will require further processing, using sacrificial layers such as Ge that can later be selectively etched away via etch trenches.

[00193] According to some embodiments, an LED is fabricated by applying minor variations, including removing the DBRs and adding multiple Si microstructures. The LED can use MQW or just a simple heterojunction of P-GaAs/I-InGaAs/N-GaAs for example. Other semiconductors can also be used such as InGaAsN, InGaAsP, GaAsN, to name a few. The substrate can be another material such as sapphire, SOI, insulator on Si (IOS), ceramic, glass, quartz, GaN,

crystalline or non-crystalline. Addtionally, other material for blue/UV LEDs such as GaN, AlGaN, GaInN, AlN, can be grown using epitaxial reactors and methods of fabrication described above.

[00194] According to some embodiments, voids are formed, that are buried or embedded in Si or Ge on Si or Ge. As used herein "buried" refers to cases when the void is beneath the surface, and "embedded" refers to cases when the void can intersect or be slightly above the surface. As described *supra*, during regrowth of Ge on a microstructured Si with pillar and/or hole arrays, voids can develop due to the fact that growth rate during epitaxial growth often depends on the crystal orientation of the surface. Since etching microstructured pillars and/or holes in Si can expose different surface orientation of the side walls, asymmetric growth rate of Ge on these different Si surface orientation can result in void formation. According to some embodiments, the void formation is exploited to generate a buried and/or embedded microstructured void arrays that can behave as HCG and or light trapping structures that concentrate the optical field and/or resonance through interference of the optical field (amplitude and phase), scattering, near field, linear and non-linear optical effects to enhance the bulk film absorption coefficient by one to several orders of magnitude. In addition, the voids can be used to reduce the effective refractive index of a material (e.g. Si with voids) since the optical field sees an average or effective refractive index. At dimensions on the order of a wavelength or less, the refractive index of voids and Si, for example, can be approximated with an effective refractive index which is the average of the volume occupied by Si and the volume occupied by the void. For example, if Si occupies 1/2 the volume and voids occupy 1/2 volume, the Si index is 3.49 and the void is 1.0 (for air), then the average effective index is approximately 2.25.

[00195] The voids also reduce capacitance of the device if the voids are generated in the "I" region, as discussed *supra*; where the space between microstructured pillars or the microstructured holes can reduce the capacitance of the P-I-N PD diode or the P-I-P-I-N APD diode. The voids according to some embodiments are either buried (buried holes) or embedded (space between pillars) and the total capacitance is approximately the capacitance of the total area occupied by the voids plus the capacitance of the total area occupied by the semiconductor. In the case where the voids do not occupy the full thickness of the

"I" layer (i.e. only occupy part of the thickness), then the effective dielectric constant can be estimated by taking into account a volume that contains both the void and the semiconductor extending through the thickness of the "I" layer, the volume of the void and the volume of the semiconductor in a given volume; for example if the voids occupy 1/2 of a given volume of the thickness of the "I" layer and the semiconductor material occupies 1/2, and if the semiconductor material is Si with dielectric constant of 11.9, then the average effective dielectric constant is approximately 6.5, where the void is assumed to be air with dielectric constant of 1 for that given volume. The total area occupied by this effective dielectric constant, consisting of both voids and semiconductor material, is used in the capacitance calculation plus the area occupied only by semiconductor in the "I" region to give the total capacitance of the P-I-N or P-I-P-I-N diode. Reduction of capacitance leads to a reduction in RC time constant for the diode which improves the bandwidth of the PD and APD.

[00196] Although buried voids in semiconductor material are known, such voids are conventionally regarded as detrimental and as such are to be avoided. According to some embodiments, such voids are intentionally created and form useful features in the semiconductor material.

[00197] FIG. 26 is a cross section showing starting epitaxial layers in which mictrostructured voids are fabricated, according to some embodiments. To generate voids in PD, PV and APD structures start with a structure 2600. The starting material can be a Si PD or APD structure with or without the Si P^+ anode layer. Details of the layers are not shown for simplicity.

[00198] FIG. 27 is a cross section showing microstructured holes/pillars etched into the I-Si layer, according to some embodiments. The microsctured holes 2722 (or space around pillars) are etched into the Si "I" layer and can extend pass the "I" layer or can be partially into the "I" layer. Wet and/or dry etching can be used or a combination of wet chemical and dry etching (RIE, DRIE for example) where the wet etching can be used to remove damage due to dry etching or wet etching in combination with dry etching and oxidation to form a certain shape or surface smoothness. As shown in FIG. 27, the etch can be isotropic or anisotropic, the sidewall can have negative or positive slope (slope defined with respect to the plane of the substrate). For anisotropic etching both negative and positive slope

can exist at the same time for an etched feature such as a pillar or hole. Anisotropic epitaxial growth can result in void formation, with the shape of the void being determined by many factors including: side wall slope, crystal orientations of the side wall, growth conditions, pressure, temperature, flow rate, growth technique (CVD, MBE, ALD or a combination of growth methods), surface preparation, and surface oxidation. According to some embodiments, surface oxide, partial oxide or other dielectric 2726 can be intentionally deposited on the side walls, which can also influence the regrowth of Si or Ge (or any other semiconductor such as InP, GaAs, InGaAs, GaN, InGaN, to name a few) and can be used to form voids.

[00199] FIG. 28 is a cross section showing microstructured voids buried or embedded in Si with a Si capping P^+ anode layer 2826, according to some embodiments. The buried voids 2800 can be uniformly spaced, or with chirped spacing, or any complex patterns with a combination of periodic and aperiodic spacing or it can be random or pseudo-random. The buried voids 2800 can have a length ranging approximately from 0.1 to 10 micrometers and lateral dimension ranging from 10-5000 nm. The voids can also be overlapping one another. Although FIG. 28 shows buried voids in Si, according to some embodiments buried voids can be formed in Ge. For example, in a Ge epitaxial layer on Si, or any other semiconductors, such as InP, GaAs, InGaAs, GaN, InGaN, InGaAsP, and other semiconductors in the III-V material family. The voids can be non-uniform is size and shape within the void and adjacent voids. The voids may also have non-uniform spacing and/or orientation. However, with proper process control uniformity in size and shape, patterning, random and pseudo-random placements of the voids can be attained. For simplicity the voids are shown to be uniform.

[00200] FIG. 29 is a cross section showing Bragg reflectors formed on the P-Si surface to provide a highly reflective mirror, according to some embodiments. With a more planar surface, high reflectivity Bragg reflectors 2900 may be deposited or grown using dielectrics or semiconductors on the P silicon layer 2826 surface. The ohmic contact and the bond metallization 2902 can be on the peripheral in a ring configuration as shown in FIG. 29. Optical signal illuminating from the bottom will have a double/multiple pass through the absorbing I region thereby improving QE and the bandwidth of the PD/APD. In PV where bandwidth is not an issue, then the QE will be improved. According to some embodiments,

Bragg reflectors 2900 can be configured for wavelength selectivity so as to reflect the optical signal back into the absorbing I region.

[00201] According to some embodiments, voids are not only in the I region but are also formed in the P and/or N region of a PIN PD or PV, in the P charge region, in the I multiplication region and/or the P anode and N cathode region of an APD. According to some embodiments, voids can also be formed in the substrate. The density, shape and material (voids can be filled with different material from vacuum, gas, helium to dielectrics with or without doping with rare earth elements for optical gain for example, carbon/graphene/diamond,copper, ceramics for thermal conductivity for example) of the voids in each layer can be different or the same, or different/same within the same layer.

[00202] According to some embodiments, voids are also used to make the material more mechanically flexible and bend and or conform to different surface contours. For example, in PV applications where large sheets of the device are fabricated, the sheets can conform to contours in for example the roof, or the sheets of semiconductor PV can be rolled for compactness in storage prior to deployment. According to some embodiments, voids sized between 0.01 microns and 1000 microns are introduced into semiconductor and/or glass material for use with photo voltaics for purposes of increasing flexibility and/or resistance to physical damage and/or damage propagation.

[00203] High-density voids in semiconductors are also resistant to crack propagation since the crack will terminate at a boundary, in this case the boundary of the void. This is advantageous for large devices such as solar cells where if an object such as hail or stone strikes the solar cell, only the point of contact will be damaged and perhaps a small adjacent area (5-50% of the diameter of impact for example) where the damages are localized to area of impact and cracks will not propagate across the entire cell. A device may survive such small damage events with minimal degraded performance without taking the entire solar panel down.

[00204] According to some embodiments, the voids are also formed in other materials also such as glass, ceramics, polymers, metal, plastics, to name a few, to avoid crack propagation in case of foreign object impacts since cracks will terminate at a boundary, in this case the boundary at the void.

[00205] FIG. 30 shows an example of a PIN PD/PV structure 3000 with microstructured voids to enhance absorption, reduce bulk refractive index, reduce capacitance and increase mechanical flexibility of large sheets of PV on semiconductor material, according to some embodiments. The Si substrate is removed leaving only the BOX/SOI layers together with the PIN epitaxially grown layers. Ohmic contacts, bond metallizations, antireflection coatings, passivations, are not shown for simplicity. In addition to PV, the techniques are also applicable to PD, APD, light emitters such as light emitting diodes and diode lasers, and to electronic integrated circuits such as CMOS and ASIC (application specific integrated circuits) where voids can not only make the material more flexible and lighter but also as mentioned earlier more resistant to cracking. The voids, according to some embodiments can be filled with a gel that can repair impact damage and seal exposed cracked edges to prevent further deterioration due to moisture for example to the semiconducting surfaces. The gel can be spin on glass for example. According to some embodiments, the voids can be filled with material to enhance thermal conductivity for example, reduction of optical or microwave losses by removing the silicon and replacing with material that is not lossy such as Ar, He, Xe, N_2, Ne gas, or vacuum for example. The voids can have different sizes and shapes and densities and can be random, pseudo random, aperiodic, periodic, chirped, single or multiple patterns. The voids can also be in a single layer or in multiple layers of the device. Fig. 30, for example, shows the voids in P-Si layer 3002, I-Si layer 3004, and N-Si layers 3006 and 3008. According to some embodiments the index of refraction near the uppermost surface can be altered to more effectively index "match" with surrounding air so as to reduce reflections of incident light. For example, in PV applications near surface voids can be used to index match such that less incident sunlight is reflected from the PV surface. According to some embodiments, the index of refraction at lower surfaces can be altered so as to increase internal reflections that may, for examples, increase the number of passes light makes through an absorbing region.

[00206] According to some embodiments, random voids can also be generated by dry etching/electrochemical etching the surface of the semiconductor without any mask. Generating semiconductor nanowires followed by epitaxial regowth on these random nanowires will result in buried voids. As discussed in Frajtag et al,

Growing thin films that contain embedded voids, 23 June 2011, SPIE Newsroom; DOI: 10.1117/2.1201105.003750, this method can be used in GaN light emitting diodes to minimize defect formation due to lattice mismatch of the GaN epitaxial layer with the substrate which can be sapphire, Si, SOI, IOS to name a few. The random formation of semiconductor nanowires by dry etching of the surface of the semiconductor (which can be Si, Ge, III-V material family such as InP, GaAs, InGaAs, InGaAsP, GaN, InGaN, InSb, to name a few) without any mask and subsequently regrowing on the nanowires epitaxially using CVD for example, to form random buried voids can also be used to reduce the effective refractive index of the semiconductor and reduce the effective capacitance of the P-I-N, P-I-P-I-N diodes if the voids are formed in the "I" absorption layer and/or P, N layers, and/or charge, multiplication layers of the PD, APD, in any combination to optimize the performance of the device in bandwidth, QE, and energy consumption.

[00207] Fig. 31 is a cross section showing regrown I-Ge with a buried/embedded voids, according to some embodiments. The regrowth of Ge 3104 epitaxially on Si microstructured pillars and/or holes results in voids 3102 in the Ge layer that can be intrinsic or non-intentionally doped or low doped using the method shown in FIGs. 27-28, *supra*. In addition, selective masking with dielectric such as SiOx, SiNx for example can be used to generate nanowires only in the selected areas such as the Ge regrowth, for example, and with additional regrowth of Ge, random voids can be buried only in the selected Ge areas. The random voids can be combined with patterned voids to optimize a device performance in terms of bandwidths, quantum efficiencies and power consumption. The microstructures shown in FIG. 31 combine the Ge microstructure and void microstructure to enhance to bulk absorption coefficient and reduce the effective capacitance of the diode.

[00208] Fig. 32 is a cross section showing a device having buried microstructured voids in I-Si with regrown I-Ge and capped by an epitaxial layer, according to some embodiments. As can be seen in FIG. 32, the buried/embedded microstructure voids 3202 can be in I-Si layer 3200 while the Ge microstructure 3104 is also buried/embedded in Si layer 3200 using a few additional processing steps. First the voids 3202 are buried/embedded as in FIG. 28 with or without the P-Si anode layer 3226. Microstructures are then again

etched into the I-Si layer 3200 with the voids and then Ge 3104 is regrown resulting in a microstructure with voids 3202 in the Si layer 3200 and a Ge microstructure 3104 to enhance the bulk absorption coefficient and reduce the capacitance of the diode. Not shown is that the microstructured voids can also be buried/embedded entirely in Ge for Ge on Si layers, such that in Fig. 28, if the I-Si layer 3200 is replaced with I-Ge followed by a P^+ Ge capping anode layer 3226.

[00209] The buried/embedded microstructure voids is an inverse HCG structure with absorption, or a lossy HCG structure, and can have resonance, constructive and destructive optical interference effects of both phase and amplitude that can result in the enhancement of the bulk absorption coefficient. The period of the microstructure pillar, hole, void, buried/embedded Ge arrays can fall in the near-wavelength regime of the HCG effect or it can fall in the subwavelength regime where the grating period is much less than a wavelength and the diffraction regime where the period is greater than a wavelength. The HCG characteristics of the microstructure array and the input optical signal can be coupled to in-plane optical modes. The microstructured arrays can also behave as a lens to mode match the incoming optical signal. Good coupling efficiency also improves the overall QE of the PD/APD. According to some embodiments, a lossy HCG is provided where the absorbing region is a part of or included in the HCG structure (other effects such as scattering, near field, plasmonic, resonance, linear and non-linear optical effects to name a few, can also play a significant role in absorption enhancements), and where Si can be the HCG for photon energies that are below the Si bandgap and the Ge microstructures are buried or embedded within the Si that is absorbing to the photons with wavelength ranging from 950-1800 nm (where Si has relatively low optical losses).

[00210] According to some embodiments, the microstructures of holes, pillars, and voids can be arranged in any pattern or no pattern in the active area, including any parts of the P-I-N structure of a PD or P-I-P-I-N structure of an APD; the active area includes the absorbing "I" region and the P and N regions. According to some embodiments, to simplify manufacturing and to improve yield, the microstructures can extend outside the active areas of a PD/APD if it does not interfere with the PD/APD operations and performance. FIG. 33 is a top view showing distribution of microstructured pillars, holes and/or buried voids in an PD/APD, according to some

embodiments. The microstructure array 3300 consists of pillars, holes, and/or voids, and buried/embedded Ge in Si or Si in Ge or any combination of multiple semiconductors, can be distributed over the entire active area 3302 of the photodiode or avalanche photodiode or just partially for example in the center where the optical intensity is the highest. The active area can be defined as any area that contributes to the generation of electrical signal upon illumination with optical signal, or in the case of a PV, the generation of electricity upon illumination with photons. In FIG. 33, the active area 3302 is commonly the area within the metal ohmic contact/bond metal ring 3304. The distribution of the array 3300 can be non uniform, non periodic, non uniform is size of the microstructure, or in shape.

[00211] FIG. 34 is a top view showing distribution of microstructured pillars, holes and/or buried voids in an PD/APD, according to some other embodiments. In FIG. 34, the QE is optimized at the center of the active area where the optical intensity is the highest and away from the center, more semiconductor material is removed in the microstructure pattern to reduce the capacitance of the active area in order to decrease the RC (resistance, capacitance) time constant to achieve higher bandwidth for the PD/APD and or to increase the active area to allow passive alignment of the optical signal to the PD/APD thereby reducing the cost of packaging and assembly. Microstructured pillars/holes/buried voids 3400 near the center of the PD/APD optimize QE while the microstructured pillars/holes/buried voids 3410 at the periphery of active area 3402 minimize capacitance while still maintaining good QE.

[00212] Buried voids in the N (or P if P and N are switched) part of the P-I-N or P-I-P-I-N diode structure can reduce the effective refractive index of the semiconductor in the N layer. This is useful in increasing the refractive index contrast for HCG structures (to include other possible optical effects that may be significant in absorption enhancements such as scattering, plasmonic, near field, linear and non-linear optical effects to name a few), for example in Si the refractive index is approximately 3.5 (for wavelengths 950-1800 nm) and if half of the volume of the material is air, then the effective refractive index (1/2 air and 1/2 Si) would be approximately 1.8 for the air-Si composite material. Any semiconductor microstructures of pillars or holes fabricated on top of this composite air-Si material will have a index contrast of, for example Si pillars on the composite air-Si layer,

approximately 2. The high index contrast would enhance the performance of the HCG. According to some embodiments, this is used to enhance the lossy HCG performance (where loss can be as high or higher than - 1 dB/cm) and enhance the absorption coefficient with its resonance, light concentration and in-plane light coupling effects to name a few. There is an advantage in having the voids in the N and or N^+ layers since it will have a minimal effect on the electrical properties and characteristics of the diode since once electrons are swept into the N and or N^+ layer, they are majority carriers.

[00213] The microstructured voids in the N and or N^+ layer can be patterned, non-patterned or random or pseudo-random, and can be defined using lithography, masking and etching or just etching followed by a regrowth of Si, or Ge or any other material. The voids can range in length approximately from 0.01 to 10 micrometers and lateral dimensions can range approximately from 10-5000 nm with spacing between adjacent voids ranging approximately from overlapping to 5000 nm.

[00214] Fig. 35 shows the basic epitaxial structure 3500 for a conventional Si PV/PD diode on N Si substrate. FIG. 36 shows the structure of FIG. 35 with microstructured voids incorporated into the N-Si layer, according to some embodiments. The doping and thickness of the layers are dependent of the applications. For high bandwidth PD applications the "I" Si thickness ranges from 0.1 to 3 micrometers whereas for PV applications the "I" Si thickness ranges from 1 to 20 micrometers with doping range of intrinsic or not intentionally doped, background doping of $< 5.\ 10^{16}\ cm^{-3}$. Device size to define the area of the capacitance for high bandwidth PD (for circular apertures) ranges from 5 to 100 micrometer diameter whereas for PV, the lateral dimension can range from 0.1 to > 50 cm (centimeters) limited only by the size of the wafer or substrate. The doping ranges and layer thicknesses for non "I" layers are similar for PV, PD and APD; P or P^+ layer thickness ranges 0.1 to 3 micrometers P doping $> 5.\ 10^{18}\ cm^{-3}$, N or N^+ layer(s) thickness ranges of 0.1 to 10 micrometers N doping $> 1.\ 10^{17}\ cm^{-3}$. The Si substrate can be N doped, low N doped or undoped.

[00215] After growing the N/N^+ layer(s) on the Si substrate, microstructures of pillars and or holes and or nanowires are etched into the N/N^+ layer(s) 3604 and followed by a N/N^+ layer(s) regrowth resulting in buried voids 3622 as shown in Fig.

36. The regrowth surface may or may not need further planarization such as using chemical mechanical polishing (CMP). Some applications may have more optimal performance with a non-planar surface, for example PV that can couple sun light in multiple angles with minimal reflections (a rough surface reflect less light).

Subsequent "I" Si layer 3606 and P/P^+ layer 3608 are grown on the N/N^+ layer(s) 3604 with the buried voids 3622. In addition to reducing the effective refractive index, at wavelengths where Si has low loss (approximately ~1 dB/cm or less), 950-1800 nm, the buried voids 3622 can be patterned into a reversed HCG and behave as a very reflective (close to 100% reflectivity) broad spectrum mirror for any photons illuminating from the top (P side) and not absorbed in the "I" microstructured pillar/hole region on the first pass, the photons can be reflected back toward the absorbing "I" region. In addition, with the voids, the substrate may be more flexible and lightweight such that it can be more adaptable to contoured surfaces and/or for use where weight is an issue such as a solar panel, or for mobility.

[00216] FIG. 37 is a cross section showing etched Si microstructured pillars/holes with regrown Ge covering the Si, according to some embodiments. The starting structure is the same as layers 3500 in FIG. 35. The Si microstructure pillar and/or hole arrays are etched with a depth ranging from 0.1 to 10 micrometers and subsequently regrown with a I-Ge layer 3702 of thickness 0.01 to 4 micrometers including according to some embodiments a 1-10 nm low temperature buffer Ge layer to account for lattice mismatch between the Si and Ge. Note that the Ge buffer may not be included for pillar hole lateral dimensions of approximately 1000 nm or less since the lattice mismatch strain at that small area may not be significant to cause extensive defects to form. The lateral dimensions of the microstructured pillars 3704 and holes 3706 range from 10 to 5000 nm and spacing of adjacent elements from overlapping to 5000 nm. The P/P^+ Si layer 3708 is left on in FIG. 37 as it may be useful in making good P ohmic contact with the ohmic metals of Ti, W, Al silicide that are 1-50 nm thick to be semitransparent or transparent transition metal silicide.

[00217] FIG. 38 is a cross section showing microstructured Si pillars/holes with Ge regrowth on an N-Si layer having embedded microstructured voids, according to some embodiments. The structure shown in FIG. 38 is similar in starting

material as shown in FIG. 36. The buried voids 3822 in the N/N^+ layer 3804 act to reduce the effective refractive index of layer 3804. The voids spacing and lateral dimensions can be subwavelength ($< \lambda$) or even deep subwavelength ($<< \lambda$) to minimize optical scattering loss such as Rayleigh scattering which is proportional to λ^{-4} where λ is the wavelength. The wavelength of interest range from 300 to 1800 nm.

[00218] FIG. 39 is a cross section showing partial coverage I-Ge on microstructured Si pillars/holes, according to some embodiments. In the variation of the microstructure shown in FIG. 39, instead of regrowing I-Ge over the entire Si microstructured pillars and holes, it is only grown on part of the Si microstructures. Part of the Si microstructure is without I-Ge and the other part has regrown I-Ge. The partial regrowth of Ge can be accomplished by partially covering the Si microstructure with a dielectric such as SiOx or SiNx by directional deposition such as electron beam evaporation deposition, or directional laser ablation deposition or other directional methods such as ion milling to remove native oxide of Si selectively or ALD thin layer of oxides/nitrides and removing selectively and directionally with ion beam milling. Once the Si microstructure is partially coated with an oxide or nitride (or other dielectric such as CaFx, TaOx, TiOx, to name a few) Ge epitaxial regrowth will predominantly occur where there is lattice information such as a Si surface. The I-Ge regrowth 3902 thickness can range from 0.1 to 4 micrometers or more. The Si microstructure of pillars 3904 or holes 3906 can have a depth of 0.1 to 10 micrometers and a lateral dimension of 10 to 5000 nm and spacing between adjacent microstructures of overlapping to 5000 nm. Both Si and Ge microstructures are exposed to photons with wavelengths ranging from 300-1800 nm from photons impinging from the anode surface and impinging on the sidewalls of the microstructure directly, scattered, near field, resonance, HCG effect, linear and non-linear optical effects, and with enhanced absorption coefficient. Both Si and Ge will generate photocurrent due to the incident photons. The Si current generator and Ge current generator are in parallel and the total photocurrent generated by this PD/PV is the sum of the Si and Ge photocurrent generators. The buried voids 3922 reduce the refractive index of the N/N^+ layer 3914 and improve the index contrast of the microstructure and the substrate thus improving the performance of the lossy HCG for enhancing the absorption

coefficient. The voids 3922 in the Si 3914 can also behave as a good reflector to reflect photons back toward the "I" absorbing layer for a double pass (for photons illuminating from the top side). BOX or SOI 3912 can also be used in addition with the buried voids or without the buried voids, as the refractive index of SiO_2 is approximately 1.54, roughly half that of silicon at infrared and near infrared wavelengths.

[00219] FIG. 40 is a cross section showing the basic components for a microstructured Si-Ge pillar hole array PD/PV and/or APD, according to some embodiments. Note that the APD multiplication layers are not shown for simplicity. Only the very basic parts of the device is shown. After processing steps shown in FIG. 39 are completed, surface passivation is carried out using thermal oxide or ALD or PECVD or CVD deposition of oxide or nitride to passivate or SiGe as a passivation layer on Ge. A filler 4002 is spun on or deposited such as spin-on-glass, or SiOx, SiNx by PECVD or CVD. Using RIE to etch back to expose either the Ge or P/P^+ Si (during i-Ge epitaxial growth, the P dopant in the P/P^+ Si may diffuse into the Ge layer to also result in a P/P^+ Ge layer). Ge and or Si P- ohmic material may be Al, W, AuGe, Au, Au/Ti and Al, TiN, Pt, transition metal-silicide respectively; ohmic contacts to P and N semiconductors are well known in the literature and art and these are only a few examples of possible ohmic contacts. A transparent conducting oxide (TCO) 4004 such as indium tin oxide (ITO) may be used to further reduce the series resistance of the anode. For microstructured holes, since the P/P^+ layers are contiguous, TCO 4004 may not be used and only a perimeter (ring for circular apertured PD/APD/PV) border ohmic contact and metallization 4006 may be used instead to reduce series resistance of the ohmic contact, such as Al, Au/Ti. Cu, to name a few. Anti-reflection layers are not shown for simplicity. N ohmic material can be used on the substrate or on the N/N^+ layer together with metallization. Al, Pt, transition metal silicide, followed with Al or Au deposition (e-beam, sputter, thermal evaporation) on the ohmic contacts reduce series resistance. Ohmic contacts normally use an annealing process that is well known in the art. Bond and/or connecting metallization 4006 is deposited (using standard processing methods) to complete the PD/APD/PV device. Sunlight/optical signal is illuminated from the top (anode) of the device normal to the surface or at any angle off normal and may be rotated to optimize the QE. At wavelengths where

Si is low loss (950-1800 nm or more) the buried voids can both reduce the effective refractive index of Si and act as a reflector to reflect photons that are not absorbed back toward the absorbing region. The surface of the N/N^+ layer 3914 can be non-planar to help diffuse the reflected photons to optimize its absorption in the microstructured Si and Ge array. A contact pad 4008 can be provided, for example, on the side of layer 3914 as shown. Although many of the embodiments show the microstructures of Si and Ge, Si, Ge are normal to the surface (vertically aligned) and straight, according to some other embodiments if the N/N^+ surface is non-planar, subsequent layers may also be non-planar. Etching (wet chemical or dry RIE, DRIE) may result in microstructures that are off normal and not straight (with bends) which may further improve the absorption of photons. Due to the non-planar topology of the surface, the microstructures may have various orientations depending on the orientation of the crystal within the same device. The different orientations of the microstructures are advantageous to capturing photons that may be illuminating the surface of the device at different angles, for example for PV as the sun changes position in the sky and for PD/APD for applications where multiple optical signal may illuminate the PD/APD from different angles/directions.

[00220] Microstructured Si pillar and/or hole arrays/pattern/random PD shown in FIG. 5, *supra*, can also have buried voids in the N/N^+ layers as shown in FIG. 10 to both reduce the refractive index of Si so that the microstuctures of Si pillars/holes are more optimized as lossy HCG by increasing the refractive index contrast and also as a HCG reflector in Si for wavelengths where Si has low loss, 950-1100 nm for this application as a wide bandwidth (> 5 Gb/s) PD or as a PV.

[00221] The Si substrate in all the embodiments described herein can be either Si with doping, not intentionally doped, low doping, or buried oxide (BOX) or silicon on insulator (SOI) where the silicon layers again can be doped, heavily doped, lightly doped or not intentionally doped. The BOX and SOI layers allow the removal of the all or almost all of the Si substrate to reduce optical losses, increase mechanical flexibility and also the refractive index of SiO_2 in BOX and SOI have refractive index of approximately 1.54 in the infrared and near infrared wavelengths which is roughly half of silicon refractive index. The low index of SiO_2 also improves the performance of HCG, or the silicon dioxide layer can be removed for bottom illuminated PD/APD/PV.

[00222] FIGs. 41A-41B are cross sections showing aspects of a microstructured pillar/hole array device above a N-Si layer having buried microstructured voids, according to some embodiments. The bulk layers 4100 shown in FIG. 41A include I-Si layer 4112 and N-Si layer 4110. Microstructured voids 4102 are formed in the N-Si layer 4110 using techniques such as described herein *supra*. The structures in FIGs. 41A and 41B are a version of the PDs/PVs shown in FIGs. 25A-B but with buried voids 4102 in the N/N$^+$ layer 4110 to improve the refractive index contrast for lossy HCG (microstructures of Si and Ge) and to provide a reflector low loss HCG for photons. Pillars 4124 and/or holes 4122 arrays are formed in I-Si layer 4112. I-Ge is regrown in the etch region 4122 resulting in a buried/embedded Ge "I" layer with microstructure voids 4102 in the N Si layer 4110 to reduce the effective refractive index of Si and/or to reflect photons entering from the anode surface at wavelength where Si is low loss (950-1800 nm). Cap layer 4126 can be P-GE or P-Si regrowth. In the case of bottom illumination, an anti-reflection coating 4130 may be provided.

[00223] FIGs. 42A-42D are cross sections showing aspects of an APD with microstructured pillar/hole arrays above an N-Si layer having buried microstructured voids, according to some embodiments. The APDs shown in FIGs. 42A-42D are versions of the APD shown in FIGs. 24A and 24B, *supra*, except that buried voids 4202 are included in the N/N$^+$ layer 4210 to improve the refractive index contrast for lossy HCG (microstructures of Si and Ge) and to provide a reflector low loss HCG for photons. According to some embodiments, BOX/SOI Si wafers can also be used with or without buried voids to improve refractive index contrast for optimal HCG lossy operation. Only the basic structures are shown for simplicity. Electrical isolation, passivations, ohmic metallization, anneal, anti reflections, bond/interconnect metallization, guard rings, to name a few are not shown. FIG. 42A shows the bulk layers 4200, which include N-Si layer 4206, I-Si layers 4208 and 4212 and P-Si layer 4210. Microstructured voids 4202 are formed in the N-Si layer 4206 using techniques such as described herein *supra*. As in the case of FIG. 41B, I-Ge is regrowth in the etched area 4222. The voids 4202 are to reduce the effective index of the N-Si since the optical field will be an average effective refractive index composing of air and Si. If the voids 4202 are patterned for HCG effect, photons can be reflected that are not absorbed in the first pass

through the "I" absorbing region 4212 for photons illuminating the APD 4220 from the top or anode surface. The APD can also be illuminated from the bottom or cathode side.

[00224] FIGs. 42C and 42D show another variation of an APD 4230 in which voids 4204 are formed in the I-Si multiplication layer 4208 as well as in N^+ layer 4206 to reduce the effective refractive index and capacitance of those layers. Note that the elongated nature of the microstructured voids will have a minimal effect on charged carrier transport in the semiconductor materials. According to some embodiments, voids of various shapes and densities can be formed in the P anode, N cathode, P charge, and/or I multiplication layers of the APD in addition to the absorbing I layer. The addition of voids in the I multiplication layer 4208 and the I absorption layer 4212 can reduce the effective capacitance resulting in a short RC time constant for the device. The voids 4204 in the multiplication I Si layer 4208 also reduce the effective refractive index, which is helpful in enhancing the absorption coefficient in a HCG absorbing mode.

[00225] Epitaxial growth/regrowth/overgrowth/selective area growth/epitaxial lateral over growth of Si, Ge, SiGe, III-V such as InP, GaAs, GaN, InGaN, InGaAs, InGaAsP, InSb, heteroepitaxy, homoepitaxy, heterogeneous epitaxy to name a few, using chemical vapor deposition (CVD), metallic organic chemical vapor deposition (MOCVD), atomic layer deposition (ALD), molecular beam epitaxy (MBE), gas source molecular beam epitaxy (GSMBE) plasma enhanced chemical vapor deposition (PECVD), laser ablation deposition (LAD) to name a few, are well known in the art.

[00226] According to some embodiments, material other than Si and Ge on Si are used. For example, the techniques described herein can be applied to all combinations of Si, Ge, III-V and II-VI material families and substrates.

[00227] FIGs. 43-46 are top views illustrating various dimensions, spacings and shapes for microstructured elements, according to some embodiments. FIG. 43 shows a microstructured pillar and/or hole array 4300 (also applicable to embedded or buried voids) that is uniformly spaced with a fixed diameter ranging from 100-5000 nm and a spacing ranging from 100-10000 nm. The pillars and or holes can be formed in or using: Si, Ge, SiGe, or other materials such as III-V or II-VI material family. Examples includes: GaAs, InP, InGaAs, InGaAsN, InGaAsP,

InAs, GaN, InGaN, ZnTe, CdS, ZnSe, and HgTe. According to some embodiments, the microstructures can also be formed in or using absorbing polymers, glass, and/or ceramics.

[00228] FIG. 44 shows a microstructured pillar and/or hole array 4400 having a fixed diameter but with non-uniform spacing such as aperiodic or a mixture of periodic and aperiodic or random/pseudo random spacing or a mixture of random/pseudo random, periodic and aperiodic. According to some embodiments, the arrays can also be uniformly spaced periodic but with varying diameter. FIG. 45 shows a microstructured pillar and/or hole array 4500 having both variable diameters (ranging from 100 nm to 5000 nm) and variable spacing (ranging from 100 nm to 10000 nm). According to some embodiments, the variations can be random/pseudo random, or a pattern or a mixture of patterns or any combinations thereof. FIG. 46 shows a microstructured pillar and/or hole array 4600 having various shapes such as oval, circular, rectangle, doublets, triplets, and stars. In general, any shape that can be generated using a photolithographic mask, or e-beam direct write or that can be generated with a mold for imprint lithography, can be used. The pillar/hole arrays can also have a combination of different shapes and spacings, as well as variations in the depth of the microstructured holes or lengths of the microstructured pillars/mesas. The variations can be periodic, aperiodic, or random (or a mixture of periodic, aperiodic and random) within a single array.

[00229] According to some embodiments, for some applications an array dimension of Si or Ge or III-V microstructured pillars or holes of length 2 μm approximately (or depth of 2 μm approximately) with diameter of pillar/hole of 390 nm approximately and center to center spacing of 1060 nm approximately has been found to be suitable for enhancement of the absorption coefficient of greater than 50X.

[00230] According to some embodiments, the material can be Si, Ge, SiGe, Ge on Si, III-V, II-VI, III-V on Si, polymer, glass, ceramic and any combination thereof. Examples of III-VI and II-VI are InP, GaAs, AlGaAs, AlAs, AlInAs, InGaAs, InGaAsP, InAs, InGaAsN, InN, GaN, InSb, ZnSe, ZnTe, HgTe, and CdS. Also III-V, II-VI and group IV material such as Ge can be embedded in Si microstructures using SAG, VLS, ELOG growth methods in MOCVD, CVD, MBE, reactors.

[00231] FIGs. 47-48 are cross sections showing microstructured pillar and hole arrays having varying lengths and depths, according to some embodiments. FIG. 47 shows a microstructured pillar array 4700 having different lengths, diameters and spacing. According to some embodiments, the pillar diameters range from 10 nm to 5000 nm and the pillar heights range from 0.1 to 10 microns. FIG. 48 shows a microstructured hole array 4800 having different depths, diameters and spacings. According to some embodiments, the holes have diameters ranging from 10 nm to 5000 nm and depths ranging from 0.1 to 10 microns. The variation in lengths and etched depths can be accomplished by additional lithographic masking steps where regions are masked for longer etch or shorter etch to vary the length of the pillars and the depth of the holes. The lengths and depths can be gradually or sharply varied. A patterned grating effect can be used to further optimize the optical path lengths and increase the enhancement factor for absorption coefficient. Other uses include forming a light trap by using constructive and destructive optical interference, generating a fresnel lens, matching the mode of the optical signal, forming a filter in wavelength selectivity in wavelength division multiplexing for example, or as a wavelength selector for spectroscopy and sensor applications. It should be noted that by varying the dimensions and spacing of the microstructured pillars and holes in an array can also result in constructive and destructive optical interferences that can also increase the enhancement factor of the absorption coefficient, improve light trapping, create fresnel lens, mode matching of radiation patterns of the optical signal.

[00232] FIG. 49 shows shows a microstructured surface having a combination of both pillars and holes, according to some embodiments. Microstructure array 4900 includes pillars and holes co-existing on the same microstructured surface either globally or locally. Both pillars and holes can exist in a single array (such as shown in FIG. 49) for the microstructured photodetector, or holes and pillars can exist on separate arrays for different microstructured photodetectors. In addition, hole(s) can exist in a pillar and pillar(s) can exist within a hole and these also can be global or local. The pillars, holes, hole(s) in pillar and pillar(s) in holes can have any shape, for example a rectangular pillar within a round hole, can have any mixture thereof to optimize enhancement of the absorption coefficient, light trapping, constructive and destructive optical interference, scattering, near field effects,

linear and non-linear optical effects, subwavelengths effects, fresnel lens, wavelength selection, optical mode matching, diffraction, high contrast grating, blazed grating, high Q resonator, highly reflective mirrors using high contrast grating.

[00233] The microstructured pillar and hole (and variations thereof) arrays can be fabricated in Si, Ge, Ge on Si, SiGe on Si, SiGe on Ge. The array structure can be any combination of Si, Ge and SiGe. The array can be entirely Si or Ge or SiGe, or Ge on Si, or Si on Ge, or Ge on Si with SiGe on both. The structure can also include III-V and II-VI material systems together with Si, Ge and SiGe and any combination of Si, Ge, and III-V, II-VI material systems. According to some embodiments, the array structure can also include polymer, glass, oxides, nitrides, sulfides and chlorides of transition metals, ceramics, quartz, SOI, IOS, organic conducting and non conducting polymers, carbon based material such as graphene to name a few.

[00234] The microstructures pillars, holes, voids, and any other shapes such as pyramids, microwires, nanowires, multiple materials, SAG microstructures, can have orientations that are not perpendicular to the surface of the substrate. They can have a single or multiple orientations that can be perpendicular and or off perpendicular to the surface. They can be random or pseudo random, single pattern or multiple pattern orientations at any angle where angle can range from 0 to 90 degrees with respect to the normal to the silicon substrate, and they can be on sidewalls and on all three dimensions. With the microstructures at certain orientations, the photosensor can have a higher sensitivity to certain direction of illumination. Conversely, with multiple orientations and or random or pseudo random orientations the photosensor can be mostly insensitive to direction of illumination.

[00235] Reducing the effective refractive index with buried voids in semiconductor has applications beyond PD/APD and PV devices. It also, for example, has applications in optical waveguides. FIG. 50 is a cross section of an optical ridge waveguide, according to some embodiments. Waveguide 5000 uses the density of voids to alter the effective refractive index of Si. According to some embodiments materials other than Si are used, for example other semiconductors such as Ge, SiGe, any of the III-V semiconductor family, or other material such as

ceramics, glass, polymer. In Si photonic optical waveguide 5000, the ridge 5002 and slab 5004 are made of Si on a BOX (buried oxide) Si substrate 5006. Due to the high refractive index of Si. 3.49 at 1100-1800 nm wavelengths, the dimensional tolerance of the solid Si waveguide is very critical. Known Si photonic components are difficult to manufacture and have low yield and are temperature sensitive. According to some embodiments, voids are buried in the Si layers. By varying the density of the voids, the refractive index of the composite Si-voids can be adjusted. In the schematic diagram of FIG. 50, a ridge waveguide 5000 has voids 5014 on slab 5004, as well as voids 5012 on ridge 5002. The density of voids 5012 in the ridge 5002 is less than the density of voids 5014 in the slab 5004. The refractive index in the ridge 5002 is therefore higher than the refractive index in the slab 5004 resulting in a ridge optical waveguide. The optical mode of the waveguide 5000 is indicated by the dotted oval 5022. The lower refractive index helps in reducing the dimensional tolerance and the optical waveguide can have a larger dimension. Thus, according to some embodiments, the refractive index can be varied by varying the void density making other components such as couplers easier to manufacture. The dimensions of the voids can be subwavelength ranging from 10nm to 1000nm depending on optical wavelengths.

[00236] According to some embodiments, voids are also buried in a silicon wafer (including BOX/SOI silicon wafers) to adjust the effective refractive index of the Si wafer. The Si wafer with buried voids can then be the starting platform for silicon photonic circuits. It can also be the platform for large area PV cells that allow mechanical flexibility but still retain the high quality of silicon and its electrical characteristics. This can also be the platform for flexible displays and other electronics that require mechanical flexibility and or light weight. According to some embodiments, burying or embedding voids is not limited to just Si, but can include Ge, GeSi, amorphous semiconductors, III-V, II-VI material families, polymers, glass, quartz, metal, alloys, ceramics and any other material that requires flexibility. In some embodiments, the voids can be filled with gas, liquid or solid for specific applications. Gel such as spin on glass that does not require anneal for example can be used for impact/crack situations where the integrity of the device is compromised such as a crack due to impact, to seal surfaces such as semiconductors or any surfaces sensitive to environment such as moisture, water,

oxygen to name a few to prevent further deterioration. Voids are also excellent in preventing crack propagation.

[00237] FIG. 51 is a cross section of a buried optical waveguide in silicon using voids, according to some embodiments. A composite waveguide 5100 is formed in Si substrate 5106 using Si-voids to selectively alter the effective refractive index in certain locations. The effective refractive index of Si can be adjusted precisely by adjusting the total volume of the voids in a given volume of Si. In the example shown in FIG. 51, the higher density voids 5114 surround a central region of lower density voids 5112. The optical mode of the waveguide 5100 is indicated by the dotted oval 5122.

[00238] According to some embodiments, the dimension and spacing of the voids are optimized to reduce scattering losses and to provide ease of manufacturing. Also, the void dimensions and spacing can be adjusted for certain applications. For example, in HCG the dimensions and spacings are selected to satisfy the near field regime where the dimensions and spacing lie approximately between the wavelength in the high refractive index material and the wavelength in the low refractive index material. In most cases, in the applications to reduce the effective refractive index, the void and the surrounding material dimensions and spacing are in the subwavelength regime where the microstructures containing the voids are less or much less than the wavelength in either the high or low index material. For coupling applications, the diffraction regime may be the microstructure (voids and material) dimensions and spacing. It can also be a mixture of two or more regimes to optimize a device performance.

[00239] Array patterns can include microstructure ensembles whose distribution of individual microstructures can be periodic, aperiodic, chirped, random, pseudo-random, uniform, or non-uniform in all three dimensions, orientations and spacings, (including overlapping). According to some embodiments, the patterns can include microstructures within microstructures. The terms "array" and "pattern" are used herein interchangeably.

[00240] The PD/APD are biased between the anode and cathode, to extract a broadband modulation signal greater than a gigabit per second (Gb/s) at a typical transmission line impedance is 25-50 ohms. According to some embodiments, the external bias is provided with a bias-tee connected to the transmission line to block

the RF signal from reaching the DC power supply and to block the DC from biasing the transmission line away from the PD/APD. The bias-tee basically consists of an inductor and capacitor, the inductor to block the RF and the capacitor to block the DC away from the PD/APD. External bias of -2 to -30 volts is applied depending on the application, PD or APD and performance desired.

[00241] In PV mode, no external bias is applied and the PV is basically a current generator. All the electrical connections are for DC current from the PV which then connects to a converter that converts the DC current/voltage to AC current/voltage.

[00242] PV devices are in DC mode whereas PD/APD for data and tele communication are all RF with modulation bandwidth ranging from 1 to 100 Gb/s. Transit time of carriers and capacitance are critical in PD and APD but not so much for PV.

[00243] The terms "modulation bandwidth" and "bandwidth" are interchangeable as used herein. Both terms refer to the modulation (e.g. of a laser or LED) where an RF signal is impressed on the light. When this modulated light (also referred to as "optical signal") illuminates the PD/APD, the RF modulated signal is extracted and converted from light to electrical signal. For example, a bandwidth or modulation bandwidth of a PD/APD of 20 Gb/s means that an RF signal impressed on the laser light beam at a data rate at 20 Gb/s can be converted by the PD/APD from optical to electrical with good signal integrity or signal replication. The laser/LED is the transmitter and the PD/APD is the receiver where the electrical signal can be further processed by an amplifier such as a transimpedance amplifier and the signal sent for further analysis and processing in application specific integrated circuits (ASIC) computers (CPU central processing unit), routers, memories, to name a few.

[00244] According to some embodiments the applications for the microstructured pillars and or holes in Si and Ge and Si regrowth with Ge, Ge on Si, with and or without buried or embedded voids photodiodes and avalanche photodiodes, are in data and tele communications. According to some embodiments, these applications include: fiber to home, local area network, data center optical interconnects board to board, on the board, rack to rack, and chip to chip, between data centers, metro area network, and optical communication for distances from less than a centimeter to over 10 kilometers or more. The

applications in consumer space also includes: game box, personal computers, tablets, mobile devices such as smart phones, animations studios, and anywhere that benefits from a bandwidth of more than one gigabit per second. Other applications of the microstructured PDs and APDs, according to some embodiments, are in sensors where broadband communication is important, such as sensors for infrastructures, health, environment, oil exploration, where the sensors communicate with a remote receiver that is connected to data centers for data analysis.

[00245] Other applications of the microstructured PD and APD, according to some embodiments, are in analytical instruments and optical tests and measurement instruments where high sensitivity and bandwidth are important.

[00246] According to some embodiments, the microstructured PV have applications in energy harvesting for power generation all the way from gigawatts to watts, to power cities and homes to powering sensors. Since the microstructured PV is lightweight and high efficiency it can be used in mobile applications, space, solar transportation, recycling of photons in home, offices and factories. The PV can also be used on windows and can be semi-transparent.

[00247] The described microstructures in Si, Ge, Si regrowth with Ge, Ge on Si, pillars, holes, and voids can be any shape and form, and are not limited to the schematics shown. According to some embodiments, the dimensions range from 10-10000 nm (nanometers). The microstructures can be within each other such as pillar(s) in hole(s), hole(s) in pillar(s) and void(s) can be in the pillar, and buried and or embedded in any layer of the semiconductor heterogeneous or homogeneous. The material used includes semiconductors such as Si, Ge, GeSi, Ge on Si, and the III-V group material family of InP, GaN, InGaAsP, GaAs, and other semiconductors such as ZnO, CdTe, CuInGaSe (CIGS), amorphous Si, or any amorphous semiconductor and or microcrystalline and crystalline semiconductor. The material can be a combination of amorphous, microcrystalline, crystalline heterogeneous and or homogeneous. The material used is also not limited to semiconductors, but also include polymers, electrically conducting, semiconducting, non conducting polymers, organic and or inorganic polymers, glass, conducting, semiconducting, non conducting glass. Nanoparticles of semiconductors and or metal can also be buried in the polymer and glass.

Semiconductors, polymer and glass can exist within the same microstructure, separately or in any combination.

[00248] According to some embodiments, in silicon photonic circuit applications, optical waveguides such as shown in FIG. 50, *supra*, can be integrated with optical sources and optical detectors such as photodiodes, avalanche photodiodes and photoconductors. FIG. 52 is a cross section of a ridge waveguide integrated with a microstructured PD/APD, according to some embodiments. Device 5200 includes a ridge waveguide that is edge coupled to a microstructered Ge on Si photodiode or avalanche photodiode (with multiplication layers added). In the ridge wave guide portion, as shown in FIG. 50, a ridge 5202 has lower density voids 5212 and slab 5204 had higher density voids 5214. Ion implantation is used to increase the N doping (region 5224) for the PD and a coplanar transmission line is fabricated on the photodiode to extract the electrical signal as shown in FIG. 53, *infra*. Anode contact 5226 is made of P-Ge, according to some embodiments. The cathode contact is made to layer 5224 (cathode contact not shown for simplicity and clarity of drawing.)

[00249] FIG. 53 is a top view the integrated ridge waveguide and microstructured PD/APD shown in FIG. 52, according to some embodiments. The device 5200 is in a coplanar transmission line configuration. Ridge portion 5202 is 0.5 to 10 μm wide and 0.1 to 10 μm deep, according to some embodiments. Slab portion 5204 has higher density voids, as shown in FIG. 52, to vary the refractive index as a platform for silicon photonic circuits. Coplaner cathodes 5228 and 5230 are in contact with the N-Si ion implanted region 5224 shown in FIG. 52. According to some embodiments, the optical field can also be coupled evanescently by placing the PD/APD above the optical waveguide such that the optical field overlaps the absorbing I microstructures.

[00250] FIGs. 54A and 54B show a microwave transmission line on Si with voids, according to some embodiments. High bit rate transmission lines on silicon suffers from a multitude of effects, from slow wave to dispersion to loss. However by removing most of the silicon material with the addition of high-density voids according to some embodiments, the dispersion and loss can be alleviated and signal integrity restored. An advantage is that silicon can be the substrate for both microwave transmission line and for ICs without the use of intermediate ceramic

such as alumina for transmission line to connect various IC chips. FIG. 54A is a cross section showing high density voids 5314 buried in silicon 5304 which reduce the effective dielectric constant of the silicon, and disrupt lateral electrical conductivity which in turn can result in lower microwave loss and dispersion which are important as bit rate increases into the multi Gb/s range (e.g. 40-60 Gb/s). Coplanar microwave metallic transmission lines 5310 are provided as means to move the electrical signal to/from electronic devices (e.g. processors, storage devices, input-output devices, ASICs, CPUs, and memories) on the same substrate. FIG. 54B is a top view. Conventional techniques use multi chip carriers that need additional packaging. According to some embodiments, having many devices all on the same silicon substrate greatly reduces the cost since it can be all fabricated at once and requires no additional packaging for each chip. According to some embodiments, the voids 5314 are arranged in a fashion where the path length in silicon laterally is significantly increased in order to increase lateral resistivity. According to some embodiments, Ion implantation of protons and or oxygen can be used to further increase electrical resistivity. Although FIGs. 54A and 54B show a co-planar arrangement, according to some embodiments other microwave transmission line arrangements (e.g. microstrip, slotline, and stripline) are used with a semiconductor substrate having high-density buried voids. According to some embodiments, the positioning and/or other properties (e.g. size, shape, and filling material) of the high-density voids can be selected such that the slow wave effect can be manipulated or "tuned" in a way that is suitable for the application at hand.

[00251] FIG. 55 is a cross section of voids for thermal conduction and thermal isolation of heat producing ICs and light emitters, according to some embodiments. The buried voids in silicon 5404 can be filled with thermal conductors such as helium gas, metal such as copper, aluminum, tungsten, or ceramic such as boron nitride, or carbon, graphene, diamond like carbon, or heterogeneous material/ceramic doped with metal nanoparticles, carbon nanotubes. The voids 5414 underneath the heat producing elements such as ICs and CPUs 5422, and light emitters 5420 such as laser diodes and bipolar drivers, can be filled with enhanced thermal conductors to extract the heat from the hot components and direct it to a heat sink 5402. Voids 5412 between hot elements are kept at a low

thermal conducting state that are either in partial vacuum or filled with a gas such as nitrogen, argon, carbon dioxide, for example to prevent thermal cross talk between the hot components or to any other components where heat is not desirable. According to some embodiments, the voids are arranged in a fashion such that the path length in silicon is vastly increased to maintain low thermal crosstalk. According to some embodiments, the techniques of FIG. 55 are used to keep PVs cool when exposed to the sun. According to some embodiments, thermoelectric devices can be integrated together with the voids to generate electricity from the excess heat.

[00252] FIG. 56 is a cross section showing a distribution of voids to increase lateral path length for increasing lateral electrical resistivity and decrease lateral thermal conduction, according to some embodiments. The buried voids 5602 configured for microwave transmission lines and/or for thermal management can be arranged in a randomly, pseudo randomly, or in a pattern in areas where lateral electrical and thermal conductance is significantly reduced and vertical electrical and thermal conductance is significantly enhanced. There may be areas where lateral electrical and thermal conductance enhancement is desired, in which case the voids can overlap to form a conducting channel.

[00253] This patent application refers to certain theories in explaining the nature and operation of devices, but it should be clear that such theories are based on current understanding and do not affect the actual operation of the disclosed devices even if future developments prove the theories incorrect. This patent specification also refers to numerical ranges of paramaters, and it should be understood that insubstantial departures from such ranges are still within the spirit of the disclosed advancements.

[00254] Although the foregoing has been described in some detail for purposes of clarity, it will be apparent that certain changes and modifications may be made without departing from the principles thereof. It should be noted that there are many alternative ways of implementing both the processes and apparatuses described herein. Accordingly, the present embodiments are to be considered as illustrative and not restrictive, and the body of work described herein is not to be limited to the details given herein, which may be modified within the scope and equivalents of the appended claims.

CLAIMS

What it claimed is:

1. A photodetector with microstructure-enhanced photoabsorption comprising:
a cathode region;
an anode region;
reverse biasing circuitry configured to apply a voltage between said cathode and anode regions such that said cathode region is driven to a more positive voltage than said anode region; and
a microstructure-enhanced photon absorbing semiconductor region operatively associated with the cathode and anode regions and configured to absorb photons from a source signal, said absorbing region including a plurality of microstructures configured to increase absorption of photons at a range of wavelengths that includes a wavelength of said source signal relative to an absorbing region that is not intentionally microstructure-enhanced.

2. A photodetector according to claim 1 wherein said microstructures are configured to increase absorption of photons at the range of wavelengths by being dimensioned and positioned to facilitate said increase of absorption.

3. A photodetector according to claim 2 wherein said microstructures have at least one dimension that is equal to or shorter than a longest wavelength in the range of wavelengths.

4. A photodetector according to claim 1 wherein said microstructures have one or more shapes selected from a group consisting of pillars, holes and voids.

5. A photodetector according to claim 1 wherein said microstructures are arranged into a periodically-spaced array.

6. A photodetector according to claim 1 wherein said microstructures are arranged into a non-periodically-spaced, randomly-spaced or multiperiodically-spaced array.

7. A photodetector according to claim 1 further including a substrate material and wherein said microstructures have a major longitudinal axis normal to an upper surface of the substrate material.

8. A photodetector according to claim 1 wherein said microstructures have major longitudinal axes that are not parallel to one another.

9. A photodetector according to claim 1 wherein said microstructures are oriented to reduce cross-talk in an application selected from a group consisting of: free space applications and coupling to multiple sources in an array, compared to an otherwise same photodetector.

10. A photodetector according to claim 1 wherein said microstructures are oriented to reduce sensitivity to any single direction of said source signal compared to an otherwise same photodetector.

11. A photodetector according to claim 1 wherein the microstructures increase absorption compared to an otherwise same photodetector at least in part by forming an absorbing mode high contrast grating.

12. A photodetector according to claim 11 wherein the microstructures increase absorption compared to an otherwise same photodetector at least in part due to one or more of the following effects: resonance effects, scattering effects, near field effects, sub-wavelength effects, and interference effects.

13. A photodetector according to claim 11 wherein said high contrast grating is in 2-dimensions or 3-dimensions.

14. A photodetector according to claim 11 wherein said high contrast grating is of one or more types selected from a group consisting of: periodic, aperodic, chirped, random, pseudo random.

15. A photodetector according to claim 11 wherein contrast for said high contrast grating is increased using a plurality of voids in one or more materials compared to an otherwise same photodetector.

16. A photodetector according to claim 1 wherein said microstructure-enhanced photon absorbing semiconductor region and said microstructures are formed of silicon.

17. A photodetector according to claim 16 wherein said photodetector is a silicon photodiode.

18. A photodetector according to claim 17 wherein said photodetector is configured to detect said source signal at a data bandwidth of greater than 5 gigabits per second, at source signal wavelengths of 850 nanometers with a quantum efficiency of at least 60%.

19. A photodetector according to claim 18 wherein said photodetector is configured to detect said source signal at a data bandwidth of greater than 10 gigabits per second, at source signal wavelengths of 850 nanometers with a quantum efficiency of at least 60%.

20. A photodetector according to claim 17 wherein said photodetector is configured for quantum efficiency of greater than 60%.

21. A photodetector according to claim 16 wherein said photodetector is an avalanche photodiode.

22. A photodetector according to claim 21 wherein said avalanche photodiode is configured to detect said source signal at a data bandwidth of greater than 5 gigabits per second, at source signal wavelengths of 850 nanometers, and having a gain of greater than 2.

23. A photodetector according to claim 21 further comprising a multiplication region that includes a second plurality of microstructures.

24. A photodetector according to claim 23 wherein said second plurality of microstructures extends into one or more multiplication layers selected from a group consisting of: P multiplication layer, N multiplication layer and charge layer.

25. A photodetector according to claim 16 wherein said photodetector is configured to detect said source signal at a data bandwidth of greater than 1 gigabit per second, at source signal wavelengths of 980 nanometers with a quantum efficiency of at least 40%.

26. A photodetector according to claim 16 wherein said photodetector is configured to detect said source signal at a data bandwidth of greater than 0.5 gigabits per second, at source signal wavelengths of 1000 nanometers with a quantum efficiency of at least 30%.

27. A photodetector according to claim 1 wherein said plurality of microstructures effectively reduces capacitance of the photodetector when compared to a microstructure-free device having a similar photon absorbing length.

28. A photodetector according to claim 1 wherein said microstructure-enhanced photon absorbing semiconductor region and said microstructures are formed of silicon and germanium.

29. A photodetector according to claim 28 wherein said microstructures are formed by etching away portions of silicon and using a selective area growth process to grow germanium in the etched away portions.

30. A photodetector according to claim 1 wherein said microstructure-enhanced photon absorbing semiconductor region and said microstructures are formed of germanium.

31. A photodetector according to claim 30 further including a substrate and wherein said cathode, absorbing and anode regions are formed above the substrate and said photodetector is configured to receive said source signal from a substrate-side of the photodetector.

32. A photodetector according to claim 31 wherein said anode region comprises a germanium P layer formed by an epitaxial lateral overgrowth process.

33. A photodetector according to claim 31 wherein the photodetector is configured for a portion of the source signal to pass through the absorbing region a first time, reflect from a surface and thereafter pass through the absorbing region a second time.

34. A photodetector according to claim 30 further including a substrate and wherein said cathode, absorbing and anode regions are formed above the substrate and said photodetector is configured to receive said source signal from directions facing a side of the photodetector opposite of said substrate.

35. A photodetector according to claim 34 wherein said anode region comprises a silicon P layer.

36. A photodetector according to claim 30 wherein said photodector is an avalanche photodiode and further comprises a multiplication region formed of silicon.

37. A photodetector according to claim 36 wherein said anode region comprises a germanium P layer formed by an epitaxial lateral overgrowth process.

38. A photodetector according to claim 36 wherein said avalanche photodiode is configured to detect said source signal at a data bandwidth of greater than 1 gigabit per second, at source signal wavelengths of 1750 nanometers or shorter, and having a gain of greater than 2.

39. A photodetector according to claim 36 wherein at least one germanium layer is grown epitaxialllly on a silicon layer.

40. A photodetector according to claim 1 wherein said microstructure-enhanced photon absorbing semiconductor region and said microstructures are at least partially formed of a III-V family material.

41. A photodetector according to claim 40 wherein said III-V family material is selected from a group consisting of: InP, GaAs, InGaAs, GaN, InGaN, InGaAsP, AlGaAs, AlGaN, GaP, InSb and InAs.

42. A photodetector according to claim 40 wherein said III-V family material is formed using a selective area growth process.

43. A photodetector according to claim 40 wherein said photodector is an avalanche photodiode and further comprises a multiplication region formed of silicon.

44. A photodetector according to claim 1 wherein said plurality of microstructures include voids buried within the absorbing semiconductor region.

45. A photodetector according to claim 44 wherein the absorbing semiconductor region is made of a material selected from a group consisting of silicon and germanium.

46. A photodetector according to claim 1 further comprising a plurality of voids buried in a layer of material effectively lowering a refractive index at said

range of wavelengths and lowering capacitance of said layer of material compared to the material when free of intentional voids.

47. A photodetector according to claim 46 wherein said layer of material is an N layer formed on a substrate material.

48. A photodetector according to claim 46 wherein said photodetector is an avalanche photodiode and said layer of material forms a multiplication layer of the avalanche photo diode.

49. A photodetector according to claim 46 wherein said plurality of voids are filed with a material selected from a group consisting: nitrogen, argon, polymer, amorphous semiconductor material, and glass.

50. A photovoltaic device comprising a semiconductor material having a plurality of voids buried therein, the semiconductor material configured to convert solar radiation into direct current electricity.

51. A device according to claim 50 wherein said plurality of voids are microstructured voids configured to enhance absorption of said semiconductor material to thereby increase conversion efficiency of the device compared with the material when free of intentional microstructured voids.

52. A device according to claim 50 wherein said plurality of voids are sized and/or spaced apart by less than 3 microns, and are configured to alter an effective refractive index of the semiconductor material near a surface of the semiconductor material to reduce reflection of incident sunlight from the device compared with an otherwise same device.

53. A device according to claim 50 wherein said plurality of microstructured voids are sized and/or spaced apart by less than 3 microns, and are configured to alter an effective refractive index of the semiconductor material

near a surface of the semiconductor material to increase internal reflection within the semiconductor material compared to an otherwise same device.

54. A glass material comprising a glass having a plurality of buried voids dimensioned between 0.01 microns to 1000 microns.

55. A glass material according to claim 54 wherein the material forms a part of a photovoltaic device.

56. A glass material according to claim 54 wherein said buried voids are filled with a material selected from a group consisting of: gel, polymer and gas.

57. A device according to claim 54 wherein said plurality of buried voids are configured to provide flexibility of the glass material.

58. A device according to claim 54 wherein said plurality of buried voids are configured to provide increased resistance of the glass material to physical damage and/or damage propagation compared to an otherwise same device.

59. A microwave transmission line structure comprising:
a semiconductor substrate material including a plurality of high-density dielectric-filled voids configured to reduce a dielectric constant of the semiconductor substrate material; and
a plurality of metallic microwave transmission lines, at least one of which is positioned above said semiconductor substrate material and is operatively associated therewith.

60. A structure according to claim 59 wherein said dielectric-filled voids are filled with one or more dielectric materials selected from a group consisting of: nitrogen, argon, vacuum, air, helium, polymer, metal oxides, silicon dioxide, silicon nitride, calcium fluoride, and zinc oxide.

61. A structure according to claim 59 wherein said voids are further configured to reduce dispersion and reduce loss associated with said microwave transmission lines at least in part by reducing current loop flow and/or eddy currents compared to an otherwise same structure.

62. A structure according to claim 59 wherein said plurality of metallic microwave transmission lines are arranged in a manner selected from a group consisting of: coplanar, microstrip, slotline, and stripline.

63. An optical waveguide structure comprising:
an optical mode region; and
a supporting semiconductor material adjacent to said optical mode region, wherein said supporting material includes a plurality of microstructured voids formed therein that are configured to alter an effective index of refraction of said supporting material.

64. An optical waveguide structure according to claim 63 wherein said effective index of refraction depends on a density of the plurality of microstructured voids.

65. An optical waveguide structure according to claim 63 wherein said optical mode region is formed into a ridge supported by said supporting semiconductor material.

66. An optical waveguide structure according to claim 63 wherein said optical mode region is surrounded by said supporting semiconductor material.

67. An optical waveguide structure according to claim 63 wherein said optical mode region includes a second plurality of microstructured voids formed therein that are configured to alter an effective index of refraction of said optical mode region.

68. A heat exchanger system comprising:

a heat generating device;
a heat sink configured to dissipate heat to a surrounding medium; and
an intermediate material mounted between said heat generating device and said heat sink, the intermediate material including a plurality of buried voids configured to alter thermal conductivity of said intermediate material.

69. A heat exchanger according to claim 68 wherein a first portion of said buried voids are filled with thermally conductive material and a second portion of said buried voids are filled with a thermally isolating material, the first and second portions being positioned to conduct heat from said heat generating device to said heat sink and to reduce thermal cross talk with other heat sensitive devices mounted on said intermediate material.

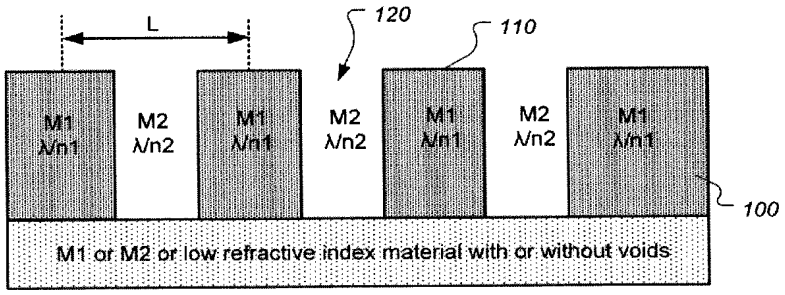


FIG. 1

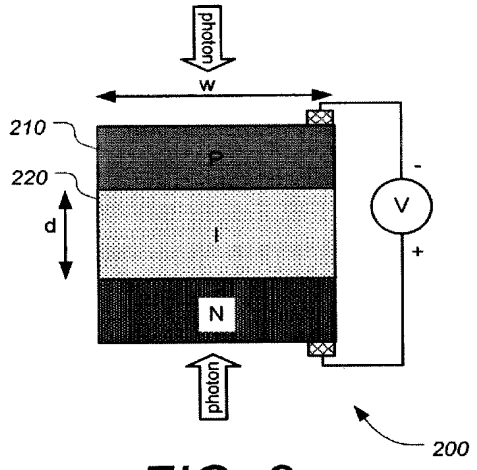


FIG. 2
(prior art)

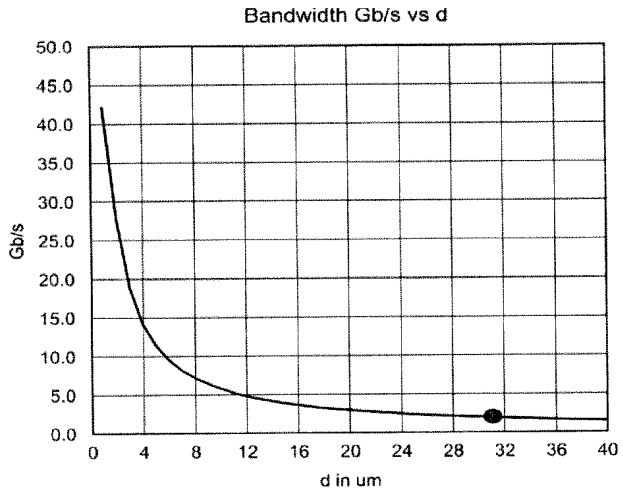


FIG. 3A
(prior art)

310

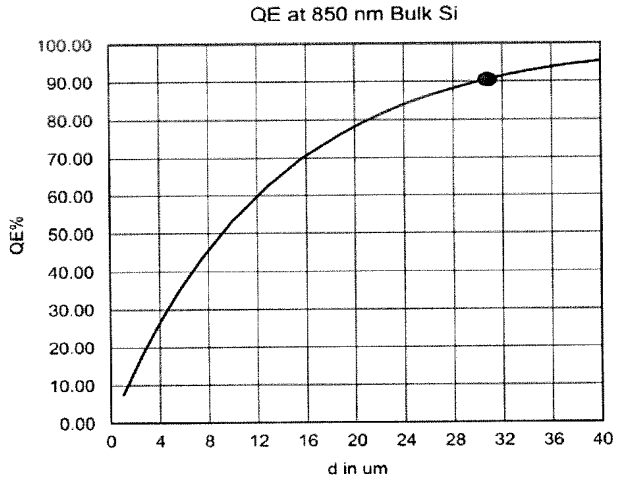


FIG. 3B
(prior art)

312

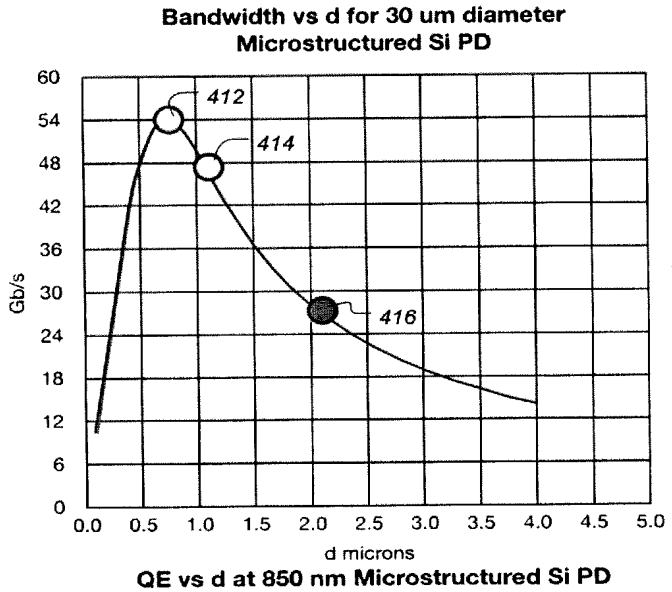


FIG. 4A

410

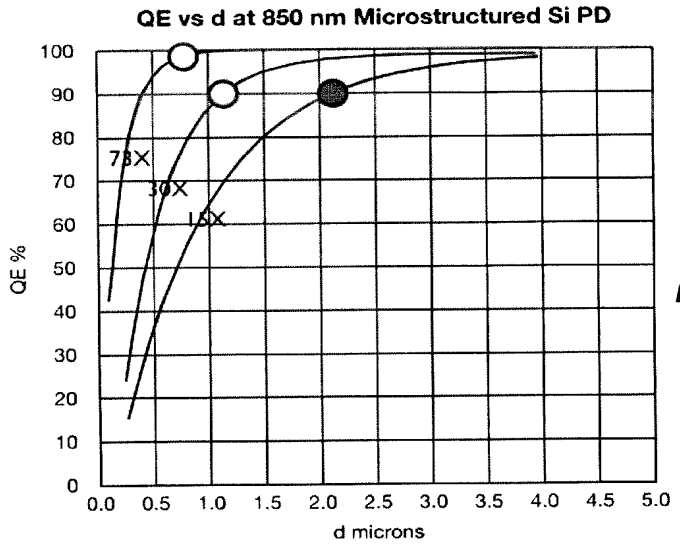


FIG. 4B

420

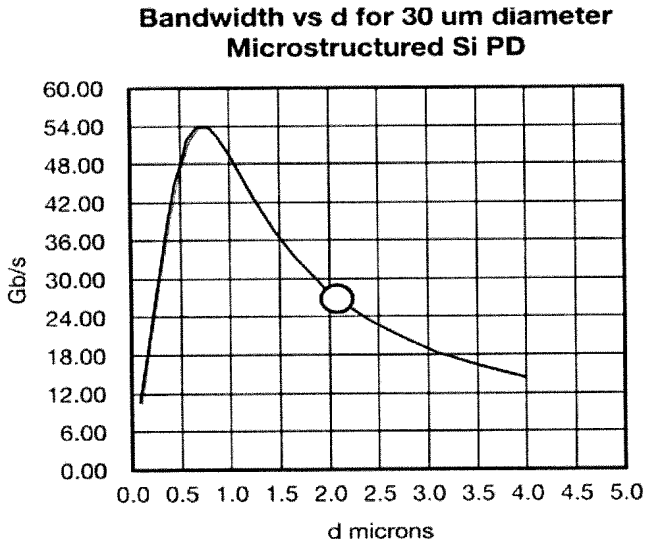


FIG. 4C

430

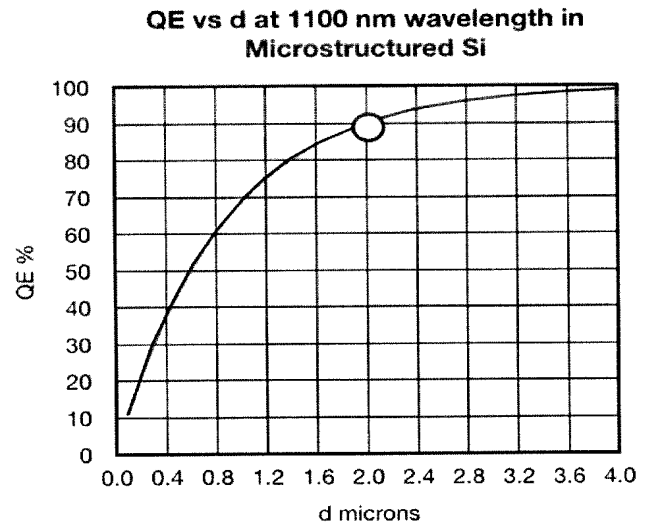


FIG. 4D

440

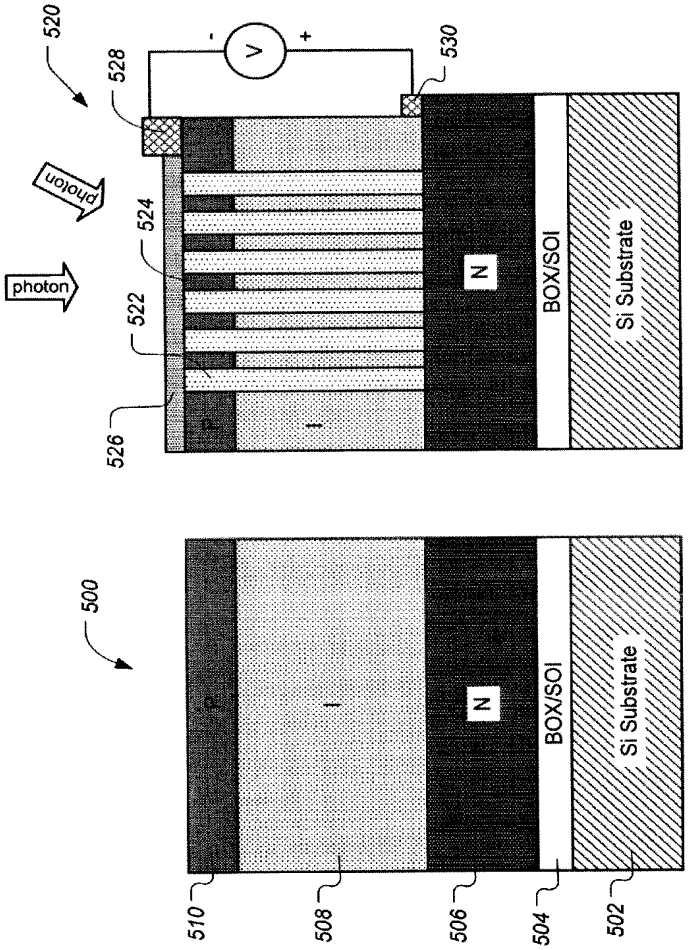

520
528
530
V
-
+
photon
photon
524
522
526
P
I
N
BOX/SOI
Si Substrate

FIG. 5B

500
P
I
N
BOX/SOI
Si Substrate
510
508
506
504
502

FIG. 5A

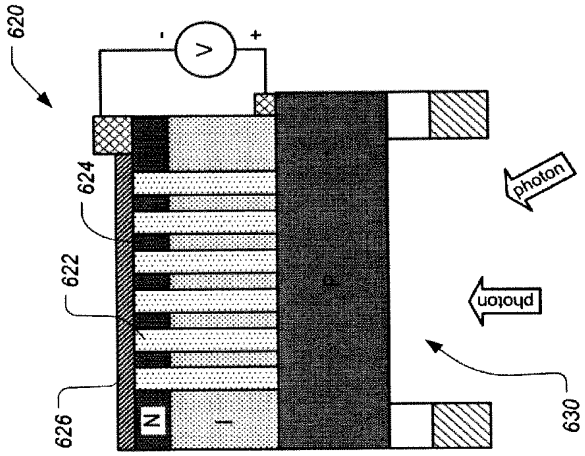

620
-
V
+
624
622
626
N
I
P
photon
photon
630

FIG. 6B

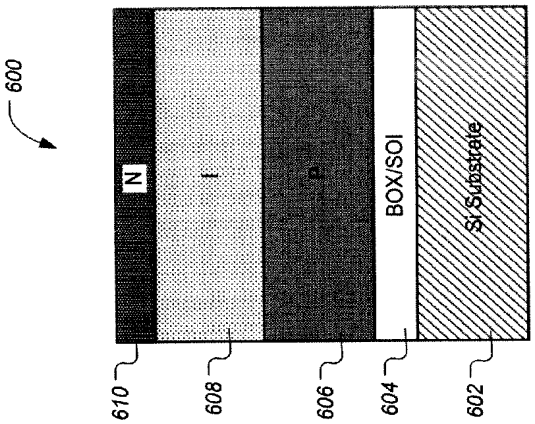

600
N
I
P
BOX/SOI
Si Substrate
610
608
606
604
602

FIG. 6A

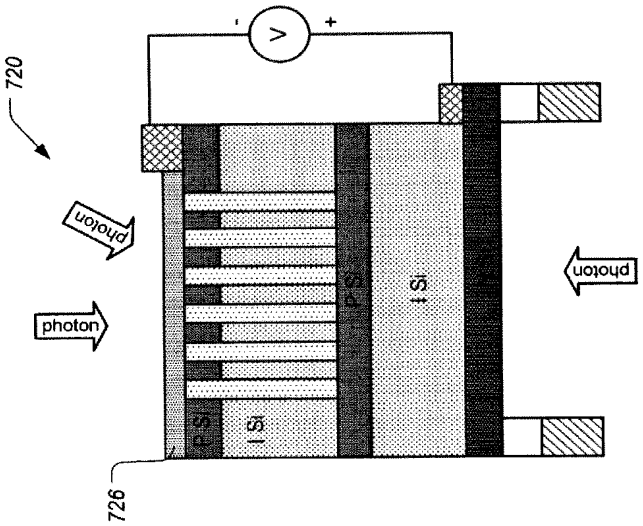

720
-
+
photon
photon
photon
p Si
i Si
n Si
726

FIG. 7B

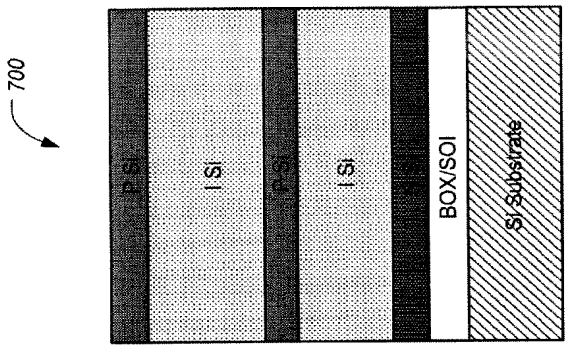

700
p Si
i Si
n Si
i Si
BOX/SOI
Si Substrate

FIG. 7A

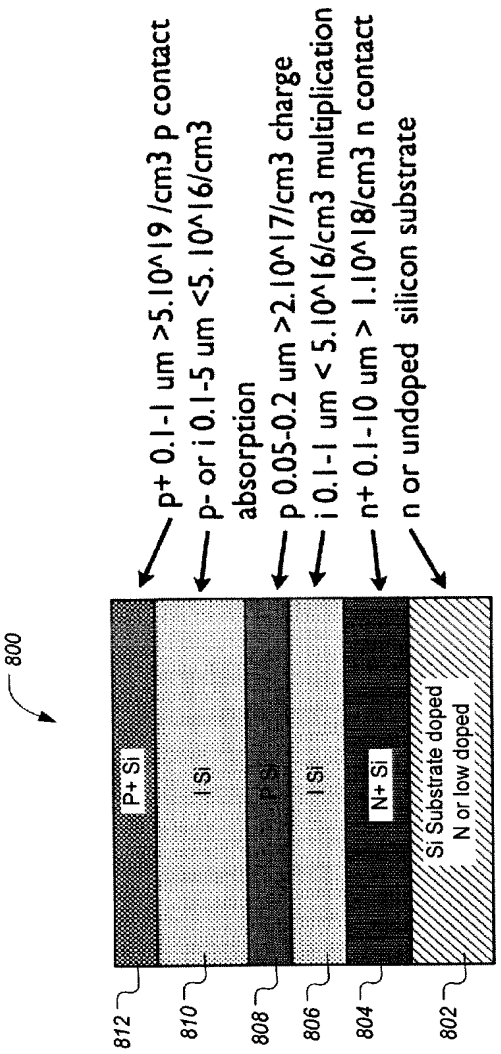

800
P+ Si
I Si
P Si
I Si
N+ Si
Si Substrate doped
N or low doped
812
810
808
806
804
802
p+ 0.1-1 um >5.10^19 /cm3 p contact
p- or i 0.1-5 um <5. 10^16/cm3
absorption
p 0.05-0.2 um >2.10^17/cm3 charge
i 0.1-1 um < 5.10^16/cm3 multiplication
n+ 0.1-10 um > 1.10^18/cm3 n contact
n or undoped silicon substrate

FIG. 8

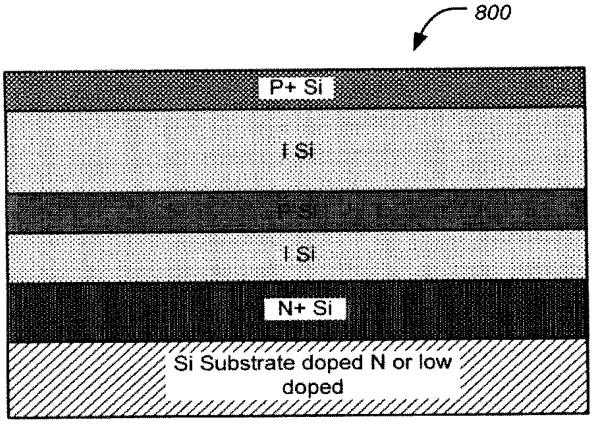

800
P+ Si
I Si
P Si
I Si
N+ Si
Si Substrate doped N or low doped

FIG. 9A

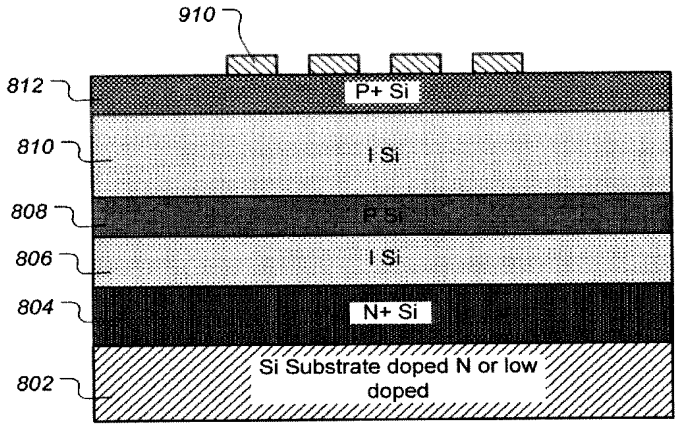

910
812
810
808
806
804
802
P+ Si
I Si
P Si
I Si
N+ Si
Si Substrate doped N or low doped

FIG. 9B

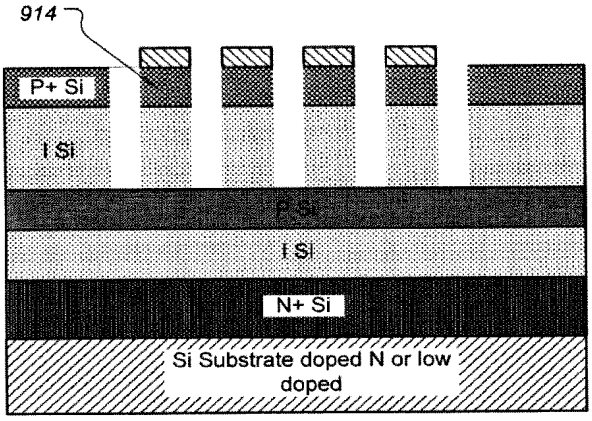

914
P+ Si
I Si
P Si
I Si
N+ Si
Si Substrate doped N or low doped

FIG. 9C

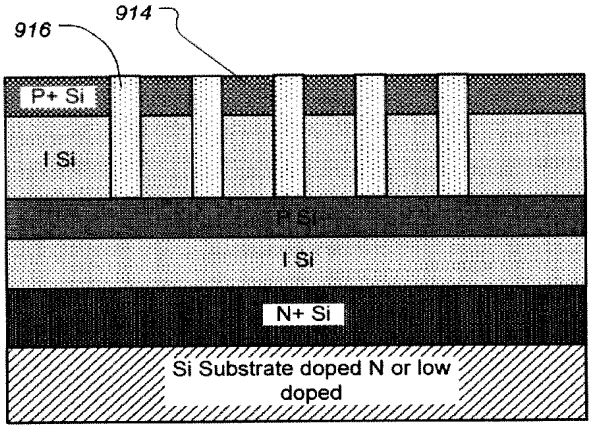

916
914
P+ Si
I Si
P Si
I Si
N+ Si
Si Substrate doped N or low doped

FIG. 9D

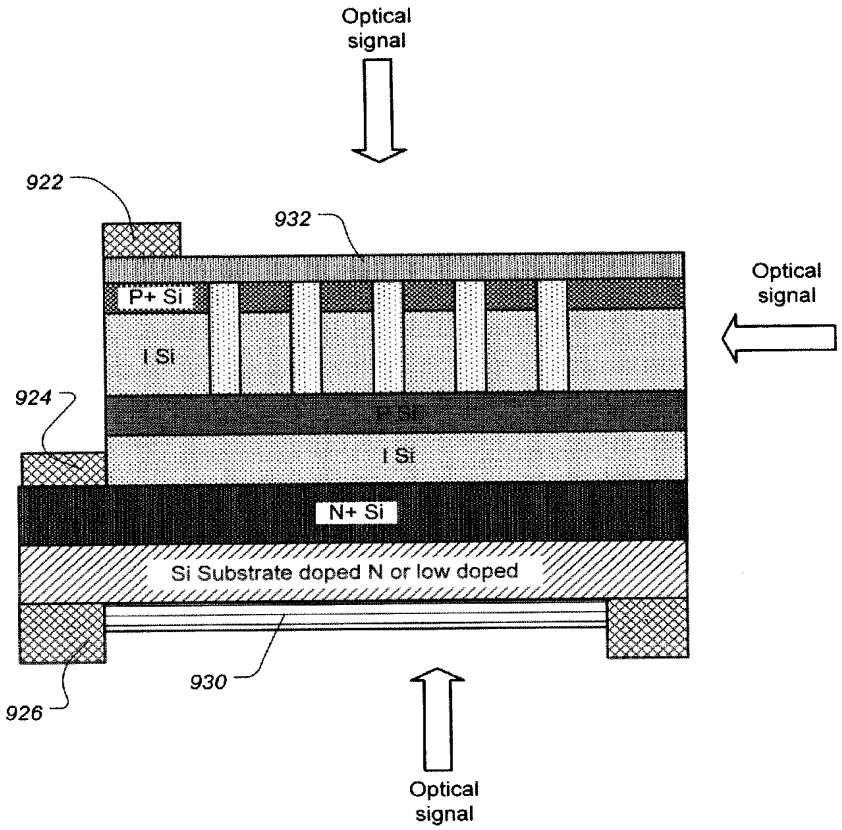

Optical signal
922
932
Optical signal
P+ Si
I Si
924
P Si
I Si
N+ Si
Si Substrate doped N or low doped
930
926
Optical signal

FIG. 9E

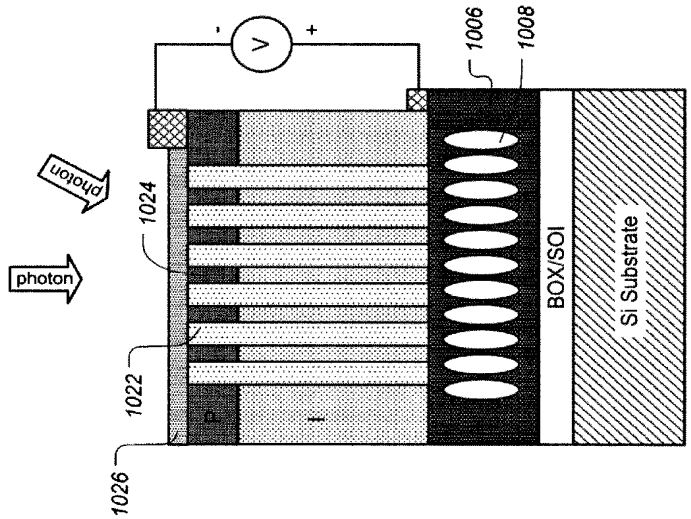


FIG. 10B

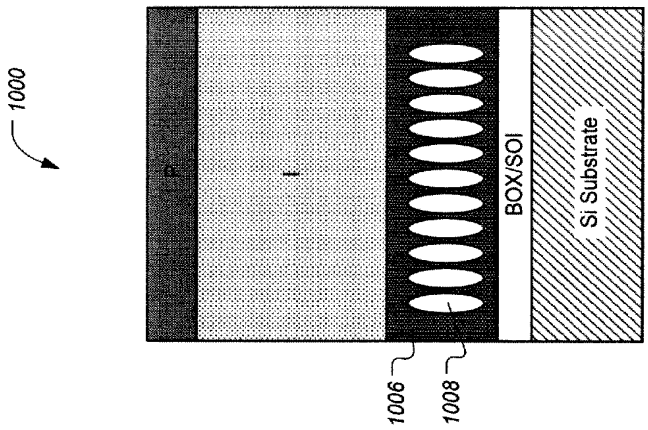


FIG. 10A

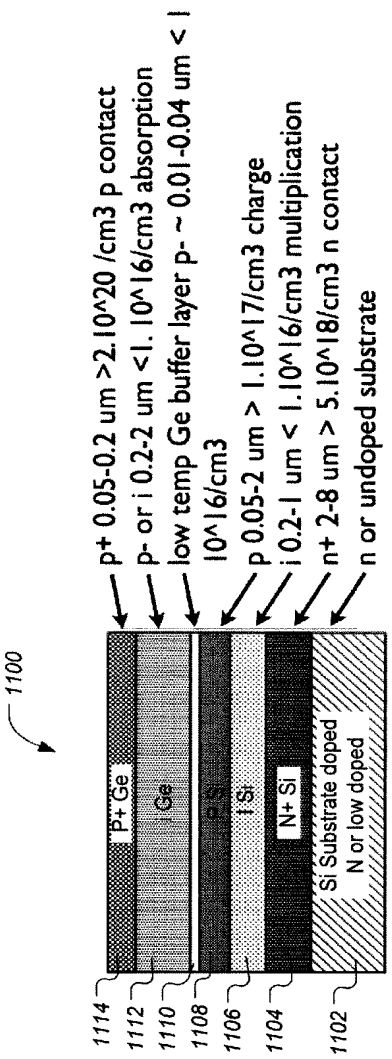

1100
P+ Ge
i Ge
P Si
I Si
N+ Si
Si Substrate doped
N or low doped
p+ 0.05-0.2 um >2.10^20 /cm3 p contact
p- or i 0.2-2 um <1. 10^16/cm3 absorption
low temp Ge buffer layer p- ~ 0.01-0.04 um < 1
10^16/cm3
p 0.05-2 um > 1.10^17/cm3 charge
i 0.2-1 um < 1.10^16/cm3 multiplication
n+ 2-8 um > 5.10^18/cm3 n contact
n or undoped substrate
1114
1112
1110
1108
1106
1104
1102

FIG. 11A

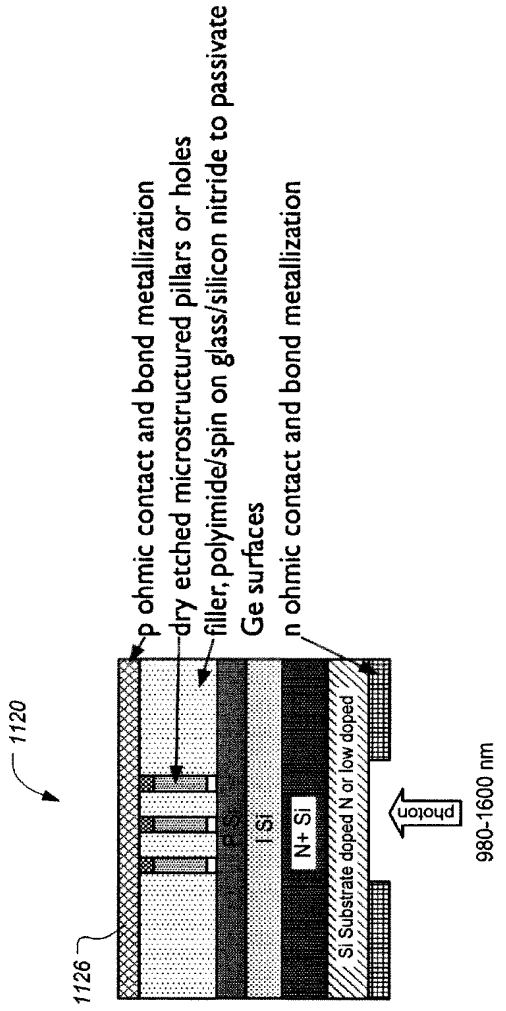

1120
1126
p ohmic contact and bond metallization
dry etched microstructured pillars or holes
filler, polyimide/spin on glass/silicon nitride to passivate
Ge surfaces
n ohmic contact and bond metallization
P+ Si
I Si
N+ Si
Si Substrate doped N or low doped
photon
980-1600 nm

FIG. 11B

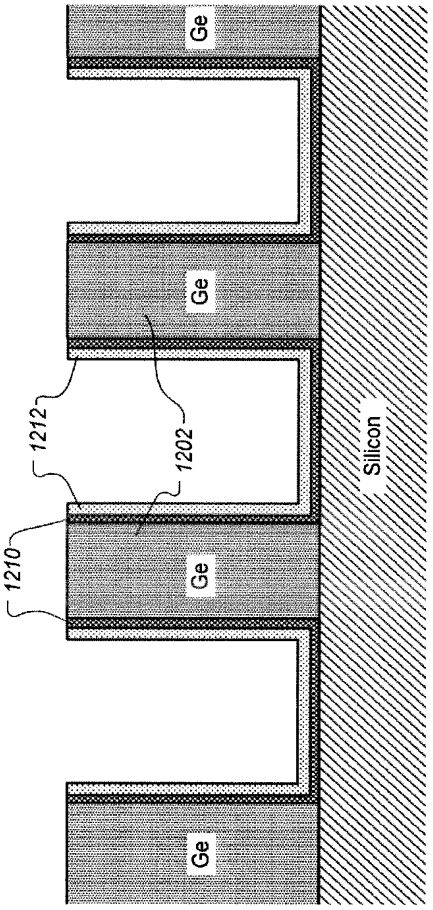


FIG. 12

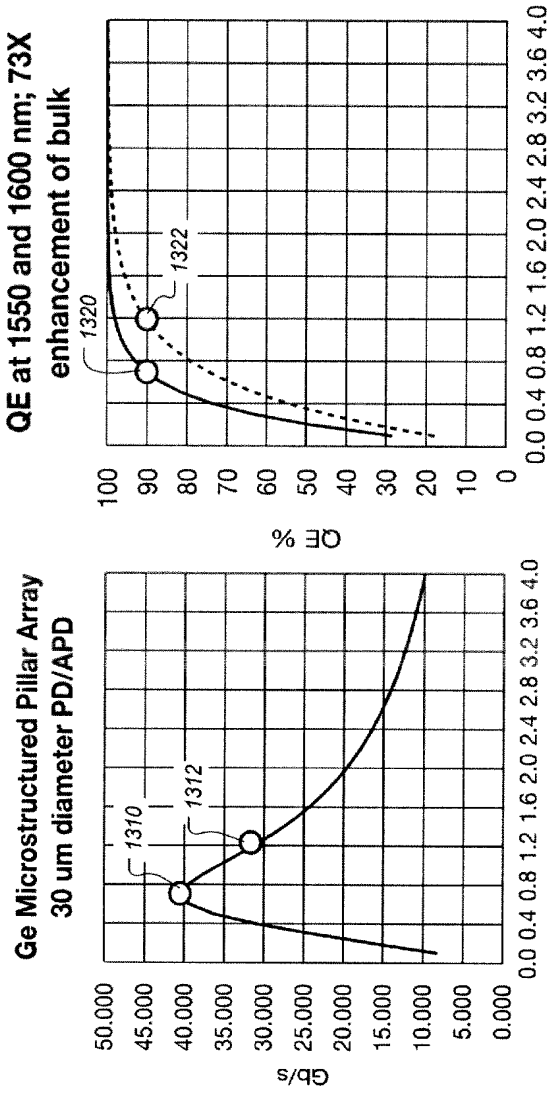


FIG. 13A

FIG. 13B

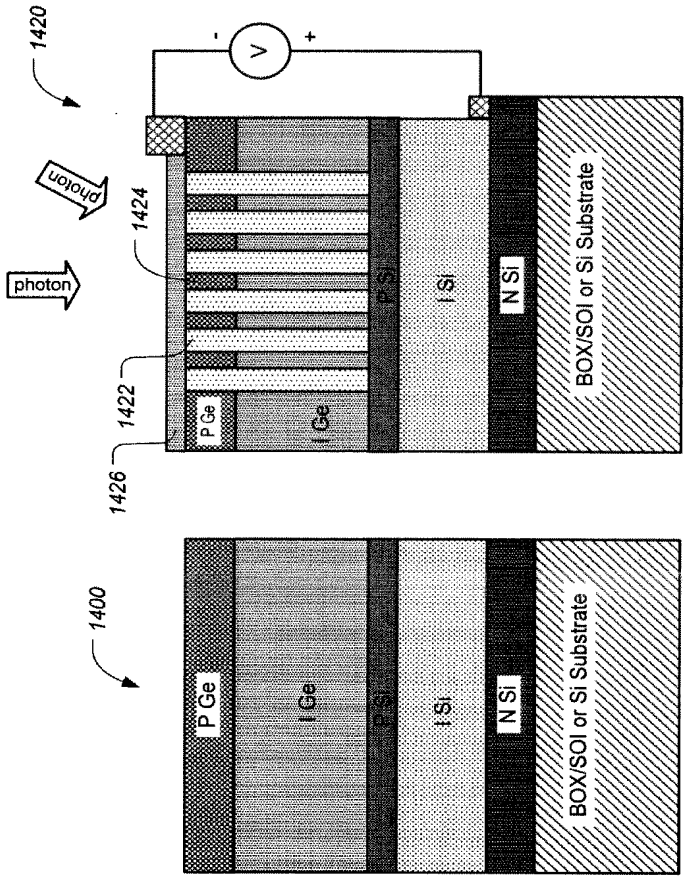


FIG. 14B

FIG. 14A

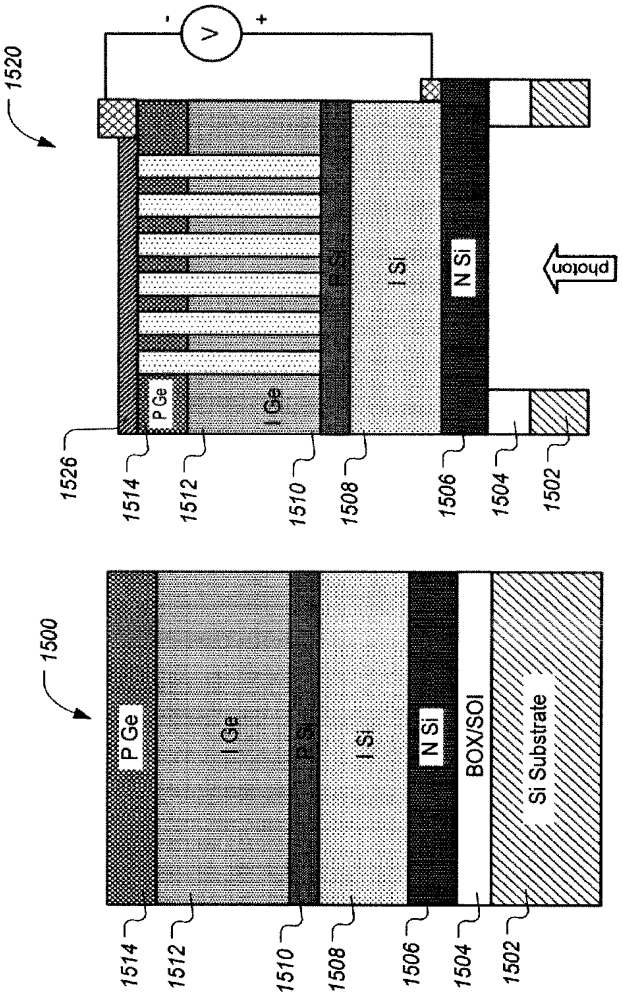


FIG. 15B

FIG. 15A

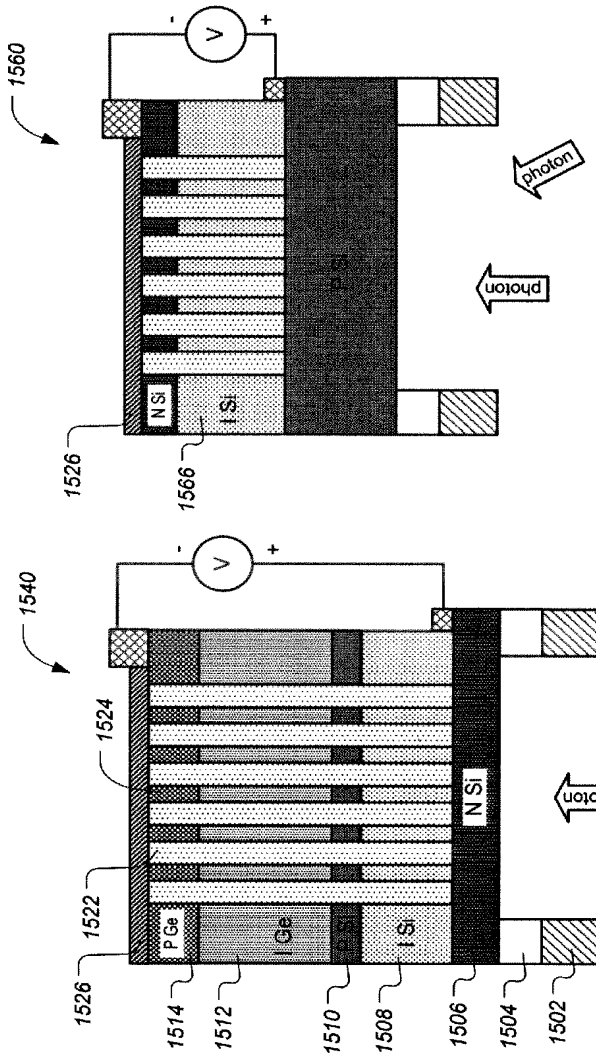


FIG. 15D

FIG. 15C

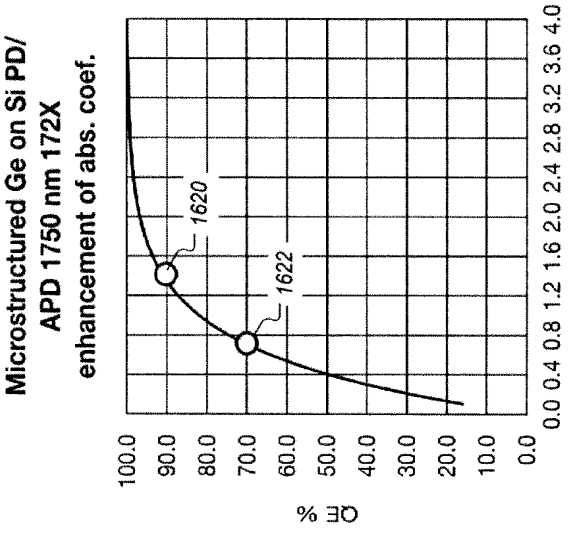


FIG. 16B

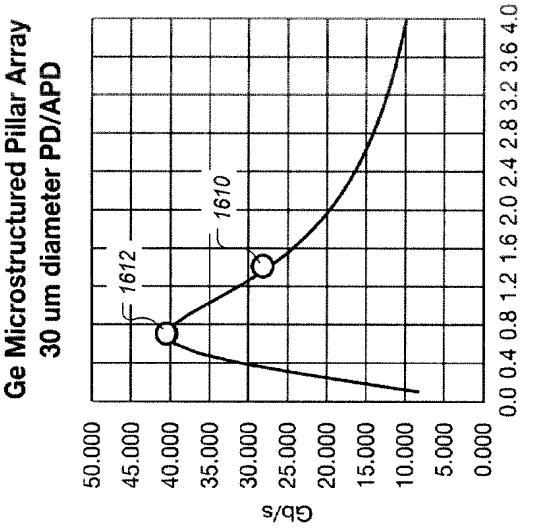


FIG. 16A

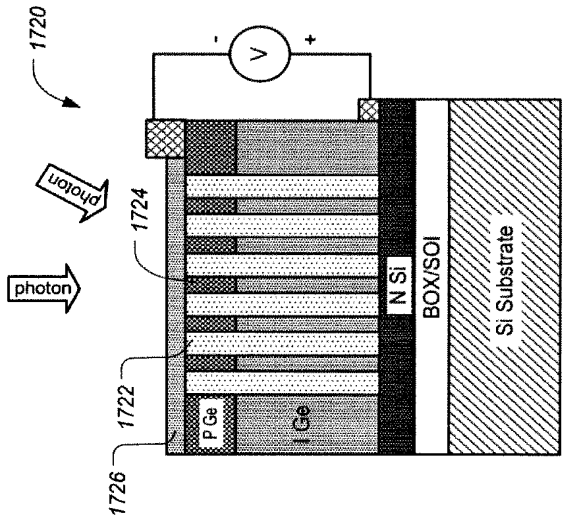


FIG. 17B

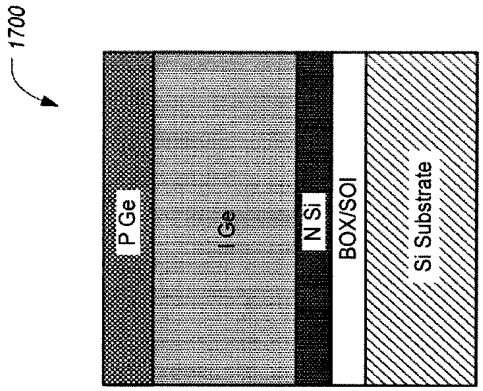


FIG. 17A

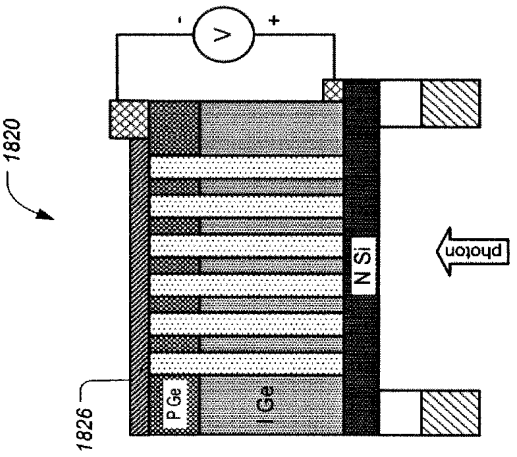


FIG. 18B

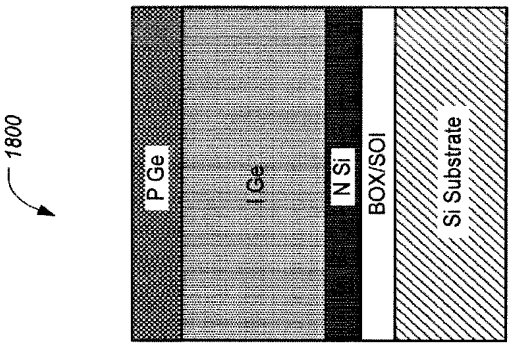


FIG. 18A

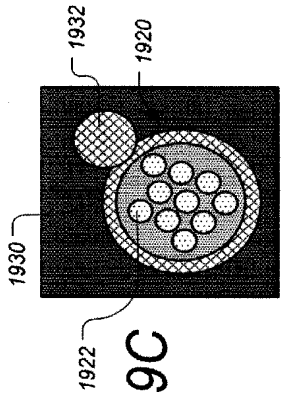


FIG. 19C

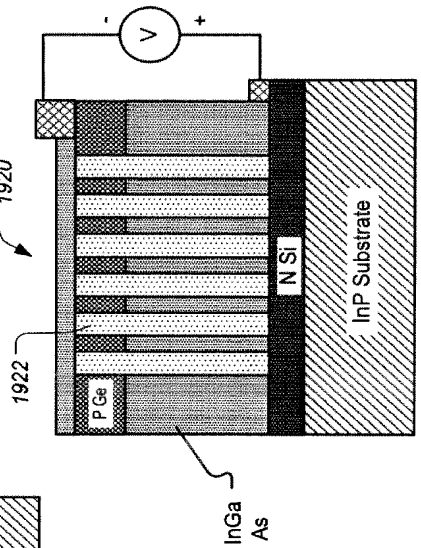


FIG. 19B

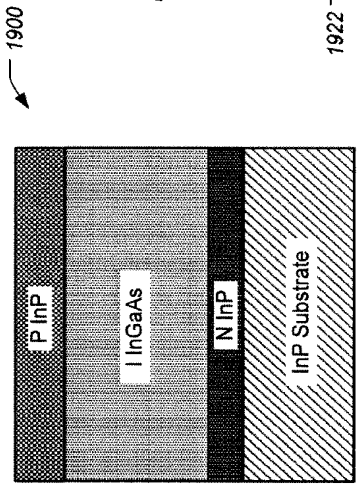


FIG. 19A

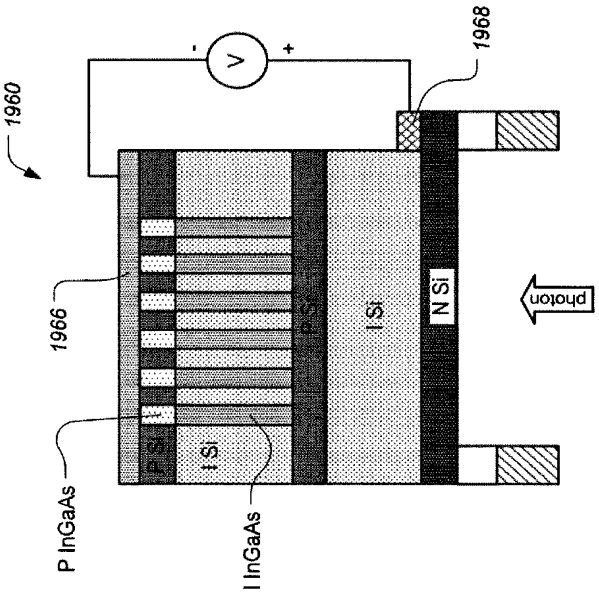


FIG. 19E

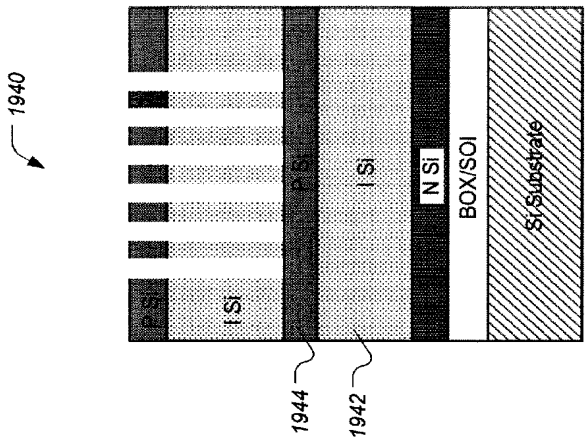


FIG. 19D

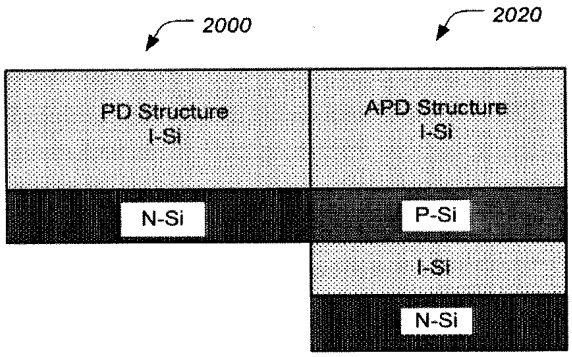

2000
2020
PD Structure
I-Si
APD Structure
I-Si
N-Si
P-Si
I-Si
N-Si

FIG. 20

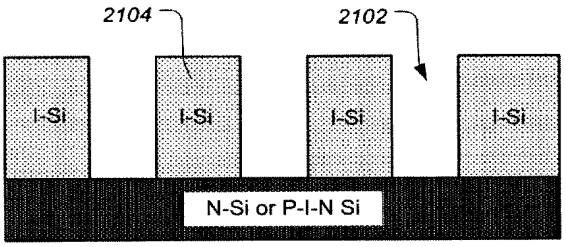

2104
2102
I-Si
I-Si
I-Si
I-Si
N-Si or P-I-N Si

FIG. 21

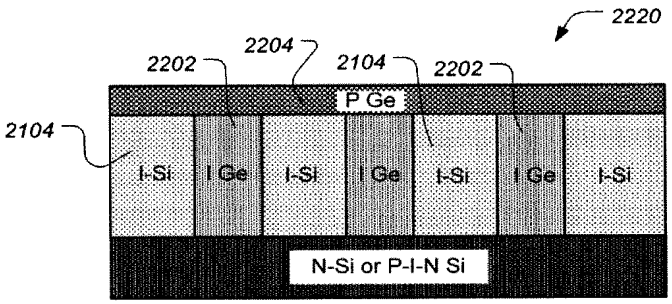

2220
2202
2204
2104
2202
P Ge
2104
I-Si
I Ge
I-Si
I Ge
I-Si
I Ge
I-Si
N-Si or P-I-N Si

FIG. 22

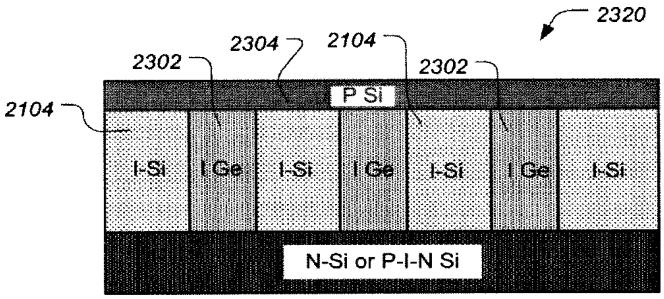

2320
2302
2304
2104
2302
P Si
2104
I-Si
I Ge
I-Si
I Ge
I-Si
I Ge
I-Si
N-Si or P-I-N Si

FIG. 23

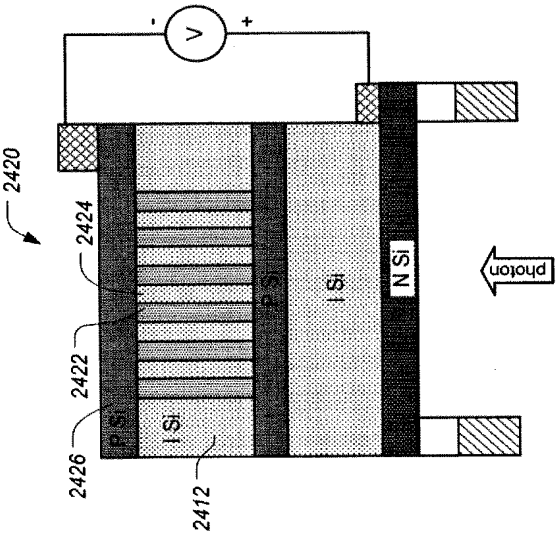


FIG. 24B

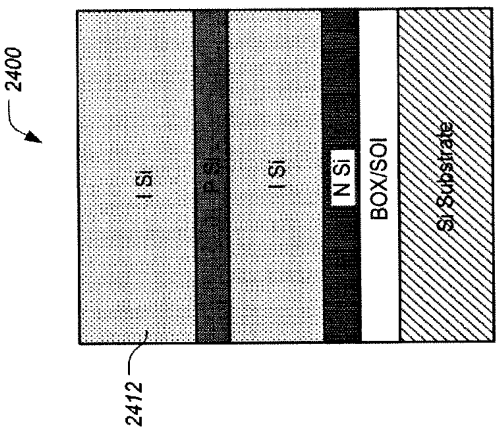


FIG. 24A

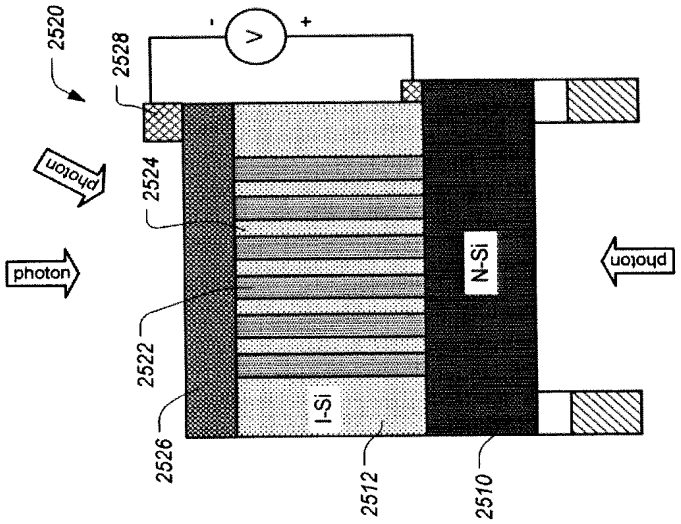


FIG. 25B

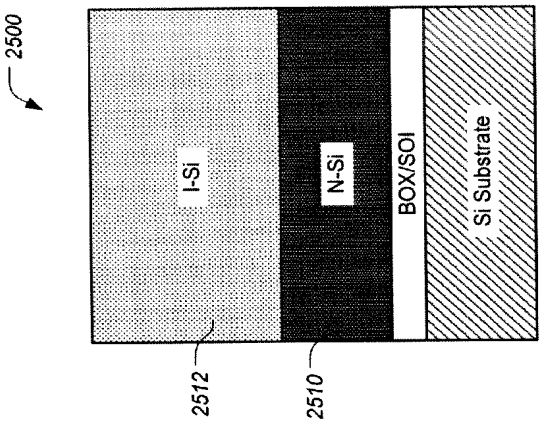


FIG. 25A

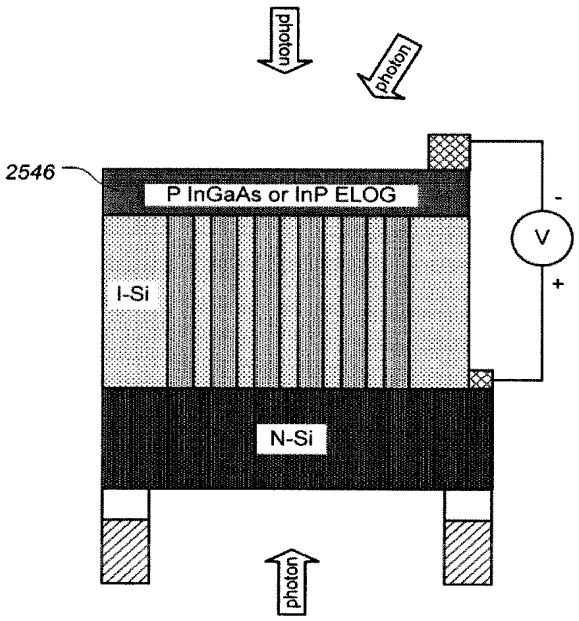


FIG. 25C

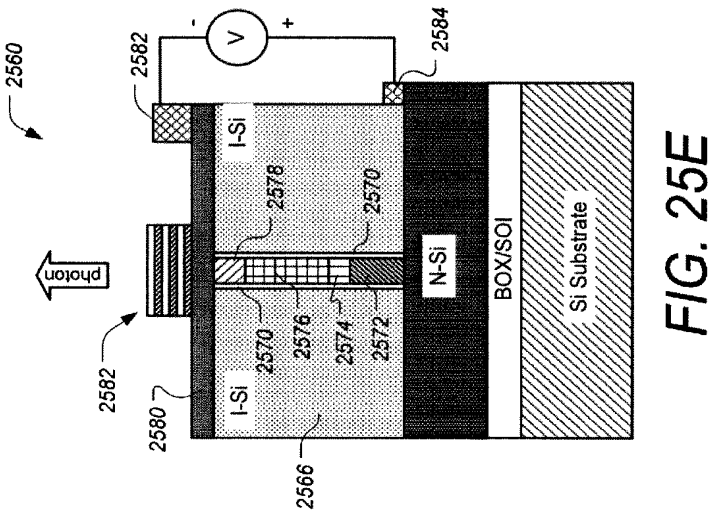


FIG. 25E

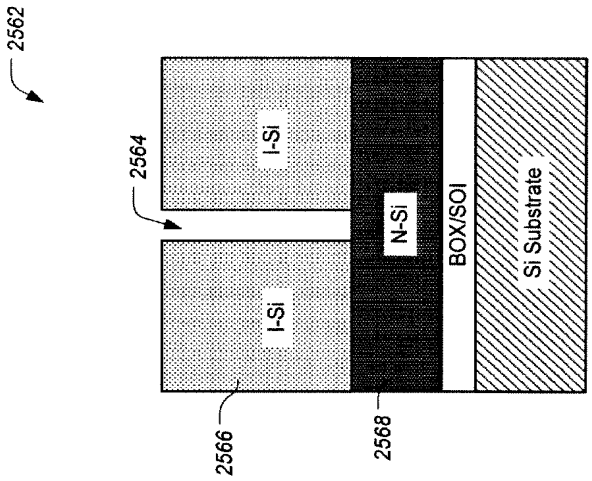


FIG. 25D

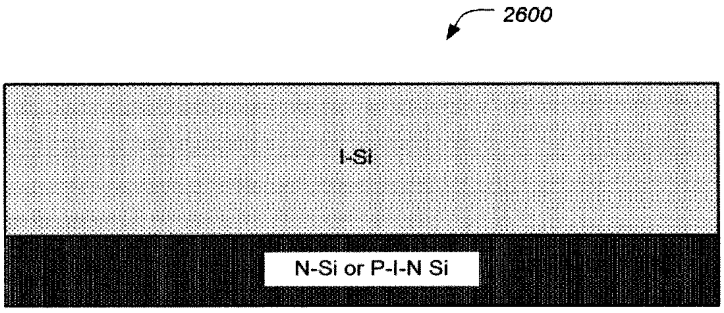


FIG. 26

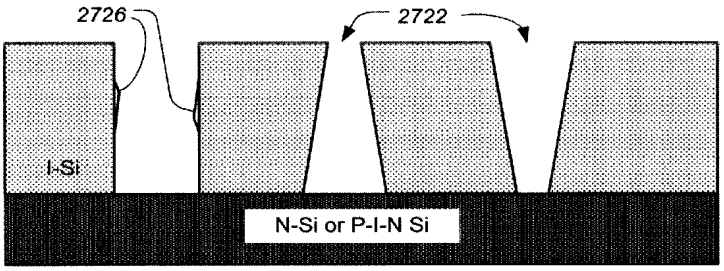


FIG. 27

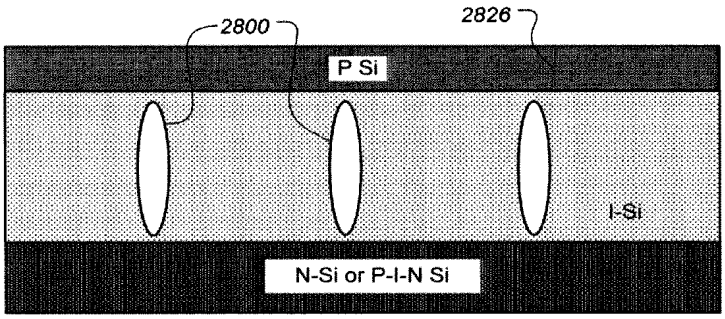

2800
2826
P Si
I-Si
N-Si or P-I-N Si

FIG. 28

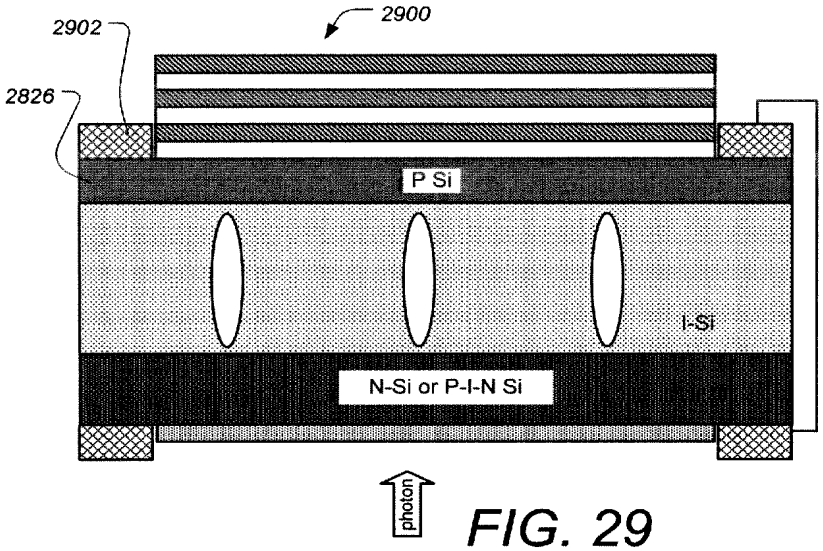

2902
2900
2826
P Si
I-Si
N-Si or P-I-N Si
photon

FIG. 29

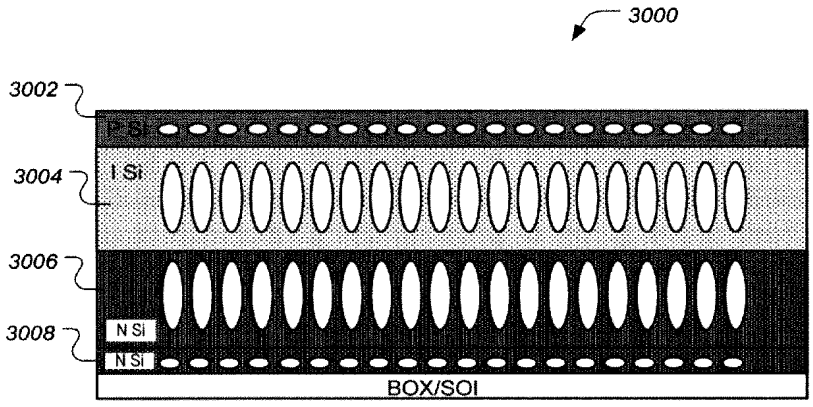

3000
3002
P Si
3004
I Si
3006
3008
N Si
N Si
BOX/SOI

FIG. 30

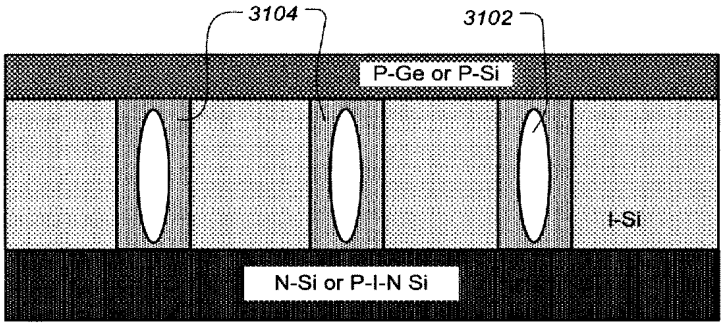

3104
3102
P-Ge or P-Si
I-Si
N-Si or P-I-N Si

FIG. 31

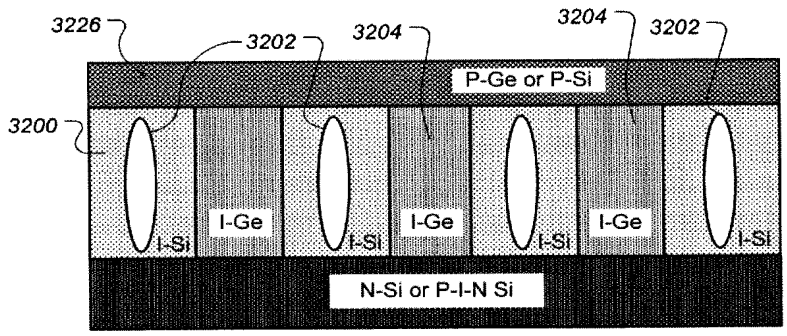

3226
3202
3204
3204
3202
P-Ge or P-Si
3200
I-Si
I-Ge
I-Si
I-Ge
I-Si
I-Ge
I-Si
N-Si or P-I-N Si

FIG. 32

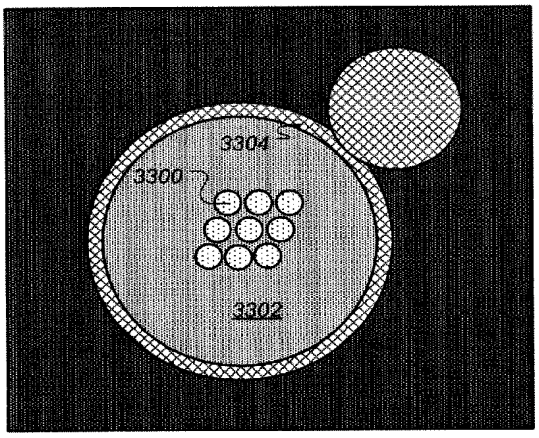

3304
3300
3302

FIG. 33

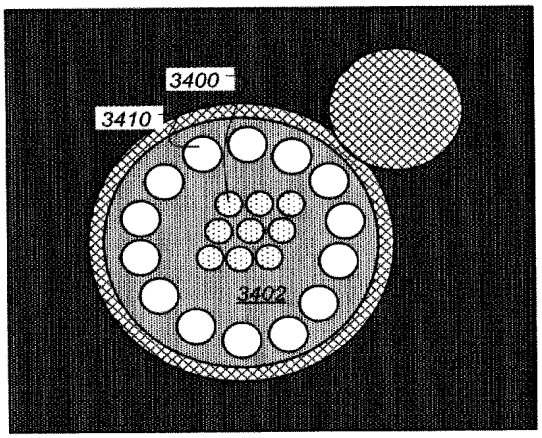


FIG. 34

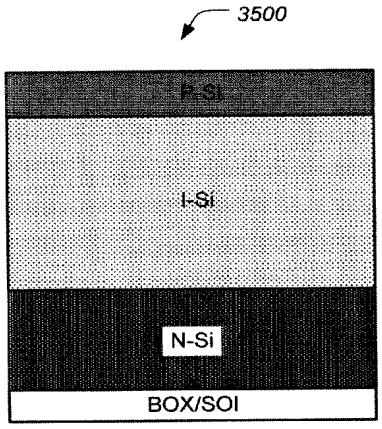


FIG. 35
(prior art)

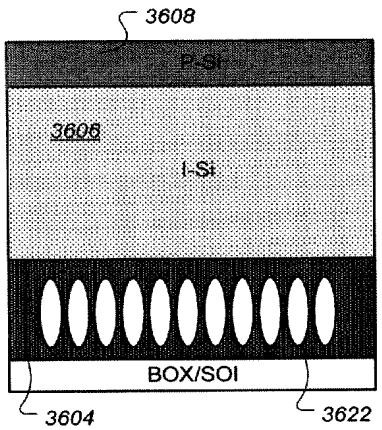


FIG. 36

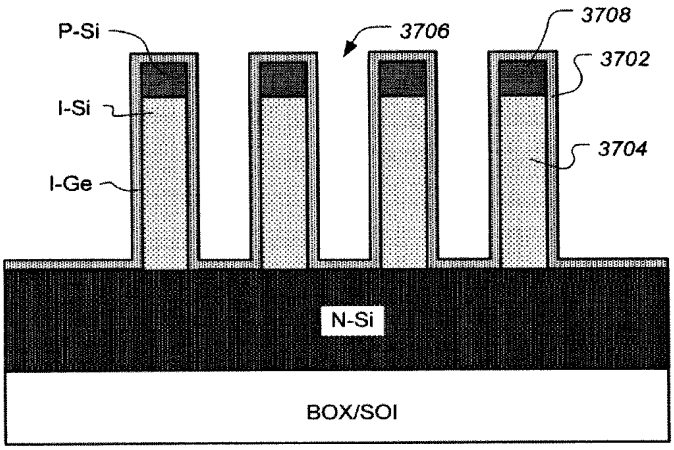

P-Si
3706
3708
3702
I-Si
3704
I-Ge
N-Si
BOX/SOI

FIG. 37

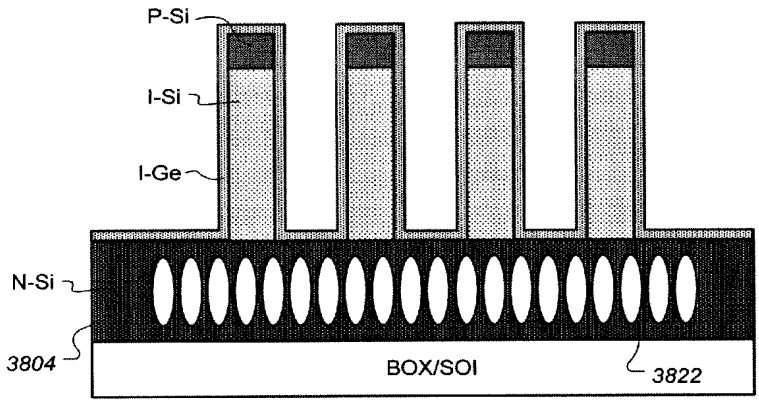

P-Si
I-Si
I-Ge
N-Si
3804
BOX/SOI
3822

FIG. 38

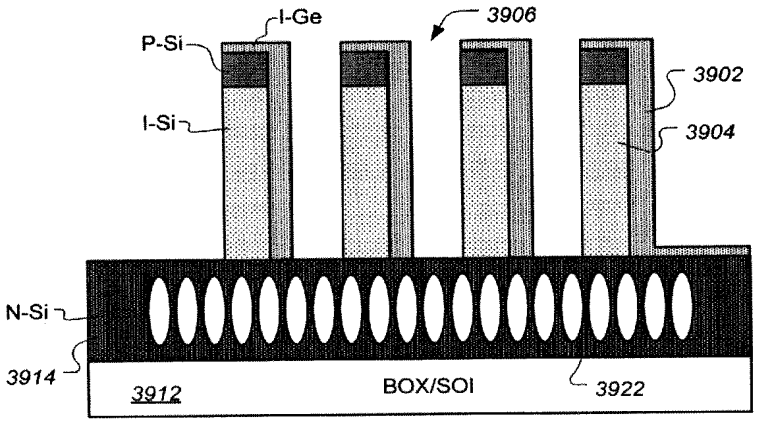

I-Ge
3906
P-Si
3902
I-Si
3904
N-Si
3914
3912
BOX/SOI
3922

FIG. 39

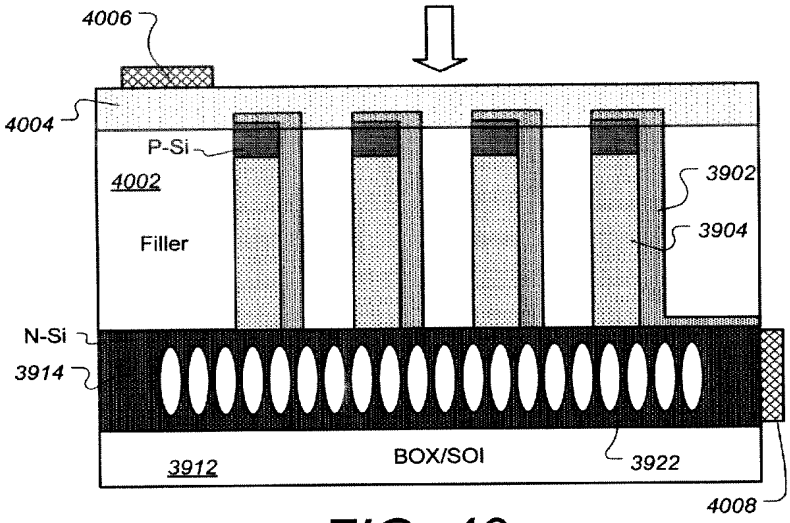

4006
4004
P-Si
4002
Filler
3902
3904
N-Si
3914
3912
BOX/SOI
3922
4008

FIG. 40

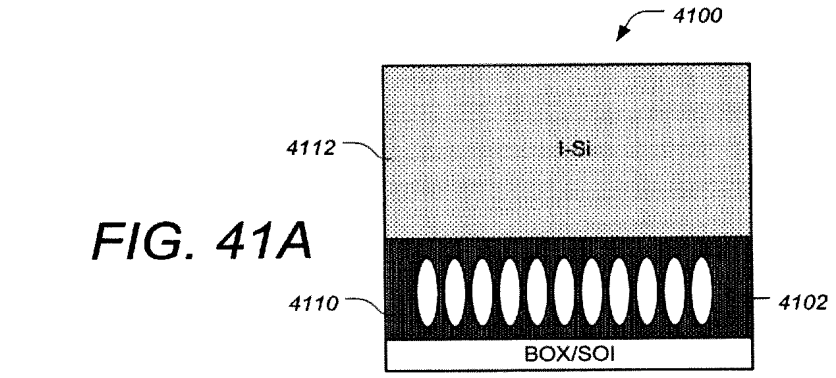


FIG. 41A

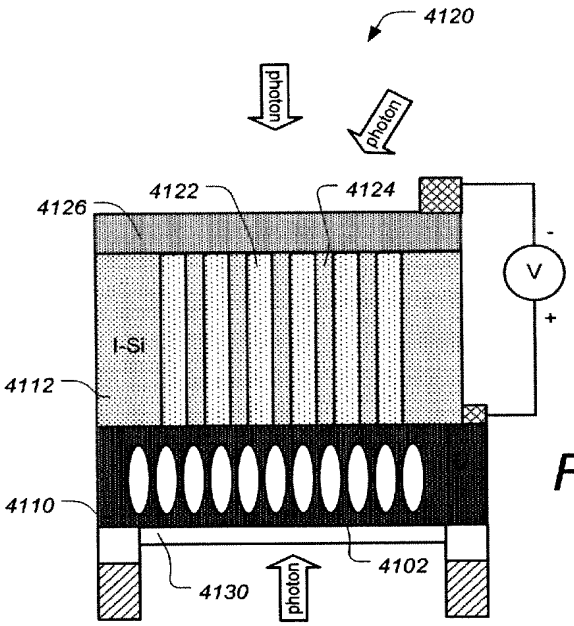
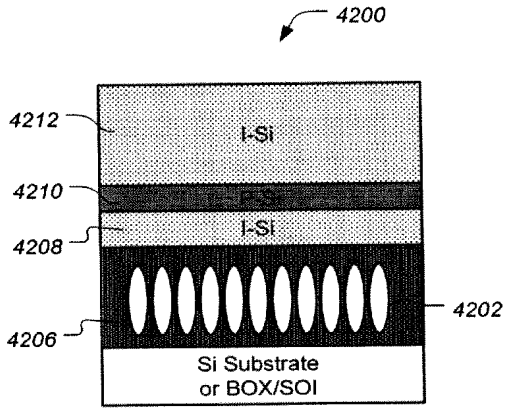


FIG. 41B

FIG. 42A



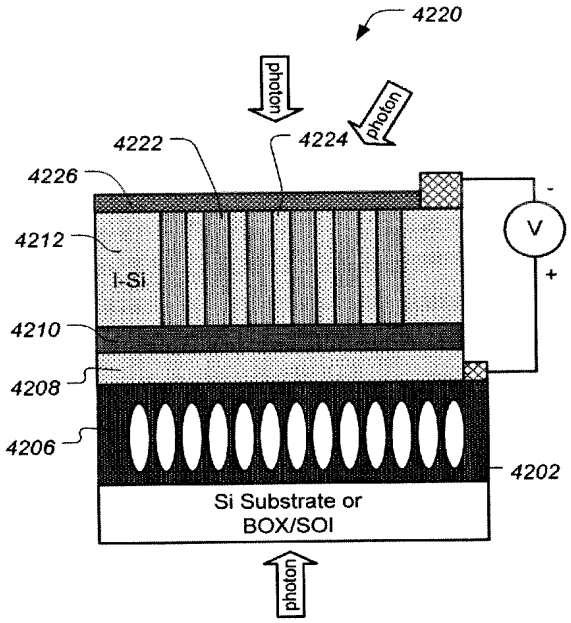
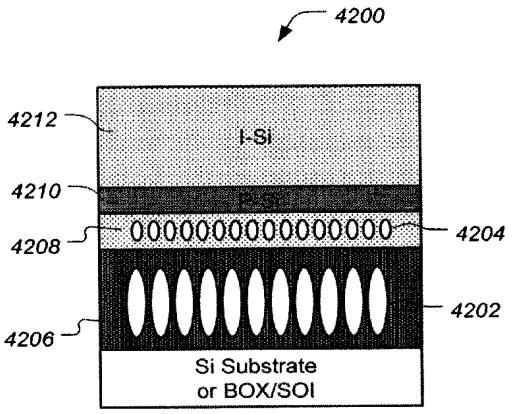


FIG. 42B

FIG. 42C



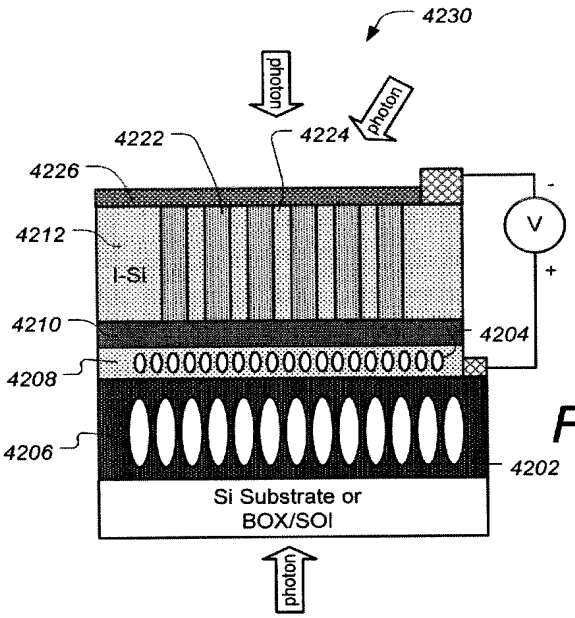


FIG. 42D

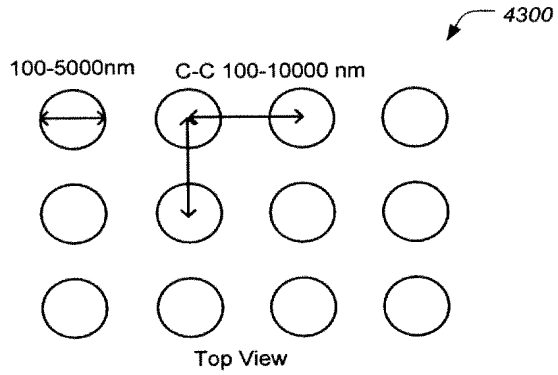

4300
100-5000nm
C-C 100-10000 nm
Top View

FIG. 43

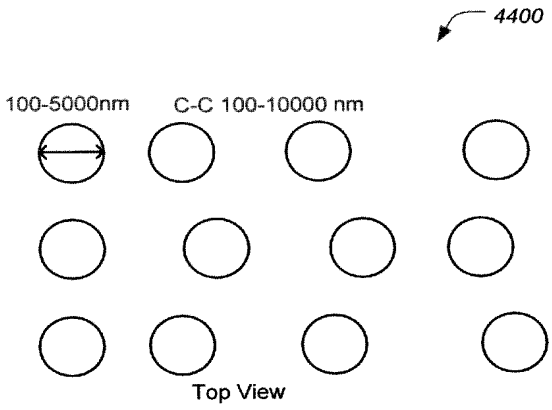

4400
100-5000nm
C-C 100-10000 nm
Top View

FIG. 44

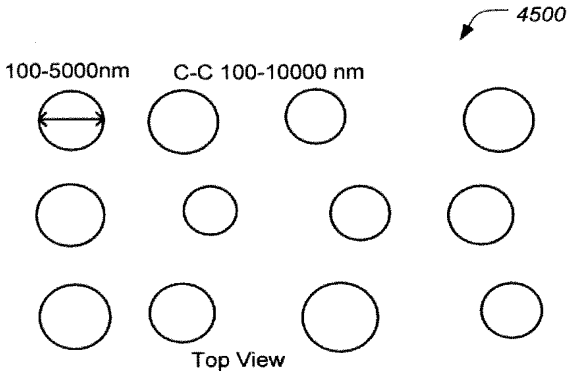

4500
100-5000nm
C-C 100-10000 nm
Top View

FIG. 45

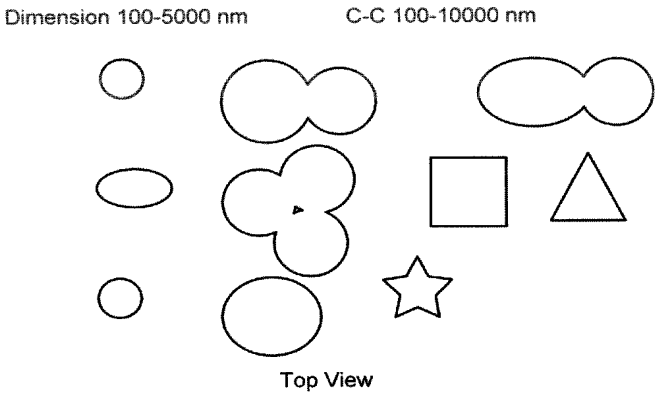

Dimension 100-5000 nm
C-C 100-10000 nm
Top View

FIG. 46

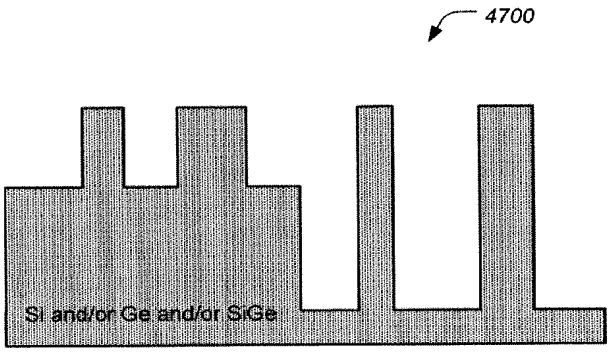


FIG. 47

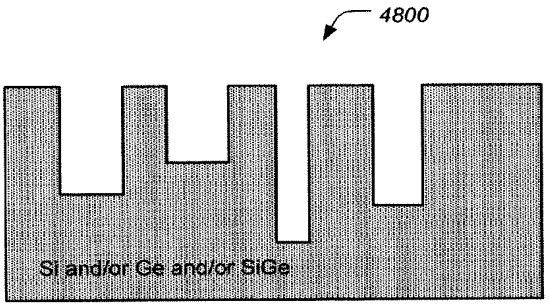


FIG. 48

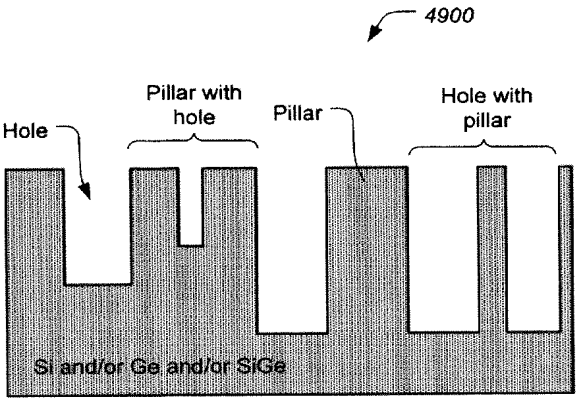

4900
Hole
Pillar with hole
Pillar
Hole with pillar
Si and/or Ge and/or SiGe

FIG. 49

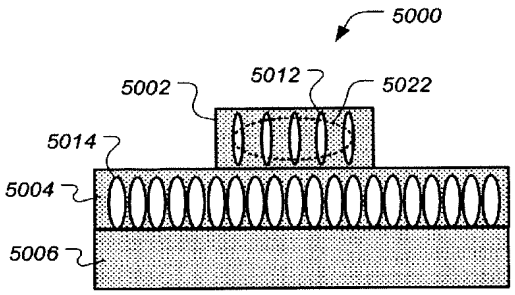

5000
5002
5012
5022
5014
5004
5006

FIG. 50

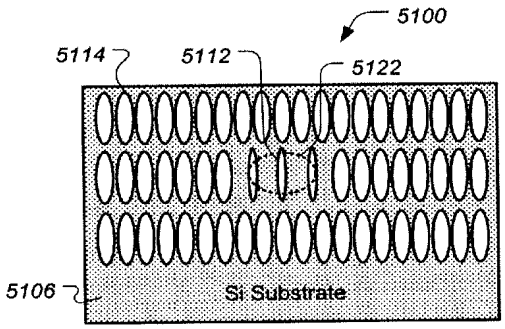

5100
5114
5112
5122
5106
Si Substrate

FIG. 51

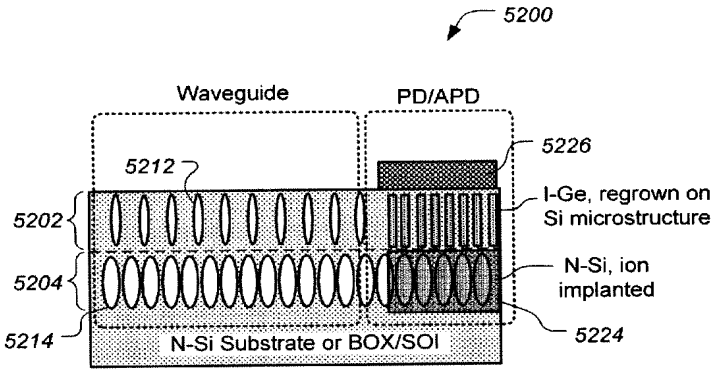

5200
Waveguide
PD/APD
5212
5226
I-Ge, regrown on
Si microstructure
5202
5204
N-Si, ion
implanted
5214
5224
N-Si Substrate or BOX/SOI

FIG. 52

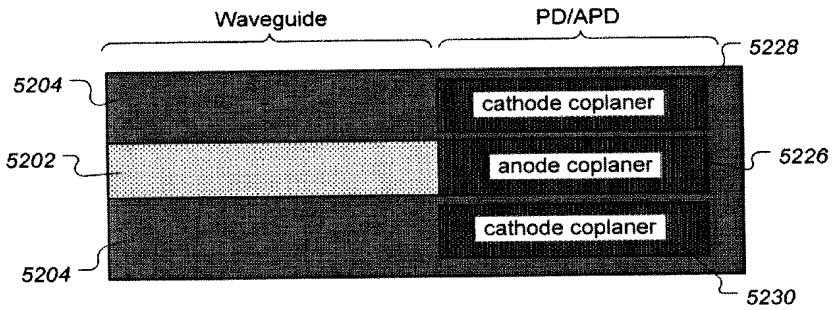


FIG. 53

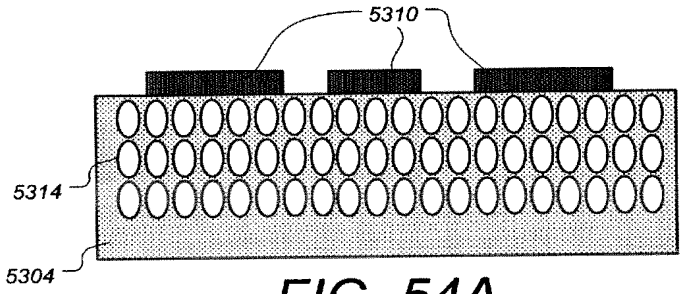


FIG. 54A

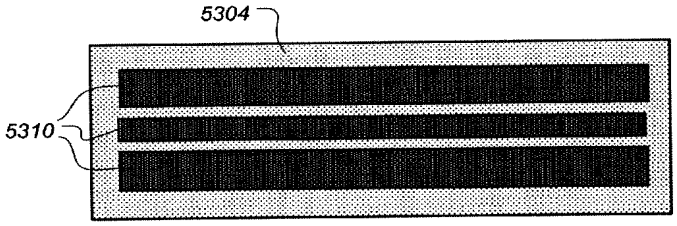


FIG. 54B

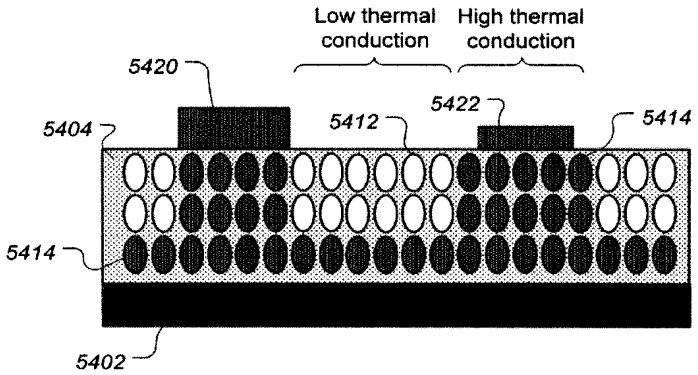

Low thermal conduction
High thermal conduction
5420
5422
5404
5412
5414
5414
5402

FIG. 55

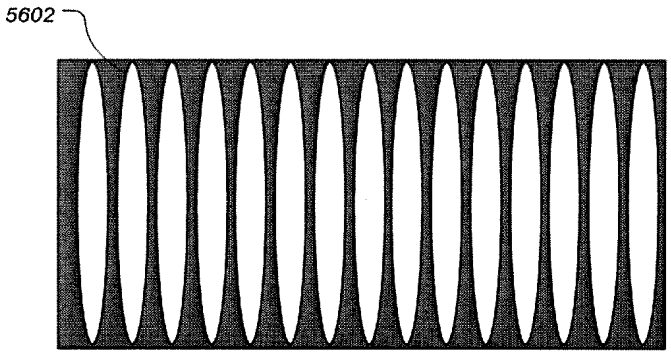

5602

FIG. 56

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Declarations under Rule 4.17:

— *as to the applicant's entitlement to claim the priority of the earlier application (Rule 4.17(iii))*

Published:

— *without international search report and to be republished upon receipt of that report (Rule 48.2(g))*

(54) **Title**: HIGH EFFICIENCY VERTICAL OPTICAL COUPLER USING SUB-WAVELENGTH HIGH CONTRAST GRATING

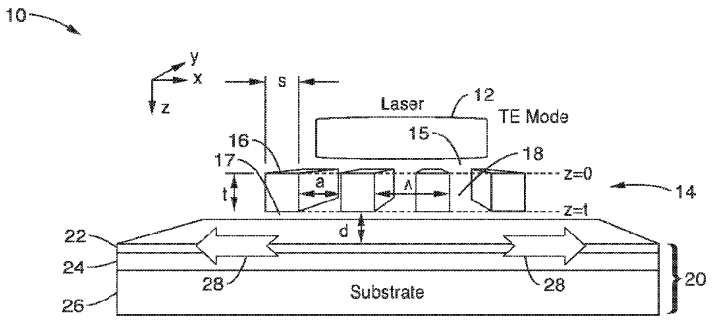


FIG. 1

(57) **Abstract**: A vertical optical coupler which redirects light transmission in response to the interaction between a sub-wavelength high contrast grating (HCG) having a plurality of spaced apart segments of grating material which is optically coupled to a wave-guide. For a selected set of material, grating geometry, gaps and spacing, the light directed at a normal incidence into the optical coupler is angularly displaced in traveling in the optical waveguide, while light directed along the optical waveguide is angularly displaced in being output at normal incidence from the optical coupler. The coupler is integrated into a number of device embodiments, including: a coupler between angularly displaced waveguides, lasers, light emitting diodes (LEDs) and solar cells.

WO 2012/149441 A2

HIGH EFFICIENCY VERTICAL OPTICAL COUPLER USING SUB-WAVELENGTH HIGH CONTRAST GRATING

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application claims priority from U.S. provisional patent application serial number 61/480,467 filed on April 29, 2011, incorporated herein by reference in its entirety.

STATEMENT REGARDING FEDERALLY SPONSORED RESEARCH OR DEVELOPMENT

[0002] This invention was made with Government support under Grant Number N00244-09-1-013 awarded by the Department of Defense (DOD) under the National Security Science and Engineering Faculty Fellowship (NSSEFF) Program. The Government has certain rights in the invention.

INCORPORATION-BY-REFERENCE OF MATERIAL SUBMITTED ON A COMPACT DISC

[0003] Not Applicable

NOTICE OF MATERIAL SUBJECT TO COPYRIGHT PROTECTION

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BACKGROUND OF THE INVENTION

[0005] 1. Field of the Invention

[0006] This invention pertains generally to optical transmission, and more particularly to an optical coupler for changing the direction of light transmission.

[0007] 2. Description of Related Art

[0008] High-density photonic integrated circuits (PICs) are important to integrate various optical functionalities in one single chip for many applications, ranging from communications, sensing, display, to system-on-a-chip and lab-on-a-chip applications. These devices, by and large, utilize light guided by waveguides in the direction parallel to the wafer surface, known as the in-plane direction. Devices are cascaded longitudinally (in the direction of light propagation) or laterally (orthogonal to light propagation) to achieve higher levels of functionalities. Various material platforms have been reported, including InP-based material, silicon and silicon-on-insulator (SOI), various organic materials, and so forth. Efficient coupling of a surface-normal propagating light beam, such as from an output of an optical fiber or free-space optics, or a device, (e.g. lasers such as vertical cavity surface emitting lasers (VCSEL)), with PICs is especially desirable.

[0009] However, conventional second order gratings have limited efficiency, often significantly below 25% in each in-plane direction. Some approaches propose adding reflection DBRs or by using slanted gratings. However, those approaches can make fabrication complicated, and perhaps too complicated for practical manufacture.

[0010] Accordingly, a need exists for an optical coupling means which can couple and redirect light at high efficiencies. The present invention fulfills that need and overcomes shortcomings of prior coupling technologies.

BRIEF SUMMARY OF THE INVENTION

[0011] A vertical optical coupler with high coupling efficiency using a sub-wavelength high contrast grating (HCG), and a number of novel device

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designs into which the vertical optical coupler is integrated, are desc
HCG is a single-layer sub-wavelength grating in which the grating high-index bars are completely surrounded by a low-index material. It has been demonstrated that high-Q resonances and high reflectivity can be beneficially achieved under proper design of grating dimensions. For regular grating couplers, when the period Λ is equal to wavelength, the surface normal incident light couples into the in-plane waveguide. By utilizing the resonance nature of HCG, the coupling efficiency from vertical incidence to in-plane waveguide can be increased to a total of at least 92% in both in-plane propagation directions (combined). The inventive coupler can be used in the reverse direction, with input received from an in-plane waveguide and directed to the vertical direction as well. Efficiencies of greater than 90% are achieved for both single-side incidence and double-side incidence. Various inventive devices incorporating the vertical optical coupler are presented.

[0012] Further aspects of the invention will be brought out in the following portions of the specification, wherein the detailed description is for the purpose of fully disclosing preferred embodiments of the invention without placing limitations thereon.

BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWING(S)

[0013] The invention will be more fully understood by reference to the following drawings which are for illustrative purposes only:

[0014] FIG. 1 is a schematic of a "vertical to in-plane" coupler according to an embodiment of the present invention.

[0015] FIG. 2 is a schematic of an "in-plane to vertical" coupler with symmetrical incidence according to an embodiment of the present invention.

[0016] FIG. 3 is a schematic of a single-side "in-plane to vertical" coupler according to an embodiment of the present invention.

[0017] FIG. 4A and FIG. 4B are graphs of operating modes utilized according to an embodiment of the present invention, showing first through third modes

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in FIG. 4A, and an overall mode profile at the output plane $z = t$ in FI

[0018] FIG. 5 is a graph of HCG surface normal reflectivity utilized according to an embodiment of the present invention.

[0019] FIG. 6 is a graph of a mode dispersion relationship utilized according to an embodiment of the present invention.

[0020] FIG. 7A and FIG. 7B are graphs of vertical to in-plane coupling, utilized according to an embodiment of the present invention, showing field distribution in FIG. 7A, and coupling efficiency in FIG. 7B.

[0021] FIG. 8A and FIG. 8B are graphs of coupling utilized according to an embodiment of the present invention, showing symmetrical in-plane incidence to vertical coupling field distribution in FIG. 8A, and coupling efficiency in FIG. 8B.

[0022] FIG. 9A and FIG. 9B are graphs of in-plane characteristics utilized according to an embodiment of the present invention, showing waveguide field distribution for the case of in-plane reflection in FIG. 9A, and in-plane reflectivity in FIG. 9B.

[0023] FIG. 10A through FIG. 10C are graphs of efficiency spectrum in response to different HCG thickness utilized according to an embodiment of the present invention, showing in-plane reflection (-x direction) in FIG. 10A, vertical coupling (+z direction) in FIG. 10B, and in-plane transmission (+x direction) in FIG. 10C.

[0024] FIG. 11A and FIG. 11B are graphs of single side in-plane incidence to vertical coupling field distribution in FIG. 11A, and coupling efficiency in FIG. 11B utilized according to an embodiment of the present invention.

[0025] FIG. 12 is a schematic of light being turned in a hollow-core waveguide (HW) utilizing vertical couplers according to an embodiment of the present invention.

[0026] FIG. 13 is a schematic of light being turned in a hollow-core waveguide (HW) utilizing side-coupling according to an embodiment of the present invention.

[0027] FIG. 14 is a schematic of connecting two HCG hollow core waveguide

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couplers according to an embodiment of the present invention to turr

[0028] FIG. 15 is a schematic of an HCG multiplexer according to an embodiment of the present invention.

[0029] FIG. 16 is a schematic of an HCG demultiplexer according to an embodiment of the present invention.

[0030] FIG. 17 is a schematic of vertical incidence to single side in-plane waveguide coupling according to an embodiment of the present invention.

[0031] FIG. 18 is a schematic of parallel waveguide coupling according to an embodiment of the present invention.

[0032] FIG. 19 is a schematic of an HCG vertical coupler and reflector for surface-emitting quantum cascade laser according to an embodiment of the present invention.

[0033] FIG. 20 is a schematic of an HCG reflector as cavity mirror in GaN laser diode according to an embodiment of the present invention.

[0034] FIG. 21 is a schematic of HCG light extraction for GaN light emitter diode according to an embodiment of the present invention.

[0035] FIG. 22 is a schematic of an HCG light collector for a solar cell according to an embodiment of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

[0036] **1. High Contrast Grating Vertical Coupler Structure**

[0037] FIG. 1 through FIG. 3 illustrate different operations of the inventive vertical coupler which can couple light from a vertical light source into both directions of a horizontal waveguide (FIG. 1), or from both directions of the horizontal waveguide to the vertical direction (FIG. 2), or utilize a single side operation of the vertical coupler in which light is preferentially coupled to or from one direction of the waveguide (FIG. 3). The optical coupler thus angularly displaces light transmission passing either way through the coupler. These operations of the vertical optical coupling are described in greater detail in the following sections. In one embodiment, the vertical coupler comprises a sub-wavelength high contrast grating (HCG) configured with proper grating

dimensions and spacing for interoperation with a waveguide whose characteristics match the HCG. The period of the HCG preferably should be close to, or the same as, periodicity of the field profile for a specific waveguide mode in the propagation direction (i.e., propagation constant).

[0038] In the embodiment illustrated in FIG. 1, a laser light source 12, comprising a laser (which, for example, can be a VCSEL or edge emitting laser), is shown coupled to a HCG 14, having periodic spaced apart segments of grating material 16 of width (s) and thickness (t), with a spacing 18 of distance (a) between segments and period Λ. Although the embodiments address the use of a VCSEL, it should be appreciated that a laser or edge emitting laser can be generally substituted. The HCG is positioned with a gap 15 beneath the VCSEL, and a gap 17 above the waveguide 20.

[0039] The gap size is a design parameter which can influence power coupling efficiency and its spectral width from laser into waveguide. The gap size design can be optimized by finite-difference time-domain (FDTD) simulations or numerical analysis. A typical value is in the range from 10 nm to about 1,500 nm, depending on the refractive indices of the material used for the gap and the HCG, as well as the wavelength of interest. In the range given above, there exists an optimum value range with which a high coupling efficiency and broad spectral width is achieved. As the gap increases and reduces from the optimum range, both coupling efficiency and spectral width are reduced.

[0040] In this example embodiment, waveguide 20 is shown comprising an in-plane silicon-on-insulator (SOI) waveguide having a waveguide layer 22 and buried oxide layer 24. The buried oxide layer should be sufficiently thick that the light is guided by the waveguide 22 and does not experience significant leakage into the silicon substrate. A plane wave with the E-field polarized in the y-direction (hereinafter TE polarization) propagates in the z-direction (downward) from VCSEL 12 towards HCG 14. The three physical parameters that select the characteristics of the HCG are period (Λ), thickness (t) and duty cycle (η). The period (Λ) of sub-wavelength high contrast grating should be smaller than the working wavelength while the thickness can be

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larger. The duty cycle (η) is defined herein as the ratio of grating ba period (s/Λ). In this example, an in-plane SOI waveguide is utilized and placed beneath the HCG, separated by a gap 17 denoted by (d). In this example, the silicon waveguide thickness is 0.1 μm, SiO_2 layer thickness is 1.35 μm. Based on such structure, the light incidence from +z direction is coupled into the waveguide in both +x and –x directions 28 symmetrically. It is also seen in the figure that the top surface of the HCG waveguide is designated as z=0, while the bottom is at z= t.

[0041] In FIG. 2, operation of the vertical coupler is illustrated in example embodiment 30 with light symmetrically incident along the waveguide being output vertically. The sub-wavelength HCG 32 can have the same parameters as described for FIG. 1 with grating segments 32, and spacing 34, and gap 37 over the waveguide 38, such as having a waveguide layer 40 and buried oxide layer 42 and a substrate layer 44. Light 46 is shown traversing the waveguide 38 and coupled through the vertical optical coupler 32, with its interaction with the waveguide to direct the light in direction 48.

[0042] In FIG. 3, operation of the vertical coupler is illustrated in example embodiment 50 with light transmission through waveguide 64 being blocked from vertical coupler 52 for vertical output 74, by an in-plane reflector 58. The vertical coupler 52 can be configured with the same parameters as described for FIG. 1 with regard to spaced art segments of grating material 54, spacing 56, and gap 57 over the waveguide 64. The waveguide 64 is illustrates by way of example and not limitation with a waveguide layer 66, buried oxide layer 68 and a substrate layer 70. In the figure, arrow 72a depicts light input to the waveguide, with arrow 72b depicting transmission light that cannot be coupled vertically in a single pass. Arrow 72c represents the reflected light of 72b through in-plane reflector 58. The large vertical arrow 74 represents the total vertically out-coupling light. The reflector 58 also comprises segments of grating material 60, spaces 62, and is positioned with a gap 63 separating it from waveguide 64. HCG parameters for reflector 58 differ from that of the vertical optical coupler to provide efficient and broadband reflection.

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[0043] The coupler design procedure is as follows. The first step is t determine the HCG period Λ. The goal is to couple a down-propagating plane wave, with the E-field polarized in y-direction into the fundamental TE mode of the Si waveguide (E-field in the same direction). It will be appreciated that an HCG can be considered as a (short) slab waveguide array supporting modes propagating in the z-direction

[0044] FIG. 4A and FIG. 4B depict mode characteristics of a high contrast grating utilized in the vertical optical coupler. In FIG. 4A, in-plane lateral mode profiles for the first three modes of propagation are seen. Due to the large index contrast, there exists a wide wavelength range where the HCG supports exactly two propagating modes, while the third and higher modes are evanescent in z and are bound to input and output surfaces of HCG (surface modes). These first two modes propagate in the z-direction with different propagation constants, β_1 and β_2. At the input and output planes, z = 0 and z = t, respectively, the two modes are reflected not only back to themselves, but also couple into each other's reflections, resulting in a mixing of the two modes. The propagation wave-numbers adjusted for the mode cross-coupling are denoted herein as β'_1 and β'_2. Most importantly, due to the sub-wavelength period, the two modes do not couple into any diffraction order other than the fundamental one, which is a surface normal propagating plane wave.

[0045] In FIG. 4B, the net field profile at the existing planes is seen having a periodic spatial variation equal to the HCG period. The high coupling can be anticipated when this periodicity is matched to the propagation constant of the Si/SiO_2 waveguide mode, denoted as β_x since it propagates in x-direction. The first step for the vertical coupler is therefore calculating the effective index η_{eff} of Si/SiO_2 waveguide, where η_{eff} is $\beta_x\lambda_0/2\pi$ and λ_0 is the free space wavelength. This leads to the determination of the period of HCG, $\Lambda = 2\pi/\beta_x = \lambda_0/\eta_{eff}$.

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[0046] Next, HCG thickness is determined by finding the condition w

and $\beta'_2 t$ are a multiple of 2π, which is the condition in which the two modes are in resonance, whereby the field inside the grating under this condition is accordingly enhanced.

[0047] FIG. 5 depicts HCG surface normal reflectivity, indicating that for a given λ_0 and Λ, there are multiple sets of t and η pairs that satisfy this condition.

[0048] FIG. 6 depicts the dispersion relationship of one such resonance mode, in which the four sets of dotted lines represent HCG resonance modes, while the solid lines represent coupled waveguide modes. The flat solid line and lower dotted line depict the mode without coupling. The other lines illustrate the use of an air gap (d) of 0.25 μm, 0.30 μm and 0.35 μm, respectively. Toward the middle of the graph the dotted line curves are seen in order of air gap spacing, with 0.35 μm seen as the lowest dotted line, and 0.25 μm as the uppermost dotted line. On the other hand, the Si waveguide mode propagating in the x direction can be represented by a straight horizontal line in the dispersion curve. By changing the gap between HCG and Si waveguide, d, the HCG resonance mode couples with the waveguide mode, causing the crossed dispersion lines to repel against each other. The stronger the coupling is, the wider the bandgap of the forbidden zone. At the center of the forbidden zone, there is no longer allowed real values for k_z, indicating the wave is forbidden to propagate in the vertical direction and all energy is transferred to in-plane propagation.

[0049] **2. Coupler Performance**

[0050] **2.1 Vertical to In-Plane Coupler**

[0051] At the wavelength of 1.55 μm for this example embodiment, the waveguide effective index is 2.13. The HCG perturbs the effective index of the waveguide underneath to 2.14. Based on the design principle described above, the following parameters were chosen: period Λ = 0.724 μm, HCG

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thickness t = 0.96 μm, duty cycle η = 0.61 and air gap thickness d μm.

[0052] FIG. 7A and FIG. 7B depict results of a finite difference time domain (FDTD) simulation performed to test the design. In FIG. 7A, the intensity distribution shows the coupling effect, in which it can be clearly seen that the field inside the waveguide under the HCG is enhanced and the surface normal incident light is coupled into the waveguide. In FIG. 7B, coupling efficiency is seen for each propagation direction as a function of wavelength. The highest coupling efficiency for this example is 46% and the coupling wavelength is 1.552 μm. Therefore, in the combination of both +x and –x directions, 92% of incident energy was coupled into the waveguide. The remaining 8% was leakage due to the limited HCG width. The 1 dB and 3dB coupling bandwidths were found to be 30 nm and 50 nm, respectfully, which is substantially wide and readily makes this device useful for WDM application. The bandwidth is determined by the band gap of the forbidden zone, which can be tuned by the spacing between the HCG and the waveguide, as was shown previously in regard to FIG. 6. Therefore, wider or narrower bandwidth can be achieved by tuning the air gap and the corresponding HCG dimension.

[0053] **2.2 Coupler from Symmetrical In-Plane Incidence to Vertical Output**

[0054] Based on reciprocity, it can be expected that the symmetrical light incidence from two sides of the waveguide can be coupled into the vertical direction with high efficiency as well, as shown in the schematic of FIG. 2.

[0055] FIG. 8A through FIG. 8D depict FDTD simulation results for coupling light from two sides of the waveguide into the vertical direction. The dimensions in this configuration are the same as the vertical to in-plane coupler. In this simulation, two mode matched light sources are positioned at the waveguide symmetrically to HCG. In FIG. 8A the field distribution is plotted in a log scale, while FIG. 8B shows the coupling efficiency with plots for –z leakage (bottom line) +x, -x leakage (trough-shaped curve), upward coupling (peaked curve), and the combination (summation). At the

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wavelength of 1.551 μm, the highest coupling efficiency is found to The 1 dB and 3 dB bandwidths are 38 nm and 70 nm, respectively.

[0056] 2.3 Coupler from Single Side In-Plane Incidence to Vertical Output

[0057] For the single side in-plane incidence case, previously described in FIG. 3, to prevent optical transmission passing through the waveguide, an in-plane reflector is integrated into the device. By changing the HCG thickness t with the other dimensions fixed as in the previous designs, a broad band high efficiency in-plane reflector can be designed.

[0058] FIG. 9A and FIG. 9B depict simulated waveguide field distribution and in-plane reflectivity, respectively. The field distribution of in-plane reflectivity in FIG. 9A is shown in a log scale, for a device with HCG thickness t at 0.495 μm, a period λ of 0.724 μm, and duty cycle η at 0.61. FIG. 9B depicts the reflectivity spectrum, with the highest reflectivity in this test being 97% with a bandwidth of 30 nm. It will be noted that by varying the HCG thickness in the simulation, the HCG expresses different behaviors.

[0059] FIG. 10A through FIG. 10C, respectively, depict that the light can be reflected backward in the –x direction shown in FIG. 10A, coupled upwardly in the +z direction shown in FIG. 10B, or transmitted through in the +x direction shown in FIG. 10C across a range of different HCG thicknesses, with these transformations observed with respect to grating period.

[0060] In the above example, the HCG coupler and in-plane reflector grating were selected with the same thickness, but having different periods and duty cycles. By increasing the duty cycle, the anti-crossing behavior seen in FIG. 5 can be shifted to smaller HCG thicknesses. In FIG. 5, sharp reflectivity changes indicate the resonance conditions of specific modes. At the center, two modes which are supposed to intersect with each other repel at the crossing point, and is referred to as the anti-crossing behavior. The coupler HCG of the example embodiment has a thickness of 0.495 μm, period 0.715 μm, and a duty cycle of 0.69.

[0061] FIG. 11A and FIG. 11B depict, respectively, coupling field distribution and the coupling efficiency spectrum for this configuration. The highest

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coupling efficiency observed in this example embodiment was 91.7% wavelength of 1.554 μm, with the 1 dB bandwidth at 70 nm.

[0062] **3. Applications**

[0063] **3.1. Integration of Vertical Coupler with Hollow Core Waveguides**

[0064] Notwithstanding the numerous beneficial configurations described in the preceding sections, the inventive vertical optical coupler also provides wide applicability in the context of hollow-core waveguides (HWs). It will be appreciated that a wide range of applications exist for these hollow-core waveguides (HWs), including applications in gas sensing and gas-based nonlinear optics. With the elimination of core material, the problems with nonlinearity, dispersion effects and scattering losses in traditional SiO_2, Si or III-V waveguides can be drastically reduced. Utilizing chip-scale HWs opens up a new range of on-chip applications, such as optical buffers, optical signal processors, and RF filtering. Although integrated HWs can achieve a low propagation loss for the straight session, there is usually a relatively large light leakage when the waveguide bends. At the bending region, the sidewall reflection reduces, and thus large radiation losses can arise, in particular with integrated HWs. The small footprint of integrated optics requires unavoidably tight packing of the waveguides and sharp turns. This would introduce high loss as the bending loss increases exponentially with the decrease of the radius of curvature. These losses have imposed significant limitations on the application of integrated HWs. Use of the inventive vertical coupler can solve this problem by bridging two adjacent HWs without the need of a sharp bend.

[0065] FIG. 12 through FIG. 14 illustrate example embodiments utilizing vertical couplers with waveguides. The hollow core waveguides can be of any desired types, such as metal HWs, distributed Bragg reflection type HWs, anti-resonant HWs, HCG HWs, or other form of HW. These examples illustrate coupling so that the light is turned a full 180 degrees, although the teachings are applicable to turning light through other angular displacements. Because the coupler can be designed to have coupling with any angle, the stripe

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waveguide 98 and HCG HWs 92 and 94 can be configured to any re angle and work with the corresponding couplers.

[0066] In the embodiment 90 of FIG. 12, two HWs are seen 92, 94 having exterior 102 surrounding an interior hollow light guide region 104. At the end of each of these HWs are vertical couplers 96a, 96b, in a butt-coupling arrangement, that are in turn interconnected with each other by a strip waveguide 98. An HCG 100a, 100b are seen in each vertical coupler upon which light has normal incidence from HWs 92, 94 to the vertical coupler. Through the vertical coupler, light can be transformed from the HWs to the stripe waveguide. The propagation direction of the light thus changes 90 degrees at each vertical coupler. The first vertical coupler 96a directs light from a first waveguide 92 into a stripe waveguide 98, while a second vertical coupler 96b transforms the light back onto the adjacent HW 94. In this case, a virtually sharp turn is made without any sharp bends. With the high efficiency of the vertical coupler, the loss for the whole transformation can be small, on the order of 10% or less.

[0067] FIG 13 illustrates an alternative HW light bending technique to the above, utilizing the vertical coupler configured in a side-coupling embodiment 110. A first waveguide 112 and second waveguide 114 are shown having an exterior 102 with hollow waveguide interior 104. The grating 118a, 118b of the vertical couplers 116a, 116b are placed on top of the waveguides 112, 114 with a stripe waveguide 120 connecting the vertical couplers. This and other embodiments of the invention may also be equally realized by replacing the stripe waveguide with other forms of waveguides, such as HCG waveguide, or hollow waveguides. With a proper design, light can be coupled upwards to the stripe waveguide, and then downwards to the adjacent HW. It should be appreciated that this configuration may be particularly well-suited to simplified fabrication processing.

[0068] FIG. 14 illustrates an embodiment 130 in which the vertical coupler is utilized with HCG HWs 132, 134, to which it may be even more beneficially coupled. It will be appreciated that HCG HWs represent another class of

hollow-core waveguide, with the HCG configured as high reflection n and light is thus confined between opposing layers 136, 137 of HCGs. This form of waveguide has an extremely low propagation loss, and lateral confinement can be achieved by choosing different periods and duty cycles for the core and cladding region. A first vertical coupler 138a with its HCG 140a is shown integrated with first HCG HW 132, with light coupled through a stripe waveguide 142 to a second vertical coupler 138b, with its HCG 140b, coupled to a second HCG waveguide 134. It will be appreciated that the HCGs at the end of the waveguide can be designed as a vertical coupler to transform the light upwards to the stripe waveguide, or downwards from the stripe waveguide. The transition between the waveguide and the coupler can be designed to be smooth, and this ensures a minimum loss. It would appear that this arrangement can provide a most beneficial combination to replace traditional lossy light bending arrangements.

[0069] **3.2. WDM Multiplexer and Demultiplexer**

[0070] FIG. 15 and FIG. 16 illustrate utilizing the inventive HCG vertical coupler for multiplexing and demultiplexing in a WDM system. In the multiplexer embodiment 150 of FIG. 15, outputs from a plurality of VCSELs 152a, 152b and 152c with different wavelengths (λ_1, λ_2, λ_3) are coupled through the inventive vertical optical coupling into a waveguide 162. It will be appreciated that the multiplexor and the demultiplexer of these figures are shown having three inputs / outputs, for the sake of simplicity of illustration, however, the technique can be utilized with any desired number of inputs / outputs, respectively. It should also be appreciated that each vertical coupler is configured for its particular working wavelength, and that by optimizing HCG parameters, the crosstalk arising between different wavelengths can be essentially eliminated.

[0071] It will be seen from the figure that inputs 152a, 152b, 152c are directed through gap 154a, 154b, 154c to an HCG 156a, 156b, 156c, containing segments 158a, 158b, and 158c along with spaces 159a, 159b, 159c. Vertical coupling between HCG 156a, 156b, 156c is through gap 160a, 160b, 160c

with a waveguide 162 having a waveguide layer 164, a buried oxide and a substrate layer 168. It should be appreciated that waveguide 162, and other waveguides within the optical coupler, may comprise any desired forms of waveguides. It can be seen from the figure that the light received at λ_1 is dispersed in both directions 170a of the waveguide 162, while similarly light received at λ_2 is dispersed in both directions 170b, and light received at λ_3 is also dispersed in both directions 170c.

[0072] FIG. 16 illustrates a demultiplexer embodiment 190 configured for demultiplexing a plurality of wavelengths from a common waveguide. It will be noted that because of the reciprocity principle, the demultiplexer can have the same dimensions as the multiplexer described in FIG. 15. Based on the simulation results, the phase difference of the input light at each side of the coupler is optimally an integer multiple of 2π, which can be readily satisfied in response to tuning the distance between the couplers. By way of example and not limitation, a set of typical dimensions for multiplexing of a 1.55 μm and 1.3 μm wavelength input. For a 1.55 μm coupler, HCG thickness is 0.7 μm, duty cycle η is 0.6, period λ is 0.744 μm; while for a 1.3 μm coupler, thickness is 0.84 μm, duty cycle η is 0.635, period λ is 0.581 μm.

[0073] In the demultiplexer embodiment 190, wavelengths 206a, 206b, and 206c of light along waveguide 198 having a waveguide layer 200, an insulating layer 202 and a substrate layer 204, are vertically coupled to HCG 192a, 192b, 192c having segments of grating material 194a, 194b, 194c and spaces 195a, 195b, 195c, over gap 196a, 196b, 196c, whereby in response to vertical optical coupling operation the three wavelengths (λ_1, λ_2, λ_3) are output vertically. It will be noted that the HCG elements are configured to be frequency selective and thus perform demultiplexing of signals from the waveguide.

[0074] It should be appreciated that the waveguide can be coupled to any desired optical elements, such as optical fiber ports or other optical devices without limitation. In particular, in the case of a multiplexer, the various

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wavelengths coupled into the waveguide can be passed to an optica wherein they are coupled for communication over an optical fiber.

[0075] 3.3. Vertical to Single Side Coupler

[0076] The phases of HCG modes are significantly influenced by high index material width. By chirping the grating, that is by changing the periodicity of the grating, the coupling from surface normal incidence can have a directional preference to the in-plane waveguide.

[0077] FIG. 17 illustrates a vertical to single side coupling embodiment 210 utilizing a chirped grating. Light can be directed from a laser light source 212, depicted as VCSEL, through gap 218 to an HCG 214, having segments of grating material 216 of different widths and / or spacing 217, and coupled through gap 220 to a waveguide 222 having a waveguide layer 224, an insulating layer 226 and a substrate layer 228. It can be seen in the figure that the light 230 from the light source, VCSEL 212, is shown traversing the waveguide in a single direction 230 in response to the chirp of the HCG whose grating bar width (s) and gap width (a) are chirped in the x direction to give a phase preference in that direction, thus providing a selection of coupling direction.

[0078] 3.4. Parallel Waveguide Coupler

[0079] FIG. 18 illustrates an embodiment 250 of utilizing an HCG coupler to couple the light wave between two parallel waveguides. The HCG coupler 256 is located between two parallel waveguides 252, 264. Light from the input waveguide 252 along a first direction 254 is coupled through HCG 256 through gaps 260, 262 to waveguide 264 wherefrom light continues traveling along in a second direction 266 parallel to said first direction 254.

[0080] 3.5. Reflector and Coupler for Surface-Emitting Lasers with In-Plane Waveguide and Active Region

[0081] An HCG vertical coupler and reflector can also be utilized in fabricating in-plane lasers emitting in the surface-normal direction. This is particularly useful for devices where mirrors are hard to construct (e.g., such as due to lack of suitable material or processing techniques) and / or surface emission is

desirable for two-dimensional integration and on-wafer testing. One is quantum cascade lasers (QCL) and a second example may be GaN or ZnO2 based devices.

[0082] FIG. 19 illustrates an example surface-emitting QCL structure embodiment 270. HCG reflectors are shown 272a, 272c, having segments of grating material 274a, 274c, and spaces 276a, 276c, and located at two ends of waveguide 280 comprising a waveguide layer 282, insulating layer 284 and substrate layer 286, act as cavity mirrors with spacing 278a, 278c over waveguide 280. An HCG vertical coupler 272b having segments of grating material 274b and spaces 276b disposed over gap 278b from waveguide 280, is upon the active waveguide region to provide the vertical emitting 289 from the combination of light waves 288a, 288b. Similar to the structure in previous sections, the reflector and coupler can have identical thickness. In this case, a monolayer HCG can solve both vertical emitting and cavity reflection issues.

[0083] FIG. 20 illustrates the utilization of the HCG reflector within a GaN laser, exemplified by a GaN laser embodiment 290. GaN material system based laser diodes are of particular interest in recent times because of their short wavelength outputs. However, the etching of GaN facets always poses a difficulty. The implementation of the HCG reflector in a GaN laser structure provide a beneficial alternative to fabrication of the facets. The GaN laser is exemplified as having an n-electrode 292 beneath substrate 294, such as of sapphire or GaN material. Over the substrate is an n-GaN layer 296, an n-AlGaN layer 298, another n-GaN layer 300, an In-GaN layer 302, a quantum structure layer 304, such as comprising a multiple quantum well (MQW) layer, of InGaN/AlGaN within an active region, another In-GaN layer 306, a p-AlGaN layer 308 and a p-GaN layer 310. It should be appreciated that the active region may comprise quantum wells, quantum wires, quantum dots, either separately or in combination, or even a bulk region.

[0084] At the upper portion of the device there is stopper layers (SLs) 312 of AlGaN/p-GaN. Shoulders of SiO_2 in layer 314 flank a vertical portion of layer 312 of AlGaN/p-GaN, which is capped with a layer of p-GaN 316. An HCG

318 is integrated on the flanks of the vertical portions of layer 312 wi segments 320 within a p-electrode layer 322. It will be appreciated that HCGs 318 are sitting at two edges of the laser diode acting as the reflector of the GaN laser cavity, while SiO_2 layer 314 is the low index gap between HCG and the semiconductor in the cavity. The HCG reflectors 318 are incorporated within the laser heterostructure to confine the light mode in the active region between the two HCG reflectors, so that device edges do not require special treatments, such as etching and reflective coating. If surface-normal emission is desirable, a vertical output coupler can also be made on the laser, similar to that of FIG. 18.

[0085] 3.6. LED Coupling

[0086] FIG. 21 illustrates an example embodiment 330 of a GaN light emitting diode incorporating an HCG vertical coupler on the active region. The light extraction efficiency for GaN based light emitting diodes has been an ongoing obstacle to the advance of LED efficiency, which without special treatment is only around 4%. One method to improving this light extraction efficiency is to roughen the emitting surface. However, utilizing the present invention optical coupling light extraction efficiency is dramatically increased.

[0087] The example LED embodiment 330 is shown fabricated with a metal base 332, upon which is an n-electrode layer 334, a layer of n-GaN 336, above which is an active region of InGaN 338 followed by a layer of p-GaN 340, a layer of SiO_2 342, above which is an HCG layer 344 having grating segments 346 and spaces 347, and a p-electrode 348 disposed centrally. It is preferable that the central p-electrode be of a heavily doped material to inject the current. It goes through SiO_2 layer 342 and connect to p-GaN layer 340. It should also be noted that the shape depicted in the top plane view of FIG. 21 is not necessarily constricted, but is dependent on how the LED is designed. Typically, the shape of the p-electrode is as a circle or a ring. It will be appreciated that the above describes an improvement to conventional GaN diodes, whose operating principles need not be discussed in detail as they are well known in the art.

[0088] **3.7. Solar Cells**

[0089] FIG. 22 illustrates an example solar cell embodiment 350, incorporating an HCG vertical coupler 352 with respect to a solar cell instead of a waveguide. The HCG 352 comprises segments of grating material 354 and spaces 355, positioned with a gap 356 over a solar cell 358 acting as a light collector, and shown comprising a p-n junction layers 360, 362 on a substrate 364. The incorporation of the HCG vertical coupler increases solar cell efficiency by reducing light reflection, because of the resonant nature of HCG in this configuration the light can be confined in the active region and therefore help to enhance efficiency

[0090] **3.9. Use of Different Materials**

[0091] The material requirement for an HCG coupler and reflector are readily achieved using a wide range of materials, as any material combinations can be utilized in which the refractive index of the grating materials have a high contrast with refractive index of the surrounding materials. The larger the contrast, the better the performance (bandwidth, coupling efficiency, and so forth) of the HCG coupler and reflector. Some possible materials include Si, Ge, GaAs, InAs, AlSb, InP, AlGaInP, InGaAs, AlGaAs, AlAs, CaSe, ZnSe, GaSb, AlSb, GaN, and similar dielectric materials.

[0092] From the discussion above it will be appreciated that the invention can be embodied in various ways, including the following:

[0093] 1. An apparatus for optical coupling, comprising: a sub-wavelength high contrast grating (HCG) having a plurality of separate spaced apart segments of material with a gap between adjacent segments; and an optical waveguide proximally coupled through a selected gap to said sub-wavelength high contrast grating (HCG); wherein light is coupled between normal incidence on said sub-wavelength high contrast grating (HCG) and transmission through said optical waveguide.

[0094] 2. The embodiment of claim 1, wherein said spaced apart segments of material of said high contrast grating (HCG) comprise a high refractive index material surrounded by low index material.

[0095] 3. The embodiment of claim 1, wherein the index of refractior high index material and the index of refraction of said low index material have a differential that is greater than one unit.

[0096] 4. The embodiment of claim 1, wherein said spaced apart segments of material comprising said high contrast grating have a width (s), thickness (t), a spacing (a) between segments, and a period Λ.

[0097] 5. The embodiment of claim 1, wherein said optical waveguide comprises a slab waveguide, HCG, or hollow-core waveguides (HW).

[0098] 6. The embodiment of claim 1, wherein said sub-wavelength high contrast grating (HCG) can be chirped to support asymmetrical waveguide transmission.

[0099] 7. The embodiment of claim 1, further comprising an in-plane reflector for preventing transmission along selected directions of angular displacement of said light.

[00100] 8. The embodiment of claim 1, wherein said optical coupler comprises a multiplexer or demultiplexer for coupling, through an angular displacement, a number of wavelengths of light between a normal incident direction to said HCG and transmission through said waveguide.

[00101] 9. The embodiment of claim 1, wherein said apparatus comprises materials selected from the group of materials consisting of Si, Ge, GaAs, InAs, InAlGaAs, AlAs, AlSb, GaSb, GaAlSb, InP, AlGaInP, InGaAlAs, CdSe, ZnSe, CdSSe, InAlGaN, InN, AlN, GaN, ZnO2, and SiN.

[00102] 10. The embodiment of claim 1, wherein said optical coupling is integrated within the surface of a light emitting diode to transfer light reaching the waveguide along the surface to a vertical output.

[00103] 11. The embodiment of claim 1, wherein said optical coupling is integrated within the surface of a solar cell to transfer light impinging on the surface into the p-n junction taking the place of a waveguide along said surface.

[00104] 12. An apparatus for optical coupling, comprising: a sub-wavelength high contrast grating (HCG) having a plurality of separate spaced apart

segments of material with a gap between adjacent segments; where spaced apart segments of material comprise a high refractive index material surrounded by low index material;wherein the index of refraction of said high index material and the index of refraction of said low index material have a differential that is greater than one unit; and an optical waveguide proximally coupled through a selected gap to said sub-wavelength high contrast grating (HCG); wherein light is coupled between normal incidence on said sub-wavelength high contrast grating (HCG) and transmission through said optical waveguide

[00105] 13. The embodiment of claim 12, wherein said waveguide comprises a slab waveguide, HCG, or hollow-core waveguides (HW).

[00106] 14. The embodiment of claim 12, wherein said sub-wavelength high contrast grating (HCG) of said optical coupler can be chirped to support asymmetrical waveguide transmission.

[00107] 15. The embodiment of claim 12, further comprising an in-plane reflector for preventing transmission along selected directions of angular displacement of said light.

[00108] 16. The embodiment of claim 12, wherein said apparatus comprises materials selected from the group of materials consisting of Si, Ge, GaAs, InAs, InAlGaAs, AlAs, AlSb, GaSb, GaAlSb, InP, AlGaInP, InGaAlAs, CdSe, ZnSe, CdSSe, InAlGaN, InN, AlN, GaN, ZnO2, and SiN.

[00109] 17. An apparatus for multiplexing or demultiplexing optical signals, comprising: a plurality of sub-wavelength high contrast gratings (HCGs), each having a plurality of separate spaced apart segments of material with a gap between adjacent segments; and an optical waveguide proximally coupled through a selected gap to said plurality of sub-wavelength high contrast gratings (HCGs); wherein light received by each of said sub-wavelength high contrast gratings (HCGs) is multiplexed onto said optical waveguide; and wherein light received by said optical waveguide is demultiplexed through said plurality of sub-wavelength high contrast gratings (HCGs) which contain sub-wavelength high contrast gratings (HCGs) that are adapted to pass different

wavelengths of said light.

[00110] 18. A surface-emitting quantum cascade laser apparatus, comprising: an active region having quantum wells; a reflector on either side of said active region; and at least two reflective sub-wavelength high contrast gratings (HCGs) near an output the surface-emitting laser to confine the light mode in an active region of the laser between two HCG reflectors.

[00111] 19. A light emitting diode apparatus, comprising: an n-electrode region; a p-electrode region; an active region disposed between said n-electrode region and said p-electrode region; and an optical coupler disposed on an output of said light emitting diode and comprising a waveguide layer for collecting light in a horizontal plane and coupled with a sub-wavelength high-contrast grating for redirecting collected light for output in a vertical direction.

[00112] 20. A solar cell apparatus, comprising: a sub-wavelength high contrast grating (HCG) having a plurality of separate spaced apart segments of material; and a solar cell having layers of a p-n junction upon which light from said HCG is directed and converted to electrical energy.

[00113] Although the description above contains many details, these should not be construed as limiting the scope of the invention but as merely providing illustrations of some of the presently preferred embodiments of this invention. Therefore, it will be appreciated that the scope of the present invention fully encompasses other embodiments which may become obvious to those skilled in the art, and that the scope of the present invention is accordingly to be limited by nothing other than the appended claims, in which reference to an element in the singular is not intended to mean "one and only one" unless explicitly so stated, but rather "one or more." All structural, chemical, and functional equivalents to the elements of the above-described preferred embodiment that are known to those of ordinary skill in the art are expressly incorporated herein by reference and are intended to be encompassed by the present claims. Moreover, it is not necessary for a device or method to address each and every problem sought to be solved by the present invention, for it to be encompassed by the present claims. Furthermore, no element,

component, or method step in the present disclosure is intended to b dedicated to the public regardless of whether the element, component, or method step is explicitly recited in the claims. No claim element herein is to be construed under the provisions of 35 U.S.C. 112, sixth paragraph, unless the element is expressly recited using the phrase "means for."

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CLAIMS

What is claimed is:

1. An apparatus for optical coupling, comprising:

a sub-wavelength high contrast grating (HCG) having a plurality of separate spaced apart segments of material with a gap between adjacent segments; and

an optical waveguide proximally coupled through a selected gap to said sub-wavelength high contrast grating (HCG);

wherein light is coupled between normal incidence on said sub-wavelength high contrast grating (HCG) and transmission through said optical waveguide.

2. The apparatus recited in claim 1, wherein said spaced apart segments of material of said high contrast grating (HCG) comprise a high refractive index material surrounded by low index material.

3. The apparatus recited in claim 1, wherein the index of refraction of said high index material and the index of refraction of said low index material have a differential that is greater than one unit.

4. The apparatus recited in claim 1, wherein said spaced apart segments of material comprising said high contrast grating have a width (s), thickness (t), a spacing (a) between segments, and a period Λ.

5. The apparatus recited in claim 1, wherein said optical waveguide comprises a slab waveguide, HCG, or hollow-core waveguides (HW).

6. The apparatus recited in claim 1, wherein said sub-wavelength high contrast grating (HCG) can be chirped to support asymmetrical waveguide transmission.

7. The apparatus recited in claim 1, further comprising an in-plar reflector for preventing transmission along selected directions of angular displacement of said light.

8. The apparatus recited in claim 1, wherein said optical coupler comprises a multiplexer or demultiplexer for coupling, through an angular displacement, a number of wavelengths of light between a normal incident direction to said HCG and transmission through said waveguide.

9. The apparatus recited in claim 1, wherein said apparatus comprises materials selected from the group of materials consisting of Si, Ge, GaAs, InAs, InAlGaAs, AlAs, AlSb, GaSb, GaAlSb, InP, AlGaInP, InGaAlAs, CdSe, ZnSe, CdSSe, InAlGaN, InN, AlN, GaN, ZnO2, and SiN.

10. The apparatus recited in claim 1, wherein said optical coupling is integrated within the surface of a light emitting diode to transfer light reaching the waveguide along the surface to a vertical output.

11. The apparatus recited in claim 1, wherein said optical coupling is integrated within the surface of a solar cell to transfer light impinging on the surface into the p-n junction taking the place of a waveguide along said surface.

12. An apparatus for optical coupling, comprising:

a sub-wavelength high contrast grating (HCG) having a plurality of separate spaced apart segments of material with a gap between adjacent segments;

wherein said spaced apart segments of material comprise a high refractive index material surrounded by low index material;

wherein the index of refraction of said high index material and the index of refraction of said low index material have a differential that is greater than one unit; and

an optical waveguide proximally coupled through a selected gap to said sub-

wavelength high contrast grating (HCG);

wherein light is coupled between normal incidence on said sub-wavelength high contrast grating (HCG) and transmission through said optical waveguide

13. The apparatus recited in claim 12, wherein said waveguide comprises a slab waveguide, HCG, or hollow-core waveguides (HW).

14. The apparatus recited in claim 12, wherein said sub-wavelength high contrast grating (HCG) of said optical coupler can be chirped to support asymmetrical waveguide transmission.

15. The apparatus recited in claim 12, further comprising an in-plane reflector for preventing transmission along selected directions of angular displacement of said light.

16. The apparatus recited in claim 12, wherein said apparatus comprises materials selected from the group of materials consisting of Si, Ge, GaAs, InAs, InAlGaAs, AlAs, AlSb, GaSb, GaAlSb, InP, AlGaInP, InGaAlAs, CdSe, ZnSe, CdSSe, InAlGaN, InN, AlN, GaN, ZnO2, and SiN.

17. An apparatus for multiplexing or demultiplexing optical signals, comprising:

a plurality of sub-wavelength high contrast gratings (HCGs), each having a plurality of separate spaced apart segments of material with a gap between adjacent segments; and

an optical waveguide proximally coupled through a selected gap to said plurality of sub-wavelength high contrast gratings (HCGs);

wherein light received by each of said sub-wavelength high contrast gratings (HCGs) is multiplexed onto said optical waveguide; and

wherein light received by said optical waveguide is demultiplexed through said plurality of sub-wavelength high contrast gratings (HCGs) which contain sub-

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wavelength high contrast gratings (HCGs) that are adapted to pass differen wavelengths of said light.

18. A surface-emitting quantum cascade laser apparatus, comprising:

an active region having quantum wells;

a reflector on either side of said active region; and

at least two reflective sub-wavelength high contrast gratings (HCGs) near an output the surface-emitting laser to confine the light mode in an active region of the laser between two HCG reflectors.

19. A light emitting diode apparatus, comprising:

an n-electrode region;

a p-electrode region;

an active region disposed between said n-electrode region and said p-electrode region; and

an optical coupler disposed on an output of said light emitting diode and comprising a waveguide layer for collecting light in a horizontal plane and coupled with a sub-wavelength high-contrast grating for redirecting collected light for output in a vertical direction.

20. A solar cell apparatus, comprising:

a sub-wavelength high contrast grating (HCG) having a plurality of separate spaced apart segments of material; and

a solar cell having layers of a p-n junction upon which light from said HCG is directed and converted to electrical energy.

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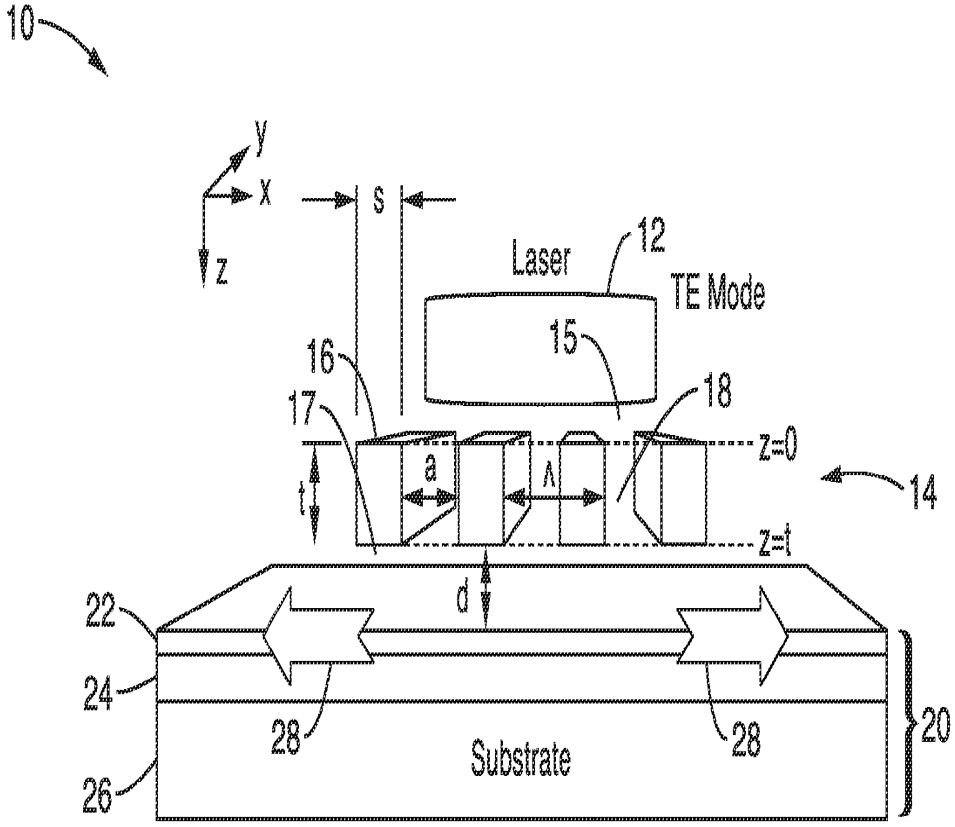

10
y
x
z
s
Laser
12
TE Mode
15
16
17
18
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a
Λ
t
z=t
d
22
24
26
28
28
Substrate
20

FIG. 1

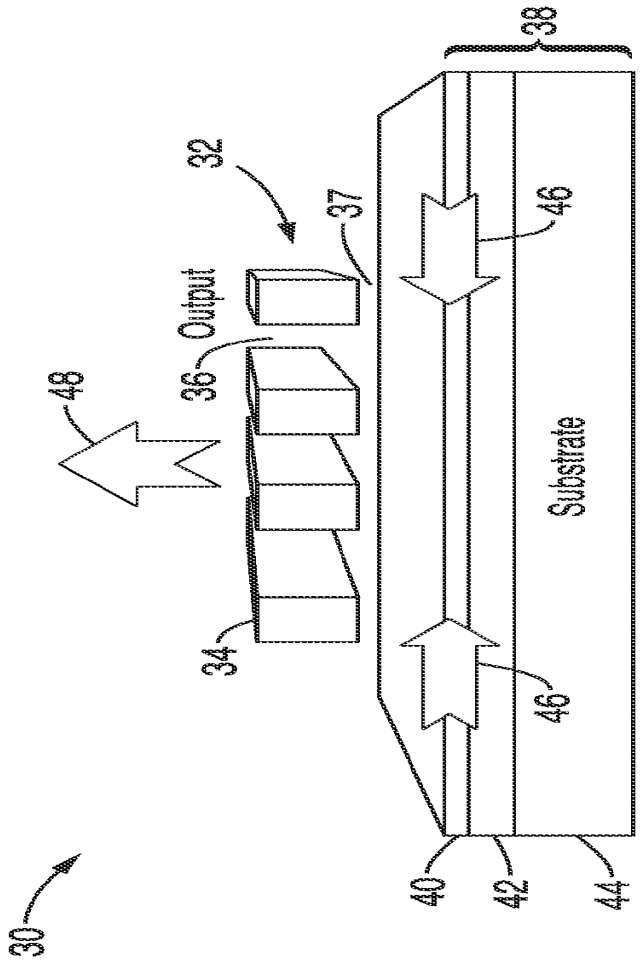


FIG. 2

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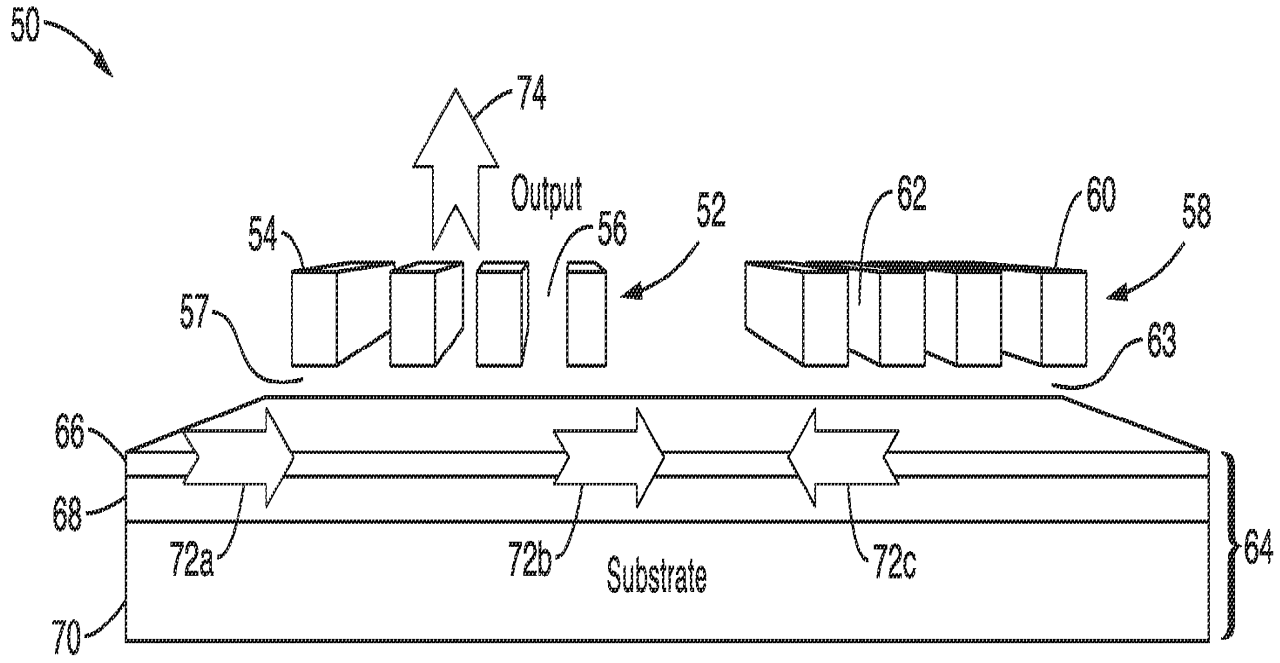

50
74
Output
54
56
52
62
60
58
57
63
66
68
72a
72b
Substrate
72c
64
70

FIG. 3

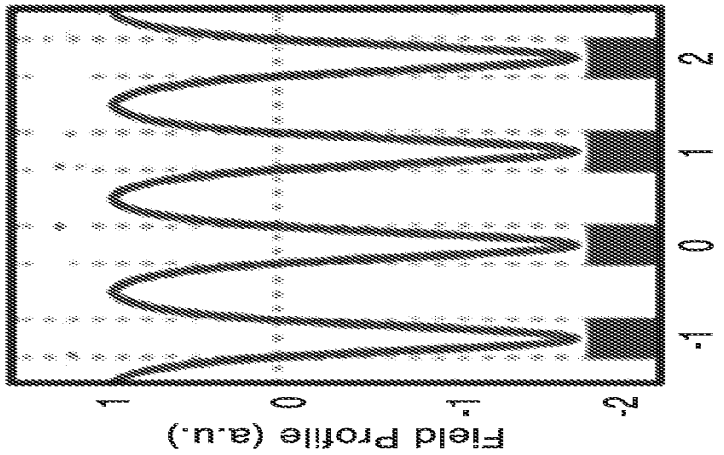


FIG. 4B

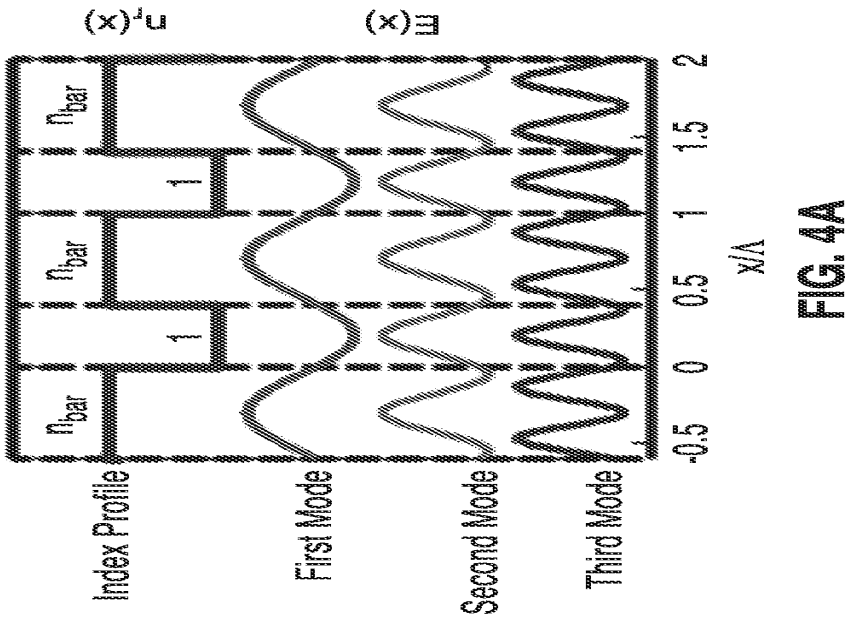


FIG. 4A

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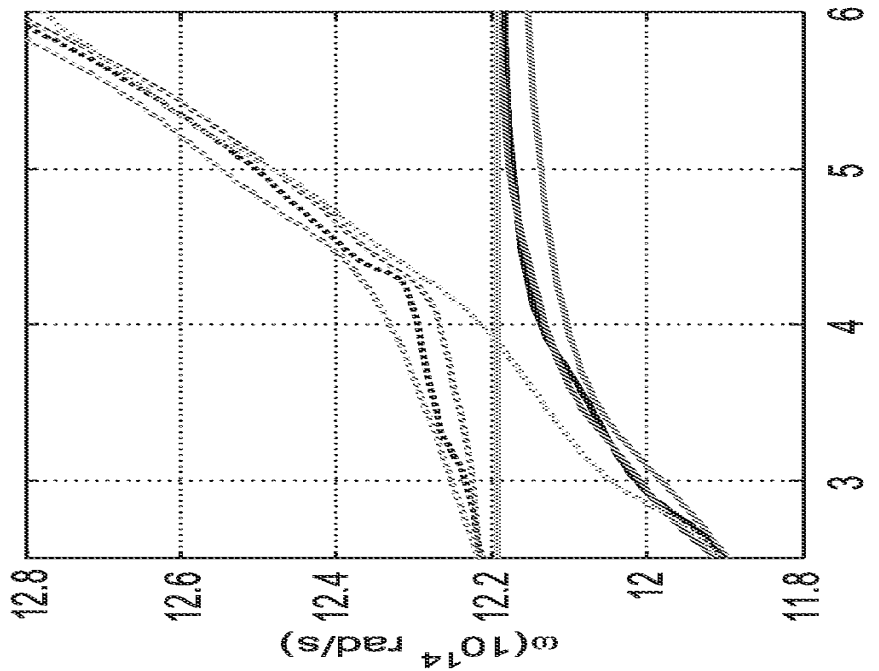


FIG. 6

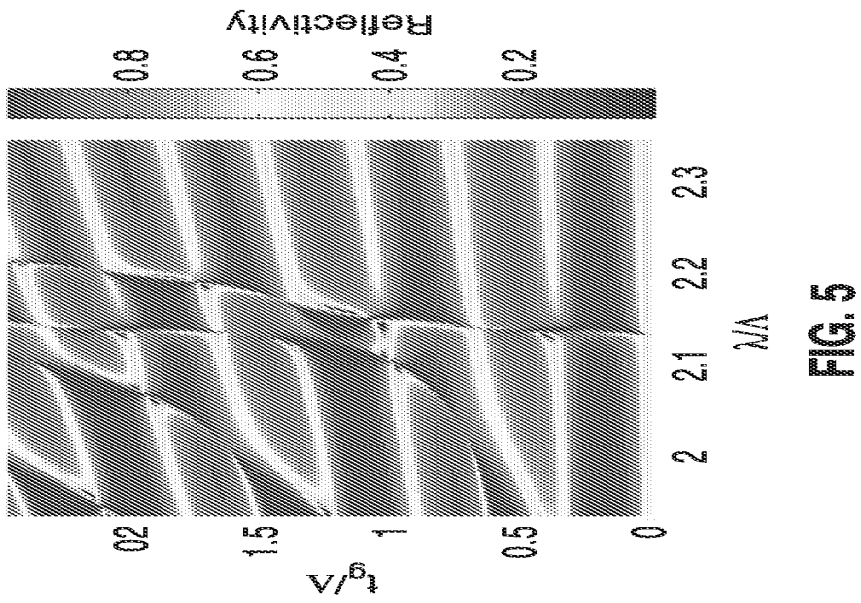


FIG. 5

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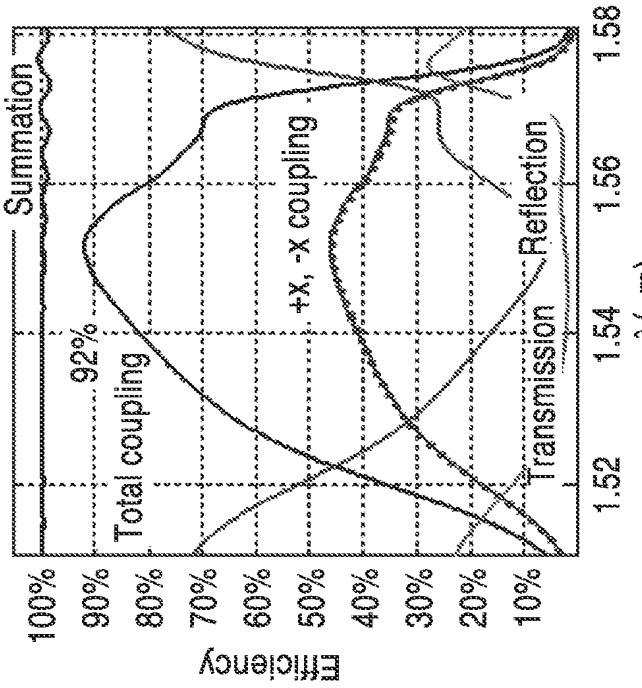

Summation
92%
Total coupling
+x, -x coupling
Reflection
Transmission
Efficiency
100%
90%
80%
70%
60%
50%
40%
30%
20%
10%
1.52
1.54
1.56
1.58
λ(μm)

FIG. 7B

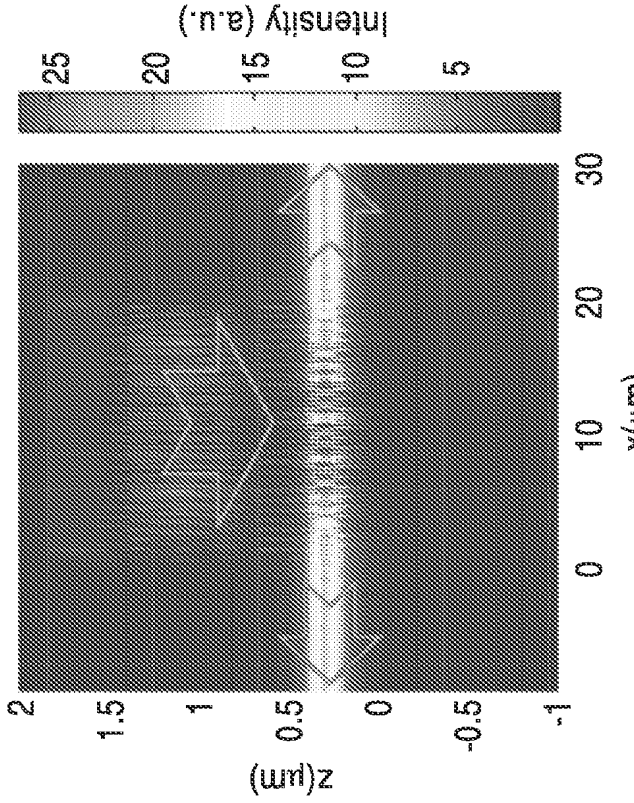

Intensity (a.u.)
25
20
15
10
5
z(μm)
2
1.5
1
0.5
0
-0.5
-1
0
10
20
30
x(μm)

FIG. 7A

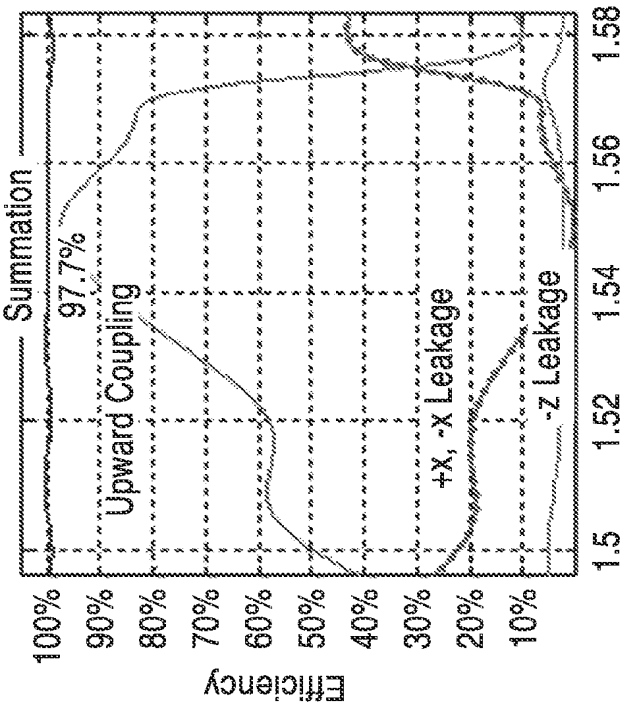

Summation
97.7%
Upward Coupling
+x, -x Leakage
-z Leakage
Efficiency
100%
90%
80%
70%
60%
50%
40%
30%
20%
10%
1.5
1.52
1.54
1.56
1.58
λ(μm)

FIG. 8B

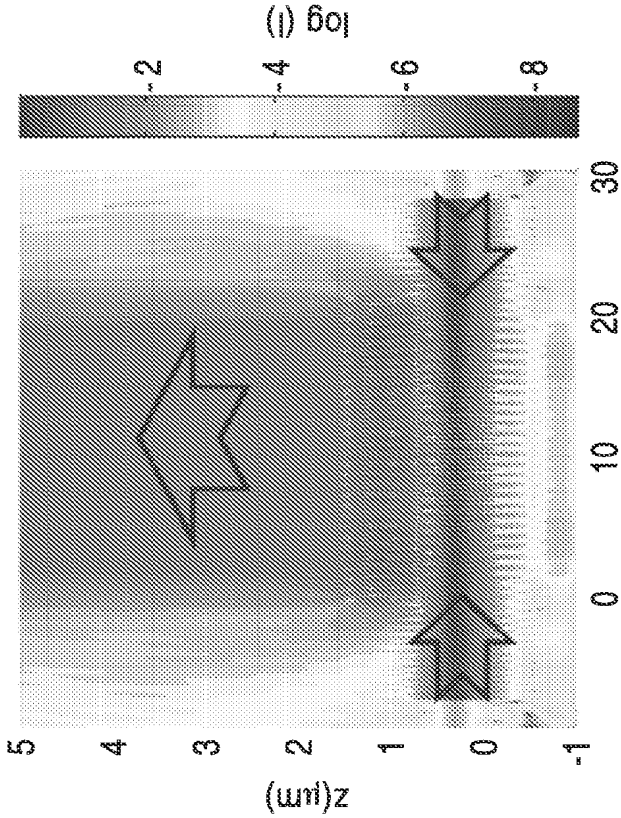

log (I)
-2
-4
-6
-8
z(μm)
5
4
3
2
1
0
-1
0
10
20
30
x(μm)

FIG. 8A

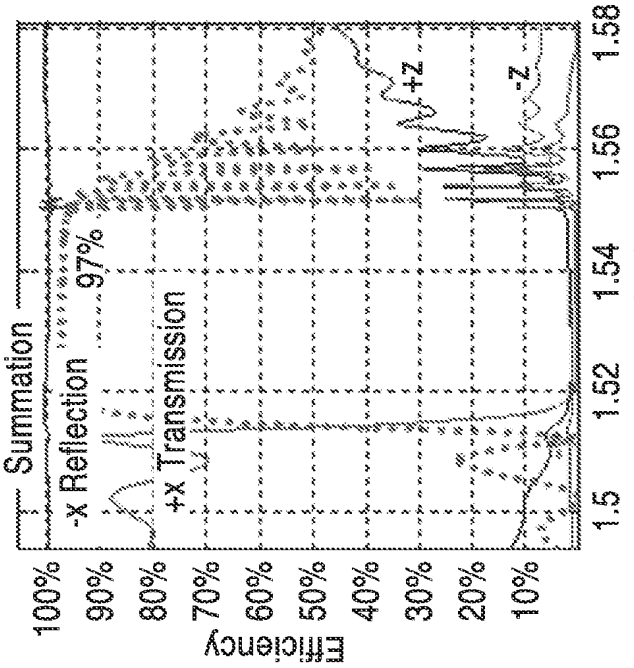

Summation
-x Reflection
97%
+x Transmission
+z
-z
Efficiency
100%
90%
80%
70%
60%
50%
40%
30%
20%
10%
1.5
1.52
1.54
1.56
1.58
λ(μm)

FIG. 9B

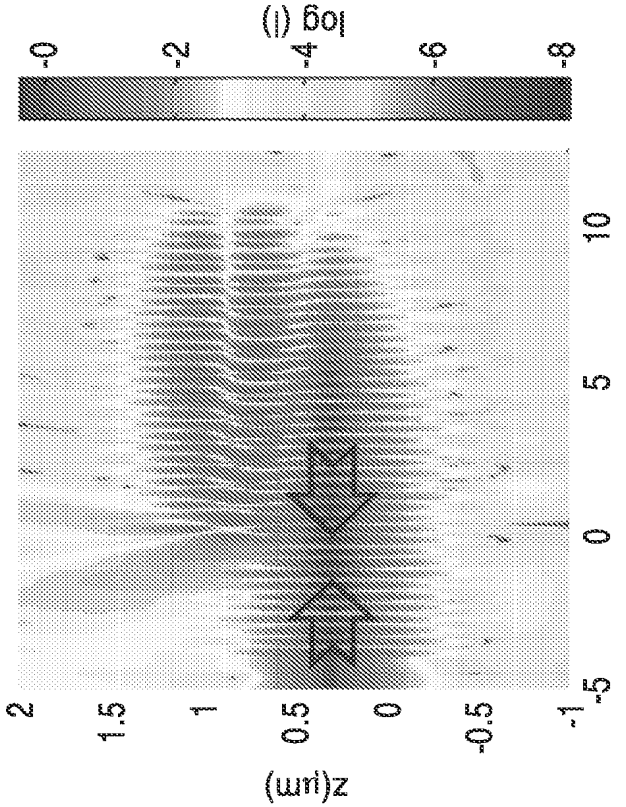

log (I)
-0
-2
-4
-6
-8
z(μm)
2
1.5
1
0.5
0
-0.5
-1
-5
0
5
10
x(μm)

FIG. 9A

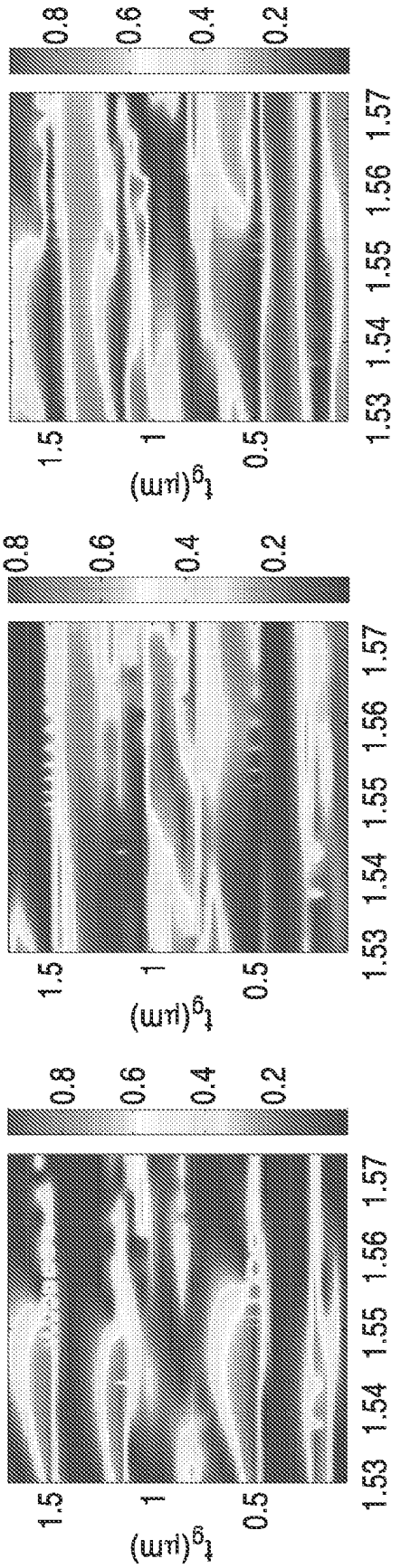


FIG. 10A

FIG. 10B

FIG. 10C

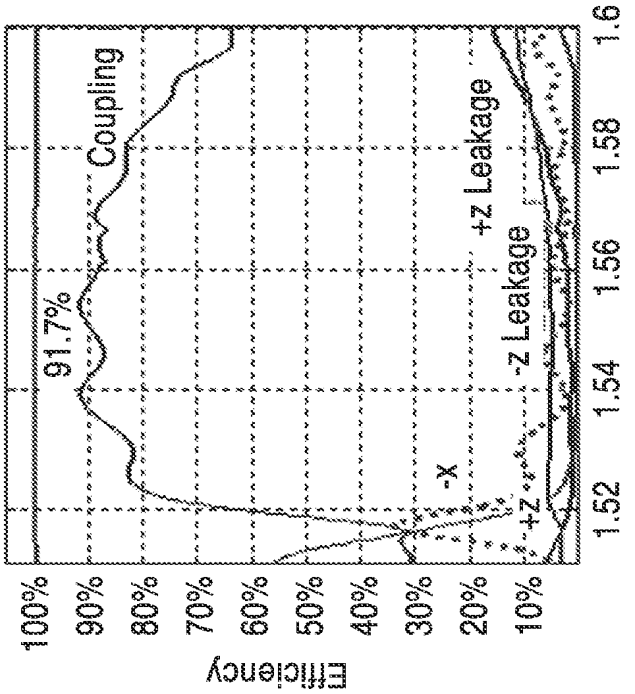


FIG. 11B

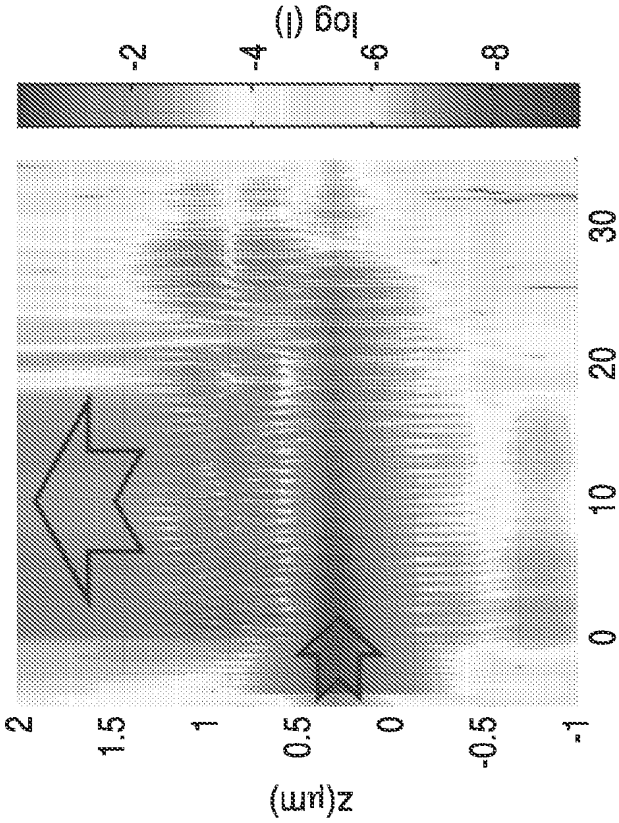


FIG. 11A

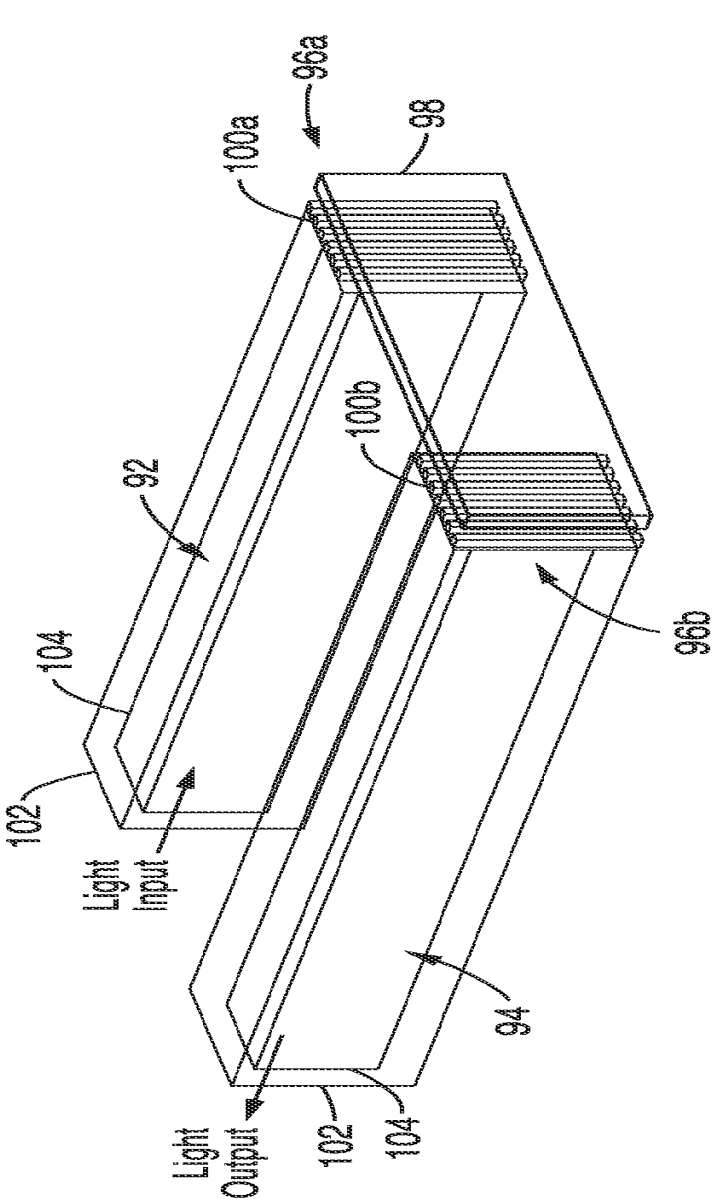


FIG. 12

Samsung Exhibit 1003, Page 636 of 1137

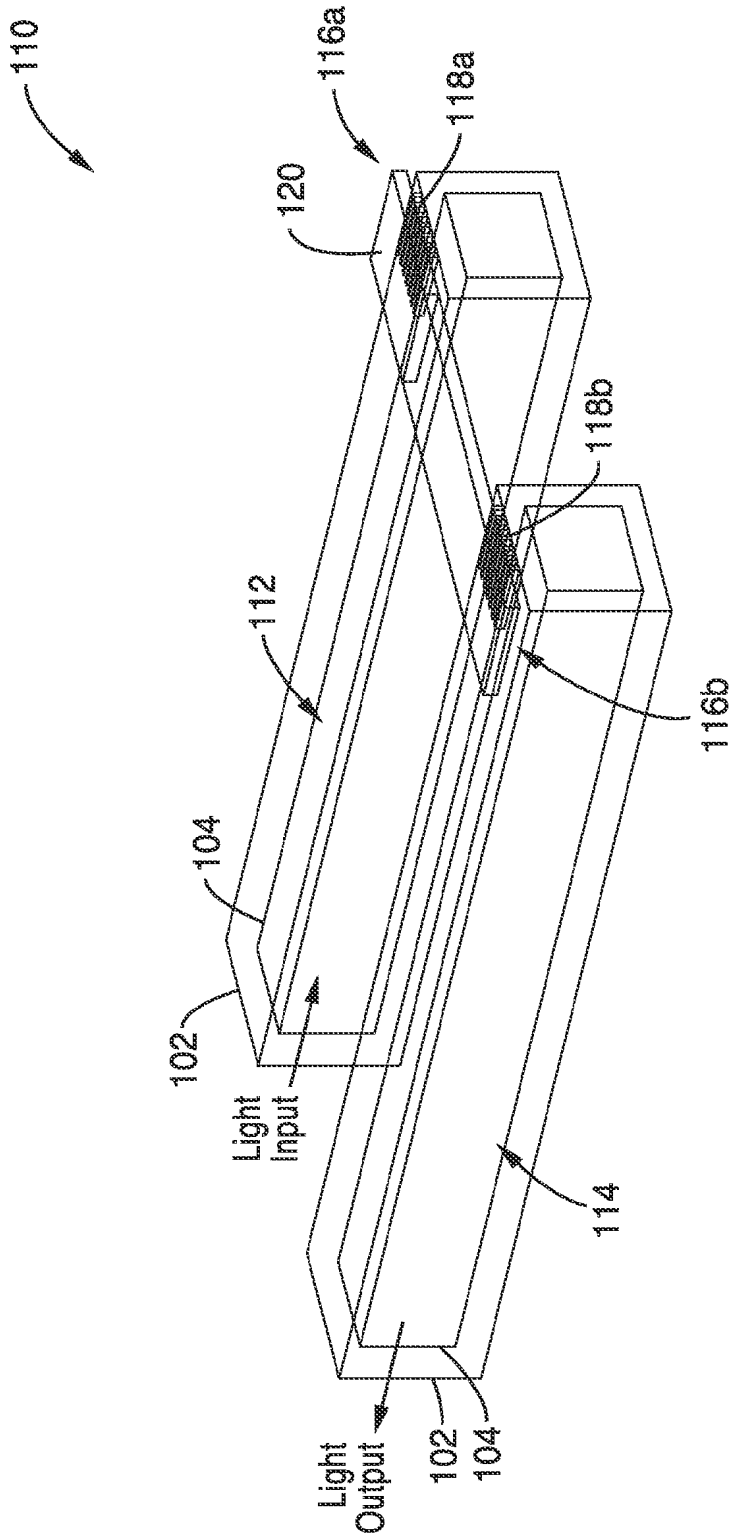

110
116a
118a
120
118b
112
116b
104
102
Light Input
114
Light Output
102
104

FIG.13

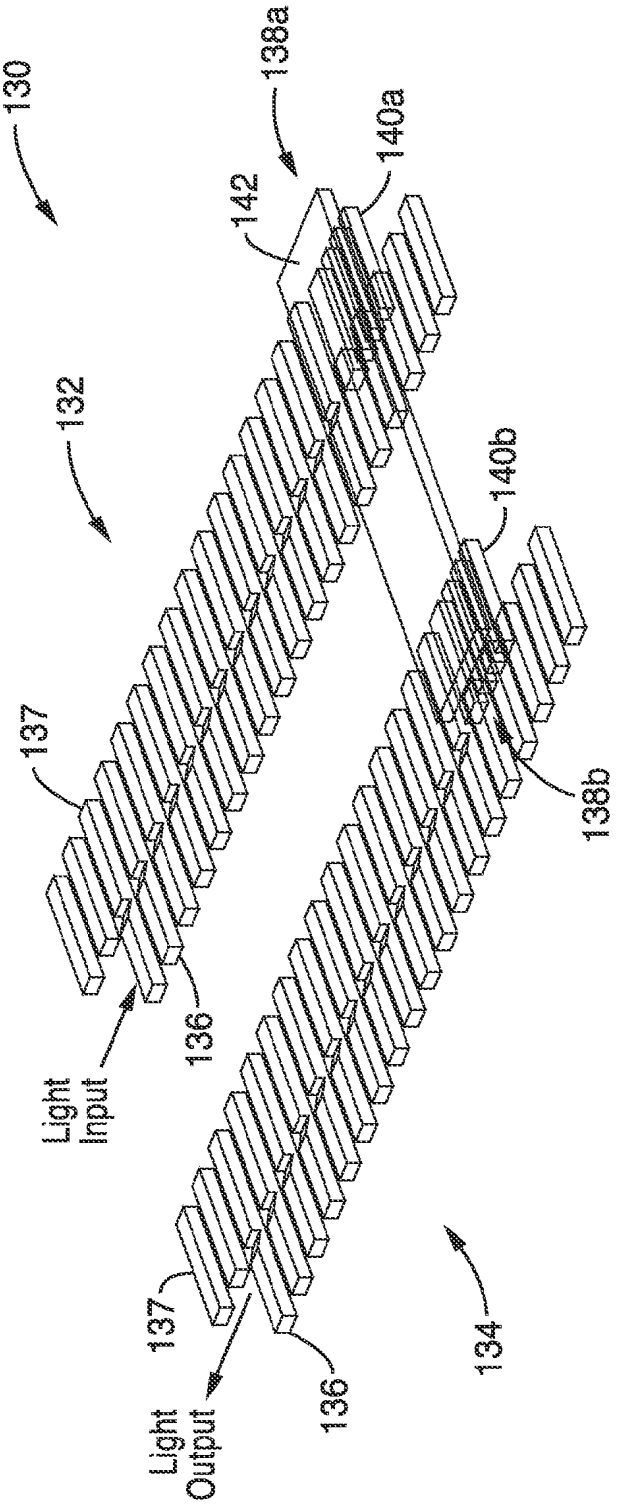

130
138a
140a
142
132
140b
137
138b
Light Input
136
137
Light Output
136
134

FIG. 14

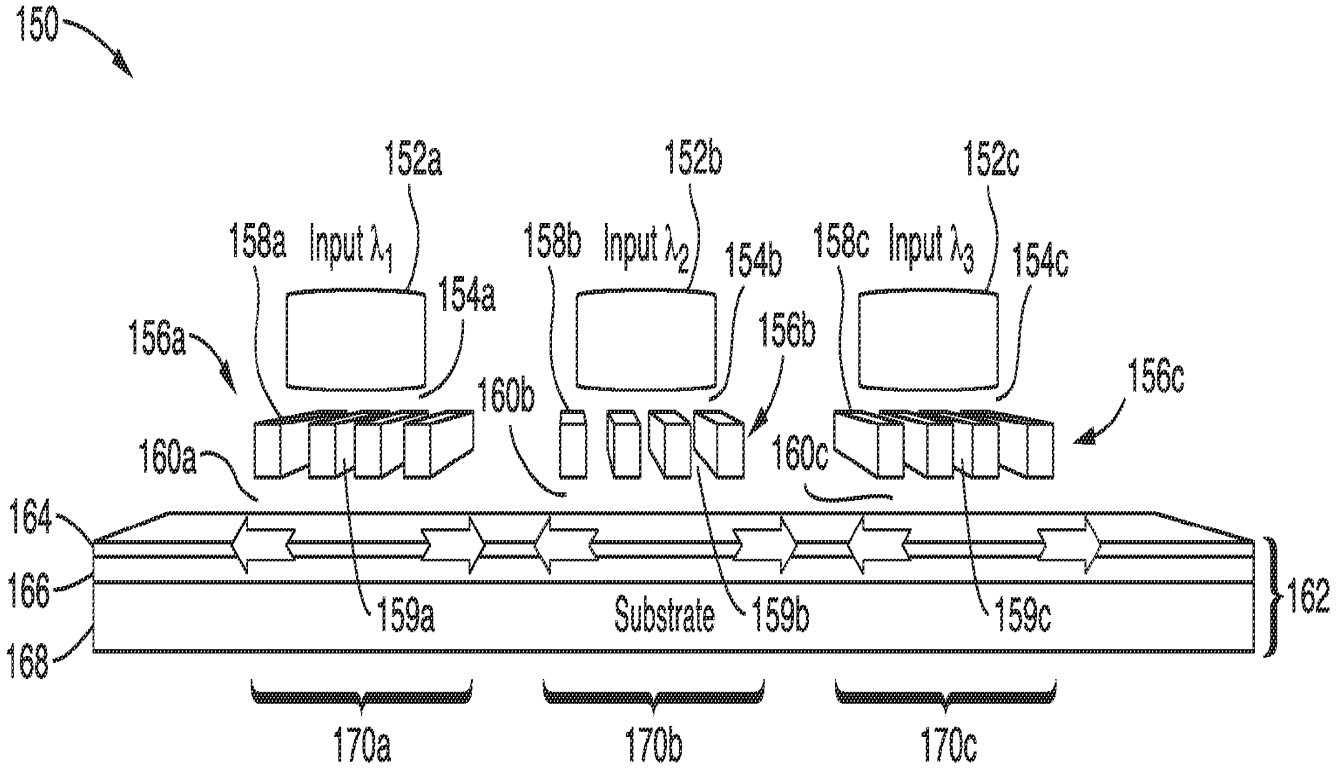

150
152a
152b
152c
158a
Input λ_1
158b
Input λ_2
158c
Input λ_3
154a
154b
154c
156a
156b
156c
160a
160b
160c
164
166
168
159a
Substrate
159b
159c
162
170a
170b
170c

FIG. 15

190
192a
192b
192c
194a
Output λ_1
Output λ_2
Output λ_3
194b
194c
196a
196b
196c
200
202
204
195a
195b
Substrate
195c
198
206a
206b
206c

FIG. 16

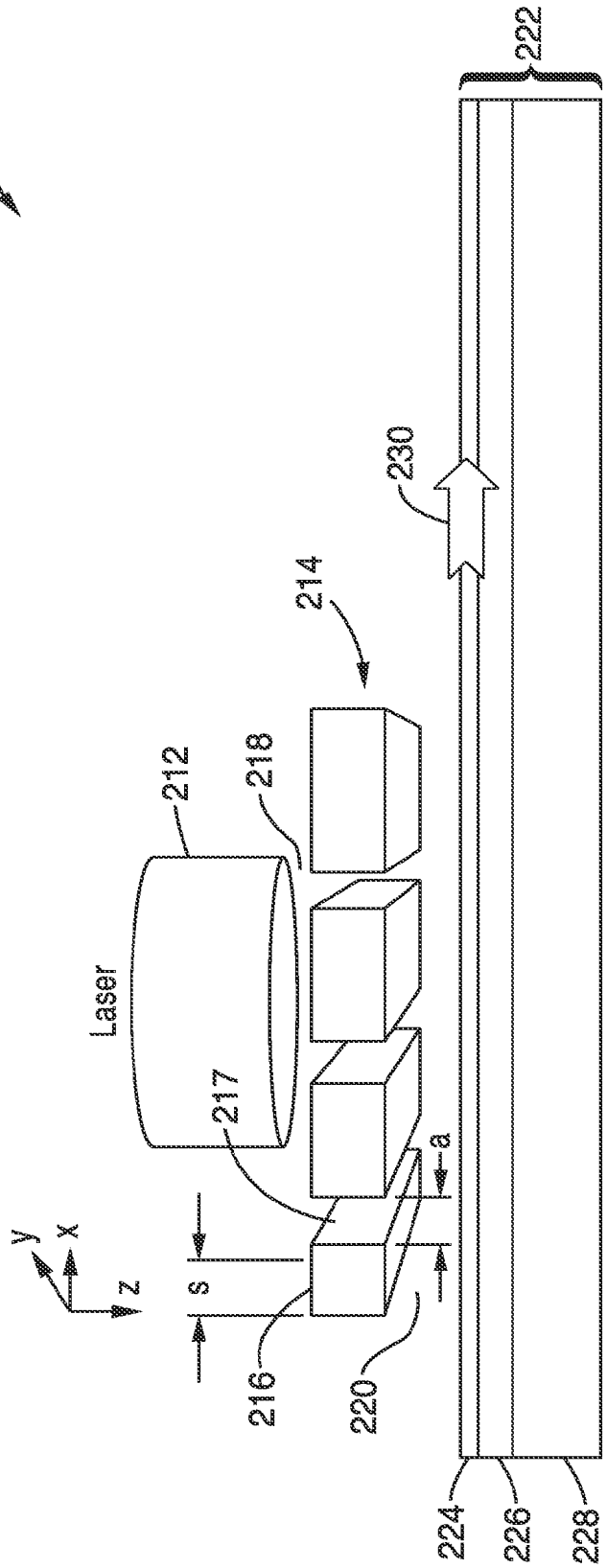


FIG. 17

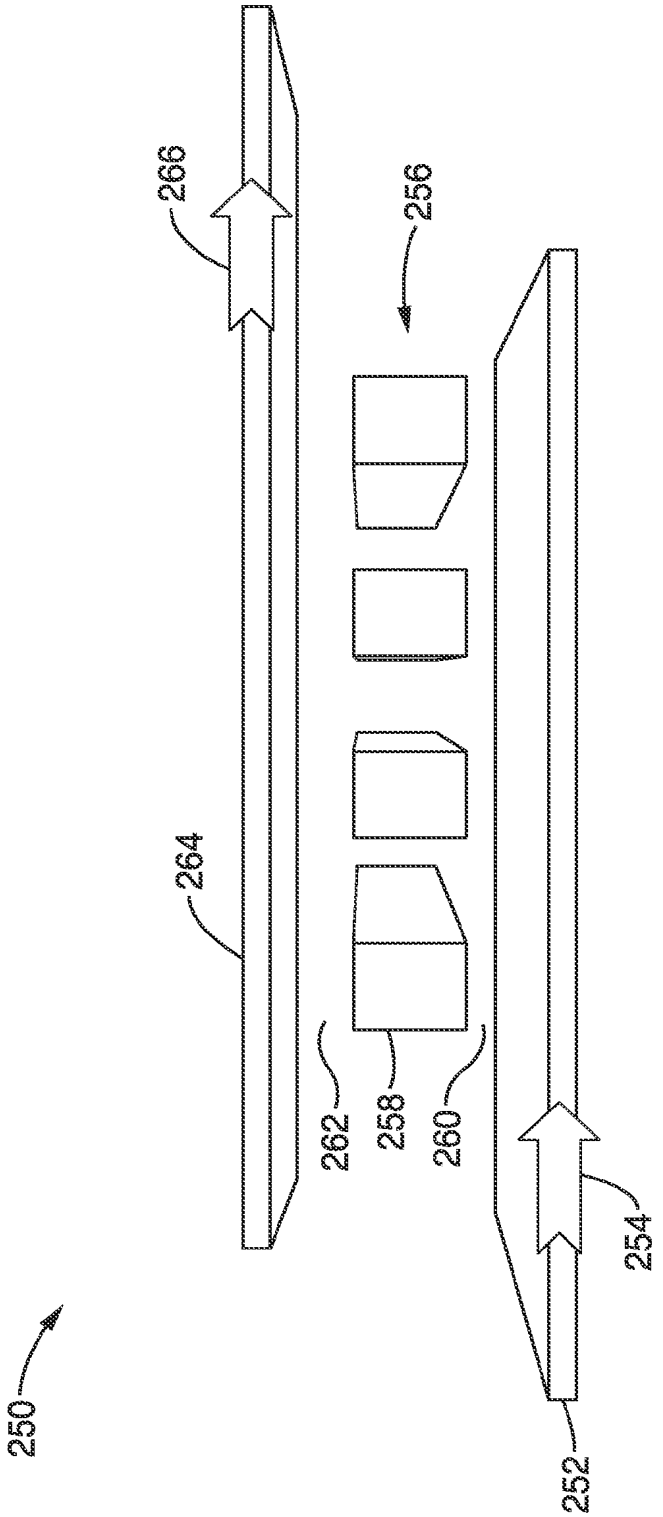


FIG. 18

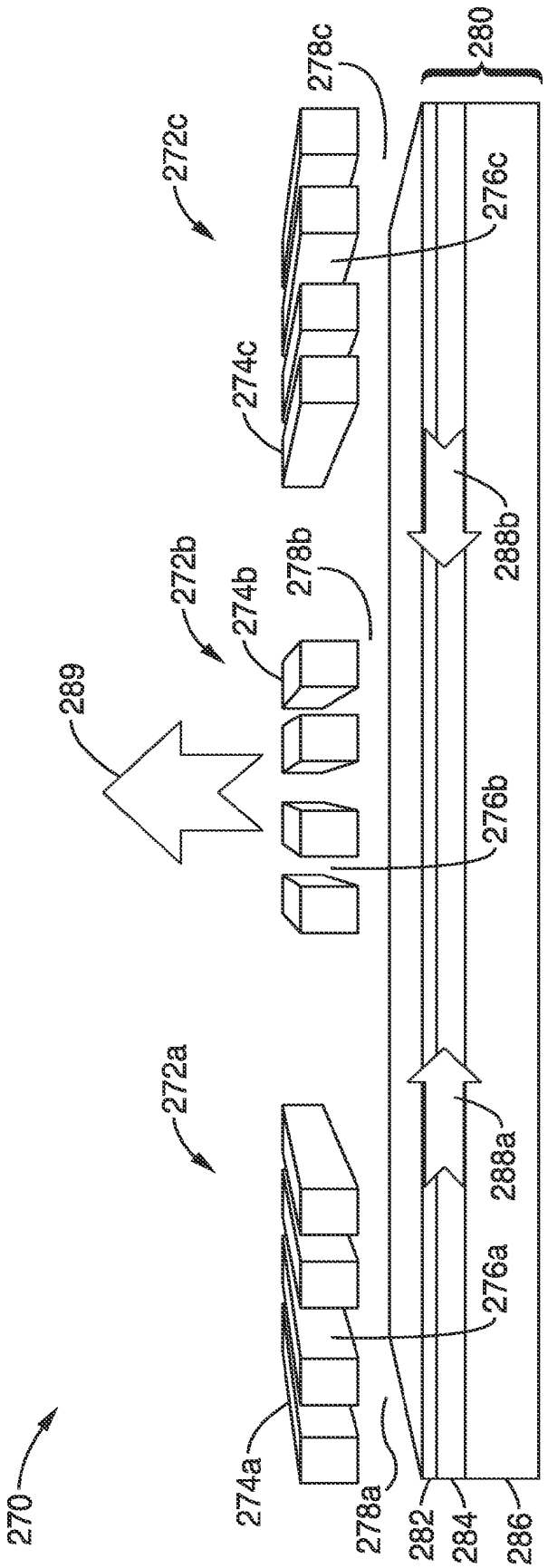

270
272a
272b
272c
274a
274b
274c
276a
276b
276c
278a
278b
278c
280
282
284
286
288a
288b
289

FIG. 19

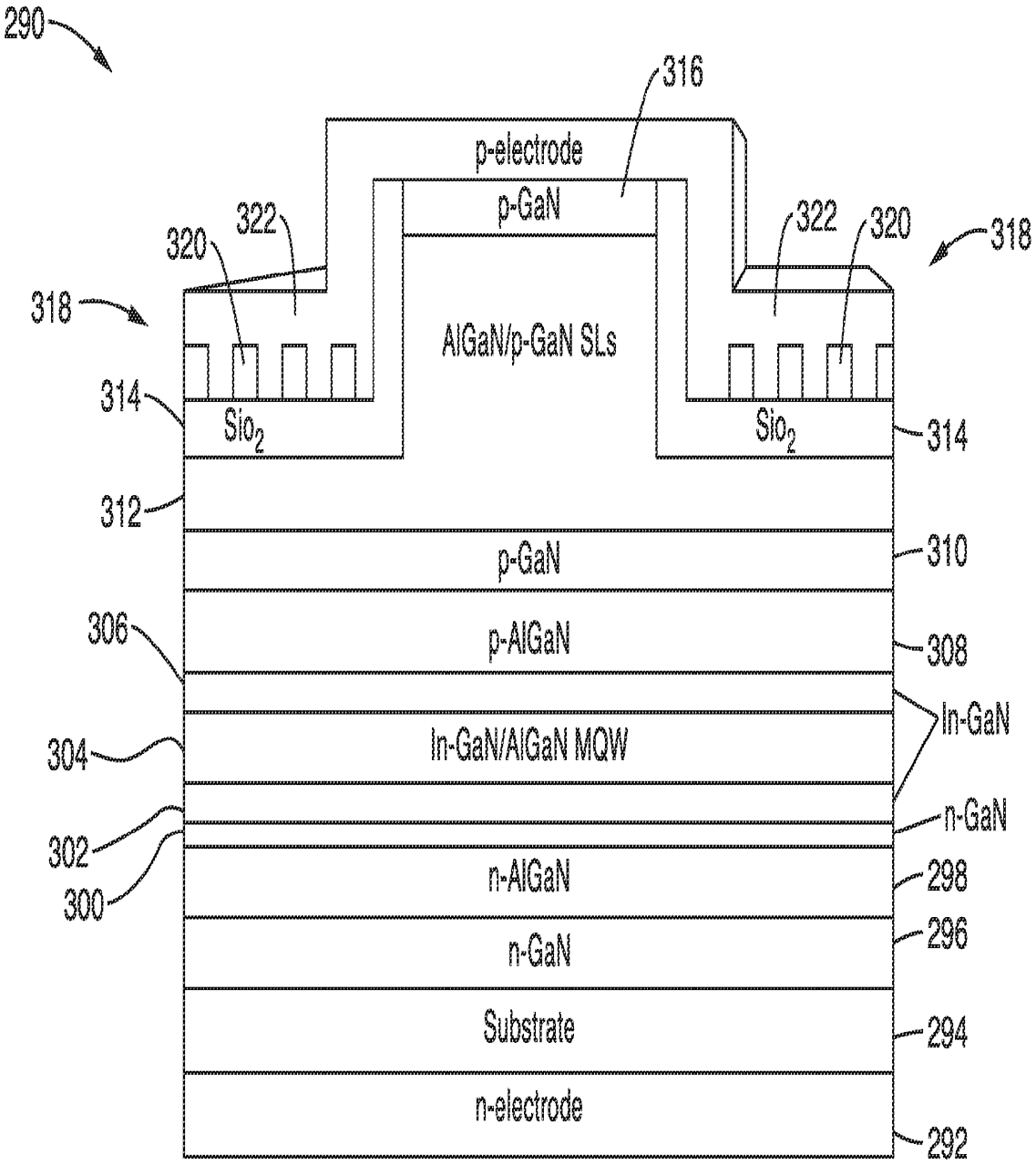

290
316
p-electrode
p-GaN
322
320
322
320
318
318
AlGaN/p-GaN SLs
314
SiO_2
SiO_2
314
312
p-GaN
310
306
p-AlGaN
308
In-GaN
304
In-GaN/AlGaN MQW
n-GaN
302
n-AlGaN
298
300
n-GaN
296
Substrate
294
n-electrode
292

FIG. 20

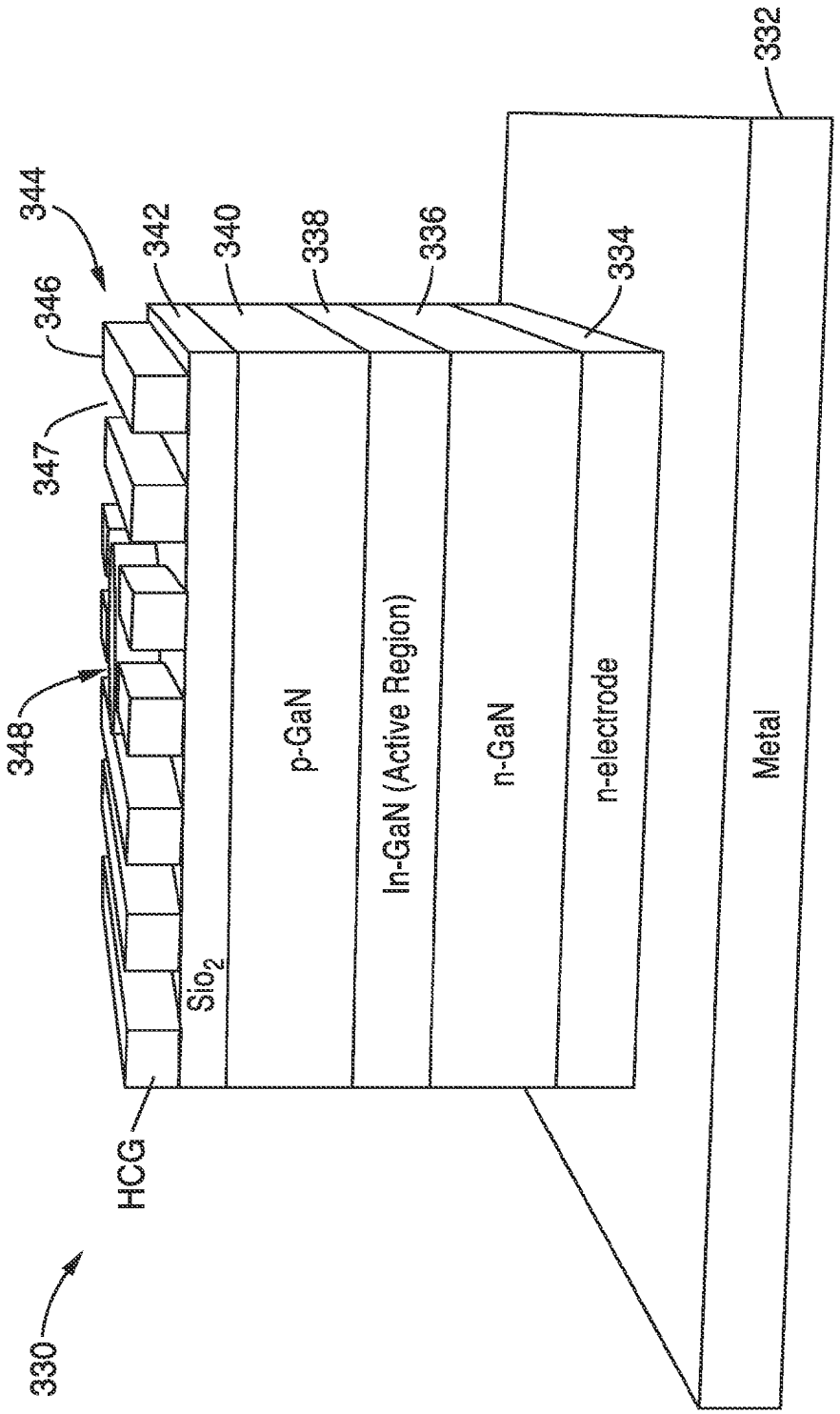

332
344
342
340
338
336
334
346
347
348
330
HCG
Sio_2
p-GaN
In-GaN (Active Region)
n-GaN
n-electrode
Metal

FIG. 21

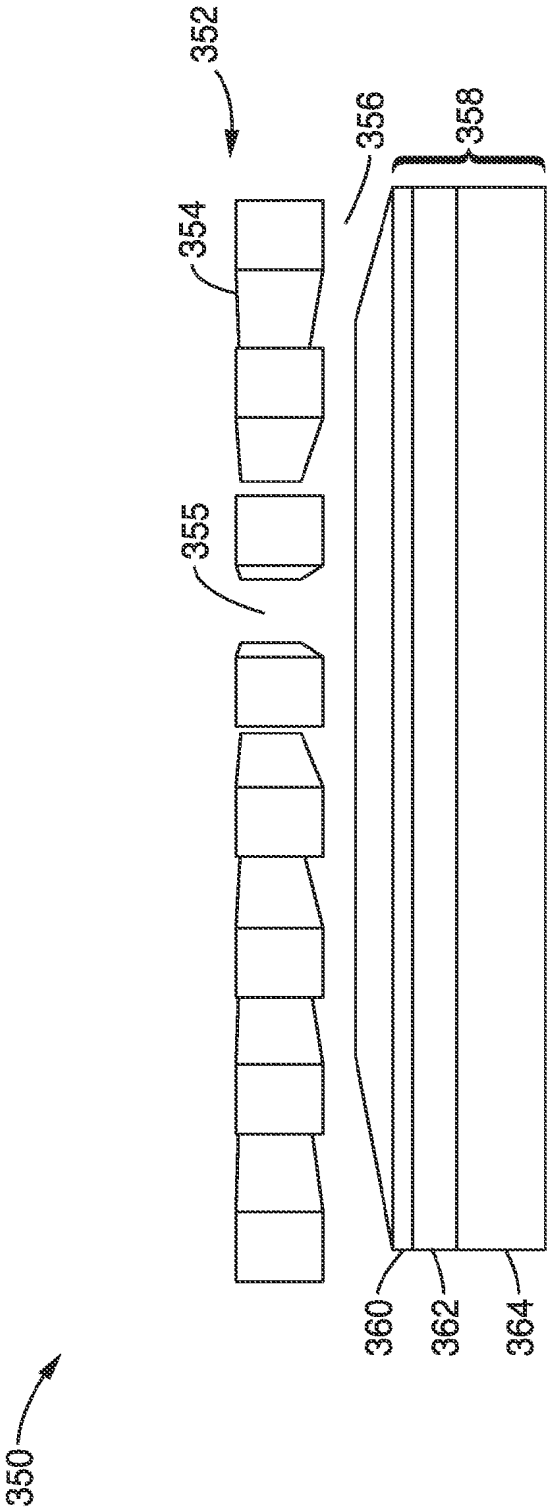


FIG. 22

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	TOT CLAIMS	IND CLAIMS
14/945,003	11/18/2015	2642	1600	2901/88184-2	30	3

CONFIRMATION NO. 1200

UPDATED FILING RECEIPT

23432
COOPER & DUNHAM, LLP
30 Rockefeller Plaza
20th Floor
NEW YORK, NY 10112

OC000000084299847

Date Mailed: 07/12/2016

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Inventor(s)

Shih-Yuan WANG, Palo Alto, CA;
Shih-Ping Wang, Los Altos, CA;

Applicant(s)

Shih-Yuan WANG, Palo Alto, CA;
Shih-Ping Wang, Los Altos, CA;

Power of Attorney: None

Domestic Priority data as claimed by applicant

This appln claims benefit of 62/232,716 09/25/2015
and claims benefit of 62/213,556 09/02/2015
and claims benefit of 62/209,311 08/24/2015
and claims benefit of 62/205,717 08/15/2015
and claims benefit of 62/199,607 07/31/2015
and claims benefit of 62/197,120 07/27/2015
and claims benefit of 62/188,876 07/06/2015
and claims benefit of 62/182,602 06/21/2015
and claims benefit of 62/175,855 06/15/2015
and claims benefit of 62/174,498 06/11/2015
and claims benefit of 62/171,915 06/05/2015
and claims benefit of 62/157,876 05/06/2015
and claims benefit of 62/154,675 04/29/2015
and claims benefit of 62/153,443 04/27/2015
and claims benefit of 62/139,511 03/27/2015
and claims benefit of 62/111,582 02/03/2015
and claims benefit of 62/100,025 01/05/2015

and claims benefit of 62/090,879 12/11/2014
and claims benefit of 62/081,538 11/18/2014

Foreign Applications for which priority is claimed (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see http://www.uspto.gov for more information.) - None.
Foreign application information must be provided in an Application Data Sheet in order to constitute a claim to foreign priority. See 37 CFR 1.55 and 1.76.

Permission to Access Application via Priority Document Exchange: No

Permission to Access Search Results: No

Applicant may provide or rescind an authorization for access using Form PTO/SB/39 or Form PTO/SB/69 as appropriate.

If Required, Foreign Filing License Granted: 12/02/2015

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 14/945,003**

Projected Publication Date: 10/20/2016

Non-Publication Request: No

Early Publication Request: No
** **SMALL ENTITY** **
Title

MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES

Preliminary Class

455

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications: No

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application

serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at http://www.uspto.gov/web/offices/pac/doc/general/index.html.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, http://www.stopfakes.gov. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4258).

LICENSE FOR FOREIGN FILING UNDER

Title 35, United States Code, Section 184

Title 37, Code of Federal Regulations, 5.11 & 5.15

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This license is to be retained by the licensee and may be used at any time on or after the effective date thereof unless it is revoked. This license is automatically transferred to any related applications(s) filed under 37 CFR 1.53(d). This license is not retroactive.

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www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
14/945,003	11/18/2015	Shih-Yuan WANG	2901/88184-2

CONFIRMATION NO. 1200

23432
COOPER & DUNHAM, LLP
30 Rockefeller Plaza
20th Floor
NEW YORK, NY 10112

INFORMAL NOTICE

OC000000084299648

Date Mailed: 07/12/2016

INFORMATIONAL NOTICE TO APPLICANT

Applicant is notified that the above-identified application contains the deficiencies noted below. No period for reply is set forth in this notice for correction of these deficiencies. However, if a deficiency relates to the inventor's oath or declaration, the applicant must file an oath or declaration in compliance with 37 CFR 1.63, or a substitute statement in compliance with 37 CFR 1.64, executed by or with respect to each actual inventor no later than the expiration of the time period set in the "Notice of Allowability" to avoid abandonment. See 37 CFR 1.53(f).

The item(s) indicated below are also required and should be submitted with any reply to this notice to avoid further processing delays.

- A properly executed inventor's oath or declaration has not been received for the following inventor(s):
  Shih-Yuan WANG
  Shih-Ping Wang

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at **(571) 272-4000** or **(571) 272-4200** or **1-888-786-0101**.

/sareebuddin/

PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number: 14/945,003

APPLICATION AS FILED - PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY FEE($)
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A	70		N/A	
SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A	300		N/A	
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A	360		N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	30 minus 20 =	* 10	x 40 =	400	OR		
INDEPENDENT CLAIMS (37 CFR 1.16(h))	3 minus 3 =	*	x 210 =	0.00			
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).			400			
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))				0.00			
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL	1530		TOTAL	

APPLICATION AS AMENDED - PART II

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY ADDITIONAL FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE($)
AMENDMENT A	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY ADDITIONAL FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE($)
AMENDMENT B	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".

The "Highest Number Previously Paid For" (Total or Independent) is the highest found in the appropriate box in column 1.

MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES

REFERENCE TO RELATED APPLICATIONS

[0001] This patent application claims the benefit of and incorporates by reference each of the following provisional applications:

U.S. Prov. Ser. No. 62/081,538 filed November 18, 2014;
U.S. Prov. Ser. No. 62/090,879 filed December 11, 2014;
U.S. Prov. Ser. No. 62/100,025 filed January 05, 2015;
U.S. Prov. Ser. No. 62/111,582 filed February 03, 2015;
U.S. Prov. Ser. No. 62/139,511 filed March 27, 2015;
U.S. Prov. Ser. No. 62/153,443 filed April 27, 2015
U.S. Prov. Ser. No. 62/154,675 filed April 29, 2015;
U.S. Prov. Ser. No. 62/157,876 filed May 06, 2015;
U.S. Prov. Ser. No. 62/171,915 filed June 05, -2015;
U.S. Prov. Ser. No. 62/174,498 filed June 11, 2015
U.S. Prov. Ser. No. 62/175,855 filed June 15, 2015;
U.S. Prov. Ser. No. 62/182,602 filed June 21, 2015;
U.S. Prov. Ser. No. 62/188,876 filed July 06, 2015;
U.S. Prov. Ser. No. 62/197,120 filed July 27, 2015;
U.S. Prov. Ser. No. 62/199,607 filed July 31, 2015;
U.S. Prov. Ser. No. 62/205,717 filed August 15, 2015;
U.S. Prov. Ser. No. 62/209,311 filed August 24, 2015;
U.S. Prov. Ser. No. 62/213,556 filed September 02, 2015; and
U.S. Prov. Ser. No. 62/232,716 filed September 25, 2015.

[0002] This patent application relates to the following provisional and non-provisional applications that are each incorporated by reference:

International Patent Appl. No. PCT/US14/39208 filed May 22, 2014;
U.S. Prov. Ser. No. 61/826,446 filed May 22, 2013;
U.S. Prov. Ser. No. 61/834,873 filed June 13, 2013;
U.S. Prov. Ser. No. 61/843,021 filed July 4, 2013;
U.S. Prov. Ser. No. 61/905,109 filed November 15, 2013; and
U.S. Prov. Ser. No. 62/017,915 filed June 27, 2014.

All of the above-referenced provisional and non-provisional patent applications are collectively referenced herein as "the commonly assigned incorporated applications."

FIELD

[0003] Thhis patent specification present invention generally relates mainly to photosensitive devices. More particularly, some embodiments relate to photosensitive devices having microstructure enhanced absorption characteristics.

BACKGROUND

[0004] Fiber-optic communication is widely used in applications such as telecommunications and communication within large data centers. Because of attenuation losses associated with using shorter optical wavelengths most fiber-optic communication uses optical wavelengths of 800 nm and longer. Commonly used transmission windows exist between 800 nm and 1675 nm. A main component of optical receivers used in fiber-optic communication system is the photo detector, usually in the form of a photodiode (PD) or avalanche photodiode (APD).

[0005] High-quality low-noise APDs can be made from silicon. However, while silicon will absorb light in the visible and near infrared range, it becomes more transparent at longer optical wavelengths. Silicon PDs and APDs can be made for optical wavelengths of 800 nm and longer by increasing the thickness of the absorption "I" region of the device. However, in order to obtain adequate quantum efficiency, the thickness of the silicon "I" region becomes so large that the device's maximum bandwidth is too low for many current and future telecom and data center applications.

[0006] To avoid the inherent problem that silicon PDs and APDs have with longer wavelengths and higher bandwidths, other materials are used. Germanium (Ge) detects infrared out to a wavelength of 1700 nm, but has relatively high multiplication noise. InGaAs can detect out to longer than 1600 nm, and has less multiplication noise than Ge, but still has far greater mulitiplacation noise than silicon. InGaAs is known to be used as the absorption region of a heterostructure diode, most typically involving InP as a substrate and as a multiplication layer. This

material system is compatible with an absorption window of roughly 900 to 1700 nm. However, both InGaAs devices are relatively expensive and have relatively high multiplication noise when compared with silicon and are difficult to integrate with Si electronics as a single chip.

[0007] Information published by a major company in the business of photodetectors (See http://files.shareholder.com/downloads/FNSR/0x0x382377/0b3893ea-fb06-417d-ac71-84f2f9084b0d/Finisar_Investor_Presentation.pdf,) indicates at page 10 that the current market for optical communication devices is over 7 billion U.S. dollars with a compounded annual growth rate of 12%. The photodiodes (PD) used for 850 nm wavelength employ GaAs material and for 1550 nm wavelength the photodiodes are InP material based, which is both expensive and difficult to integrate with Si based electronics. Therefore, there is a large market and a long-felt need that has not met for the development of a better device. To date there are no Si material based photodiodes nor avalanche photodiodes (APD) for 850 nm and no Ge on Si material based photodiodes nor avalanche photodiodes for 1550 nm that are top or bottom illuminated and with data rate of 5 Gb/s or greater, that are commercially available to the knowledge of the inventors herein. However, there has been no lack of trying to develop a better device for this large market. For example, there have been proposals for resonant photodiodes fabricated in Si material (see Resonant-Cavity-Enhanced High-Speed Si Photodiode Grown by Epitaxial Lateral Overgrowth, Schaub et al, IEEE PHOTONICS TECHNOLOGY LETTERS, VOL. 11, NO. 12, DECEMBER 1999), but they have not reached the known commercial market. Other forms of high speed photodiodes in a waveguide configuration have been proposed, such as in Ref. 40 GHz Si/Ge uni-traveling carrier waveguide photodiode, Piels et al, DOI 10.1109/JLT.2014.2310780, Journal of Lightwave Technology; Monolithic Ge/Si Avalanche Photodiodes, Kang et al, 978-1-4244-4403-8/09/$25.00 ©2009 IEEE ; High-speed Ge photodetector monolithically integrated with large cross-section silicon-on-insulator waveguide, Feng et al, Applied Physics Letters 95, 261105 (2009); doi: 10.1063/1.3279129; where light is coupled edge-wise into an optical waveguide and where the absorption length can be 100 um or longer to compensate for the weak absorption coefficient of Ge at 1550 nm. In these previously proposed waveguide photodiode

structures, light propagates along the length of the waveguide and the electric field is applied across the PIN waveguide such that the direction of light propagation and the direction of the electric field are predominately perpendicular. Since light in Si travels approximately 1000 times faster than the saturated velocity of electrons/holes, a waveguide PD can be 200 microns long for example and the "I" in the PIN can be 2 microns for example and achieve a bandwidth of over 10 Gb/s. Such edge coupling of light is costly in packaging as compared to surface illumination as described in this patent specification, where dimensions of the waveguide cross section are typically a few microns as compared to tens of microns for known surface illuminated photodiodes or avalanche photodiodes. Known waveguide PD/APD are often only single mode optical systems whereas surface illuminated PD/APD described in this patent specification can be used in both single and multimode optical systems. In addition, known waveguide photodiodes are difficult to test at wafer level, whereas surface illuminated photodiodes described in this patent specification can be easily tested at wafer level. Known waveguide photodiodes/avalanche photodiodes are used mostly in specialty photonic circuits and are not widely commercially available. A top or bottom illuminated Si and Ge on Si PD/APD that can be integrated with Si is not known to be commercially available at data rates of 5 Gb/s or more at wavelengths of 850 nm and 1550 nm. In contrast, photodiodes on Si based material, as described in this patent specification, can be monolithically integrated with integrated electronic circuits on a single Si chip, thereby significantly reducing the cost of packaging. In addition, the microstructured PD/APD at 850 nm nominal wavelength described in this patent specification can be predominately for short haul, distances less than a meter and in certain cases less than 10 meters and in certain cases less than 100 meters and in certain cases less than 1000 meters optical data transmission for example. The microstructured PD/APD direction of incident optical beam and the electric field in the "I" region of a PIN or NIP structure, are predominately collinear and or almost collinear. This patent specification enables such a device and is expected to transform the current data centers to almost all optical data transmission between blades and or within a blade, that will vastly increase the data transmission bandwidth capabilities and significantly reduce electrical power usage.

[0008] The subject matter claimed herein is not limited to embodiments that solve any specific disadvantages or that operate only in environments such as those described above. Rather, this background is only provided to illustrate one exemplary technology area where some embodiments described herein may be practiced.

SUMMARY

[0009] According to some embodiments, an integrated detector/processor circuit for data communication comprises oth a photodetector with microstructure-enhanced photoabsorption and an electronic processor formed into a single semiconductor chip. The single chip comprises a photodetector formed on a semiconductor substrate that has a photon absorbing region configured to absorb photons from an optical source signal modulated for data communication and provide an ouput electrical signal corresponding thereto, wherein the photon absorbing region comprises a plurality of holes therein exending toward said substrate and configured to concurrently receive the same source signal at a plural number of the holes; an electronic processor also formed on said semiconductor substrate and operatively associated with said photon absorbing region to receive therefrom and procces said output electrical signal into a processed output, thereby forming a single semiconductor chip that receives the optical source signal and ouputs the processed output; wherein said photon absorbing region and said electronic processor have respective thicknesses that are of the same order of magnitude; and a cathode region and an anode region operatively associated with said photon absorbing region and reverse biasing circuitry configured to apply a voltage between said cathode and anode regions such that said cathode region is driven to a more positive voltage than said anode region. The thickness of the photon absorbing region preferably is in the range of 0.5 to 5 micrometers. The electronic processor can be an application specific integrated circuit (ASIC) comprising at least one of complementary metal oxide semiconductor (CMOS) devices, bipolar (Bi) devices, and BiCMOS devices. The photon absorbing region can be configured to absorb in excess of 40%, or 50%, or 60% of the incident source signal at wavelengths from 800 nm to 900 nm, or from1400 nm nm to 1700 nm, and provide an output electrical signal corresponding thereto. The photon

absorbing region can be configured to absorb the incident source signal at an absorption percentage that varies by less than 20% over selected wavelength spans of at least 20 nm of source signal wavelengths from 800 nm to 900 nm, or from 1400 nm to 1700 nm. Each hole can have a cross-section parallel to a surface of the substrate, having a maxium dimension of between 400 nm and 2500 nm, and each hole can have a center that is spaced apart by less than 3500 nm from a center of a nearest adjacent hole of the plurality of holes. The photodetector preferably further comprises a P layer and an N layer highly doped at or exceeding 10^{19} per cm^3 and flanking said photon absorbing region, and the photon absorbing region preferably is lightly doped or not intentionally doped at most at 10^{16} per cm^3. The photodector can comprise an avalanche photodetector, and the photon absorbing region can comprise at least one of Si and Ge. The photodetector can comprise a tapered or stepped hole configured to accept an optical fiber carrying said source signal and maintaining an end of the fiber at a selected distance from said photon absorbing region. A lens can be included between said end of the fiber and the photon absorbing region. The photodector can further comprise a reflecting structure configured to cause multiple reflections of the source signal thereby traversing the photon absorbing region with said source signal multiple times. The photodector can be configured to receive the source signal from two opposite sides of the photon absorbing region, and said holes can be configured to cause coupled resonance in conversion of light to electrical signals at plural groups of the holes thereby enhancing source signal absorption.

[0010] One or more additional photodetectors can be formed on said semiconductor substrate, having respective photon absorbing regions receiveing respective additional source signals and providing respective output electrical signals corresponding thereto, and one or more additional electronic processors can also be formed on said semiconductor substrate and operatively associated with the respective photon absorbing regions of said additional photodetectors to receive therefrom and procces said respective output electrical signals therefrom. The plurality of holes can be configured to enhance absorption of photons compared to a hole-free but othewise same photodetector at a range of wavelengths that includes a wavelength of said source signal. The electronic processor can include one or more types selected from a group consisting of:

transimpedance amplifier, signal processing electronics, and routing electronics. A capacitance associated with the photodetector is decreased compared to an otherwise same photodetector having its anode and cathode regions operatively connected to a conventional bond pad. The photodector can further compre a multiplication region making it an avalanche photodiode configured to detect the source signal at a data bandwidth of greater than 10 gigabits per second, at source signal wavelengths of 800 to 900 nanometers, and having a gain of greater than 2.

[0011] In some embodiments, an optical/electonic system comprises a photodetector and an active electronic circuit built on the same semiconductor substrate and operatively associated with each other to thereby form a single integrated circuit chip; a laser modulated at Gb/s rates of data to thereby generate the optical source signal carrying information at Gb/s rates; and an optical fiber associated with the laser to receive the optical source signal at an input end thereof and transport it to an output end thereof; wherein the photodetector is associated with the output end of the optical fiber to receive the optical source signal therefrom and is configured to convert it to an electrical output signal; and wherein the active electronic circuit is associated with the photodetector to receive the output electrical signal therefrom and is configured to process the electrical output signal and output said processed electrical signal. Each of the source signal and the electrical output signal can be modulated at rates of at least 5 Gb/s. The photodector and the active electronic circuit can have thicknesses that are of the same order of magnitude. The photodector can comprise a photon absorbing region that includes a plurality of holes extending toward the semiconductor substrate, wherein plural holes are configured to concurrently receive the same source signal. Highly doped P and N layers can flank the photon absorbing region, and the photon absorbing region can have a thickness in the range of 0.1-5.0 mircometers and preferably is not intentionally doped or is lightly doped compared with the P and N regions. The photodetector can be biased to cause electrons or holes to be swept in a direction along a direction in which the source signal is received by the photodetector. Each of the photodetector and the active electronic circuit can be silicon-based. The photodector can be an avalanche photodector.

[0012] In some embodiments, a photodetector with microstructure-enhanced photoabsorption comprises a photon absorbing region preferably having a thickness between 0.5 and 5 micrometers and configured to absorb photons from a source signal modulated for data communication and provide an ouput electrical signal corresponding thereto; said photon absorbing region comprising a plurality of holes exending through at least a portion of the thickness of the photon absorbing region and configured to concurrently receive the same source signal at a plural number of the holes; and said photon absorbing region being configured to absorb in excess of 40% of the incident source signal at wavelengths in at least one of the ranges from 800 nm to 900 nm and from 1400 nm to 1700 nm and provide an output electrical signal corresponding thereto. The photon absorbing region can be configured to absorb in excess of 40% or 50% or 60% of the incident source signal at wavelengths from 800 nm to 900 nm or from 1400 nm nm to 1700 nm and provide an output electrical signal corresponding thereto. The photon absorbing region can be configured to absorb the incident source signal at an absorption percentage that varies by less than 20% over wavelength spans of at least 20 nm of source signal wavelengths from 800 nm to 900 nm or from 1400 nm to 1700 nm. Each hole has a cross-section parallel to the upper surface of the substrate that preferably has a maxium dimension of between 400 nm and 2500 nm, and each hole has a center that preferably is spaced apart by less than 3500 nm from a center of a nearest adjacent hole of the plurality of holes. The photodetector can further comprise a P layer and an N layer preferably highly doped at or exceeding 10^{19} per cm^3 and flanking said photon absorbing region, and the photon absorbing region is preferably lightly doped or not intentionally doped at most at 10^{16} per cm^3. The photodector can comprise an avalanche photodetector. The photon absorbing region can comprises Si or Ge. The photodetector can comprise a tapered or stepped hole configured to accept an optical fiber carrying said source signal and maintaining an end of the fiber at a selected distance from said photon absorbing region, and a lens can be included between said end of the fiber and the photon absorbing region. The photodetector can comprise a reflecting structure configured to cause multiple reflections of the source signal thereby traversing the photon absorbing region with said source signal multiple times. The

photodector photodector can be configured to receive the source signal from two opposite sides of the photon absorbing region.

[0013] In some embodiments, a photodetector with microstructure-enhanced photoabsorption comprises a cathode region; an anode region; reverse biasing circuitry configured to apply a voltage between said cathode and anode regions such that said cathode region is driven to a more positive voltage than said anode region; a substrate material having an upper surface; and a photon absorbing region made of silicon operatively associated with the cathode and anode regions and configured to absorb photons from a source signal, said silicon absorbing region including a plurality of holes each having a cross section parallel to the upper substrate surface having a maxium dimension of between 400 nm and 2500 nm, and each hole having a center that is spaced apart by less than 3500 nm from a center of a nearest adjacent hole of the plurality of holes. The source signal can have a wavelength that is greater than 800 nm and less than 1000 nm. The plurality of holes can be arranged into a periodically-spaced array that can have a hexagonal or square lattice pattern. The plurality of holes enhances absorption of photons compared to a hole-free but othewise same photodetector at a range of wavelengths that includes a wavelength of said source signal. Each of the holes can have a predominatly circular cross-section parallel to the upper substrate surface. The cathode and anode regions can be operatively connected to integrated circuit electronics and the photodetector and integrated circuit electronics can be integrated into a single silicon chip where the integrated circuit electronics can include one or more types selected from a group consisting of transimpedance amplifier, signal processing electronics, and routing electronics. A capacitance associated with the photodetector can be decreased compared to an otherwise same photodetector having its anode and cathode regions operatively connected to a conventional bond pad. The photodetector can further comprise a multiplication region formed of silicon and wherein the photodetector is an avalanche photodiode configured to detect the source signal at a data bandwidth of greater than 5 gigabits per second, at source signal wavelengths of 850 nanometers, and having a gain of greater than 2. The photodetector can be configured to detect said source signal at a data bandwidth of greater than 2.5 gigabits per second or greater or equal to 5 gigabits per second at source signal

wavelengths of 850 nanometers with a quantum efficiency of at least 30%, or 50%. The plurality of holes can be formed by etching away portions of silicon. The photodetector can be configured for a portion of the source signal to pass through the photon absorbing region a first time, reflect from a surface, and thereafter pass through the photon absorbing region a second time. The photodetector can further include a substrate, wherein the cathode, absorbing and anode regions are formed above the substrate and the photodetector is configured to receive the source signal from directions facing a side of the photodetector opposite of the substrate.

[0014] In some embodiments, a photodetector with microstructure-enhanced photoabsorption comprises a cathode region; an anode region; reverse biasing circuitry configured to apply a voltage between said cathode and anode regions such that said cathode region is driven to a more positive voltage than said anode region; a substrate material having an upper surface; and a photon absorbing region made of germanium-based material operatively associated with the cathode and anode regions and configured to absorb photons from a source signal, said germanium-based absorbing region including a plurality of holes each having a cross section parallel to the upper substrate surface having a maxium dimension of between 750 nm and 3000 nm, and each hole having a center that is spaced apart by less than 5000 nm from a center of a nearest adjacent hole of the plurality of holes. The germanium-based photon absorbing layer can be formed by at least one of an epitaxial growth and an epitaxial laterial overgrowth process above one or more layers of material made of silicon. The photodetector can further comprise a Ge buffer layer configured to initiate crystalline growth of Ge on an uppermost silicon layer. The photodetector's anode region can comprise a P-doped germanium layer formed by at leat one of an epitaxial growth and an epitaxial lateral overgrowth process. The photodetector can be an avalanche photodiode and can further comprise a multiplication region formed of silicon. The source signal can have a wavelength that is greater than 1200 nm and less than 1900 nm, or greater than 1400 nm. The photodetector can be configured to detect said source signal at a data bandwidth of greater than 2 gigabits per second, or 5 gigabits per second, at source signal wavelengths of 1550 nanometers with a quantum efficiency of at least 30%, or 50%.

[0015] As used herein, the grammatical conjunctions "and", "or" and "and/or" are all intended to indicate that one or more of the cases, object or subjects they connect may occur or be present. In this way, as used herein the term "or" in all cases indicates an "inclusive or" meaning rather than an "exclusive or" meaning.

[0016] As used herein the terms "hole" and "holes" refer to any opening into or through material or materials. In general the opening can have any shape and cross-section including round, elliptical, polygonal, and random shape.

BRIEF DESCRIPTION OF THE DRAWINGS

[0017] To further clarify the above and other advantages and features of the subject matter of this patent specification, specific examples of embodiments thereof are illustrated in the appended drawings. It should be appreciated that these drawings depict only illustrative embodiments and are therefore not to be considered limiting of the scope of this patent specification or the appended claims. The subject matter hereof will be described and explained with additional specificity and detail through the use of the accompanying drawings in which:

FIG. 1 is a diagram illustrating an optical data transmission system in which the microstructured photodiode/avalanche photodiode may be used, according to some embodiments;

[0018] FIG. 2 is a diagram showing wavelength selective elements included with the microstructured photodiode (MS-PD) and microstructured avalanched photodiode (MS-APD), according to some embodiments;

[0019] FIG. 3 is a diagram showing a MS-PD/APD having multiple wavelength selective elements, according to some embodiments;

[0020] FIGs. 4A-D are plots showing various bandpass filter characterisitcs, according to some embodiments;

[0021] FIG. 5 is a diagram showing a coarse wavelength division multiplexing (CWDM) configuration, according to some embodiments;

[0022] FIGs. 6A and 6B are diagrams showing some basic parts of a microstructured photodiode, according to some embodiments;

[0023] FIGs. 7A and 7B are diagrams showing some basic parts of a bottom illuminated photodiode, according to some embodiments;

[0024] FIGs. 8A and 8B are diagrams showing some basic parts of an MS-APD structure, according to some embodiments;

[0025] FIGs. 9A and 9B are diagrams showing aspects of a selective area growth (SAG) APD structure before and after SAG of III-V or Ge material, according to some embodiments;

[0026] FIG. 10 is a diagram showing a simplified microstructured silicon photodiode with PIN epitaxial layers, according to some embodiments;

[0027] FIG. 11 is a diagram showing a simplified microstructured silicon photodiode with PIN epitaxial layers, according to some embodiments;

[0028] FIGs. 12A-C show aspects of a simulation of a particular microstructured hole pattern, according to some embodiments;

[0029] FIG. 13 is a diagram showing an epitaxial layer structure for a high contrast microstructured photodiode (PD) with a P-I-N doping, according to some embodiments;

[0030] FIG. 14 is a diagram showing an epitaxial layer structure for a high contrast microstructured photodiode (PD) with a P-I-N doping, according to some embodiments;

[0031] FIG. 15 is a diagram showing an epitaxial layer structure for a high contrast microstructured photodiode (PD) with a P-I-N doping, according to some embodiments;

[0032] FIG. 16 is a diagram showing some aspects of fabrication of a high contrast microstructured photodiode (PD), according to some embodiments;

[0033] FIGs. 17A-D are diagrams showing examples of the hole arrangements, spacing, size, and passivation layers, according to some embodiments;

[0034] FIG. 18 is a diagram showing some further aspects of fabrication of a high contrast microstructured photodiode (PD), according to some embodiments;

[0035] FIG. 19 is a diagram showing some further aspects of fabrication of a high contrast microstructured photodiode (PD), according to some embodiments;

[0036] FIG. 20 is a diagram showing some further aspects of fabrication of a high contrast microstructured photodiode (PD), according to some embodiments;

[0037] FIG. 21 is a diagram showing some aspects a high contrast microstructured photodiode (PD), according to some other embodiments;

[0038] FIGs. 22A-B show aspects of a simulation of a particular microstructured PD, according to some embodiments;

[0039] FIG. 23 is a diagram showing aspects of a high contrast microstructured PD, according to some embodiments;

[0040] FIG. 24 is a diagram showing aspects of a heterogeneous epitaxial microstructured PD, according to some embodiments;

[0041] FIG. 25 shows a high contrast structure for an optical emitter such as a light emittting diode (LED) or a vertical surface emitting laser (VCSEL), according to some embodiments;

[0042] FIG. 26 shows for example the basic structure for a high contrast 1.3 micron wavelength photo emitter (PE), according to some embodiments;

[0043] FIG. 27 is a diagram showing some basic features of a high contrast microstructured photo emitter (PE) structure with etched holes, according to some embodiments;

[0044] FIG. 28 is a diagram showing some aspects of a PE, according some other embodiments;

[0045] FIG. 29 is a diagram showing some aspects of a PE, according some other embodiments;

[0046] FIG. 30 is a diagram showing some aspects of a PE, according some other embodiments;

[0047] FIG. 31 is a diagram showing some aspects of a Simple PIN photodiode structure, according to some embodiments;

[0048] FIG. 32 is a diagram showing aspects of MS-PD fabrication, according to some embodiments;

[0049] FIG. 33 is a diagram showing aspects of MS-PD fabrication, according to some embodiments;

[0050] FIG. 34 is a diagram showing aspects of MS-PD fabrication, according to some embodiments;

[0051] FIG. 35 is a diagram showing aspects of a MS-PD, according to some embodiments;

[0052] FIG. 36 is a diagram showing aspects of a MS-PD, according to some embodiments;

[0053] FIG. 37 is a diagram showing a technique to reduce minority carrier lifetime, according to some other embodiments;

[0054] FIGs. 38A-C describe various parameters for microstructured photodiodes that were simulated;

[0055] FIG. 39 is a graph plotting simulation results of microstructured hole photodiodes;

[0056] FIG. 40 is a diagram showing a microstructured avalanche photodiode (APD) with a P-I-P-I-N epitaxial structure, according to some embodiments;

[0057] FIG. 41 is a diagram showing a microstructured avalanche photodiode (APD) with a P-I-P-I-N epitaxial structure, according to some other embodiments;

[0058] FIG. 42: is a diagram showing a microstructured APD with a Ge absorption layer and Ge P capping layer, according to some embodiments;

[0059] FIGs. 43A-D show polarization sensitivity of the microstructured photodiode and APD, according to some embodiments;

[0060] FIG. 44 shows a MS-PD/APD that is integrated with a transimpedance amplifier and/or other ASIC (application specific integrated circuits) for data processing and routing, according to some embodiments;

[0061] FIG. 45 is a diagram showing some aspects of a flip chip arrangement for a MS-PD/APD integrated with a TIA and/or other signal processing IC on a single silicon chip, according to some embodiments;

[0062] FIG. 46 is a diagram showing some aspects of a flip chip arrangement for a MS-PD/APD integrated with a TIA and/or other signal processing IC on a single silicon chip, according to some other embodiments;

[0063] FIG. 47 is a diagram showing some aspects of a flip chip arrangement for a MS-PD/APD integrated with a TIA and/or other signal processing IC on a single silicon chip, according to some other embodiments;

[0064] FIG. 48 is a diagram showing some aspects of a flip chip arrangement for a MS-PD/APD integrated with a TIA and/or other signal processing IC on a single silicon chip, according to some other embodiments;

[0065] FIG. 49 is a diagram showing some aspects of a flip chip arrangement for a MS-PD/APD integrated with a TIA and/or other signal processing IC on a single silicon chip, according to some other embodiments;

[0066] FIG. 50 is a diagram showing some aspects of a flip chip arrangement for a MS-PD/APD integrated with a TIA and/or other signal processing IC on a single silicon chip, according to some other embodiments;

[0067] FIG. 51 is a diagram showing some aspects of a flip chip arrangement for a MS-PD/APD integrated with a TIA and/or other signal processing IC on a single silicon chip, according to some other embodiments;

[0068] FIG. 52 is a diagram showing an array of MS-PD/APDs integrated with IC electronics such as TIA and/or other signal processing and routing electronics on a single Si chip, according to some embodiments;

[0069] FIG. 53 is a diagram showing an epitaxial structure for a high data rate MS-PD, according to some embodiments;

[0070] FIG. 54 is a diagram showing an epitaxial structure for a high data rate MS-PD, according to some embodiments;

[0071] FIG. 55 is a diagram showing an epitaxial structure for a high data rate MS-PD, according to some embodiments;

[0072] FIG. 56 is a table showing the mesa size, hole diameters, hole period distances, and lattice patterns for MS-PDs, according to some embodiments;

[0073] FIGs. 57A and 57B are diagrams showing hexagonal and square lattice hole patterns, according to some embodiments;

[0074] FIG. 58 is a diagram showing an epitaxial layer structure for a silicon MS-PD, according to some embodiments;

[0075] FIG. 59 is a diagram showing aspects of a MS-PD, according to some embodiments;

[0076] FIG. 60 is a diagram showing aspects of a MS-PD, according to some embodiments;

[0077] FIG. 61 is a diagram showing aspects of a MS-PD, according to some embodiments;

[0078] FIG. 62 shows a Ge on Si PIN epitaxial layer structure for a MS-PD, according to some embodiments;

[0079] FIGs. 63-65 are diagrams showing aspects of Ge on Si MS-PDs, according to some embodiments;

[0080] FIGs. 66-67 are diagrams showing aspects of Ge on Si PDs, according to some embodiments;

[0081] FIGs. 68-69 are diagrams showing aspects of MS-APDs, according to some embodiments;

[0082] FIG. 70 is a diagram showing a MS-APD without the SiO2 layer, according to some embodiments;

[0083] FIGs. 71-72 are diagrams showing Ge on Si microstructured avalanche photodiodes (MS-APDs), according to some embodiments;

[0084] FIG. 73 is a diagram showing a Ge on Si microstructured avalanche photodiode (MS-APD) with an etch stop layer, according to some embodiments;

[0085] FIG. 74 is a diagram showing a Ge on Si microstructured avalanche photodiode (MS-APD), according to some embodiments;

[0086] FIG. 75 is a diagram showing another SI NIP epitaxial layer structure for a MS-PD, according to some embodiments;

[0087] FIGs. 76A-C are diagrams showing Si N-I-P epitaxial layers on buried oxide for a MS-PD, according to some embodiments;

[0088] FIG. 77 is a diagram showing a MS-PD with Si NIP epitaxial layer and a SiGeB stop etch layer on a P Si substrate, according to some embodiments;

[0089] FIG. 78 is a diagram showing a Ge on Si NIP on SiGeB epitaxial layer structure for MS-PD, according to some embodiments;

[0090] FIG. 79 is diagram showing a Ge on Si epitaxial structure for MS-PD, according to some embodiments;

[0091] FIG. 80 is a diagram showing another Ge on Si epitaxial structure, according to some embodiments;

[0092] FIG. 81 is a diagram showing a Ge on Si epitaxial structure, according to some embodiments;

[0093] FIGs. 82A-82C relate to a simulation using finite difference time domain (FDTD) on a Ge on Si microstructured photodiode similar to the structure depicted in FIG. 79;

[0094] FIGs. 83A-83C relate to a simulation using finite difference time domain (FDTD) on a Ge on Si microstructured photodiode similar to the structure in FIG. 80;

[0095] FIGs. 84A and 84B shows result of a simulation using finite difference time domain (FDTD) on a Ge on Si microstructured photodiode similar to the structure in Fig. 79;

[0096] FIG. 85 shows a schematic top view of a microstructured photodiode chip, according to some embodiments;

[0097] FIG. 86 is a top view diagram showing a MS-PD/APD integrated with a transimpedance amplifier and/or other electronics on a single chip, according tosome embodients;;

[0098] FIG. 87 shows a simple epitaxial structure without any microstructures.

[0099] FIG. 88 shows another simple epitaxial structure without any microstructures;

[00100] FIG. 89 shows an epitaxial structure the same as in FIG. 87 where microstructured hole arrays are etched to the Si P epitaxial layer, according to some embodiments;

[00101] FIG. 90 shows an epitaxial structure the same as in FIG. 88 where microstructured hole arrays are etched to the BOX SiO2 layer, according to some embodiments;

[00102] FIGs. 91A-91B are plots showing results of simulations for the example structures depicted in FIGs. 87-90;

[00103] FIG. 92 is a diagram showing a microstructured region in the silicon where holes are etched into the silicon, according to some embodiments;

[00104] FIG. 93 is a diagram showing a MS-PD structure with tapered holes, according to some embodiments;

[00105] FIG. 94 is a diagram showing a MS-PD structure with gradually tapered holes, according to some embodiments;

[00106] FIG. 95 is a diagram showing a material structure with different diameter microstructured holes, according to some embodiments;

[00107] FIG. 96 shows a top view the material structure with different diameter microstructured holes, as depicted in FIG. 95;

[00108] FIGs. 97A and 97B are graphs showing the absorption for light incident on a microstructure with layer structure as shown in FIG. 82A;

[00109] FIG. 98 is a graph showing simulated absorption for the structure shown in FIG. 82A and simulated in FIGs. 97A and 97B;

[00110] FIG. 99 shows another preferred epitaxial structure for a Si avalanche photodiode for operation in wavelength range from 800 to 1000 nm, according to some embodiments;

[00111] FIG. 100 is a diagram showing some features of a microstructured APD, according to some embodiments;

[00112] FIG. 101 shows another preferred epitaxial structure for Ge on Si avalanche photodiode for operation in wavelength ranges from 800 to 1600 nm, according to some embodiments;

[00113] FIG. 102 is a diagram showing some features of a microstructured Ge on Si SPD;

[00114] FIGs. 103A-C show hole diameters, periods, and other parameters for microstructured silicon and germanium on Si photodiodes and avalanche photodiodes, according to some embodiments;

[00115] FIGs. 104A and 104B are graphs showing simulation results using FDTD (finite difference time domain) for absorption verse wavelength for the structure shown in FIG. 82A which is microstructured Ge P-Ge I - Si N on Si N substrate photodiode;

[00116] FIGs. 105A and 105B relate to eigenmodes for a square lattice hole pattern, according to some embodiments;

[00117] FIG. 106 is a schematic diagram showing microstructured holes with two square lattices arranged overlapping each other, according to some embodiments;

[00118] FIG. 107 is a diagram showing an epitaxial structure of Ge on Si, according to some embodiments;

[00119] FIG. 108 is a diagram showing the basic features of a microstructured photodiode of Ge on Si, according to some embodiments;

[00120] FIGs. 109A and 109B are graphs showing results of FDTD simulations using Maxwell equations for a microstructured hole array, according to some embodiments;

[00121] FIG. 110 shows plots of absorption verses wavelength for microstructured photodiodes/avalanche photodiodes with different hole diameters and lattice periods, according to some embodiments;

[00122] FIGs. 111A and 111B shows a simulation using FDTD methods of a structure as in FIG. 82A where two lattices and two different hole diameters are used, according to some embodiments;

[00123] FIG. 112 is a diagram shows another lattice structure where two hexagonal lattices with the same period are combined and interlaced within each other, according to some embodiments;

[00124] FIG. 113 shows a hexagonal lattice with 6 unit cells, each cell with its Eigen modes where any field propagation/distribution can be an expansion of its Eigen modes;

[00125] FIG. 114 shows a Si NIP microstructured photodiode with hole arrays and textured surfaces, according to some embodiments;

[00126] FIG. 115 is a graph showing absorption coefficient of Si and Ge verses wavelength;

[00127] FIG. 116 is a graph showing enhanced effective absorption coefficient of Ge due to microstructured hole arrays, according to some embodiments; and

[00128] FIG. 117 is graph showing the enhanced absorption of a Si microstructured PD/APD, according to some embodiments.

DETAILED DESCRIPTION

[00129] A detailed description of examples of preferred embodiments is provided below. While several embodiments are described, it should be understood that the new subject matter described in this patent specification is not limited to any one embodiment or combination of embodiments described herein, but instead encompasses numerous alternatives, modifications, and equivalents. In addition, while numerous specific details are set forth in the following description in order to provide a thorough understanding, some embodiments can be practiced without some or all of these details. Moreover, for the purpose of clarity, certain technical material that is known in the related art has not been described in detail in order to avoid unnecessarily obscuring the new subject matter described herein. It should be clear that individual features of one or several of the specific embodiments described herein can be used in combination with features or other described embodiments. Further, like reference numbers and designations in the various drawings indicate like elements.

[00130] According to some embodiments, microstructures are used to improve bulk absorption constant or absorption of the material at wavelengths in the

proximity of the semiconductor material's band gap. This allows for extending the operating optical wavelengths and/or operating spectrum of the photosensor. The enhanced bulk absorption constant (or coefficient) is called the effective absorption constant (or coefficient). The term "effective" is used since absorption constant or coefficient is an inherent material property. However, with resonance effects, coupled resonance effects, slow wave effects, plasmonic effects, field enhancement effects, scattering effects, near field and sub wavelength effects, linear and non-linear effects, the effective absorption constant or coefficient can be greater than the bulk or material absorption constant or coefficient. Since absorption is exponentially dependent on the product of the absorption coefficient and absorption length, by keeping the bulk absorption coefficient, the effective absorption length can be greater than the physical length of the “l” absorbing region of a PD/APD to achieve the same absorption which is proportional to quantum efficiency. As used herein, the following terms are used interchangeably: enhanced absorption constant, enhanced absorption coefficient; enhanced effective absorption constant; enhanced effective absorption coefficient; and effective absorption constant; and effective absorption coefficient, enhanced absorption length, effective absorption length, enhanced effective absorption length. Enhanced absorption or effective absorption can be due to either or both enhanced absorption coefficient and or enhanced absorption length.

[00131] According to some embodiments, enhanced absorption can also have drastic effects on path length. In one bulk absorption example, the path length for the photons to be absorbed to 1/e of its original amplitude is 100 micrometers (μm), whereas under enhanced absorption according to some embodiments described in this patent specification, the path length is 1 micrometer for the optical amplitude to decay to 1/e of its original amplitude. Equivalently, if path length is kept constant to one micrometer then the enhanced absorption coefficient is 100 times greater than the bulk absorption coefficient and or the enhanced effective absorption length is 100 times greater than the actual physical length.

[00132] This is seen by the relationship $A= A_0 e^{-\alpha L}$ where A is the decaying amplitude of the incident photon flux A_0 and α is the absorption coefficient and L the path length for absorption to take place. So, rather than have L be 100 times longer, an effective α can be defined such that it is 100 times greater than a non

enhanced absorption coefficient such as the bulk absorption coefficient. The resonance/ coupled resonance/scattering/near field effects of microstructures, for example, gives the equivalence of the path length that is 100 times longer where the resonant/scattering/near field microstructure is just one micron long. A more simplistic description of this is that the photons in the resonant/coupled resonace structures make 50 round trips before reaching the 1/e value of its original amplitude, so the equivalent linear length is 100 times the length of the coupled resonant structure. For simplicity, resonance/coupled resonance/ linear and nonlinear field enhancement/scattering/near field effects will collectively be referred to herein as “resonant” which can include, resonant, coupled resonance, slow wave, scattering, near field, plasmonic, nonlinear and linear optical field effects.

[00133] As used herein the terms "microstructures" and “microstructured” refer to: pillars, voids, holes and mesas, of various shapes and sizes having at least one dimension in the micrometer scale, or submicrometer scale, and/or sub-wavelength scale and or wavelength scale.

[00134] According to some embodiments, the techniques for enhancing effective absorption can be applied to various materials including: silicon, germanium, III-V material such as InP, GaAs, GaN, InGaAs, and any combination of the III-V material family. As used herein, the term "material family" of a III-V material is defined as any material that is lattice matched or approximately lattice matched (within a few percent) to GaAs, InP, GaN, InSb semiconductors. For example, the InP material family can include InGaAs, InGaAsP, InAlAs, InAs. According to some embodiments, in the case of microstructures, regrowth such as selective area growth (SAG), epitaxial lateral over growth (ELOG), epitaxial growth (EG) with or without a thin buffer layer of Ge, InGaAs, or other III-V material in silicon microstructures can be carried out without the detrimental effects of lattice mismatch since the dimension of the footprint of the lattice mismatched material on silicon is small (approximately a few micrometers to sub-micrometers). This allows Ge and other III-V materials to be integrated with silicon without the use of a conventional buffer layer (such as amorphous Ge in the case of Ge on Si growth). The heterogeneous integration of materials can be homo or hetero structures, combination of crystalline and microcrystalline and amorphous semiconductor, conductor such as carbon, graphene, insulator, dielectrics, solid, gaseous, liquid

such as glass or polymer that can be semiconducting. Ge and III-V materials can also be grown on Si with or without a buffer layer using SOG, ELOG, EG methods that can cover areas greater than micrometer scale to areas that cover wafer scale.

[00135] According to some embodiments, a low index material is used such as buried oxide (BOX), silicon on insulator (SOI), silicon on sapphire (SOS), low-density semiconductors such as amorphous semiconductor, nanowire semiconductors, voids and holes to lower the effective refractive index. Refractive index is an inherent property of a material. However, according to some embodiments, when structures such as voids, air gaps, and/or holes (which can be filled with low index material, and/or regrowth) have dimensions on the order of the optical wavelength, the optical electromagnetic field will see an average refractive index consisting of the material refractive index and the structures (which can be filled or partially filled by a low refractive index material). This average is referred to herein as the effective refractive index. According to some embodiments, a low index or low effective index material need not be used in the microstructures.

[00136] According to some embodiments, the techniques for enhancing effective absorption can be applied to various materials including: silicon, germanium, III-V material such as InP, GaAs, GaN, InGaAs, and any combination of the III-V material family.

[00137] Due to the microstructures, the capacitance can also be represented by an effective capacitance which is a parallel capacitance of (1) the dielectric constant of one semiconductor, and (2) the dielectric constant of another material, which can be a semiconductor, dielectric, gas, vacuum, partial vacuum, liquid such as glass or polymer (polyimide, mylar, or other organic compound). The effective capacitance of the device is the combination of the capacitance of the parallel capacitors, which can be two or more. An advantage of the use of microstructure, according to some embodiments, is that the effective capacitance can be significantly lower than the capacitance of a homogeneous material such as a semiconductor. The RC time (resistance capacitance) is one of the fundamental time that determine the bandwidth of a photodiode and avalanche photodiode. Lower capacitance allows a device to have a larger area while still maintaining suitably high data rate bandwidth, and/or increase the data rate bandwidth by reducing the thickness of the device to reduce the electron and or hole transit time

which is also a fundamental time that determine the bandwidth of the PD/APD. Another fundamental time is the optical transit time.

[00138] According to some embodiments, the photosensor can be a photodiode (PD), avalanche photodiode (APD), photovoltaic (PV) or solar cell, or any optoelectronic device that converts photons to electrons. According to some embodiments, emitters such as lasers and light emitting diodes that convert electrons/holes to photons can also be implemented using microstructures.

[00139] According to some embodiments, the enhanced absorption allows the APD/PD to: (1) extend the sensitivity of the APD/PD to photons with energies (or wavelength) closer to the material band gap where the bulk absorption coefficient is weak, for example approximately 1000 1/cm or less with QE (quantum efficiecy) greater than 30% or greater than 50% and data bandwidth greater than 3 Gb/s; (2) operate at a high data rate bandwidth (e.g. >10 Gb/s), due to shorter absorption length therefore shorter transit time; (3) increase quantum efficiency with enhanced absorption; (4) be manufactured of silicon which has superior multiplication properties with low excess noise for avalanche photodiode; (5) be compatible with Si Photonics and CMOS processes. According to some embodiments, the PD/APD can be integrated with an ASIC (application specific integrated circuit) such as signal processing, signal amplification, memory, cpu, electrical transmitter, optical waveguides, integrated optics, and other ICs for specific applications. This is advantageous for mass production using CMOS foundries. In addition the surface (or bottom) illuminated PD/APD integrated with or without electronics can be tested at wafer level probing and in addition can handle both single and multimode. The single optical and electronic chip by pass the need of ceramic multichip carriers and significantly reduce the cost of assembly and packaging. Silcion bench can also be used in conjuction for optical alignment to optical components such as lens, fibers, if needed.

[00140] According to some embodiments, silicon is used for avalanche gain. Silicon has lower excess noise for an avalanche photodiode. By integrating Ge with silicon, the absorption takes place in the Ge material and the electronic gain occurs in silicon. Depending on the optical wavelengths, for example shorter than 1100 nm, silicon may be used for both absorption and electronic gain with the use of microstructures.

[00141] According to some embodiments, the absorption of photons in semiconductors is enhanced with the use of microstructures. The microstructures can have effects such as resonance, coupled resonances, field enhancement, near field and sub wavelength effects, scattering, plasmonics, linear and non linear optical field, photonic crystal, absorption mode or lossy mode in high contrast grating at the near field regime, which are both linear and non linear effects that can effectively increase the effective absorption length resulting in a greater absorption of the photons for a given physical length and or the absorption coefficient can be enhaced to an effective coefficient.

[00142] According to some embodiments, microstructures used for absorption enhancement, due to length and/or coefficient enhancement, for silicon photodiodes and silicon avalanche photodiodes can result in silicon PD and APD with bandwidths in excess of 10 Gb/s (or equivalently 6.75 GHz approximately depending of the digital coding format) at photons with wavelengths of 850 nm approximately (which is the current datacom preferred wavelength) with quantum efficiencies of approximately 50% or more, in some cases QE of 70% ot more.

[00143] Silicon optical detectors are very robust due to the maturity of the material and processing techniques, the surfaces can be easily passivated to eliminate dangling bonds that can cause surface states and carrier recombination centers, they have excellent carrier lifetimes due to low defects and high material purity, and for APD applications, the noise is low due to the small ionization ratio between holes and electrons (k factor, silicon have the lowest k factor than any III-V material) and such detectors are CMOS compatible for integration with electronics for signal processing and with Si photonics.

[00144] According to some embodiments, the photogenerated carriers are swept out with an external reverse bias in the absorbing “i” (some times referred to as “I”) region of a P-I-N diode (PD) or P-I-P-I-N diode (APD) for high modulation bandwidth (greater than or equal to 10 Gb/s bandwidth) and high quantum efficiency and for APD for high current gain, with gain greater than 3 dB.

[00145] The microstructured photodiodes and avalanched photodiodes with bandwidths of greater than 1 Gb/s are used in communication. An optical signal has information impressed on the light using techniques such as: binary (intensity), phase/frequency shifting (coherent, heterodyne communication); polarization

coding; multiple wavelength such as wavelength division multiplexing; and polarization multiplexing. The optical signal travels through air and or fiber, and impinges on the microstructure photodiode and/or avalanche photodiode where the information impressed on the optical light can be extracted into electrical signals. In some cases, another optical source or sources need to be mixed as in heterodyne or homodyne.

[00146] FIG. 1 is a diagram illustrating an optical data transmission system in which the microstructured photodiode/avalanche photodiode may be used, according to some embodiments. The optical data transmission system 100 consists of an optical source(s) 110, a transmission medium such as air and/or optical fiber(s) 120 and the microstructured photodiode(s)/avalanche photodiode(s) MS-PD/APD) 130. According to some embodiments, optical source 110 can be a laser. Electrical data 112 is impressed on the optical signal with a power supply 114 forward biasing the laser 110 for direct modulation. The output of the laser 110 can be coupled to an optical fiber 120 via a coupler 122 such as a ball lens. The optical signal propagates through the fiber 120 (or air) and can be coupled from the fiber 120 via a lens 124, for example, to the high speed microstructure photodiode/avalanched photodiode 130, where the optical signal is converted to electrical signal and the redulting data 132 (which matches data 112) is recovered. The microstructure photodiode/avalanche photodiode is reverse biased using power supply 134.

[00147] According to some embodiments, wavelength selective elements can be integrated with the microstructured photodiode and microstructured avalanche photodiode. In particular, arrays of microstructured photodiodes/avalanche photodiodes can be fabricated on a single chip that can include application specific integrated circuits comprising CMOS, bi-CMOS, bipolar devices and circuits, for example. A wavelength selective element, such as a bandpass filter, can be used for coarse wavelength division multiplexing (CWDM) where, for example, 810, 820, 830, 840, 850, 860, 870, 880 nm wavelengths each carrying 10-40 Gb/s of modulated data can have an aggregated data rate of 80-320 Gb/s within a single transmission medium.

[00148] Examples of wavelength selective elements include: high contrast subwavelength gratings; arrays of subwavelength holes in a metal film or dielectric

film, and dielectric layers with alternating refractive indicies as in Bragg reflectors. The wavelength selective element can be a bandpass filter that includes multiple high contrast gratings to form a resonance cavity. The element can also be a combination of gratings and other wavelength selective elements such as subwavelength hole arrays on metallic or semi-metallic films and/or Bragg mirrors.

[00149] In addition, the microstructure of the photodiode/avalanche photodiode can itself form a reflector such as a high contrast grating such that it can be both wavelength selective and absorption length enhancing. In particular, the photon absorption region of the photodiode/avalanche photodiode can be enhanced. According to some embodiments, an additional high contrast grating can be fabricated above the microstructured photodiode/avalanche photodiode to form a resonance optical cavity for wavelength selectivity. If one of the high contrast gratings can be electrically biased such that a voltage develops between the two wavelength-selective elements, the selected wavelength can be tuned, such as a tunable optical filter.

[00150] FIG. 2 is a diagram showing wavelength selective elements included with the microstructured photodiode (MS-PD) and microstructured avalanched photodiode (MS-APD), according to some embodiments. Using wavelength selective elements 220, only wavelengths within the selected wavelength range impinge on the MS-PD/APD 130. According to some embodiments, the window can be 1-20 nm in width (e.g. a center wavelength of 820 nm +/- 5 nm where the bandpass is 10 nm centered at 820 nm). Shown in the case of FIG. 2 is a high contrast grating 220 made of silicon that can be integrated with the silicon MS-PD/APD 130. According to some embodiments, the microstructure features 210 of the microstructured photodiode/avalanche photodiode 130 can also behave as a wavelength selector by itself, in addition to their function of enhancing the absorption properties of the photodiode and avalanche photodiode. If the microstructures 210 of the MS-PD/APD 130 are designed as a wavelength selector, than the addition of a high contrast grating 220 will create a resonance cavity that can function as a bandpass filter.

[00151] FIG. 3 is a diagram showing a MS-PD/APD having multiple wavelength selective elements, according to some embodiments. In this case, multiple wavelength selective elements 320 and 322 are fabricated and integrated into MS-

PD/APD 130. Wavelength selective elements 320 and 322 can be a dual high contrast grating that function as a bandpass filter. According to some embodiments, if a voltage is applied to one wavelength selective element with respect to the other, a tunable bandpass filter can be fabricated.

[00152] FIGs. 4A-D are plots showing various bandpass filter characteristics, according to some embodiments. The plots in FIGs. 4A, 4B, 4C and 4D have center wavelengths at 820, 830, 840 and 850 nm, respectively where "R" is the reflectivity. At the center wavelength with a bandwidth of 10 nm for example, the reflectivity is practically nil and most of the light is transmitted, while outside the bandwidth, the reflectivity is almost 100% and transmission is practically nil.

[00153] FIG. 5 is a diagram showing a coarse wavelength division multiplexing (CWDM) configuration, according to some embodiments. In this case, four wavelengths propagate within a transmission medium, such as a multimode optical fiber with center wavelengths of 820, 830,840 and 850 nm each with a modulated data rate of 25 Gb/s for an aggregated data rate of 100 Gb/s. The optical bands are separated by the bandpass filter on the MS-PD/APDs 530, 532, 534 and 536 by reflecting off each wavelength selective MS-PD/APD. After each reflection, the light is reflected to the next wavelength selective MS-PD/APD via reflector 550 and so on, until all the optical bands are absorbed by the designated MS-PD/APD. Each center wavelength carries a data channel, for example 820 nm carries data channel 1 at a data rate of 25 Gb/s and the MS-PD 530 with bandpass filter at 820 nm separates the 820 nm signal from the rest of the optical signals and generates restored Data Channel 1 for further signal processing by an integrated CMOS ASIC (not shown).

[00154] According to some embodiments, the MS-PD/APD epitaxial layer thickness is compatible with the epitaxial layer thickness and structure of CMOS (Complementary metal–oxide–semiconductor) processes and therefore can be integrated with a CMOS ASIC. In contrast, a conventional silicon photodiode at 850 nm with a data rate of 1.25 Gb/s has an epitaxial layer greater than 10 μm thickness and a 53% quantum efficiency. Thus the relatively thick layers of conventional silicon photodiodes are not easily compatible with CMOS processing.

[00155] According to some embodiments, the light absorbing layer can be non crystalline. In particular, it can be hydrogenated amorphous Si (a-Si:H) deposited,

for example, by plasma enhanced chemical vapor deposition (PECVD) and/or hot wire chemical vapor deposition (HWCVD). The layer typically is the order of 0.3-3 μm thickness. A voltage is applied across the light absorbing region (or i region of a pin photodiode structure) in reverse bias to sweep out the photogenerated carriers to enable high efficiency and high bandwidth for high speed data communication applications. The layer on top of the non crystalline layer can be a transparent or semitransparent conducting metal or conducting oxide such as indium tin oxide. The top layer can be a thin layer of doped non crystalline material to form a pin structure.

[00156] FIGs. 6A and 6B are diagrams showing some basic parts of a microstructured photodiode, according to some embodiments. FIG. 6A shows material structure 600 prior to etching a microstructure and FIG. 6B shows the MS-PD 660 after etching. Note that according to some embodiments the microstructures are holes 622, and in some other embodiments the microstructures are pillars. In some other embodiments the microstructures are a combination of holes and pillars. The "Ia" layer 608 can be non-crystalline (e.g. hydrogenated amorphous Si (a-Si:H)) grown on crystalline or non-crystalline N layer. The P layer 610 can be non-crystalline and highly doped P or a conductive oxide or metal. The N layer 606 can also be a metal or conductive oxide. A bias is applied between the P and N layers using ohmic contacts 628 and 630 to create a high field in the I layer 608 that sweeps out the photogenerated carriers. The substrate 602 can be non-crystalline and/or dielectric such as quartz, glass, ceramic and/or conductor such as metal, silicide, conductive polymer for example. According to some embodiments, the "Ia" also known as "i" layer 608 can have a thickness range of 0.3 to 3 micrometers.

[00157] FIGs. 7A and 7B are diagrams showing some basic parts of a bottom illuminated photodiode, according to some embodiments. FIG. 7A shows material structure 700 prior to etching microstructure and FIG. 7B shows bottom illuminated MS-PD 760 after etching microstructures (such as holes 722). For a bottom illuminated PD/APD, the "Ia" or "I" region 708 can be non-crystalline such as a-Si:H and the "N" layer 710 can also be non-crystalline whereas the "P" layer 706 can either be crystalline or non-crystalline on BOX/SOI 704 and crystalline or non-crystalline substrate 702. However to minimize optical losses, it is desirable that

the substrate 702 and the P layer 706 are crystalline since it is less absorbing than amorphous silicon at wavelengths from 800 to 1100 nm range. For a "double or multiple bounce" PD/APD the absorption region "Ia" layer 708 can have a thickness range of 0.2 to 2 micrometers since the optical signal will reflect off the N metal contact 726 and back into the "Ia" absorbing layer 708. The "Ia" layer 708 thickness can be reduced and therefore reduce the transit time and increase the bandwidth of the photodiode or avalanche photodiode.

[00158] FIGs. 8A and 8B are diagrams showing some basic parts of an MS-APD structure, according to some embodiments. FIG. 8A shows material structure 800 prior to etching a microstructure and FIG. 8B shows MS-APD 860 after etching. The "Ia" region 808 for light absorption can be crystalline or non-crystalline such as a-Si:H. A crystalline avalanche gain region of PIN silicon (820, 818 and 806) is grown on silicon substrate or a BOX/SOI (buried oxide/silicon on insulator) substrate 802. The Pa top layer 810 can be crystalline or non-crystalline. A transparent metal oxide layer 826 can be provided to form an ohmic contact with P Si layer 810 and or to reduce the sheet resistance. Note that the optical signal can come straight on (perpendicular) to the upper surface or it can come from an angle, as shown by the photon arrows. The microstructures 822 can be holes, pillars or a combination of the two. Shown in FIG. 8B is a top illuminated APD 860, however according to some embodiments, using BOX/SOI the bulk of the substrate can be removed and the APD can be illuminated from the bottom at wavelength ranges of 800-1100 nm. A reverse bias is applied between P ohmic and bond metal 828 through the P layer 810 and N ohmic and bond metal 830 through N substrate 806. The reverse bias both sweeps out the photogenerated carriers and provides electronic gain. Typical bias voltages for PD are 1 to 10 volts reverse bias and for APD the range is 5 to 50 volts reverse bias approximately. As in all PIN, PIPIN devices described herein, the P and N can be interchanged for example PIN can be NIP and PIPIN can be NINIP for photodiodes and avalanche photodiodes. The anode or p layer is biased negatively with respect to the cathode N layer.

[00159] FIGs. 9A and 9B are diagrams showing aspects of a selective area growth (SAG) APD structure before and after SAG of III-V or Ge material, according to some embodiments. FIG. 9A shows a Si APD structure with etched holes 922 (or the area around pillars). Selective area growth (SAG) epitaxial growth

of III-V material or Ge can be performed, as shown in FIG. 9B where Pa layer 910 and Ia layer 908 can be non-crystalline such as a-Si:H or it can be crystalline silicon. In particular, the I area 934 of the microstructures can be InGaAs or Ge, and the P area 932 can be InGaAs. According to some embodiments, starting with a PD structure, with the avalanche gain layers (P layer 920 and I layer 918) removed, a SAG PD with InGaAs or Ge can be fabricated. Other materials may also be used in SAG such as GaN, ZnSe, InP, GaAs. According to some embodiments, other amorphous semiconductors may also be used such as amorphous Ge. According to some embodiments, amorphous silicon can be used due to its higher absorption coefficient than crystalline silicon of photons with energies above the indirect bandgap.

[00160] FIG. 10 is a diagram showing a simplified microstructured silicon photodiode with PIN epitaxial layers, according to some embodiments. Holes 1022 are etched to the buried oxide layer (BOX) 1004 which can be 0.2 to 10 micrometers thick. This structure 1060 offers a high contrast in refractive index between the silicon and the silicon dioxide that can result in absorption enhancement. The I layer 1008 can be in the range of 0.5 to 5 micrometers in thickness and the P layer 1010 and N layer 1006 can be in the range of 0.1 to 5 micrometers in thickness. The enhance absorption can be greater than 50% in the wavelength region of 800 to 900 nm or more. The enhanced absorption can be optimized for certain wavelength ranges of the optical signal, which is generated by directly modulating a laser such as a vertical cavity surface emitting laser or indirectly modulation where an optical modulator modulate the laser light. The modulated laser light at Gb/s rate is the optical signal. The optical signal impinges onto the microstructured photodiode 1060 either at normal incidence or at an angle to normal incidence. Reverse bias is applied between the P ohmic contact, anode 1028 and N ohmic contact cathode 1030 for high speed operation of the microstructured photodiode 1060. Not shown is a passivation layer on the silicon surfaces of 10 to 100 nm thickness for example grown by wet (steam) or dry oxidation of Si, atomic layer deposition of silicon dioxide, chemical vapor deposition, in order to reduce dangling bonds that results in surface recombination.

[00161] FIG. 11 is a diagram showing a simplified microstructured silicon photodiode with PIN epitaxial layers, according to some embodiments. MS-PD

1160 is identical to MS-PD 1060 except that the microstructured holes 1122 are not etched fully through to the BOX layer 1004. According to some embodiments, 0.01 to 2 micrometers of N layer 1006 can be left.

[00162] FIGs. 12A-C show aspects of a simulation using finite difference time domain (FDTD) of Maxwell propagation equations method of a particular microstructured hole pattern, according to some embodiments. FIG. 12A shows a hexagonal hole pattern with center to center spacing of the holes of 495 nm in the x direction and 860 nm in the y direction. As shown in FIG. 12B, the holes are completely etched through to a depth of 2 micrometers with hole diameter of 385 nm on top and 430 nm on bottom. FIG. 12C is a plot showing results of the simulation that used a finite difference time domain technique. Curves 1210, 1212 and 1214 show absorption, reflectance and transmittance, respectively. It can be seen that with a thickness of 2 micrometers of silicon, more than 60 percent of the light with wavelength range from 805 to 830 nm can be absorbed in this particular example. By varying the hole diameter, spacing and depth of etch, the absorption can be optimized for particular wavelengths of the optical signal. According to some embodiments, hole diameters can be varied from 200 to 1800 nm, spacing can vary from 200 to 3500 nm, and depths can vary from 0.1 to 20 micrometers.

[00163] FIG. 13 is a diagram showing an epitaxial layer structure for a high contrast microstructured photodiode (PD) with a P-I-N doping, according to some embodiments. Starting with a BOX (buried oxide) 1304 in Si 1302 where the oxide layer thickness range from 0.1 to 10 microns or more, a thin Ge buffer layer 1370 can be grown on top of the N Si 1302. With or without the Ge buffer layer 1370, subsequent N, I, P layers 1306, 1308 and 1310 can be Ge and/or III-V material family such as InGaAs, InP, InGaAsP, GaAs, AlGaAs, GaN, InGaN, AlGaN. If the N, I, P layers 1306, 1308 and 1310 are Si, then the Ge buffer layer 1370 may be omitted. For high speed operation of the PD, the N layer 1306 can range from 0.1 to 5 microns, the I layer 1308 can range in thickness from 0.2 to 3 microns, and the P layer 1310 can range from 0.1 to 2 microns. The final layer, in this example, the P layer 1310 can be a combination of layers, such as a P layer with InP with a capping of a thin InGaAs.

[00164] FIG. 14 is a diagram showing an epitaxial layer structure for a high contrast microstructured photodiode (PD) with a P-I-N doping, according to some

embodiments. The PIN heterogeneous structure is similar to that of FIG. 13 except that Ge buffer layer 1470 can be at the interface of I layer 1408 and N layer 1406, or thereabout, where I layer 1408 and P layer 1410 can be Ge and/or III-V material family. The advantage of this structure example is that for photon energies less than the bandgap of Si, less electron hole pairs are generated in the N layer 1406 where the photogenerated carriers can diffuse to the high field region in the I layer 1408, resulting in a slow component in the high speed response of the PD. The Ge buffer layer may also not be necessary for the heterogeneous growth.

[00165] FIG. 15 is a diagram showing an epitaxial layer structure for a high contrast microstructured photodiode (PD) with a P-I-N doping, according to some embodiments. The PIN heterogeneous structure is similar to that of FIGs. 13 and 14 except that only the I region 1508 is a lower bandgap material, such as Ge and/or III-V material family such as InGaAs, InSb, InGaAsP, InAs. Both the P layer 1510 and N layer 1506 are made of a higher bandgap material. According to some embodiments, the P layer 1510 and N layer 1506 have bandgap energies higher than the photon energy and the I layer 1508 has a bandgap energy that is lower or equal to the photon energy. For example, the N layer 1506 can be Si, the I layer 1508 can be InGaAs and/or Ge, and the P layer 1510 can be Si and/or InP. The Ge buffer layer may or may not be necessary for the heterogenous growth. The advantage of having higher bandgap material in the P and N region is to minimize photocarriers generated in those regions. Photocarriers generated in the P and N regions can diffuse to the high field region, resulting in a relatively slow component in the response of the photodiode to short optical pulses. Reducing the photocarriers generated in the P and N regions thus reduce the “tail effect” - the fall time of the electrical pulse output of the PD in response to an optical input pulse or set of pulses as in a bit stream for transmitting data optically. High doping of the P and N region also reduces the minority carrier lifetime such that photocarriers generated in these regions can recombine before diffusing to the high field “I” region.

[00166] FIG. 16 is a diagram showing some aspects of fabrication of a high contrast microstructured photodiode (PD), according to some embodiments. The example structure depicted in FIG. 13 is shown with holes 1622 etched through the PIN layers 1310, 1308 and 1306 all the way to the oxide layer 1304 buried in

silicon layer 1302. Dry and/or wet etch can be used, a passivation layer can be added to the exposed surfaces by atomic layer deposition. In this example, the Ge buffer layer 1370 is at the interface of N layer 1306 and Si layer 1302. According to some embodiments, similar fabrication methods are used for the structures shown in FIGs. 14 and 15.

[00167] FIGs. 17A-D are diagrams showing examples of the hole arrangements, spacing, size, and passivation layers, according to some embodiments. FIG. 17A shows a hexagonal layout with a spacing of 280 nm and a passivation layer thickness of 50 nm. FIG. 17B shows a square layout. FIGs. 17C and 17D show tapered and vertical hole profiles, respectively. The examples shown are for Silicon, but with small modification of the dimensions, the techniques are also applicable to Ge and the III-V material family. The hole can have circular cross sections or according to some embodiments, other shapes such as oval, rectangular, for example can be implemented.

[00168] FIG. 18 is a diagram showing some further aspects of fabrication of a high contrast microstructured photodiode (PD), according to some embodiments. The example structure depicted in FIGs. 13 and 16 is shown after the microstructured holes 1622 are etched, and the P ohmic contact layer 1828 is deposited and annealed.

[00169] FIG. 19 is a diagram showing some further aspects of fabrication of a high contrast microstructured photodiode (PD), according to some embodiments. The example structure depicted in FIGs. 13, 16 and 18 is shown. After P ohmic metal 1828 is deposited and annealed, a mesa can be etched, removing material 1972, to define the capacitance of the PD. The diameter of the mesa can range from 5 microns to over 100 microns depending on the RC time that is desired for the PD. Passivation of the exposed P, I and N regions is performed to minimize leakage current due to dangling bonds for example. According to some embodiments, ion implantation such as proton bombardment can also be used in place of mesa etching to define the capacitance of the PIN structure by generating an electrically semi-insulating or insulating region.

[00170] FIG. 20 is a diagram showing some further aspects of fabrication of a high contrast microstructured photodiode (PD), according to some embodiments. The example structures depicted in FIGs. 13, 16, 18 and 19 are shown. After the

mesa etch, a ring or partial ring-shaped N ohmic contact 2030 is formed on the N layer 1306. Additional processing steps to complete the PD are not shown, such as forming an insulating layer from a material such as polyimide so that a bridging path is formed for connecting metallization from the P ohmic contact 1828 to a bond pad (also not shown) for applying an electrical bias to the P region 1310. Also, connecting metal between the N ohmic contact 2030 and an N bond pad is not shown for simplicity. A reverse electrical bias is applied to the P and N ohmic contacts 1828 and 2030 to create a high field in the I layer 1308. According to some embodiments, voltages of negative 1 to negative 10 volts can be applied.

[00171] FIG. 21 is a diagram showing some aspects of a lossy high contrast microstructured photodiode (PD), according to some embodiments. FIG. 21 shows a microstructured PD with the light transiting twice in the absorbing layer 1308. This is achieved by removing a portion 2174 of the Si substrate 1302 to the oxide layer 1304 and coating the oxide with a metallic reflector 2176, such as Au, Ag, Al, or Cu. According to some embodiments, a Bragg reflector can be configured for either broadband or wavelength selectivity. According to some embodiments, a Bragg layer can also be included on the upper surface of P layer 1310 to further provide wavelength selectivity especially for use in coarse wavelength division multiplexing, or wavelength division multiplexing.

[00172] FIGs. 22A and 22B show aspects of a simulation using FDTD method of a particular microstructured PD, according to some embodiments. FIG. 22B is a plot showing results of a simulation of the absorption of the photons versus wavelength of the photons for a double bounce structure as depicted in FIG. 21. The following example thicknesses were used in the simulation: oxide 1304 is 2 microns; P silicon 1310 is 300 nm, I Si 1308 is 2 microns, and N silicon 1302 is 300 nm, the reflector 2176 is Au of 100 nm thickness. A hexagonal microstructured hole is assumed as shown in FIG. 22A. The holes are 600 nm center-to-center hexagonal period, 480 nm hole diameter and 30 nm of SiO2 passivation as shown in FIG 22A. These dimensions are just one example for the microstructured holes with the corresponding simulation of its absorption characteristics versus wavelength. The absorption was found to be significantly higher than in the case of Si without microstructured holes, as can be seen from curves 2210 (absorption)

and 2212 (reflection) of FIG. 22B. In the vicinity of 850 nm wavelength the absorption is better than 70% for example.

[00173] FIG. 23 is a diagram showing aspects of a high contrast microstructured PD, according to some embodiments. The lower structure is similar to the structure of FIG. 20: Si substrate 2302, SiO2 layer 2304, and Si N layer 2306. A lower Si I layer 2308 can also be provided. In this case, Ge is used as an upper I layer 2309 and the P layer 2310. The P layer 2310 can also be made of InP, which can be grown on the Ge I layer 2309. The advantage of an InP P layer 2310 is that it is less absorbing at wavelengths from 0.9 to 2 micrometers. The P layer 2310 can also be made of GaAs grown on Ge I layer 2309. Also shown are microstructure holes 2322, P ohmic contact 2328 and N ohmic contact 2330. Note that light can impinge on the upper surface of P layer 2310 and/or on the Si substrate surface 2302.

[00174] FIG. 24 is a diagram showing aspects of a heterogeneous epitaxial microstructured PD, according to some embodiments. In this case, the I region can be a composite of Si (lower I layer 2408) and InGaAs (upper I layer 2409) separated by Ge layer 2470. The P region 2410 is InP. According to some embodiments, the I region can also be entirely InGaAs grown on a thin layer of buffer Ge layer 2470. Also shown are Si substrate 2402, oxide layer 2404, N layer 2408, microstructure holes 2422, P ohmic contact 2428 and N ohmic contact 2430. This is an example of a high contrast Microstructured PD structure. It can also incorporate a metal reflector as in FIG. 21 where the Si is removed by etching below the PD to the oxide layer and Au, Ag, Al or Cu metal layers can be deposited to reflect the light back toward the I absorbing layer. Bragg reflectors can also be used as described above. Light comes from the P layer side in this example. Light can also come from the Si substrate side, in which case, a reflector is placed on the P layer surface for a double transit through the I layer. Advantages of such arrangements includes keeping the I layer thickness unchanged from that of a single pass, while the absorption is greatly improved by transiting the absorption region twice or more. By reducing the absorption region thickness to, for example, half that of a single pass PD, the speed of the PD increases since the transit time for the photogenerated carriers have to traverse only half the distance of a single pass PD. High contrast microstructure refers to the refractive index difference

between the microstructure and the space or atmosphere at one surface interface and the SiO2 and or the bulk semiconductor material at another surface interface. Light interact with the microstructures in a complex manner of coupled eigen cells or resonantor cells where each hexagonal or square cell in the lattice can be considered as an individual resonator that is coupled to its adjacent cell or resonator in addition to linear and nonlinear optical field enhancements that may occur. If there are no or very little optical losses, the coupled resonator structures can have a high Q (quality factor of a resonator) or, in other words, light can bounce back and forth in the microstructure over 10^4 to over 10^6 times before damping out for example. However with optical loss such as due to weak absorption, the Q may be low and light may bounce back and forth in the microstructure less than 100 times, or even less than 20-30 times. The microstructures in the PD/APD are low Q high contrast stuctures or lossy high contrast structures with the Q of each cell coupled to adjacent cells.

[00175] FIG. 25 shows a high contrast structure for an optical emitter such as a light emittting diode (LED) or a vertical surface emitting laser (VCSEL), according to some embodiments. Optical emitter 2500 is a heterogeneous epitaxial layer structure. Si layer 2506 is formed on Si substrate 2502 and BOX/SiO2 layer 2504. A buffer Ge layer 2570 can be grown on Si layer 2506 followed layer 2510, which can be InAs quantum dots 2572, cladded by GaAs and AlGaAs. In addition, a simple Si PIN microstructure where the “I” layer can be thin of approximately 1000 nm or less and where the structure in forward bias, can be a photon emitter.

[00176] FIG. 26 shows, for example, the basic structure for a high contrast 1.3 micron wavelength photo emitter (PE), according to some embodiments. An active layer for 1.3 micron wavelength emitter is formed usingan InAs quantum dot layer 2570 (shown in FIG. 25) or 2670 in Fig. 26, sandwiched by GaAs P layer 2604 and N layer 2606 which in turn is sandwiched by AlGaAS P layer 2608 and N layer 2602, and a P GaAs capping layer 2610 as the final layer. Typical thickness can be found in the literature. See, e.g. AY Liu, S Srinivasan, J Norman, AC Gossard, JE Bowers, Quantum Dot Lasers For Silicon Photonics, Photonics Research 3 (5), B1-B9 (2015), which is incorporated by reference herein. In addition there can be multiple layers of quantum dots and/or cladding layers. The microstructures can be designed such that the standing wave peak is positioned at one or more of the QD

layers to optimize the gain and optical field overlap. For MS-PD/APD, the length of the microstructure can also be such that at a particular wavelength, an integer number of wavelengths is in a round trip to optimize the absorption enhancement at that particular wavelength for example. In addition a single microstructure for example a single hole can also have enhancement of absorption or emission for either PE or MS-PD/APD over than of a similar structure without any microstructures.

[00177] FIG. 27 is a diagram showing some basic features of a high contrast microstructured photo emitter (PE) structure with etched holes, according to some embodiments. The material structure is similar to that of PE 2500 shown in FIG. 25. Microstructure holes 2722 are etched into active layer 2510. Using P and N ohmic contacts 2728 abd 2730, the device 2700 is biased in a forward bias, P positive in respect to N, to generate photons from the active layer 2510 comprising in this example of InAs quantum dots 2572 at a wavelength of 1.3 microns. Other active layers, cladding layers can be used to generate light at other wavelengths, from visible to infrared. Depending on the wavelength of light, light can be emitted from the top surface and/or the bottom surface through the oxide layer 2504. The advantage of a microstructured high contrast photon emitter is that the photons interact with the active layer and/or the gain layer in the case of a laser longer since the high contrast structure can have very high Q, with Q ranging from 10^3 to over a million since the structures have very little optical loss and the quantum dots provide optical gain. The high contrast low loss microstructured photo emitter can operate as a LED, as a VCSEL and/or a laser and/or a super-radiant LED. The PE is forward biased with the anode, 2728 is the P ohmic, or P layer at a positive voltage with respect to the cathode, 2730 that is the N ohmic, or N layer.

[00178] FIG. 28 is a diagram showing some aspects of a PE according some other embodiments. PE 2800 is similar to PE 2700 shown in FIG. 27 except that a portion 2874 of the substrate 2502 is removed underneath the light emitting region to the oxide layer 2504. A reflector, metal and/or Bragg such as distributed Bragg reflector (DBR) 2876 is formed on the oxide layer to reflect light generated in the active layer back toward the P layer 2510 surface. According to some embodiments, device 2800 operates in an LED mode and/or in a laser mode.

[00179] FIG. 29 is a diagram showing some aspects of a PE, according to some embodiments. PE 2900 is similar to PE 2800 of FIG. 28, except that in includes a reflector 2928, which can be metal and also can act as a P ohmic contact, if desired. According to some embodiments, a separate P ohmic can be provided. The reflector 2928 also can be a distributed Bragg reflector and/or partially metal and partially DBR. Light is emitted from the lower surface of oxide layer 2504 and through the substrate 2502 where a portion 2874 has been removed. The photo emitter 2900 can operate in LED and/or a laser mode such as VCSEL mode. According to some embodiments, the photo emitter 2900 can operate in an edge mode, where light is emitted in the plane of the active layer rather than perpendicular to it, with or without mirrors such as DBR or metal along the emitting edges.

[00180] FIG. 30 is a diagram showing some aspects of a PE, according to some other embodiments. PE 3000 is similar to PE 2900 of FIG. 29, but is configured as a VCSEL (vertical cavity surface emitting laser). PE 3000 is heterogeneous epitaxially grown on Si with high contrast microstructured holes (or pillars). Note that only the very basic components are shown for simplicity. The high contrast structure can be sandwiched by reflectors 2928 and 3076. The P layer 2510 can be a DBR grown by semiconductor epitaxy and followed by P ohmic metallization layer 2928. According to some embodiments, the DBR can be formed from conductive oxides or non-conducting oxides, with either the P metal on the DBR and/or on the side as in Fig. 28 . The mirror 3076 on the bottom side of oxide layer 2504 can be metal and/or DBR of dielectric layers of different refractive index. Light output as shown is from the bottom, but can also be from the top.

[00181] FIG. 31 is a diagram showing some aspects of a Simple PIN photodiode structure, according to some embodiments. To minimize diffusion current due to photocarriers generated in the regions outside the high field region, the “I” layer 3108, the P and N layers 3110 and 3106 are highly doped and/or doped degenerately to reduce minority carrier lifetime. N and P doping can range from $1x10^{18}$ to $8x10^{21}/cm^3$ or more. I layer 3108 is not intentionally doped and can be less than $5x10^{16}/cm^3$. Also shown is an oxide layer 3104 and a Si substrate 3102. As in earlier examples, with or without the addition of a Ge buffer layer, Ge and/or III-V materials can be grown and the P and N layers can also be highly doped

and/or doped degenerately. The doping need not be uniform and can have a gradation, for example where the doping is reduced in the P or N layer near the "I" layer interface to minimize diffusion of dopants into the "I" layer during epitaxial growth.

[00182] By reducing minority carrier lifetime in the P and N layers, photogenerated carriers in these layers can recombine before diffusing and/or drifting into the high field "I" where the electrons and/or holes can contribute to a photocurrent that can result in a degradation of the photodiode modulated frequency response. Therefore, it is beneficial to minimize photocurrent contributions due to carriers generated outside the high field region.

[00183] Other methods of reducing minority carrier lifetime include introducing defects, such as via ion implantation partially and/or entirely in the P and/or N regions. The introduced ions can be inert ions, and/or active ions with partial, full or no thermal annealing. In addition, the microstructured holes (and/or pillars) can be with or without partial passivation, such that the surface states in the low field regions of N and P layers can act as carrier sinks whereas in the high field regions of the "I" layer, the carriers are swept out rapidly. Passivation can also be selective, on the "I" layer predominately.

[00184] FIG. 32 is a diagram showing aspects of MS-PD fabrication, according to some embodiments. The starting material structure can be such as depicted in structure 3100 of FIG. 31. A simple NIP (N and P can be interchanged for a PIN) microstructured photodiode is shown where holes 3222 are etched to the top of P layer 3106. The purpose is to passivate the N and "I" layer walls, and not passivate the P layer walls to thereby reduce the lifetime of minority carriers in the P layers that are generated by the light with wavelengths from 780 to 980 nm for example. Surface states on the un-passivated P walls can act as a potential sink for minority carriers where they are recombined.

[00185] FIG. 33 is a diagram showing aspects of MS-PD fabrication, according to some embodiments. Passivation of the side walls of the holes 3222 of the N and "I" layers is shown resulting in passivation layer 3324. The passivation can be carried out using thermal oxidation and/or atomic layer deposition of SiO2. Thermal oxides 3324 of 5-50 nm thick can be grown on the side walls for example. Other thicknesses can also be grown. After thermal oxidation, etching the holes can be

continued to etch through the P layer 3106 to the SiO2 layer 3104, for example. Not all processing steps are shown, for example, the N layer can be protected by thermal oxide, not shown, during the continuation of the hole etch.

[00186] FIG. 34 is a diagram showing aspects of MS-PD fabrication, according to some embodiments. After passivation, the holes 3222 are further etched as shown by area 3422. Note that the N and P layers can be interchanged so that instead of the NIP structure as shown in this example it can also be a PIN structure. The holes 3222 can be etched to the SiO2 layer 3104 and/or they can be etched only partially through the P layer 3106 so that a thin P layer remains. The sides of the holes 3222 within the P layer 3106 are not passivated in this example to allow the surface states to pull any minority carriers generated by the light toward its potential sink and result in recombination. According to some embodiments, the P layer 3106 can also be passivated and/or partially passivated. Since layer 3106 can also be heavily doped, the minority carrier lifetime may be in the 10s of picosecond or less.

[00187] FIG. 35 is a diagram showing aspects of a MS-PD, according to some embodiments. The microstructured NIP photodiode 3560 has microstructure holes 3222 with passivated sidewalls of the N and "I" layers, but not passivated sidewalls of the P layer. Ohmic contacts 3528 and 3530 to the N and P layers respectively are added to provide a reverse bias for high-speed operation of the photodiode 3560. Light impinging on the N side of the photodiode is either normal and/or off normal to the N layer plane.

[00188] FIG. 36 is a diagram showing aspects of a MS-PD, according to some embodiments. The microstructured hole photodiode 3660 has Si NIP layers where passivation is partially on the sidewalls similar to PD 3560 shown in FIG. 35. With PD 3660, however, light comes in via an optical fiber 3680 from the Si substrate side where a via 3672 is etched to allow a self-aligning process where the fiber 3680 with or without a lens 3682 is guided along the via 3672 to the correct position for optimal coupling of light into the microstructured photodiode 3660. A dielectric layer 3676 of 0.1-10 micrometer thickness approximately can be positioned on the N layer 3110 over the holes 3222. On top of the dielectric layer 3676 can be a metal reflector 3678 such as Ag or Au (or any other suitable metal or alloy, such as Al, Ni, Cr, for example) and/or a dielectric stack such as a Bragg

Reflector (BR), to reflect the light back toward the absorbing "I" layer 3108. An anti-reflective coating 3674 can also be provided. Also as in earlier examples, Ge and/or III-V materials can also be grown with or without the addition of a Ge buffer layer.

[00189] FIG. 37 is a diagram showing a technique to reduce minority carrier lifetime, according to some embodiments. In this case, surface and bulk recombination is used rather than passivating or partial passivating hole surfaces. A high doping of greater than $10^{20}/cm^3$ can reduce the diffusion length to less than 0.1 micrometer (Auger recombination) for example. In addition, ion implantation is used to introduce defects 3770 and 3772 in layers 3710 and 3706. The defects in the semiconductor can also cause reduced lifetimes via the Shockley-Read-Hall recombination process. Ions such as Xe, Bi, Ti, Cr, Ar, N, to name a few can be implanted into the N and/or P layers. Contrary to known structures where long minority carrier lifetimes are desirable for device operation, the described techniques introduce defects either by epitaxial growth and/or ion implantation of metal, non-metal and inert ions to increase the recombination rate due to Shockley-Read-Hall effects. Deep and/or shallow traps can be created due to the defects that can result in short lifetimes of the minority carriers. The short lifetime of minority carriers is desirable in the P and N regions to minimize the contribution of diffusion currents that find their way to the high field region "I" layer that can contribute to the photocurrent. These "slow" diffusion currents that diffuse and/or drift into the "I" region can cause degradation of the time response of the photodiode by contributing a slow component to the photocurrent-time response characteristic of the photodiode.

[00190] FIGs. 38A-38C describe various parameters for microstructured photodiodes that were simulated. FIG. 38A shows a hexagonal hole pattern having a distance "d" between the hole centers. FIG. 38B shows a square hole pattern having distance "d" between the hole centers. FIG. 38C is a table of parameters used for the simulation using FDTD method. It was found that absorption of greater than 90% can be accomplished with a 2 micrometer thick silicon layer on SiO2 layer of 2-2.5 micrometers thick, with holes ranging from 1300 to 1500 nm in diameter and with a period of 2000 nm in a hexagonal lattice of holes for wavelengths of the optical signal ranging from 850 to 950 nm and to 980

nm for example. In addition, wavelengths can range from 750-1000nm. Hole diameters can be subwavelength to greater than a wavelength of the incident optical signal, ranging from 100 to 3000 nm in diameter. Thickness of the Si absorbing layer can range from 0.3 to 10 micrometers. The SiO2 layer can range from 0.2 to 10 micrometers. According to some embodiments, a mixture of hole diameters can also be used to optimize the absorption of the incident photons.

[00191] FIG. 39 is a graph plotting simulation results of microstructured hole photodiodes using FDTD for absorption verses wavelength. The photodiode absorption "I" layer was 2 micrometers thick, with hole diameters ranging from 1000 to 1500 nm. Incident energy wavelengths ranged from 850 to 950 nm. Three curves 3910, 3912 and 3914 plot the absorption for hole diameters of 1000 nm, 1300 nm and 1500 nm respectively. The simulations show that with hole diameter of 1500 nm, greater than 90% absorption is achieved over a wavelength range of 850-870 nm and with a hole diameter of 1300nm, absorption of greater than 80% can be achieved over a wavelength range of 875 to 950 nm with a hexagonal lattice of holes with a period of 2000 nm. The 2 micrometer Si is on top of a 2-2.5 micrometer SiO_2 layer. As can be seen, having a hole diameter larger than the incident wavelength can be used to enhance the absorption over that of a comventional silicon layer without any features.

[00192] FIG. 40 is a diagram showing a microstructured avalanche photodiode (APD) with a P-I-P-I-N epitaxial structure, according to some embodiments. In the case of FIG. 40 all the layers of APD 4060 are silicon for optical communication wavelength ranging from 780 to 1000 nm for example. The APD 4060 can also operate in the visible wavlength range. Data rates can range from 100 Mb/s to 50 Gb/s or more. A reverse bias voltage is applied between the P and N ohmic contacts 4028 and 4030 with voltage range of -4 to -50 volts. Avalanche microstructured photodiode 4060 can have the following doping and thicknesses: P layer 4010, doping > $1x10^{19}$ /cm^3, thickness 0.1-1.0 μm; I layer 4008, doping < $1x10^{16}$/cm^3, thickness 0.5-3 μm; P layer 4020, doping 1-$3x10^{17}$/cm^3, thickness 0.1-0.5 μm; I layer 4018, doping < $1x10^{16}$/cm^3, thickness 0.3-1 μm; and N layer 4006, doping > $1x10^{19}$/cm^3, thickness 0.5-3 μm for example. According to some embodiments, the top two layers 4010 and 4008 can also be Ge instead of Si. The

holes 4022 can be etched partially through the APD layers or completely to the SiO_2 layer 4004 as shown in FIG. 40.

[00193] As in the case of microstructured photodiodes, for APDs the optical signal can impinge from the front side (epitaxial layer side) or the backside (substrate side). Additionally, with a via in the substrate, a reflector can be deposited on the SiO2 resulting in a double or multiple bounce of the optical signal within the APD structure. According to some embodiments, the P and N can be interchanged resulting in a N-I-N-I-P microstructured APD.

[00194] FIG. 41 is a diagram showing a microstructured avalanche photodiode (APD) with a P-I-P-I-N epitaxial structure, according to some other embodiments. The APD 4160 is identical to APD 4060 depicted in FIG. 40, except that the holes 4122 (or pillars) are partially etched. In the example shown in FIG. 41, the holes 4122 are partially etched into the P layer 4020 and/or stop at the P layer 4020. According to some other embodiments, the holes 4122 can be partially etched into the I absorption layer 4008.

[00195] FIG. 42 is a diagram showing a microstructured APD with a Ge absorption layer and Ge P capping layer, according to some embodiments. The APD 4260 is similar or identical to APD 4060 depicted in FIG. 40 except that the two upper layers, 4210 and 4208 are Ge instead of Si. The APD 4260 can have the same doping and thicknesses ranges as described above for APD 4060 except that the P Ge layer 4210 can have a doping level greater than 1 $10^{20}/cm^3$. After the epitaxial growth of the APD structure P(Ge)-I(Ge)-P(Si)-I(Si)-N(Si) on a buried oxide (BOX) silicon substrate, the microstructures are then etched. The microstructures can be holes, pillars or a combination of the two. The etching can be made to the SiO2 layer or it can also be etched partially to a depth before reaching the SiO2 layer 4004, for example the holes can be etched to or into the P Si layer 4020. The Ge absorption layer 4208 with microstructures is expected to allow the optical signal to operate with wavelengths from 780 to 2000 nm at data rates from 100 Mb/s to 50 Gb/s or more. The optical signal can impinge from the top surface (epitaxial surface) or the bottom surface (substrate surface). With a via and a reflector deposited on the SiO2, the optical signal impinging from the top surface can be reflected back to the absorption I (Ge) layer 4208 for a second time and/or multiple times. Since there are optical refractive index differences between

the Si, Air and Ge, standing waves can be established and the thickness of the structure can be optimized to have the absorbing layer at the peak intensity of a standing wave(s) also known as stationary waves or eigen modes. In addition, at wavelengths where Si is transparent, a microlens can be etched into the Si substrate to assist in coupling of the optical signal into the APD from the bottom surface. SiO2 and a reflector can also be placed on the P (Ge) 4210 surface to reflect the optical signal that impinges from the bottom back to the absorbing I (Ge) layer 4208. Reverse bias voltages are applied between the P and N ohmic contacts 4028 and 4030 ranging from -4 to -50 volts.

[00196] FIGs. 43A through 43D show polarization sensitivity of the microstructured photodiode and APD, according to some embodiments. FIG. 43A shows the geometry used for the simulation. The holes are symmetric in size and period; the electric field polarization of the optical signal either along B or A shows less than 5% difference in the absorption characteristic of the MS-PD/APD. Absorption is equal to the incident light minus the transmission and reflection of the light, and the quantum efficiency is directly proportional to the absorption. In cases where the dimensions of the hole dimensions “a” and “b” are not the same, the MS-PD/APD shows polarization sensitivity. In FIG. 43B, curve 4310 plots absorption vs wavelength where the “a” and “b” dimensions are both equal to 1000 nm. The absorption characteristic show less than 5% difference. FIG. 43C shows results for the case where a=1300 nm and b=870 nm. The curves 4320 and 4322 show that the difference in absorption value with polarization along A or B can be seen by as much as 2 times. FIG. 43D shows results for the case where a=1500 nm and b=650 nm. The curves 4330 and 4332 show that absorption differences due to polarization orientation can also be as much as 2 times. With further dimensional changes in both “a”, “b”, A and B, absorption differences due to polarization orientation can be 10 to 100 times different, or more. Both polarization “insensitive” (with absorption changes due to polarization orientation less than 5%) and polarization sensitive (with absorption changes to to polarization orientation of 10 or more times) photodiodes and APD are useful. In cases where signals are not polarization multiplexed, for example where using the same wavelength, two channels can be transmitted, one with one polarization and another that is orthogonal to the first channel. For example, each channel can transmit at 25 Gb/s

at a particular polarization at the same wavelength. At the receiver end, polarization sensitive photodetectors are used to demultiplex the signal. The aggregated data rate is 50 Gb/s at a wavelength of 850 nm. In direct modulation of a laser, the spectrum of the laser is always wider than, for example, a laser that is operating in CW mode. The spectrum can be broadened by as much as a few nanometers (e.g. 3 nm). Therefore at 850 nm, if the laser is directly modulated, the center frequency can be at 850 nm with a broadening of as much as 1.5 w nm approximately, plus or minus. In vertical cavity surface emitting lasers, lateral modes can contribute significantly to a wider spectrum due to multiple lateral modes. In multimode systems, this is desirable as it reduces mode selective losses.

[00197] FIG. 44 shows a MS-PD/APD that is integrated with a transimpedance amplifier and/or another ASIC (application specific integrated circuits) for data processing and/or routing, according to some embodiments. The process can be CMOS and/or BiCMOS. MS-PD/APD 4420 is shown electrically connected to electronics 4430 (e.g. transimpedance amplifier (TIA) and/or another ASICs) via electrical leads 4422. The components are all integrated onto a single silicon substrate 4410. One advantage for integrating the microstructured PD/APD with IC electronics is a reduction of packaging costs, where instead of two or more individual devices, a single chip is used which may also be placed directly on a circuit board without the use of a multichip ceramic carrier. Another advantage of integrating the MS-PD/APD with electronics on a single chip is potentially lower capacitance, due to the omission of relatively large bond pads connected to the ohmic contacts. Operating wavelengths range from 800-990 nm for all silicon microstructured PD/APD. Operating wavelength can be extended to 1800 nm with the addition of Ge microstructured absorbing layer. Operating at data rates of 10, 28, 56 Gb/s can be achieved singly or in an array. The data rate can also be 1, 5, 20, 25, 30, 40 Gb/s depending on the protocol and link applications. Typically high data rates over multimode fiber and/or fibers are used at distances from under 1 meter to a length of over 100 meters. Multiple fibers and array of microstructured PD/APD (MS-PD/APD) can be utilized to give an aggregated data rate of 100 to over 400 Gb/s. For example a 10 fiber channel with each fiber operating at 10 Gb/s with a 10 MS-PD/APD array integrated with IC electronics such as

transimpedance amplifiers (TIA) and/or other signal processing/routing IC electronics on a single silicon chip can have an aggregated data rate of 100 Gb/s. If each channel is at 56 Gb/s, the 10 channel can have an aggregated data rate of over 500 Gb/s.

[00198] FIG. 45 is a diagram showing some aspects of a flip chip arrangement for a MS-PD/APD integrated with a TIA and/or another signal processing IC on a single silicon chip, according to some embodiments. According to some embodiments, the TIA and/or other signal processing integrated circuits 4530 are fabricated using CMOS and/or BiCMOS processes. Solder bumps 4512 and 4514 and/or similar bump technologies are used to attach the chip 4510 to a PCB (printed circuit board) 4550. According to some embodiments, some or all of solder bumps 4512 are used to make electrical connections between chip 4510 and PCB 4550, while solder bumps 4514 are used for physical mounting and/or stabilization only since electrical connection directly between MS-PD/APD 4520 and PCB 4550 may be unnecessary. According to some embodiments, chip 4510 is attached to another chip or multichip carrier instead of PCB 4550. Packaging the chip 4510 directly onto PCB 4550 reduces the cost of packaging by as much as 80% over known prior art packaging where the PD and IC electronics are first mounted on a multichip ceramic carrier prior to placing the carrier on a PCB. In addition, an integrated optical lens 4522 can be fabricated on the silicon chip 4510 to focus the light to the MS-PD/APD 4520 from the optical fiber 4524. Note that in this arrangement, light signal enters from the substrate side of of MS-PD/APD 4520. The integrated lens 4522 on Si can be used in the case where the operating wavelength is greater than 1100 nm (e.g. 1100 nm to 1800 nm) where Ge microstructures can be used for absorption of the incoming optical signal.

[00199] FIG. 46 is a diagram showing some aspects of a flip chip arrangement for a MS-PD/APD integrated with a TIA and/or another signal processing IC on a single silicon chip, according to some other embodiments. The chip and mounting techniques are similar or identical to those depicted in and described with respect to FIG. 45. In this case, chip 4510 includes a via 4626 where most or all the silicon in the optical path to the MS-PD/APD 4520 is removed. An integrated dielectric lens 4622 is provided to collect the light and direct it on the MS-PD/APD 4520. According to some embodiments, a light pipe is used instead of lens 4622. The

sidewall of the via 4626 can be coated with dielectric and/or metal to assist in the collection of light. Anti-reflection coating can be provided on the lens 4622 to reduce any reflection of the optical signal back into the optical fiber 4524. In addition, the fiber 4524 or chip 4510 can be tilted to reduce any reflection back into the fiber 4524. The optical fiber 4524 is used to bring the optical signal from a laser source to the integrated PD/APD and IC electronic chip 4510 with data rates ranging from less than a Gb/s to greater than 60 Gb/s. According to some embodiments, data rates of approximately 1, 5, 10, 20, 28, 50, 56 Gb/s can be used. According to some embodiments, optical signal wavelengths can range from 800-990 nm for all silicon microstructured PD/APD (MS-PD/APD), and with microstructured Ge for the absorbing layer, the wavelength can be extended to 1800 nm.

[00200] FIG. 47 is a diagram showing some aspects of a flip chip arrangement for a MS-PD/APD integrated with a TIA and/or another signal processing IC on a single silicon chip, according to some other embodiments. The chip and mounting techniques are similar or identical to those depicted in and described with respect to FIGs. 45 and 46. As in FIGs. 45 and 46, a single chip 4510 contains both the optical and electronic elements. With a via 4626 in the substrate of chip 4510 to eliminate most or all of the Si in the optical path to the MS-PD/APD 4520 together with an integrated Fresnel lens 4722, the optical signal is efficiently collected from the optical fiber 4524. The collected optical signal is impinged on the MS-PD/APD 4520. According to some embodiments, instead of Fresnel lens 4722, a high contrast grating (HCG) is used. According to some embodiments, the HCG can have filtering effects so that only specific optical wavelengths can be transmitted to the MS-PD/APD while the rest is reflected. This bandpass property is useful for coarse wavelength division multiplexing (CWDM) where multiple wavelengths are used in a single fiber.

[00201] FIG. 48 is a diagram showing some aspects of a flip chip arrangement for a MS-PD/APD integrated with a TIA and/or another signal processing IC on a single silicon chip, according to some other embodiments. The chip and mounting techniques are similar or identical to those depicted in and described with respect to FIGs. 45-47. The walls of via 4626 may be coated with dielectric and/or metal to provide a light pipe for the light to impinge on the MS-PD/APD 4520. The optical

fiber 4524 can then be inserted into the via 4626 such that it provides a guide to align the fiber 4524 to the MS-PD/APD 4520 thereby simplifying the optical packing and alignment of the optical fiber to the MS-PD/APD with a cost reduction of approximately 30% or greater. According to some embodiments, the fiber 4524 may be also be tapered and/or the via 4626 may have multiple diameters such that it provides a stop for the fiber 4524. For example, a step in the via 4626 is provided such that the edge of the fiber 4524 can rest on the step, where it can be attached to the silicon. This step arrangement also provides a precise distance between the fiber and the MS-PD/APD for optimal light collection. According to some embodiments, index matching fluid, gel and/or polymer and/or dielectric bulk or thin film may be used in the via 4626, particularly in the space between the fiber 4524 and the MS-PD/APD 4520 to optimize the transfer of optical signal from the fiber to the MS-PD/APD.

[00202] As mentioned above, with light entering from the substrate side (bottom illumination) the MS-PD/APD may employ a double and/or multiple bounce of the optical signal within the MS-PD/APD. This allows the absorption layer to be made thinner while still achieving high quantum efficiency. The thinner absorption layer will also allow a faster transit time thereby allowing the MS-PD/APD to operate at a higher data rate.

[00203] FIG. 49 is a diagram showing some aspects of a flip chip arrangement for a MS-PD/APD integrated with a TIA and/or another signal processing IC on a single silicon chip, according to some other embodiments. The chip and mounting techniques are similar or identical to those depicted in and described with respect to FIGs. 45-48. In this example a ball lens 4922 is positioned within via 4626 to couple light from the optical fiber 4524 to the MS-PD/APD 4520 efficiently. The ball lens 4922 can sit in the via 4626 for alignment of the lens to the MS-PD/APD 4520.

[00204] FIG. 50 is a diagram showing some aspects of a flip chip arrangement for a MS-PD/APD integrated with a TIA and/or another signal processing IC on a single silicon chip, according to some other embodiments. The chip and mounting techniques are similar or identical to those depicted in and described with respect to FIGs. 45-49. In this example, the ball lens 5022 sits in the via 4626 where most or all of the silicon is etched away so that light travels mostly in air and/or index matching material such as fluid, gel, polymer, solid. Additionally, the via 4626 acts

as a guide and/or a stop for alignment of the optical fiber 4626 to the ball lens 5022 and in turn to the MS-PD/APD 4520.

[00205] FIG. 51 is a diagram showing some aspects of a flip chip arrangement for a MS-PD/APD integrated with a TIA and/or another signal processing IC on a single silicon chip, according to some other embodiments. The chip and mounting techniques are similar to those depicted in and described with respect to FIGs. 45-50 except that MS-PD/APD 5120 and TIA and/or other signal processing integrated circuits 5130 are mounted on or near the upper surface of silicon chip 5110. The metallic conductor conduits 5132 and 5134 can be made of Al, Cu, Mo, W, Ni, or TiN, to name a few. The conduit 5132 connects the MS-PD/APD 5120 to the IC electronics 5130. Conduit 5134 connects the IC electronics 5130 to traces on the PCB 4550 (or chip carriers) using, e.g., bump technologies, such as solder bumps for example, which allow good alignment of the chip to the PCB and/or chip carrier. According to some embodiments, other methods of using wire bonding may also be employed to connect the IC electronics to traces on the PCB and/or chip carrier. The fiber 4524 is brought to close proximity of the MS-PD/APD 5120 and the arrangement may include a ball lens on the tip of the fiber 4524, and/or a ball lens between the fiber and the MS-PD/APD. Other light focussing elements such as gratings, Fresnel lens, to name a few, may also be used, such as described with respect to FIGs. 45-50. According to some embodiments, light illuminating from the epitaxial surface (top illuminated) may also have a double and/or multiple bounce of the optical signal within the MS-PD/APD 5120 if there is a refractive index discontinuity such as a buried silicon dioxide layer (BOX, buried oxide) as shown in MS-PD/APD structures discribed above and/or a change in effective index of the microstructure to the refractive index of bulk material. Double and/or multiple bounce of the optical signal within the MS-PD/APD allows for a thinner absorption layer without significantly sacrificing quantum efficiency and short transit time, thereby allowing higher data rate operation of the MS-PD/APD. Double or multiple bounce of light refers to light that is not absorbed in the pass of the MS-PD/APD and is exiting the MS-PD/APD structure; these photons are reflected back toward the MS-PD/APD structure. Within the micorstructure of holes and or pillars, light can also be in a resonance and or coupled resonance state which can result in an

enhanced effective absorption coefficient and/- or enhanced effective absorption length.

[00206] FIG. 52 is a diagram showing an array of MS-PD/APDs integrated with IC electronics such as TIA and/or other signal processing and routing electronics on a single Si chip. Arrays can include 2 to over 10 MS-PD/APDs integrated with IC electronics such as TIA and/or ASIC for signal processing, routing, storage, for example. In the example shown, four MS-PD/APDs 5220, 5222, 5224 and 5226 are shown mounted on a single Si chip 5210. The MS-PD/APDs 5220, 5222, 5224 and 5226 are connected to IC electronics 5230, 5232, 5234 and 5236 respectively. According to some embodiments, however, multiple MS-PD/APDs are connected to a single IC electronics unit on the Si chip or multiple IC electronics units are connected to a single MS-PD/APD. The MS-PD/APDs in the array may be identical, for example the microstructure such as hole diameter and period are optimized for the same wavelength, for example 850-870 nm. According to other embodiments, each MS-PD/APD in the array may be optimized for a different band of wavelengths. For example, if there are four MS-PD/APDs in the array, the MS-PD/APDs can be optimized at 850-870 nm, 875-895 nm, 900-920 nm and 920-950 nm respectively (or any combination thereof) by optimizing the hole diameter and periods of each MS-PD/APD. See, e.g., Molin et al, 850-950 nm wideband OM4 multimode fiber for next generation WDM systems, OFC (2015), which is incorporated by reference herein. Data rates of 1, 5, 10, 16, 20, 25, 28, 32, 40, 56 and greater and all ranges in between are possible depending on the standard and protocol and applications for the optical data link. The optical fibers 5240, 5242, 5244 and 5246 may be separate fibers, or can be provided as a parallel fiber ribbon. The optical fibers 5240, 5242, 5244 and 5246 can each carry a single band of wavelength and/or multiple bands of wavelengths for WDM and CWDM to give an aggregated data rate of 100 Gb/s to 1 Tb/s or more. For example, an array of ten MS-PD/APDs with ten fiber channels each at 10 Gb/s give an aggregated data rate of 100 Gb/s. A four MS-PD/APD array with 4 fiber channels each at 25-28 Gb/s gives an aggregated data rate of 100 Gb/s, a two MS-PD/APD array with 2 fiber channels each at 56 Gb/s gives an aggregated data rate of 100+ Gb/s. If each fiber channel can carry multiple wavelength bands, for example 850-870 nm and

875-895 nm, and each wavelength band can transmit at 25-28 Gb/s, then a 4 fiber array can effectively have an aggregated data rate of over 200 Gb/s.

[00207] FIG. 53 is a diagram showing an epitaxial structure for a high data rate MS-PD, according to some embodiments. The structure shown is capable of greater than 10 Gb/s. Holes 5322 are etched to the SiO2 BOX layer 5304 or they can be etched to the P layer 5306 and/or partially etched into the P layer 5306, for example. Doping and thicknesses are as follows: Si substrate 5302 is 150 μm thick; BOX layer 5304 is 2-4 μm thick; P+ layer 5306 is 0.2 -1 μm thick with doping of > $1x10^{20}/cm^3$; I layer 5308 is 1.5-2 μm thick and not intentionally doped (less than $5x10^{16}/cm^3$); and N+ layer 5310 is 0.2-0.5 μm thick with doping of > $1x10^{19}/cm^3$. The high doping of the N and P layers 5310 and 5308 reduce the minority carrier lifetime to minimize diffusion current that can result in a slow response of the PD. According to some embodments, doping as high as > $1x10^{20}$ and $1x10^{21}/cm^3$ is used so that minority carrier lifetimes are in the picoseconds and the in-series resistances are reduced.

[00208] FIG. 54 is a diagram showing an epitaxial structure for a high data rate MS-PD, according to some embodiments. The structure and doping is similar or identical to those depicted in and described with respect to FIG. 53, except that the holes 5422 are etched to the top of the P layer 5306 and/or just into the P layer 5306.

[00209] FIG. 55 is a diagram showing an epitaxial structure for a high data rate MS-PD, according to some embodiments. The structure and doping is similar or identical to those depicted in and described with respect to FIGs. 53 and 54, except that the holes 5522 are etched at least half way into the P layer 5306.

[00210] FIG. 56 is a table showing the mesa size, hole diameters, hole period distances, and lattice patterns for MS-PDs, according to some embodiments. In these examples the lattice can be either hexagonal or square. The holes can be circular, oval, polygonal. The holes are 1300 nm in diameter with a period of 2000 nm, 1500 nm in diameter with a period of 2000 nm, 700 nm in diameter with a period of 1000 nm and 630 nm in diameter with a period of 900 nm. The wavelength of operation is from 800-990 nm and the material is Si. A thin passivation layer of SiO2 may be included with thicknesses ranging from 3-100 nm. The mesa size, which in part defines the capacitance of the MS-PD (excluding the

bond pads and contact metals), are 5 μm, 10 μm, 20 μm, 25 μm, 30 μm, 40 μm, 50 μm and 80 μm, depending on the data rate of the MS-PD. Low capacitance and short transit times result in higher data rate MS-PD.

[00211] FIGs. 57A and 57B are diagrams showing hexagonal and square lattice hole patterns, according to some embodiments. FIG. 57A shows a hexagonal lattice pattern and FIG. 57B shows a square pattern where "d" is the period in each case. According to some embodiments, these layouts are used for the example parameters for the MS-PDs shown in FIG. 56.

[00212] FIG. 58 is a diagram showing an epitaxial layer structure for a silicon MS-PD, according to some embodiments. The structure thickness and doping is as follows: Si substrate 5802 is 150 μm; BOX (buried oxide) layer 5804 is 2-4 um thick; Si P layer 5806 is 0.2-0.5 μm thick and doped to > $2x10^{20}/cm^3$; Si I layer 5808 is approximately 1.5-2 μm thick and is not intentionally doped (having background doping of less than $5x10^{16}/cm^3$; Si N layer 5810 is approximately 0.2 μm thick and doped to > $2x10^{20}/cm^3$. The high doping of the P and N layers can also be > $1x10^{19}/cm^3$ for example. According to some embodiments, an etch stop layer made of a material such as SiGeB, SiGeC or SiGeBC, with thickness of 5 nm to 50 nm can be included at the interface of P Si 5806 and I Si 5808 to assist in processing during the etching of microstructured holes and/or the mesa. If SiGeB is used which is heavily P doped, a structure is N-I-P may be desireable. The high doping of the P and N regions, in addition to reducing the sheet resistance, also reduces the minority carrier lifetime such that photons absorbed in the P and N region will have minimal contribution to the photocurrent. The reduced minority carrier lifetime in the P and N regions reduces the diffusion of photogenerated carriers to the high field "I" region where the minority carriers are swept to the anode and cathode and contribute to the photocurrent.

[00213] FIG. 59 is a diagram showing aspects of a MS-PD, according to some embodiments. The material structure, including thickness and doping is similar or identical to that depicted in and described with respect to FIG. 58. In the case of FIG. 59 the P and N doping in layers 5910 and 5906 are interchanged resulting in a P-I-N arrangement. Note that in either FIG. 58 or 59 the arrangement can be P-I-N or N-I-P. Holes 5922 are etched to the SiO2 layer 5804, and P and N ohmic contacts 5928 and 5930 are made to the P and N layers 5910 and 5906,

respectively. A mesa is etched to define the photosensitive area and to define the capacitance of the PIN structure. Mesa diameters range from 10 μm to 80 μm depending on the data rate the that the MS-PD is designed for (as described with respect to FIG. 56). For 20-40 Gb/s, diameters of the mesa are typically 20-40 μm diameter. The P layer 5910 with 0.2 μm thickness and doping of > $2x10^{20}/cm^3$ can have a sheet resistivity of less than 50 ohms approximately, The N layer 5906 with 0.2 μm thickness and doping > $2x10^{20}/cm^3$ can give a sheet resistance of less than 35 ohms approximately. The high doping of the P and N layers can also be > $1x10^{19}/cm^3$ for example. The thinner P and N layer allow a higher percentage of the optical power to be in the "I" layer and smaller percentage in the P and N layers, thereby maximizing the quantum efficiency of the MS-PD. Passivation, polyimide bridge, bond pads and other processing steps are not shown for simplicity. A reverse bias voltage is applied between the P and N contact to form a high field region in the "I" layer. Voltages typically range from about 2-6 V. In the case shown, illumination is from the top at normal angle or at an angle off normal. Wavelength range from 800-990 nm, but other wavelengths such as 780 nm may also be used. The nominal wavelength is 850 nm, but may also include wavelengths such as 810-830, 830-850, 850-880, 930-960, 960-990.

[00214] FIG. 60 is a diagram showing aspects of a MS-PD, according to some embodiments. The MS-PD, including thickness and doping of the material structure, is similar or identical to that depicted in and described with respect to FIGs. 58 and 60. In this case, holes 6022 are etched to and/or into the N layer 5906, but not all the way to the SiO2 layer 5804 as in FIG. 59. Accordingly, there is no enhanced absorption in the N layer, which may result in a higher percentage of the optical power in the "I" layer. This tends to improve the quantum efficiency of the MS-PD. The SiO2 layer 5804 may or may not be necessary.

[00215] FIG. 61 is a diagram showing aspects of a MS-PD, according to some embodiments. The MS-PD, including thickness and doping of the material structure, is similar or identical to that depicted in and described with respect to FIGs. 58-61. In this case, the Si MS-PD is illuminated from the substrate side (also referred to herein as backside illuminated or bottom illuminated). A via 6170 is etched to remove the silicon substrate, and is etched to the SiO2 layer 5804 or almost to the SiO2 layer or into the SiO2 layer or through the SiO2 layer. The Si

substrate 5802 is removed to minimize optical loss at wavelength ranges from 800-990 nm. A reflector 6132 on the P layer 5910 surface is fabricated that may include a filler process such as polyimide, solid carbon dioxide or spin on glass (SOG) such that the reflector 6132 doesn't short the PIN diode. Note that the reflector 6132 doesn't need to be exactly planar, but may be concave in the regions with holes, which may enhance the trapping of the light waves. The reflector 6132 may be dielectric, Bragg reflectors, conductive transparent metal oxide, metal or alloy such as Ag, Au, or any combination thereof. Indium tin oxide (ITO) may also be used, together with non-conductive dielectrics to form a Bragg reflector. Metal and/or conductive oxide can further reduce the sheet resistance of the P layer 5910, thereby reducing the parasitic resistance and improving the modulated frequency response (data rate) of the MS-PD. According to some embodiments, the "I" layer 5808 can be thinner in the case of back illumination with a reflector since light can transit at least twice and perhaps more times through the "I" layer without degrading the quantum efficiency while at the same time improving the modulated frequency (data rate) response of the MS-PD. This is because with a thinner "I" layer the transit time of the photogenerated carriers is shorter. The frequency response of a photodiode is determined by its capacitance and resistance (RC time) and the transit time. Optical transit time may become important at high enhanced effective absorption length of greater than a factor of 100 or more for certain high data rates for example.

[00216] FIG. 62 shows a Ge on Si PIN epitaxial layer structure for a MS-PD, according to some embodiments. The material structure, including thickness and doping, is similar or identical to that depicted in and described with respect to FIGs. 58-62. In this case, the N Si layer 6206 with doping > $2x10^{19}/cm^3$ can have thicknesses of 0.2-2 μm. Also included is a Ge "I" layer 6208 that is not intentionally doped with doping less than $2x10^{16}/cm^3$ and with a thickness of 0.5-2 μm. An upper Ge P layer 6210 with doping > $2x10^{20}/cm^3$ is formed with a thickness of 0.1-0.2 μm. According to some embodiments, a thin Ge buffer layer (not shown) may be used at the interface of N Si layer 6206 and "I" Ge layer 6208 to initiate good crystal growth of Ge on Si. The high doping of the P and N also reduces the minority carrier lifetime, thereby minimizing the diffusion of

photogenerated carriers that can be swept into the high field "I" region that can contribute to the overall photocurrent.

[00217] FIG. 63 shows a Ge on Si MS-PD, according to some embodiments. The MS-PD, including thickness and doping of the material structure, is similar or identical to that depicted in and described with respect to FIGs. 58-62. Holes 6322 are etched to the SiO2 layer 5804 or the holes can be etched to the N Si layer 6208 in which case SiO2 layer 5804 may or may not be necessary, and the MS-PD is illuminated from the top or front (the epitaxial surface). The absorption of photons in the wavelength range from 1100 to 1800 nm is mostly in the Ge regions rather than the Si regions. By keeping the P Ge layer 6210 thin, a large percentage of the photons are absorbed in the Ge "I" layer 6208 thereby increasing the quantum efficiency. The high refractive index difference between Ge and Si may require that the holes only be etched to the top of Si N layer 6206. However in this example, the holes 6322 are etched to the SiO2 layer 5804. The N Si layer 6206 can be up to 2 μm thick in this case and doping can be in the range of $>1x10^{19}/cm^3$ to give a sheet resistance of less than 50 ohms. For 850 nm operation, or for wavelengths in the range of 800-990 nm, a thin N Si layer can increase the percentage of photons absorbed in the I Ge region. A 0.2 μm thick N Si layer with doping $>2x10^{20}/cm^3$ will give a sheet resistance of less than 50 ohms and also reduce the minority carrier lifetime. A thick N Si layer of 2 μm can also be used for the wavelength ranges of 800-990 nm or 800-1800 nm, since for wavelengths in the range of 800-990nm, Ge absorbs over 90% of the photons over a length of 2 μm. Therefore, less than 5% of the photons reach the N Si layer. At wavelengths of 850 nm less than 1% reach the N Si layer, and at 990 nm less than 3% reach it.

[00218] In certain cases, for wavelength ranges 800-990 nm, microstructured holes may not be used predominately for enhancing the absorption, but rather to reduce capacitance with holes partially or fully etched into Ge layer(s). In addition, holes may not be necessary and bulk Ge may be used. According to some embodiments, microstructures can be used to also reduce reflections.

[00219] FIG. 64 shows a Ge on Si MS-PD, according to some embodiments. The MS-PD, including thickness and doping of the material structure, is similar or identical to that depicted in and described with respect to FIGs. 58-63. In this case, holes 6422 are etched to the Si layer 6206. The index of refraction for Ge is

approximately 4 and the index of refraction for Si is approximately 3.45. This difference in refractive index may provide for sufficient enhanced absorption in the Ge region. In this case, the SiO2 layer 5804 may not be necessary and the MS-PD may be grown on a Si wafer without the BOX layer 5804. For wavelength ranges 1100-1800 nm, Si has acceptably low optical losses and most of the absorption is in the Ge regions. For top illuminated MS-PDs, the P Ge layer can be made thin so that the bulk of the photons are absorbed in the I Ge region, which increases the quantum efficiency. ITO (indium tin oxide) may be use in conjunction with the P Ge layer 6210 to further reduce the sheet resistance of the P layer.

[00220] FIG. 65 shows a Ge on Si MS-PD, according to some embodiments. The MS-PD, including thicknesses and doping of the material structure, is similar or identical to that depicted in and described with respect to FIGs. 58-64. In this case, the MS-PD is back or bottom illuminated. This structure is very good for wavelength ranges from 800-1800 nm using a thin N Si layer of 0.2 μm. Less than 3% of the photons with wavelength at 800 nm are absorbed in the N Si layer 6206. Furthermore, in a single pass through 1 μm of Ge, over 85% of 990 nm photons are absorbed. In a double pass over 95% of 990 nm photons are absorbed. In the back illuminated MS-PD where Ge I is grown on N Si, together with a reflector 6532 on the P Ge layer, double and/or multiple passes of the photons allow a thinner I absorbing layer 6208, which reduces the transit time of the photogenerated electrons and holes. A photodiode with higher bandwidth of 40 Gb/s or more is achievable. Holes 6322 can be etched to the SiO2 layer 504 or can be etched to the Si layer 6206 (as shown in FIG. 64). With microstructured hole arrays, enhanced absorbing can occur at wavelengths of 1100-1800 nm. For example at 1550 nm, with double pass through a 1 μm thick bulk Ge, less than 9% is absorbed, whereas with microstructured holes in the Ge layer, absorption of greater than 30% can be achieved and in some cases, greater than 50% absorption can be achieved. In certain cases, absorption in a MS-PD with Ge I layer, greater than 70% can be achieved at 1550 nm for double pass in a 1 μm thick Ge or for a single pass in a 2 μm thick Ge MS-PD.

[00221] The MS-PD can have the following layers: Ge (or SiGe) P layer 6210 can be doped to $> 2x10^{20}/cm^3$ with thickness of approximately 0.1 μm, Ge I (absorbing layer) 6208 can be not intentionally duped ($< 5x10^{16}/cm^3$) with a

thickness of 0.5-2.0 μm, and finally Si N layer 6206 can be doped to >$2x10^{19}/cm^3$ with a thicknesses of 0.2-0.5 μm. In addition, during via etch to remove the Si substrate, the SiO2 layer can be left intact, partially etched or etched entirely to remove the SiO2.

[00222] FIG. 66 is a diagram showing a Ge on Si PD, according to some embodiments. The PD, including thicknesses and doping of the material structure, is similar to that depicted in and described with respect to FIGs. 58-65. FIG. 66 is shown arranged as a flip chip although a front illuminated arrangement is also possible with slight degradation due to the P Ge layer. The PD is similar to the MS-PD shown in FIG. 64 without the microstructured hole arrays. The Ge on Si photodiode with epitaxial structure as shown for operation in the 800-1300 nm takes advantage of double bounce especially for the 1300 nm wavelength region and still maintains high data rate operation. The PD can be integrated with SiGe BiCMOS. According to some embodiments, the SiO2 layer is omitted. With solder bump technology the PD can be flip chip mounted directly on a PCB, as described above for other embodiments, e.g., as shown in FIGs. 44-52. According to some embodiments, the PD can have the following layers: Ge (or SiGe) P layer 6210 doped to > $2x10^{20}/cm^3$ with a thickness of approximately 0.1 μm, Ge I (absorbing layer) 6208 not intentionally doped (< $5x10^{16}/cm^3$) with a thickness of 0.5-2.0 μm, and finally Si N layer 6206 doped to > $2x10^{19}/cm^3$ with a thicknesses of 0.2-0.5 μm. In addition, during the etching of via 6670 to remove the Si substrate, the SiO2 layer 5804 can be left intact (as shown in FIG. 65), etched partially or etched entirely to remove the SiO2 (as shown in FIG. 66). An antireflection layer (not shown) can be applied to the Si N layer to minimize reflection in the case the SiO2 layer is completely etched off.

[00223] FIG 67 is a diagram showing a Ge on Si PD, according to some embodiments. The PD, including thicknesses and doping of the material structure, is similar to that depicted in and described with respect to FIGs. 58-66. In this case voids 6722 are formed to reduce the device PIN junction capacitance. The voids 6722 can be partially etched into the Ge layers to remove a sufficient amount of material to reduce the capacitance by a certain amount. The capacitance reduction allows for a larger area PD while maintaining the same data rate bandwidth as a similar Ge on Si PD but without the voids. The larger area PD

allows for greater tolerance in misalignment of the optical fiber and/or light source to the photodiode, thereby reducing packaging costs. Data rate bandwidth is determined by the RC time and the transit time. Integration of this structure as with all the structures discussed are possible with electronics such as TIA, which together with solder bump technology, can be directly attached to PCB. According to some embodiments, the wavelength of operation for this structure range from 800-1300 nm and with data rate in excess of 40 Gb/s.

[00224] Note that a BOX structures does need not be used. The PD can have the following layers: Ge P layer 6210 doped to > $2x10^{20}/cm^3$ with a thickness of approximately 0.1 μm; Ge I (absorbing layer) 6208 that is not intentionally doped (< $5x10^{16}/cm^3$) with a thickness of 0.5-1.0 μm; and finally Si N layer 6206 doped to >$2x10^{19}/cm^3$ with a thicknesses of 0.2-0.5 μm; and a buried oxide layer 5804 of 2-4 μm.

[00225] FIG. 68 is a diagram showing aspects of a microstructured avalanche photodiode (MS-APD), according to some embodiments. The MS-APD can have the following layers: Si P layer 6810 P doped to >$2x10^{19}/cm^3$ with a thickness of approximately 0.1-0.2 μm; Si I (absorbing layer) 6808 that is not intentionally doped (<$5x10^{15}/cm^3$) with a thickness of 0.5-2.0 μm; Si N layer 6806 n doped to >$2x10^{19}/cm^3$ with a thicknesses of 0.2-0.5 μm; and a buried oxide layer 6804 with thickness of 2-4 μm on an Si substrate 6802. The MS-APD device has two additional layers, a charge layer and a multiplication layer. The charge layer 6820 is right below the absorbing I layer 6808. The Si P charge layer 6820 is doped to about $1.8x10^{17}/cm^3$ and has a thickness of approximately 0.1 μm. Directly below the charge layer is the multiplication layer 6818 of the MS-APD. Si I layer 6818 is not intentionally doped (< $1x10^{16}/cm^3$) and has a thickness of approximately 0.5 μm. A via 6870 is etched in the silicon substrate to the SiO2 layer (an antireflection coating can be applied to minimize reflection) and light with wavelength ranging from 800-990 nm is applied through the via. A reflector 6832 on the top surface of the MS-APD provides a double/multiple pass of the photons through the absorbing "I" layer 6808. An advantage is a thinner absorbing layer, which results in a shorter transit time. The MS-APD data rate bandwidth is therefore enhanced. Microstructured hole arrays 6822 are etched to the SiO2 layer 6804 and/or almost to the SiO2 layer. P and N contacts 6828 and 6830 are shown on the same surface

for solder bumps to be applied so that the MS-APD can be flip chip mounted directly on a ceramic multi chip carrier and/or on a printed circuit board. Only the most basic processing steps are shown for simplicity. Additional steps or elements such as passivation, bond pads, polyimide/spin on glass planarization, antireflection coatings, are not shown. In addition, during etching of via 6870, after removal of the Si substrate, the SiO2 layer can be partially etched or etched away entirely for either MS-APD or MS-PD structures. Without the reflector 6832, optical signal can also impinge from the top surface.

[00226] FIG. 69 is a diagram showing aspects of a microstructured avalanche photodiode (MS-APD), according to some embodiments. The MS-APD, including thicknesses and doping of the material structure, is similar to that depicted in and described with respect to FIG. 68. The microstructured hole array 6922 is etched to the charge layer 6820, multiplication layer 6818 and/or the N layer 6806 of the APD structure. The holes 6922 are not etched all the way to the SiO2 layer. Light is illuminated through the via 6970 where the silicon substrate is removed to the SiO2. The SiO2 layer can also be etched so that light is impinging directly on the N Si layer 6806. This can be applicable for all bottom illuminated MS-PD and MS-APD devices where an antireflection coating can be applied directly to Si. For wavelengths ranging from 800-990 nm, a thin N Si layer 6806 of 0.2 μm approximately is preferred to reduce absorbing in the regions away from the absorbing "I" layer 6808. Light can also impinge from the top/front surface where the reflector 6832 is removed. In such cases, a via might be omitted and the Si "I" layer may be increased to 1.5 - 2 μm for quantum efficiency > 30%. In some cases the quantum efficiency is > 50%, in some cases > 70%, and in some cases > 80%. The multiplication factor or gain of the avalanche can be > 2. In some cases the gain is > 5. In some other cases it is > 10. In some further cases it is > 15, and in yet some other cases the gain is > 20. The data rate bandwidth can be > 10 Gb/s. In some cases the bandwidth is > 15 Gb/s. In some cases it is > 20 Gb/s/. In some cases the bandwidth is > 25 Gb/s and in some cases > 30 Gb/s. In addition, the SiO2 layer can be removed entirely, partially and/or it can have voids which are or are not filled with Si, for MS-PD and MS-APD, and an etch stop layer such as SiGeB, SiGeC or SiGeBC can be used during the removal of the Si substrate for formation of a via used for back/bottom illumination.

[00227] FIG. 70 is a diagram showing a MS-APD without the SiO2 layer, according to some embodiments. The MS-APD, including thicknesses and doping of the material structure, is similar to that depicted in and described with respect to FIGs. 68-69. An etch stop layer 7034 of SiGe or SiGeC or SiGeB (where the SiGe has about 1% Ge and heavily doped with boron to > $1x10^{20}/cm^3$) and a thickness ranging from 0.1 to 2 μm. SiGeBC can be grown on the Si substrate 6802 and/or on Si epitaxial layer(s) such as N Si layer 6806. According to some embodiments, the MS-APD has the following thickness and doping levels: Si N layer 6806 has a thickness ranging from 0.2 to 1 μm and doping ranging from > $2x10^{19}/cm^3$ to > $2x10^{20}/cm^3$; Si I multiplication layer 6818 is not intentionally doped (< $1x10^{16}/cm^3$) and has a thickness of approximately 0.5 μm; Si P charge layer 6820 doped to about $1.8x10^{17}/cm^3$ and a thickness of approximately 0.1 μm; Si I absorption layer 6808 is not intentionally doped (< $5x10^{15}/cm^3$) with a thickness of 0.5-1.0 μm; and Si P capping layer 6810 doped to > $2x10^{20}/cm^3$ with a thickness of approximately 0.1 μm. According to some embodiments, multiple etch stop layers can be used. For example, another etch stop layer can be formed at the interface of the Si I multiplication layer 6818 and the Si N layer 6806. Thickness of the etch stop layer can range from 1 nm to 100 nm, and can be doped P or N, or not intentionally doped to match the adjacent layer electrical characteristics. Wavelengths of the optical signal can range from 800 to 990 nm and if illuminated from the backside, a reflector can be formed of a dielectric such as SiO2/Ag. According to some embodiments, the reflector 6832 is a Bragg reflector consisting of two dielectrics with different indices such as SiO2 and HfO2, or ITO together with Ag, Au, and/or Pt. Reflector 6832 is used to reflect any un-absorbed signal photons for double and/or multiple pass through the absorbing Si I region 6808. In addition, the device can be front illuminated where the reflector 6832 is omitted and the absorbing Si I layer 6808 thickened to 1.5-2 μm for optimizing the quantum efficiency. According to some embodiments, a via can also be included in the front/top illuminated MS-APD. Similarly, a MS-PD can also be use this structure with the Si P charge and Si I multiplication layers omitted. A front and back illuminated MS-PD can be beneficial since the removal of the Si substrate improves the refractive index contrast and has improved absorption efficiency in the microstructure, which in turn improves the quantum efficiency.

[00228] The high dopings of the P and N layers are to both reduce the sheet resistivity and to reduce the lifetime of the minority carriers in the P and N layers to reduce diffusion of minority carriers into the high field Si I absorption layer that can cause degradation in the data rate response (also referred to as the frequency response) of the MS-PD/APD. The microstructured hole array can be etched to the SiGeC and/or SiGeB stop layer and/or past the stop layer either during the hole etch and/or during the via etch. The etch stop layer can also be entirely or partially removed after the hole etch or during the via etch. In this way, the SiGeC, SiGeBC or SiGeB layer is not in the optical path for a back illuminated MS-PD/APD. Note that in SiGeB where Ge is about 1% (e.g. $Si_{0.99}Ge_{0.01}$) the bandgap is approximately that of Si. In addition, as in FIG. 69, the microstructured hole arrays can be etched to a depth that corresponds to the absorbing Si I layer and/or to a depth that is greater than the Si I absorbing layer and partially into the avalanche region.

[00229] FIG. 71 is a diagram showing a Ge on Si microstructured avalanche photodiode (MS-APD), according to some embodiments. The MS-APD, including thicknesses and doping of the material structure, is similar to that depicted in and described with respect to FIGs. 68-70. A Ge I absorption layer 7108 is not intentionally doped ($< 5x10^{15}/cm^3$) and has a thickness of 0.5-2.0 μm. An upper Ge P capping layer 7110 is doped to $> 2x10^{20}/cm^3$ with a thickness of approximately 0.1 μm. Microstructured hole array 7122 is etched to the Si P charge layer 6820 or just before the Si P layer. Alternatively, the holes 7122 can be etched into the Si P charge layer 6820 and/or into the Si multiplication layer 6818. A via 6970 is etched, removing the Si substrate from the optical path. The SiO2 layer can be left intact, partially etched or etched through entirely or a N Si substate without SiO2 can be used. Antireflection layer (not shown) can be applied to the Si N layer 6806, if exposed, to minimize reflection. Wavelength ranges can be 800-1800 nm, 1300-1600 nm, 810-880 nm, and 930-990 nm, for example. Hole dimensions and period can be optimized for certain wavelength ranges. A reflector 6832 can be formed on the P Ge or SiGe layer 7110. The reflector 6832 can be made of dielectric and metal, ITO (indium tin oxide or similar transparent conducting oxides) and metal, all dielectric such as a Bragg reflector, or any combination thereof. The reflector 6832 reflects photons that are not absorbed on the first pass back toward the absorber

Ge I layer 7108 for a double or multiple pass. A thinner Ge I absorbing layer 7108 can be used as compared to photodiodes with a single pass. The thinner Ge I layer results in shorter transit times and therefore higher data rates. The growth of Ge on Si may use a Ge buffer layer, which is grown to initiate high quality crystalline growth of Ge. See, e.g. Kang et al, Epitaxially-grown Ge/Si avalanche photodiodes for 1.3É m light detection, Vol. 16, No. 13 / OPTICS EXPRESS 9365 (2008) (hereinafter "Kang et al") which is incorporated herein by reference. For wavelength ranges 1200-1750 nm, the via 7270 is not necessary as Si is mostly transparent at those wavelengths. In addition, without the reflector 6832, optical signal can impinge from the top surface and the Ge "I" layer 7108 can be increased in thickness to approximately 2 microns.

[00230] FIG. 72 is a diagram showing a Ge on Si microstructured avalanche photodiode (MS-APD), according to some embodiments. The MS-APD, including thicknesses and doping of the material structure, is similar to that depicted in and described with respect to FIGs. 68-71. In this case, the microstructure hole array 7222 is etched to the SiO2 layer 6804. According to some embodiments the holes 7222 are etched to within a few tenths of a micrometer of SiO2 layer 6804 and the via 7270 is etched to the SiO2 layer. The SiO2 layer can remain whole, be partially-etched, or can be etched through entirely during the via etch. The light impinging from the backside has wavelengths ranging from 800-1800 nm. Other wavelengths may also be used such as 630-780 nm, for example. Some photo generated carriers can occur in the Si layers, but the bulk of the photo generated carriers will be in the Ge I layer 7108, especially in the wavelength range of 800-1800 nm and in particular in the wavelength ranges of 1100-1800 nm. The epitaxial structure is similar to that shown in FIG. 71 as is the reflector 6832 on the Ge P layer for reflecting the light back toward the Ge I absorbing layer. The removal of the SiO2 layer allows for a high reflective index contrast between the microstuctured semiconductor holes, which can improve the light gathering properties of the microstructured hole array and the air. Also, reflections are removed that could occur at the SiO2-air interface and SiO2-semiconductor interface. For a front illuminated MS-APD, the reflector 6832 is removed and the Ge I absorbing layer 7108 is thickened to the range of 1-2 μm. The via and SiO2 removal can be

implemented for front side illuminated MS-APD. By removing the avalanche layers, P charge and I multiplication the MS-APD becomes a MS-PD.

[00231] FIG. 73 is a diagram showing a Ge on Si microstructured avalanche photodiode (MS-APD) with an etch stop layer, according to some embodiments. The MS-APD, including thickness and doping of the material structure, is similar to that depicted in and described with respect to FIGs. 68-72. An etch stop layer 7334 such as SiGe, SiGeC, SiGeB or SiGeBC is grown on the Si wafer. Note that the Si substrate (wafer) 6802 may already have layers, such as an N Si epitaxial layer, subsequent APD layers, other buffer layers, spacer layers, or other etch stop layers on it (not shown) which promote good crystalline growth and processing reproducibility. The basic APD layers are: a Si N layer 6806 of thickness ranging from 0.2 to 0.5 μm with doping ranging from > $2x10^{19}/cm^3$ to > $2x10^{20}/cm^3$; Si I multiplication layer 6818 not intentionally doped and with a thickness of approximately 0.5 μm; Si P charge layer 6820, doped to about $1.8x10^{17}/cm^3$ and having a thickness of approximately 0.1 μm; Ge I absorption layer 7108, which is not intentionally doped has a thickness of 0.5-1.0 μm; and Ge or SiGe P capping layer 7110 doped to > $2x10^{20}/cm^3$ and having a thickness of approximately 0.1 μm. Microstructured hole arrays are etched with hole diameters and periods that are optimized for specific wavelength ranges. Specific wavelength ranges include the following: 800-860, 860-880, 880-920, 920-990, 990-1100, 1100-1350, 1350-1450, 1450-1550, 1550-1650, and 1650-1800 nm. Hole and mesa passivations are not mentioned for simplicity, but examples can be found in Kang et al. Other passivation methods exist in the literature. Light impinges from the backside, through a via 7370 where the etch stop layer can be removed. Light can also impinge from the front side, but with the absorption Ge I layer 7108 thickness increased to the range of 1-2 μm approximately. For front side illuminated MS-APD/PD, the via can also be implemented to increase reflective index contrast between the semiconductor microstructure and air for example. Other layers such as planarization layers, bridging layers, bond pads, and fillers are also not shown for simplicity.

[00232] FIG. 74 is a diagram showing a Ge on Si microstructured avalanche photodiode (MS-APD), according to some embodiments. The MS-APD, including thicknesses and doping of the material structure, is similar to that depicted in and

described with respect to FIGs. 68-73, except that with the Ge P layer replaced with SiGe or SiGeC P layer 7410 to reduce absorption of photocarriers in the P contact layer. SiGe and/or SiGeC have a larger bandgap than Ge and therefore the absorption coefficient is smaller than in Ge for the same thickness. See e.g. Kolodzey et al, 'Optical and electronic properties of SiGeC alloys grown on Si substrates', Journal of Crystal Growth 157, 386-391 (1995) (hereinafter "Kolodzey, et al.") which is incorporated herein by reference. For example, from Kolodzey et al., with $SiGe_{0.88}C_{0.12}$, the band gap is 1.3 eV (direct) as compared to Si of 1.11 eV and 0.66 eV for Ge. SiGe alloy will give a bandgap between that of Si and Ge, therefore any addition of Si to Ge will increase the bandgap and reduce absorption in the P layer. According to some embodiments, this P layer replacement technique is applied to all the MS-PD/APD structures shown and described herein. In particular, a Ge P layer is replaced with SiGe P and/or SiGeC P layers. According to some further embodiments, in all MS-PD/APD structures shown and described herein, the Si P and N layers can also be fully or partially replaced with SiBeC P and SiGeC N which reduces absorption of the optical signal in the P and N regions of the MS-PD/APD. In some cases, the multiplication region of the APD, which is Si can also be replaced with SiGeC I to reduce absorption of the optical photons in this invention. At certain wavelengths 1200-1750 nm, Si is mostly transparent and either or both of a via 7370 and an etch stop layer 7334 are not necessary. In this case a N Si substrate is used with the back surface polished and antireflection coated.

[00233] FIG. 75 is a diagram showing another SI NIP epitaxial layer structure for a MS-PD, according to some embodiments. The holes 7522 are etched to a depth of approximately 2.3 μm and can terminate a few tenths of a micron before and/or after the Si P layer 7506. Doping and thicknesses are approximately as follows: Si P substrate 7502; a Si P layer 7506 of 0.2 μm (or a range of 0.1-1 μm) with a P doping > $2x10^{20}/cm^3$ that can also be > $1x10^{19}/cm^3$; Si I layer 7508 that is not intentionally doped with background doping < $5x10^{16}/cm^3$ and in some cases < $5x10^{15}/cm^3$ with a thickness of about 2 or in the range of 1-2.5 μm; N Si layer 7510 with doping of > $2x10^{19}/cm^3$ with a thickness of about 0.3 μm or in the range of 0.2-0.5 μm. N contact 7528 is on the Si N layer 7150. The P contact(s) can be on the upper surface of the Si P substrate as in contact 7530 and/or on the

bottom/backside of the substrate as in contact 7532. A mesa etch is used to define the PIN junction area and therefore the capacitance. Mesa is etched to the P layer 7506 and/or to the P substrate 7502 and the P contact 7530 can be deposited on the Si P layer 7506 and/or on the Si P substrate 7502 back side 7532. According to some embodiments, other electrical isolation can be used also such as proton bombardment to define the PIN area or other doping techniques such as PN junction doping, or trench doping. Light in this structure impinges from the front side with wavelength ranges from 800-990 nm approximately. Hole diameters of 1300 nm with a period of 2000 nm, and hole diameters of 1500 nm and period of 2000 nm can be used with either a hexagonal and/or square lattice pattern. According to some embodiments, the range of hole diameters is from 600 nm to 1500 nm approximately and the range of periods is from 900 to 2500 nm approximately.

[00234] FIGs. 76A-76C are diagrams showing Si N-I-P epitaxial layers on buried oxide for a MS-PD, according to some embodiments. In FIG. 76A, the holes 7622 are etched to the Si P layer 7606, partially into the Si P layer and/or to the SiO2 layer 7604. Doping and thicknesses are approximately as follows: Si BOX (buried oxide) 7604 in substrate 7602; Si P layer 7606 of 1 μm (or a range of 0.1-1 μm) with a P doping > $2x10^{20}/cm^3$; Si I layer 7608 that is not intentionally doped with background doping < $5x10^{16}/cm^3$ and in some cases < $5x10^{15}/cm^3$ and with thickness of 2 μm or a range from 0.5-2.5 μm; and N Si layer 7610 with doping of > $2x10^{19}/cm^3$ and with thickness of 0.3 μm or a range from 0.2-0.5 μm for example. N and P contacts 7628 and 7630 can be on the front side, where P contact is made after a mesa etch to the P layer 7606. An etch stop layer, such as SiGeB or SiGeC, can be used at the interface between the P layer 7606 and I layer 7608. The I layer 7608 can be thin, 0.5-1 μm, for example, if the light impinges from the backside and a reflector is placed on the top surface Si N layer 7610 such that light can have multiple passes through the I layer 7608. The P and N can be interchanged and the microstructured photodiode (MS-PD) can be PIN, for example. If SiGeB is used as an etch stop layer, the SiGeB is heavily P type and the NIP structure is preferred. The etch stop layer can be 0.05 to 1 μm thick for example and may replace in whole or in part the Si P layer. Light can impinge either from the front

side and/or from the backside with proper device or epitaxial layer modifications. Wavelength ranges are 800-990 nm approximately.

[00235] In FIG. 76B, the P Si 7606 layer in FIG. 76A is replaced by a $Si_{0.99}Ge_{0.01}B$ layer 7616 with P doping > $2x10^{20}/cm^3$ and a thickness of 0.5 μm or a range of thicknesses from 0.2-1 μm. All other layers are as in FIG. 76A. The microstructured holes 7622 are etched and can stop at the SiGeB layer and/or pass through the SiGeB layer and stop at the SiO2 layer and/or go into the SiO2 layer. A via 7670 can be etched that stops at the SiO2 layer, or stops into or goes through the SiO2 layer. N and P ohmic contacts 7628 and 7630 are formed on the Si N layer and SiGeB P layer respectively. Light can impinge either from the top surface (the epi surface) and/or the bottom surface (the substrate surface), and reflectors can be placed on either the top or bottom with a dielectric spacer layer, for a multiple pass through the I absorbing layer. Wavelength ranges from 800 to 1000 nm. Not shown for simplicity are other elements such as passivation layers, polyimide bridge layers, mesas, bond metals.

[00236] In FIG. 76C, a P Si layer 7626 of approxiamtely 0.1 μm thick and with doping greater than $1x10^{20}/cm^3$ is added as the first layer on the SiO2 7604 onto which $Si_{0.99}Ge_{0.01}B$ layer 7616 is grown with P doping greater than $1x10^{20}/cm^3$ and with a thickness of approximately 0.3 μm. As in Fig. 76A and 76B, light can impinge from the top and/or bottom surfaces where a via is etched. N and P ohmic contacts are placed on the N and P layers, respectively. Microstructured hole array 7622 is etched through to the SiO2 layer 7604 and/or etched partially into the P layer 7626. If light is impinging from the bottom, a via 7670 is etched into the silicon substrate 7602 and into the SiO2 layer 7604, which can be partially or entirely etched. A reverse bias voltage is applied between the P and N contact of 1-10 volts.

[00237] In some applications, light can impinge from the top and bottom of a MS-PD/APD simultaneously. The light can have same or different wavelengths, data rates, polarization, and amplitude for coherent optical communications. An advantage of having light coming from both top and bottom is that the use of a beam splitter is not necessary and can save 3 dB in optical power loss.

[00238] FIG. 77 is a diagram showing a MS-PD with Si NIP epitaxial layer and a SiGeB stop etch layer on a P Si substrate, according to some embodiments. The