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(54) Title of Invention

LATERAL-TYPE SEMICONDUCTOR LIGHT-RECEIVING ELEMENT HAVING
A PIN STRUCTURE

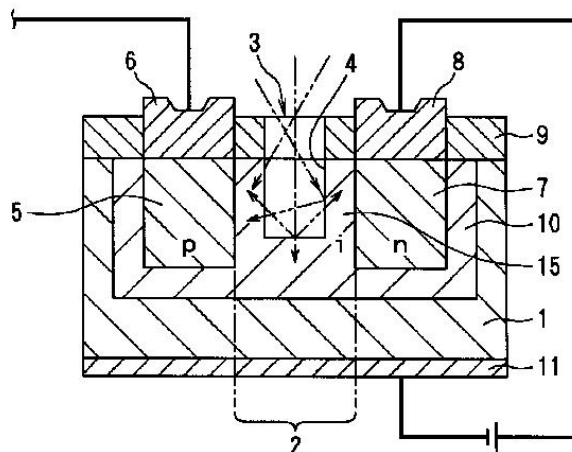
(57) Abstract

Problem

To provide a lateral-type semiconductor light-receiving element having a PIN structure, in which light-receiving sensitivity is improved without causing a decrease in response speed.

Solution

In a lateral-type semiconductor light-receiving element, in which interfaces between an i-layer 15 and a p-layer 5 and between the i-layer 15 and an n-layer 7, respectively, of a PIN structure are formed perpendicular to a semiconductor substrate surface, and light that enters the i-layer is converted into electric current and detected, a hole 4, which extends from a light-receiving surface 3 to a prescribed depth of the i-layer 15, is provided in a light-receiving region 2.



CLAIMS

1. A lateral-type semiconductor light-receiving element having a PIN structure in which interfaces between an i-layer and a p-layer and between the i-layer and an n-layer, respectively, of the PIN structure are formed perpendicular to a semiconductor substrate surface, and light that enters the i-layer is converted into electric current and detected, wherein:

a hole, which extends from a light-receiving surface to a prescribed depth of the i-layer, is provided in a light-receiving region.

DETAILED DESCRIPTION OF THE INVENTION

[0001]

TECHNICAL FIELD PERTAINING TO THE INVENTION

The present invention relates to a lateral-type semiconductor light-receiving element having a PIN structure.

[0002]

BACKGROUND ART

In a vertical-type photodiode, in which a p-n junction surface is formed parallel to a semiconductor substrate surface, light impinges a depletion layer after passing through a p-layer or an n-layer; in contrast, in a lateral-type photodiode, in which the p-n junction surface is formed perpendicular to the semiconductor substrate surface, light directly impinges the depletion layer (without passing through the p-layer or the n-layer). Consequently, the lateral-type photodiode is advantageous in that it has better light-receiving efficiency than the vertical-type photodiode.

[0003] Conventionally, an i-layer (intrinsic layer) is provided in the photodiode between the p-layer and the n-layer to make the depletion layer thick. In a vertical-type photodiode having this kind of PIN structure, the i-layer is formed to a thickness that is the absorption length or more to make the light-receiving sensitivity high. Thereby, a quantum efficiency of 70% or more can be obtained at wavelengths of approximately 700 nm to 870 nm.

[0004] A lateral-type photodiode having a PIN structure (a photodiode in which interfaces between the i-layer and the p-layer and between the i-layer and the n-layer of the PIN structure are formed to be perpendicular to the semiconductor substrate surface) is produced by, for example: providing a region, which has an extremely light impurity concentration and will become the i-layer, on a front surface portion of the semiconductor substrate; and then forming the p-layer and the n-layer by adding and diffusing p-type impurities and n-type impurities respectively from an upper surface at locations that are at a prescribed spacing from this region, wherein the spacing between both the layers remains as the i-layer.

[0005] Consequently, in the case of the lateral-type photodiode having a PIN structure, when attempting to make the thickness of the i-layer (the depth from a light-incident surface) large, the p-layer and the n-layer must also be formed deeply. To form the p-layer and the n-layer deeply while maintaining a uniform width (i.e., the distance between the p-layer and the n-layer) of the i-layer in the thickness direction of the substrate, the distance between the p-layer and the n-layer must be made large at the substrate front surface. When the distance between the p-layer and the n-layer is made large at the substrate front surface, the width of the i-layer becomes large. When the width of the i-layer is large, the migration distance for an electron generated on the p-layer side of the i-layer to the n-layer electrode becomes long, and the response speed becomes slow.

[0006] Accordingly, in the lateral-type photodiode having a PIN structure, making the thickness (the depth from the

light-incident surface) of the i-layer large cannot simply be adopted as a method of further increasing the light-receiving sensitivity. Consequently, providing an anti-reflection film on the upper surface of the i-layer and making the incidence efficiency of the i-layer high is effective as a method of further increasing the light-receiving sensitivity of the lateral-type photodiode having a PIN structure.

[0007]

PROBLEMS TO BE SOLVED BY THE INVENTION

However, there is a problem in that, in the lateral-type photodiode having a PIN structure, which has the anti-reflection film on the upper surface of the i-layer, the response speed becomes low in the situation in which the photodiode is used as an element for receiving high-speed light signals. In view of such problems in the related art, an object of the present invention is to improve light-receiving sensitivity of a lateral-type semiconductor light-receiving element having a PIN structure without causing a decrease in response speed.

[0008]

MEANS FOR SOLVING THE PROBLEMS To solve the above-mentioned problem, the present invention provides a lateral-type semiconductor light-receiving element having a PIN structure in which interfaces between an i-layer and a p-layer and between the i-layer and an n-layer, respectively, of the PIN structure are formed perpendicular to a semiconductor substrate surface, and light that enters the i-layer is converted into electric current and detected, wherein a hole, which extends from a light-receiving surface to a prescribed depth (a shallower location than the depths of the p-layer and the n-layer) of the i-layer, is provided in a light-receiving region.

[0009]

EMBODIMENTS OF THE INVENTION An embodiment of the present invention is explained below. FIG. 1 is a cross-sectional view that shows a photodiode corresponding to one embodiment of the present invention. FIG. 2 is a diagram that shows one example of a planar shape in the situation in which the photodiode of this embodiment is formed in an array. FIG. 1 corresponds to a cross-sectional view through line A-A in FIG. 2.

[0010] This photodiode is a lateral-type photodiode (semiconductor light-receiving element) in which a PIN structure is formed perpendicular to a substrate surface of a silicon substrate (semiconductor substrate) 1, and holes 4 are provided in a light-receiving region 2 (the region sandwiched between a p-layer 5 and an n-layer 7 of an i-layer 15), the holes 4 extending from a light-receiving surface 3 to a prescribed depth in the i-layer 15 and perpendicular to the surface of the silicon substrate 1.

[0011] A p-electrode 6 and an n-electrode 8 are formed on the upper surface of the p-layer 5 and the n-layer 7, respectively. A p-electrode 11 is formed on the lower surface of the silicon substrate 1. In addition, an element-protection layer 9, which is composed of a silicon oxide film or the like, is formed to a prescribed thickness on the upper surface of the silicon substrate 1 on portions outside of the locations having both of the electrodes 6, 8 and the holes 4. This photodiode can be produced, for example, by the following method.

[0012] First, an n-well (a region having an extremely low impurity concentration) 10 is provided on a surface-layer portion of the p-type silicon substrate 1. Next, p-type impurities are added to and diffused into one of two regions of the n-well 10, and n-type impurities are added to and diffused into the other region of the n-well 10, with a prescribed spacing between the two regions. Thereby, the p-layer 5 and the n-layer 7 are formed in the n-well 10, and a

portion of the n-well 10 that is between the p-layer 5 and the n-layer 7 remains as the i-layer 15. Next, the electrodes 6, 8 are formed on the p-layer 5 and the n-layer 7, respectively, and then the element-protection layer 9 is formed.

[0013] Next, a focused ion beam processing apparatus (FIB) is employed to irradiate the portion sandwiched by both the electrodes 6, 8 on the upper surface of the silicon substrate 1 with an ion beam so as to etch the element-protection layer 9 and the i-layer 15, thereby creating the holes 4, which extend from the light-receiving surface 3 to a prescribed depth (a location shallower than the depth of the p-layer 5 and the n-layer 7) in the i-layer 15 in the thickness direction of the silicon substrate 1.

[0014] Here, the dimension of the holes 4 in the direction between the p-layer 5 to the n-layer 7 is set to the dimension at which the i-layer 15 of a prescribed thickness exists between the holes 4 and the p-layer 5 and between the holes 4 and the n-layer 7, respectively. In addition, in the situation in which the light-receiving surface 3 between the pairs of electrodes is large, preferably a plurality of the holes 4 is provided within the light-receiving surface 3, as shown in FIG. 2. In this situation, for example, width W1 of each of the electrodes 6, 8 is 1 μm , spacing W2 between the electrodes 6, 8 is 2–4 μm , pitch K of the holes 4 is 2–4 μm , and the diameter of each of the holes 4 is 1 μm .

[0015] By connecting a power supply between the n-electrode 8 that contacts the upper surface of the n-layer 7 and the p-electrode 11 on the lower surface of the substrate 1, with the n-layer 7 side as the positive, applying a reverse-bias voltage, and connecting the p-electrode 6, which contacts the upper surface of the p-layer 5, to an output circuit, this photodiode can convert the light incident on the i-layer 15 from the light-receiving surface 3 into electric current to detect the light. In addition, in this photodiode, the light (a portion of which is shown in FIG. 1 by chain, double-dashed lines) that enters the interior of the hole 4 from the light-receiving surface 3 directly enters the light-receiving region 2 from a bottom surface and side surfaces of the hole 4, and by being reflected from the bottom surface and the side surfaces, the light travels from the bottom surface toward the side surfaces and enters the light-receiving region 2, and travels from one side surface toward the opposing side surface and enters the light-receiving region 2. Consequently, the light-receiving efficiency at the light-receiving region 2 becomes higher than in the situation in which no holes 4 are present.

[0016] In the situation in which the light-receiving surface 3 is merely made large without providing the holes 4 in order to make the light-receiving surface area large, the migration time increases for the electrons generated on the p-layer side of the i-layer to reach the electrode on the n-layer, and the response speed becomes slow because parasitic capacitance increases. In contrast, by providing the holes 4, the light-receiving surface area in this photodiode becomes larger, to the extent of the side surfaces of the holes 4, than in the situation in which no holes 4 are present. Consequently, in this photodiode, in no situation will the migration time for the electrons generated on the p-layer side of the i-layer to reach the electrode on the n-layer become longer than in the situation in which the light-receiving surface 3 is the same size with no holes 4 being provided. In addition, the parasitic capacitance of this photodiode becomes smaller than the situation in which the light-receiving surface 3 is the same

size with no holes 4 being provided. Hence, according to this photodiode, the light-receiving surface area can be made large and light-receiving efficiency can be made high without reducing response speed.

[0017] Furthermore, by having the holes 4, localized electric-field intensity applied to a portion of the i-layer 15 that surrounds the holes 4 becomes large in this photodiode. Thereby, compared with the situation in which there are no holes 4, response speed becomes faster because the light is absorbed at the portion of the i-layer 15 that surrounds the holes 4, and generated electron holes and electrons can migrate through the i-layer 15 at high speed. Accordingly, according to this photodiode, by providing the holes 4, the light-receiving efficiency at the light-receiving region 2 becomes high, which improves light-receiving sensitivity and also increases response speed.

[0018] It is noted that, although the lateral-type photodiode having a PIN structure is explained in this embodiment, the lateral-type semiconductor light-receiving element of the present invention, which has a PIN structure, is not limited thereto, and the present invention can also be applied to a lateral-type phototransistor, etc., in which the base and the collector portions have a PIN structure.

[0019]

EFFECTS OF THE INVENTION As explained above, according to the lateral-type semiconductor light-receiving element having a PIN structure according to the present invention, light-receiving sensitivity can be improved without causing a decrease in response speed.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a cross-sectional view that shows a photodiode corresponding to one embodiment of the present invention and is a diagram that corresponds to a cross-sectional view through line A-A in FIG. 2.

FIG. 2 is a diagram that shows one example of a planar shape in the situation in which the photodiode in FIG. 1 is formed in an array.

EXPLANATION OF THE REFERENCE NUMBERS

1	Silicon substrate (semiconductor substrate)
10	n-well
11	p-electrode
15	i-layer
2	Light-receiving region
3	Light-receiving surface
4	Hole
5	p-layer
6	p-electrode
7	n-layer
8	n-electrode
9	Element-protection layer

FIG. 1

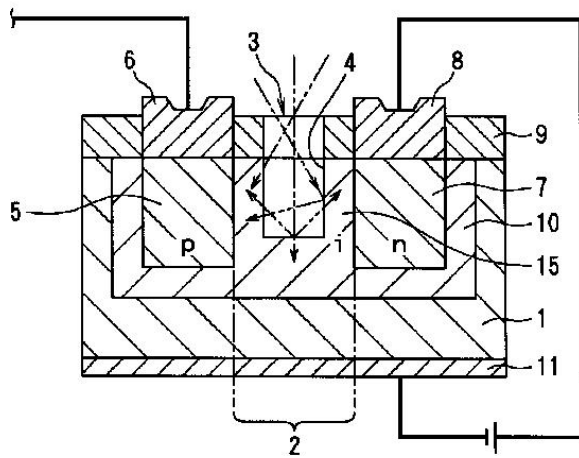
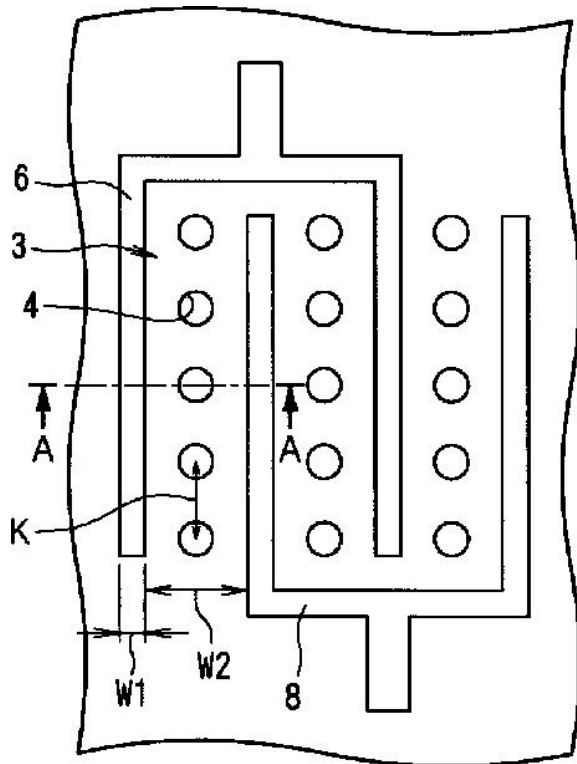


FIG. 2



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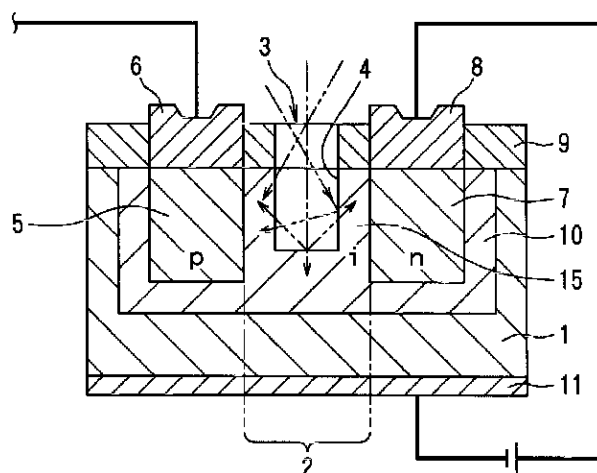
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(54) 【発明の名称】 P I N構造のラテラル型半導体受光素子

(57) 【要約】 (修正有)

【課題】 応答速度を低下させることなく受光感度を向上させたP I N構造のラテラル型半導体受光素子を提供する。

【解決手段】 P I N構造のi層15とp層5とn層7との界面が半導体基板面に対して垂直に形成され、i層に入射された光を電流に変換して検出するラテラル型半導体受光素子において、受光領域2に、受光面3からi層15の所定深さまで延びる穴4を設けた。



【特許請求の範囲】

【請求項1】 P I N構造のi層とp層およびn層との界面が半導体基板面に対して垂直に形成され、i層に入射された光を電流に変換して検出するラテラル型半導体受光素子において、

受光領域に、受光面からi層の所定深さまで延びる穴を設けたことを特徴とするP I N構造のラテラル型半導体受光素子。

【発明の詳細な説明】

【0001】

【発明の属する技術分野】本発明は、P I N構造のラテラル型半導体受光素子に関する。

【0002】

【従来の技術】p n接合面が半導体基板面に対して平行に形成されている縦型フォトダイオードでは、p層またはn層を通して空乏層に光が入射されるのに対して、p n接合面が半導体基板面に対して垂直に形成されているラテラル型フォトダイオードでは、空乏層に直接（p層やn層を介さずに）光が入射される。そのため、ラテラル型フォトダイオードは縦型フォトダイオードよりも、受光効率の点で有利である。

【0003】従来より、フォトダイオードにおいては、p層とn層との間にi層（真性層）を設けて、空乏層を厚くすることが行われている。このようなP I N構造を有する縦型フォトダイオードでは、受光感度を高くするために、i層を吸収長以上の厚さに形成することが行われている。これにより、波長700nm～870nm前後において、70%以上の量子効率が得られるようになる。

【0004】P I N構造のラテラル型フォトダイオード（P I N構造のi層とp層およびn層との界面が半導体基板面に対して垂直に形成されたフォトダイオード）は、例えば、i層をなす不純物濃度の極めて薄い領域を半導体基板の表層部に設けた後、この領域の所定間隔を開けた各位置に、上面からp型不純物及びn型不純物をそれぞれ添加して拡散させることによりp層及びn層を形成し、両層の間をi層として残すことによって作製される。

【0005】そのため、P I N構造のラテラル型フォトダイオードの場合にi層の厚さ（光入射面からの深さ）を大きくしようとすると、p層及びn層を深く形成する必要がある。基板の厚さ方向でi層の幅（p層とn層との距離）を均一に保持しながら、p層及びn層を深く形成するためには、基板表面でのp層とn層との距離を大きくとる必要がある。基板表面でのp層とn層との距離を大きくとるとi層の幅が大きくなる。i層の幅が大きいと、i層のp層側で生じた電子がn層の電極に達するまでの移動距離が長くなって、応答速度が遅くなる。

【0006】したがって、P I N構造のラテラル型フォトダイオードでは、受光感度をより高くする方法とし

て、i層の厚さ（光入射面からの深さ）を大きくすることを単純に採用することができない。そのため、P I N構造のラテラル型フォトダイオードの受光感度をより高くする方法としては、i層の上面に反射防止膜を設けてi層への入射効率を高くすることが有効である。

【0007】

【発明が解決しようとする課題】しかしながら、i層の上面に反射防止膜を有するP I N構造のラテラル型フォトダイオードには、高速の信号を受光する素子とした場合に応答速度が低くなるという問題点がある。本発明は、このような従来技術の問題点に着目してなされたものであり、P I N構造のラテラル型半導体受光素子において、応答速度を低下させることなく受光感度を向上させることを課題とする。

【0008】

【課題を解決するための手段】上記課題を解決するために、本発明は、P I N構造のi層とp層およびn層との界面が半導体基板面に対して垂直に形成され、i層に入射された光を電流に変換して検出するラテラル型半導体受光素子において、受光領域に、受光面からi層の所定深さ（p層およびn層の深さより浅い位置）まで延びる穴を設けたことを特徴とするP I N構造のラテラル型半導体受光素子を提供する。

【0009】

【発明の実施の形態】以下、本発明の実施形態について説明する。図1は本発明の一実施形態に相当するフォトダイオードを示す断面図である。図2は、この実施形態のフォトダイオードがアレイ状に形成されている場合の平面形状の一例を示す図である。図1は図2のA-A線断面図に相当する。

【0010】このフォトダイオードは、P I N構造がシリコン基板（半導体基板）1の基板面に対して垂直に形成されたラテラル型フォトダイオード（半導体受光素子）であり、受光領域（i層15のp層5とn層7とで挟まれた領域）2に、受光面3からi層15の所定深さまで、シリコン基板1面に垂直に延びる穴4が設けてある。

【0011】p層5およびn層7の上面には、p電極6およびn電極8がそれぞれ形成されている。シリコン基板1の下面にはp電極11が形成されている。また、シリコン基板1の上面の両電極6、8および穴4の位置を除いた部分に、シリコン酸化膜等からなる素子保護層9が所定の厚さで形成されている。このフォトダイオードは、例えば以下の方法で作製できる。

【0012】まず、p型のシリコン基板1の表層部にnウエル（不純物濃度の極めて薄い領域）10を設ける。次に、nウエル10の所定間隔を開けた2つの領域の一方にp型不純物を、他方にn型不純物をそれぞれ添加して拡散させる。これにより、nウエル10にp層5及びn層7が形成され、nウエル10のp層5とn層7との

間の部分がi層15として残る。次に、p層5及びn層7の上に電極6、8を形成した後、素子保護層9を形成する。

【0013】次に、集束イオンビーム加工装置(FIB)を用い、シリコン基板1上面の両電極6、8で挟まれた部分にイオンビームを照射して、素子保護層9とi層15をエッチングすることにより、受光面3からi層15の所定深さ(p層5およびn層7の深さより浅い位置)まで、シリコン基板1の厚さ方向に延びる穴4を開ける。

【0014】ここで、穴4のp層5-n層7間方向の寸法は、穴4とp層5との間および穴4とn層7との間にそれぞれ所定厚さのi層15が存在する寸法に設定する。また、各電極対間の受光面3が大きい場合には、図2に示すように、受光面3内に複数の穴4を設けることが好ましい。この場合には、例えば、電極6、8の幅W1を1 μ m、電極6、8の間隔W2を2~4 μ m、穴4のピッチKを2~4 μ m、穴4の直径を1 μ mとする。

【0015】このフォトダイオードは、n層7の上面に接触するn電極8と基板1の下面のp電極11との間に、n層7側を正として電源を接続して逆バイアス電圧を付与し、p層5の上面に接触するp電極6を出力回路に接続することにより、受光面3からi層15に入射された光を電流に変換して検出することができる。また、このフォトダイオードでは、受光面3から穴4内に入射された光(一部を図1に2点鎖線で表示)は、穴4の底面や側面から受光領域2に直接入射するとともに、底面や側面で反射されることで、底面から側面に向かって受光領域2に入射されたり、側面から対向する側面に向かって受光領域2に入射されたりする。そのため、穴4が無い場合よりも受光領域2での受光効率が高くなる。

【0016】受光面積を大きくするために穴4を設けず単純に受光面3を大きくした場合には、i層のp層側で生じた電子がn層の電極に達するまでの移動時間が長くなるとともに、寄生容量が大きくなるため、応答速度が遅くなる。これに対して、このフォトダイオードでは、穴4を設けることで、穴4が無い場合よりも穴4の側面の分だけ受光面積が大きくなっている。そのため、このフォトダイオードでは、i層のp層側で生じた電子がn層の電極に達するまでの移動時間が、受光面3が同じ大きさで穴4を設けない場合よりも長くなることはない。また、このフォトダイオードの寄生容量は、受光面3が

同じ大きさで穴4を設けない場合よりも小さくなる。これらのことから、このフォトダイオードによれば、応答速度を遅くすることなく、受光面積を大きくして受光効率を高くすることができる。

【0017】さらに、このフォトダイオードは、穴4を有することによって、i層15の穴4の周囲部分に掛かる電界強度が局所的に大きくなっている。これにより、i層15の穴4の周囲部分で光を吸収して発生した正孔と電子はi層15を高速で移動することができるため、穴4の無い場合と比較して応答速度が速くなる。したがって、このフォトダイオードによれば、穴4を設けることによって、受光領域2での受光効率が高くなって受光感度が向上するとともに、応答速度も高くなる。

【0018】なお、この実施形態では、PIN構造のラテラル型フォトダイオードについて説明しているが、本発明のPIN構造のラテラル型半導体受光素子はこれに限定されず、ベースとコレクタの部分がPIN構造になっているラテラル型フォトトランジスタ等にも適用される。

【0019】

【発明の効果】以上説明したように、本発明のPIN構造のラテラル型半導体受光素子によれば、応答速度を低下させることなく受光感度を向上させることができる。

【図面の簡単な説明】

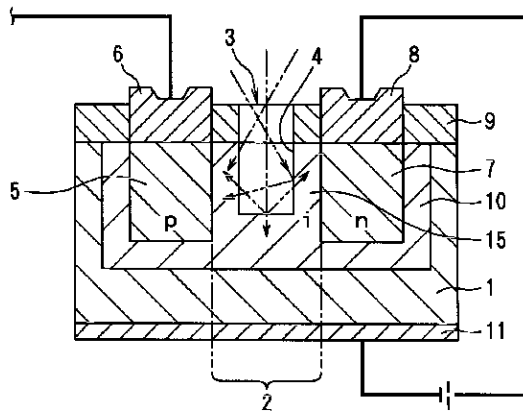
【図1】本発明の一実施形態に相当するフォトダイオードを示す断面図であって、図2のA-A線断面図に相当する図である。

【図2】図1のフォトダイオードがアレイ状に形成されている場合の平面形状の一例を示す図である。

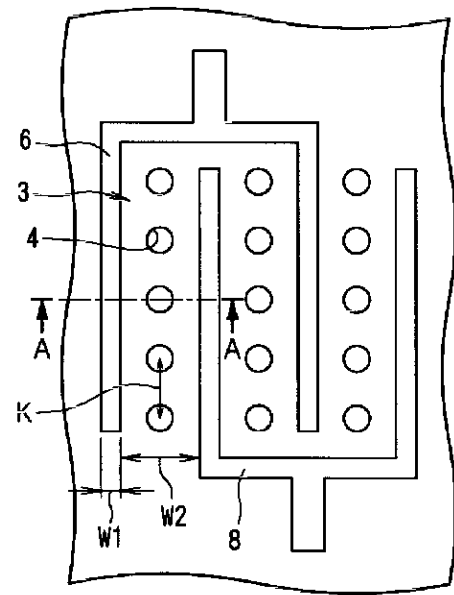
【符号の説明】

- 1 シリコン基板(半導体基板)
- 10 nウェル
- 11 p電極
- 15 i層
- 2 受光領域
- 3 受光面
- 4 穴
- 5 p層
- 6 p電極
- 7 n層
- 8 n電極
- 9 素子保護層

【図1】



【図2】



フロントページの続き

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I, Nadine A. Edwards, declare as follows:

1. I am over 21 years of age and am competent to make this declaration.
2. I am a native speaker of English.
3. I am fluent in Japanese.
4. I have 14 years of experience translating Japanese to English.
5. I translated the attached patent document "JP2002314116A" from Japanese to English.
6. I certify that the above-mentioned translation of the document "JP2002314116A" is, to the best of my knowledge, a true and accurate translation from Japanese to English.
7. In signing this declaration, I understand that the translation and this declaration may be filed as evidence in a contested case. I acknowledge that I may be subject to cross-examination within the United States.
8. I declare under penalty of perjury that all statements made herein are true and accurate to the best of my knowledge and belief, and that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

Executed: April 2, 2025

By: 
Nadine A. Edwards