Briefs

CMOS Active Pixel Image Sensor

Sunetra Mendis, Sabrina E. Kemeny, and Eric R. Fossum

Abstract—**A new CMOS active pixel image sensor is reported. The sensor uses a 2.0 μm double-poly, double-metal foundry CMOS process and is realized as a 128 × 128 array of 40 μm × 40 μm pixels. The sensor features TTL compatible voltages, low noise and large dynamic range, and will be useful in machine vision and smart sensor applications.**

I. Introduction

Charge-coupled devices (CCD's) are typically employed for image acquisition. While offering high performance, CCD area arrays are difficult to integrate with CMOS due to their high capacitances, complicating the integration of on-chip drive and signal processing electronics. CCD's are also highly susceptible to image smear. Some achievement in on-chip signal processing with CCD's has been reported [1]–[4] but a fully CMOS-compatible sensor technology enabling a higher level of integration would greatly benefit many applications [5]. These include machine vision, vehicle navigation, video phones, computer input devices, surveillance systems, auto focus, and star trackers. Simple p-n junction photodiode arrays have been fabricated using CMOS processes but typically have high read noise and suffer from image lag [6]. Both bipolar [7] and charge modulation device [8] image sensors are compatible with CMOS integration, but require specialized fabrication processes. In this paper, a new, 100% CMOS-compatible image sensor with good performance is reported.

II. Active Pixel Sensor Design and Operation

The CMOS active pixel sensor (APS) is shown schematically in Fig. 1. In essence, a small single-stage CCD has been fabricated in each pixel. For discussing the operation of the image sensor, it is assumed that the sensor is operated with voltage rails of 0 and +5 V, though higher and lower voltage operation is possible and has been demonstrated. Operation of the sensor is as follows. During signal integration, the pixel photogate (PG) is biased at +5 V, the transfer gate TX and reset transistor R are biased at +2.5 V, and the selection transistor S is biased off (0 V). Following signal integration, all pixels in the row to be read are read out simultaneously onto column lines by the following process. First, the pixels are addressed by the row selection transistor S biased at +5 V. This activates the source-follower output transistor in each pixel (the load transistor is located at the bottom of the pixel column and is biased at +2.5 V). The reset gate R is then briefly

Manuscript received June 14, 1993; revised October 11, 1993. The review of this brief was arranged by Associate Editor W. F. Kosonocky. This work was supported in part by the Defense Advanced Research Projects Agency and in part by the National Aeronautics and Space Administration.

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IEEE Log Number 9214896.

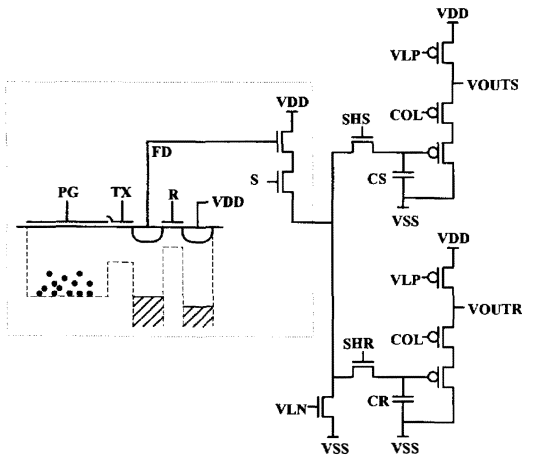

Fig. 1. Schematic illustration of image sensor circuit. Dotted line shows boundary of in-pixel circuits. The remainder of circuit is at bottom of column.

pulsed to +5 V to reset the floating diffusion output node FD to approximately +3.5 V. The output of the source follower is then sampled onto a holding capacitor at the bottom of the column. The photogate PG is then pulsed low to 0 V (with TX held at +2.5 V) to transfer the integrated signal charge under the photogate to the floating diffusion output node FD. The new source follower output voltage is sampled onto a second holding capacitor at the bottom of the column. Storing the reset level and the signal level on separate capacitors permits correlated double sampling of the pixel [9], eliminating kTC noise from the pixel, and suppressing 1/f noise and fixed pattern noise from the output transistor. In this circuit, the major source of readout noise is the kTC noise introduced by the sample/hold capacitors, since kTC noise from the pixel is suppressed by the differential output technique. The rms noise on these 1 pF capacitors is estimated to be 64 μV per capacitor, or 91 μV in differential mode.

All transistors were sized for readout at the rate of 30μHz corresponding to a row readout time of 260 μs/row. The total time to capture the row signal, in parallel, to the bank of capacitors at the bottom of each column was designed to be 0.7 μs. The capacitors are sequentially scanned for serial readout.

The APS was designed using highly conservative 2 μm p-well CMOS design rules and practices. The array was sized at 128 × 128 elements for a total die size of 6.8 × 6.8 mm. The fill factor of the 40 μm × 40 mm pixel, as measured by the ratio of active area (by design) to the total pixel area, is 26%.

The row and column selection 7-to-32 decoders were implemented using a 7-input NAND gate designed to fit in the 40 μm pixel pitch. The PG and R pulses were gated with the row selection. The reset and signal channels for each column were laid out to be as symmetric as possible to ensure good common-mode rejection and differential output. The digital decoder was designed to be highly isolated from the column-wise analog circuitry. A light shield surrounding the imaging area was made using second level metal. A photograph of the completed sensor is shown in Fig. 2.

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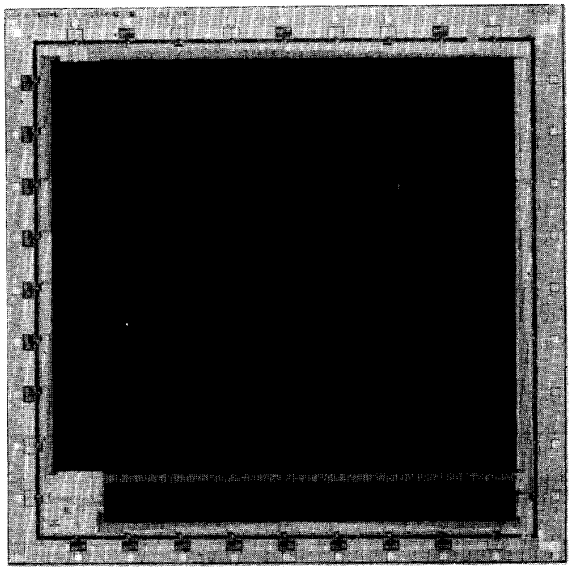

Fig. 2. Photograph of fabricated 128 × 128 CMOS APS array.

Fig. 3. Unprocessed output of 128 × 128 CMOS active pixel sensor.

III. Experimental Results

The image sensors were driven in accordance to the timing and voltage levels described above. A sample image is shown in Fig. 3. Using an electrical test circuit on a separate IC, output conversion was determined to be 4.0 μV/electron. Saturation was measured to be 600 mV, or 150 000 electrons. The saturation level was determined by the output amplifier rather than well capacity since the 2.5 V well capacity was estimated to be approximately 6×10^6 electrons for this surface-channel device. No lag or smear was observed. The design of the CMOS APS reset transistor results in a lateral anti-blooming drain so that blooming is suppressed. The fixed pattern noise (FPN) was approximately 3.3% *p-p* of the saturation level. Dark current was found to be well behaved and measured to be 62 e-/ms/pixel or under 1nA/cm^2 at ambient temperature. Dark current shot noise determines the noise floor of 42 e-rms at a 30 Hz frame rate at room temperature, corresponding to a dynamic range of 71 dB.

IV. Conclusion

A new, 100% CMOS active pixel image sensor has been demonstrated. The high performance obtained using standard foundry CMOS has encouraged us to continue to pursue a more highly integrated CMOS APS in the near future. A reduction in noise of more than a factor of 2, an increase in fill-factor to 35%, and reduction in FPN to below 0.5% *p-p* is believed to be readily feasible in later generations. The use of 0.8 μm design rules could yield a 15 μm × 15 μm pixel size. Coupled with a microlens technology, the effective aperture could reach 65% or more. This initial work paves the way for more complex pixel structures and on-chip electronics for robot vision, guidance and navigation, and other smart sensor applications.

Acknowledgment

The authors appreciate useful conversations and encouragement from their colleagues at JPL, especially B. Pain and R. Gee. The support of V. Sarohia of JPL and G. Johnston of NASA HQ is gratefully acknowledged. The research described in this paper was carried out by the Jet Propulsion Laboratory, California Institute of Technology.

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