Advances in fully CMOS integrated photonic devices

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ABSTRACT

The complete integration of photonic devices into a CMOS process flow will enable low cost photonic functionality within electronic circuits. BAE Systems, Lucent Technologies, Massachusetts Institute of Technology, Cornell University, and Applied Wave Research are participating in a high payoff research and development program for the Microsystems Technology Office (MTO) of DARPA. The goal of the program is the development of technologies and design tools necessary to fabricate an application specific, electronic-photonic integrated circuit (AS-EPIC). The first phase of the program was dedicated to photonics device designs, CMOS process flow integration, and basic electronic functionality. We will present the latest results on the performance of waveguide integrated detectors, and tunable optical filters.

Keywords: photodetector, optical filter, modulator driver, optical receiver, EPIC

I. INTRODUCTION

The introduction of photonics building blocks like integrated detectors and modulators, high performance optical filters, and low loss optical waveguides into a CMOS process flow opens a wide range of possibilities for a large range of novel devices spanning from application specific devices to transceiver chips, eventually improving the performance of microprocessor. Application specific devices benefit from added functionalities by introducing optical components. Transceiver chips, fabricated in a CMOS fabrication line, will introduce low cost devices that are produced in large volumes. Process reliability will eventually improve so that those components can be introduced into a microprocessor design with the promise to improve performance and reduce energy consumption, extending the microprocessor roadmap, know as Moore's law.

In order to reach those goals, there are multiple challenges. Photonic devices built on a silicon platform have to perform similar to discreet devices. The process flow for these devices has to fit seamlessly into a standard CMOS process flow without degrading the performance of the electronic components. The process flow has to be flexible enough so it can be adapted to future CMOS process flows. In this paper we address some of those challenges and summarize the achievements and advances in detector and filter performance and process integration.

II. THE EPIC CMOS PLATFORM

Our AS-EPIC chip is one of the very first signal processing applications of monolithic electronic-photonic integration on the silicon wafer platform. It is designed to provide a high resolution, Fast Fourier Transformation of an input RF signal. The RF signal is encoded on an optical carrier with an electro-optic modulator; timing channelization is performed with an optical filter network; and the signal of each channel is read by a dedicated photodetector. The size, power dissipation, bandwidth, and noise of the individual devices are important, but the integrated E-P circuit functions

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(measured, for example, by the Spurious Free Dynamic Range) are the key performance metrics. A CMOS EPIC design can utilize a circuit of many standardized devices that perform a more complex, signal processing function. Our channelizing application is one of a new class of 'technology shrink' functions that reduce the size, weight, and power of traditional microwave signal processors by encoding on an optical carrier. In fact many of the devices, such as ring resonators, have identically functioning devices in the microwave regime. We have learned that many of the circuit design paradigms for microwave circuits can be applied directly to EPIC.

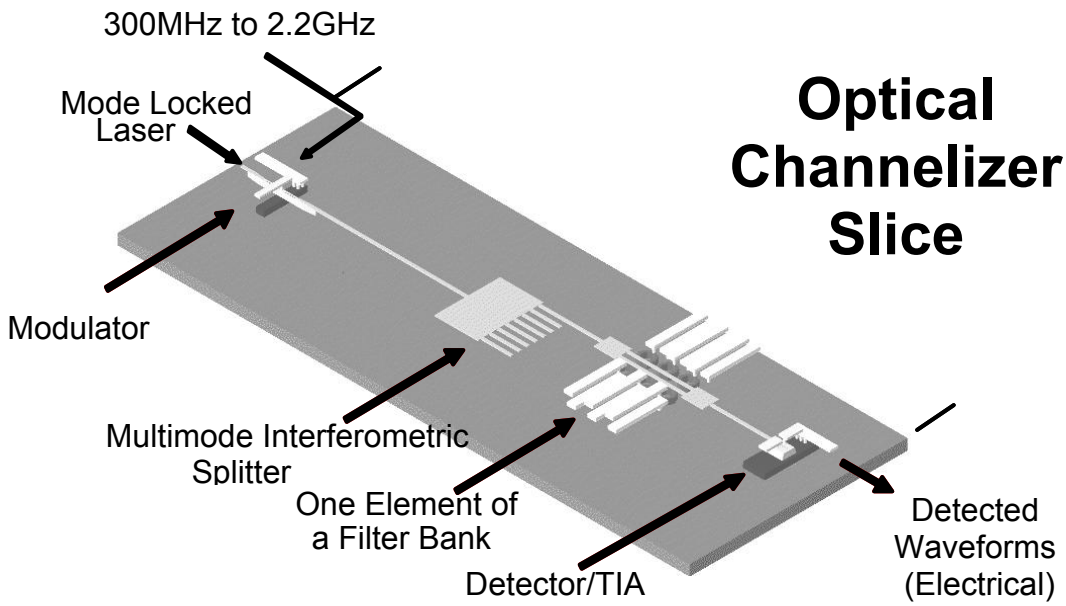

Fig. 1. Schematic representative of a single channelizer link on the AS-EPIC chip.

A schematic of our device is shown in Figure 1. The first node of E-P integration is the modulator/driver where the RF signal is encoded on the optical carrier. We use an 'optical power supply' architecture where the carrier is coupled to the chip from an external mode-locked laser. The frequency of the optical carrier is always much higher than the RF signal frequency. The choice of wavelength is dictated by the source performance and the modulator/waveguide design. Current high performance sources are designed for long haul telecommunications applications and operate near the fiber transparency optimum at 1550nm. Therefore, E-P circuits that can operate at these wavelengths have currently an advantage but alternative wavelengths may be available in the near future.

Materials selection for CMOS compatibility is not a limiting constraint. Si, SiO_2, Si_3N_4, Ge, and their alloys perform well for our designs and, once the optical source constraint is removed, they meet the integration constraint best. Silicon is transparent in the 1550nm wavelength range and its high index contrast with a SiO_2 cladding (n_{Si}/n_{SiO2}~3.5/1.5) allows micron turn radii for ultra-dense integration. The high refractive index of silicon also facilitates impedance matching for waveguide coupling to the active modulator (n=3.5 or 4.0) and photodetector (n=4) devices. At this stage of development, we use silicon for waveguides, modulator, and filters and germanium for the photodetectors and modulators. While the performance of these devices meets specifications, ease of materials and process integration may dictate some fine tuning among them in the future.

The optical signal is filtered in the time domain by phase management using ring resonator structures for dispersion-control. Each filter is tuned to a specific time domain and an array of filters provides an equivalent Fourier Transform of the input RF signal. After the timing deconvolution, the next E-P node, photodetector/TIA, transduces the optical signal to the electronic regime for A/D conversion. The circuit performance of our AS-EPIC chip is dependent on achieving several key specifications. Reconfigurable filters are required for good channel separation. Efficient photodetector/TIA

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nodes are required to achieve the specified high digital resolution. High linearity of the modulator/driver to detector/TIA signal path is required to meet the SFDR requirements of the circuit. Each of these issues and their dependence on materials, processes, and process integration is discussed in the following sections.

III. FABRICATION

The waveguide structures were fabricated upon a Silicon on Insulator wafer that consisted of a 200nm Si layer on top of 3000nm thermal oxide. The waveguide patterns were delineated using an ASML 5500/850 Deep UV Scanner linked to an FSI Polaris 2500 lithography processing cluster. The imaging of the ring resonators with smaller coupling gaps showed improved latitude when a illumination partial coherence of 0.7 was used and the main lens was set wide open at 0.8 numerical aperture.

The waveguide etch was performed with an AMAT Centura system with an etch chemistry that was very similar to the polysilicon etch that the CMOS process uses for the polysilicon gate of the transistor. Selective epitaxy of the Ge was inserted after the CMOS final anneal to avoid the excessive thermal budget. The Chemical Mechanical Polish of the post grown films was carried out on the Ebara F REX 150 with a custom slurry. The standard oxide slurry did not perform well with Ge films.

The first contact at the beginning of the Back End Of the Line was also adjusted to compensate for the additional height added to the topography. The new contact depth was extended ~ 2.5X and a new deeper etch was developed on a different AMAT Centura chamber. The tungsten deposition thickness for the plug fill was also adjusted to compensate for the deeper contact stud. Following this subsequent tungsten polish the remaining BEOL process steps were then standard CMOS type flow.

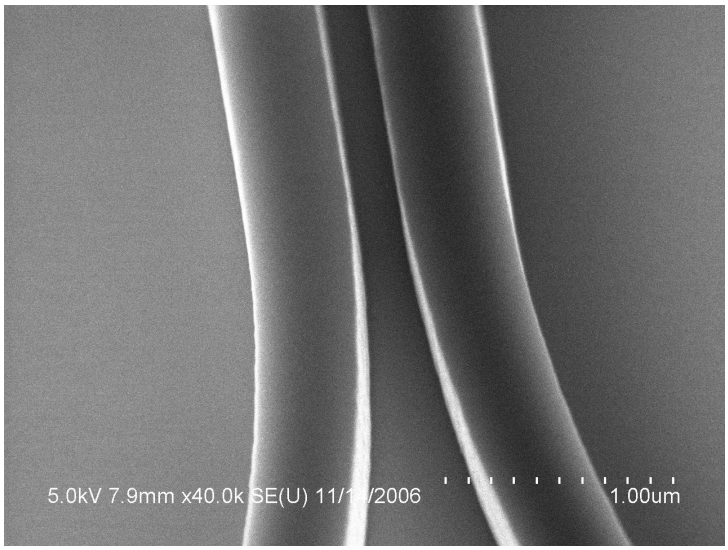

Fig. 2. Example of gap spacing between a Si waveguide and a Si ring resonator.

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IV. WAVEGUIDE INTEGRATED DETECTORS

High performance detectors are one of the essential building blocks for our AS-EPIC chip. In order to reach highly reliable channel readout, the external quantum efficiency of the detectors has to reach 90%. Therefore, the optical signal in the waveguide had to be coupled to the detector nearly loss free. We tested 3 different coupling schemes: top coupled; bottom coupled; and butt coupled detectors.

We introduced the bottom and butt coupled waveguide integrated detectors into the full EPIC process flow. For process integration purposes we choose 0.8% Si in Ge as detector material. The waveguide was formed by single crystal silicon-on-insulator (SOI). The SiGe was grown into dry etched silicon oxide trenches directly on the single crystal silicon [1]. In case of the bottom coupled detector, the single crystal Si was part of the waveguide structure. In case of the butt coupled detector, the optical signal was first coupled from the single crystal Si waveguide to a deposited poly Si waveguide. The poly Si waveguide was aligned to the center of the SiGe detector (see Fig. 3 for a cross sectional view of both coupling schemes). Although the crystalline quality of the SiGe was poor due to the existence of a polymer layer between the single crystalline Si and the SiGe, the butt coupled detector showed a 83% external quantum efficiency [2]. The detector bandwidth was > 4.5GHz. The bottom coupled detector showed a somewhat poorer performance with an external quantum efficiency of 20% and a bandwidth of 1.5GHz [2]. The performance of this detector is mainly limited by the polymer layer at the bottom of the detector, reducing the coupling efficiency significantly. We observed that the responsivity is flat through the full range of our tunable laser from 1470 nm to 1570 nm for a 10 μm long device. This result shows that the efficiency of the SiGe detectors can be high even at longer wavelength where the absorption coefficient of the material is much smaller than at the direct bandgap absorption.

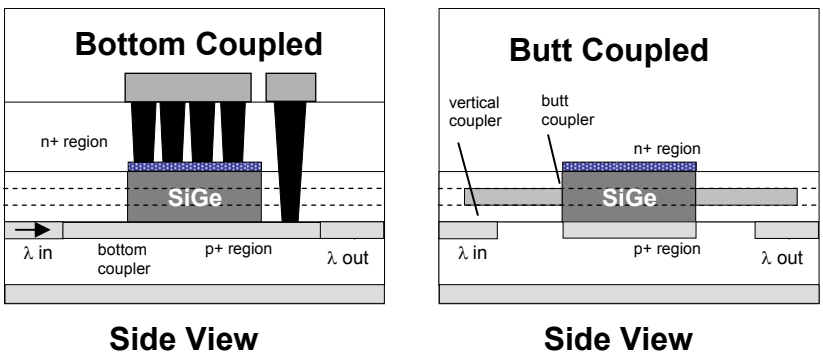

Fig. 3. Schematic cross sections for bottom coupled and butt coupled waveguide integrated detector.

The top coupled design was tested in a separate process run. We used 100% Ge as detector material and varied the waveguide material. We tested SiON of different compositions for the waveguide, thereby varying the refractive index of the waveguide material between 1.7 and 2.2. We found that with increasing refractive index of the waveguide material the coupling to the photodetector improved. Siliconnitride with a refractive index of 2.2 showed the best performance. With a 40μm long device we reached more than 90% external quantum efficiency even without bias (see Fig. 4). With 1.5V reverse bias we measured 95% external quantum efficiency. The bandwidth of the device was 7.5 GHz at 3V reverse bias [3]. We are currently fabricating Si waveguides that are top coupled to the Ge detectors. We expect even better coupling performance for a Si waveguide compared to a SiN waveguide.

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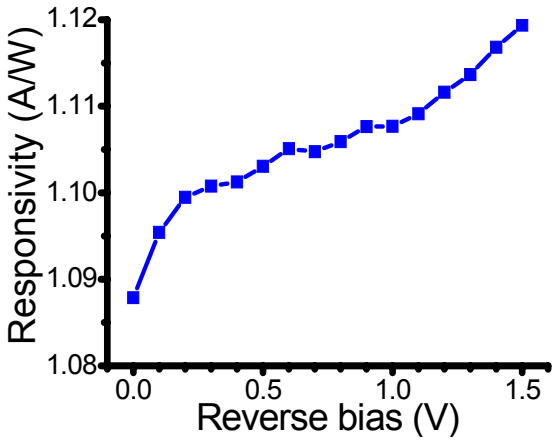

Fig. 4. Responsivity of a top coupled waveguide integrated detector as function of the detector bias. The responsivity was measured at 1550nm. The photodetector was 40μm long.

V. NARROW PASSBAND FILTER WORKING PRINCIPLE

A. Design and implementation

Reconfigurable and narrow Box-like filter response can be achieved using tunable all-pass ring resonators in a Mach-Zehnder (MZ) configuration [4,5]. This pole/zero filter design requires fewer stages than an all pole filter to attain a narrow passband response, making the tuning of this filter easier to control. The filter is composed of a MZ interferometer with a 3-dB splitter at the input, cascaded all-pass filters (APFs) on each arm, and a 3-dB combiner at the output. The input splitter divides the power equally between the upper and lower APFs. The APFs are composed of nominally identical cascaded ring resonators. The filter response can be tailored by changing the strength of the coupling into each resonator while tuning the resonant frequency via the resonator phase. The output combiner then serves to add and subtract the two APF responses [6]. The resulting filter response is periodic with the free spectral range (FSR) of the ring resonators. This architecture also offers great flexibility in tailoring the ripple in the passband and the stopband since the same physical device can be dynamically tuned to create a Butterworth, Chebyshev or elliptic filter response [6,7]. In this work, we chose to implement 4th order filter to demonstrate this technology. A schematic diagram and an image of a fabricated filter are shown in Fig. 5a and 5b, respectively.

For optimal filter response, low waveguide propagation loss is needed. The filter response as a function of ring round trip loss is shown in Fig. 6 for passbands with a nominally constant 3-dB bandwidth. The ring round trip loss causes rounding of the passband and increases its inband loss. To reduce optical waveguide losses, smooth waveguide facets and careful waveguide surface treatment during processing is essential [8]

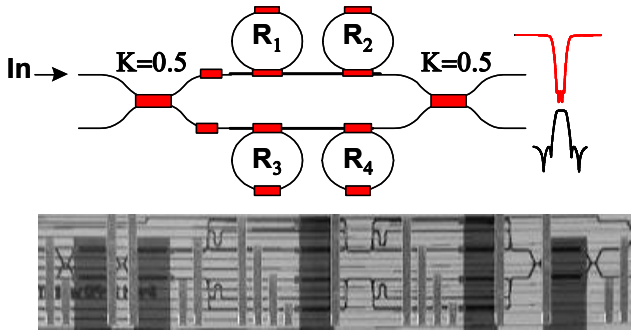

Fig. 5. Schematic diagram of the filter architecture.

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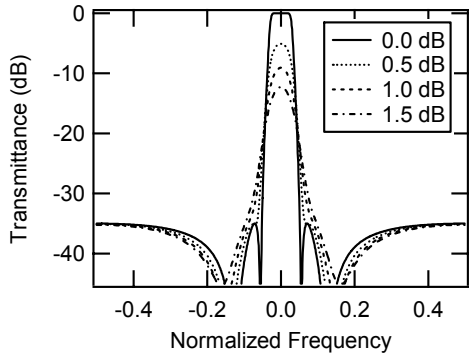

Fig.6. Impact of the ring round trip loss on the filter passband.

Tunability of the filter passband response is a key requirement for this application. We used thermo-optic phase shifters to set the coupling ratios and phases of the APFs. These thermo-optic heaters were processed using standard CMOS metallization. Though thermo-optic phase shifters have relatively slow switching speeds, it introduces negligible optical propagation losses compared to other fast tuning techniques [9, 10]. Furthermore, one advantage of using silicon waveguides is its large thermo-optic coefficient compared to silica. In our devices, only 27mW and 115mW needed to obtain a π phase change across a waveguide for the TE and TM modes, respectively.

B. Measured Filter response

The filter response is characterized for the TE optical polarization mode. All the APFs showed a similar round trip loss of about 0.78 dB. Using a lensed fiber to couple light into and out of the chip, we measured approximately 1 dB/facet coupling loss when waveguide dimension of about 0.2x0.2μm at the chip facet are used. Figure 7 shows a measured narrow passband of a 3-dB bandwidth of 1.0 GHz and 25-dB bandwidth of 2.9 GHz response obtained by tuning our filter. Note that the thick solid line corresponds for as fabricated response before the filter is tuned. Here, the transmittance is defined as the difference between the filter throughput and the throughput of a neighboring straight waveguide. The stopband rejection is >25 dB and the filter insertion loss is <6 dB. Figure 7 also shows excellent agreement between the measured and simulated passbands.

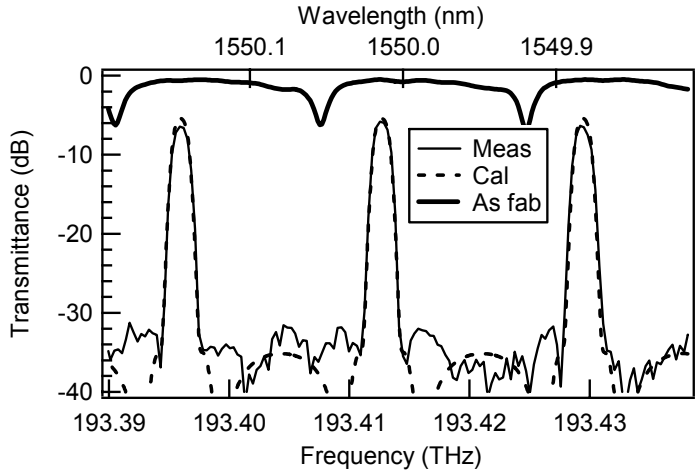

Fig. 7. Measured passband from a 4th order filter fabricated using SOI buried channel waveguides.

To further demonstrate the tunability of this filter, we configured the APFs to produce wider passbands simply by tuning the coupling ratios and phases of the APFs. Fig. 8 shows measured passbands with different 3-dB bandwidths from 0.8 GHz to 2.4 GHz. This filter also allows for fine control over the center frequency of a passband.

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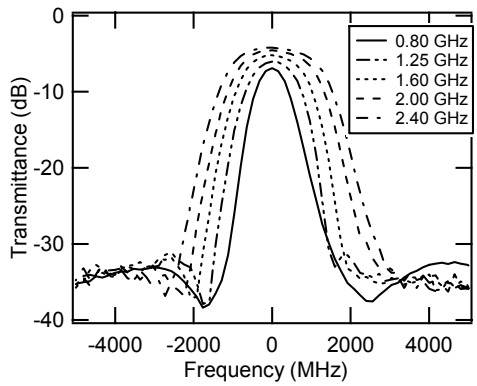

Fig. 8. Measured filter responses for different 3-dB bandwidths.

The passband can be tuned to any desired frequency simply by applying the appropriate power to heaters to tune the phases of the ring resonators. Figure 9 shows three such passbands set 2.5 GHz apart measured from the same filter using three different heater settings. Furthermore, with the filter simply mounted on a temperature-stabilized copper block, we were able to tune these passband frequencies with open loop control to a precision of 25 MHz.

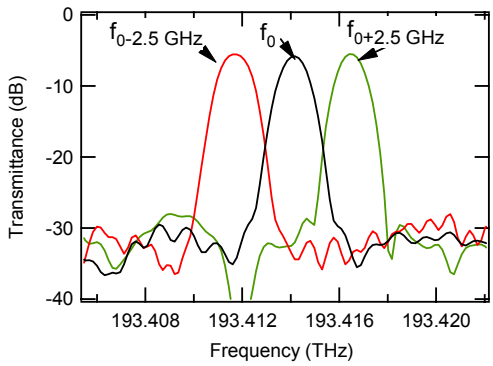

Fig. 9. Measured filter passbands positioned at 2.5 GHz spacing.

A key test for the viability of this technology is the reproducibility of filter response across different wafers. Figure 10 shows two filter passband responses of filters taken from the same wafer location but from two different wafers. As shown in this figure, the responses of the two filters are similar. A slight difference is observed though; this difference could be due to variation in the round trip loss and/or slight differences in filter settings.

The channelizer RF performance was measured with all optical components [11]. A system SFDR of 88dB$*$Hz$^{(2/3)}$ has been demonstrated for the channelizer function.

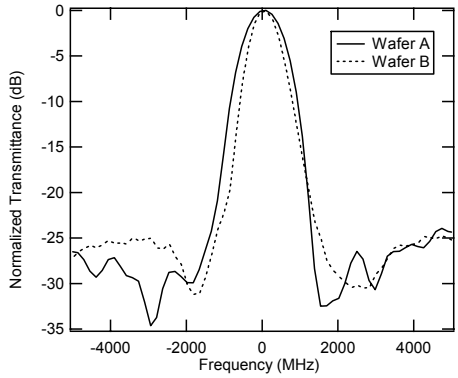

Fig. 10. Measured passband from two filters fabricated on two different wafers.

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VI. ELECTRONICS

The primary focus of the electronics for the EPIC program is to develop CMOS circuit topologies that fully exploit the accompanying integrated photonics. The integration of electronics and photonics on the same die relieves many of the bottlenecks typically encountered at the electronic-photonic interface. Consequently design challenges are shifted to other parts of the circuit.

Electronic-photonic interface circuits include optical modulator drivers and optical receivers. There is extensive literature covering these types of circuits, though they generally cover the use of photonics for telecom and datacom digital communication links. Circuit topologies for applications of photonics in analog and microwave systems are less common, and are the focus of this project. The types of circuits we are investigating include broadband modulator drivers and linear transimpedance amplifiers (TIA) for microwave applications. While major design concerns including gain, bandwidth, and noise are familiar from the more common digital implementations, microwave systems also need to preserve the analog integrity of the signals passing through them, requiring high linearity and dynamic range.

A. Modulator Driver

A microwave optical modulator driver accepts an input signal and conditions that signal for delivery to an optical modulator. Although, the input signal can be delivered directly to the modulator, a driver circuit can potentially extend the dynamic range of the modulator through reduced noise. Noise can be improved in two ways including cascaded noise figure reduction and removal of the typically noisy impedance matching network required in the absence of a driver.

In cascaded systems such as a microwave photonic link, placing a low noise amplifier in front of a noisy block reduces the effect of the offending noise via Friis' Formula:

$$F_{tot} = F_1 + \frac{1-F_2}{A_1} + \frac{1-F_3}{A_1 \cdot A_2} + \cdots$$

where F_i and A_i represent the noise factor and gain, respectively, of the ith block in the chain. This typically results in the noise of the cascade being dominated by the first block, in this case a driver designed to have low noise.

In the absence of a driver, some form of impedance matching is required at the modulator. This matching is often implemented by a resistor to cover a wide frequency band. However, such a resistor has thermal noise. If the modulator has large or small impedance relative to 50Ω, the matching resistor must be 50Ω resulting in a noise figure of at least 3dB. With an integrated driver circuit, matching can be designed into the driver input and the noisy matching resistor will not be necessary.

The primary topology we have investigated for a modulator driver is the distributed amplifier (DA) as shown in Fig. 11. The distributed amplifier is well known for breaking the traditional gain-bandwidth tradeoff encountered in lumped element amplifier design by creating a gain-delay tradeoff instead [12,13]. By using transmission lines to carry the input and output signals to spatially separated gain blocks in a temporally synchronized way, the circuit provides useful gain up to and beyond the unity gain frequency of the FET (f_T). This effect allows the designer to extract the maximum bandwidth available from the CMOS to fully utilize the broadband photonics on chip.

Noise figure can be below 3dB over most of the bandwidth of a DA, although very low and very high frequencies typically have higher noise than mid-band. Fig. 12 shows the simulated noise figure of a 20GHz monolithic DA in 180nm CMOS. The excess noise at low frequencies and near the 20GHz cutoff is evident. We are investigating techniques targeted at reducing the excess noise at low frequency.

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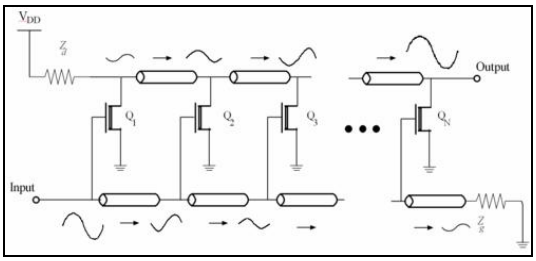

Fig. 11. Basic distributed amplifier

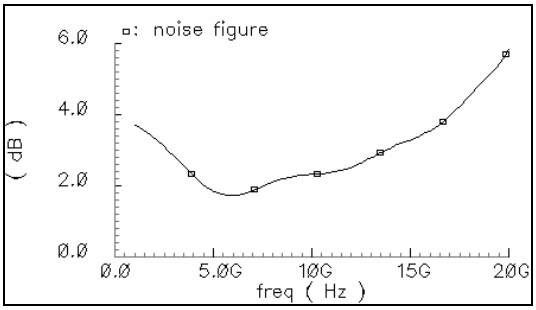

Fig. 12. Simulated noise figure of a monolithic CMOS distributed amplifier

B. Optical Receiver

As with the modulator driver, we are looking at microwave solutions to what is usually a digital problem – conveying the photocurrent output of a photodetector to the off-chip world. A transimpedance amplifier (TIA) is the natural choice to convert a small photocurrent to a large voltage with high bandwidth and low noise. The new challenge lies in developing a high dynamic range (high linearity and low noise) TIA that operates over a large bandwidth.

The traditional resistive feedback TIA (Fig. 13) is a natural starting point for a microwave optical receiver as negative feedback with a linear resistor has potential to provide high linearity in addition to low noise and large bandwidth. We have also developed a common-source feedback (CSFB) TIA (Fig. 14) which uses common-source active feedback instead of resistive feedback [14]. This topology pre-distorts the incoming photocurrent with the FET I-V curve. Following such a TIA with a common-source voltage gain stage corrects the pre-distortion via the FET's V-I curve, delivering an undistorted and amplified version of the photocurrent into a linear passive load. Analysis and simulation show that this topology can potentially simultaneously improve gain, bandwidth, noise, and linearity over traditional resistive feedback.

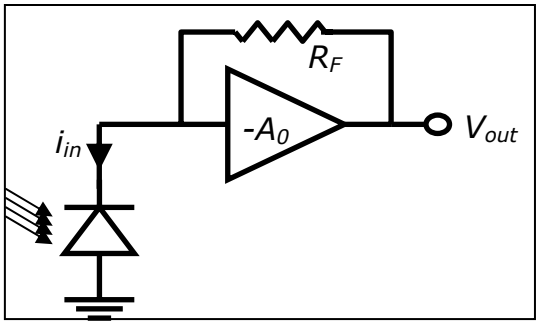

Fig. 13. Resistive feedback TIA

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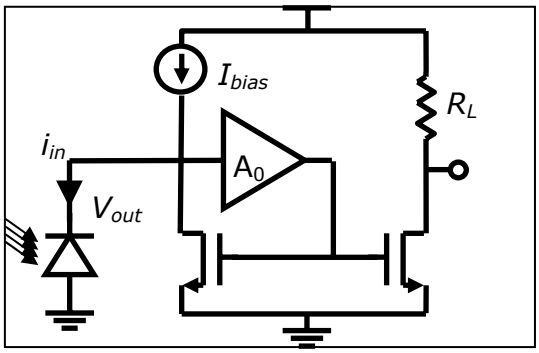

Fig. 14. Common-source feedback (CSFB) TIA

VII. CONCLUSIONS

We have reported on the progress in optical and electronic device performance for the CMOS implementation of an Application Specific Electronic Photonic Integrated Circuit (AS-EPIC). Our chip performs a RF channelization function that is equivalent to a Fast Fourier Transform in the time regime. We have implemented device design rules, process integration design rules, and an optical signal processor link consisting of waveguide, optical modulator, optical time domain filter, couplers, and photodetectors for CMOS implementation. The devices and circuits perform at state-of-the-art levels. The waveguide coupled germanium photodetectors reach a bandwidth of 7.5GHz with > 90% external quantum efficiency under an applied bias of <1V at a photon wavelength of 1550nm. The optical filters show passbands with 3-dB bandwidths from 0.8 GHz to 2.4 GHz. The stopband rejection is >25 dB and the filter insertion loss is <6 dB. Modulator drivers and optical receivers have been designed for low noise and are currently fabricated.

ACKNOWLEDGMENT

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