

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD., SAMSUNG ELECTRONICS
AMERICA, INC., SAMSUNG SEMICONDUCTOR, INC., and SAMSUNG
AUSTIN SEMICONDUCTOR LLC,

Petitioner

v.

W&WSENS DEVICES INC.,

Patent Owner

Case IPR2025-00997

Patent No. 9,525,084

PETITION FOR *INTER PARTES* REVIEW

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PETITIONER’S EXHIBIT LIST

Exhibit	Description
Ex-1001	U.S. Patent No. 9,525,084 B2 to Wang et al. (“’084 patent”)
Ex-1002	Declaration of Dr. Michael Lebby, Ph.D. (“Lebby”)
Ex-1003	Prosecution History of the ’084 patent (downloaded from Patent Center)
Ex-1004	Japanese Patent Application Publication No. JP2002-314116A to Harada et al. (“ <i>Harada</i> ”)
Ex-1005	Japanese Patent Application Publication No. JP2007-129024A to Hasegawa (“ <i>Hasegawa</i> ”)
Ex-1006	European Patent Application EP 2 172 974 A1 to NXP B.V. (“ <i>NXP</i> ”)
Ex-1007	Nor Afifah Yahaya et al., <i>Characterization of light absorption in thin-film silicon with periodic nanohole arrays</i> , Optics Express, Vol. 21, No. 5 (Mar. 2013), pp. 5924-30 (“ <i>Yahaya</i> ”)
Ex-1008	Xianqin Meng et al., <i>Design, fabrication and optical characterization of photonic crystal assisted thin film monocrystalline-silicon solar cells</i> , Optics Express, Vol. 20, No. S4 (July 2012), pp. A465-75 (“ <i>Meng</i> ”)
Ex-1009	U.S. Patent Application Publication No. 2012/0146172 A1 to Carey et al. (“ <i>Carey</i> ”)
Ex-1010	Zhihong Huang et al., <i>Microstructured silicon photodetector</i> , Applied Physics Letter, Vol. 89 (2006), pp. 033506-1 to -3.
Ex-1011	Richard A. Myers et al., <i>Enhancing near-infrared avalanche photodiode performance by femtosecond laser microstructuring</i> , Applied Optics, Vol. 45, No. 35 (Dec. 2006), pp. 8825-31.
Ex-1012	Abbas El Gamal et al., <i>CMOS Image Sensors</i> , IEEE Circuits & Devices Magazine (2005), pp. 6-20.
Ex-1013	Eric R. Fossum, <i>CMOS Image Sensors: Electronic Camera-On-A-Chip</i> , IEEE Transactions on Electron Devices, Vol. 44, No. 10 (Oct. 1997), pp. 1689-98.

Exhibit	Description
Ex-1014	Sunetra Mendis et al., <i>CMOS Active Pixel Image Sensor</i> , IEEE Transactions on Electron Devices, Vol. 41, No. 3 (Mar. 1994), pp. 452-53.
Ex-1015	Renato Turchetta et al., <i>Introduction to CMOS Image Sensors</i> ,” Molecular Expressions™ Optical Microscopy Primer: Digital Imaging in Optical Microscopy - Introduction to CMOS Image Sensors (July 16, 2004), pp. 1-9, <i>available at</i> https://web.archive.org/web/20120508153832/https://micro.magnet.fsu.edu/primer/digitalimaging/cmosimagesensors.html
Ex-1016	U.S. Patent Application Publication No. 2008/0259981 A1 to Wang et al. (“ <i>Wang</i> ”)
Ex-1017	“Optical storage”. <i>Encyclopedia Britannica</i> , 9 Jul. 2020, https://www.britannica.com/technology/optical-storage . Accessed 25 June 2025
Ex-1018	Reserved
Ex-1019	Reserved
Ex-1020	Japanese Patent Application Publication JP2007-165359A to Makita (“ <i>Makita</i> ”)
Ex-1021	Jerald G. Graeme, <i>Photodiode Amplifiers Op Amp Solutions</i> (McGraw Hill 1996).
Ex-1022	Japanese Patent Application Publication JP2008-311562A to Obara et al. (“ <i>Obara</i> ”)
Ex-1023	Joseph R. Kiniry, <i>WAVELENGTH DIVISION MULTIPLEXING: Ultra High Speed Fiber Optics</i> , IEEE Internet Computing, Vol. 2, No. 2 (Mar.-Apr. 1998), pp. 13-15.
Ex-1024	Declaration of June Ann Munford
Ex-1025	Reserved
Ex-1026	Reserved
Ex-1027	Reserved
Ex-1028	Reserved

Exhibit	Description
Ex-1029	Jurgen Michel et al., <i>Advances in fully CMOS integrated photonic devices</i> , Proceedings of SPIE, Vol. 6477 (2007), pp. 64770P-1 to -11 (“ <i>Michel</i> ”).
Ex-1030	Mark Beals et al., <i>Process Flow Innovations for Photonic Device Integration in CMOS</i> , Proceedings of SPIE, Vol. 6898 (2008), pp. 689804-1 to -14 (“ <i>Beals</i> ”).

I. Preliminary Statement

Petitioner Samsung Electronics Co., Ltd.; Samsung Electronics America, Inc.; Samsung Semiconductor, Inc.; and Samsung Austin Semiconductor LLC (collectively, “Samsung”) requests *inter partes* review of U.S. Patent No. 9,525,084 (Ex-1001) and cancellation of claims 1-9, 11-15, 17-21, and 24.

The challenged claims pertain to a single-chip device with a photodetector and an electronic processor on a single substrate. The photodetector, called a microstructure-enhanced photodetector (“MS-PD”) in the ’084 patent, features a plurality of holes to increase light absorption. However, photodetectors with holes, and integration with an electronic processor on a single substrate, were widely known characteristics of CMOS sensors. For example, *Harada* (Ex-1004) and *Hasegawa* (Ex-1005), which were not considered during prosecution, disclose and/or render obvious all recited features of the microstructure-enhanced photodetector, and disclose that it was known to integrate a photodetector and an electronic processor on the same substrate.

Other features of the challenged claims were known before the ’084 patent priority date. For example, it was known to use photodetectors for optical data communication, and that optical data communication involved modulating a source signal with imprinted data, as taught by *Hasegawa*. It was also widely known to apply a reverse-bias voltage to a photodetector to sweep electrical charges out of

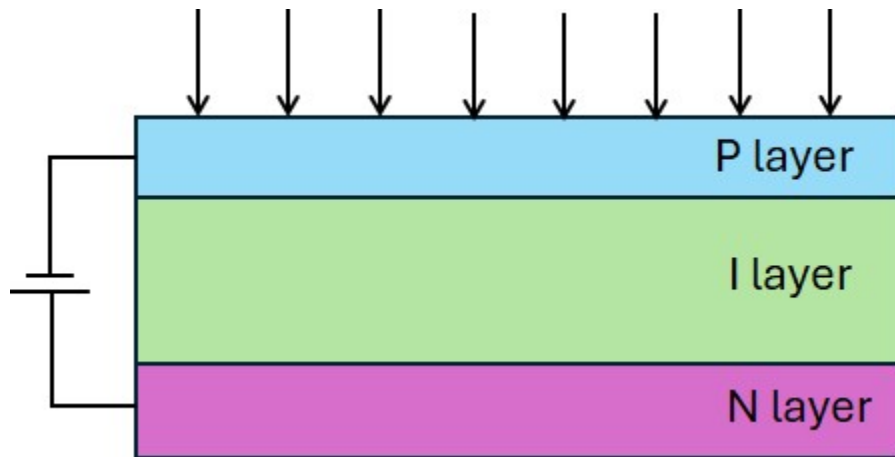
the photo absorption layer, as disclosed in *Harada* and *Hasegawa*. The challenged claims also recite various dimensions, signal wavelengths, and associated absorption percentages. The prior art, such as *Yahaya* (Ex-1007), demonstrates that the claimed absorption percentages were known for such wavelengths, dimensions and photodetector configurations, including those of *Harada* and *Hasegawa*.

As detailed below and in the supporting declaration of Dr. Michael Lebby, Ph.D. (“Lebby”) (Ex-1002), the challenged claims are unpatentable over the cited prior art. The Board should institute review and cancel all challenged claims.

II. State of the Art

A. Photodetectors

A photodetector is a semiconductor device that transforms photons into electrical signals, enabling electrical circuits to detect and measure incident light. Lebby, ¶51. As illustrated below, a PiN photodetector is a specific type of photodiode characterized by an **intrinsic (undoped) layer** positioned between highly doped **P-type** and **N-type** semiconductor layers (hence “**PiN**”):



When light enters the photodetector, photons are absorbed in the intrinsic layer, generating electron-hole pairs. Applying a reverse bias across the photodetector causes the separated electrons to move towards the N-type layer and the holes towards the P-type layer, producing a measurable photocurrent. Lebbly, ¶52.

B. Microstructure-Enhanced Photodetectors

Conventional silicon photodetectors exhibit high responsivity at light wavelengths below about 850 nm. Ex-1010, 1; Lebbly, ¶53. Although other materials detect longer wavelengths, silicon was widely preferred for its lower cost and ease of manufacturing. '084 patent, 1:61-2:18. The prior art recognized that creating microstructures in silicon increases sensitivity and efficiency and extends the operability of these photodetectors to longer wavelengths. For instance, etching the silicon photodetector to create micron-sized pillars or grooves in the surface was known to enhance a photodetector's responsiveness and efficiency at longer wavelengths. Ex-1010, 1-2; Ex-1011, 1-6; Lebbly, ¶53.

Photodetectors featuring microstructures enhanced by etched holes were known well before the '084 patent's priority date. Lebbby, ¶54; Ex-1016, [29]-[32], Figs. 1-2. Integrating photodetectors and signal processing circuitry on a single substrate to form a single-chip device was also known. Ex-1012, 1-14; Ex-1013, 1-8; Ex-1014, 1-2; Ex-1015, 1-5. For example, *NXP* discloses a single-chip device 1300 where a microstructure-enhanced silicon **PiN** photodiode is integrated with CMOS signal-processing circuitry (not shown) on a single substrate 102. *NXP*, ¶¶[15]-[16], [32]-[37], [42]. This **PiN** photodiode includes an **intrinsic layer** 710 disposed between an **N⁺ layer** 708 and a **P⁺ layer** 712, and **pores** 106 (holes) formed on the **PiN** layers by etching:

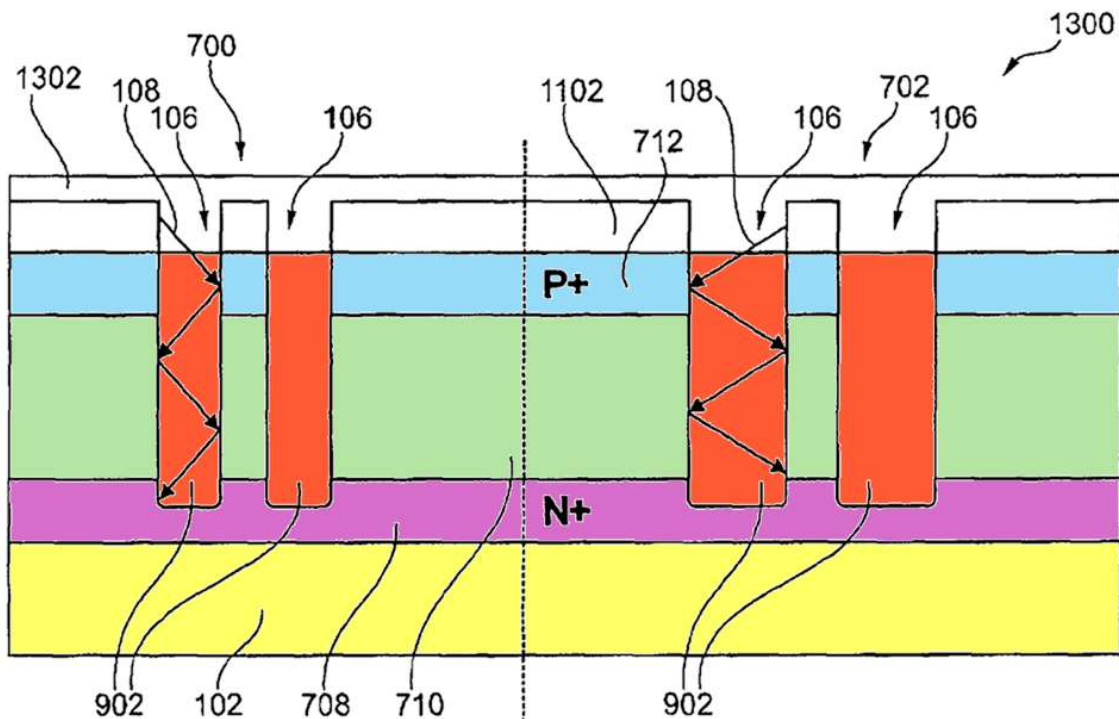


Fig. 13

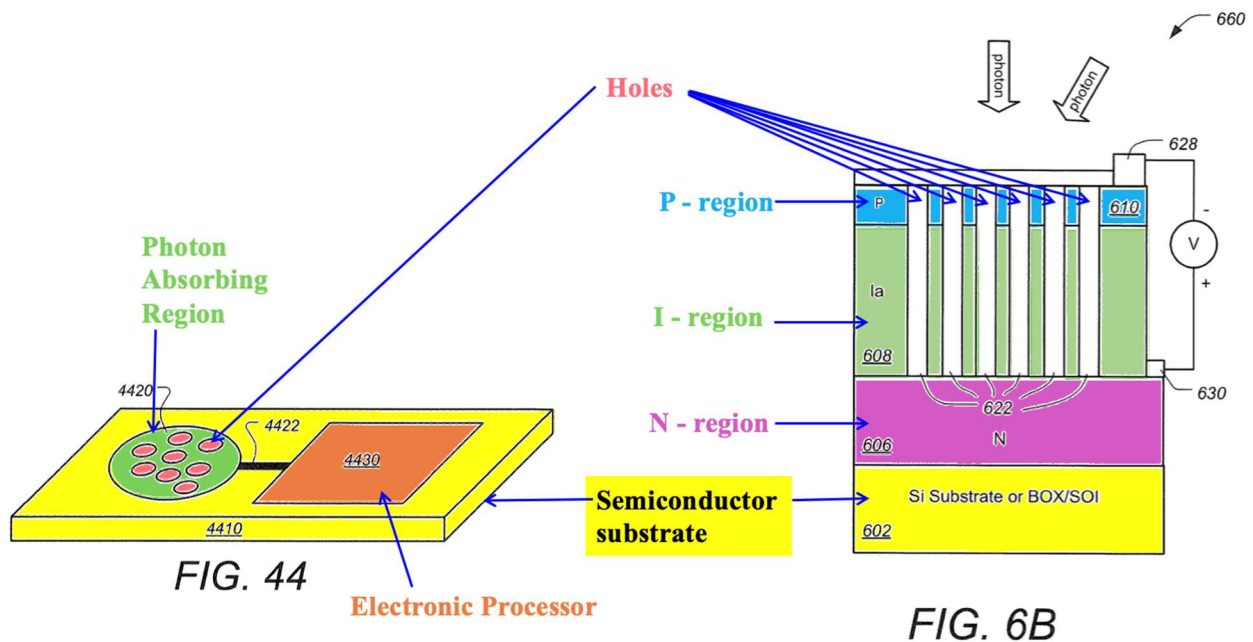
NXP, Fig. 13,¹ ¶¶[77]-[78]. Pores 106 increase the photodiode's quantum efficiency—a measure of the photodiode performance that relates to absorption.

NXP, ¶¶[13], [38]; Lebbby, ¶¶55-63.

III. The '084 Patent

A. Specification

The '084 patent details a single-chip device that integrates photodetectors (referred to as MS-PDs and MS-APDs) with an electronic processor on a semiconductor substrate. Lebbby, ¶64.



'084 patent, 4:47, 18:39-59, 29:64-30:5, Figs. 44 (left), 6B (right).

¹ All color and colored annotations have been added.

These photodetectors include a silicon substrate with a first region (P layer), an intermediate layer called the intrinsic region (i region), and a second region (N region) with holes etched in at least the intrinsic region toward the substrate. *Id.*, 18:39-59, 19:14-44, Fig. 6B. An optical source signal impinges on the photodetectors' top and/or bottom surfaces. *Id.*, Figs. 6B, 7B. The holes extend into the light absorbing layer(s), enhancing light absorption and increasing external quantum efficiency over a similar structure without holes. *Id.*, 12:65-13:60. Figure 44 (above) shows the photodetector integrated with an electronic processor (e.g., CMOS or ASIC) on the same substrate to form a single-chip device. *Id.*, 29:64-30:5, Fig. 44; Lebbby, ¶¶64-65.

B. Claim Construction

The Board construes claims per *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005) (en banc). 37 C.F.R. §42.100(b). Claims must be construed only to the extent necessary to resolve a controversy. *Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017). Here, no terms need construction to resolve the controversy.²

² Petitioner retains the right to contend in another proceeding that certain limitations are indefinite.

IV. Statement of Precise Relief Requested

A. Prior Art

The application for the '084 patent was filed on November 18, 2015, claiming priority to provisional applications as early as November 18, 2014.³ The earliest claimed priority date is November 18, 2014.

- *Harada* (Ex-1004), Japanese Patent Application Publication JP2002-314116A, which published on October 25, 2002, is prior art under AIA 35 U.S.C. §102(a)(1).
- *Hasegawa* (Ex-1005), Japanese Patent Application Publication JP2007-129024A, which published on May 24, 2007, is prior art under AIA 35 U.S.C. §102(a)(1).
- *NXP* (Ex-1006), European Patent Application Publication EP2172974A1, which published on April 7, 2010, is prior art under AIA 35 U.S.C. §102(a)(1).
- *Yahaya* (Ex-1007), a publication titled *Characterization of Light Absorption in Thin-Film Silicon with Periodic Nanohole Arrays*, was published and made publicly available by March 11, 2013, in *Optics Express*, Vol. 21, No. 5. Ex-1007; Ex-1024. *Yahaya* was publicly

³ Petitioner retains the right to dispute the claimed priority in another proceeding.

available soon after its publication in March 2013, including at the Penn State University Library in March 2013, on the website <http://www.opticsinfobase.org> in May 2013, and at an Optics InfoBase website no later than May 26, 2013. Ex-1024, ¶¶13-20. It is therefore prior art under AIA 35 U.S.C. §102(a)(1).

B. Challenges

Ground	Challenged Claims	Basis	Prior Art
1	1-9, 11-15, 17-21, and 24	§103	<i>Harada</i> in view of <i>Hasegawa</i>
2	7	§103	<i>Harada</i> in view of <i>Hasegawa</i> and <i>NXP</i>
3	5 and 14	§103	<i>Harada</i> in view of <i>Hasegawa</i> and <i>Yahaya</i>

Lebby, ¶¶75-77.

V. Level of Ordinary Skill in the Art

A person of ordinary skill in the art (“POSITA”) would have had at least a master’s degree in electrical engineering or a similar field and at least five years of experience working with semiconductor systems and semiconductor dice. Lebby,

¶¶72-74. Additional relevant work experience can compensate for less education, and vice versa. *Id.*

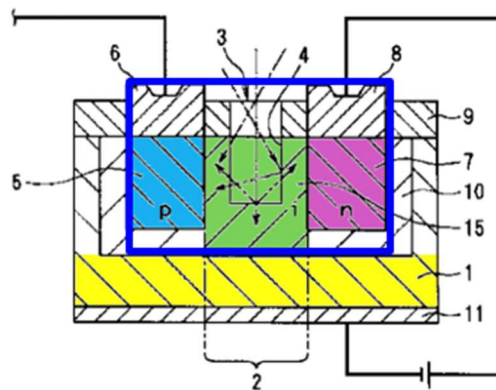
VI. The Challenged Claims Are Unpatentable

A. Ground 1: Claims 1-9, 11-15, 17-21, and 24 Are Obvious over *Harada* in View of *Hasegawa*

1. Overview of the Prior Art and Motivation to Combine

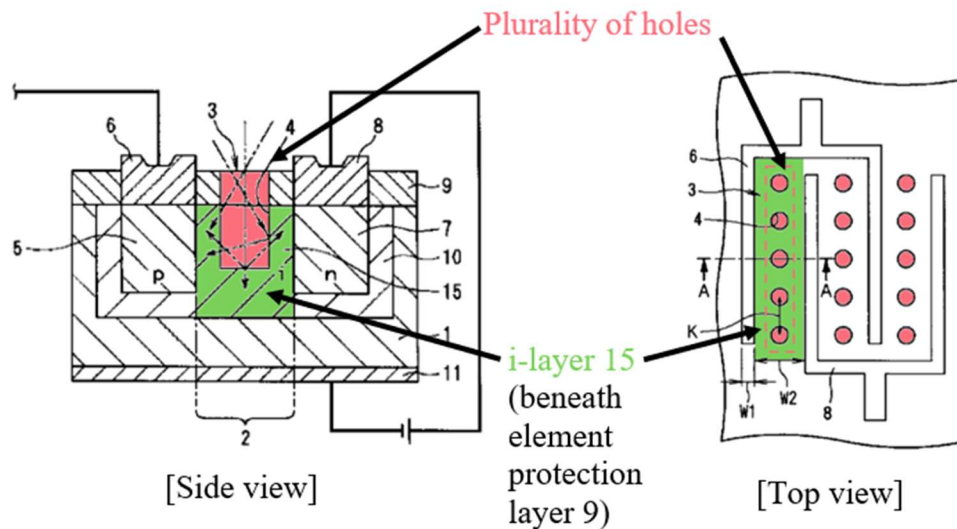
a. Overview of *Harada*

Harada discloses a “lateral-type semiconductor light-receiving element having a PIN structure.” *Harada*, Title, [1]; Lebby, ¶78. *Harada*’s light-receiving element is a **PiN photodiode** having a **p-layer 5**, an **i-layer 15**, and an **n-layer 7** formed on a **silicon semiconductor substrate**:



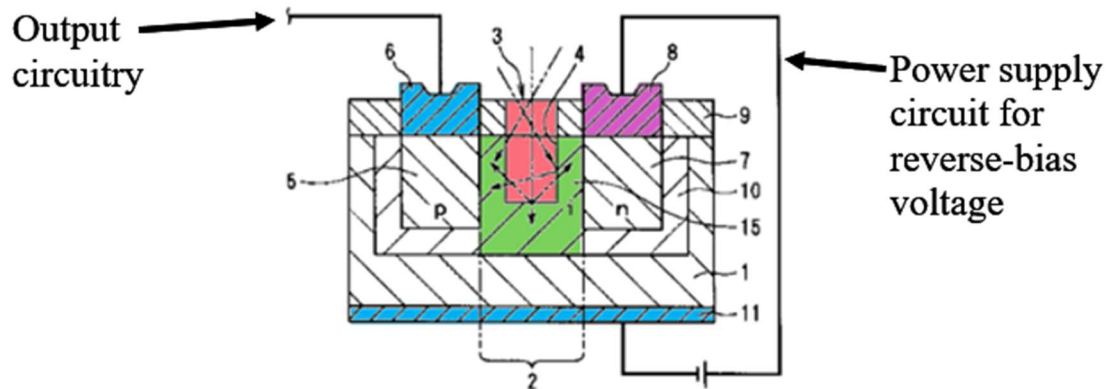
Harada, Fig. 1, [10]. The PiN photodiode receives “high-speed light signals” and improves upon conventional photodiodes that receive signals of 700-870 nm wavelength. *Harada*, [3], [7]; Lebby, ¶78.

Harada discloses improving a PiN photodiode's light-receiving sensitivity by creating a plurality of holes 4 in the light-receiving surface 3 and i-layer 15:



Harada, [7]-[10], [13]-[17], Figs. 1 (left), 2 (right). “[B]y providing the holes 4, the light-receiving efficiency at the light-receiving region 2 becomes high, which improves light-receiving sensitivity and also increases response speed.” *Harada*, [17]; Lebby, ¶79.

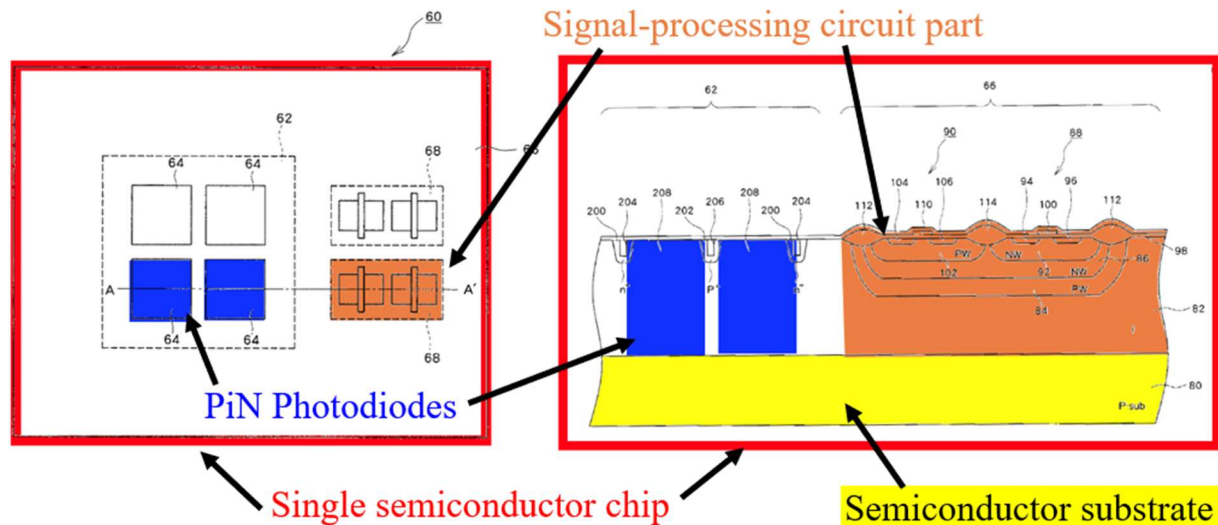
Harada discloses that p-electrode 6 (associated with p-layer 5) connects to an output circuit. *Harada*, [15]. And n-electrode 8 (associated with n-layer 7) connects to a power supply to apply a reverse-bias voltage and enables the photodiode to detect light by converting incident light to an electric current for processing.



Harada, Fig. 1, [15]; Lebby, ¶80.

b. Overview of *Hasegawa*

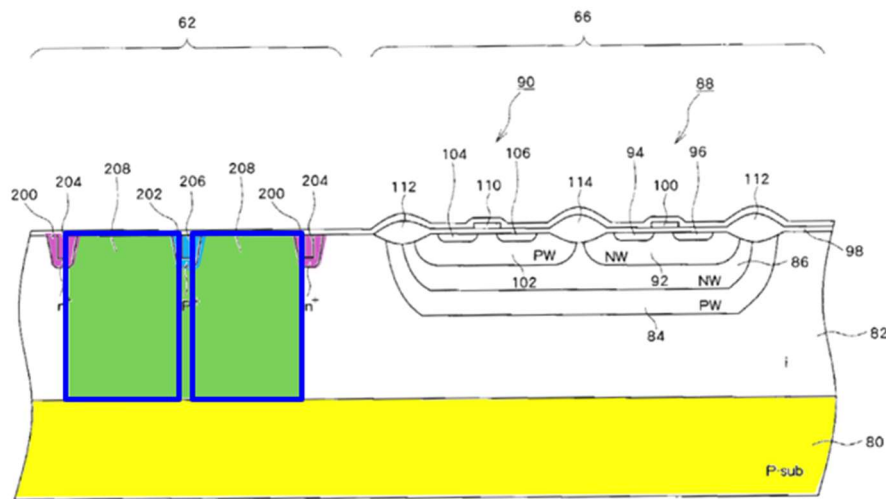
Hasegawa's photodetector is a **single semiconductor chip** that includes **PiN photodiodes** and **signal-processing circuits** formed on the same **semiconductor substrate**.



Hasegawa, Abstract, [14], [42], Figs. 1 (left), 7 (right). The **single semiconductor chip** (60 above) has a **light-receiving portion 62** that includes four **photodiodes 64**

(photodetectors) and a signal-processing circuit part 66 that includes CMOS devices 68. A portion of the signal-processing circuit part is associated with one or more of the photodiodes. Hasegawa's photodiodes detect laser light reflected off an optical disc and receive recorded data from the optical disc at a high data rate. Hasegawa, [2]-[6], [9]; Lebby, ¶¶81-82.

Within each photodiode is a p-type anode well 84 and an n-type cathode well 86 at the sides of a photo absorption i-layer:



Hasegawa, [32], [42], [46]-[47], [52], Figs. 7 (above), 8. Each photodiode connects via wiring to signal-processing circuitry, such as CMOS devices 68 and operational amplifiers 122 (“op amp”). Hasegawa, [16], [22], [26], Figs. 1-2, 4, 7-8. Hasegawa applies a reverse-bias voltage to the photodiodes by connecting the anode and cathodes to circuitry that applies a positive voltage V_b to the cathode regions. Hasegawa, [5]-[9], [26]-[27], [46]-[47], Figs. 1, 7-8; Lebby, ¶83.

To achieve high-speed operation while minimizing noise and current leakage, *Hasegawa* (1) locates the signal-processing circuit part close to the photodiodes so that the wiring is “as short as possible”; and (2) provides the p-type and n-type wells at the photodiodes’ sides to prevent current leakage from the absorption i-layer. *Hasegawa*, [9], [32], [42], [52]; Lebby, ¶84.

c. Motivation to Combine *Harada* with *Hasegawa*

It would have been obvious to combine *Harada*’s PiN photodiode (“photodetector”) with *Hasegawa*’s integrated processing circuit onto a single substrate. Lebby, ¶85.

Harada and *Hasegawa* are analogous art to the ’084 patent because they are reasonably pertinent to addressing at least one problem in silicon-based photodetectors by improving absorption and/or response time of silicon-based photodetector devices, such as PiN photodiodes and single semiconductor devices having photodetectors that receive high-speed light signals. ’084 patent, Abstract, 1:44-2:18, 18:29-38; *Harada*, Abstract, [7], [10]-[17]; *Hasegawa*, Abstract, [6]-[10], [12]-[14], [22]-[23]; Lebby, ¶86. *Harada* and *Hasegawa* are in the same field of endeavor as the ’084 patent because they address drawbacks in silicon-based photodetector devices. Lebby, ¶86. *Harada* discloses a photodiode with holes for enhancing light-receiving sensitivity, and *Hasegawa* forms signal-processing

circuitry and at least one photodiode on the same substrate to minimize noise and power requirements for high-speed optical data communication. *Id.*

A POSITA would have been motivated to combine *Harada*'s microstructure-enhanced photodiode with *Hasegawa*'s signal-processing circuitry. Leebby, ¶87. The combination would have entailed combining known elements, including *Harada*'s microstructure-enhanced photodiodes and *Hasegawa*'s signal-processing circuitry, to form a combined device as taught by *Hasegawa*. *Id.* Such a combination would have involved using known methods of forming a photodiode and processing circuitry on a single substrate, and yield predictable results as discussed below. *Id.* Alternatively, the combination would have involved forming *Harada*'s enhanced photodiodes in *Hasegawa*'s device's light-receiving part, which lacks microstructure-enhanced absorption, yielding *Harada*'s enhanced photodiodes in place of *Hasegawa*'s photodiodes 64. *Id.*

The benefits of integrating photodetectors and signal-processing circuitry on a single substrate to form a single-chip device, as taught by *Hasegawa*, were well understood. Leebby, ¶88; Ex-1012, 1-14; Ex-1013, 1-8; Ex-1014, 1-2. For instance, integrating signal-processing circuitry and photodiodes on the same substrate “may be more reliable” and advantageously result in a smaller package (for mobile applications). *NXP*, ¶¶[16], [32], [37]; Leebby, ¶88. Using an integrated device to receive and process optical data signals also reduces manufacturing costs and

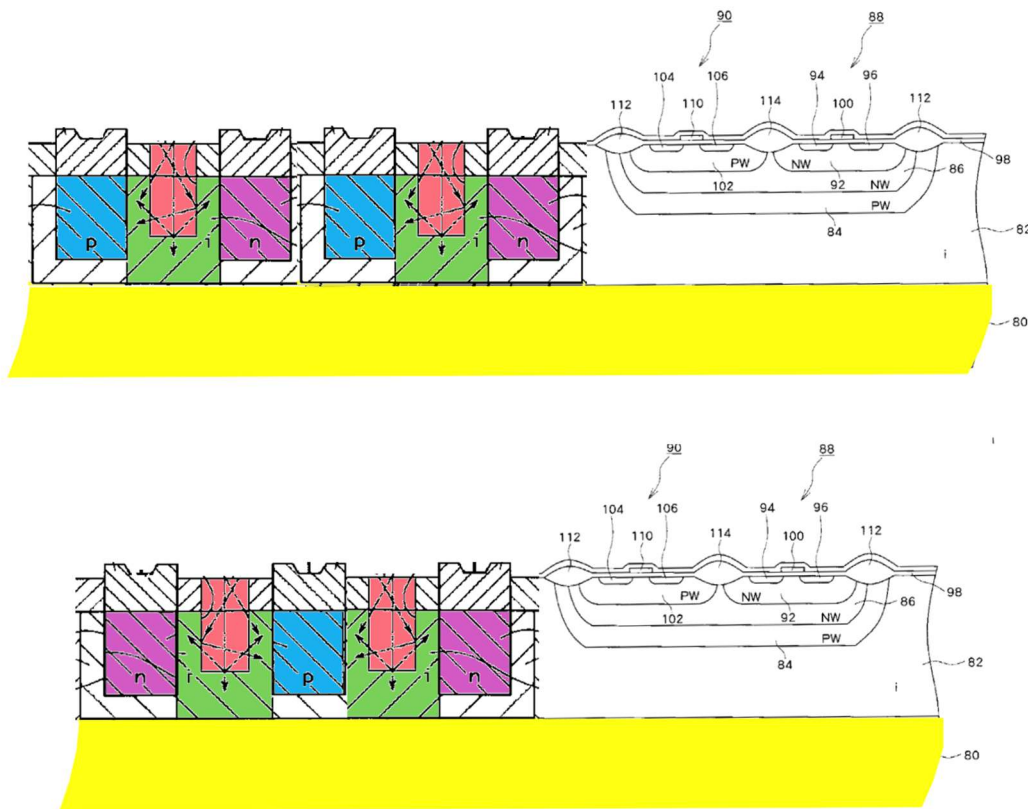
power requirements, while maintaining high data speeds. *Hasegawa*, [9]-[10], [12], [26], [46]. A POSITA would have been motivated to make smaller packages that reduce manufacturing costs and power requirements, while maintaining high data speeds. Lebbby, ¶88.

The *Harada-Hasegawa* combination (“*Harada-Hasegawa*”) would have positioned signal-processing circuitry close to the photodetector, enabling the wiring to be “as short as possible.” *Hasegawa*, [9]. According to *Hasegawa*, short connections advantageously “curtail[] attenuation of the photo-electrical conversion signals” and “suppress[] the superimposition of noise.” *Id.*; Lebbby, ¶89

Similarly, implementing *Harada*’s enhanced photodiode in *Hasegawa*’s device would increase the light-receiving performance and response speed of the photodiodes when used with *Hasegawa*’s signal-processing circuit. Lebbby, ¶90. *Harada*’s photodiode’s enhanced light sensitivity would have improved the light-detecting performance of *Hasegawa*’s integrated device when used for receiving and processing high data rate optical signals from an optical disc. *Hasegawa*, [6], [9]-[10], [12]; Lebbby, ¶90.

A POSITA would have found it obvious to combine *Harada*’s microstructure-enhanced PiN photodiode with *Hasegawa*’s signal-processing circuitry in various configurations without departing from *Harada*’s or

Hasegawa's disclosures. Lebbby, ¶91. For example, it would have been obvious to form a single semiconductor device in either configuration below:

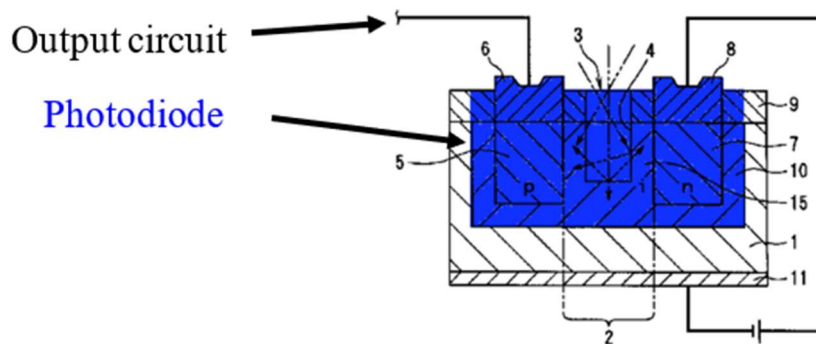


Diagrams A (top) and B (bottom) illustrating exemplary Harada-Hasegawa combinations, based on Harada's Figure 1 and Hasegawa's Figure 7

In the upper diagram, *Hasegawa*'s photodiodes are replaced with a complete *Harada* photodiode having a separate p-layer for each photodiode. Lebbby, ¶91. In the lower diagram, *Harada*'s photodiodes share a common p-layer, similar to *Hasegawa*'s Figure 7. *Id.* Both configurations show *Harada*'s photodiodes extending to the depth of *Hasegawa*'s substrate layer 80, but a POSITA would

have understood that the photodiode's size and dimensions would vary depending on design requirements and targeted wavelengths. *Id.*

Additionally, a POSITA would have been motivated to connect *Harada's* photodiode's output circuit to *Hasegawa's* signal-processing circuitry. Lebbby, ¶92. *Harada's* photodiode is a photodetector that converts light to current and then outputs an electrical signal via an output circuit:



Harada, [15], Fig. 1. A POSITA would have understood that *Harada's* output circuit would have connected to processing circuitry, such as an electronic processor, for processing and interpreting the signal. Lebbby, ¶92. Indeed, it was well known to combine photodetectors with processing circuitry in devices known as optoelectronic integrated circuits (OEICs). *Obara*, [110]. *Harada's* photodiode also connects to a voltage supply to provide a reverse-bias voltage. *Harada*, [15]; Lebbby, ¶92.

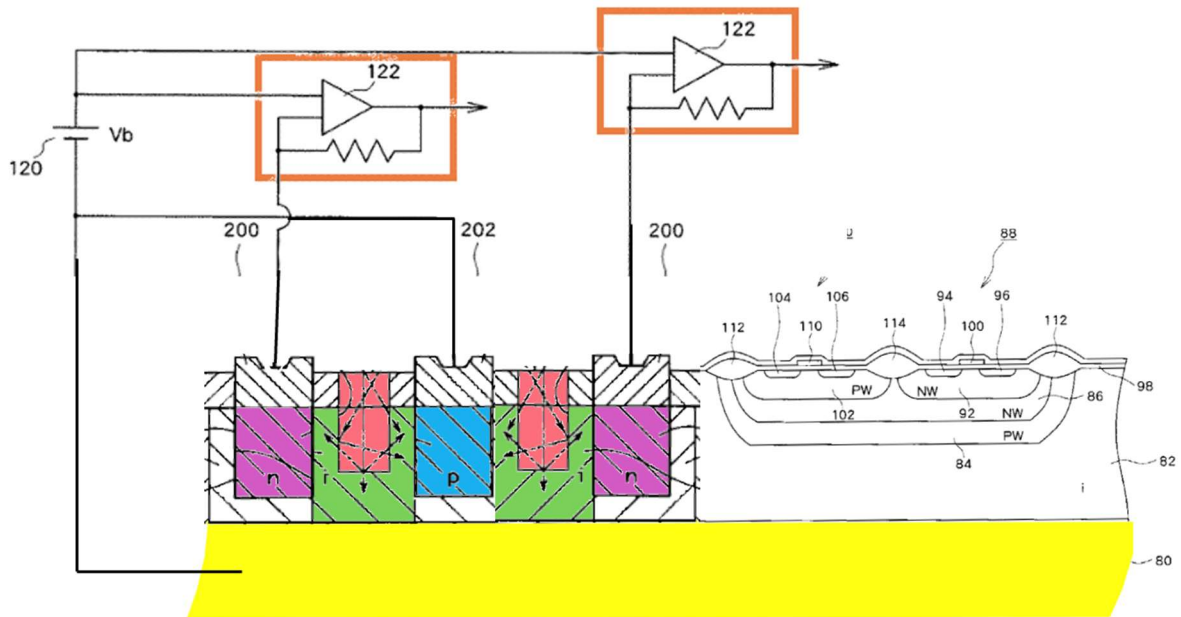
A POSITA would have reasonably expected success in combining *Harada's* photodiode with *Hasegawa's* integrated signal-processing circuit. Lebbby, ¶93. A

POSITA would have understood that forming holes in a PiN photodiode enhances light-receiving performance and understood the advantages of implementing the enhanced PiN photodiode in a single device that receives and processes light signals for data communication. Lebbby, ¶¶79, 93-94.

Harada-Hasegawa would have required minimal modification of *Harada*'s PiN photodiode. Lebbby, ¶95. Both references disclose silicon photodiode structures and similar PiN layouts with p-type and n-type impurity regions arranged horizontally, using CMOS-compatible processes. *Harada*, [4], [10]-[13]; *Hasegawa*, Abstract, [14]-[15], [18], [39], [42], [52], Figs. 3, 7-8. The same semiconductor materials and processes used to fabricate *Harada* and *Hasegawa*, individually, would have been used to fabricate *Harada-Hasegawa*. Lebbby, ¶95. Any modifications would have been within a POSITA's knowledge, including connecting *Harada*'s output circuit wiring to *Hasegawa*'s signal-processing circuitry. *Id.*

Indeed, *Hasegawa*'s diagrams and disclosure would have led a POSITA to form a single semiconductor chip having both *Harada*'s silicon photodiode as well as CMOS signal-processing circuitry. *Hasegawa*, [10]-[13], [22]-[26], [46], [55], Figs. 1-8; Lebbby, ¶96. A POSITA would have been guided by *Hasegawa*'s disclosures of connecting cathode and anode regions to signal-processing circuitry

part, such as by connecting *Harada's* PiN photodiodes to op amps, as taught by *Hasegawa*:



Exemplary connections of Harada's PiN photodiodes connected to Hasegawa's op amps 122, based on Harada's Figure 1 and Hasegawa's Figures 7-8

Hasegawa, [15]-[17], [26], [42], [46], Figs. 2-3, 7-8; Lebbby, ¶96. A POSITA would have connected *Harada's* P-type and N-type electrodes to *Hasegawa's* reverse-bias voltage connections without significant modification to *Harada's* photodiode or *Hasegawa's* circuitry. *Harada*, [15], Fig. 1; *Hasegawa*, [26], [46]-[47], Figs. 2-4, 8; Lebbby, ¶96.

2. Independent Claim 1

- a. [1pre]: “An integrated detector/processor circuit for data communication comprising both a photodetector with microstructure-enhanced photoabsorption and an electronic processor formed into a single semiconductor chip, comprising:”

To the extent the preamble is limiting, *Harada-Hasegawa* renders it obvious. Lebbby, ¶97.

i. [1pre(i)]: “a circuit for data communication”

Harada alone or in view of *Hasegawa* discloses a “circuit for data communication.” Lebbby, ¶98. *Harada* discloses a “circuit for data communication” because its photodiode is used for receiving “high-speed light signals.” *Harada*, [7]; Lebbby, ¶98.⁴

It would have also been obvious to use *Harada*’s photodiode for data communication, as taught by *Hasegawa*. Lebbby, ¶98. *Hasegawa* discloses using a high-speed photodetector device for data communication, having photodiodes as an optical pickup mechanism to detect laser light reflected off an optical disc and to receive recorded data from the light signal at a high data rate. *Hasegawa*, [2]-[6], [9]-[10]; Lebbby, ¶98. *Harada* discloses enhancements to a photodiode

⁴ Petitioner’s “data communication” mapping is consistent with Patent Owner’s infringement contentions in the parallel litigation.

designed for receiving high-speed light signals, and it would have been obvious to utilize *Harada*'s photodiode for receiving light carrying recorded data from an optical disc at a high data rate, as taught by *Hasegawa*. Lebbby, ¶¶79, 99. The combination would have increased the functionality of *Harada*'s photodiode to include data communication involving light reflected off an optical disc. Lebbby, ¶100. The combination would have also improved the performance or efficiency of an optical pickup device, such as *Hasegawa*'s device, using *Harada*'s hole-enhanced photodiode. *Id.*

Indeed, additional prior art shows the benefits of using *Harada*'s photodiode for data communication. *Obara* discloses photodetectors used for optical pickup and for data communication that have holes ("cavities") formed in the photodetector to improve light-receiving performance to meet "demand[s] for higher-speed operation." *Obara*, Abstract, [2]-[3], [65], [68]; Lebbby, ¶101.

A POSITA would have understood that *Harada*'s photodiode may be used for data communication, as taught by *Hasegawa*. Lebbby, ¶102. To the extent necessary, modifying *Harada* for data communication would have involved applying *Hasegawa*'s known technique of receiving data by detecting laser light reflected off an optical disc to *Harada*'s PiN photodiode. *Id.* A POSITA would have had a reasonable expectation of success in applying *Hasegawa*'s teaching to *Harada* because *Harada*'s photodiode is designed for use with "high-speed light

signals.” *Harada*, [7]. Any modifications for using *Harada*’s photodiode as an optical pickup device for receiving recorded data communicated from an optical disc would have been within a POSITA’s skill. Lebbby, ¶102.

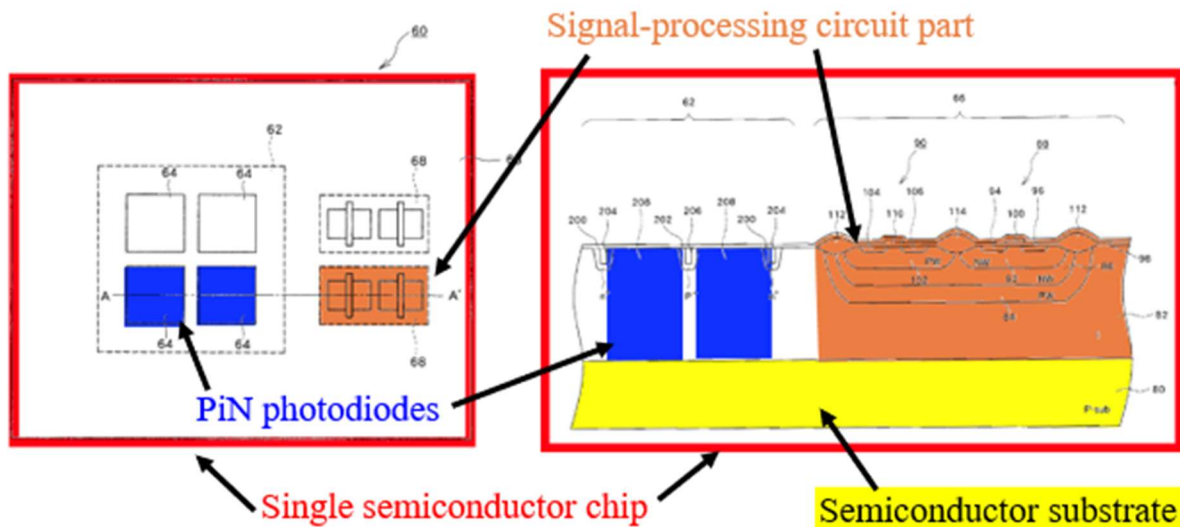
ii. [1pre(ii)]: “[a circuit ... comprising:] ... a **photodetector** with microstructure-enhanced photoabsorption”

Harada discloses a **photodiode** receiving light signals and therefore discloses a “**photodetector**.” *Harada*, [1], [7], [10], [15]-[16]; Lebbby, ¶103. *Harada*’s photodiode has holes in the light-receiving surface that increase the light-receiving surface area and efficiency. *Harada*, [10], [15]-[16]. *Harada* therefore discloses a photodetector “with microstructure-enhanced photoabsorption.” Lebbby, ¶103.

iii. [1pre(iii)]: “[an integrated detector/processor circuit ... comprising:] both a **photodetector** ... and an **electronic processor** formed into a **single semiconductor chip**”

Harada’s **photodiode** is a “**photodetector** with microstructure-enhanced photoabsorption.” VI.A.2.a.ii; Lebbby, ¶104.

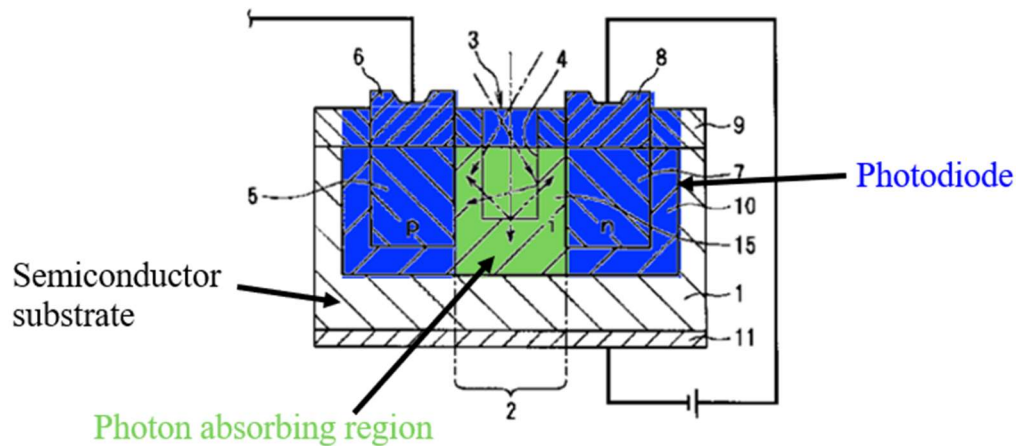
Harada-Hasegawa is an integrated detector/processor having **photodiodes** and **signal-processing circuit part** formed together on a single **semiconductor substrate** and into a **single semiconductor chip**. *Hasegawa*, Abstract, [9], [14], [22]-[23], [42].



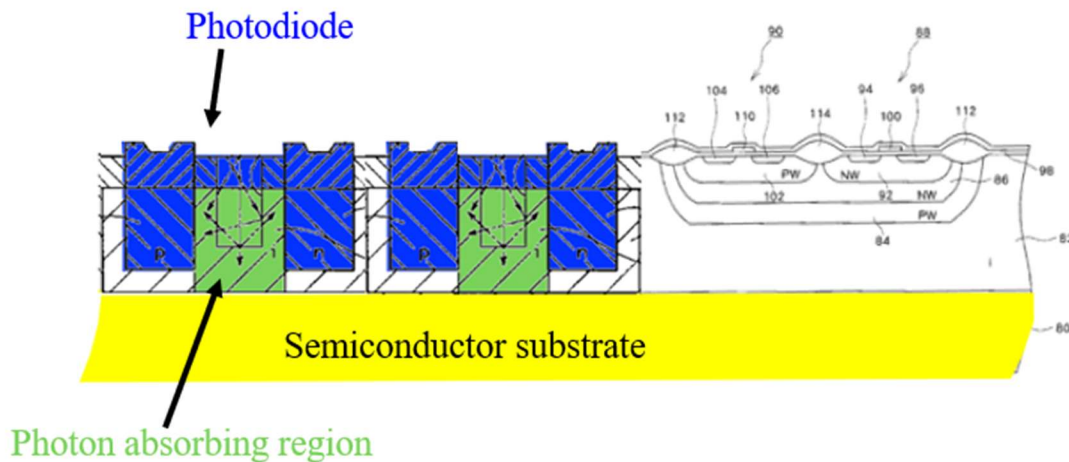
Hasegawa, Figs. 1 (left), 3, 7 (right); *Lebby*, ¶105. A portion of **signal-processing circuit part** is an “**electronic processor**” associated with a photodiode and includes components such as CMOS devices 68 and op amps 122. *Hasegawa*, [16], [22], [26], Figs. 2, 4, 7-8. As explained in VI.A.1.c, it would have been obvious to combine *Harada*’s **photodiode** with *Hasegawa*’s **signal-processing circuitry** to form a **single semiconductor chip**, as taught by *Hasegawa*. *Lebby*, ¶105.

- b. [1a(i)]: “a **photodetector** formed on a **semiconductor substrate** and comprising a **photon absorbing region** configured to absorb photons from an optical source signal ... and provide an output electrical signal corresponding thereto”

Harada-Hasegawa renders obvious this limitation. *Lebby*, ¶106. *Harada*’s **PiN photodiode** (“**photodetector**”) is formed on silicon substrate 1:



Harada, [8], [10]-[11], [15], [17], [19], Fig. 1; Lebbby, ¶106. *Harada-Hasegawa* includes *Harada*'s *PiN photodiode* formed on a *semiconductor substrate* with signal-processing circuitry:

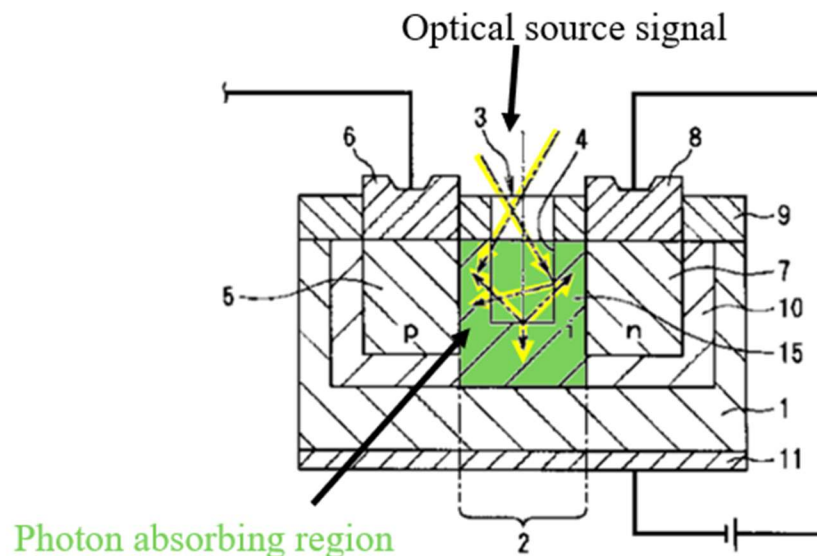


Exemplary combinations of *Harada*'s *PiN photodiode* with *Hasegawa*'s processing circuitry, based on *Harada*'s Figure 1 and *Hasegawa*'s Figure 7

The *photodiode* includes an *intrinsic i-layer*, which is a "*photon absorbing region*." Lebbby, ¶106. Alternatively, *Harada*'s "*photon absorbing region*" includes the entire *PiN* structure (including *i-layer* 15, *p-layer* 5, and *n-layer* 7) because a

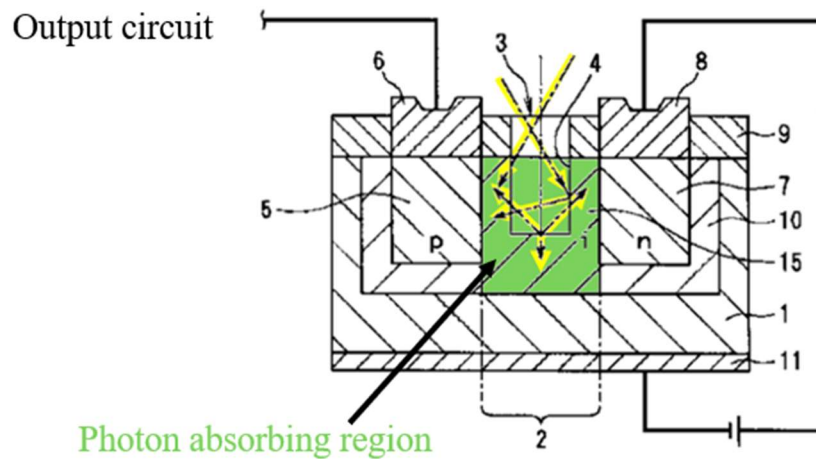
POSITA would have understood that the entire PiN structure is a region involved in photon absorption. *Harada*, [10]-[11], [15], [19]; Lebbby, ¶106.

Harada further discloses improving photodetectors that receive high-speed light signals of about 700-870 nm wavelength (i.e., exemplary “optical source signal”). *Harada*, [3], [7], [15]. *Harada*’s photon absorbing region is “configured to absorb photons from an optical source signal,” at least because *Harada* discloses light from the high-speed signal being absorbed in i-layer 15 around the holes. *Harada*, [15].



Harada, Fig. 1. A POSITA would have understood that absorbing light means absorbing *photons* (elementary light particles). Lebbby, ¶107.

Harada’s photodiode connects to an output circuit to output a current generated by the detected light:



Harada, [15], Fig. 1. *Harada*'s photodiode thus “provide[s] an output electrical signal corresponding” to the received optical source signal. Lebbby, ¶108.

c. [1a(ii)]: “... an optical source signal modulated for data communication ... ;

Harada-Hasegawa renders this limitation obvious. *Harada*'s photodiode is a photodetector that receives an “optical source signal,” including “high-speed light signals”⁵ and a signal at wavelengths of 700-870 nm. *Harada*, [3], [7]; Lebbby, ¶109.

In *Harada-Hasegawa*, *Harada*'s high-speed light signal would have been “an optical source signal modulated for data communication.” Lebbby, ¶110. It

⁵ To the extent Patent Owner contends that this limitation is met by an unmodulated high-frequency carrier wave, then *Harada*'s “high-speed light signal[.]” meets this limitation. Lebbby, ¶109.

would have been obvious to configure *Harada*'s photodiode to receive "an optical source signal modulated for data communication," as taught in *Hasegawa*, for the reasons explained for the "data communication" in [1pre(i)]. VI.A.2.a.i; Lebby, ¶110. A source signal that is "modulated for data communication" would have also furthered the purpose of *Hasegawa*'s device of receiving an optical signal with recorded data. *Hasegawa*, [2]-[3]; Lebby, ¶110.

As explained, *Hasegawa* teaches using a photodetector for data communication. VI.A.2.a.i ([1pre(i)]); Lebby, ¶111. *Hasegawa* discloses a high-speed photodetector used as an optical pickup mechanism to detect laser light reflected off a track of an optical disc and receive recorded data from the light signal at a high data rate. *Hasegawa*, [2]-[3], [5]-[6], [9]. A POSITA would have understood that the optical disc track includes pits and/or highly-reflective spots that modulate a laser light intensity to impress a binary sequence of data onto the reflected laser light, so that the laser light carries data that is communicated to an optical pickup photodetector. *Hasegawa*, [2]-[3]; Ex-1017; Lebby, ¶111.

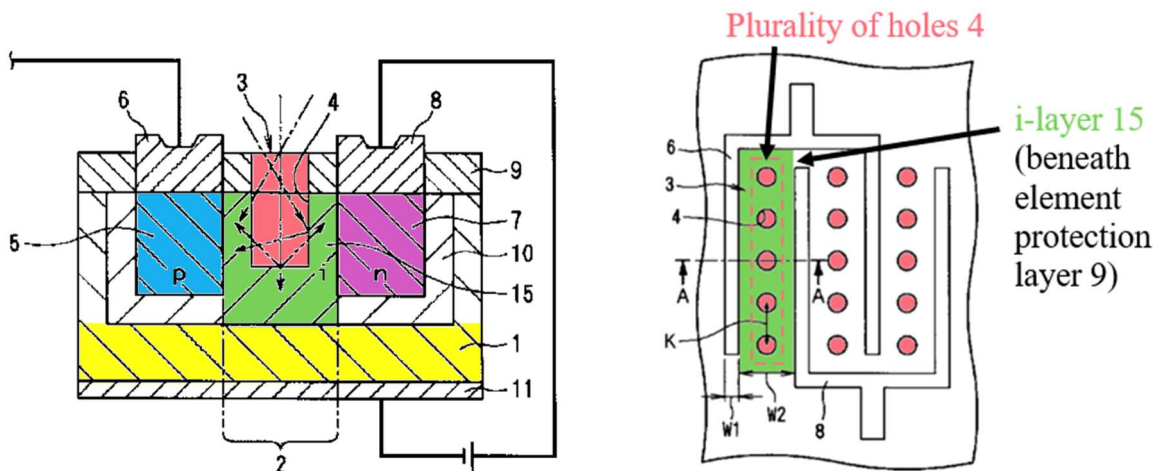
Hasegawa demonstrates that it was known to receive "an optical source signal modulated for data communication" using a photodetector, such as *Harada*'s photodiode with enhanced sensitivity for high-speed light signals. Lebby, ¶111.

Hasegawa's disclosure of receiving data from an optical disc is consistent with the '084 patent, which discloses data communication using optical signals

modulated with “information impressed on the light,” involving various techniques of manipulating the optical signal to carry gigabits of data per second. ’084 patent, 16:22-45; Lebbby, ¶112.

- d. [1b(i)]: “said **photon absorbing region** comprising an **I-region** that is between an **N-region** and a **P-region** and comprises a substantially continuous layer interrupted by a **plurality of holes** extending in said **I-region** toward said **substrate**”

Harada discloses this limitation. Lebbby, ¶113. *Harada* discloses a **PiN** photodiode having **i-layer 15** (“**I-region**”) between **p-layer 5** (“**P-region**”) and **n-layer 7** (“**N-region**”), as shown below:



Harada, Figs. 1 (left), 2 (right), [4]-[5], [8], [10]-[12]. I-layer 15 includes **plurality of holes 4** extending “in the **i-layer 15** in the thickness direction of the **silicon substrate 1**.” *Harada*, [10]-[13], Fig. 1. **Holes 4** extend to a depth that is shallower than the depth of **p-layer 5** and **n-layer 7**. *Harada*, [13], Fig. 1; Lebbby, ¶¶113-114.

I-layer 15 is “substantially continuous” because the i-layer connects around and under holes 4. *Harada*, Figs. 1-2; Lebby, ¶115. I-layer 15 is therefore an I-region that “comprises a substantially continuous layer interrupted by a plurality of holes extending in said I-region toward said substrate.” Lebby, ¶115.

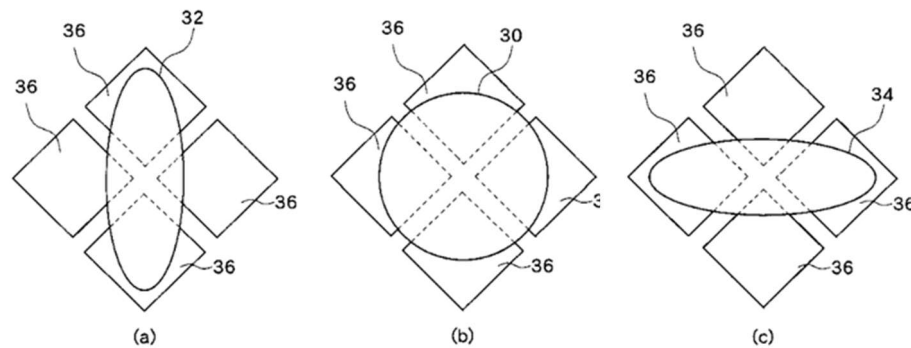
e. [1b(ii)]: “and configured to concurrently receive the same source signal at a plural number of the holes;”

Harada-Hasegawa renders this limitation obvious. *Harada* discloses a photodiode having light-receiving surface 3 with plurality of holes 4. *Harada*, [10]-[13], Figs. 1-2; VI.A.2.d; Lebby, ¶116. *Harada-Hasegawa* is an integrated detector/processor circuit that receives a source signal modulated for data communication, such as a high-speed laser light signal carrying recorded data from an optical disc. VI.A.1.c, VI.A.2.a.i; Lebby, ¶116.

Harada’s modified photodiode is “configured to concurrently receive the same source signal at a plural number of the holes.” Lebby, ¶117. *Harada* discloses “convert[ing] the light incident on the i-layer 15 from the light-receiving surface 3 into electric current to detect the light.” *Harada*, [15]. A POSITA would have understood that *Harada*’s photodiode may concurrently receive a source signal at some or all of light-receiving surface 3. Lebby, ¶117. *Harada* also teaches that “in the situation in which the light-receiving surface 3 between the pairs of electrodes is large, preferably a plurality of the holes 4 is provided within the light-

receiving surface 3.” *Harada*, [14]-[16]. A POSITA would have understood that *Harada*’s photodiode is “configured to concurrently receive the same source signal at a plural number of the holes,” based at least on *Harada*’s disclosure of a large light-receiving surface and multiple holes in the light-receiving surface. Leiby, ¶117.

Hasegawa discloses an array of light-receiving elements 36, or photodiodes 64, that receives an optical light signal distributed across surfaces of the light-receiving elements, as illustrated by circle 30 and ellipses 32 and 34:



Hasegawa, Figs. 9(a)-(c) (above), 7, [4]-[5], [14], [36], [42]. *Hasegawa* demonstrates that it was known for an optical signal to illuminate a photodetector’s large light-receiving surface and to concurrently illuminate multiple photodiodes. Leiby, ¶118. *Harada-Hasegawa* includes *Harada*’s photodiode with holes formed in the light-receiving surface, as shown in *Harada*’s Figure 2. *Id.* A POSITA would have understood that an optical source signal illuminates at least a portion of the light-receiving surface in *Harada-Hasegawa*, as suggested by *Harada* and

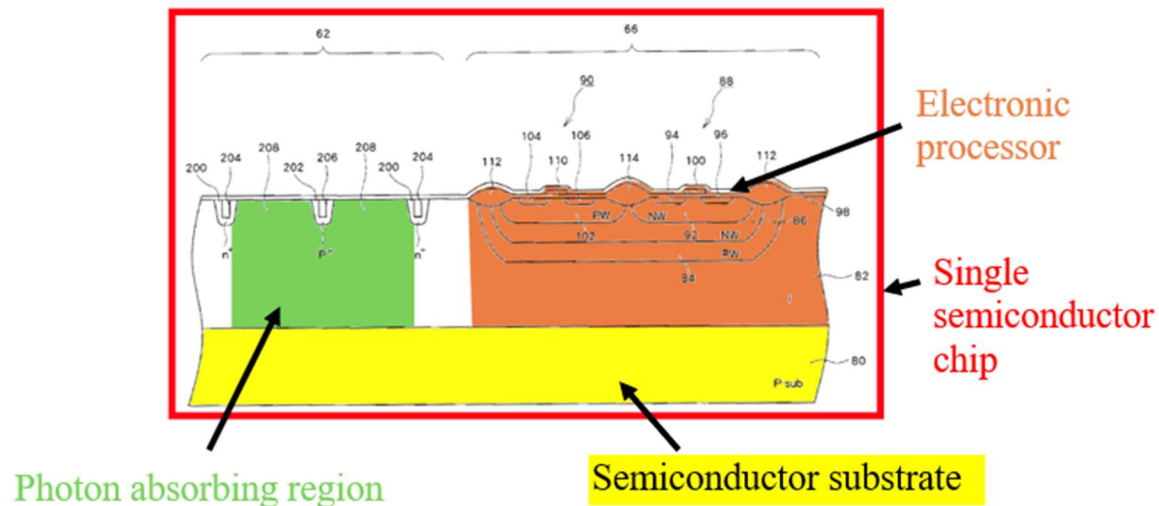
expressly taught by *Hasegawa*. *Id.* As a result, a plurality of holes would concurrently receive the optical source signal. *Id.*

A POSITA would have also understood that an optical source signal irradiating a light-receiving surface would be distributed across at least a portion of the surface, and that a plurality of holes in the light-receiving surface would concurrently receive the same optical source signal. Lebbby, ¶119. For example, *Makita* discloses that “the intensity distribution 57 of the input signal light [has] a Gaussian distribution, and [the] light intensity is high at the center of photoreceptor area 54.” *Makita*, [5]. A POSITA would have therefore understood that a light signal is distributed across a light-receiving surface, and that a plurality of holes in the light-receiving surface would concurrently receive the optical source signal. Lebbby, ¶119.

- f. [1c]: “an **electronic processor** also formed on said **semiconductor substrate** and operatively associated with said **photon absorbing region** to receive therefrom and process said output electrical signal into a processed output, thereby forming a **single semiconductor chip** that receives the optical source signal and outputs the processed output;”

Harada-Hasegawa renders this limitation obvious because it includes a photodetector and electronic processor formed on a single substrate and into a **single semiconductor chip**. VI.A.1.c, VI.A.2.a; Lebbby, ¶120. A POSITA would have been motivated to form a photodetector (having a “**photon absorbing region**”)

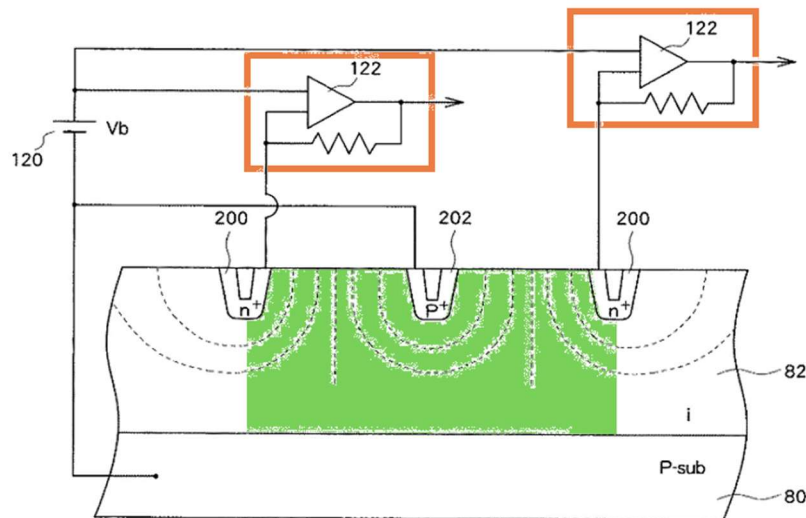
and signal-processing circuit part (at least a portion of which being an “**electronic processor**”) on the same **silicon semiconductor substrate** and into a **single semiconductor chip**, as taught by *Hasegawa* and explained above.



Hasegawa, [9], [14], [42], Fig. 7; VI.A.1.c, VI.A.2.a; Lebby, ¶120. At least a portion of **signal-processing circuit part** is an “**electronic processor**” because it has components that amplify a photo-electric conversion signal, detect a current from a photodiode, and perform “later-stage” signal processing. *Hasegawa*, [9], [14], [26], [46]. *Hasegawa*’s signal-processing circuit part is “formed on a semiconductor substrate” with light-receiving elements. *Hasegawa*, [11]-[12], [14]-[15], [26], [46], Figs. 1, 3, 7; Lebby, ¶120.

Harada-Hasegawa’s **signal-processing circuit part** (“**electronic processor**”) is “operatively associated” with *Harada*’s photodiode’s **photon absorbing region**. Lebby, ¶121. *Harada*’s photodiode’s output circuit would have connected to

Hasegawa's op amp 122 (illustrated below, part of **signal-processing circuit**) and to an output terminal of op amp 122, to connect *Harada*'s output circuit carrying an electrical current to *Hasegawa*'s current detector device:



Hasegawa, Fig. 8 (above), [46]; *see also Hasegawa*, Fig. 4, [26]; Lebbby, ¶121.

A POSITA would have understood that *Harada*'s photodiode's output circuit connects to *Hasegawa*'s wiring 76 and op amp 122. *See Harada*, [15], Fig. 1; *Hasegawa*, [9], [26], [46], [54], Figs. 4, 8. *Hasegawa* discloses that its signal-processing circuitry detects electrons collected by the photodetector by detecting a current from the photodetector. *Hasegawa*, [6], [49]. The connection between *Harada*'s photodiode output circuit and *Hasegawa*'s wiring would have detected the current generated from the high-speed light signal incident on *Harada*'s light-receiving surface and provided a processed output of the detected current. Lebbby, ¶122.

Harada-Hasegawa is a **single semiconductor chip** that “receives the optical source signal and outputs the processed output.” Lebbby, ¶123. **Signal-processing circuit part** receives and processes an output signal from *Harada*’s photodiode’s **photon absorbing region**. *Id.* *Hasegawa*’s **signal-processing circuit** provides a processed output based on the current from *Harada*’s output circuit in at least two ways. *Id.*

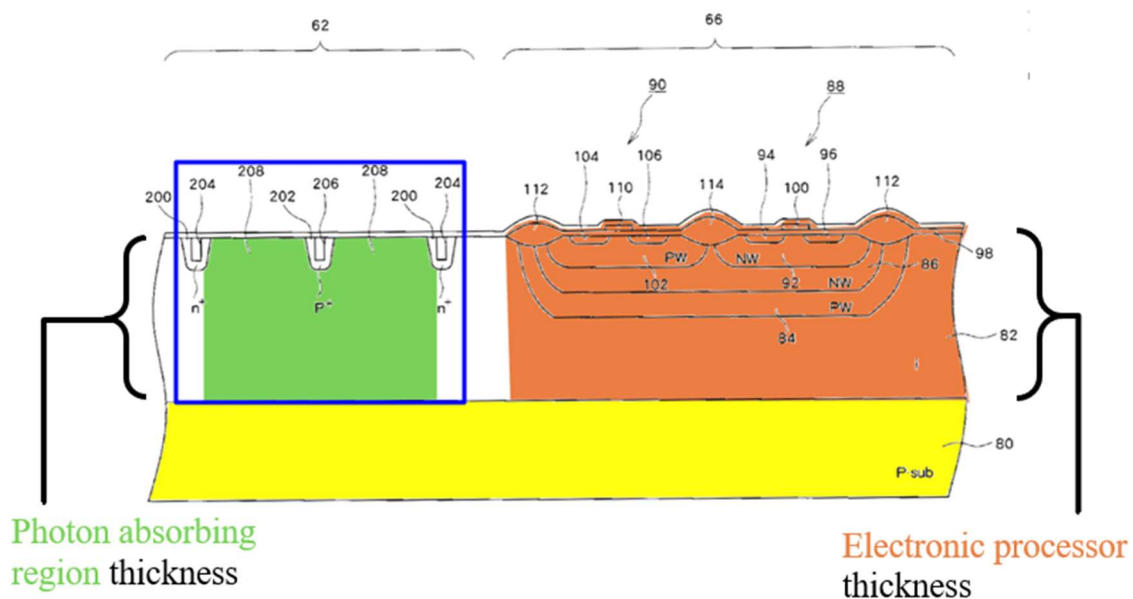
First, *Hasegawa*’s op amp 122 receives an output signal from the **photon absorbing region** because it detects signal charges collected in the photon absorbing region. *Hasegawa*, [6], [26], [49]. *Hasegawa* discloses “process[ing] said output electrical signal into a processed output” and “output[ting] the processed output,” because “[t]he weak photo-electrical conversion signals generated by the light-receiving parts are amplified by an amplifier and output to a later-stage signal-processing circuit.” *Hasegawa*, [9], [14], Figs. 4, 8; Lebbby, ¶124.

Second, *Hasegawa*’s later-stage signal-processing circuit processes the amplified signal from op amp 122. *Hasegawa*, [9], [26]; *see also Hasegawa*, [14] (discussing “another signal-processing circuit”). For example, a POSITA would have understood that op amp 122’s output is connected to one or more CMOS devices 68 in **signal-processing circuit part** for further processing of the photodiode electrical signal. Lebbby, ¶125. *Hasegawa* therefore discloses another example of an

electronic processor that receives an output electrical signal from a photon absorbing region and processes it into a processed output. *Id.*

- g. [1d]: “wherein said **photon absorbing region** and said **electronic processor** have respective thicknesses that are of the same order of magnitude; and”

Harada-Hasegawa renders this limitation obvious. Lebbby, ¶126. *Harada-Hasegawa* is a photodetector/integrated circuit device having *Harada*’s **photodiode** (**photodetector**) formed on a single substrate with signal-processing circuitry, as taught by *Hasegawa*. *Id.* *Hasegawa* discloses a light-receiving portion 62 (photodetector) having a **photon absorbing region** and a **signal-processing circuit part** formed on the same **semiconductor substrate**. *Id.* The **photon absorbing region** has a thickness that is a same order of magnitude as the **signal-processing circuit part**, as shown:



Hasegawa, Fig. 7, [12], [14]-[15], [17]-[18], [42]; Lebby, ¶126.

The '084 patent does not describe “respective thicknesses that are of the same order of magnitude.” Lebby, ¶127. If Patent Owner contends that a photon absorbing region and an electronic processor integrated on or in the same substrate meets “respective thicknesses that are of the same order of magnitude,” then *Harada-Hasegawa* meets this element. *Id.* A thickness that is within ten times of the other thickness meets the “order of magnitude” limitation. *Id.*

Regardless of whether *Hasegawa*’s figures are drawn to scale, they establish that the photon absorbing region and signal-processing circuit part (“electronic processor”) have similar thicknesses above a semiconductor substrate 60 and are therefore “the same order of magnitude.” *Hasegawa*, Figs. 3, 7; Lebby, ¶128.

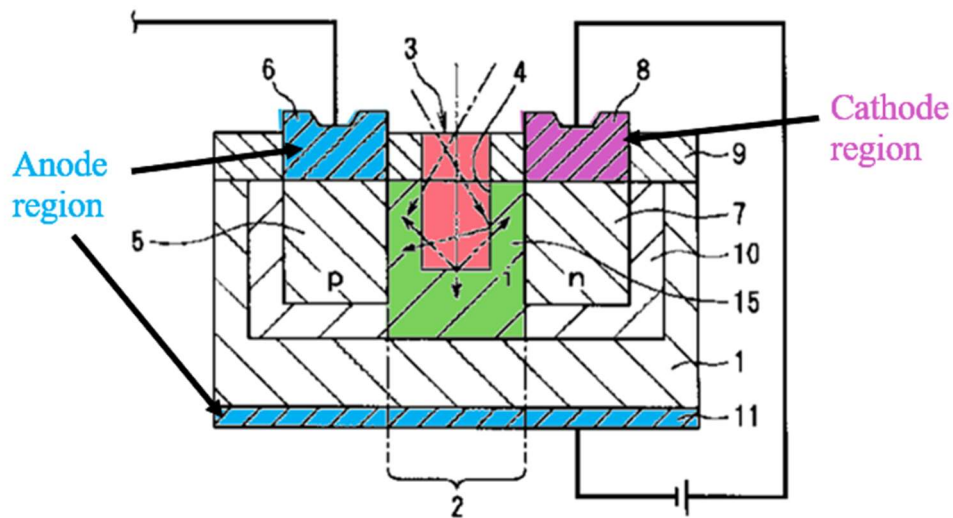
A POSITA would have expected *Harada*’s photodiode in *Harada-Hasegawa* to have a thickness that is a “same order of magnitude” as a thickness of *Hasegawa*’s signal-processing circuit part, at least because both *Harada*’s and *Hasegawa*’s devices are formed in the same epitaxial layer 82 on the same substrate using the same materials and processes. Lebby, ¶129; *Hasegawa*, [19]-[23], [35]-[37], [39]-[47]. *Harada* discloses a photodetector made with silicon and silicon oxide, which a POSITA would have understood are materials used in CMOS fabrication. *Harada*, [11]. *Hasegawa* also discloses CMOS devices and

CMOS-compatible photodetector fabrication. *Hasegawa*, Abstract, [9], [12], [14]-[15], [18]-[19], [22]-[24]; Lebbby, ¶129.

Harada's CMOS-compatible photodetector would have had a thickness of the same order of magnitude of CMOS signal-processing circuitry formed on the same substrate using similar processes. Lebbby, ¶130. Indeed, it would have been obvious to a POSITA to implement known CMOS fabrication techniques for forming integrated circuits and a photodetector on the same substrate, as taught in *Hasegawa*, using *Harada*'s similar silicon-based photodetector. *Id.* The resulting combination would predictably include a photon absorbing i-layer that is of the same order of magnitude in thickness as the CMOS integrated circuit, at least because the i-layer and the integrated circuit would have been located within the same layers formed on the substrate, as taught by *Hasegawa*. *Id.*

- h. [1e(i)]: “a cathode region and an anode region operatively associated with said photon absorbing region and”

Harada discloses this limitation because *Harada* discloses p and n electrodes that are an anode region and cathode region, respectively. Lebbby, ¶131. *Harada* discloses “[a] p-electrode 6 and an n-electrode 8 [that] are formed on the upper surface of the p-layer 5 and the n-layer 7.” *Harada*, [11]-[15], Fig. 1 (below). *Harada* also discloses a “p-electrode 11 [that] is formed on the lower surface of the silicon substrate 1.” *Harada*, [11], [15].



Harada, Fig. 1. A POSITA would have understood that **n-electrode 8** is a **cathode region**, and **p-electrode 6** and **p-electrode 11** are **anode regions**. Lebbby, ¶131.

Harada's disclosure is consistent with the '084 patent's disclosure of "N and P ohmic contacts" placed on the N and P layers that apply a reverse-bias voltage through the N and P layers. '084 patent, 18:51-54, 19:33-36, 20:17-20, 44:7-8; Lebbby, ¶131.

Harada's **anode** and **cathode** regions are "operatively associated with [the] photon absorbing region." Lebbby, ¶132. For example, *Harada* discloses applying a reverse-bias voltage to the PiN photodetector via **n-electrode 8** and **p-electrode 11**. *Harada*, [15]. *Harada* also discloses connecting **p-electrode 6** to an output circuit. *Id.* By applying the reverse-bias voltage via **n-electrode 8** and **p-electrode 11** and connecting **p-electrode 6** to an output circuit, *Harada*'s photodiode "convert[s] the light incident on the **i-layer 15** from the light-receiving surface 3 into electric

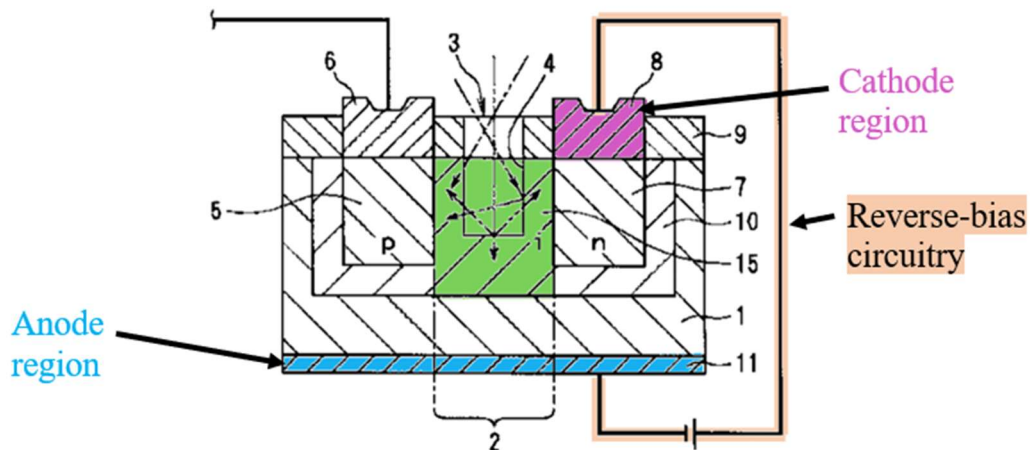
current to detect the light.” *Id.* Therefore, n-electrode 8, p-electrode 6, and p-electrode 11 are each “operatively associated” with i-layer 15 (“photon absorbing region”). Lebbby, ¶132.

- i. [1e(ii)]: “reverse biasing circuitry configured to apply a voltage between said cathode and anode regions such that said cathode region is driven to a more positive voltage than said anode region.”

Harada discloses this limitation and *Harada-Hasegawa* also renders this limitation obvious. Lebbby, ¶133. First, *Harada* discloses connecting anode and cathode regions to a circuit and applying a reverse-bias voltage via a p-electrode and n-electrode (exemplary cathode and anode regions, respectively). *Id.* For example, *Harada* discloses:

By connecting a power supply between the n-electrode 8 that contacts the upper surface of the n-layer 7 and the p-electrode 11 on the lower surface of the substrate 1, with the n-layer 7 side as the positive, applying a reverse-bias voltage, and connecting the p-electrode 6, which contacts the upper surface of the p-layer 5, to an output circuit, this photodiode can convert the light incident on the i-layer 15 from the light-receiving surface 3 into electric current to detect the light.

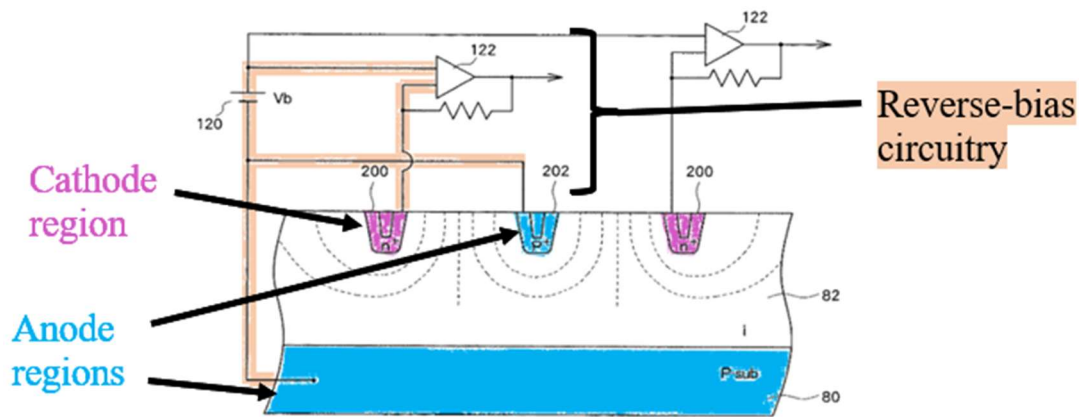
Harada, [15] (emphases added). These connections are illustrated below:



Harada, Fig. 1. *Harada* discloses connecting the “n-layer 7 side [via n-electrode 8] as the positive,” and a POSITA would have understood that p-electrode 11 (anode) is connected to a power supply’s negative terminal, at least based on *Harada*’s Figure 1. *Harada*, [15]; Lebby, ¶133. *Harada* therefore discloses that “said cathode region is driven to a more positive voltage than said anode region.” Lebby, ¶133.

Second, a POSITA would have also been motivated to connect *Harada*’s photodiode’s output circuit (via p-electrode 6, an anode region) to *Hasegawa*’s signal-processing circuitry to detect a current and provide a processed output from a received high-speed light signal. VI.A.1.c; Lebby, ¶134.

Hasegawa teaches connecting a PiN photodiode’s anode region and cathode region to voltage terminals and applying a reverse-bias voltage between the voltage terminals to the i-region of the epitaxial layer 82 located between the anode and cathode regions. *Hasegawa*, [7]. *Hasegawa* discloses placing cathode regions 200 in a reverse-bias state in relation to anode region 202:



Hasegawa, Fig. 8, [46]-[47]; see also *Hasegawa*, Fig. 7; Lebbby, ¶135. Cathode 200 and positive voltage V_b are connected to op amp 122. Lebbby, ¶135. Anode region 202 and p-sub 80 (another example of an anode region similar to *Harada*'s p-electrode 11) are connected to a negative voltage. *Id.* Cathode region 200 is thus driven to a more positive voltage than anode region 202 and/or p-sub 80. *Id.*

Hasegawa's technique creates and expands a depletion region between the anode and cathode connected to the reverse-bias circuit, to sweep signal charges generated in the i-layer and generate an output current that is processed.

Hasegawa, [6]-[7], [11]-[12], [20]. *Hasegawa* further teaches reverse biasing between an anode and cathode located near the top surface of the photodetector, such as *Harada*'s p-electrode 6 and n-electrode 8, to form the depletion layer extending from the top of the photodetector and improve "photoelectric conversion efficiency." *Hasegawa*, [6]-[7], [20], [46]-[47], Fig. 8; Lebbby, ¶136.

It would have been obvious to a POSITA to connect *Harada*'s p-electrode 6 and/or 11 and n-electrode 8 to reverse-biasing circuitry, as taught by *Hasegawa*. *Hasegawa*, Fig. 8; Lebby, ¶137. The modification would have involved substituting or supplementing *Harada*'s voltage connection to p-electrode 11 (bottom of *Harada*'s photodiode) with a voltage connection to p-electrode 6, as taught in *Hasegawa*. *Hasegawa*, [26], [46], Figs. 4, 8; Lebby, ¶137. Such a modification to *Harada*'s reverse-biasing connections would enable detection of a current generated by photons in *Harada*'s i-layer 15 in *Harada-Hasegawa*'s device. VI.A.2.h; Lebby, ¶137.

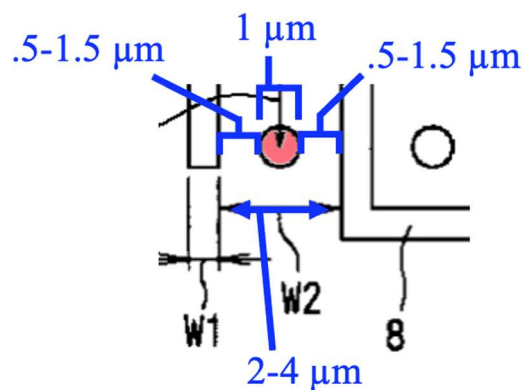
A POSITA would have reasonably expected success in modifying *Harada* based on *Hasegawa*'s teachings because *Harada*'s photodiode would require only minimal modifications that were well within a POSITA's capabilities including substituting one voltage connection for another. Lebby, ¶138. *Hasegawa* provides schematics (Figures 2, 4, 8) and associated descriptions that would have guided a POSITA to make any necessary modifications. *Id.*

3. Claim 2: “The integrated detector/processing circuit of claim 1, wherein the thickness of the photon absorbing region is in the range of 0.5 to 5 micrometers.”

Harada-Hasegawa renders this limitation obvious. Lebby, ¶139. *Harada*'s lateral-type PiN photodiode includes an i-layer between a p-layer and an n-layer. *Harada*, [3]. *Harada* discloses conventional photodiodes having an i-layer (photon

absorbing region) that “is formed to a thickness that is the absorption length or more to make the light-receiving sensitivity high.” *Id.* This “thickness” refers to “the depth from a light-incident surface.” *Harada*, [5]-[6]. *Harada* forms holes 4 in the i-layer, and it further discloses that light enters the holes’ interior, side, and bottom surfaces. *Harada*, [15]. Claim 2 does not require the “thickness” to be measured in any particular direction or relative to any other particular component. Lebbby, ¶139. Accordingly, a “thickness of the photon absorbing region” may also be an i-layer depth measured between the side surface of a hole (light-incident surface) and the surrounding p-layer or n-layer. *Id.*

Harada’s i-layer’s (photon absorbing region) thickness ranges from 0.5-4 micrometers (μm). *Harada*, [14], Fig. 2; Lebbby, ¶140. *Harada* discloses a spacing W2 between p-electrode 6 and n-electrode 8 of 2-4 μm and a hole diameter of 1 μm , leaving 0.5-1.5 μm on either side of the hole:



Harada, Fig. 2 (excerpted), [14]. The i-layer thickness on either side of the hole ranges between 0.5-1.5 μm , depending on dimension W2. Lebbby, ¶140. At a minimum, the i-layer thickness is 0.5 μm between the hole wall and the p-layer or the n-layer beneath the respective electrode. *Id.* The maximum i-layer thickness is 4 μm , which is the maximum W2 dimension where there is no hole. *Id.* Therefore, *Harada* discloses a “thickness of the photon absorbing region” that is fully encompassed by the claimed “range of 0.5 to 5 micrometers.” *Id.*

4. **Claim 3: “The integrated detector/processing circuit of claim 1, wherein the electronic processor comprises an application specific integrated circuit (ASIC) comprising at least one of complementary metal oxide semiconductor (CMOS) devices, bipolar (Bi) devices, and BiCMOS devices.”**

Harada-Hasegawa renders this limitation obvious. Lebbby, ¶141. A POSITA would have understood that *Harada-Hasegawa* includes the claimed “application specific integrated circuit (ASIC).” *Id.* *Hasegawa*’s signal-processing circuit part includes components and circuits designed specifically for processing the output signal from a photodetector’s light-receiving part, and a POSITA would have understood this constitutes an application-specific processing circuit. *Id.* As discussed, it would have been obvious to use *Hasegawa*’s signal-processing circuit part to detect current from *Harada*’s photodiode and provide a processed output of a high-speed data signal. *Id.*; VI.A.2.f.

The '084 patent broadly describes an ASIC as including “signal processing, signal amplification, memory, [CPU], electrical transmitter, optical waveguides, integrated optics, and other ICs for specific applications.” '084 patent, 15:27-31. Therefore, the '084 patent does not require anything more than what is taught by *Harada-Hasegawa*. Lebbby, ¶142.

Claim 3 requires the ASIC to include at least one of CMOS, bipolar, and BiCMOS devices, all of which were known as typical for integrated photodetector/processor devices. Lebbby, ¶143. Both *Harada* and *Hasegawa* disclose silicon-based photodetector devices, and a POSITA would have understood that CMOS devices are formed using standard processes and materials in silicon-based devices. *Harada*, [10]-[13]; *Hasegawa*, [14]; Lebbby, ¶143.

Harada-Hasegawa includes *Hasegawa*'s signal-processing circuit part (an ASIC), at least a portion of which is an electronic processor. VI.A.1.c, VI.A.2.f ([1c]). Signal-processing circuit part includes components such as CMOS devices 68 and op amps 122. *Hasegawa*, [9], [14], [23], [26], [42], [46], Figs. 1, 4, 8. Therefore, *Harada-Hasegawa* has an “electronic processor” comprising CMOS devices. Lebbby, ¶144.

5. **Claims 4 and 6:⁶ “The integrated detector/processing circuit of claim 1, wherein the photon absorbing region is configured to absorb in excess of 60% of the incident source signal at wavelengths from 800 nm to 900 nm and provide an output electrical signal corresponding thereto.”**

Harada discloses these additional limitations. Lebbby, ¶145. As explained, *Harada* discloses a “photon absorbing region configured to absorb photons from an optical source signal” and “provide[s] an output electrical signal corresponding thereto.” VI.A.2.b ([1a(i)]). Claims 4 and 6 further require that the photon absorbing region be “configured to absorb in excess of 60% of the incident source signal at wavelengths from 800 nm to 900 nm.” *Harada* discloses these additional limitations. Lebbby, ¶146.

Harada’s conventional photodiodes include an i-layer (photon absorbing region) configured to achieve quantum efficiency of 70% or more at wavelengths of approximately 700-870 nm, which substantially overlaps with the claimed 800-900 nm range and includes at least two wavelengths in the claimed range. *Harada*, [3]. *Harada* further improves on these conventional photodiodes by forming holes in the i-layer to improve absorption performance relative to conventional photodiodes (having no holes). *Harada*, [15]-[16]. A POSITA would have understood that *Harada*’s improved photodiodes thus include at least 70%

⁶ Claims 4 and 6 each depend directly from claim 1 and recite identical limitations.

quantum efficiency in the same wavelength range, and that *Harada*'s 70% quantum efficiency disclosure meets the claim limitation "configured to absorb in excess of 60% of the incident source signal." Lebbby, ¶147. The '084 patent states: "Absorption and quantum efficiency are directly proportional, and approximately 90% absorption with minimal reflection can be equivalent to approximately 90% quantum efficiency." '084 patent, 55:51-54. Accordingly, *Harada* discloses at least 70% absorption over 700-870 nm, which is "in excess of 60%." Lebbby, ¶147 (citing *Yahaya*, Fig. 4(a)).

6. **Claim 5: The integrated detector/processing circuit of claim 1, wherein the photon absorbing region is configured to absorb the incident source signal at an absorption percentage that varies by less than 20% over selected wavelength spans of at least 20 nm of source signal wavelengths from 800 nm to 900 nm.**

Harada-Hasegawa renders this limitation obvious. Lebbby, ¶148. *Harada-Hasegawa* discloses "[t]he integrated detector/processing circuit of claim 1."

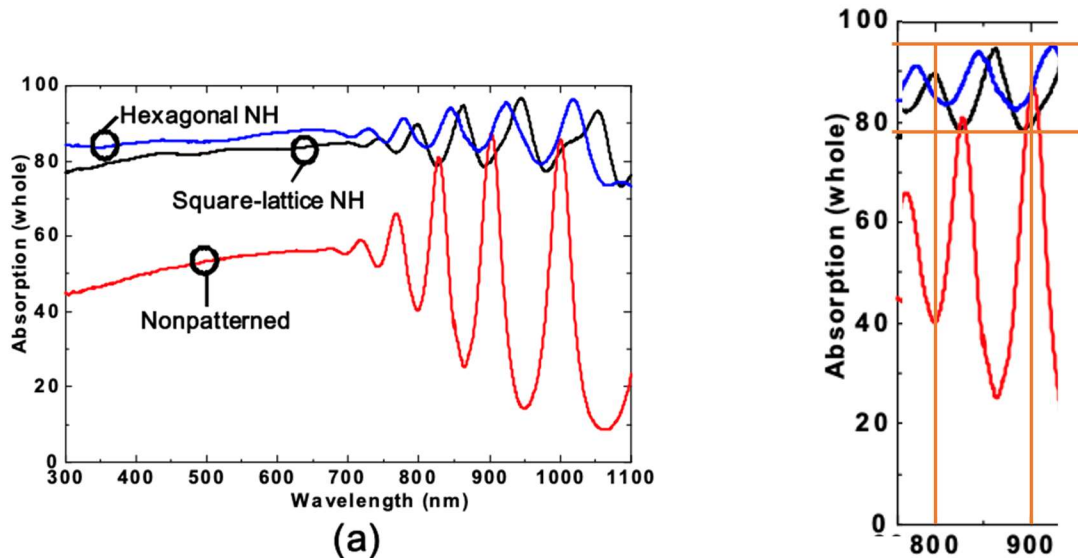
VI.A.2. *Harada*'s photodiode receives high-speed light signals of 700-870 nm wavelength, and is enhanced with holes in the photon absorbing i-layer 15 that improve absorption. *Harada*, [3], [7], [9]-[13], Figs. 1-2; VI.A.2.d; Lebbby, ¶148.

A POSITA would have been motivated to configure photodiodes to achieve consistent performance across a target wavelength range for the relevant implementation. Lebbby, ¶149. A POSITA would have understood that consistent

performance is achievable by minimizing the variation of absorption rates across the desired wavelength range. *Id.* And it was understood that “[t]exturing the cell active layer with nanostructures” enhances absorption performance, and that “periodic nanohole (NH) arrays exhibit[] better absorption” than other nanostructure types such as nanorods. *Yahaya*, 2; Lebby, ¶149. *Harada-Hasegawa* is designed to receive high-speed optical data signals, and a POSITA would have been motivated to configure the *Harada-Hasegawa* photodiodes to absorb light consistently across the 700-870 nm wavelength range to receive the high-speed optical signals with reliable and consistent performance. Lebby, ¶149. A POSITA would have therefore been motivated to configure *Harada*’s photodiode to achieve <20% variation in absorption over 20 nm spans of wavelength between 800-900 nm. *Id.*

A POSITA would have expected success in achieving <20% variation tolerance over wavelength spans over 700-870 nm because multiple known configurations achieved this absorption. *See generally Yahaya; Carey; Meng.* For example, *Yahaya* improves absorption levels of a silicon photodetector across 300-1100 nm source signals. *Yahaya*, 2-3, 5, Fig. 4(a) (“Introduction”); VI.C.1. Like *Harada*, *Yahaya*’s silicon photodetector is enhanced with holes. *Yahaya*, Figs. 1, 3. *Yahaya* discloses absorption measurements of a silicon photodetector configuration, demonstrating that a POSITA would have expected success in

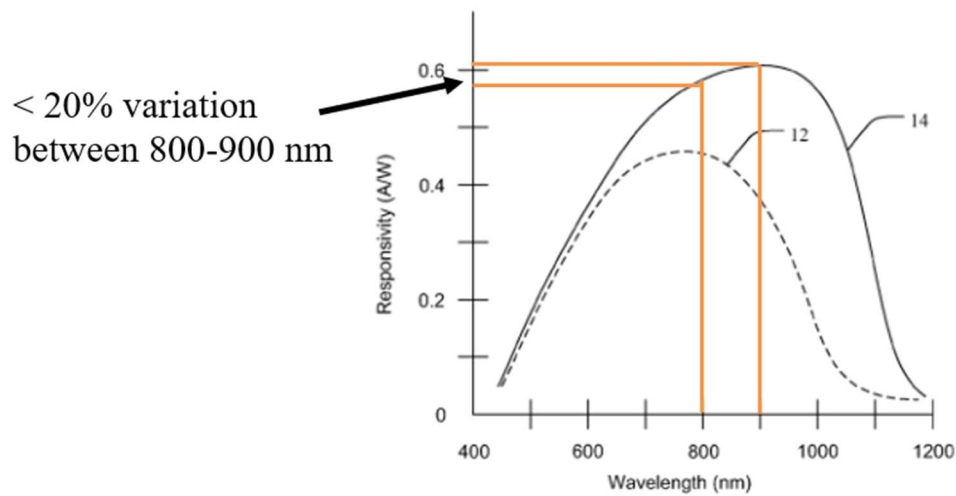
achieving consistent absorption performance with <20% variation across a wide range of wavelengths including 800-900 nm.



Yahaya, 5, Fig. 4(a) (left), diagram based on Fig. 4(a) (right); *Lebby*, ¶¶150-151.

Carey discloses various configurations of a silicon PiN photodiode for optical communication having a “textured region” with nanostructures such as pores (holes) that enhance absorption. *Carey*, [2], [32], [43]-[44], [52]-[53], [67].

Carey discloses a wide range of nanostructure dimensions and illustrates absorption characteristics from 400-1200 nm wavelength and shows <20% variation between 800-900 nm:



Carey, [2], [8], [28]-[32], [46], [67], [94], Fig. 1. A POSITA would have understood that Figure 1 illustrates an absorption characteristic proportional to absorption. Carey, [46]; Lebby, ¶¶152-153.

Meng's silicon photodetector has an array of holes, like Harada, Yahaya, and Carey, and it discloses absorption measurements that vary by less than 20% between 800-900 nm incident light. Meng, 7-9, Fig. 6(b); Lebby, ¶154. These references show that a POSITA would have reasonably expected success in achieving absorption performance with <20% variation in absorption in wavelength spans between 800-900 nm, using a variety of different silicon photodiodes such as Harada's photodiodes in Harada-Hasegawa. Lebby, ¶¶155-157.

It would have thus been obvious to configure the *Harada-Hasegawa* photodiode to achieve the absorption characteristics of claim 5, and a POSITA would have reasonably expected success. Lebbby, ¶158.

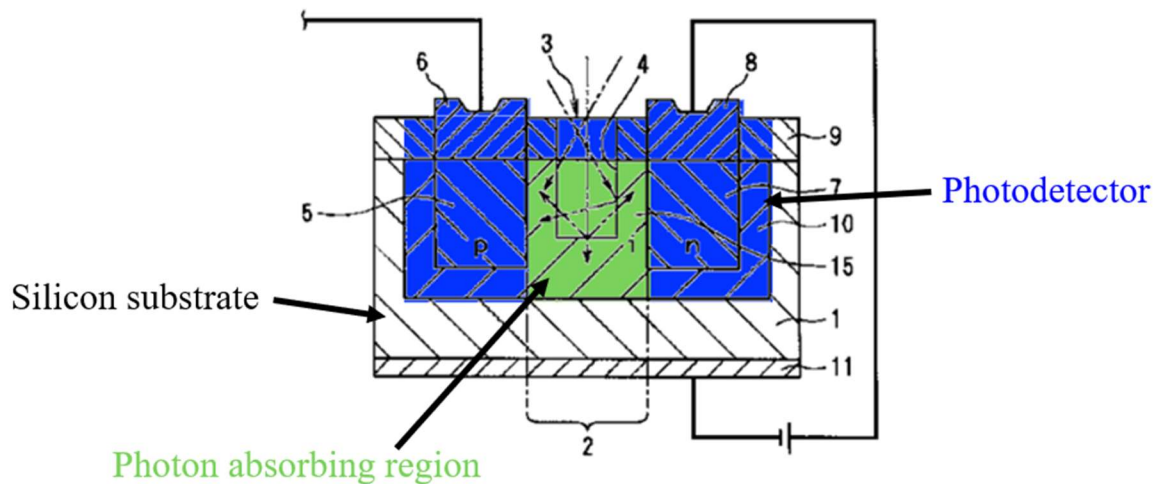
7. Claim 7

- a. [7a]: “The integrated detector/processing circuit of claim 1, further including one or more additional **photodetectors** formed on said **semiconductor substrate** and having respective **photon absorbing regions** receiving respective additional source signals and providing respective output electrical signals corresponding thereto,”

Harada-Hasegawa renders this limitation obvious. Lebbby, ¶159.

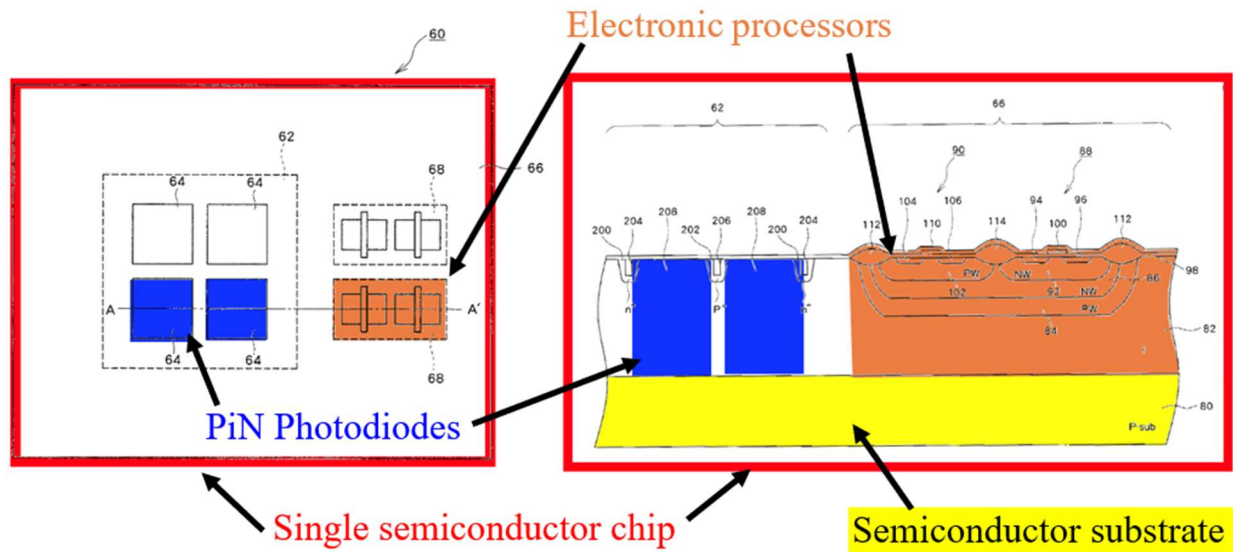
- i. [7a(i)]: “one or more additional **photodetectors** formed on said **semiconductor substrate** and having respective **photon absorbing regions** ... and providing respective output electrical signals corresponding thereto”

Harada’s **photodiode** (“**photodetector**”) is formed on a silicon semiconductor substrate that includes **i-layer 15** (**photon absorbing region**) configured to receive a source signal on light-receiving surface 3:



Harada, [8], [10]-[11], [15], [17], [19], Fig. 1; VI.A.1.c, VI.A.2.a, VI.A.2.b. The photodetector converts light incident on i-layer 15 into electric current and provides that current to an output circuit. *Harada*, [15]; Lebby, ¶160.

Hasegawa discloses multiple photodiodes (photodetectors) each having an i-layer that emits signal charge electrons based on incident light for output to an op amp. *Hasegawa*, [29], [46], [49], Figs. 1, 4, 8, 9; Lebby, ¶161. *Harada-Hasegawa* incorporates *Harada*'s photodiode (above) into a single semiconductor chip that includes light-receiving part 62 having an array of photodiodes and a signal-processing part with processing electronics (CMOS devices), all formed on the same semiconductor substrate:



Hasegawa, Fig. 1 (left), Fig. 7 (right); VI.A.1.c. *Harada-Hasegawa* thus discloses “one or more additional photodetectors formed on said semiconductor substrate” because *Hasegawa* discloses light-receiving part 62 has an array of photodiodes 64 (photodetectors). *Hasegawa*, [5], [14], Figs. 1-2, 6, 9. It would have been obvious to implement *Harada*’s photodiodes (each having a photon absorbing region) as photodiodes 64 in *Hasegawa*’s light-receiving part 62, resulting in an array of *Harada*’s photodiodes formed on *Hasegawa*’s silicon semiconductor substrate 1.

Lebby, ¶161; VI.A.1.c.

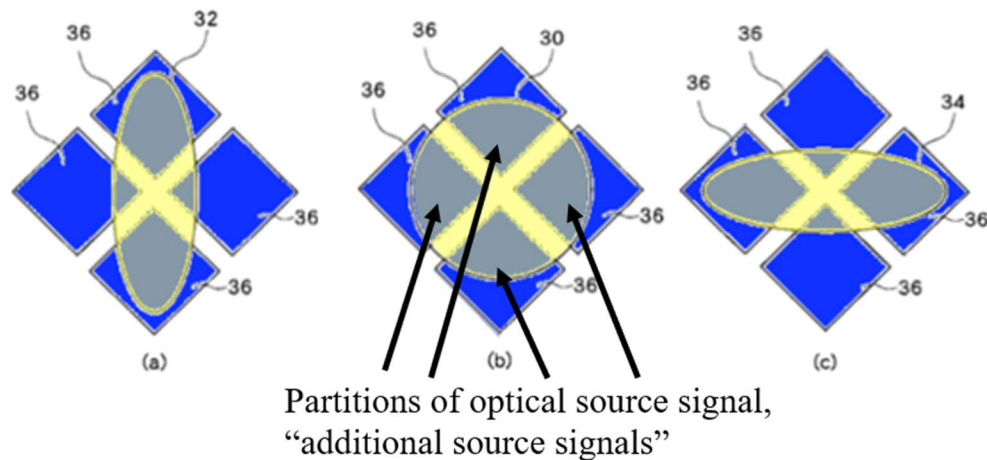
ii. [7a(ii)]: “photon absorbing regions receiving respective additional source signals”

The '084 patent discloses exemplary photodiodes that may be configured to receive multiple spatial portions (partitions) of a source signal⁷ or receive different wavelength bands of signal channels. This includes an array of multiple identical MS-PDs, where each photodiode in the array receives a partition (e.g., a spatial portion) of an optical signal incident on multiple photodiodes in the array. '084 patent, 33:8-24; Leiby, ¶162. The '084 patent also discloses an array of nonidentical MS-PDs that have different hole diameters and periods so that the array includes MS-PDs optimized for different wavelength bands. '084 patent, 33:8-52, Fig. 52. An array of nonidentical MS-PDs detects data channels in a “wavelength division multiplex” (WDM) configuration having multiple wavelength bands combined in a single optical signal. *Id.*, 16:61-67, 17:62-18:13, 33:24-33, 33:38-52. Using WDM, an optical signal may carry multiple wavelength channels that are each detected by one or more of the nonidentical MS-PDs. Leiby, ¶162.

⁷ Petitioner’s mapping of “respective additional source signals” to spatial portions of a source signal is consistent with Patent Owner’s infringement contentions in the parallel litigation.

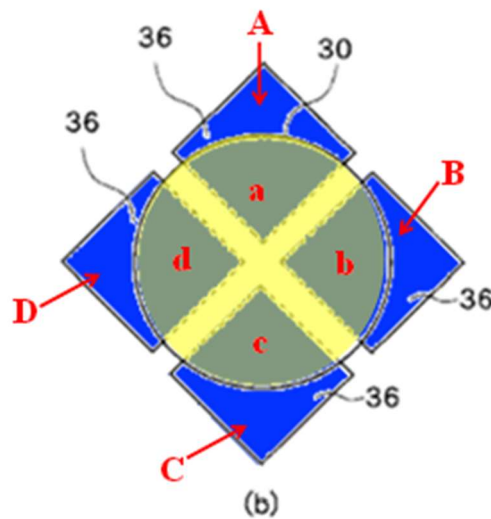
A POSITA would have thus understood that the claimed “respective additional source signals” includes (1) identical MS-PDs receiving spatial portions (partitions) of a light signal, or (2) nonidentical MS-PDs receiving different channel wavelength bands of a multiplexed transmission of an optical signal. Lebbby, ¶163. Ground 1 addresses identical MS-PDs, and Ground 2 addresses nonidentical MS-PDs.

Harada-Hasegawa has photodiodes (“**photodetectors**”) with “**photon absorbing regions** receiving respective additional source signals.” Lebbby, ¶164. *Hasegawa* discloses **photodiodes 64** in an array that “partitions light incident from an optical system onto the substrate front surface into four blocks, 2×2 and receives that light.” *Hasegawa*, [5], [14]. A POSITA would have understood that each photodiode 64 has a **photon absorbing region** that receives a partition of the incident optical signal. Lebbby, ¶164. *Hasegawa* illustrates examples of photodiodes each receiving a partition of an optical signal:



Hasegawa, Figs. 9(a)-(c).

Harada-Hasegawa teaches photodetectors with “respective photon absorbing regions receiving respective additional source signals.” Lebbby, ¶165. *Hasegawa* discloses four photodiodes 64 in a 2×2 array that receive incident light and output signals. *Hasegawa*, [3]-[5], [14]. A POSITA would have understood that *Harada*’s photodiode would be integrated into each photodiode 64 in *Hasegawa*’s 2×2 array to enable each of them to output a received-light signal. Lebbby, ¶165; VI.A.1.c; *Hasegawa*, [29] (discussing received-light signals output by “left-side PD 64” and “right-side PD 64”). Additionally, a POSITA would recognize that in *Harada-Hasegawa*, each photodiode (“one or more additional photodetectors,” labeled A–D below) receives a corresponding portion (“respective additional source signal,” marked a–d) of the incident optical signal. Lebbby, ¶165.

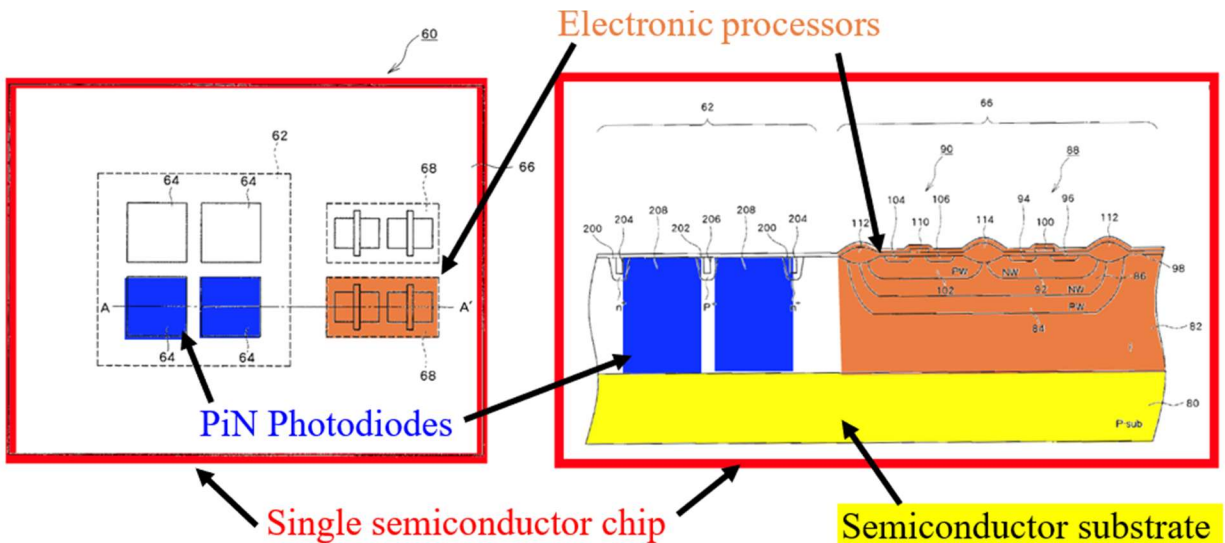


Hasegawa, Fig. 9(b). For instance, photodiode **A** receives portion **a** of the incident light, while photodiode **B** receives portion **b**. *Hasegawa*, [4]-[5]. Photodiode **A** corresponds to claim 1’s “photodetector,” whereas photodiodes **B–D** represent the “additional photodetectors” referenced in this claim. Lebbly, ¶165. Portion **a** of the optical signal received by photodiode **A** constitutes claim 1’s “optical source signal,” while portions b–d, received by photodetectors **B–D**, respectively, are claimed “respective additional source signals.” *Id.*

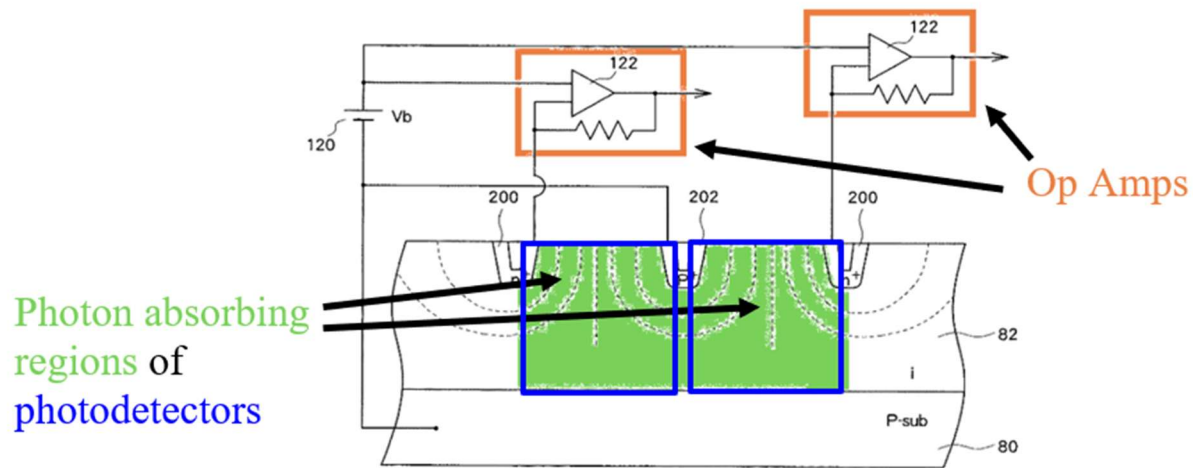
- b. [7b]: “and one or more additional **electronic processors** also formed on said **semiconductor substrate** and operatively associated with the respective **photon absorbing regions** of said additional **photodetectors** to receive therefrom and [procces] [sic] process said respective output electrical signals therefrom.”

Harada-Hasegawa renders this limitation obvious. Lebbly, ¶166. *Harada-Hasegawa* includes *Harada*’s photodiode combined with *Hasegawa*’s signal-

processing circuitry, formed on a single substrate. VI.A.1.c. *Hasegawa's* signal-processing circuitry includes multiple portions of signal-processing part 66 (one or more additional electronic processors) formed on the same semiconductor substrate, each portion including one or more components such as CMOS devices 68 and/or op amps 122:



Hasegawa, Fig. 1 (left), Fig. 7 (right); *Hasegawa*, [23], [26], [42], [46].



Hasegawa, Fig. 8. *Hasegawa*'s portions of signal-processing circuitry (electronic processors), including CMOS devices and/or op amps, are “operatively associated with the respective photon absorbing regions of said additional photodetectors,” because components of signal-processing circuit part receive electrical current generated by light incident on the i-layer regions (photon absorbing regions) of *Hasegawa*'s photodiodes (additional photodetectors). *Hasegawa*, [26]-[29], [46]-[47], [49]; Lebbby, ¶166.

Hasegawa applies a reverse-bias voltage to the cathode and anode regions to create and expand a depletion layer in the i-layer. *Hasegawa*, [27], [31], [46], [47]. In this way, *Hasegawa*'s additional electronic processors are “operatively associated” with the photon absorbing regions of one or more additional photodetectors. Lebbby, ¶167.

As previously discussed, *Hasegawa*'s electronic processor receives and processes an output signal from the photon absorbing region and provides a processed output. VI.A.2.f ([1c]). POSITAs would have understood that additional electronic processors would have similarly received and processed output signals from photon absorbing regions of at least one additional photodetector, consistent with *Hasegawa*'s disclosure of [1c]. VI.A.2.f; Lebbby, ¶168.

8. Claim 8: “The integrated detector/processing circuit of claim 1, wherein the plurality of holes enhances absorption of photons compared to a hole-free but otherwise same photodetector at a range of wavelengths that includes a wavelength of said source signal.”

Harada-Hasegawa renders obvious this limitation. Lebbby, ¶169. *Harada* creates holes in the i-layer so that “the light-receiving surface area can be made large and light-receiving efficiency can [be] made high without reducing response speed.” *Harada*, [16]. “[B]y providing the holes 4, the light-receiving surface area in this photodiode becomes larger,” and due to the presence of “side surfaces of the holes 4,” absorption is greater “than in the situation in which no holes 4 are present.” *Harada*, [14], [16]. *Harada*'s disclosure of increasing the light-receiving surface area and improving efficiency thus discloses the claim limitation: “the plurality of holes enhances absorption of photons compared to a hole-free but otherwise same photodetector.” Lebbby, ¶169.

Harada-Hasegawa renders obvious an “optical source signal modulated for data communication.” VI.A.2.c ([1a(ii)]). *Harada* also discloses enhancing photo absorption for “[c]onventional[]” photodiodes that detect optical wavelengths of approximately 700-870 nm, thus disclosing the claimed “range of wavelengths that includes a wavelength of said source signal.” *Harada*, [3]; Lebbby, ¶170.

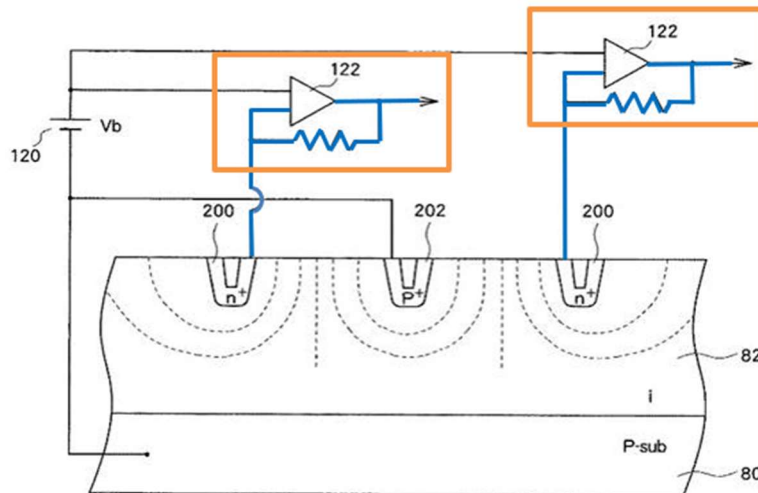
9. **Claim 9: “The integrated detector/processing circuit of claim 1, wherein the electronic processor includes one or more types selected from a group consisting of: transimpedance amplifier, signal processing electronics, and routing electronics.”**

Harada-Hasegawa renders this limitation obvious. Lebbby, ¶171. *Harada-Hasegawa* includes *Harada*’s photodiode combined with *Hasegawa*’s signal-processing circuit part (electronic processor). VI.A.1.c, VI.A.2.a, VI.A.2.f. *Hasegawa*’s signal-processing circuit part includes at least the claimed “signal processing electronics” and “transimpedance amplifier.” *Hasegawa*, [9], [14], [17], [25]-[26], [42], [46], Figs. 4, 8; Lebbby, ¶171.

Signal-processing circuit part 66 includes “signal processing electronics.” Lebbby, ¶172. For example, *Hasegawa*’s signal-processing circuit part includes “circuit elements, such as CMOSs 68,” which constitute the claimed “signal processing electronics.” *Hasegawa*, [14], [17], [22], [25]; Lebbby, ¶172.

Signal-processing circuit part 66 also includes a “transimpedance amplifier.” Lebbby, ¶173. For example, *Hasegawa*’s signal-processing circuit includes op

amps 122, which have a resistor bridging the input from the photodiode to the amplifier 122 output, creating a current detector device:



Hasegawa, Figs. 4, 8, [26], [46]. Op amps 122 are examples of a “transimpedance amplifier.” Lebbby, ¶173. A transimpedance amplifier (also known as a “current-to-voltage converter”) was understood to be an “op amp circuit configuration consisting of the op amp and a single, negative feedback resistor for converting an input current signal into an output voltage signal.” *Graeme* (Ex-1021), 135, 139; Lebbby, ¶173. *Hasegawa* describes this configuration and thus discloses claim 9’s “signal processing electronics” and “transimpedance amplifier.” *Hasegawa*, Figs. 4, 8, [26], [46]; Lebbby, ¶173.

10. Independent Claim 11

- a. [11pre]: “A photodetector with microstructure-enhanced photoabsorption comprising:”**

Harada discloses the preamble for the same reasons explained for [1pre(ii)].

VI.A.2.a.ii; Lebbby, ¶174.

- b. [11a(i)]: “a photon absorbing region that comprises an I-region between an N-region and a P-region, said I-region having a thickness between 0.5 and 5 micrometers”**

Harada-Hasegawa renders obvious this limitation for the reasons explained for [1b(i)] and [2]. VI.A.2.d, VI.A.3; Lebbby, ¶175.

- c. [11a(ii)]: and configured to absorb photons from a source signal modulated for data communication and provide an output electrical signal corresponding thereto;**

Harada-Hasegawa renders obvious this limitation for the reasons explained for [1a(i)]. VI.A.2.b; Lebbby, ¶176.

- d. [11b(i)]: said photon absorbing region comprising silicon in a substantially continuous layer interrupted by a plurality of holes extending through at least a portion of the thickness of the I-region**

Harada discloses this limitation. Lebbby, ¶177. *Harada*’s “photon absorbing region” ([11a(i)]) comprises “silicon.” *Harada*, [10]-[13]; VI.A.10.b. *Harada*’s “photon absorbing region” meets this limitation for the reasons discussed for [1b(i)]. VI.A.2.d; Lebbby, ¶177.

- e. **[11b(ii)]: and configured to concurrently receive the same source signal at a plural number of the holes; and**

Harada-Hasegawa renders obvious this limitation for the reasons explained for [1b(ii)]. VI.A.2.e; Lebbby, ¶178.

- f. **[11c]: said photon absorbing region being configured to absorb in excess of 40% of the incident source signal at wavelengths in at least one of the ranges from 800 nm to 900 nm and from 1400 nm to 1700 nm and provide an output electrical signal corresponding thereto.**

Harada-Hasegawa renders obvious this limitation. Lebbby, ¶179. *Harada* discloses conventional photodiodes that achieve a quantum efficiency of 70% or more at wavelengths of approximately 700-870 nm (“at least one of the ranges from 800 nm to 900 nm and from 1400 nm to 1700 nm”), using an i-layer (photon absorbing region) having a thickness equal to or larger than the absorption length. *Harada*, [3]; VI.A.3, VI.A.5. *Harada*’s techniques improve upon conventional photodiodes without increasing the i-layer thickness. *Harada*, [7]-[9]. Thus, a POSITA would have understood that *Harada*’s improved photodiodes include at least 70% quantum efficiency. Lebbby, ¶179. As explained for claims [4]/[6], a POSITA would have understood that the absorption of incident source signal light is proportional to the photodiode’s quantum efficiency. VI.A.5; Lebbby, ¶179.

Therefore, *Harada* discloses absorption “in excess of 40% of the incident source signal” in at least the 800-900 nm range. *Harada*, [3]; Lebbby, ¶179.

Harada’s photodiode includes p-electrode 6 that connects to an “output circuit” for outputting electric current generated from the absorbed photons. *Harada*, [15]. *Harada* thus discloses “provid[ing] an output electrical signal corresponding” to the absorbed incident source signal. Lebbby, ¶180.

11. **Claim 12: “The photodetector of claim 11, wherein the photon absorbing region is configured to absorb in excess of 40% of the incident source signal at wavelengths from 800 nm to 900 nm and provide an output electrical signal corresponding thereto.”**

Harada-Hasegawa renders obvious this limitation for the reasons that *Harada-Hasegawa* renders obvious [11c]. VI.A.10.f; Lebbby, ¶181.

12. **Claim 13: “The photodetector of claim 11, wherein the photon absorbing region is configured to absorb in excess of 50% of the incident source signal at wavelengths from 800 nm to 900 nm and provide an output electrical signal corresponding thereto.”**

Harada-Hasegawa renders obvious this limitation. Lebbby, ¶182. As explained for [11c], *Harada* discloses a quantum efficiency of 70% or more at wavelengths between 700-870 nm. *Harada*, [3]. *Harada*’s disclosure of absorption of 70% or more is “in excess of 50%.” VI.A.10.f; Lebbby, ¶182.

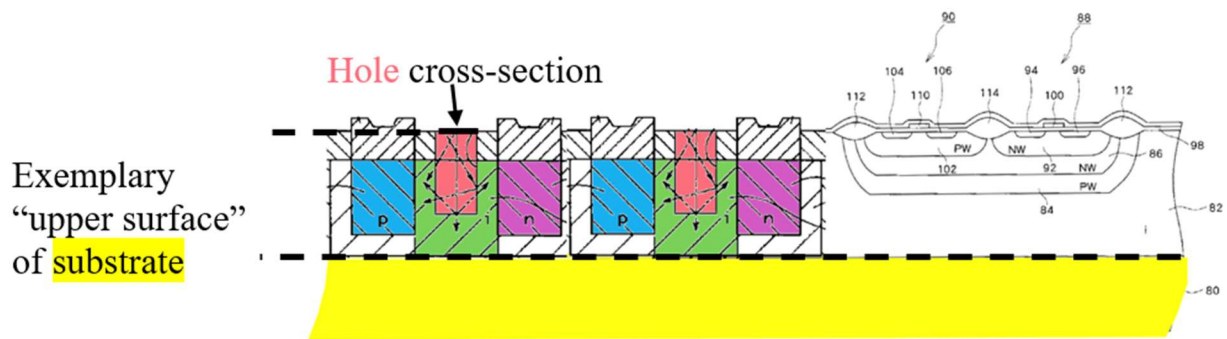
13. **Claim 14: The photodetector of claim 11, wherein the photon absorbing region is configured to absorb the incident source signal at an absorption percentage that varies by less than 20% over wavelength spans of at least 20 nm of source signal wavelengths from 800 nm to 900 nm.**

Harada-Hasegawa renders this limitation obvious for the reasons explained for [5]. VI.A.6; Lebbby, ¶183.

14. **Claim 15**

- a. [15a]: “The photodetector of claim 11, wherein each **hole** has a cross-section parallel to the upper surface of the **substrate** and has a maximum dimension of between 400 nm and 2500 nm,”

Harada-Hasegawa discloses this limitation. Lebbby, ¶184. In *Harada-Hasegawa*, *Harada*’s photodiode is formed on a **substrate** alongside *Hasegawa*’s signal-processing circuit part:



Exemplary combination of Harada's PiN photodiodes with Hasegawa's processing circuitry on the same substrate, based on Harada's Figure 1 and Hasegawa's

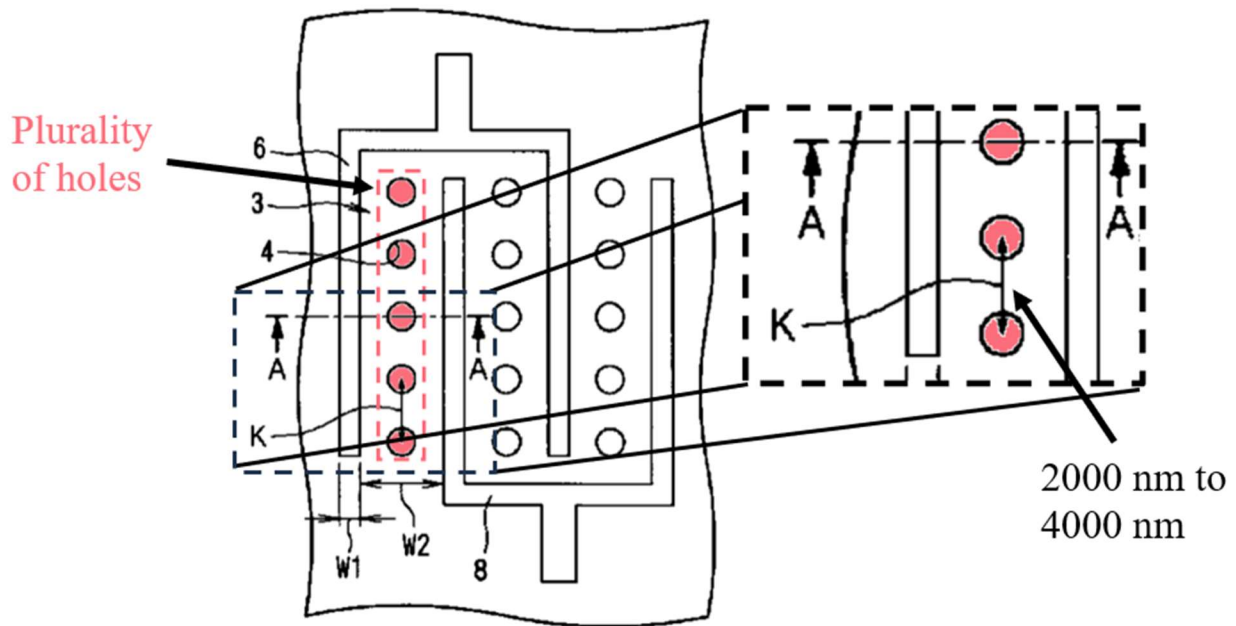
Figure 7

Harada-Hasegawa's substrate is directly beneath Harada's photodiode's i-layer and i-layer 82 in Hasegawa's signal-processing circuit part. The substrate includes an "upper surface," and a cross-section of Harada's photodiode hole is parallel to the substrate's "upper surface" indicated by the dashed line. Lebbby, ¶184.

Each hole of Harada's photodiode has a "maximum dimension of between 400 nm and 2500 nm" because Harada discloses a "1 μm " (or 1000 nm) hole diameter. Harada, [14], Fig. 1; Lebbby, ¶185; *In re Peterson*, 315 F.3d 1325, 1329 (Fed. Cir. 2003) ("[E]ven a slight overlap in range establishes a *prima facie* case of obviousness.").

- b. [15b]: “and each hole has a center that is spaced apart by less than 3500 nm from a center of a nearest adjacent hole of the plurality of holes.”

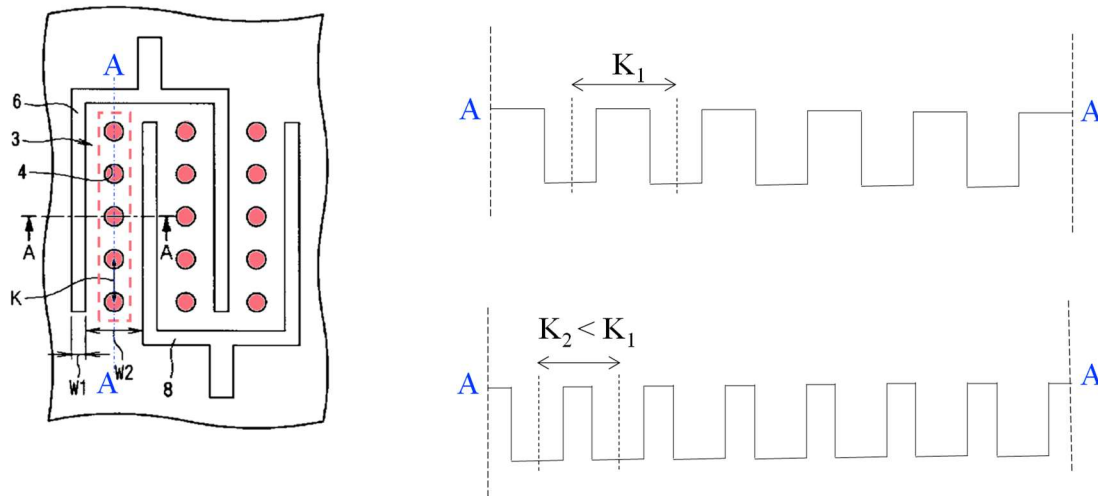
Harada-Hasegawa renders obvious this limitation. Lebbby, ¶186. *Harada* discloses a plurality of holes spaced apart by pitch K of 2000-4000 nm:



Harada, Fig. 2, [14]. Pitch K is a distance between the centers of nearest adjacent holes. Lebbby, ¶186. Because *Harada* discloses 2000-4000 nm spacing, *Harada* discloses that “each hole has a center that is spaced apart by less than 3500 nm.” *Id.*

Additionally, *Harada*’s disclosed hole-hole spacing range—2000-4000 nm—overlaps with the claimed range of less than 3500 nm, and thus *Harada* renders the claimed range obvious. Lebbby, ¶187; *In re Peterson*, 315 F.3d at 1329. A range of less than 3500 nm would have been obvious based on *Harada*’s disclosure.

Harada's holes increase light-receiving efficiency of its photodiode by increasing the light-receiving surface area. *Harada*, [16]. A POSITA would have recognized that increasing the number of holes 4 increases the light-receiving surface area and therefore the light-receiving efficiency. Lebbly, ¶187.



Harada, Fig. 2 (left); Lebbly, ¶187 (right). Thus, it would have been obvious to select a hole-hole spacing (K) closer to the lower end of *Harada*'s 2000-4000 nm range, or less than the claimed 3500 nm, to allow for more holes and increase light-receiving efficiency. Lebbly, ¶187.

15. Independent Claim 17

- a. [17pre]: “A photodetector with microstructure-enhanced photoabsorption comprising:”

Harada discloses [17pre] for the same reasons that *Harada* discloses [1pre(ii)]. VI.A.2.a.ii; Lebbly, ¶188.

b. [17a]: “a cathode region;”

Harada discloses this limitation for the same reasons that *Harada* discloses “a cathode region” for [1e(i)]. VI.A.2.h; Lebby, ¶189.

c. [17b]: “an anode region;”

Harada discloses this limitation for the same reasons that *Harada* discloses “an anode region” for [1e(i)]. VI.A.2.h; Lebby, ¶190.

d. [17c]: “reverse biasing circuitry configured to apply a voltage between said cathode and anode regions such that said cathode region is driven to a more positive voltage than said anode region;”

Harada-Hasegawa renders this limitation obvious for the same reasons as [1e(ii)]. VI.A.2.i; Lebby, ¶191.

e. [17d]: “a substrate material having an upper surface; and”

Harada-Hasegawa renders obvious this limitation. As explained for [15a], *Hasegawa* teaches a single semiconductor substrate made of silicon which is a “substrate material.” *Hasegawa*, [14], Fig. 1. The *Harada-Hasegawa* substrate has an “upper surface.” VI.A.14.a; Lebby, ¶192.

- f. **[17e(i)]: “a photon absorbing I-region comprising silicon, operatively associated with the cathode and anode regions, and configured to absorb photons from a source signal, said photon absorbing I-region including a substantially continuous layer interrupted by a plurality of holes”**

Harada discloses this limitation. Lebbby, ¶193. *Harada* discloses the claimed “photon absorbing I-region” for the same reasons that *Harada* discloses “said photon absorbing region comprising silicon in a substantially continuous layer interrupted by a plurality of holes extending through at least a portion of the thickness of the I-region.” VI.A.10.d ([11b(i)]). *Harada* also discloses this limitation for the reasons *Harada* discloses “a cathode region and an anode region operatively associated with said photon absorbing region.” VI.A.2.h ([1e(i)]). Furthermore, *Harada* discloses a photon absorbing region configured to absorb photons from a source signal for the same reasons that *Harada* discloses [1a(i)]. VI.A.2.b; Lebbby, ¶193.

- g. **[17e(ii)]: “each having a cross section parallel to the upper substrate surface having a maximum dimension of between 400 nm and 2500 nm, and each hole having a center that is spaced apart by less than 3500 nm from a center of a nearest adjacent hole of the plurality of holes,”**

Harada-Hasegawa renders obvious this limitation for the same reasons as explained for claim [15]. VI.A.14.a. Furthermore, the claimed range of “less than

3500 nm” would have been obvious to a POSITA in view of *Harada*. VI.A.14.b; Lebbby, ¶¶194-195.

- h. [17e(iii)]: “said I-region being configured to absorb photons from a source signal that has a substantially continuous profile illuminating an area that includes plural holes in the I-region.”**

Harada discloses an “I-region being configured to absorb photons from a source signal” for the reasons discussed for [1a(i)]. VI.A.2.b; Lebbby, ¶196.

Harada further renders obvious “a source signal that has a substantially continuous profile illuminating an area that includes plural holes in the I-region” for the same reasons that *Harada-Hasegawa* renders obvious a “photon absorbing region ... configured to concurrently receive the same source signal at a plural number of the holes.” VI.A.2.e ([1b(ii)]); Lebbby, ¶197. A POSITA would have understood that a source signal that is “concurrently receive[d] ... at a plural number of the holes” ([1b(ii)]) would be a source signal having “a substantially continuous profile illuminating an area that includes plural holes.” Lebbby, ¶198.

Harada discloses a light-receiving surface having multiple holes (*Harada*, [15], Fig. 2), and *Hasegawa* discloses an optical signal illuminating multiple photo detectors (*Hasegawa*, [4]-[5], Fig. 9). Furthermore, a POSITA would have understood that an optical signal has a distribution of intensity over a light-receiving area. Lebbby, ¶199. The light signal would have a profile that is spread

over an area of the light-receiving surface such that it “has a substantially continuous profile illuminating an area that includes plural holes.” *See Makita*, [23], Fig. 5; Lebbby, ¶199.

- 16. Claim 18: “The photodetector of claim 17 wherein the source signal has a wavelength that is greater than 800 nm and less than 1000 nm.”**

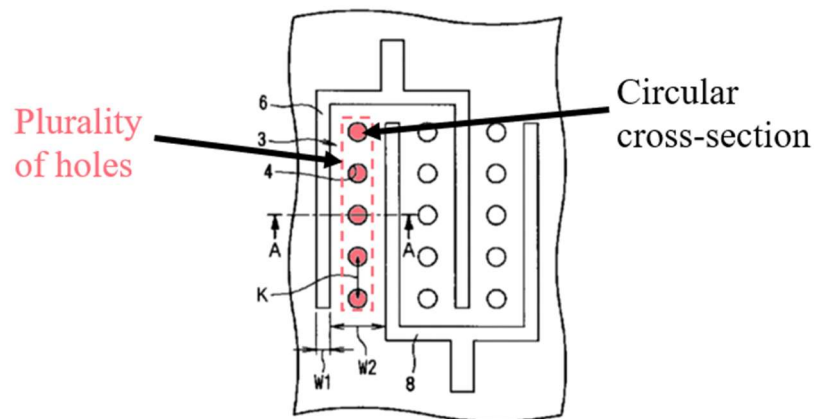
Harada discloses this limitation because *Harada* discloses improving upon photodiodes configured to detect wavelengths of 700-870 nm (“greater than 800 nm and less than 1000 nm”). *Harada*, [3]; Lebbby, ¶200.

- 17. Claim 19: “The photodetector according to claim 17 wherein the plurality of holes enhances absorption of photons compared to a hole-free but otherwise same photodetector at a range of wavelengths that includes a wavelength of said source signal.”**

Harada discloses this limitation for the same reasons that *Harada* discloses [8]. VI.A.8; Lebbby, ¶201.

- 18. Claim 20: “The photodetector according to claim 17 wherein each of the holes has a predominately circular cross-section parallel to the upper substrate surface.”**

Harada discloses this limitation. Lebbby, ¶202. Each of the plurality of *Harada*’s **holes** has a *circular* cross-section:



Harada, Fig. 2; Each hole has a “cross-section parallel to the upper substrate surface” for the same reasons that *Harada-Hasegawa* renders obvious “a cross-section parallel to the upper surface of the substrate.” VI.A.14.a ([15a]); Lebby, ¶202.

19. **Claim 21: “The photodetector according to claim 17 wherein the cathode and anode regions are operatively connected to integrated circuit electronics and the photodetector and integrated circuit electronics are integrated into a single silicon chip.”**

Harada-Hasegawa renders claim 21 obvious. Lebby, ¶203. *Harada*’s photodiode includes cathode and anode regions. VI.A.2.h ([1e(i)]). *Harada*’s photodiode is connected to an output circuit (*Harada*, [15]), but *Harada* does not otherwise detail whether its cathode and anode regions are “operatively connected to integrated circuit electronics.” It would have been obvious to combine *Harada* with *Hasegawa*, yielding a photodiode (photodetector) and signal-processing

circuit part (integrated circuit electronics) integrated into a single silicon (semiconductor) chip. VI.A.1.c; Lebby, ¶203.

Harada-Hasegawa includes a photodiode with anode and cathode regions “operatively connected to integrated circuit electronics.” Lebby, ¶204. *Harada*’s photodiode provides an output signal by converting absorbed light to a current. *Harada*, [8], [15]. *Harada*’s photodiode includes “anode” and “cathode region[s].” VI.A.2.h ([1e(i)]). A POSITA would have understood that *Harada*’s anode and cathode regions would be “operatively connected to integrated circuit electronics,” such as *Hasegawa*’s signal-processing circuit part, because *Harada* teaches using its p-electrodes 6 and 11 (exemplary anode regions) and its n-electrode 8 (cathode region) to detect a current. *Harada*, [15]; Lebby, ¶204.

Hasegawa teaches connecting anode and cathode regions to integrated circuit electronics. Lebby, ¶205. *Hasegawa*’s reverse-biasing circuitry applies a reverse-bias voltage to drive cathode regions 200 to a more positive voltage than anode region 202, by connecting a positive voltage and cathode regions 200 to op amp 122 (an example of integrated circuit electronics). *Hasegawa*, [46]-[47], Fig. 8. *Hasegawa* further discloses wirings 74/76 connecting anode and cathode regions to CMOS devices 68 (integrated circuit electronics) for detecting and processing an electrical signal generated by light incident on an i-layer. *Hasegawa*, [16], [22], [26], [42], [55], Figs. 1-4, 7-8; Lebby, ¶205.

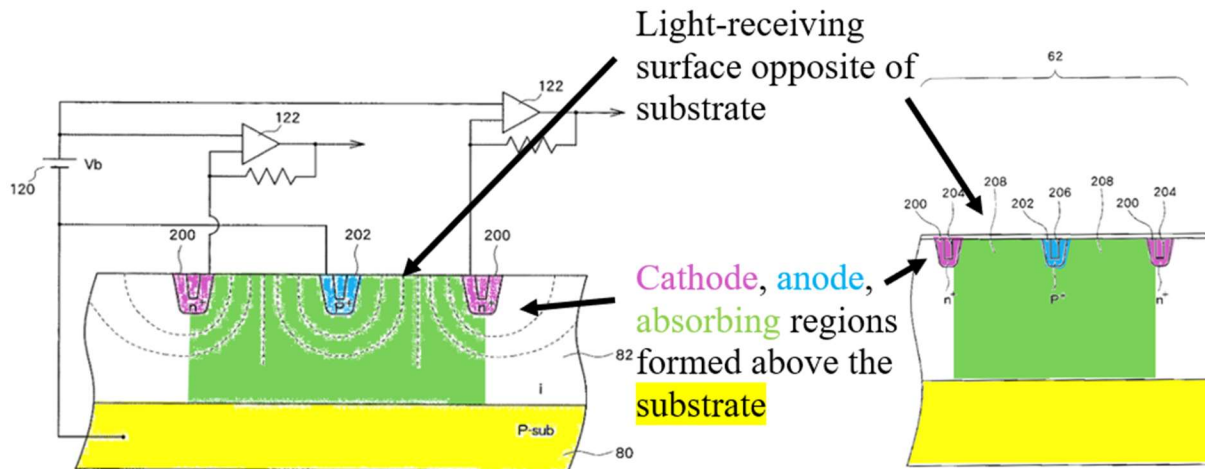
It would have been obvious to apply *Hasegawa*'s wiring and output connections to *Harada*'s cathode regions (n-electrode 8 and/or n-layer 7) and anode regions (p-electrode 6 and/or p-layer 5) to detect a current generated by photons in *Harada*'s i-layer 15. VI.A.2.h; Lebby, ¶206.

20. **Claim 24: “The photodetector according to claim 17 further including a substrate and wherein the cathode, absorbing[,] and anode regions are formed above the substrate and the photodetector is configured to receive the source signal from directions facing a side of the photodetector opposite of the substrate”**

Harada-Hasegawa renders claim 24 obvious. *Harada-Hasegawa* has “a substrate” for the same reasons that *Harada-Hasegawa* discloses a “substrate.” *Harada*, [10], [13], Fig. 1; VI.A.14.a ([15a]); Lebby, ¶207.

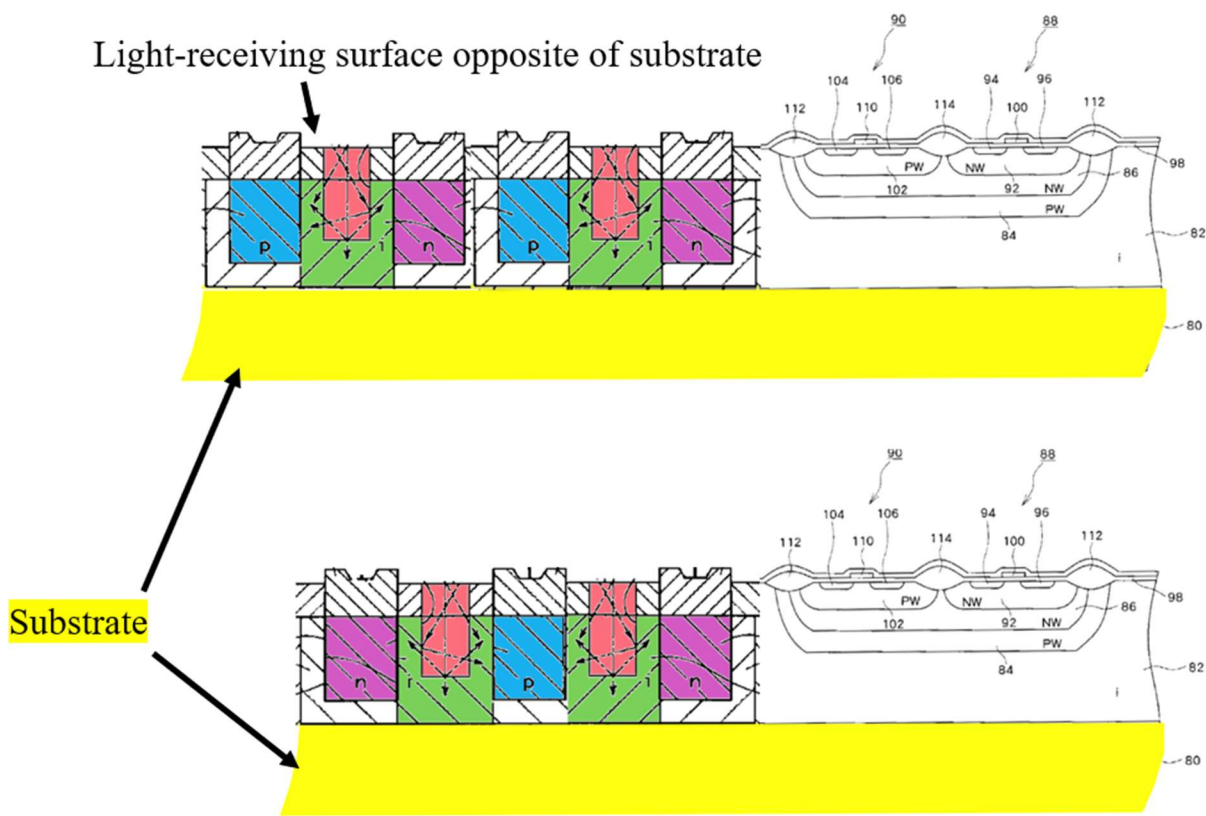
Harada-Hasegawa includes a single substrate on which both the photodetector (having one or more photodiodes) and electronic processor are formed, as taught by *Hasegawa*. VI.A.1.c. *Harada* discloses cathode, absorbing, and anode regions formed above a substrate, and the photodiode is configured to receive the source signal at a light-receiving surface 3 on a side of the photodiode opposite of the substrate. *Harada*, [10], [13]-[16], [19], Fig. 1; VI.A.2.h; Lebby, ¶208. *Hasegawa* discloses (1) a substrate; (2) cathode, absorbing, and anode regions formed above the substrate; and (3) that the photodiode receives the source

signal at a light-receiving surface on a side of the photodiode opposite of the
substrate:



Hasegawa, [14], [18]-[21], [29], [35]-[36], [39], [42], Figs. 8 (left), 7 (right, excerpted); see also *Hasegawa*, Figs. 3-4; Lebbby, ¶208.

Consistent with *Harada*'s and *Hasegawa*'s disclosures above, a POSITA would have understood that *Harada-Hasegawa* includes *Harada*'s photodiode formed on a substrate such as *Hasegawa*'s substrate 80, such that the anode, cathode, and absorbing regions would be formed above the substrate, consistent with *Harada*'s Figure 1. Lebbby, ¶209.



Diagrams A (top) and B (bottom)

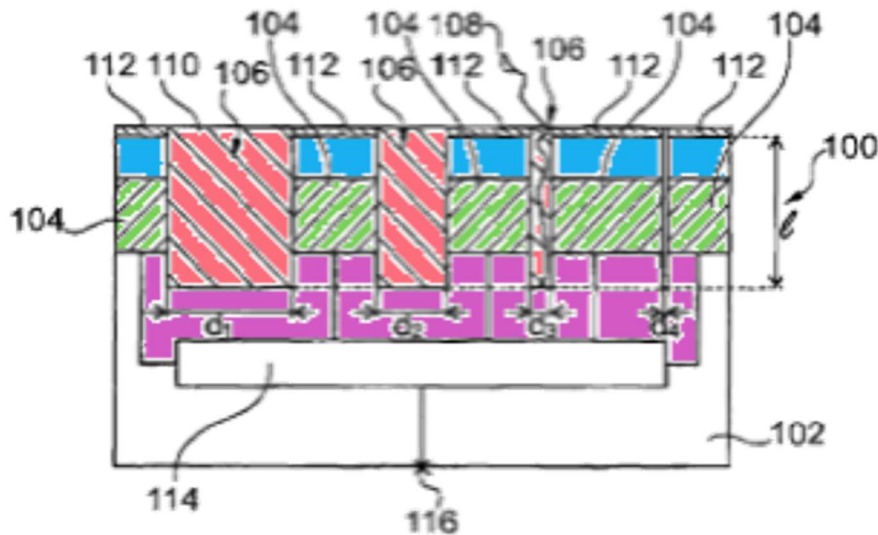
As shown, a POSITA also would have understood that *Harada-Hasegawa* includes a photodiode that is a photodetector “configured to receive the source signal from directions facing a side of the photodetector opposite of the **substrate**.” Leiby, ¶209.

B. Ground 2: Claim 7 Is Obvious over *Harada* and *Hasegawa* in View of *NXP*

1. Overview of *NXP*

NXP’s photodetector device has one or more photodiodes for detecting electromagnetic radiation including light signals. *NXP*, Abstract, ¶¶[8], [11]. The

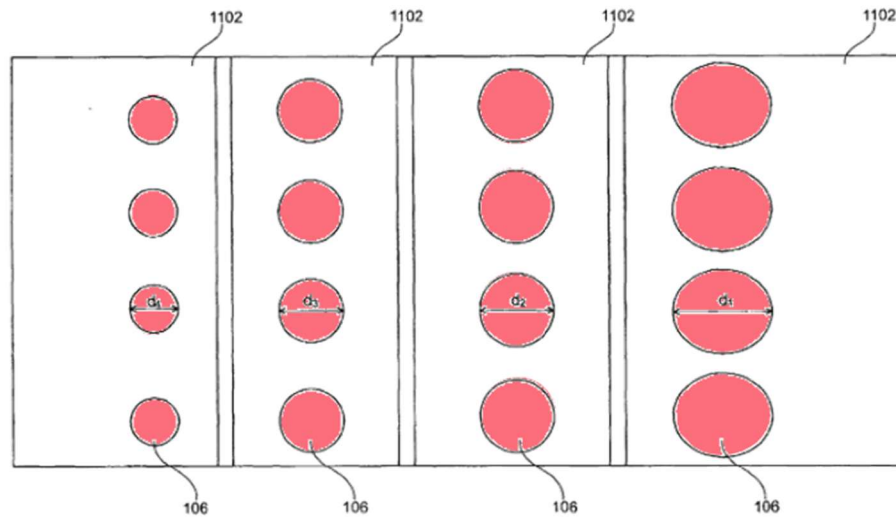
photodetector includes an array of **PiN** photodiodes having **pores (holes)** formed in the **I-layer** and a signal-processing circuit 114:



NXP, ¶¶[11]-[12], [26], [32], [69], Fig. 6 (above). *NXP*'s photodiodes and processing circuitry are monolithically integrated on the same silicon substrate.

NXP, ¶[32], Figs. 15-16. Lebbby, ¶210.

NXP's diodes each have a plurality of pores (holes), and the pore dimensions in one diode differ from pores of another diode. Lebbby, ¶211. For example, as shown below, a first diode's pore diameter d_1 is smaller than a second diode's pore diameter d_2 :



NXP, Fig. 14, ¶¶[72], [90]. *NXP*'s silicon photodiodes detect wavelengths of 190-1100 nm, and each diode is configured to be sensitive to a different target wavelength based on the pore dimensions. *NXP*, ¶¶[8], [16], [37]-[38], [71]-[74], [87], [96]; Lebbby, ¶211.

2. Claim 7

Harada-Hasegawa-NXP renders claim 7 obvious. Lebbby, ¶212. *Harada-Hasegawa* is an integrated photodetector/integrated circuit having “one or more additional photodetectors formed on said semiconductor substrate and having respective photon absorbing regions.” VI.A.7.a. *Harada*'s photodiodes are formed on a substrate with *Hasegawa*'s signal-processing circuit (one or more additional electronic processors). *Hasegawa*'s signal-processing circuit includes CMOS device 68 and op amp 122, which are “operatively associated with the respective photon absorbing regions of said additional photodetectors.” VI.A.7.b. And as

discussed, *Hasegawa*'s electronic processor receives and processes an output signal from the photon absorbing region and provides a processed output. VI.A.2.f ([1c]); Lebbby, ¶212.

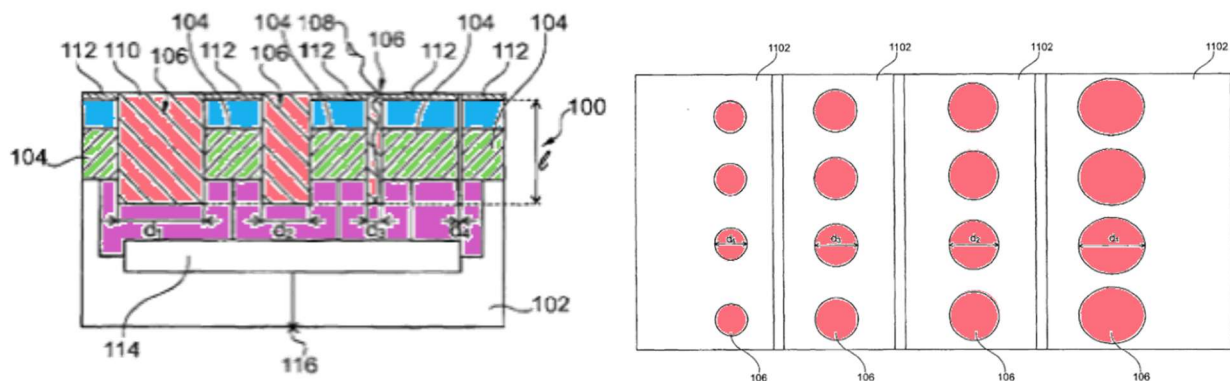
As discussed in VI.A.7.a, “respective additional source signals” may include different wavelength bands of an optical signal transmission, such as channels of a wavelength division multiplexing (WDM) transmission.⁸ '084 patent, 16:61-67, 17:62-18:13, 33:24-33, 33:38-52; Lebbby, ¶213; *see also* VI.A.7.a.ii. WDM was known before the '084 patent as a technique of transmitting multiple light wavelength channels simultaneously in a combined optical signal to carry independent information in each channel. Ex-1023 (published 1998). WDM uses microstructure-enhanced photodetectors configured for receiving different wavelength channels, as taught by *NXP*. Lebbby, ¶213.

Harada-Hasegawa discloses all structural elements of an integrated photodetector/integrated circuit device having one or more “additional photodetectors” and “additional electronic processors,” as explained in Ground 1. Lebbby, ¶214. *Harada-Hasegawa*, further modified in view of *NXP*, renders

⁸ As discussed in VI.A.7.a.ii, to the extent “respective additional source signals” requires only spatial portions (partitions) of a source signal, *Harada-Hasegawa* renders this limitation obvious.

obvious “having respective **photon absorbing regions** receiving respective additional source signals.” *Id.*

NXP discloses different photodiodes in an array that can detect different wavelengths (additional source signals) by forming holes in each photodiode having a diameter and period configured for a target wavelength band:



NXP, ¶¶[8], [69]-[70], [96], Figs. 6 (left), 14 (right), 8, 13, 18, 20; Lebbby, ¶215.

NXP’s figures disclose an integrated photodetector/integrated circuit device having four **PiN** diodes. Lebbby, ¶215. Each photodiode has a plurality of **pores 106 (holes)** of the same diameter, and the pore diameters differ between different photodiodes.

Id. Like *Harada*’s PiN photodiode with holes in i-layer 15 (photon absorbing region), *NXP* discloses PiN diodes with holes extending into an intrinsic region.

NXP, ¶¶[3], [5], [17], [77], [87]-[88]. *NXP* discloses that “any kind of wavelength detector can be made as it is only depending of the via diameter,” and it further discloses detecting wavelengths from 190-1100 nm using silicon. *NXP*, ¶¶[11],

[37]-[38]. *NXP*'s technique of forming holes of different sizes in different diodes would have enabled those diodes to receive different signal wavelengths ("additional source signals" under the second interpretation of [7a]). Lebbby, ¶215.

It would have been obvious to a POSITA to modify *Harada*'s photodiodes' hole dimensions based on *NXP*'s teachings, yielding an integrated photodetector/integrated circuit device configured to receive signals of different wavelengths (respective additional source signals) at each photodiode. Lebbby, ¶216. *NXP* is analogous art to the '084 patent, because both *NXP* and the '084 patent are pertinent to improving silicon-based photodetector device performance. *NXP*, ¶¶[15], [17], [70]-[74], [87]-[88]; '084 patent, 1:44-47; Lebbby, ¶216.

Modifying *Harada-Hasegawa* based on *NXP* would have involved applying *NXP*'s known technique of forming different hole sizes in different photodiodes to the array of *Harada*'s photodiodes in *Harada-Hasegawa*. Lebbby, ¶217. *Harada*'s photodiode and *NXP*'s photodiode are both silicon photodetectors with holes for enhanced absorption and sensitivity to light. *Id.* The modification would enable *Harada-Hasegawa*'s device to detect different wavelength bands at different diodes, expanding the uses of the combined device to include, for example, wavelength division multiplexing. *Id.* Detecting different wavelength bands with different photodiodes advantageously enables simultaneous reception of multiple separate communication channels. Ex-1023, 1. A POSITA would have understood

this would increase data bandwidth and speed of optical data transmissions. Ex-1023, 1-2; Lebbby, ¶217.

A POSITA would have reasonably expected success in achieving the modification. Lebbby, ¶218. Like *Harada* and *Hasegawa*, *NXP* discloses a silicon photodiode and fabrication processes that are compatible with silicon detectors. *NXP*, ¶¶[37], [40]. Like *Hasegawa*, *NXP* also discloses forming photodiodes and CMOS processing circuits together on the same substrate and “different detectors on the same silicon wafer.” *NXP*, ¶¶[16], [32], [37], [40], [46], [48], Fig. 6. A POSITA would have reasonably expected success in applying *NXP*’s teachings to form different size holes and/or periods in the photodiodes of *Harada-Hasegawa*. Lebbby, ¶218.

C. Ground 3: Claims 5 and 14 Are Obvious over *Harada* and *Hasegawa* in View of *Yahaya*

1. Overview of *Yahaya*

Yahaya discloses absorption measurements of silicon photodiodes showing improved absorption with holes in the silicon. *Yahaya*, 2-3. *Yahaya* discloses that nanostructures in a photodiode’s “active layer” (photon absorption i-layer) were known to enhance absorption performance. *Yahaya*, 2. *Yahaya* discloses absorption measured at wavelengths of 300-1100 nm for a silicon layer 1 μm thick having holes of $\sim 0.5 \mu\text{m}$ diameter and 0.5 μm depth:

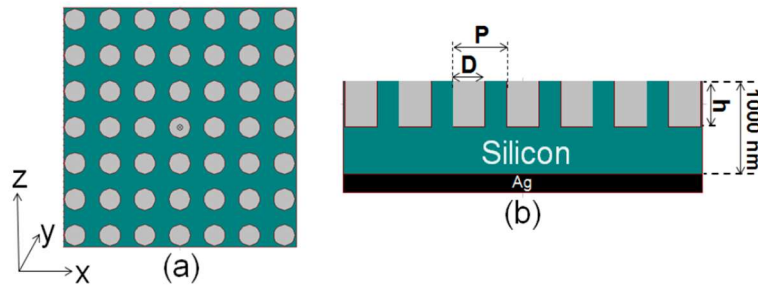


Fig. 1. Schematic of the c-Si NH arrays: (a) top view and (b) side view.

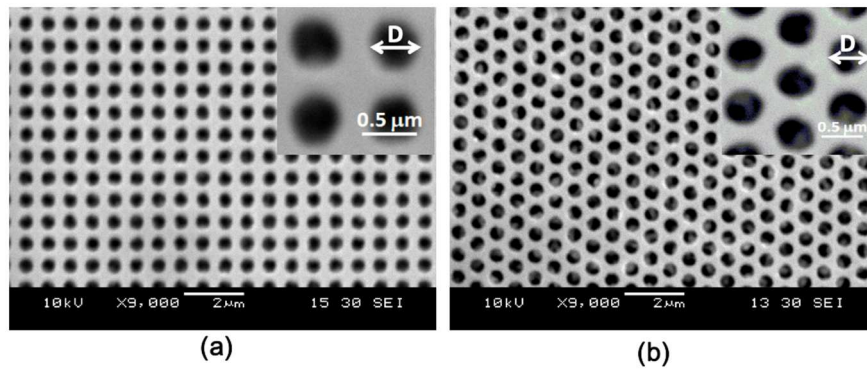
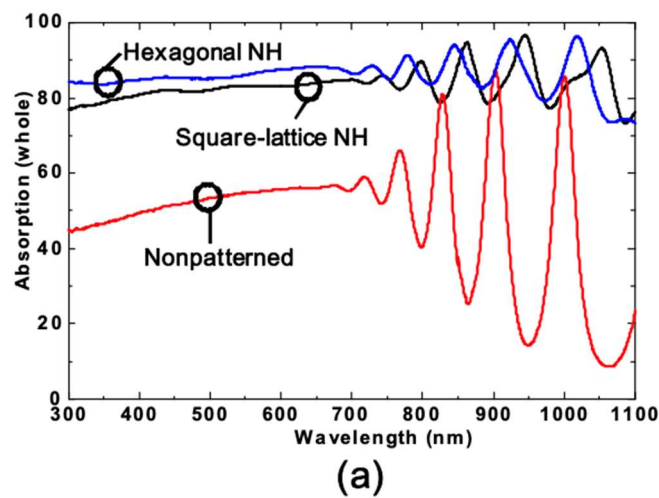


Fig. 3. SEM images of the fabricated (a) square-lattice and (b) hexagonal NH arrays on c-Si.

Yahaya, 3, 5, Figs. 1, 3. Absorption for nanohole (“NH”) silicon is typically above 80% and significantly higher than “nonpatterned” silicon:



Yahaya, 5, Fig. 4(a). Between 800-900 nm, absorption levels remained within the range of about 78%-95%, varying by less than 20%:

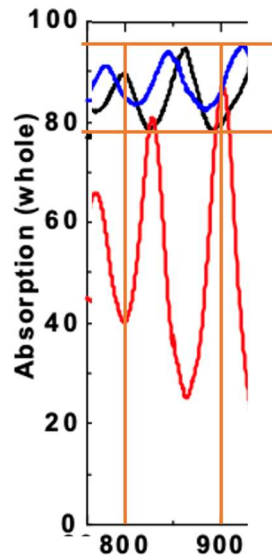


Diagram based on *Yahaya*'s Figure 4(a)

Yahaya, 5, Fig. 4(a); *Lebby*, ¶219.

2. Claim 5

Harada-Hasegawa includes *Harada*'s silicon photodiode with a photon absorbing region configured to absorb light. VI.A.2.a.iii, VI.A.2.b. Ground 1 explains how *Harada-Hasegawa*'s photodiode—having an array of holes in a silicon absorption layer—would render obvious claims 5 and 14's absorption properties. VI.A.6, VI.A.13; *Lebby*, ¶220. To the extent Patent Owner asserts otherwise, it would have been obvious to modify *Harada-Hasegawa*'s photodiode's holes based on *Yahaya*'s hole dimensions to achieve the claimed absorption properties. *Lebby*, ¶220.

Harada teaches improving photodiodes that receive wavelengths including 700-870 nm with 70% quantum efficiency, by creating holes in silicon i-layer 15 to efficiently receive a high-speed signal. *Harada*, [3], [15]-[17], [19]. *Harada* thus discloses absorption of 70% or greater over the 700-870 nm wavelength range. Lebbby, ¶221. *Harada* also discloses a 1000 nm hole diameter and 2000-4000 nm spacing, and *Harada* does not preclude using other hole dimensions. *Harada*, [14], Fig. 2; Lebbby, ¶221.

Yahaya discloses absorption measurements for silicon with nanoholes “optimized” for photoabsorption across wavelengths of 300-1100 nm. *Yahaya*, 5; Lebbby, ¶222. To achieve optimal absorption, *Yahaya* discloses a 0.5 μm hole depth, $<0.5 \mu\text{m}$ diameter, and 0.6 μm hole period/spacing.

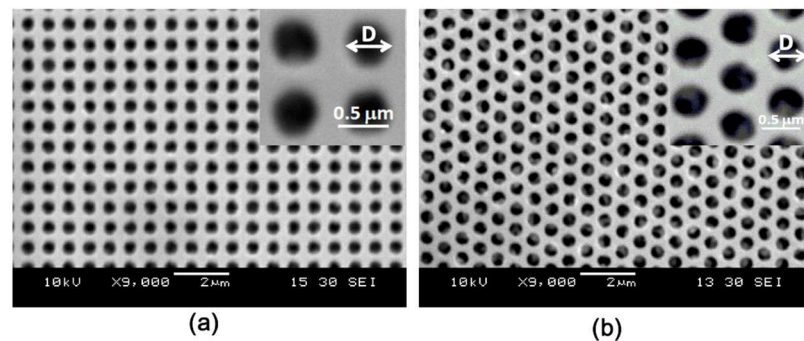
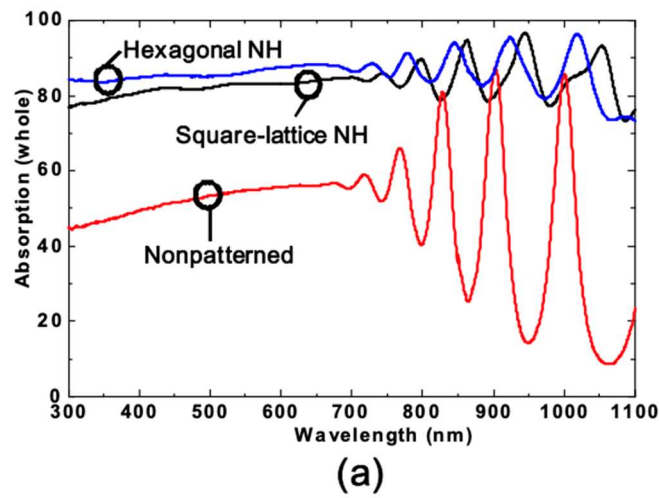


Fig. 3. SEM images of the fabricated (a) square-lattice and (b) hexagonal NH arrays on c-Si.

Yahaya, 3-6, Figs. 1, 3(a)-(b). *Yahaya*’s nanohole absorption measurements are significantly higher than “nonpatterned” silicon. *Yahaya*, 4-5.



Yahaya, 5, Fig. 4(a). For wavelength spans of at least 20 nm between 800-900 nm, absorption varies by less than 20% because all measured absorption levels between 800-900 nm are within ~78% to ~95%:

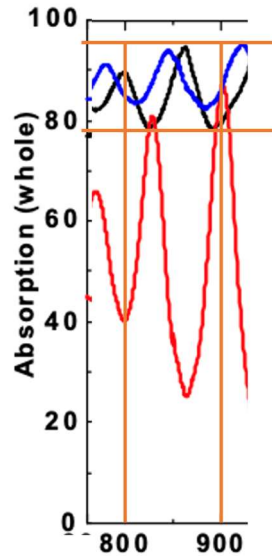
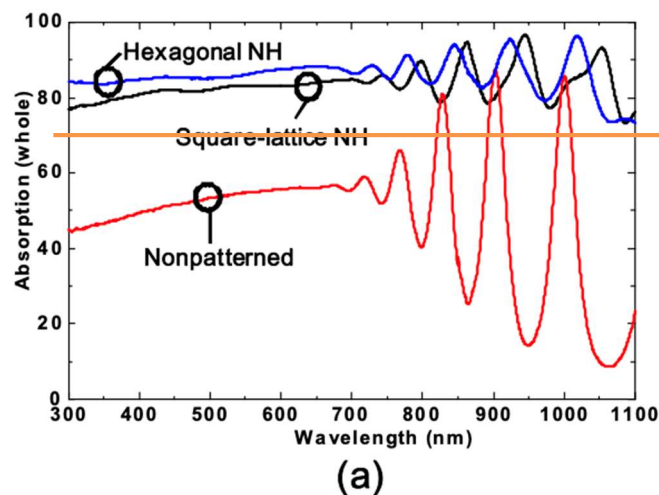


Diagram based on *Yahaya*'s Figure 4(a)

Yahaya, 5, Fig. 4(a); Lebby, ¶¶222-223.

It would have been obvious to a POSITA to modify *Harada-Hasegawa*'s photodiode based on *Yahaya*. Lebbby, ¶224. *Yahaya* is analogous art to the '084 patent because both are directed to improving performance of silicon-based photodiodes, such as by enhancing absorption using holes. *Id.* *Harada* discloses that it was known for silicon photodiodes to have 70% quantum efficiency between wavelengths of 700-870 nm, and *Harada* teaches creating holes to improve the light-receiving sensitivity and response time. *Harada*, [3], [7]-[8]. *Yahaya* echoes these teachings, disclosing hole dimensions for optimizing absorption with greater than 70% absorption. Lebbby, ¶224. *Yahaya* discloses that it was known for nanoholes to improve absorption in silicon, and discloses absorption greater than 70% at wavelengths of 700-870 nm:



Yahaya, 2, 5, Fig. 4(a) (orange line added indicating 70% absorption). Lebbby, ¶224.

A POSITA would have been motivated to adjust *Harada-Hasegawa*'s photodiode's hole sizing and spacing based on *Yahaya*'s teachings. Lebbby, ¶225. The combination includes *Harada*'s photodiode with an **array of holes** in the i-layer, having *Yahaya*'s hole sizing and spacing for optimal absorption across a wide range of wavelengths. *Id.*

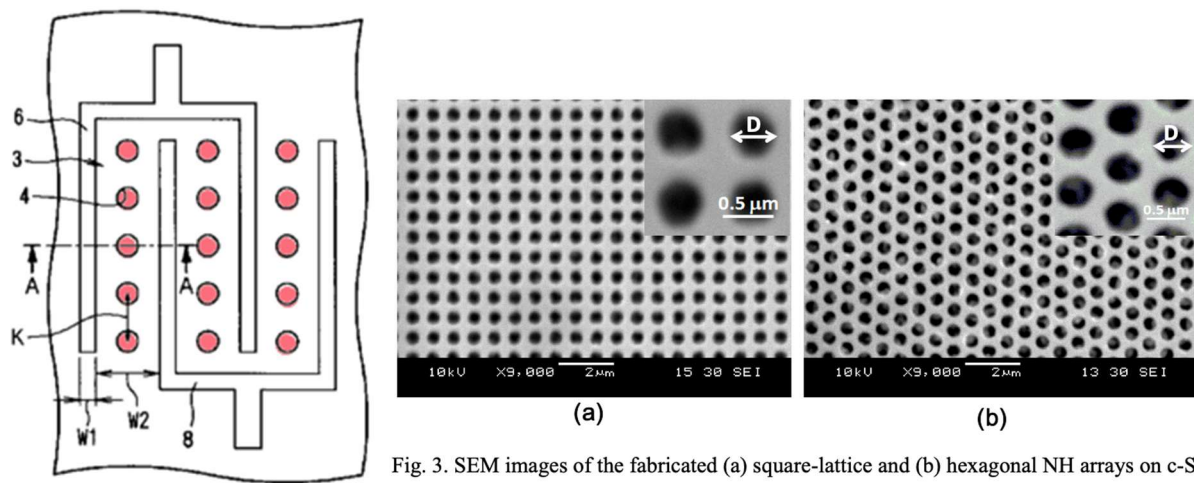


Fig. 3. SEM images of the fabricated (a) square-lattice and (b) hexagonal NH arrays on c-Si.

Harada, [6]-[8], [13]-[17], Fig. 2 (left); *Yahaya*, 3, 5-6, Figs. 3(a)-(b) (center and right). Additionally, while *Harada* illustrates a 1x5 array between p-electrode 6 and n-electrode 8, a POSITA would have been motivated to try different array sizes (e.g., a 2x5 array of smaller holes with closer spacing) between *Harada*'s electrodes to maximize light absorption, as taught by *Yahaya*. Lebbby, ¶¶226-228. The modification would have yielded absorption greater than 70% that varies by less than 20% across 20 nm spans between 800-900 nm (improving *Harada*'s photodiode), as shown in *Yahaya*'s Figure 4(a). Lebbby, ¶228.

A POSITA would have reasonably expected success in making such a modification because the only required changes would have been altering *Harada*'s holes according to *Yahaya*'s dimensions. Leiby, ¶229. Any modifications would have been within the abilities of a POSITA, and a POSITA would have understood that the combination would not have required any modification to the operation of *Harada*'s photodiode. Leiby, ¶¶229-230.

3. Claim 14

Harada-Hasegawa-Yahaya renders claim 14 obvious. Leiby, ¶231. Claim 14 depends from independent claim 11 and recites substantially the same limitations recited in [5]. Claim 14 is therefore obvious for substantially the same reasons that [5] is obvious based on *Harada-Hasegawa-Yahaya*. VI.C.2; Leiby, ¶231.

VII. Mandatory Notices

A. Real Parties-in-Interest

The real parties-in-interest are Samsung Electronics Co., Ltd.; Samsung Electronics America, Inc.; Samsung Semiconductor, Inc.; and Samsung Austin Semiconductor LLC.

B. Related Matters

Patent Owner W&Wsens Devices Inc. asserted the '084 patent in *W&Wsens Devices Inc. v. Samsung Electronics Co., Ltd., Samsung Electronics America, Inc.,*

Samsung Semiconductor, Inc., and Samsung Austin Semiconductor LLC, Case No.
2:24-cv-00854-JRG (E.D. Tex.).

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Please address all correspondence to counsel at the address above. Petitioner consents to electronic service by email at the above email addresses.

VIII. Grounds for Standing

Petitioner certifies that the '084 patent is available for IPR and that Petitioner is not barred or estopped from requesting IPR challenging the patent claims on the grounds identified herein.

IX. Conclusion

For the reasons above, Petitioner requests institution of IPR and cancellation of each challenged claim. The Office may charge any required fees to Deposit Account No. 06-0916.

Date: July 14, 2025

Respectfully submitted,

By: /Joshua L. Goldberg/
Joshua L. Goldberg
Lead Counsel
Reg. No. 59,369

CERTIFICATION OF WORD COUNT

Pursuant to 37 C.F.R. §42.24, Petitioner certifies that the word count of Petitioner's Petition for *Inter Partes* Review (exclusive of any table of contents, table of authorities, mandatory notices under §42.8, certificates of service and word count, and list of exhibits or claim listing) as measured by Microsoft Word is 13,696.

Dated: July 14, 2025

By: /Joshua L. Goldberg/
Joshua L. Goldberg
Lead Counsel
Reg. No. 59,369

CERTIFICATE OF SERVICE

Pursuant to 37 C.F.R. §§42.6(e) and 42.105(a), the undersigned certifies that on July 14, 2025, a copy of the foregoing **Petition for *Inter Partes* Review, the associated powers of attorney, and Exhibits 1001-1024, 1020-1024, and 1029-1030** were served by FedEx Priority Overnight on the correspondence address of record indicated in the Patent Office's public Patent Center system for U.S. Patent No. 9,525,084:

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Date: July 14, 2025

By: /William Esper/
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