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Photon-trapping microstructures enable high-speed high-efficiency silicon photodiodes

Yang Gao[1†], Hilal Cansizoglu[1†], Kazim G. Polat[1], Soroush Ghandiparsi[1], Ahmet Kaya[1], Hasina H. Mamtaz[1], Ahmed S. Mayet[1], Yinan Wang[1], Xinzhi Zhang[1], Toshishige Yamada[2,3], Ekaterina Ponizovskaya Devine[3], Aly F. Elrefaie[1,3], Shih-Yuan Wang[3] and M. Saif Islam[1*]

High-speed, high-efficiency photodetectors play an important role in optical communication links that are increasingly being used in data centres to handle higher volumes of data traffic and higher bandwidths, as big data and cloud computing continue to grow exponentially. Monolithic integration of optical components with signal-processing electronics on a single silicon chip is of paramount importance in the drive to reduce cost and improve performance. We report the first demonstration of micro- and nanoscale holes enabling light trapping in a silicon photodiode, which exhibits an ultrafast impulse response (full-width at half-maximum) of 30 ps and a high efficiency of more than 50%, for use in data-centre optical communications. The photodiode uses micro- and nanostructured holes to enhance, by an order of magnitude, the absorption efficiency of a thin intrinsic layer of less than 2 μm thickness and is designed for a data rate of 20 gigabits per second or higher at a wavelength of 850 nm. Further optimization can improve the efficiency to more than 70%.

The bandwidth limitations and microwave losses of copper cables and transmission lines are causing a data traffic bottleneck in data centres. The large volumes of data traffic at the rack-to-rack, board-to-board, chip-to-chip and intra-chip level in computer data centres have intensified the desire to develop monolithically integrated transmitters and receivers on Si. Optical-component fabrication methods need to be fully compatible with integrated circuit (IC) fabrication processes to enable integration with electronics such as trans-impedance amplifiers (TIAs) and other circuit elements necessary for signal processing and communication[1,2]. In the case of normal incident photodiodes for free-space or optical-fibre illumination, having a single Si chip rather than two chips and a multi chip carrier significantly reduces the cost of packaging the transceiver sub-assembly and improves performance, as parasitic capacitance, resistance and inductance are greatly suppressed when different components are monolithically integrated on a single chip. An important factor regarding optics for data communication in data centres is the cost per gigabit per second (Gb s^{-1}), which is currently on the scale of tens of dollars per Gb s^{-1}, on average, end to end. This needs to be reduced to single-digit dollars per Gb s^{-1} (ref. 3).

Si photodiodes are currently used predominantly in the visible wavelength regime, where the absorption coefficient α of Si is large. For example, α is 4,000 cm^{-1} and greater for wavelengths of 600 nm and shorter. However, for the short-reach (<300 m) multimode data communications wavelengths of 840–860 nm and also at a new short wavelength division multiplexing (SWDM) band of 850–950 nm that is being proposed[4], α for Si is 591 cm^{-1} at 840 nm and drops to 480 cm^{-1} at 860 nm wavelengths[5]. With such weak absorption, Si photodiodes need to have a thick absorption layer (the intrinsic or 'i' layer) to achieve an external quantum efficiency (EQE) of >50% in a p–i–n photodiode. For example, the i-layer needs to be 13 μm or thicker for a wavelength of 850 nm ($\alpha = 535$ cm^{-1}). This limits the data rate to 4 Gb s^{-1} or less due to the long transit time of photogenerated carriers in the thick i-region.

In addition to Si p–i–n photodiodes, several types of Si photodiodes have been demonstrated for wavelengths between 800 and 1,310 nm, including metal–semiconductor–metal (MSM) photodiodes[6], surface plasmon enhanced photodiodes[7] and avalanche photodiodes (APDs)[8–12], although low quantum efficiency, higher operating voltages, along with high noise (as in APDs) and low reliability, have limited their applications[13]. Another approach to effectively enhance the response of a weakly absorbing medium, without sacrificing device bandwidth, involves integrating an absorbing layer within a high-finesse planar Fabry–Pérot, or resonant, cavity[14]. A number of resonant cavity enhanced (RCE) photodiodes have been demonstrated using Si at 850 nm (ref. 14), employing distributed Bragg reflectors. Although there is a potential to fabricate such devices for 10 Gb s^{-1} applications with an EQE of ~50%, they are very wavelength-specific[15], which may require pairing of the transmitter wavelength with the receiver wavelength. A Si photodiode with less wavelength sensitivity is desirable in many applications, and this has motivated the research community to explore alternatives, including emerging two-dimensional materials-based photodiodes[16–18], flip-chip bonding of non-Si materials to Si (ref. 19), heteroepitaxy[20], waveguide integrated edge-illuminated photodiodes[21] and transfer printing[22] for high-speed and efficient photodetection on Si. However, in each case (as shown in Supplementary Table 1), there are issues in terms of yield, IC process compatibility, performance and packaging, which can make it too costly to implement in data centres. The 850 nm multimode optical data link is the most widely used for distances of less than 100 m for 25 Gb s^{-1} and 300 m for 10 Gb s^{-1} in data centres and is therefore the most price- and performance-sensitive[23].

This Article presents a new approach to designing and fabricating an all-silicon photodiode with wide spectral responses from 800 to 860 nm, >50% EQE and an ultrafast impulse response of 30 ps full-width at half-maximum (FWHM), measured using a subpicosecond 850 nm mode-locked fibre laser. The device is fabricated using

[1]Electrical and Computer Engineering, University of California, Davis, Davis, California 95618, USA. [2]Electrical Engineering, Baskin School of Engineering, University of California, Santa Cruz, Santa Cruz, California 95064, USA. [3]W&WSens Devices, Inc., 4546 El Camino, Suite 215, Los Altos, California 94022, USA. †These authors contributed equally to this work. *e-mail: sislam@ucdavis.edu

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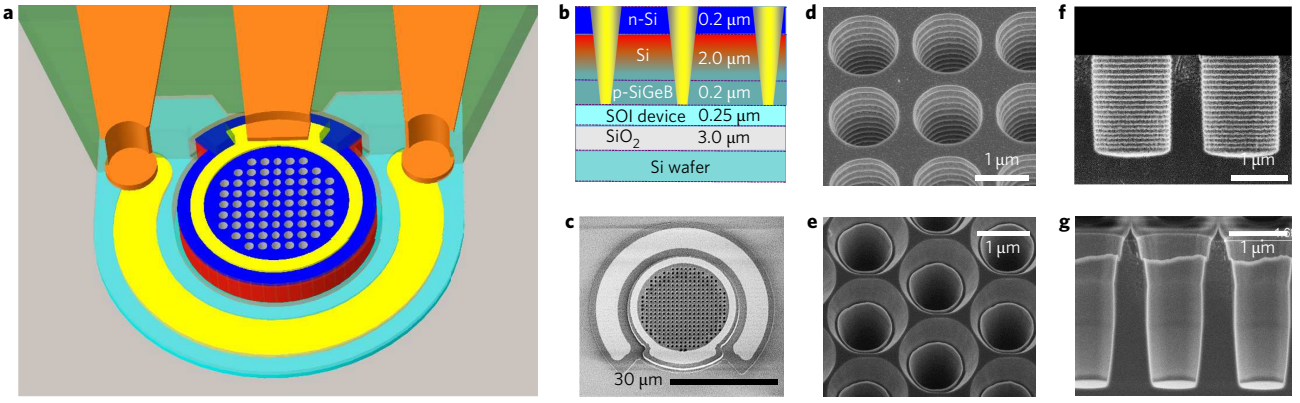

Figure 1 | Silicon photodiode with integrated micro- and nanoscale holes. a, Schematic of the ultrafast photodiode with a thin absorbing region. Colour coded layers: blue, n-Si layer; red, i-Si layer; turquoise, p-Si layer; transparent, insulating nitride/oxide layer; yellow, ohmic contact metal; brown, high-speed coplanar waveguide (CPW); green, polyimide planarization layer. **b**, The n–i–p photodiode structure on an SOI wafer, showing the integrated tapered holes that span the n, i and p layers. **c**, Scanning electron micrograph of the active region of a high-speed photodiode (30 μm diameter). **d**,**e**, Square (**d**) and hexagonal (**e**) hole lattice integrated in the photodiodes. **f**,**g**, Cross-sections of cylindrical (**f**) and funnel-shaped or tapered (**g**) holes etched into the active photodiode regions.

IC fabrication processes that enable its integration with electronic amplifiers and other IC elements. By using micro- and nanostructured holes for efficient light trapping[24–34] in high-speed p–i–n photodiodes, we demonstrate an increased effective absorption coefficient or, equivalently, an enhanced effective optical path for absorption by more than an order of magnitude, resulting in enhanced EQEs of 52% at 850 nm and 62% at 800 nm in less than 2 μm of i-layer and a data rate of more than 20 Gb s^{-1}.

Design and simulations

Silicon IC-compatible photodiode design. Conventional top-illuminated datacom photodiodes used in 850 nm optical transceivers are made of GaAs/AlGaAs on a semi-insulating GaAs substrate, with a p–i–n mesa structure where the i-layer is GaAs with a thickness of ~1.8 μm. The p and n layers are composed of AlGaAs and are transparent to the datacom wavelengths (840–860 nm) for distances <300 m using multimode optical fibre and a multimode, directly modulated GaAs/AlGaAs vertical cavity surface-emitting laser (VCSEL) as the optical transmitter. The GaAs photodiode chip is typically attached to a ceramic multichip carrier that also includes a Si electronic chip with a TIA. Our all-silicon photodiodes were designed and fabricated using IC-compatible processes to facilitate very-large-scale integration (VLSI) and to leverage the cost reduction enabled by the CMOS industry[35,36]. The devices comprise an n–i–p mesa structure on top of a silicon-on-insulator (SOI) wafer, over a 3 μm SiO_2 layer. Micro- and nanoscale holes (diameters ranging from 600 to 1,700 nm and periods from 900 to 2,000 nm) were etched through the mesa to a depth sufficient to reach the bottom p layer (Fig. 1). The detailed fabrication schematic diagram is described in Supplementary Fig. 1. Holes were etched into the active region of the photodiode as square or hexagonal lattices, and were fabricated either as uniform cylindrical shapes or gradual funnel shapes with tapered sidewalls (~65°), as shown in Fig. 1d,e. The different etching schemes used to create the cylindrical and funnel-shaped holes are described in Supplementary Table 2 and Supplementary Figs 2 and 3.

The photodiode structure was grown epitaxially on an SOI substrate with a 0.25 μm device layer (p-Si) (Fig. 1b). The thin absorption region was designed to comprise a 2-μm-thick i-Si layer to minimize the transit time for electrons and holes. Lattice-matched 0.2 μm p^{++}-$Si_{0.988}Ge_{0.01}B_{0.002}$ was used as the bottom p-contact layer, and an etch-stop layer was used for the n-mesa isolation step. A 0.3 μm P-doped n^{++} thin layer served as the top n-ohmic contact. High doping decreases the minority carrier lifetime and minimizes the diffusion of photocarriers generated in the n and p layers into the high field i-region, as well as reducing the series resistance. The structure was optimized for top illumination by multimode optical fibre.

Simulation of lateral propagating modes for enhanced photon absorption. To address the weak absorption in Si, researchers have investigated several wide-spectral photon-trapping schemes for a variety of applications, including photovoltaic (PV) devices[28–34,37]. Such schemes include the formation of micro- and nanowires[27,31,38], nanocones[26], nanoholes[33], photonic crystals[29,39] and graded-index multilayer films, which exhibited efficient absorption by trapping the photons and thereby enhancing the absorption, possibly with the generation of lateral modes at near-infrared (NIR) wavelengths where the absorption coefficient is below 1,000 cm^{-1}. Recently, based on a similar approach, near-unity absorption was demonstrated for solar cells with an absorption thickness of ~10 μm (ref. 24).

The designed photodiodes have two-dimensional periodic holes, whose cross-sections are in the x–y plane and axes are in the z direction, as shown in Fig. 2. The hole array supports a set of modes with wavevectors in the z direction (k_z) and with wavevectors k_c in the x–y plane. Depending on the parameters of the array, collective modes are formed, similar to the modes in photonic crystals[29]. The analysis of photonic crystals reveals that, with particular parameters, slow modes can appear[40]. Several researchers have shown that slow modes can contribute to the achievement of considerably higher absorption[30].

If k_c in the x–y plane of the collective modes in the two-dimensional periodic micro- and nanoscale holes array is small and the wave mainly propagates in the vertical (z) direction, the enhancement of absorption is associated only with resonance in the slab, due to reflection from the bottom. However, resonant photodetectors would have a sharp spectral response, making them unsuitable for most communications applications. Lateral modes with larger k_c can have full reflection from the bottom of the photodiode. The longer they propagate into the i-region, the better the absorption for a wider range of wavelength. The photodiode diameter in the x–y plane is much larger than the thickness of the i-region, and the modes in the x–y plane are absorbed almost completely, in contrast to modes propagating in the z direction. At the same time,

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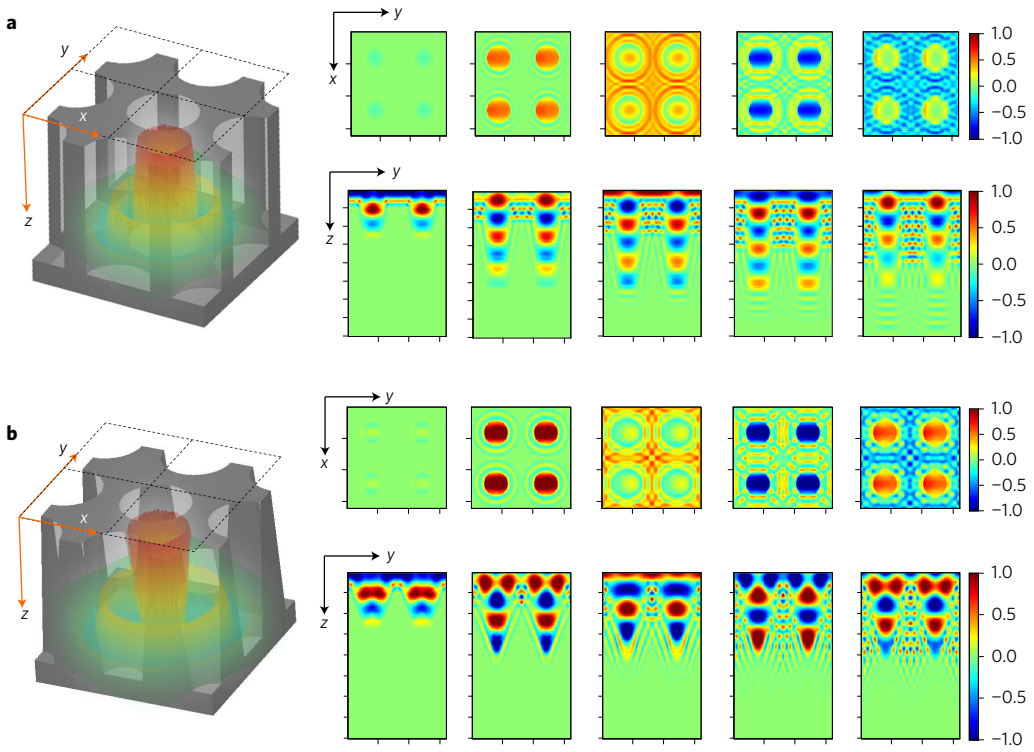

Figure 2 | Slow light in the micro- and nanoscale holes when illuminated by a normal incident beam of light. FDTD numerical simulations show the formation of lateral modes around holes. **a**,**b**, E_x component of the field in the square lattice of cylindrical holes (**a**) and funnel-shaped holes (**b**), with time increasing from left to right. Top row: *x*–*y* plane. Bottom row: *y*–*z* plane. Light illuminates the holes in the *z* direction. Time from left to right: $t = 1.4$, 6.2, 11, 16 and 21 fs. The field first goes into the hole and then spreads laterally into the Si as cylindrical waves. See Supplementary Movies for details of lateral field propagation and the direction of the Poynting vector around the holes in the *x*–*y* and *y*–*z* planes for both cylindrical and funnel-shaped holes. The simulations take into account the absorption of Si.

photocurrent generated in the i-region flows in the *z* direction, allowing us to achieve high-speed characteristics because of its small thickness. The effect is similar to the Lambertian reflector, which helps to trap light in Si (ref. 28). The Lambertian limit for the enhanced absorption length is $4n^2L$, where n is the refractive index of Si and L is the absorption length. The limit can be exceeded for micro- and nanoscale holes if most of the light modes supported by the hole structure are trapped in the x and y directions until they are completely absorbed.

Recent reports on solar cell applications have discussed the extension of the absorption spectrum to 800–950 nm with an array of holes with period (p) smaller than 800 nm (refs 34,37). It has been shown previously that, when $p < \lambda$, the array can support fundamental modes with $k_c = 0$, channelling modes that are travelling through the holes and guided resonance modes that exist in the high-index air–Si hole region between the air and the substrate. The cutoffs for guided and channelling modes were found assuming an effective medium with $p \ll \lambda$, when Maxwell–Garnett theory is valid[34]. Because our focus is on photodiode optimization for wavelengths around 850 nm, we analysed the modes for $p > \lambda$. We found that there are modes with $k_z < k_c$ that leak from the holes into the Si, forming lateral collective modes that could be entirely absorbed in the Si. As a result, holes with periods larger than 900 nm could provide better absorption with much smaller Fabry–Pérot features in the 800–900 nm range, because most of the incident light flux excites modes that are propagating and/or stationary in the lateral plane. Thus, we achieve a successful conversion of an initial incident vertical plane wave to an ensemble of lateral collective modes, realized in a two-dimensional periodic array of holes.

Figure 2a shows holes in square lattice formation illuminated with a vertical plane wave that generates laterally propagating modes. The initial transient time evolution from $t = 0$ to 21 fs is depicted in the figure for the two-dimensional periodic boundary condition. The simulation includes the SOI bottom layer and was carried out for several wavelengths in the range 800–950 nm, taking into account the absorption of Si at this wavelength range. This is the result of finite-difference time-domain (FDTD) simulations, which show the lateral waves appearing around the holes and forming the collective lateral modes over time. These basic features were the same for different wavelengths (only the simulations for 850 nm are shown in Fig. 2).

FDTD simulation results for tapered or funnel-shaped holes are shown in Fig. 2b for a wavelength of 850 nm. The size, depth and shape of the holes can have an influence on the initial generation of lateral modes and the intensity distribution between the n, i and p regions. Light can be trapped between the top and bottom boundaries of the hollow holes if the relationship between k_z and k_c satisfies the condition for full reflection. The lateral waves start to form in the *x*–*y* plane and are trapped in the Si. Animations of field propagation over time around the holes in the *x*–*y* and *y*–*z* planes for cylindrical and funnel-shaped holes are shown in Supplementary Movies 1–4. The Poynting vector was also calculated and is shown in Supplementary Movies 5 and 6. The Poynting vector is directed from the holes into the Si, which means that the energy comes from the holes and propagates in the lateral (in-plane) direction in Si, where it is absorbed.

The funnel-shaped holes offer several advantages over cylindrical holes. Tapered pillars with sidewalls have already been shown to have superior absorption compared to cylindrical pillars[41]. The

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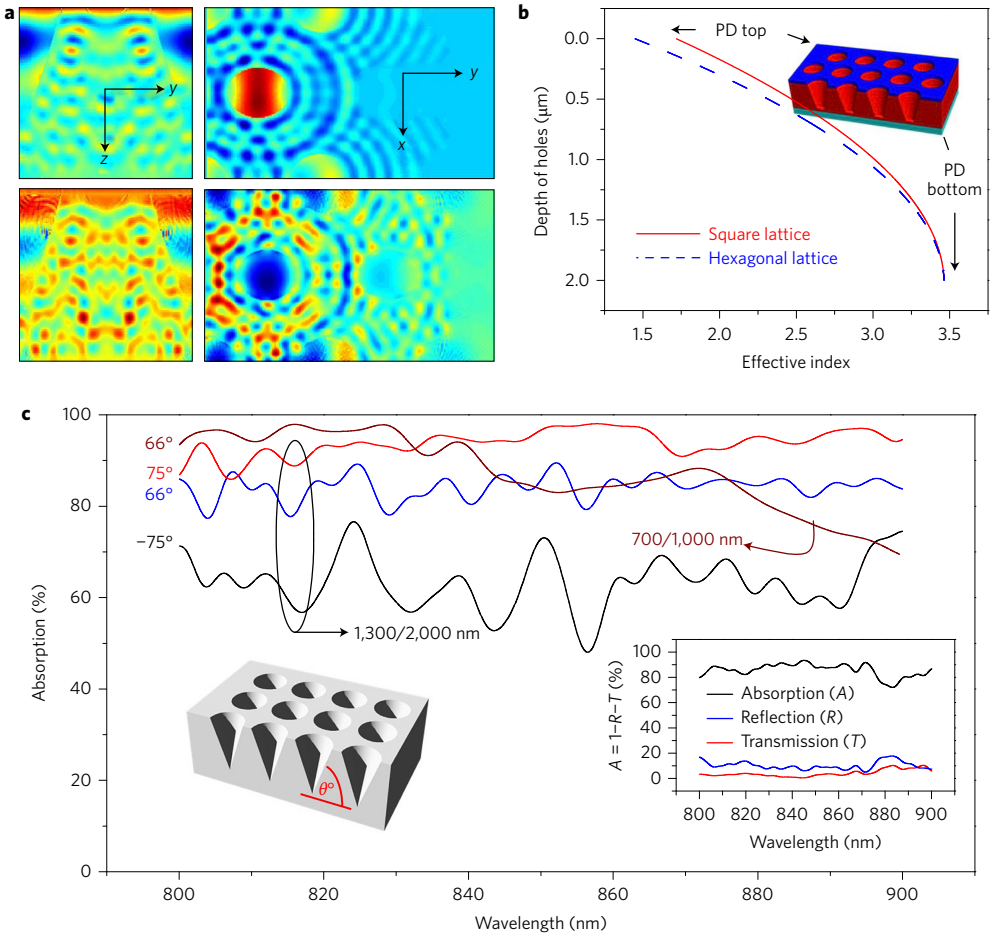

Figure 3 | Slow slight contributing to high efficiency. a, Lateral field propagation in the *y*–*z* plane (left column) and *x*–*y* plane (right column). Time increases from top to bottom. For simulations, only the centre hole was illuminated and the figure depicts the lateral wave propagating from left to right. **b**, Effective refractive index versus distance from the top to the bottom of the funnel-shaped holes, showing a gradually increasing effective index. **c**, Absorption (1–*R*–*T*) in a p–i–n stack that includes p and n contact layers as well as the absorbing i-Si layer with funnel-shaped holes (1,300 nm diameter, 2,000 nm period) with angles of 75°, 66° and −75° (for −75°, holes are wider at the bottom). A single absorption curve for 700-nm-diameter, 66° funnel-shaped holes with 1,000 nm period is also presented. Inset: individual components—absorption (*A*), reflection (*R*) and transmission (*T*)—for a cylindrical hole array in a p–i–n stack. PD, photodiode.

numerical FDTD simulation (Fig. 2b) for the square lattice shows the modes that are leaking from the holes into Si. The absorption spectrum of the funnel-shaped hole is also less sensitive to wavelength. FDTD simulations confirm that the modes in the *x*–*y* directions are much stronger for the funnel-shaped holes, and the absorption versus wavelength dependence is more uniform than for cylindrical holes. Funnel-shaped holes also experience smaller reflection. When one of the dimensions of the micro- or nanostructure—diameter of the holes *d* and/or spacing between adjacent holes (*p*–*d*)—is less than the wavelength λ (*p* is the period), the effective refractive index gradually changes from the surface through the Si, in contrast to the cylindrical holes, where there is an abrupt change. Thus, the funnel-shaped holes create an effect similar to a graded-refractive-index antireflection (AR) coating[42], with smaller refraction.

Figure 3a shows the propagation of lateral modes in an area that was not illuminated. Light absorption in Si is expressed using a complex dielectric permittivity based on the Lorentz model with the parameters that fit crystalline Si at wavelengths of 800–900 nm. The simulations used the perfectly matched layer (PML) boundary conditions in the lateral directions. Only the leftmost column of funnel-shaped holes was illuminated, and it can be seen that the lateral modes propagate into the non-illuminated area, with amplitude decreasing with distance due to the cylindrical geometry of the modes and due to absorptions in the Si. A plot of effective index versus distance from the top is shown in Fig. 3b for funnel-shaped holes with a diameter of 1,500 nm at the top, a lattice period of 2,000 nm and a taper angle of 66°. Funnel-shaped holes provide better coupling into the lateral modes than the cylindrical holes, thus resulting in smaller reflection.

The photodiodes were then simulated numerically using FDTD to examine absorption for the wavelength range 800–900 nm for the following diameters and periods (*d*/*p*): 1,300/2,000 nm, 1,500/2,000 nm, 700/1,000 nm and 630/900 nm. Most of the field intensity is trapped in the slab, and one can calculate the trapped light in the photodiodes by subtracting the reflected (*R*) and transmitted (*T*) components from the total intensity. The results of the FDTD numerical simulations are shown in Fig. 3c for a hexagonal lattice with cylindrical (inset) and funnel-shaped holes (*d*/*p*: 1,300/2,000 nm and 700/1,000 nm) with different sidewall angles (75°, 66°, −75°) in an n–i–p structure with a 2-μm-thick depletion region. The simulation results suggest that a positive sidewall angle is advantageous over a negative sidewall angle where the bottom diameter is larger than the top diameter of the holes. In

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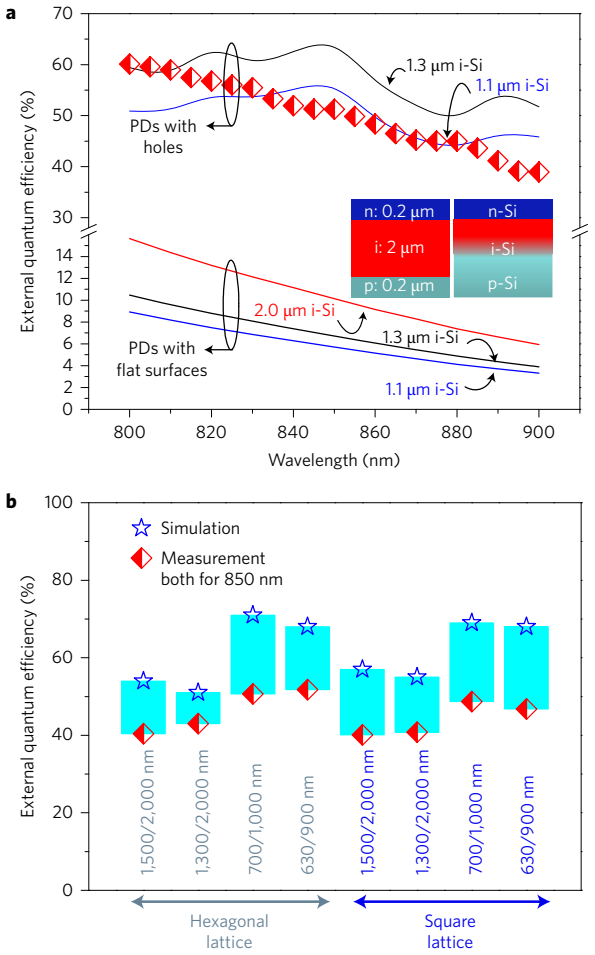

Figure 4 | Enhanced quantum efficiency enabled by integrated holes. **a**, EQE versus wavelengths for photodiodes (PDs) with holes with diameter/period (d/p) of 700 nm/1,000 nm (half-filled red diamonds). The EQE was above 62% at 800 nm and 52% at 850 nm. The simulation results (black and blue lines, top) show that photodiodes with holes have a 1.1–1.3 μm i-Si layer, although the designed thickness was 2 μm. Inset: schematics of dopant diffusion from the p-layer to the i-layer, reducing the thickness of the i-layer. Between six and ten times higher broadband EQE values were observed than in devices without holes and with similar i-layer thickness (black and blue lines, bottom). **b**, Comparison of simulated (considering a 2 μm i-Si layer) and measured EQEs of devices with tapered holes at various d/p at 850 nm. A 2 μm absorbing i-Si layer is estimated to offer >70% efficiency.

addition, the FDTD simulation results presented in Fig. 3c show that photodiodes with tapered holes confine light more efficiently than photodiodes with cylindrical holes (inset).

Results

Demonstration of enhanced EQE and photodiode performance. Micro- and nanoscale hole-integrated photodiodes with lateral propagating modes experience enhanced photon–matter interactions and offer the potential for higher absorption efficiency than that of bulk Si. Figure 4a shows EQE values measured for devices with tapered holes (700 nm in diameter and 1,000 nm period, half-filled red diamonds) at 66° sidewalls. The simulated absorption ($1-R-T$) values depicted in Fig. 3c were compared with the experimentally observed EQE values, and the measured EQE values were conspicuously lower than the simulated values of absorption. For example, although the simulation predicted a peak absorption above 80% for $\lambda = 800$–900 nm (Fig. 3c), the measured maximum EQE was around 62% at 800 nm and 52% at 850 nm (Fig. 4a).

The discrepancy between the experimental results and simulation originates primarily from B diffusion into the i-Si region, which reduces the i-region by more than half in terms of thickness, negatively impacting the collection efficiency of a large fraction of the photogenerated carriers. As will be discussed later, capacitance–voltage (C–V) measurements show a severely reduced i-layer thickness of 0.93 μm (the designed thickness was 2 μm). If we calculate the enhanced absorption coefficient ($\alpha_{\text{effective}}$), assuming an i-layer thickness of ~1 μm for our hole-based photodiode with a measured EQE of 62% at 800 nm, $\alpha_{\text{effective}}$ is found to be ~9,670 cm^{-1}, more than 10 times higher than the α for bulk Si at 800 nm (850 cm^{-1}).

Although incident photons are absorbed everywhere, a fraction of the photons trapped in the photodiodes do not contribute to the device photocurrent. In particular, most of the photons absorbed in the n and p regions of the photodiodes do not contribute to the photocurrents or EQE, due to a lack of electric field in the doped p–n contact regions. A small fraction of photogenerated carriers in the photodiode contact regions are collected via the carrier diffusion process and contribute to the overall EQE. This is how photocurrent generated outside the i-Si region (0.93 μm) defined by our C–V measurements also contributes to the measured EQE. To understand our measured EQE and to extrapolate the effective absorption coefficient in a photodiode with integrated holes, the simulation thus needs to consider an absorption layer thickness larger than 0.93 μm, but smaller than 2 μm. Taking this into account, the simulated absorption ($1-R-T$) values in Fig. 3c were recalculated for an absorption layer with a thickness of ~1.1–1.3 μm for several wavelengths around 850 nm. The black and blue solid lines in Fig. 4a represent absorption taking place only in the i-layer (thickness of 1.3 and 1.1 μm, respectively), where the top two curves are for photodiodes with holes and the bottom two curves are for photodiodes without holes. Our measured values of EQE are closely represented by an absorption layer with thickness between 1.1 and 1.3 μm. The slight discrepancy between the measured and simulated EQE values is caused by process-induced variations in hole depths, diameters, sidewall roughness and taper angle.

The results presented in Fig. 4a for an active photodiode region with integrated holes (d/p: 700/1,000 nm) represent an effective absorption length equivalent to more than 13 times that of the absorption possible in bulk Si. In other words, at $\lambda = 850$ nm, one needs a more than 13 times thicker i-Si region to achieve the same magnitude of absorption with a flat Si thin film than in a Si film of the same thickness that has integrated absorption-enhancement micro- and nanostructures. Such enhancement of absorption enabled by integrated holes contributes to EQE values above 60% (Fig. 4a) at 800 nm. At the datacom wavelength ($\lambda = 850$ nm), a Si photodiode with a flat surface designed with an i-layer thickness of 1.3 μm will exhibit an EQE of only ~6%, assuming all photons impinge on the i-layer and a perfect AR coating is used. In contrast, photodiodes with integrated holes exhibited >52% EQE at 850 nm in our experiments. A similar significant enhancement—close to an order of magnitude higher EQE—was observed in a wide spectral range from 800 to 900 nm, as shown in Fig. 4a. Supplementary Fig. 9 shows broadband EQE values for photodiodes with holes with different d/p and lattice structures. Figure 4a also shows that even an ideal flat photodiode with 2 μm i-layer thickness and a perfect AR coating performs at least four times worse in terms of efficiency than a hole-integrated photodiode with ~1 μm i-layer thickness. To investigate whether temperature variations could impact the absorption characteristics of the photodiodes, we also simulated the absorption of the photodiodes between −40 and 80 °C, and found it to vary by less than 10%, as shown in Supplementary Fig. 7. There was less than 3% polarization dependence in the photocurrent.

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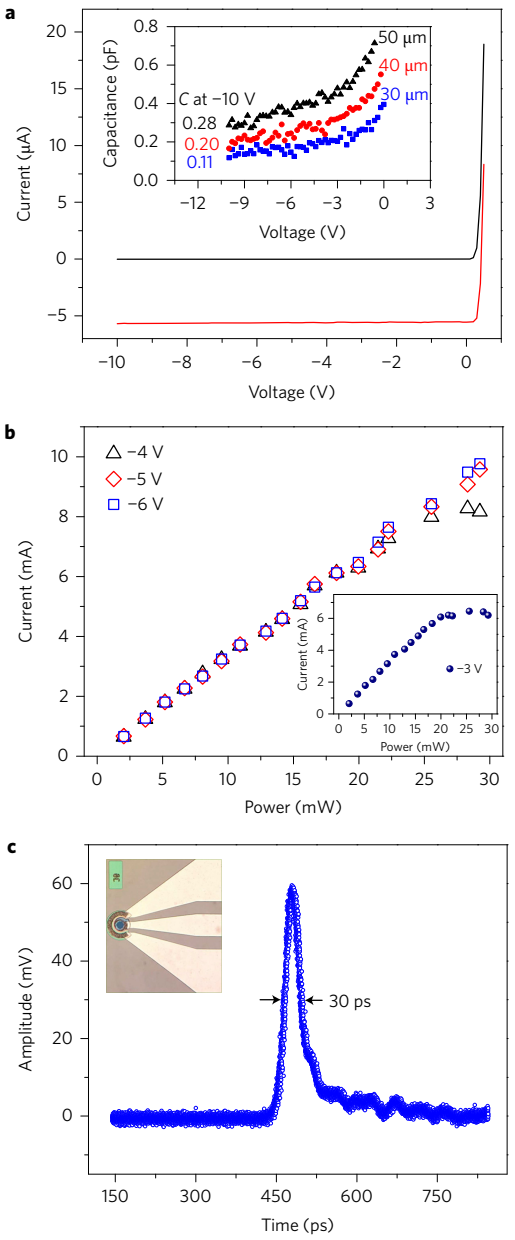

Figure 5 | d.c. and ultrafast characteristics of the photodiodes. a, Current–voltage (*I–V*) characteristics of a PD in dark and under illumination. Dark current of a device with a diameter of 30 μm is 0.06 nA. Inset: capacitance–voltage (*C–V*) characteristics of PDs of different sizes with no holes, indicating 0.93 μm i-Si layer thickness (Supplementary Fig. 8), although the device was designed with a thickness of 2 μm i-Si. P-doping (boron) diffusion from the bottom p-Si layer to the i-Si layer contributed to a reduction in the thickness of the i-Si layer. **b**, Lateral light propagation keeps the power per volume at a low level and contributes to high linear photocurrent. Inset: at −3 V bias, the PDs remain linear up to 20 mW input power. **c**, By illuminating a PD with a subpicosecond pulse, a 30 ps FWHM response was observed by a 20-GHz oscilloscope. When corrected for the oscilloscope bandwidth and laser pulse width, the device temporal response is estimated to be 23 ps at 850 nm. Inset: optical micrograph of a 30 μm PD with a CPW.

To accurately estimate the potential EQE for a photodiode with 2 μm i-layer thickness, the simulated EQE of the p–i–n structure was corrected to a reduced value by subtracting the contributions of the lateral modes that are trapped and absorbed in the n and p regions of the structures. Most of the photocarriers generated in such doped regions do not experience a drift field and thus do not contribute to the photocurrent. Figure 4b shows simulated EQEs for tapered holes of varying *d*/*p* illuminated with light at 850 nm wavelength. For comparison, measured EQEs from photodiodes with integrated holes and corresponding dimensions are also presented in Fig. 4b. The shaded bar shows the difference between currently measured EQEs and potentially achievable EQEs with a 2 μm i-layer and abrupt p–i and i–n interfaces.

The imperfections of the fabrication processes that contributed to the variations in sidewall angle, deviation from the ideal smooth sidewalls (Fig. 1d–g) and reactive ion etch (RIE)-induced surface roughness and damage, which result in traps and higher recombination rates, are also causes of lower than expected EQEs. Even with such limitations in the materials and fabrication processes for the devices, with a reduced i-layer that resulted in an EQE of 52% at 850 nm, an EQE of 70% or more can be achieved with an i-layer of 2 μm. We also designed large test devices to characterize their PV efficiency, and measured more than 7.3% energy conversion efficiency. This efficiency is more than 30% higher than that of devices designed without integrated holes (Supplementary Table 4).

The photodiodes were biased at varying voltages and were found to show a flat EQE above 2.0 V bias (Fig. 5a). The dark current of a device with a diameter of 30 μm at −5 V bias was 0.06 nA (Supplementary Fig. 8a). As is shown in the inset of Fig. 5a, the measured capacitance of a photodiode of 30 μm diameter (with no holes) is 110 fF, but it is expected to be 36 fF for a 2-μm-thick i-layer. Repeated measurements on a number of devices with different sizes and shapes resulted in an i-Si layer thickness of less than 1 μm (0.93 μm), as depicted in Supplementary Fig. 8. We believe this reduction of the intrinsic layer was caused by the diffusion of impurities from the bottom p-contact layer to the i-Si layer during the epitaxial growth process. Secondary ion mass spectrometry (SIMS) characterization shows more than 1 μm of B diffusion into the i-Si layer from the bottom p-Si layer, which was epitaxially grown with a doping concentration of 10^{20} cm^{-3}. A design with p-Si as the top contact layer and choosing a larger n-dopant atom such as As, which has a reduced diffusion coefficient, can inhibit the dopant diffusion issue and address the discrepancy in the measured and simulated EQE.

A high density of photon-trapping structures (such as cylindrical and tapered hole patterns) generated on photodiode surfaces using RIE causes the devices to experience increased crystalline defects such as vacancies, interstitials, dislocations or stacking faults, surface roughness, impurities and device charging. All these defects contribute to undesirable surface states, traps and recombination sites, which degrade the device characteristics and impact detection sensitivity and energy conversion efficiency. The surface states in nanoscale photodiodes can cause persistent photocurrent[43], contributing to noise and possible signal distortion during high-speed operations. As described in Supplementary Section VI, we applied several possible methods to inhibit device degradation induced by surface damage, including thermal oxidation and oxide removal, low ion energy etch, solution-based hydrogen passivation (Supplementary Table 3) and the growth of a nanoscale thin passivating oxide film via a rapid thermal oxidation (RTO) process. Hydrogen passivation helped to suppress leakage current (Supplementary Fig. 10) in devices that were freshly etched, and allowed efficient carrier collection even with a low electrical field (Supplementary Fig. 11). Thermal oxidation and hydrogen passivation reduced the leakage current to the nA level, even in large devices (500 μm in diameter), but the leakage current was on the scale of μA after low ion energy etch. However, wet oxidation caused a decrease in the EQE of hole-integrated photodiodes due to additional dopant diffusion (Supplementary Fig. 12).

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In datacom and computer networks, the link length is between 100 m at 25 Gb s^{-1} and 300 m at 10 Gb s^{-1} (ref. 23) and the photodiodes may need to absorb at higher power than is typically used in communication links[4]. A thin absorption region can limit the maximum power-handling capability of a photodiode, contributing to some nonlinearities in the currents. Nonlinearity is caused by a decrease in the electric field under intense illumination, which lowers the carrier velocity and decreases the width of the depletion region due to a space-charge effect or electric-field screening[44,45]. This may degrade the signal-to-noise ratio, especially in the newly proposed four-level pulse-amplitude modulation (PAM-4) systems[46]. Due to effective light propagation parallel to the direction of the photodiode surface, the power per unit volume remains at a low level in our photodiodes, contributing to high linearity. Even with an absorption layer (~1 μm) thinner than the designed thickness (2 μm), the devices were found to remain linear for a d.c. current as high as ~10 mA when biased above 5 V (Fig. 5b).

Ultrafast photodiode response. For the high-speed characterizations we used a mode-locked pulsed fibre laser with a wavelength of 850 nm, a total output average power of 1 mW, a subpicosecond pulse width and a repetition rate of 20 MHz. The incident power on the photodiodes during a.c. measurements was kept at ~100 μW. The pulse spectral width was 10–20 nm. For a 2 m fibre with dispersion of 120 ps km^{-1} nm^{-1}, the pulse was broadened by ~0.5 ps. The laser pulse was focused onto the active region of the photodiodes using a single-mode lensed fibre tip on a microwave probe station. The centre of the laser beam was aligned with a translational stage to maximize the photocurrent of a device with a diameter of 30 μm. The resulting photoresponse in the form of electrical pulses was observed on a sampling oscilloscope with a 20 GHz electrical sampling module. Figure 5c shows the measured pulse response when the device was biased above 3 V using a 25 GHz bias-T. The measured FWHM from the oscilloscope was 30 ps. Considering the 20 ps FWHM response for the 20 GHz sampling oscilloscope and the optical laser pulse width of <1 ps, the actual response of the device was estimated to be 23 ps at 850 nm, based on equation (1)[47]:

$$\tau_{\mathrm{meas}} = \sqrt{\tau_{\mathrm{actual}}^2 + \tau_{\mathrm{scope}}^2 + \tau_{\mathrm{optical}}^2} \quad (1)$$

where τ_{meas}, τ_{actual}, τ_{scope} and τ_{optical} are the measured, actual, oscilloscope and laser optical pulse widths in the time domain. This is acceptable for Gaussian pulses and is a valid approximation for our actual measurements. This is the fastest reported response for a silicon photodetector with such wide-spectral high quantum efficiency. The performance corresponds to a data transmission rate of 20 Gb s^{-1} or higher. There is a residual photocurrent tail after the pulse fall time due to slow diffusion of photogenerated minority carriers in the p and n layers where the doping profile is soft and not abrupt with the i-layer due to dopant diffusion of B and P during epitaxial growth. The slow diffusion tail can be minimized by growing more abrupt p–i and i–n interfaces. Based on the measured high-speed performance and EQE, it is possible to design Si photodiodes with >30 GHz bandwidth and 40% efficiency, as elaborated in Supplementary Fig. 13.

Conclusions

We have demonstrated a normal incident Si photodiode with a deconvolved temporal impulse response of 23 ps (FWHM), corresponding to a data transmission rate of 20 Gb s^{-1} or higher. The device exhibits more than 50% quantum efficiency for 820–860 nm wavelengths. This is the fastest reported response for a Si photodiode with such high quantum efficiency. Our work reveals that an optical beam normally incident on a Si photodiode integrated with periodic photon-trapping micro- and nanoholes can generate lateral propagating slow and stationary optical modes that provide greater interaction of light with Si, in terms of both duration and length. Such modes of propagation increase the effective optical absorption coefficient by more than an order of magnitude in a thin Si layer while ensuring an ultrafast transit time for the carriers. This enables the development of efficient high-speed Si photodiodes suitable for monolithic integration with CMOS electronics for the short-reach multimode optical data links used in datacom and computer networks. Such an all-Si optical receiver offers great potential to reduce the cost of short-reach, <300 m optical data links in data centres where these links are most abundant and where it is most cost- and performance-sensitive.

Methods

Methods and any associated references are available in the online version of the paper.

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Author contributions

E.P.D., T.Y., A.F.E. and S.G. simulated the photodiode structures. M.S.I., H.H.M., Y.G., H.C. and S.-Y.W. designed the photodiodes. Y.G., H.C., K.G.P. and H.H.M. fabricated the devices. H.C., S.G., A.K., A.S.M., Y.W. and X.Z. carried out the d.c. and high-speed characterization of the photodiodes. Y.G., H.C., S.G., A.F.E., T.Y. and A.K. discussed the processing and characterization results and analysed the data. Y.G., H.C., S.-Y.W. and M.S.I. drafted the manuscript. S.-Y.W., T.Y., E.P.D., A.F.E. and M.S.I. revised the manuscript. S.-Y.W. and M.S.I. co-supervised the research.

Additional information

Supplementary information is available in the online version of the paper. Reprints and permissions information is available online at www.nature.com/reprints. Publisher's note: Springer Nature remains neutral with regard to jurisdictional claims in published maps and institutional affiliations. Correspondence and requests for materials should be addressed to M.S.I.

Competing financial interests

The authors declare no competing financial interests.

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Methods

Device fabrication. Devices were fabricated by etching holes using a deep reactive ion etching (DRIE) or reactive ion etching (RIE) process, followed by n- and p-mesa isolation (Supplementary Fig. 4) and the delineation of coplanar waveguides (CPW, characteristic impedance $Z = 50\ \Omega$) designed for on-wafer high-speed characterization. A dielectric bridge of a 600-nm-thick (150 nm/300 nm/150 nm $Si_3N_4/SiO_2/SiO_2$) insulating layer was deposited via plasma-enhanced chemical vapour deposition at 250 °C onto the entire wafer surface, so that the metal contact to the n layer could cross over the p layer, and later be patterned for subsequent contact metallization. Different passivation methods (Supplementary Table 3 and Supplementary Fig. 5) were carried out to remove the DRIE- and RIE-induced Si surface damage to reduce leakage current. An additional layer of polyimide (thickness of 3 μm) was used to reduce the parasitic capacitance of the large-area CPWs (Supplementary Fig. 6). For more fabrication details, see Supplementary Section II.

EQE measurement. EQE measurements were conducted using a supercontinuum laser (600–1,100 nm) and a tunable filter that transmits a band of wavelengths with 1 nm width blocking the adjacent wavelength. Five discrete fibre-coupled lasers at 780, 800, 826, 848 and 940 nm were also used to deliver light to the devices via a single-mode fibre probe on a probe station. For more details of the EQE measurement set-up and results, see Supplementary Section V.

Data availability. The data that support the plots within this Article and other findings of this study are available from the corresponding author upon request.

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SUPPLEMENTARY INFORMATION

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Photon-trapping microstructures enable high-speed high-efficiency silicon photodiodes

Yang Gao, Hilal Cansizoglu, Kazim G. Polat, Soroush Ghandiparsi, Ahmet Kaya, Hasina H. Mamtaz, Ahmed S. Mayet, Yinan Wang, Xinzhi Zhang, Toshishige Yamada, Ekaterina Ponizovskaya Devine, Aly F. Elrefaie, Shih-Yuan Wang, M. Saif Islam*

*Correspondence to: sislam@ucdavis.edu

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I. Comparison between PDs in literature and the PDs in this work

The performances of PDs in other literature are compared to the PD of this work in Table S1.

Table S1 | Performance comparison between PDs in literature and in this work

Material	Device type	Responsivity (A/W) or EQE	Wavelength (nm)	Bandwidth (GHz) or data rate (Gb/s)	CMOS compatibility and other challenges
Si [S1]	p^+-p-n avalanche	0.74 A/W (at 823 nm)	850	1.6 GHz, 3.5 Gb/s	0.18 μm CMOS technology
Si[S2]	p^+-n-p	N.A.	850	3 Gb/s with an analog equalizer	0.18 μm CMOS technology
Si[S3]	Resonant cavity *pin*	40 % EQE	860	10 Gb/s	Complex cavity mirror fabrication
Si[S4]	Resonant cavity *pin*	40 % EQE	822	10 GHz, >10 Gb/s	Complex cavity mirror fabrication
Si[S5]	MSM	N.A.	850	2.5 GHz	CMOS compatible
Ge on Si[S6]	*pin*	0.9 A/W (at 1310 nm)	800-1360	10 Gb/s	Limited CMOS compatibility
Ge on Si[S6]	APD	N.A.	830-1000	25 Gb/s	Limited CMOS compatibility Hard to couple fiber due to small aperture (20 μm)
Ge on Si[S7]	APD	0.4 A/W	1300	>30 GHz	CMOS compatible expensive packaging for waveguide APD
Ge on Si[S8]	APD	5.88 A/W (at 1310 nm)	1300	>30GHz, and 340GHz GB product	CMOS compatible
Si[S9]	APD	0.07 A/W	850	5 GHz, 12.5 Gb/s with equalizer circuit	0.25 μm Si/Ge BiCMOS technology
Si[S10]	APD	10% EQE	850	8 Gb/s	0.13 μm CMOS technology
Si[S11]	APD (double PD)	0.84 A/W	850	0.7 GHz	40 nm CMOS technology
Si[S12]	Spatially-modulated APD	0.18 A/W	850	8 GHz, 12.5 Gb/s with TIA, equalizer and limiting amplifier	0.13 μm CMOS technology
Si[S13]	APD	4.67 A/W	850	10 Gb/s	0.13 μm CMOS technology
Si[S14]	APD	2.94 A/W	850	3.2 GHz > 1THz GB product	65 nm CMOS technology
Si[S15]	Surface plasmon antenna	0.001% EQE	840	100 GHz (estimation)	Not CMOS compatible
Si [S16]	lateral *pin*	47% internal QE	840	N.A.	CMOS compatible
Si[S17]	lateral *pin*	0.32 A/W (from 4 PDs)	850	10 Gb/s with TIA	0.13 μm CMOS technology
Si (this work)	**vertical *pin***	**52% EQE at 850 nm**	**broadband absorption between 800-900 nm**	**>20 Gb/s**	**CMOS compatible**

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The speed of Si pin PDs available in the market for optical communication applications at 850 nm is not sufficient for the receivers operating at high data rates. However, there are Ge-on-Si pin PDs and avalanche photodiodes (APDs) available for 25 Gb/s operation.[S6] A *Ge-on-Si* APD is reported for 1300 nm operation with a bandwidth above 30 GHz.[S7] On the other hand, Ge-on-Si PDs requires additional epitaxial growth of Ge on Si substrate. However, APDs usually work at a high voltage close to breakdown. Short reach optical links require PDs powered with a DC bias around 3V or less. The high power consumption of APDs compared to their pin counterparts make them unfavorable for short reach optical links. In addition, Si APDs have a higher level of noise than pin PDs.

II. Device Fabrication:

Fig. S1 shows the schematics of fabrication processes of the photon-trapping photodiodes (PDs). There are two types of micro- and nanoholes (cylindrical and tapered) in our PDs, and their fabrication processes are slightly different. In Fig. S1, we only show the schematics of cylindrical holes for simplicity.

1) DUV Photolithography

The starting pin SOI wafer was pre-cleaned in piranha solution to remove any organic contaminants. Then, the wafer was spin coated with bottom anti-reflective coating (BARC) layer and deep ultraviolet (DUV) resist. BARC is used to absorb light and has little reflection at the resist and BARC interface, thus improves the resolution of the patterned resist. Subsequently, the holes pattern was generated by DUV photolithography. It required different DUV resist coating thicknesses as well as different exposure doses for tapered and cylindrical holes fabrication, as shown in Table S2.

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Table S2 | Comparison between cylindrical and tapered hole etching schemes.

Hole type	DUV resist coating thickness (μm)	DUV exposure dose (mJ/cm^2)	Etching method
Cylindrical	0.4	18	DRIE
Tapered	1.7	45	Two step RIE

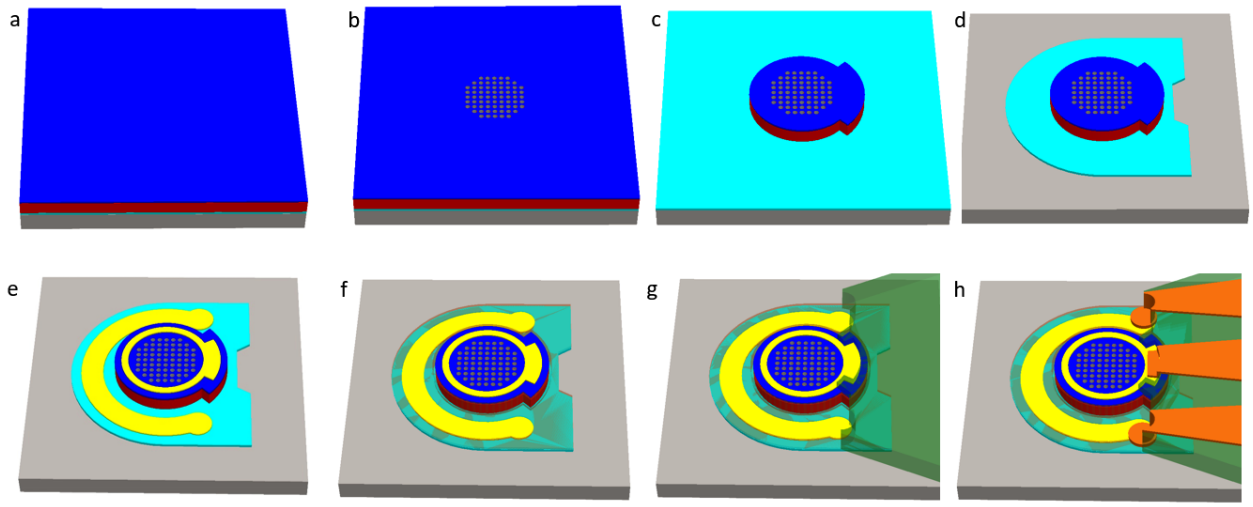

Figure S1 | Schematic diagram of fabricating the photon trapping PDs. a, Starting wafer (gray: SOI wafer substrate; turquoise: *p*-type layer, composed of 0.2 μm of SiGeB and 0.25 μm *p*-Si SOI device layer; red: 2 μm *i*-Si layer; blue: 0.2 μm *n*-Si layer). **b,** DUV photolithography and holes etch to create tapered or cylindrical holes with diameters ranging from 600 to 1500 nm in a square (shown here) or hexagonal (not shown here) lattice. **c,** *N*-mesa etch to *p*-Si layer. **d,** *P*-mesa etch to the substrate layer. **e,** Ohmic metal deposition (100 nm Al, 20 nm Pt) followed by HF dip passivation. **f,** Sandwiched insulation layer (150 nm Si_3N_4/300 nm SiO_2/150 nm Si_3N_4) PECVD deposition to isolate the *n* and *p* mesas. (Semitransparent brownish layer represents this insulation layer on both *n*-mesa sidewall and top surface of *p*-mesa with contacts opening). **g,** Polyimide planarization (semitransparent green color). **h,** Coplanar waveguides (CPWs) metal deposition (brown color).

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2) Holes etch

After the holes were patterned, the wafer was put inside an oven at 120°C to hard bake the DUV resist. Reactive Ion Etch (RIE) or Deep Reactive Ion Etch (DRIE) was used to form tapered or cylindrical holes, respectively, as also shown in Table S2. The schemes of creating such two types of holes are outlined below.

A) <u>Cylindrical holes fabrication scheme</u>

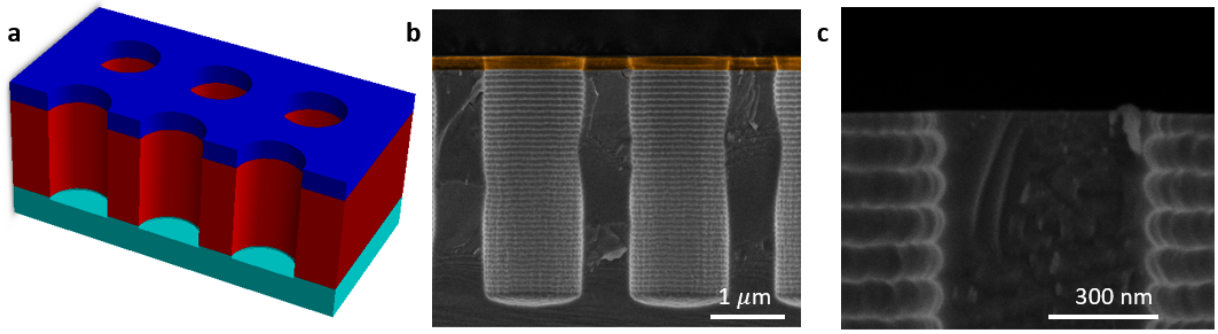

Figure S2 | Cylindrical holes etched in the active region of the PDs. a, Schematic diagram of the cylindrical holes, colored layers represent *n*-Si (blue), *i*-Si (red), *p*-Si (turquoise), respectively. **b,** SEM image of cross-sectional cylindrical holes etched by DRIE, showing holes of 1300 nm in diameter and 2000 nm in period in a square lattice. **c,** SEM image of the cross-section of the cylindrical holes' edge. The scallop on the sidewall is caused by the alternate etching and passivation cycles in DRIE. The size of the scallop is optimized to be around 35 nm.

DRIE is a highly anisotropic etch process used to create high aspect ratio vertical holes, and it utilizes Bosch process which alternates between two modes to achieve holes with almost 90º anisotropic etching [S18]. One mode is isotropic etching of Si by sulfur hexafluoride (SF_6) gas, and the other mode is passivation/deposition by octafluorocyclobutane (C_4F_8) gas to protect the sidewalls. The schematics and actual SEM images of the cylindrical etched holes by DRIE are shown in Fig. S2a and b, respectively. The scalloping caused by the switching cycles of DRIE

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process was minimized to be less than 35 nm to achieve smooth surfaces of the sidewalls as Fig. S2c shows.

B) <u>Tapered holes fabrication scheme</u>

DRIE process usually produces vertical holes, but it can also produce tapered holes with 50º-80º by adjusting the isotropic etching and deposition cycles or simultaneously employing the SF_6 and C_4F_8 gasses with the right ratio [S19-21]. However, the isotropic etch nature of the SF_6 gas in DRIE process results in almost identical lateral etch rate as vertical etch rate and thus produces large undercut beneath the photoresist [S22]. Since the spacing between the holes in our PDs is very small, ranging from 270 to 700 nm, it is not sufficient enough to create tapered etched holes with microns deep by DRIE method. In this paper, RIE process was employed to etch a gradual funnel shaped holes. In our RIE etching system, HBr and Cl_2 gasses were used to etch Si, and it normally produces almost vertical holes with an angle of 83º-87º. To create tapered sidewall profile, one can start with a near vertical hole etch and then convert it into a tapered one after an additional maskless etching step that eroded the silicon structure laterally while etching along the vertical direction [S23]. However, the maskless etch step can also remove very thin top *n*-layer in our PDs. We employed a similar etch scheme as maskless etch to create tapered holes, but with pyramid shaped islands resist profile. Fig. S3a shows the schematics of the tapered holes in our PD device. Due to the high density of the holes in our PD device, the resist between the holes is consumed faster than bulk resist during the RIE process. As Fig. S3b shows, the resist (brown color) in the spacing of the holes formed pyramid shaped islands (~250 nm thick) when the bulk resist remains around 400 nm thick. These pyramid shaped islands enable the lateral etch of the holes and formed a widened opening at the top session with 60º-70º sidewall while the sidewall still keeps a nearly vertical profile at 84º at the bottom. To achieve this tapered structure by this

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etch process, the DUV resist thickness has to be precisely controlled around 1.7 μm, so that the bulk resist was consumed to just around 400 nm when the holes were close to their desired etch depth.

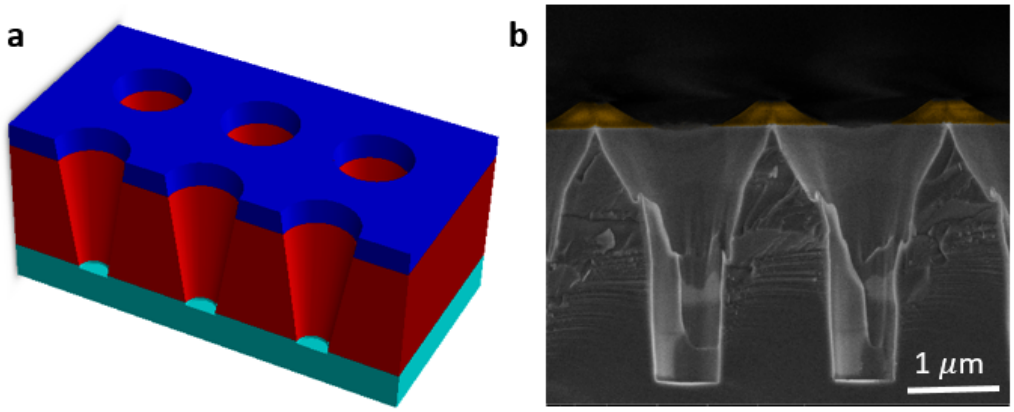

Figure S3 | Tapered holes in PD device. a, Schematic of the tapered holes, colored layers represent *n*-Si (blue), *i*-Si (red), *p*-Si (turquoise), respectively. **b,** SEM image of the cross-section of the tapered holes by two step RIE etch. The resist (brown color) on the spacing of the holes formed pyramid shaped islands of less than 250 nm thick, and thus facilitated the lateral Si etch. The design of the holes is 1500 nm in diameter and 2000 nm in period, and the holes are in a square lattice. The angle of the opening of the holes is around 60°; the angle of the sidewall at the bottom side is around 84°.

3) Mesa Isolation

After holes etch, *n*-mesa was etched into the *p*-Si layer and *p*-mesa was etched to buried oxide (BOX) layer of the SOI wafer by using the DRIE process. The schematics of *n* and *p*-mesas cross section is illustrated in Fig. S4a. The thickness of each *pin* layer is also identified in Fig. S4a. The SEM of an 80 μm PD device after *n*-mesa and *p*-mesa DRIE etch is shown in Fig. S4b.

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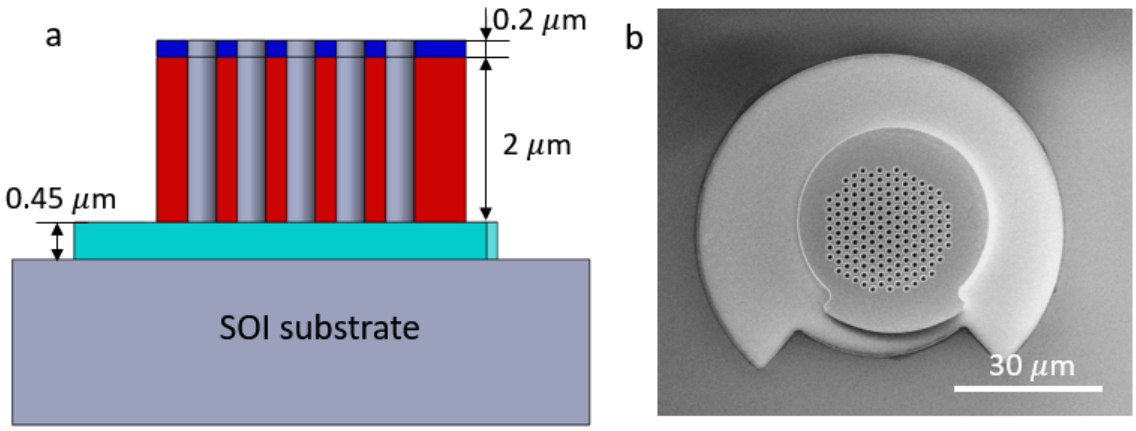

Figure S4 | PD Mesa Isolation. a, Cross-sectional schematics of *n*-mesa and *p*-mesa isolation by DRIE process and the thickness of each layer. Turquoise: *p*-layer, 0.45 μm, composed of 0.25 μm SOI *p*-type device layer and 0.2 μm SiGeB *p*-layer; red: *i*-Si layer, 2 μm; blue: *n*-Si layer, 0.2 μm. **b,** SEM image of an actual 80 μm PD device with holes in hexagonal lattice after *n*- and *p*-mesa isolation process.

4) Dry Etch Damage Removal

Dry etching such as RIE and DRIE, not only uses the chemical effects of the ions and radical species but also relies on the physical effects of the ion bombardment to remove the silicon or other etching targets [S24-27]. Different types of defects can be generated as surface damage after dry etching. These include crystalline defects such as vacancies, interstitials, dislocations, or stacking faults, surface roughness, impurities, and device charging [S28,29]. These defects contribute to undesirable surface states, traps and recombination sites that degrade the device characteristics impacting detection sensitivity and energy conversion efficiency. It is reported that the dry etch induced damaged Si layer can be of 50-150 nm thick [S29,30]. The dry etch induced damage layer can be removed by several methods illustrated in Table S3. Wet etch is usually employed to remove the damaged layer caused by RIE especially for photovoltaic application [S28,30]. However, the Si etch rate of the wet etch is very sensitive to temperature and difficult to control. Thus, the wet etch methods are not used in this paper. Thermal oxidation forces an oxidizing agent, usually

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O_2 or H_2O, to diffuse into the damaged Si surface and react with it at high temperature and convert it into a layer of SiO_2. The SiO_2 surface is hydrophilic and the oxide etchant can easily get inside of the holes to remove the oxide layer. As it can be seen from Fig. S5, around 110 nm of the SiO_2 layer was formed uniformly on the surface and sidewall of the holes via wet oxidation at 900°C, and this oxide layer was successfully removed by a buffered oxide etch (BOE) dip. It is also noted that after BOE dip, the scalloping of the remaining Si surface is decreased from 35 nm to around 10 nm. The surface roughness is greatly reduced by oxidation and subsequent BOE dip method.

Table S3 | Dry etching-induced damage Si layer removal methods

Damage removal method	Description of the method
Wet etch	HNO_3:HF (50:1) [S28,30]; HNO_3:H_2O:NH_4F (126:60:5) (Si isotropic etchant) [S31]
Oxidation	Thermal oxide consumes the damaged Si surface into oxide layer and removed by BOE (H_2O: F (10:1))
Low ion energy etch	Reduce the forward and RF power of RIE system to cause less damage to the Si surface. The etch rate of this etch is extremely small, thus it is preferable to apply this method after each normal RIE or DRIE to remove the 50-100 nm of damaged Si surface
HF passivation	HF dip for 10 s in HF: H_2O (1:10)

Another way to remove the damaged Si surface is via low ion energy etch in RIE system. Low ion energy plasma can be produced by reducing the forward and RF power of RIE system, and a two-step etch (normal RIE etch followed by a low ion energy etch) is proved to be an efficient way to reduce the damage caused by RIE [S29,32]. In this paper, the low ion energy etch was performed in a RIE system via using 3 W RF power instead of 150 W RF power for a normal RIE process. Low ion energy etch is more controllable due to the slower and more repeatable etch rate, and another advantage of this method is that it can perform in situ right after normal RIE process without exposing the wafer to atmosphere.

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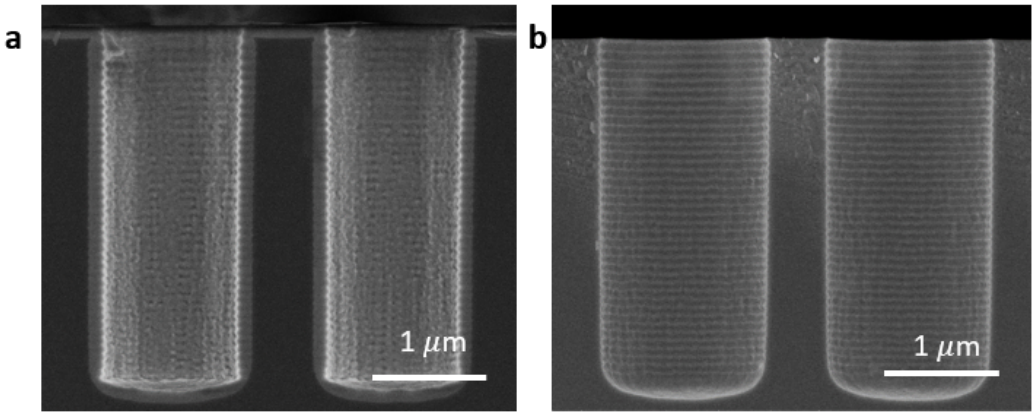

Figure S5 | Oxide passivation for removal of surface damages caused by DRIE. a, Cross-sectional SEM image of the holes of 1300 nm in diameter and 2000 nm in period after thermal oxidation. Uniform and conformal oxide layer of around 110 nm thick is formed on the surface and sidewall. **b,** Cross-sectional SEM image of the holes of 1300 nm in diameter and 2000 nm in period after BOE dip. Oxide layer is removed after BOE dip, and the size of the scallop also reduces to 10 nm.

5) Ohmic metal formation

To ensure minimum contact resistance between the metal and semiconductor junction, ohmic contacts need to be formed. A 2 μm wide ring around the active region (with holes) and 5 μm wide half ring were patterned on *n*-mesa and *p*-mesa, respectively, using S1813 g-line resist photolithography. Then, O_2 plasma was used to clean the Si surface as well as to descum the resist on the sidewall. Another BOE (1:6) dip ensures the native oxide on Si surface is removed upon metal deposition. 100 nm of aluminum (Al) and 20 nm of platinum (Pt) were sputtered accordingly on the whole wafer. Pt was used to protect the Al film during HF dipping for surface passivation purposes. A standard lift-off process was then applied to remove the resist and form the contact patterns. Last, the sample was annealed at 465°C for 20 s in 20:1 N_2: H_2 environment for a rapid thermal process (RTP) to form the ohmic contacts.

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6) Insulating layer deposition, planarization and CPW deposition

A sandwiched insulating layer, composed of 150 nm Si_3N_4/300 nm SiO_2/150 nmSi_3N_4, was deposited by plasma enhanced chemical vapor deposition (PECVD) at 250°C and was subsequently patterned to open the ohmic contact regions to avoid the short between *n* and *p* mesas. The sandwiched layer was used to minimize the pinholes that may exist in a single oxide or nitride layer to enhance the insulating performance. A 3-µm-thick photo-curable polyimide

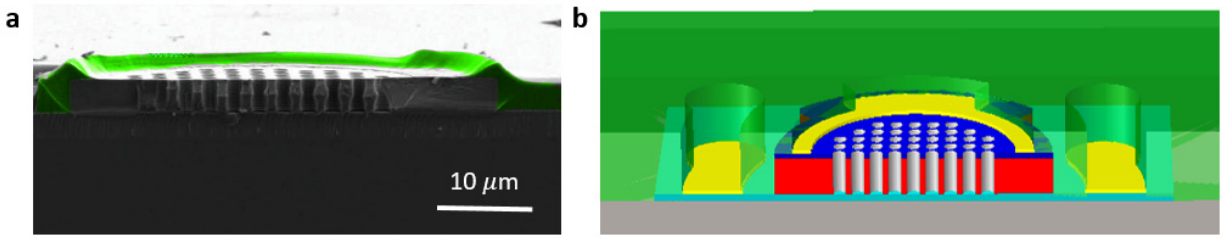

Figure S6 | Polyimide assisted planarization process. a, Cross sectional SEM of a 40 µm device (with cylindrical holes in a square lattice) with patterned polyimide after thermal curing. (Green color represents polyimide). **b,** Cross sectional schematics of a PD after polyimide planarization. Turquoise: *p*-Si layer; red: *i*-Si layer; blue: *n*-Si layer; yellow: ohmic contact metal; green: polyimide; grey: SOI substrate.

layer was then deposited for surface planarization as shown in Fig. S6a. The polyimide layer also serves as a dielectric layer to isolate the *n* and *p* mesas during the subsequent CPW metal deposition in addition to the sandwiched insulating layer as illustrated in Fig. S6b. In addition, the polyimide layer reduces the parasitic capacitance arising from the large metal pads which could limit the response speed of the PD device. After patterning, a polyimide film was cured at 350°C for 30 minutes under N_2 environment in a vacuum oven. After thermal curing, the adhesion of the polyimide film to Si surface was tested with magic tape test. Similar to ohmic contacts process, CPWs were then patterned and Ti/Al/Pt (5/300/20 nm) stack was DC sputtered, followed by a lift-off process. Ti serves as an adhesion layer to the top Pt surface of the ohmic contacts.

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III. Effect of temperature variations on optical absorption of hole based PDs

The reduction of the band gap caused by the effect of temperature would result in the increase of the absorption of Si PD device. However, Finite-Difference Time-Domain (FDTD) simulations showed less than 10% of absorption variation for our PD device with hexagonally packed tapered holes (700 nm in diameter, 1000 nm in period) for the temperature at -40, 20 and 80°C as illustrated in Fig. S7.

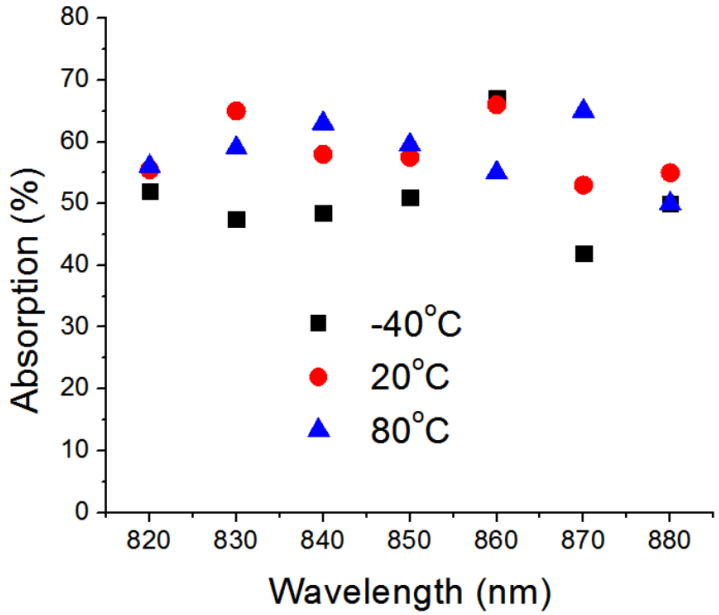

Figure S7 | PD absorption characteristics for wavelengths 820 to 880 nm for the temperature of -40, 20 and 80°C. Simulated PDs have tapered holes (depth: 2000 nm, diameter: 700 nm, period: 1000 nm) in a hexagonal lattice. The thickness of the depletion region is 2 μm.

IV. **Electrical Characteristics**

Fig. S8a shows the current-voltage characteristics of 30 µm diameter device, indicating that the dark-current at -5 V bias was 0.06 nA. In an ideal *pin* diode, the capacitance is defined as $C = \varepsilon A/d$ where A is the junction area, determined by the diameter of the mesa and d is

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depletion layer width which is composed of *i*-layer. Fig. S8b shows the capacitance-voltage (C-V) curves for PDs with different diameters. The capacitance is found to reach a constant value around ~10 V reverse bias. However, the measured capacitance values at -10 V were still lower than what is expected from 2 µm *i*-layer. For example, the capacitance of PDs (no-holes) 500 µm and 30 µm in diameter was supposed to be 10.1 pF and 36 fF, whereas the capacitance measured at -10 V was 22.5 pF and 110 fF, respectively. From the definition of ideal *pin* diode capacitance, the thickness of the intrinsic layer can be predicted from the linear relation between capacitance vs junction area. Fig. S8c shows the capacitance (measured at -10 V) vs. junction area of PDs with 6 different sizes. The slope of the linear line in Fig. S8c is ε/d, which suggests a calculated intrinsic layer thickness of 0.93 µm. Although 2 µm *i*-layer is designed and grown as the active layer, dopant diffusion from contacts (highly doped *n* and *p* layers) causes a reduction of *i*-layer thickness, (inset in Fig. S8c) contributing to higher-than-expected capacitance values. A non-zero intercept of the linear line in Fig. S8c suggests an additional capacitance which can be attributed to capacitance arising from contacts.

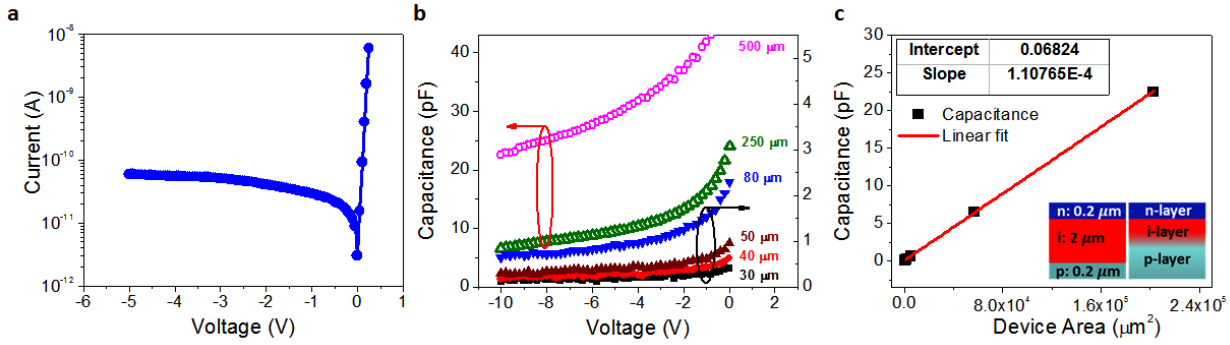

Figure S8 | Current-voltage and capacitance properties of PDs. a, Current vs voltage characteristics of a device with a diameter of 30 µm, showing dark current of 0.06 nA. **b,** Capacitance-voltage measurement of devices (no holes) with different mesa size (Left and right axes are dedicated for larger mesas and smaller mesas, respectively). **c,** Capacitance (at -10 V) vs device area, *inset:* schematic for *nip* layers with designed thicknesses and the case of dopant diffusion to *i*-layer from *p*-contact layer, indicating the *i*-layer thickness shrinkage.

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V. PD External Quantum Efficiency (EQE) and Photovoltaic (PV) Characteristics

External Quantum efficiency (EQE) measurements were conducted using a supercontinuum laser and a tunable filter that transmits a band of wavelengths with 5 nm width blocking the adjacent wavelength. Fig. S9a and b show the EQE vs wavelength measured from tapered holes with different diameters in the hexagonal and square lattice, respectively. Overall, holes with smaller dimensions (diameter and period) provide higher EQEs (an average of ~10% difference) compared to holes with larger dimensions in our current designs. In addition, the PDs with holes in hexagonal lattice provide slightly higher EQE compared to the ones with the holes in a square lattice.

An optical image of a device during EQE measurements is depicted in Fig. S9c, showing the location of electrical probes and fiber probe under the microscope. The position of the fiber probe was optimized by maximizing the photocurrent under constant bias. Fig. S9d presents the EQE values from several different devices with various designs of tapered holes under illumination of light at 850 nm.

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We also studied the photovoltaic (PV) characteristics of our devices with holes under a solar simulator. The PV efficiencies and open circuit voltage (V_{oc}) of several devices with different hole designs and passivated with different techniques were summarized in Table S4. Our best hole based solar cell produced 30.9 mA/cm^2 short circuit current and 0.38 V open circuit voltage, which provides 7.69% PV efficiency with only a ~3 μm crystalline Si layer without an

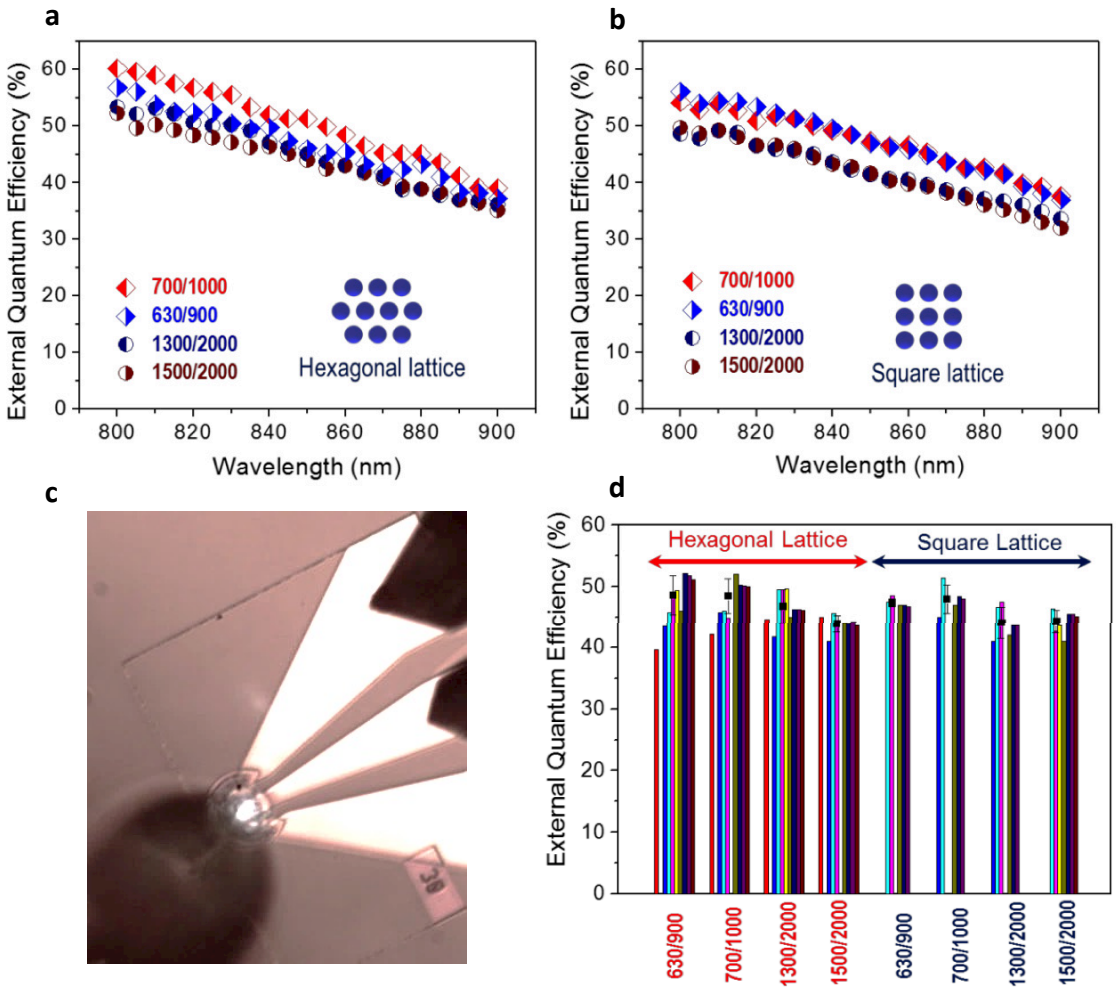

Figure S9 | External Quantum Efficiency (EQE) measurements and results. EQE vs wavelength (800-900 nm) for PDs with tapered holes with different diameters in **a**, hexagonal lattice and **b**, square lattice. **c,** Optical micrograph of a device during the EQE measurements, showing the electrical probes and fiber probe under microscope. **d,** EQEs measured from several different PDs with tapered holes with varying diameters/periodicity and lattices at wavelength of 850 nm. The black circles represent mean values. The standard deviation bars are also shown in the plot.

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antireflection coating or a back reflector mirror in the device structure.

Table S4 | Results of PV efficiency measurements for photovoltaic devices with integrated micro- and nanoholes

Hole Size diameter/period	Hole Lattice	Low Ion Energy Etch (LIEE)		Thermal oxidation		HF Passivation +PECVD oxide	
		PV Eff (%)	V_{oc} (V)	PV Eff (%)	V_{oc} (V)	PV Eff (%)	V_{oc} (V)
630/900	Hexagonal	7.44	0.38	**7.33**	0.58	4.2	0.32
700/1000	Hexagonal	**7.69**	0.38	6.6	0.53	NA	NA
1300/2000	Hexagonal	5.97	0.40	3.3	0.35	**7.34**	0.4
1500/2000	Hexagonal	6.66	0.41	NA	NA	5.4	0.35
630/900	Square	5.6	0.38	NA	NA	NA	NA
700/1000	Square	6.87	0.38	NA	NA	NA	NA
1300/2000	Square	4.69	0.39	NA	NA	NA	NA
1500/2000	Square	6.23	0.42	NA	NA	NA	NA
Flat-top	NA	4.18	0.42	3.2	0.34	**5.9**	0.48

VI. Surface Passivation

In this study, DIRE and RIE are used to create the holes in Si PDs. However, the energetic ions involved in the DRIE/RIE process cause the device to experience increased crystalline defects such as vacancies, interstitials, dislocations, or stacking faults, surface roughness, impurities, and device charging. The undesirable surface states, traps and recombination sites can be formed due to these defects and degrade the device characteristics impacting detection sensitivity, high-speed performance and energy conversion efficiency in solar cells. They are often caused by Si dangling bonds at the surfaces. Inside the Si crystal, each Si atom provides four sp^3 orbitals and when two orbitals meet, they form a covalent bond, which is the foundation of a Si diamond structure. However, since the crystal is abruptly terminated at surfaces, some sp^3 orbitals are unpaired and protrude into the vacuum. These unpaired orbitals are dangling bonds and are half-filled. If Si surfaces are unpassivated, unreconstructed/reconstructed arrays of dangling bonds will form metallic conduction channels, as predicted in [S33], and these channels will support

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undesirable dark current. Dangling bonds support metallic channels, provide surfaces states, or may cause trap centers, and therefore, they must be eliminated for PD applications. Saturating these dangling bonds with hydrogen atoms (hydrogenation) eliminates dangling bonds, surface states, and metallic channels, as shown theoretically in [S34]. Experimentally, hydrogenation of dangling bonds can be achieved with HF treatments, where Si dangling bonds exclusively react with H ions, as shown in [S35].

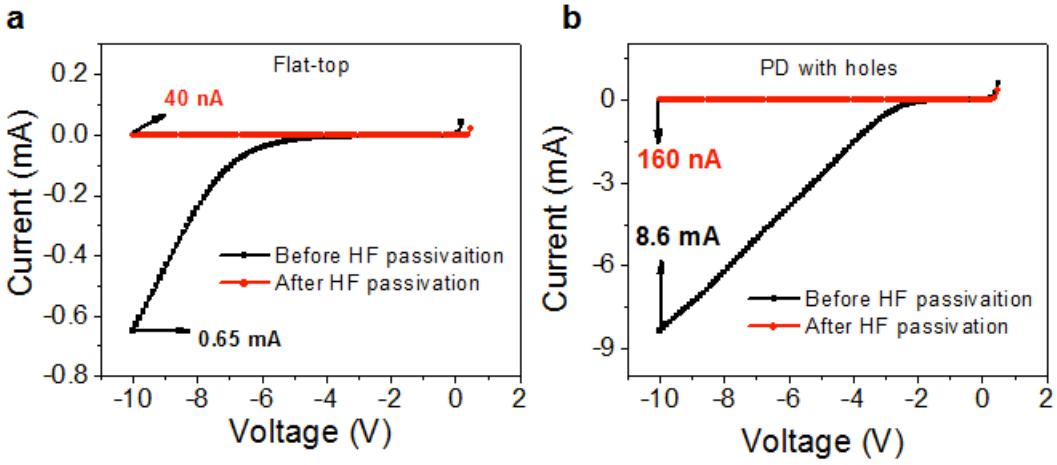

Figure S10 | Effect of HF passivation on leakage current. a, PDs with flat-top surface. **b,** PD with holes (d/p:1500/2000 nm). Both devices are large in diameter (500 μm).

After DRIE etching of holes and mesas, an extremely high leakage current was observed in our devices as shown in Fig. S10 (black curves). This high leakage can be attributed to the electrically active surface sites arisen from dangling bonds and defects created after DRIE process. H termination of Si surface is a well-known method to decrease the surface recombination velocity of Si. After dipping our devices in 1:10 HF: H_2O solution for 10 s, the leakage current was suppressed to the nA levels whereas it was in the mA range. Slightly higher current in hole based devices compared to the flat-top device after HF passivation can be attributed to the high surface area of the hole-based structures.

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The direct effects of surface states appear in PDs as low QE and low high-speed performance. The excess carriers generated by light are trapped at the surfaces and only contribute to the photocurrent when under high bias voltages. As can be seen in Fig. S11, a voltage dependent QE was observed in hole-based photodiodes whereas the QE in flat-top PDs was independent of voltage in the reverse bias. However, after HF passivation, the surface was isolated and the majority of the carriers were no longer trapped as suggested by the Fig. S11b (blue line).

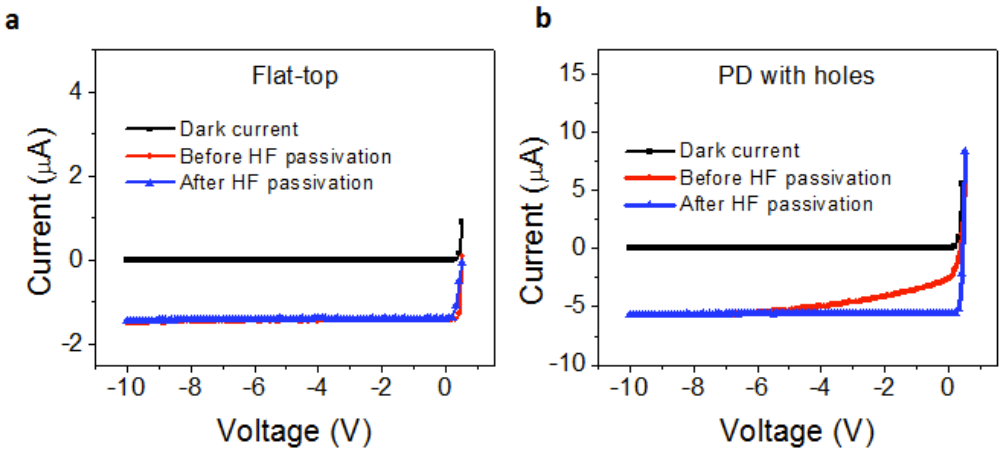

Figure S11 | Effect of HF passivation on photocurrent of PD under illumination with 850 nm wavelength of light. a, PD with the flat-top surface. **b,** PD with holes (d/p:630/900 nm).

In addition to hydrogen passivation, several other methods have been applied to inhibit device degradation induced by surface damage from the dry etch, including thermal oxidation, subsequent oxide removal, and low ion energy etch. All the passivation methods lowered the leakage current drastically, and some of these methods even reduced the leakage current by more than four orders of magnitude as shown in Fig. S12a. The high leakage (in the range of mA) was observed right after the DRIE etch before the devices went through any treatment. Oxidation and hydrogen passivation with HF dip reduced the leakage current to nA range whereas it was around ~ μA range after low ion energy etch.

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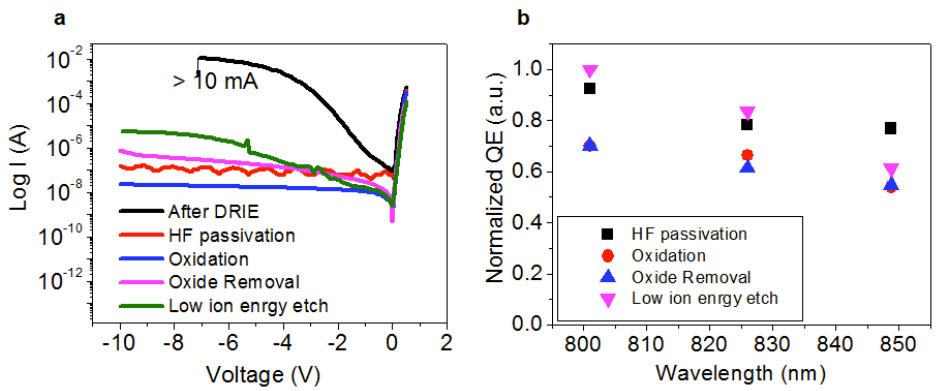

Figure S12 | Comparison of different passivation methods applied for inhibiting leakage current. a, Leakage current before and after hydrogen passivation, oxidation, oxide removal and low ion energy etch. **b,** Normalized QE measured at 3 different wavelengths (800 nm, 826 nm and 848 nm) after each passivation under 10 volts reverse bias for PDs with cylindrical holes (d/p:1500/2000 nm).

Although thermal oxidation passivated the etched surface efficiently, the inherently high temperature associated with the oxidation process could cause the dopant diffusion from highly doped contacts to the *i*-layer. As it can be seen in Fig. S12b, the efficiency of the PDs after oxidation dropped to a lower level compared to the hydrogen passivated PDs, indicating a thinner absorbing layer (reduced intrinsic layer thickness). BOE can successfully remove the thin oxide layer grown by thermal oxidation as depicted in Fig. S5, however, the efficiency after oxide removal is still lower compared to other methods. It suggests that the high-temperature oxidation process irreversibly caused the dopant diffusion which leads to the lower efficiency. On the other hand, the efficiency of the devices passivated by low energy ion etch of ~50 nm Si was similar to the devices with H-terminated surfaces, suggesting that the low energy ion etch successfully etched off the damaged Si surface caused by the DRIE and didn't cause any further damage to the device. Slight differences in QE after low ion energy etch compared to hydrogen passivated devices can be a result of a wavelength shift of higher QE after ~ 100 nm enlargement in hole diameter due to etching of ~ 50 nm Si from each side of the hole.

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VII. Projection of 3 dB bandwidth and EQE of a *pin* PD with integrated holes

Figure S13 presents a perspective for 3bB bandwidth and EQE of a *pin* PD in the case of introducing air holes in the Si matrix. Integrated holes not only provide light trapping and high optical absorption but also can be designed to reduce the junction capacitance by decreasing the junction area. In that case, a response of a *pin* PD with 50 % material fill factor can reach 40 GHz with ~0.6 μm *i*-layer. FDTD simulations predict ~30 % EQE from a PD having such a thin *i*-layer integrated with tapered holes. For simplicity, the thickness of the whole stack was kept same in the FDTD simulations while the thickness of the *i*-layer was varied and absorption only in *i*-layer was calculated to estimate EQE. The thin lines in Fig. S13 shows the ultimate response and EQE of flat-top counterparts as a comparison.

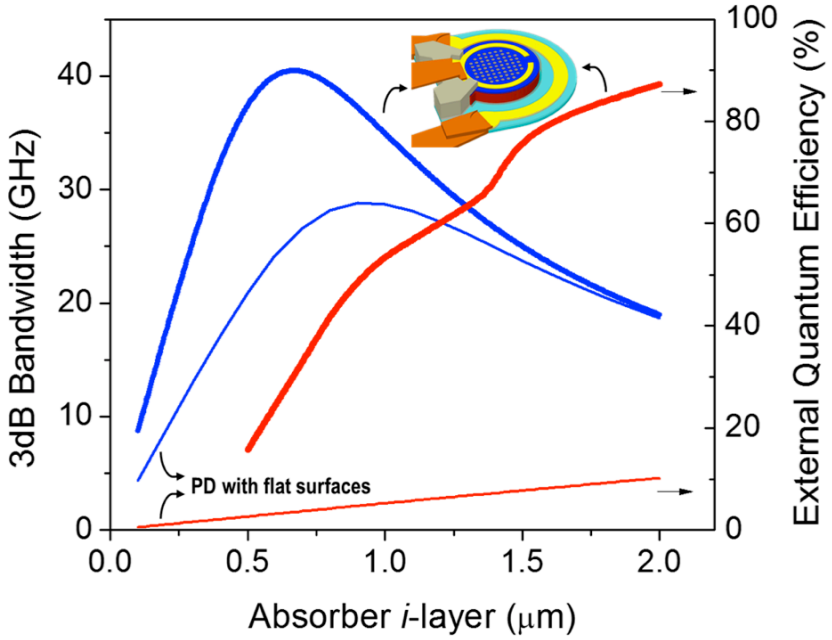

Figure S13 | Projected 3 dB bandwidth and EQE of a PD with integrated tapered holes. Thick curves show simulated 3-dB bandwidth (left axis) and EQE (right axis) of a PD with tapered holes (assuming e 50% area is filled with holes contributing to reduced junction capacitance by a factor of 2). Thin curves show the calculated 3-dB bandwidth and EQE of a PD with a flat top surface. A circular PD with a dimeter of 30 μm was taken into consideration for the calculations.

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VIII. Links and descriptions of Supplementary Videos*

Video 1: Top view of the slow and stationary optical modes in cylindrical holes. Animation showing top view of a vertically oriented incident light beam propagating laterally in the x-y plane around the cylindrical holes in a square lattice. The time scale is 0-56 femtosecond. The beam, along with the slow and stationary lateral modes, stays much longer time in the hole structure than it needs to go through a 2 μm thick Si layer. This allows lateral propagating modes to have greater interaction with silicon in both duration and length. Such modes of propagation increase the effective optical absorption coefficient by more than an order of magnitude in a thin silicon layer while ensuring ultra-fast transit time for the carriers.

Video 2: Cross-sectional view of the optical modes in cylindrical holes. Animation showing cross-sectional view of cylindrical holes in a square lattice with a vertically oriented incident light beam propagating laterally in the y-z. The time scale is 0-56 femtosecond. The description of the physical phenomenon presented in Video 1 is also valid in this video.

Video 3: Top view of the optical modes in tapered holes.
Same as Video 1, for tapered holes in a square lattice. Stronger lateral modes are excited in silicon with integrated tapered holes than their cylindrical counterpart.

Video 4: Cross-sectional view of the optical modes in tapered holes.
Same as Video 2, for tapered holes in a square lattice. The cross-section view shows that stronger lateral modes are excited in silicon with integrated tapered holes than their cylindrical counterpart.

Video 5: Top view of poynting vectors under vertical optical illumination.
Animation showing the poynting vectors directing light energy from the tapered holes in a square lattice to lateral directions in the x-y plane (top view). Time scale is 0-28 femtosecond.

Video 6: Cross-sectional view of poynting vectors under vertical optical illumination.
Animation showing the poynting vectors in the cross-sectional view of a hole. The video shows that the poynting vector is directed from the holes into silicon indicating that the energy propagates outward from the holes and is trapped in silicon until it is mostly absorbed.

**Note: the x-y* plane is the in-plane direction, and *z*-direction is the hole axis direction.

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