



W&Wsens Devices Inc.

Time-of-Flight Solutions For The Next Generation

¹
www.wwsensdevices.com

W&W Breakthrough Innovation : Photon Trapping
Speed & Efficiency in Silicon PD
Fully Compatible with CMOS / BiCMOS Process
Straight Forward Integration With Electronics

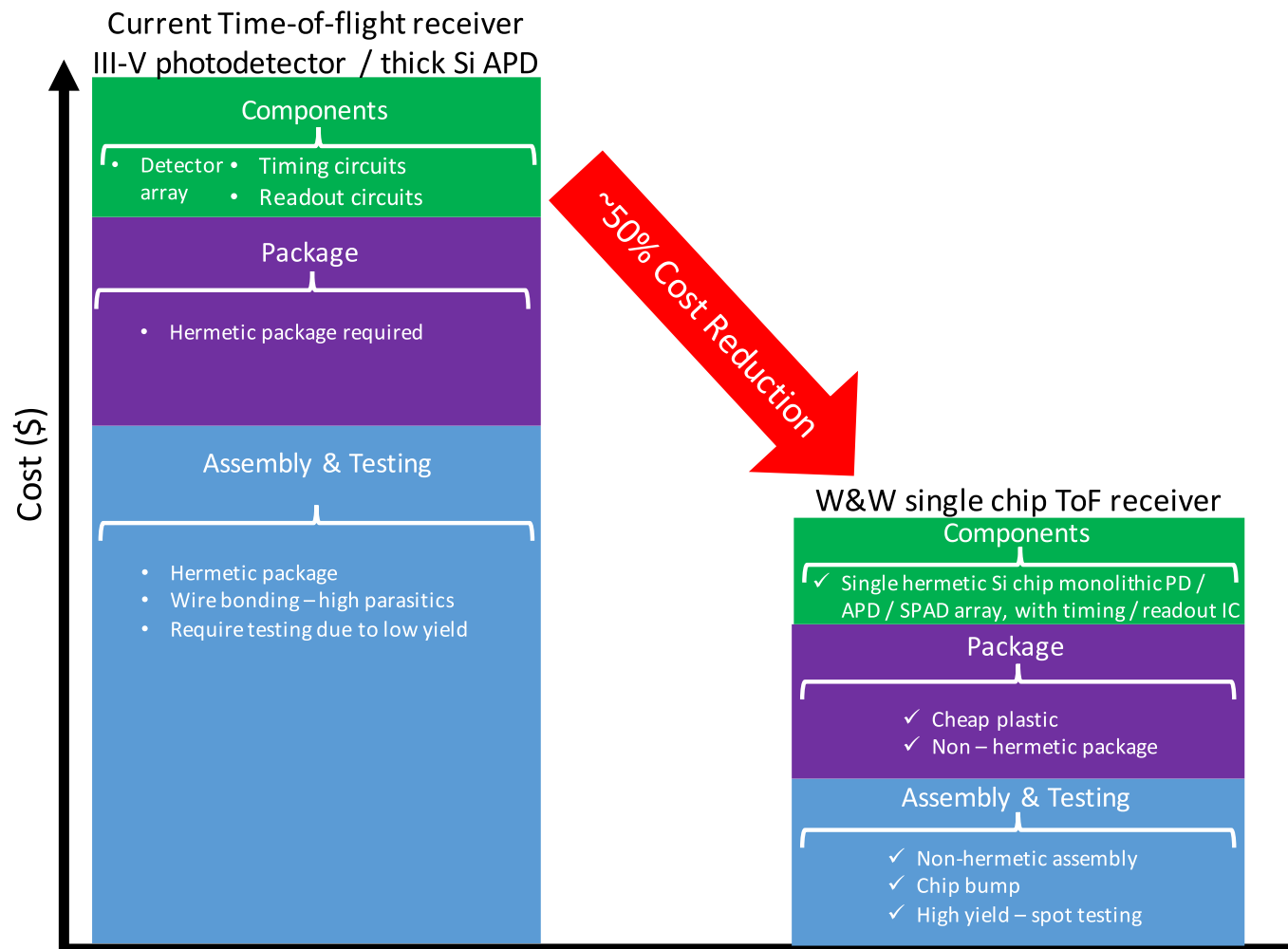
800 – 1000 nm Si
800 – 1650 nm Ge on Si



Single Chip

27 Issued & Published Patents
100+ Provisional Filings

Cost Reduction with Monolithic Integration



W&Wsens Devices Inc. IP Portfolio

27 Issued Patents and Published Patent Applications
Over 100 Provisional Patent Applications

United States Issued Patents:

1. US 9,496,435 B2 – Date issued: Nov. 15, 2016
2. US 9,525,084 B2 – Date issued: Dec. 20, 2016
3. US 9,530,905 B2 – Date issued: Dec. 27, 2016
4. US 9,818,893 B2 – Date issued: Nov. 14, 2017

United States Patent Allowed:

1. US 2018/0102442 A1 – Date published: Apr. 12, 2018

United States Published Patents:

1. US 2019/0019899 A1 – Date published: Jan. 17, 2019
2. US 2018/0102442 A1 – Date published: Apr. 12, 2018
3. US 2016/0254407 A1 – Date published: Sep. 1, 2016
4. US 2016/0308075 A1 – Date published: Oct. 20, 2016
5. US 2017/0194522 A1 – Date published: Jul. 6, 2017
6. US 2016/0307939 A1 – Date published: Oct. 20, 2016
7. US 2016/0126381 A1 – Date published: May 5, 2016

International Published Patents:

1. WO 2019/018846 A3 – Date published: Jan. 24, 2019
2. WO 2019/089437 A1 – Date published: May 9, 2019
3. WO 2017/112747 A1 – Date published: Jun. 29, 2017
4. WO 2016/081476 A1 – Date published: May 26, 2016
5. WO 2014/190189 A2 – Date published: Nov. 27, 2014

China Issued Patents:

1. CN 107078145 B – Date issued: May 7, 2019
2. CN 105556680 B – Date issued: Dec. 22, 2017

China Published Patent:

1. CN 109155340 A – Date published: Jan 4, 2019
2. CN 107078145 A – Date published: Aug. 18, 2017
3. CN 105556680 A – Date published: May 4, 2016

Japan Published Patents:

1. JP 2018-508970 A – Date published : Mar. 29, 2018
2. JP 2016-526295 A – Date published : Sep. 1, 2016

Korea Published Patents:

1. KR 10-2016-0039150 – Date published: Oct. 2016

Europe Published Patents:

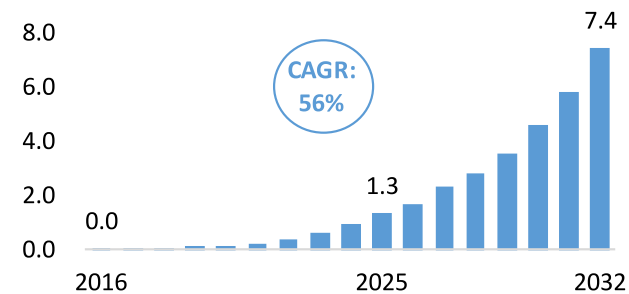
1. EP 3411906 A1 – Date published: Dec 12, 2018
2. EP 3221895 A1 – Date published: Aug. 15, 2018
3. EP 3000134 A2 – Date published: Mar. 30, 2016

Global LiDAR market outlook

LiDAR is a key enabler for capturing real-time 3D data

	LIDAR	Short Range Radar 24 GHz UWB	Long Range Radar 77 GHz	Ultrasonic	Vision	Infrared
Short Range (0-2MM)						
Nominal Range (2-30MM)						
Long Range (30-100MM)						
Narrow Vertical FOV <10deg						
Wide Vertical FOV >30deg						
Angular resolution						
Object speed measurement						
Bad weather operation						
Blockage (impurity on sensor)						
Night operation						
Sensitivity to Light						
Cost						

LiDAR Shipment Forecast⁽¹⁾ (mm units)



- LiDAR is expected to be a \$7-8bn market by 2030, with a majority of revenues coming from solid-state and flash LiDAR systems⁽¹⁾
- Between 2015 and 2025, 10 key auto OEMs are expected to spend ~\$345bn on autonomous, connectivity, and electrification R&D⁽²⁾
- IEEE estimates that roughly 75% of road-borne traffic should include self-driving cars by the year 2040⁽³⁾
- Prominent auto OEMs are asking for LiDAR modules to cost less than \$100
 - Currently, best-in-class LiDAR modules are almost 80x more expensive today

(1) Source: Yole – The Automotive LiDAR Market April 2018.

(2) Source: Frost Perspectives – July 14, 2017.

(3) Source: Technavio – Global Automotive LiDAR Sensors Market 2016-2020.

Technology differentiation of W&Wsens photodetector

- Standard CMOS / BiCMOS processing for integration ; no exotic materials
- Straight forward path to APD / SPAD CMOS process for integration
 - **Very thin** Photodetector layer (0.1 – 1.0 μ m vs 20 – 200 μ m used currently)
 - **Lower voltages** (35V vs 200-600V used current Si APD)
 - **High sensitivity** ~85% @ 850 nm (Lateral Structure)
 - **APD Gain > 1000X**
 - **Fast rise time – 10s of pico sec** allow for high depth resolution in LiDAR detection
 - **Wavelength 850 nm, 905 nm, 940 nm, 1550 nm (Ge on Si)**
- Dramatic cost reduction

W&W innovation

photodetectors in LiDAR & DCI

- Photon trapping with microstructure holes $\sim \lambda$ dimensions
- High speed & high external quantum efficiency
 - Surface illuminated
 - 2D PD array
- Enable monolithic integration with CMOS / BiCMOS ASICs
 - Improvement in performance – reduced parasitics
- Compatible with mature CMOS / BiCMOS processing & manufacturing
 - High reliability
 - High volume
 - High yield
- Wavelength range 800 nm – 1650 nm
 - Si 800 nm – 1000 nm
 - Ge on SOI 800 nm – 1650 nm

W&Wsens Demonstrated – Proof of Concept

Microstructure holes to enhance absorption (non-optimal materials / processing)

- Enable Si to have high external quantum efficiency (EQE) – in 2 structures: vertical PIN & lateral Schottky MSM
- 37X @ 905 nm enhancement of the effective absorption coefficient
- High speed
- Surface illuminated 30 – 500 micron diameter photo sensitive lateral dimension

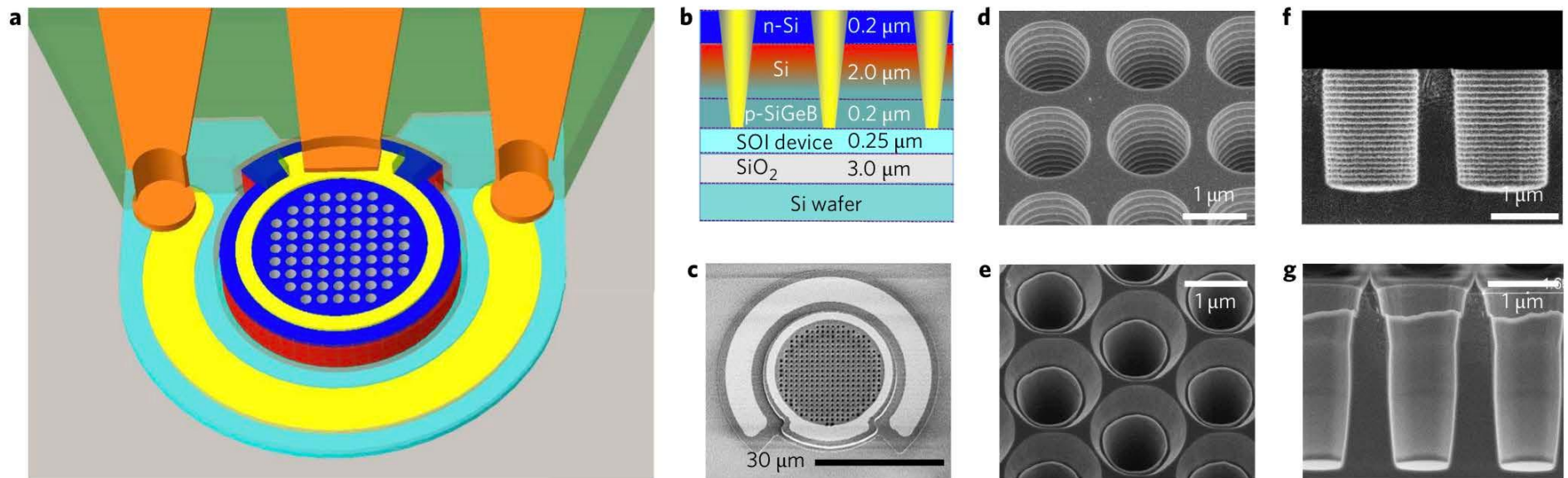
Summary

- ✓ **Disruptive photo detection technology with a simple structure for easy CMOS monolithic integration**
- ✓ **IR Sensitivity Enhancement with light trapping**
- ✓ **Wavelength 800 – 1000 nm Si ; 800 – 1650 nm Ge on Si. Pico second rise time, <35 volt APD**
- ✓ **Addresses massive and fast growing markets (Data center interconnect, LiDAR, time-of-flight)**
- ✓ **Greater than 2X cost reduction through monolithic integration**
- ✓ **Strong IP portfolio – 27 issued & published patents, 100+ provisional filings**

W&W Experimental Results

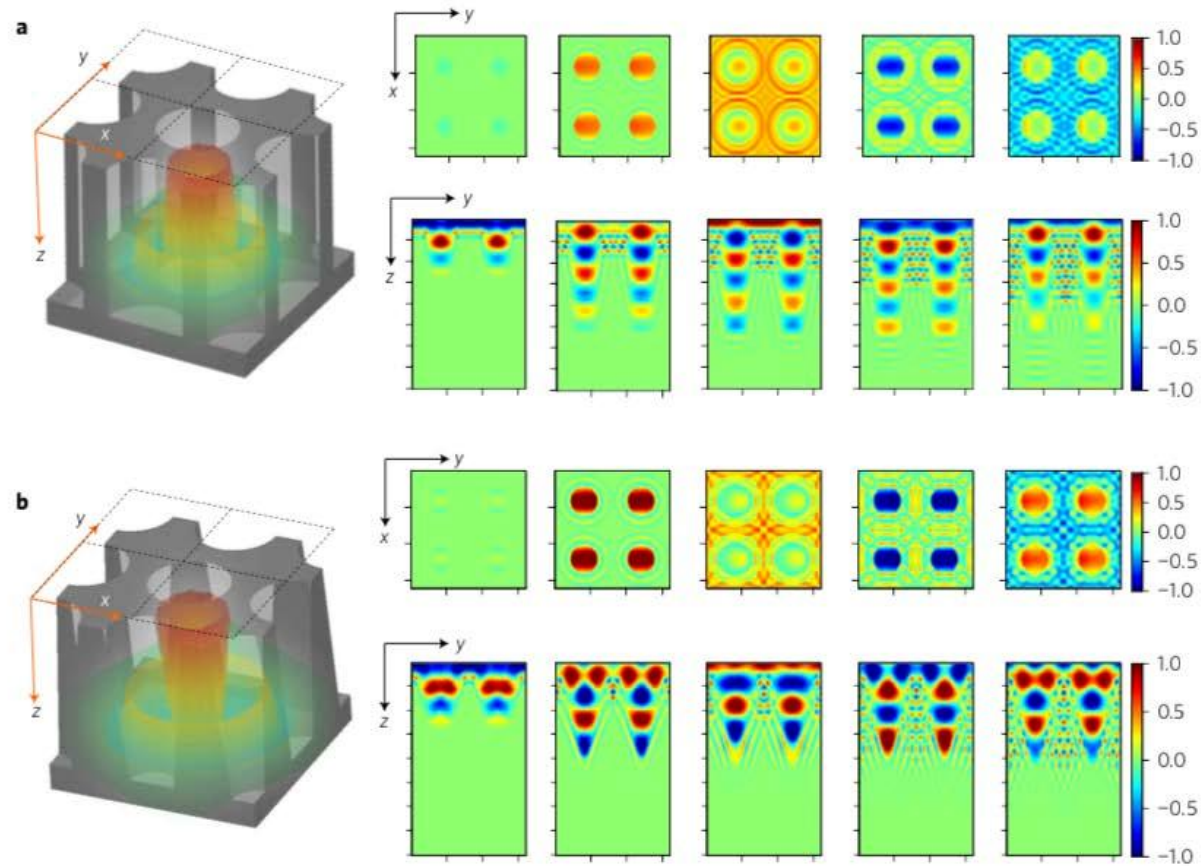
Microstructure Holes To Enhance Absorption

- Microstructure holes 400 – 1300 nm diameter
- Spacing between holes 100 – 500 nm
- PIN vertical structure
- Diameter of PD 30 – 100 μm



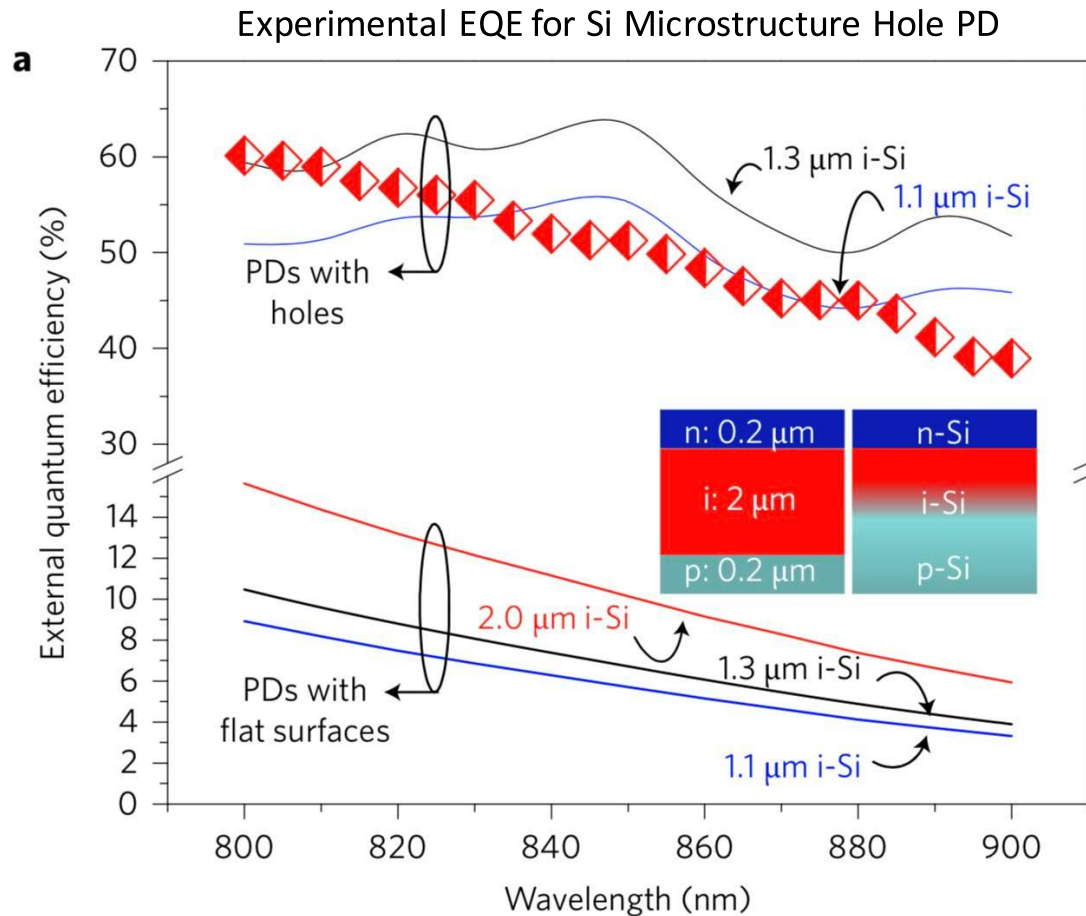
Silicon photodiode with integrated micro- and nanoscale holes. **a**, Schematic of the ultrafast photodiode with a thin absorbing region. Colour coded layers: blue, n-Si layer; red, i-Si layer; turquoise, p-Si layer; transparent, insulating nitride/oxide layer; yellow, ohmic contact metal; brown, high-speed coplanar waveguide (CPW); green, polyimide planarization layer. **b**, The n-i-p photodiode structure on an SOI wafer, showing the integrated tapered holes that span the n, i and p layers. **c**, Scanning electron micrograph of the active region of a high-speed photodiode (30 μm diameter). **d, e**, Square (**d**) and hexagonal (**e**) hole lattice integrated in the photodiodes. **f, g**, Cross-sections of cylindrical (**f**) and funnel-shaped or tapered (**g**) holes etched into the active photodiode regions.

Finite Difference Time Domain Simulation of Optical Fields in Si Microstructure Holes



Microstructure Holes To Enhance Absorption

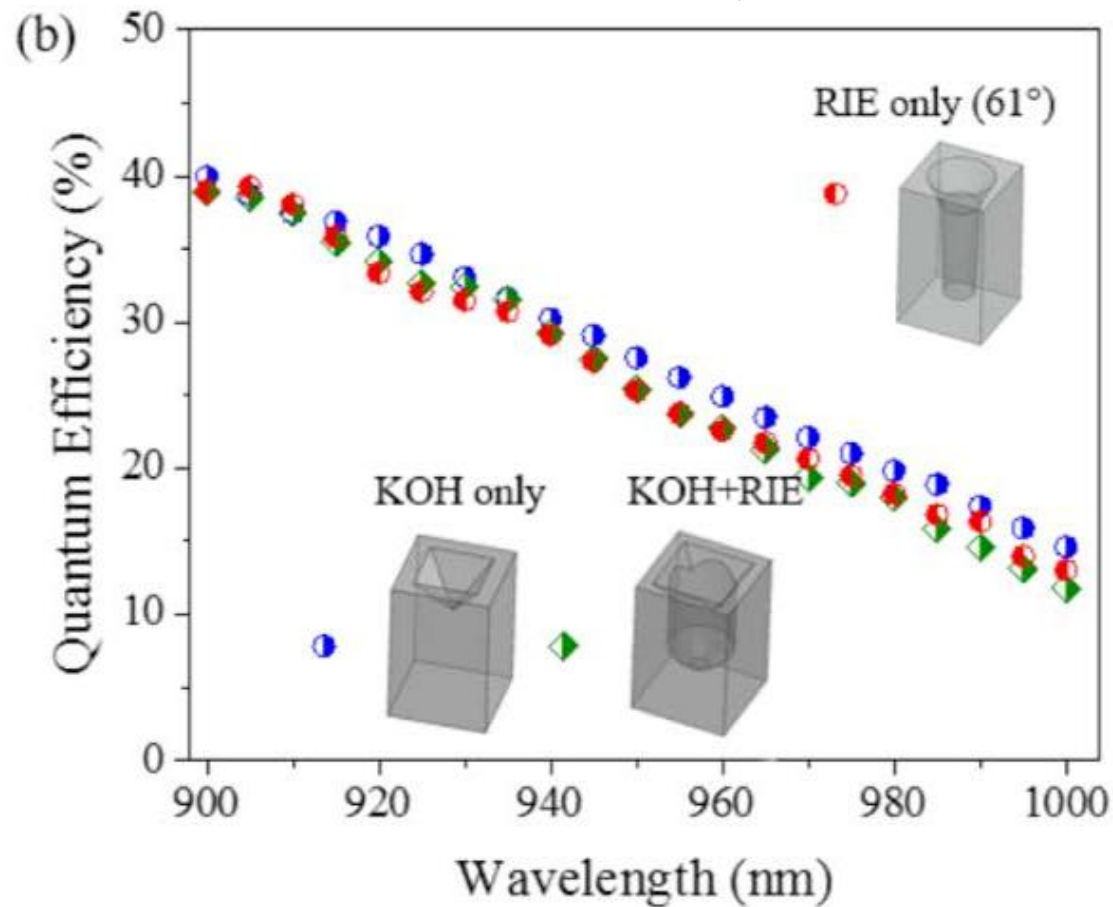
Experimental Results 800 – 900 nm



Microstructure Holes To Enhance Absorption

Experimental Results 900 – 1000 nm

Wet Etch / Wet Etch + Dry Etch Holes

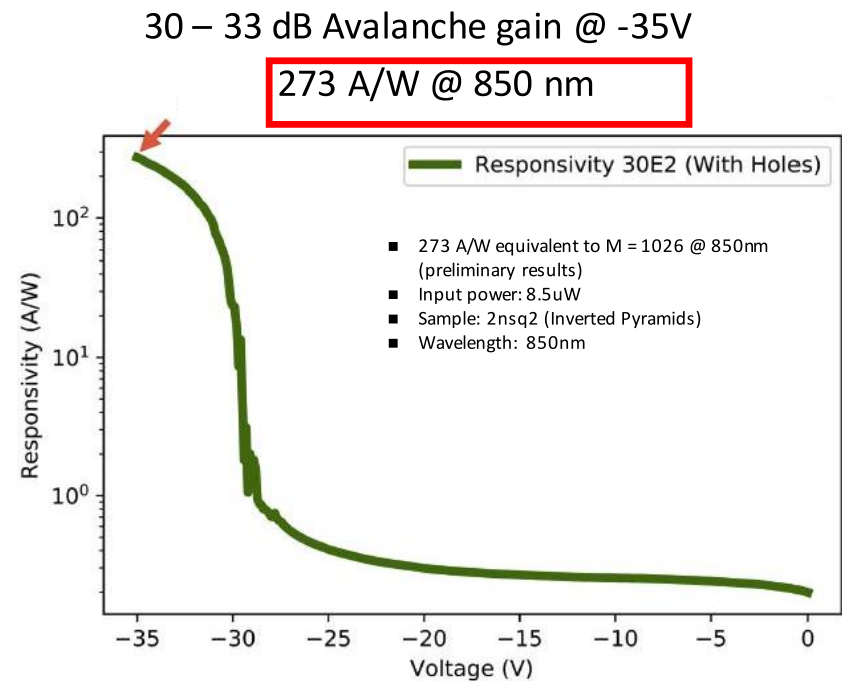
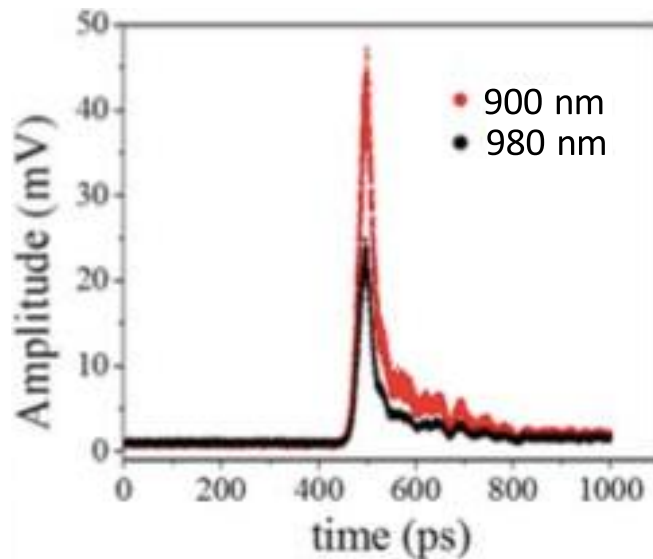


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Silicon Microstructure Hole APD

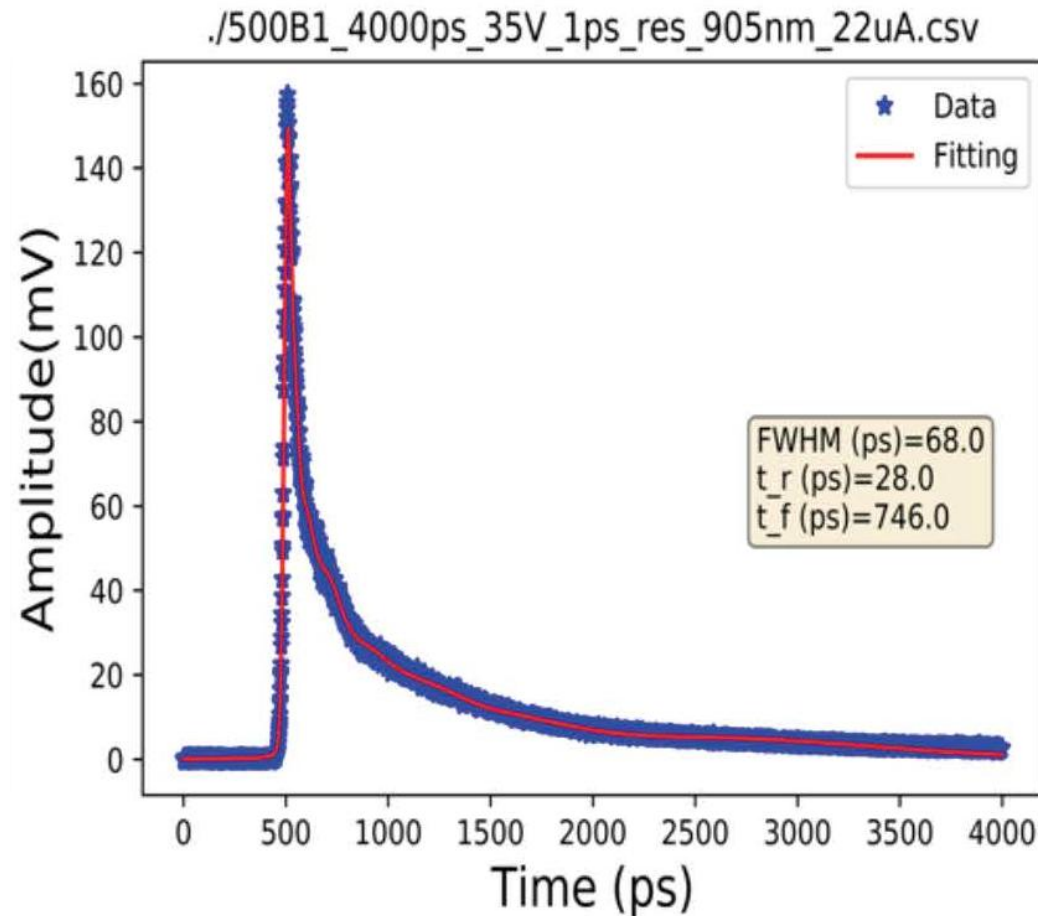
Experimental Results

Impulse response of microstructure hole
Si Pd to 900 nm and 980 nm laser pulses
30 ps FWHM 10 – 90% rise time
approximately 15 ps



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500 μm PD @ 905 nm
35 volt, rise time 28 ps, M = 1600 (37V)



Basic Fabrication Steps for Integrating with CMOS ASICs Vertical Structure

Vertical Fabrication Steps

1. Starting material SOI



2. Deep N well, shallow P well

PMOS / N implant retrograde well



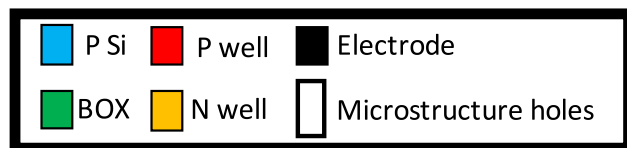
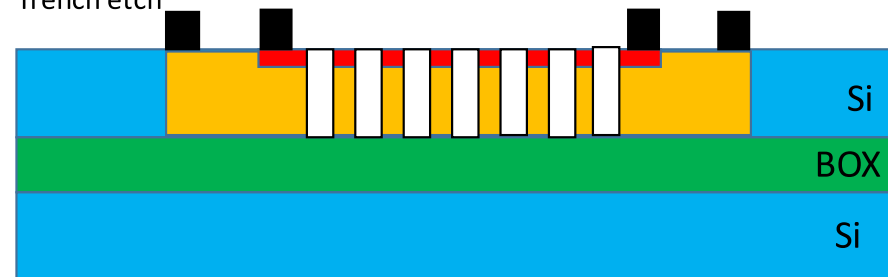
3. Electrode

Metal interconnect



4. Etch microstructure holes

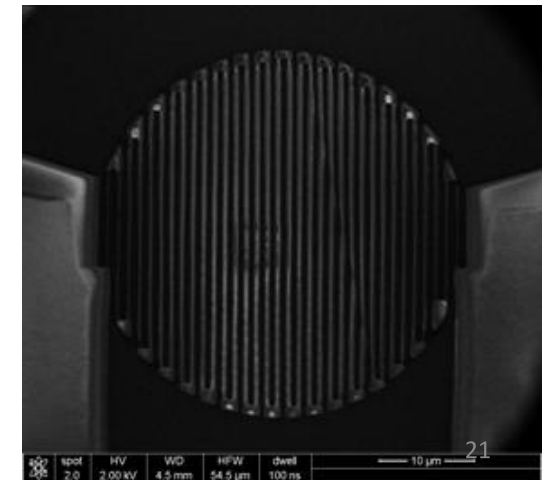
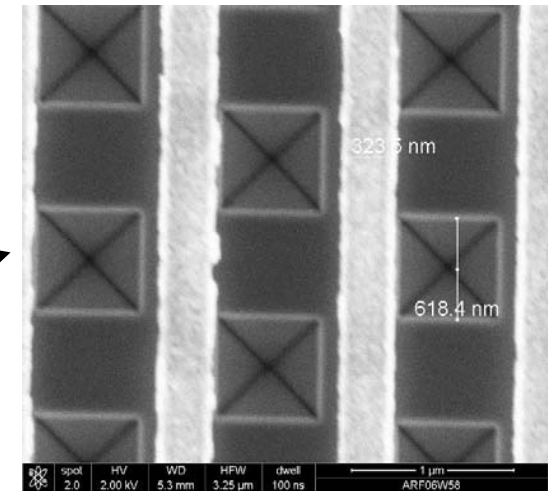
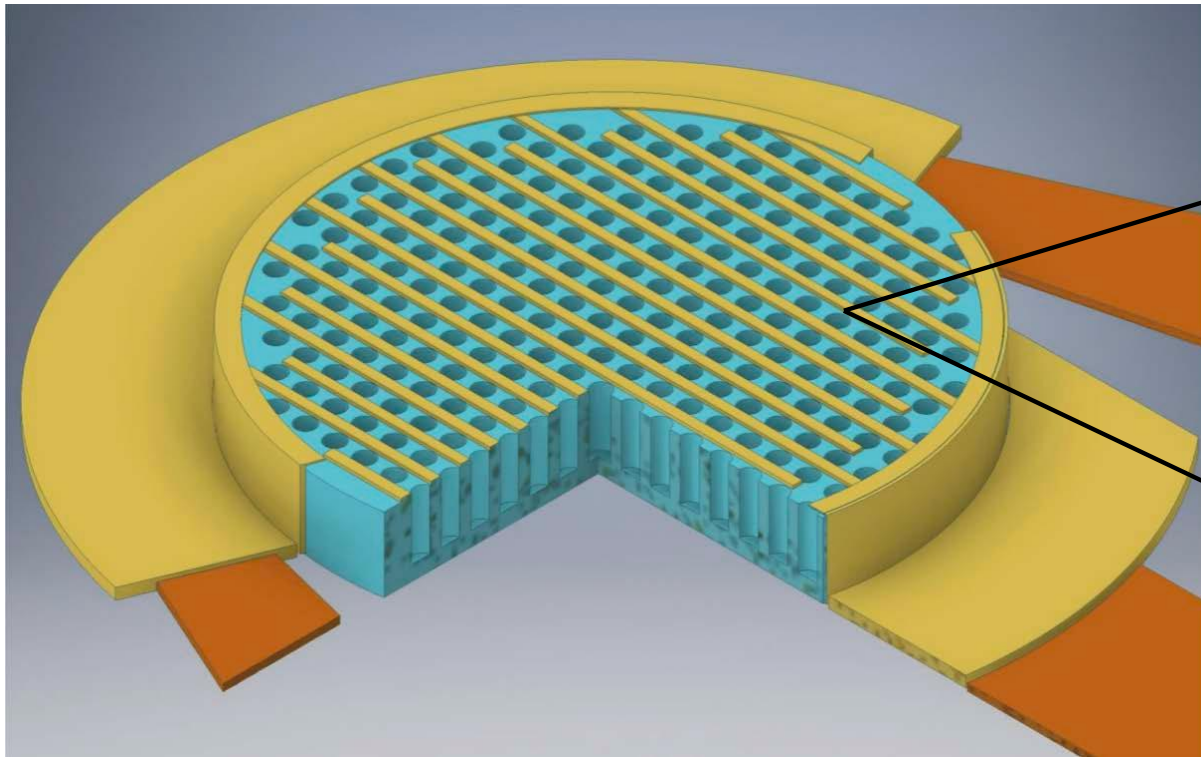
Trench etch



W&W – Lateral PIN

W&Wsens Devices Inc. Metal-Semiconductor-Metal Lateral Structure

W&Wsens Devices Inc. Lateral Si MSM PD



Basic Fabrication Steps for Integrating with CMOS ASICs Lateral Structure

Lateral Schottky MSM Fabrication Steps

1. Starting material SOI



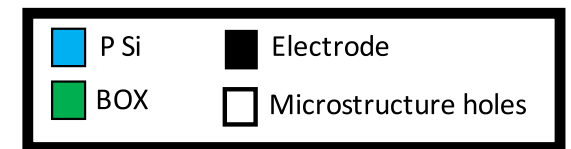
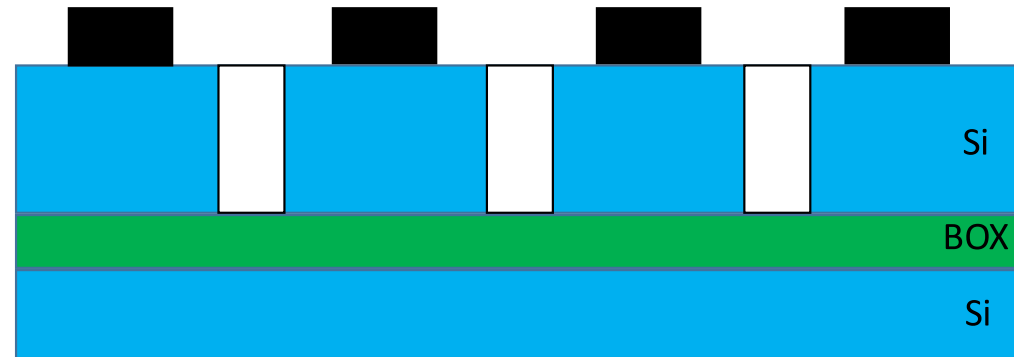
2. Interdigitated Electrodes

Interconnect metal



3. Etch microstructure holes

Trench etch

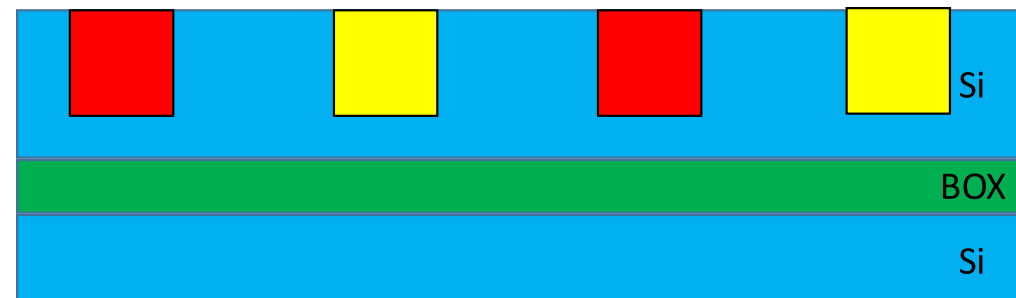


Lateral PIN Fabrication Steps

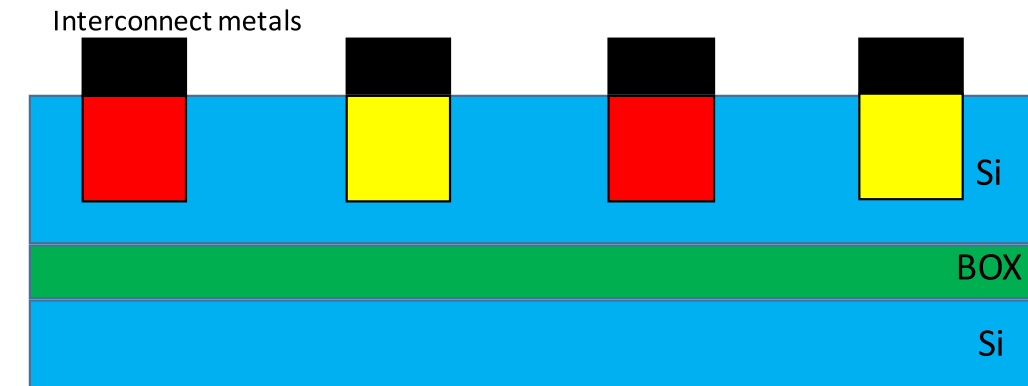
1. Starting material SOI



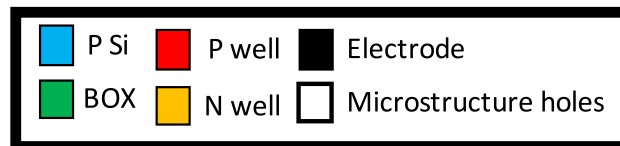
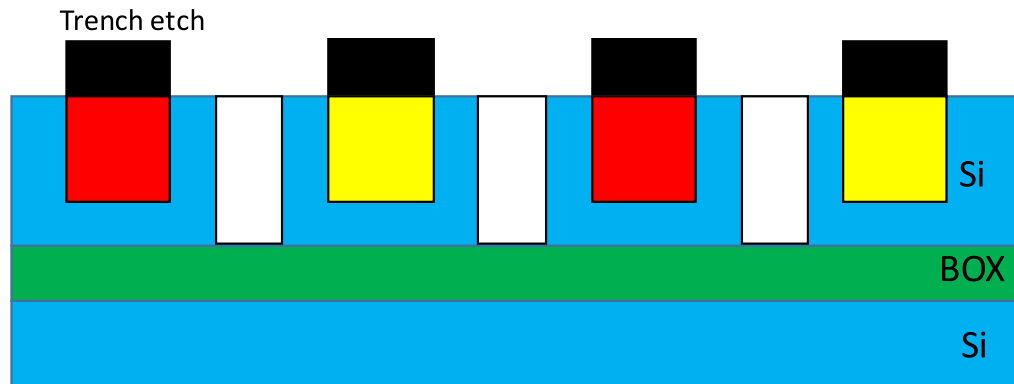
2. P and N wells
PMOS / NMOS



3. Interdigitated Electrodes

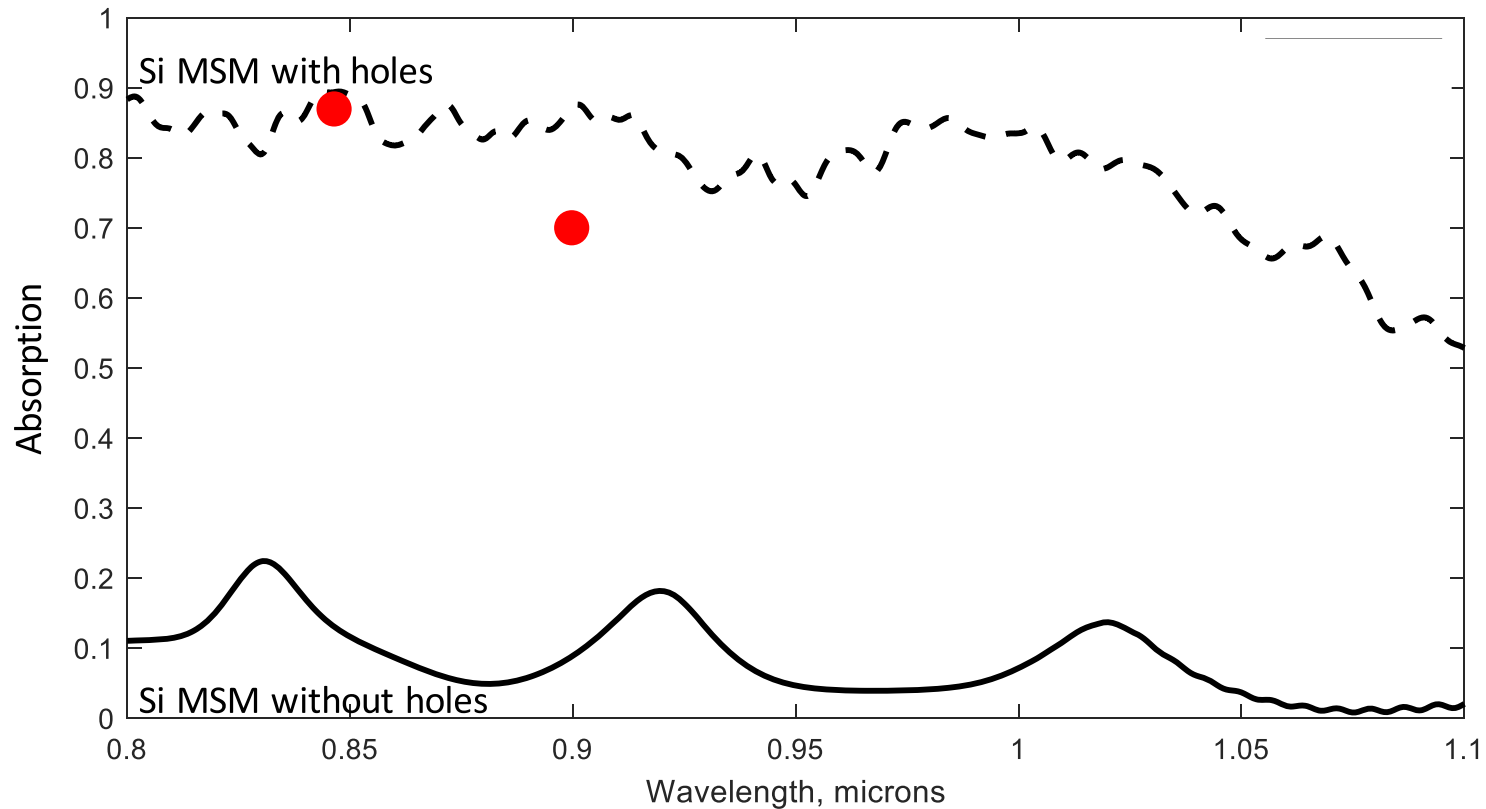


4. Etch microstructure holes

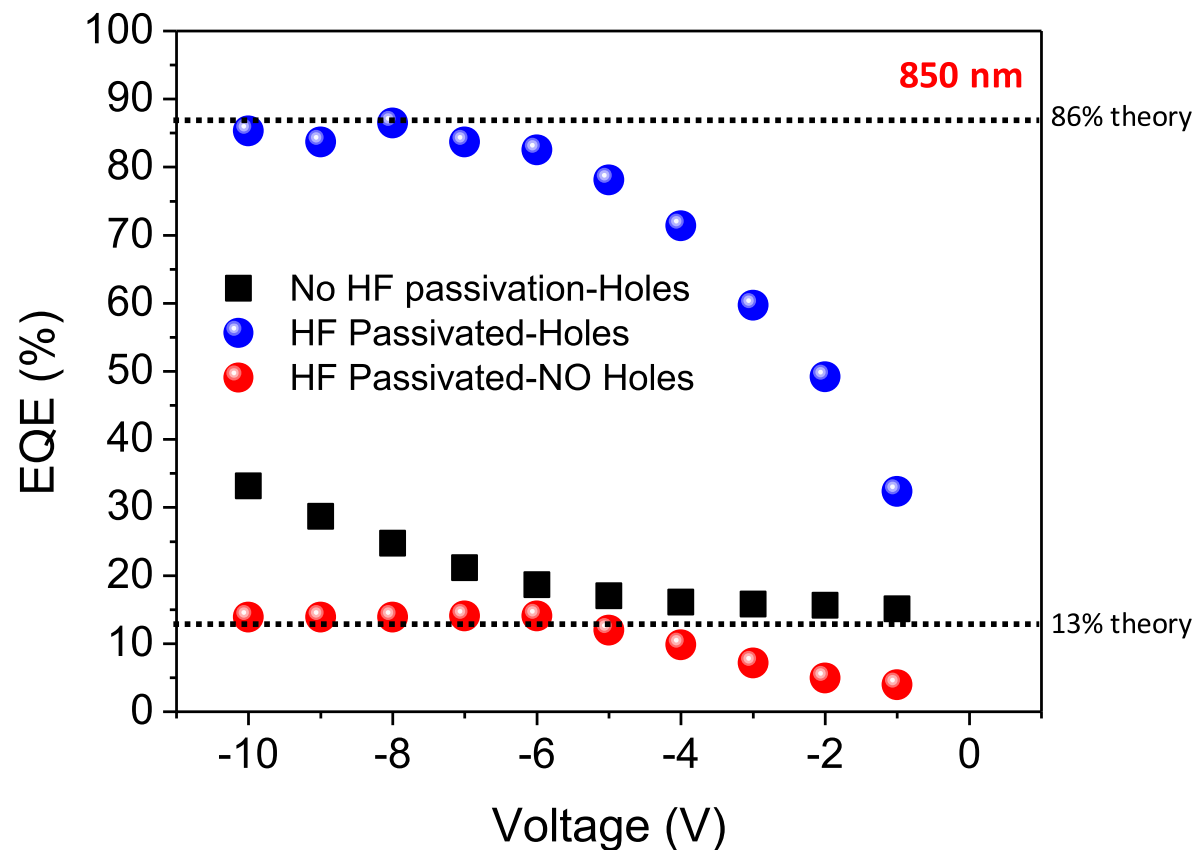


Si MSM Microstructure Hole Enhanced Absorption- FDTD Simulation

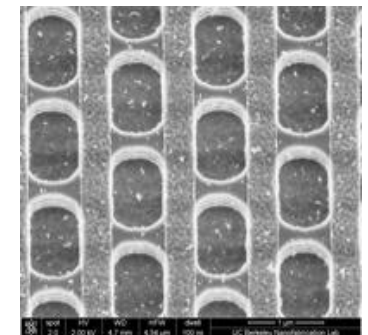
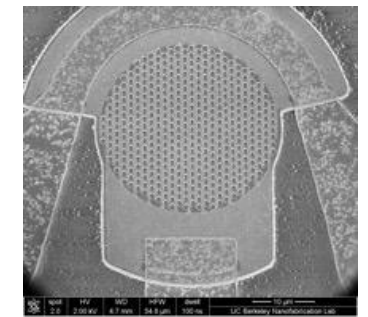
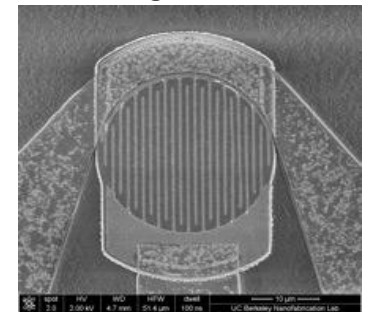
700 nm diameter, 1000 nm period, square lattice



W&Wsens Devices Inc. MSM Lateral Structure Experimental EQE Results

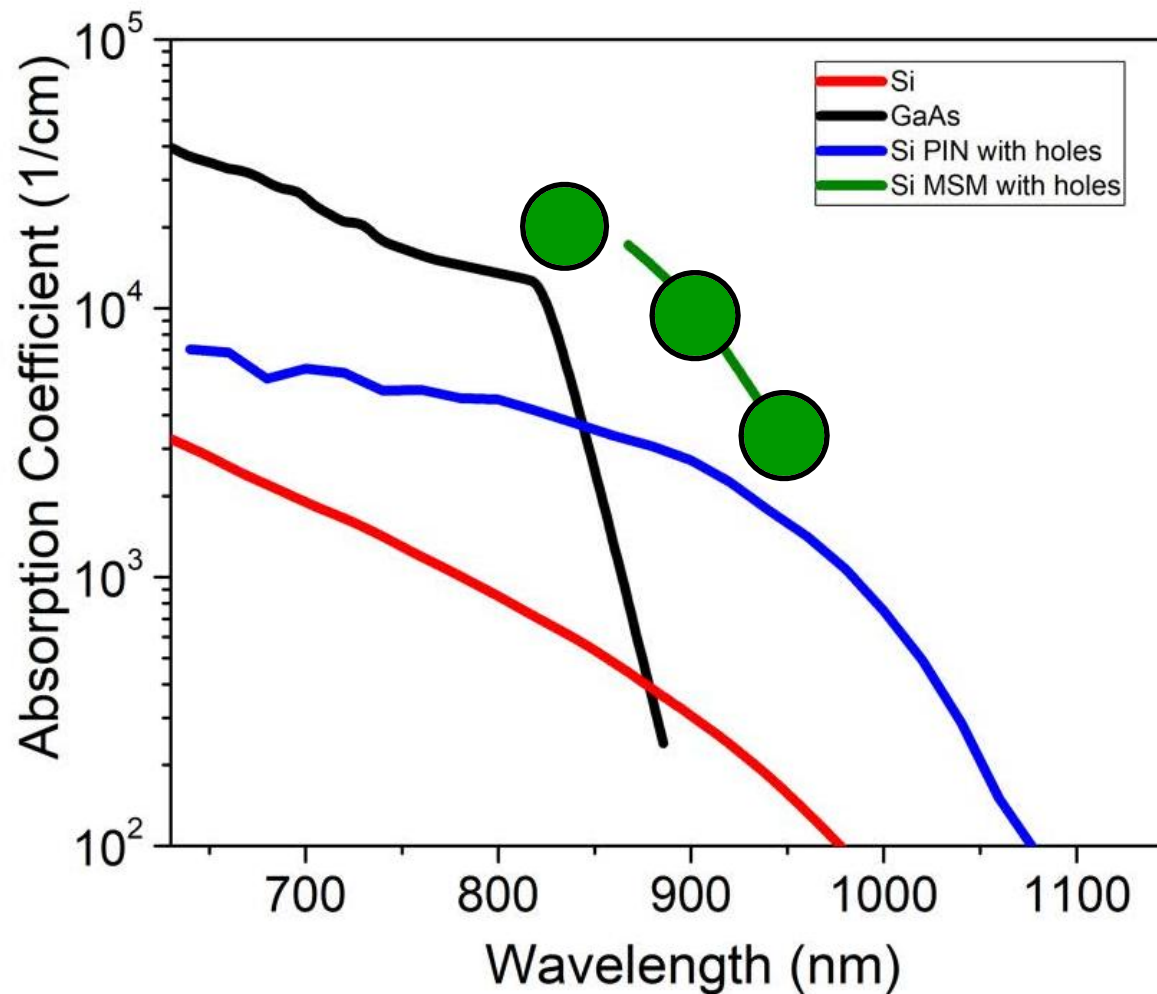


SEM Images of MSM PD

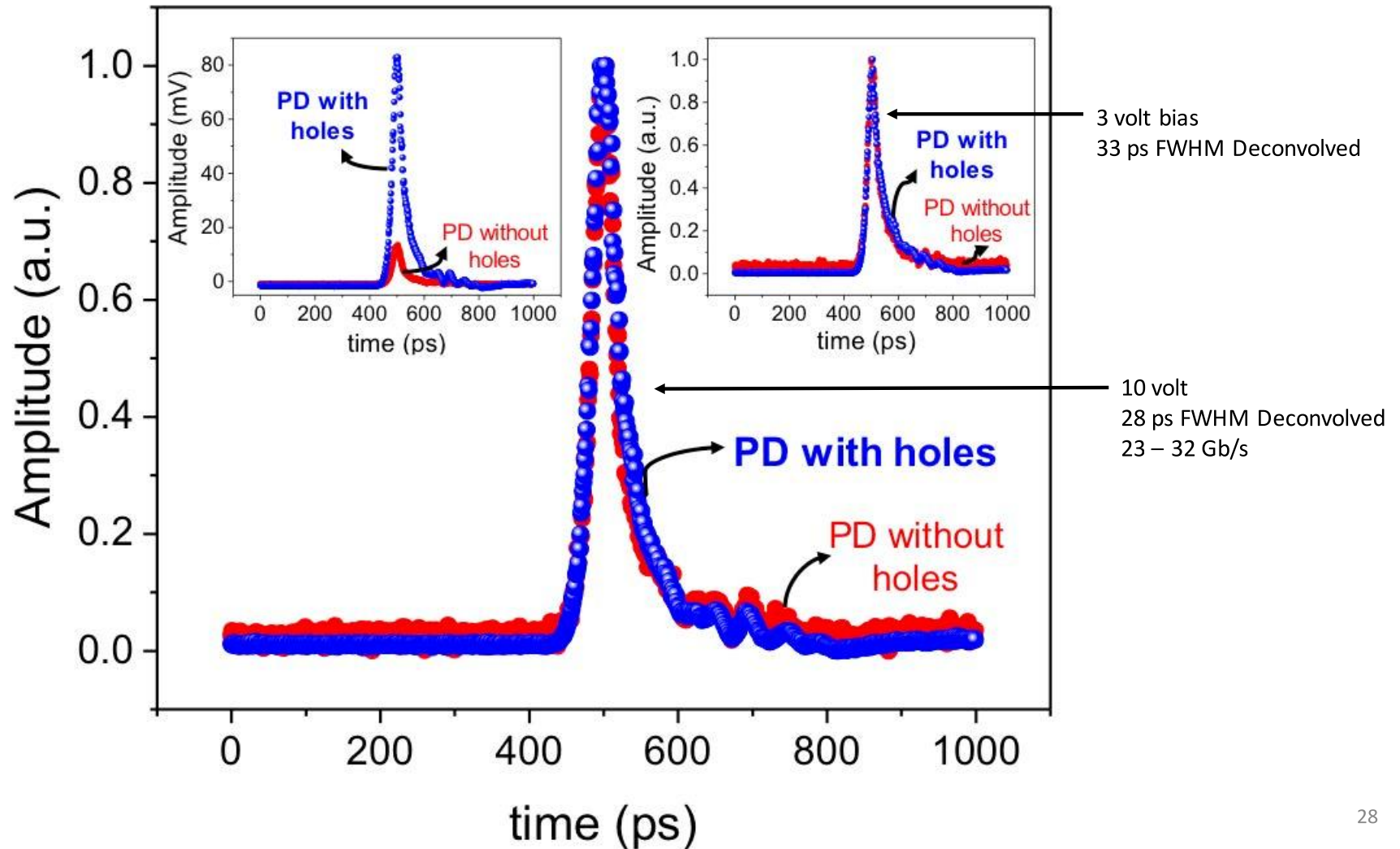


Absorption Coefficient

Enhancement 35X @ 850 nm, 37X @ 905 nm



MSM Impulse Response 850 nm



Appendix 1 – Ge on Si

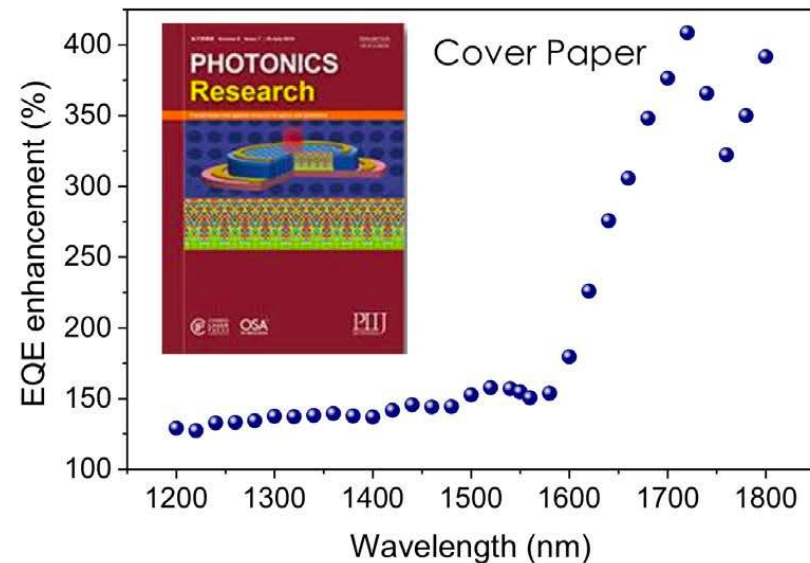
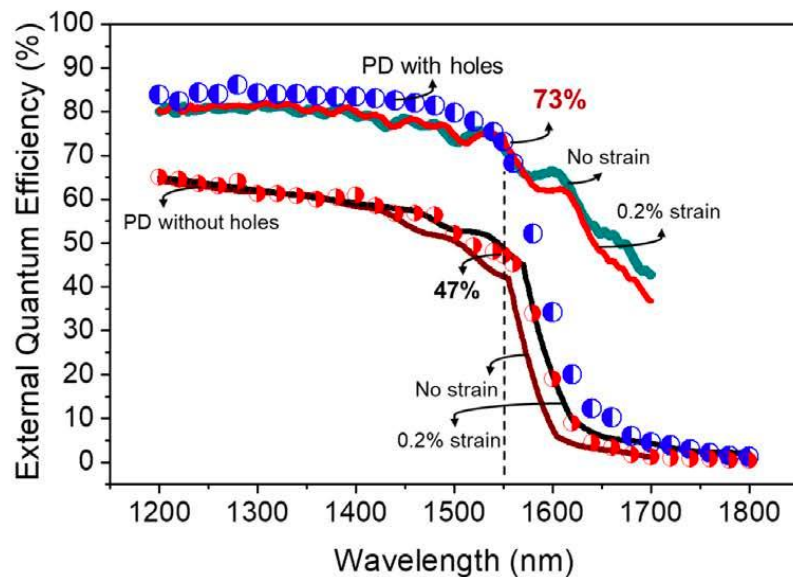
W&Wsens Devices Ge on Si PD with Microstructure Holes

- Large area PD surface illuminated
 - Single mode or multi mode fiber passive alignment
- Compatible with CMOS / BiCMOS processing
- No burying of Ge layer as in Ge waveguide PD
 - Simplified processing
 - Higher yield
- 2D array PD / APD / SPAD

Ge on Si Vertical PIN with Microstructure Holes

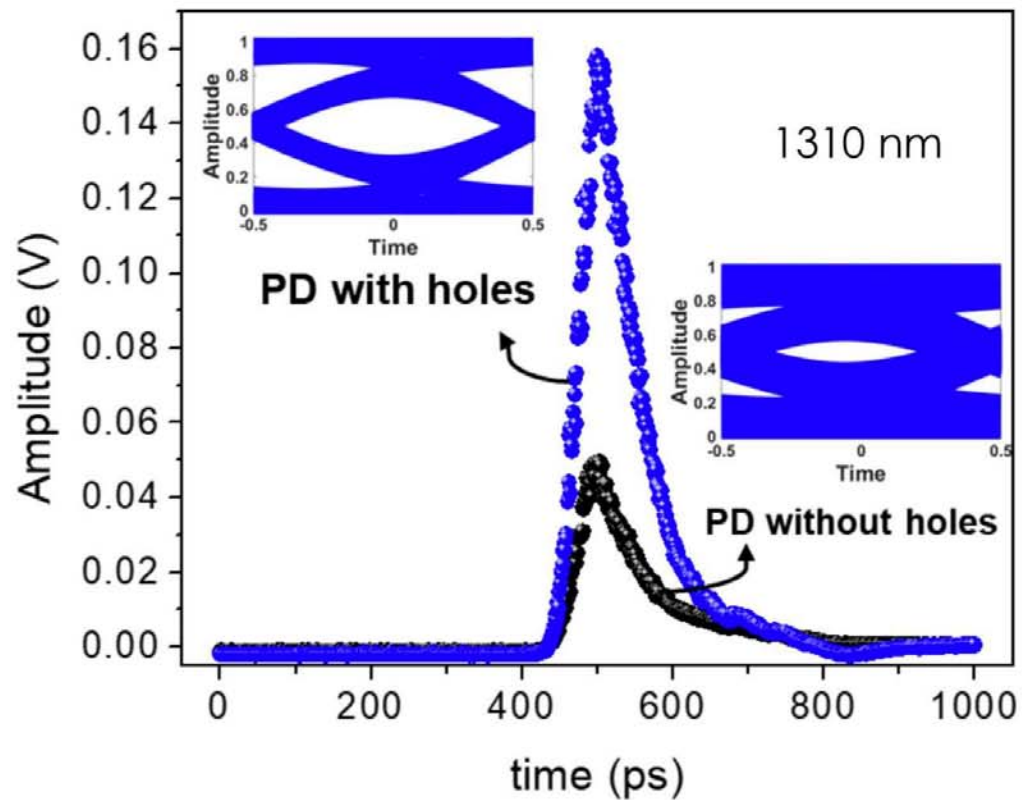
Ge on Si Vertical PIN With Microstructure holes

- Ge / GeSi on Si to extend wavelength to:
 - 900 – 1060 nm
 - 1250 – 1350 nm
 - 1550 nm

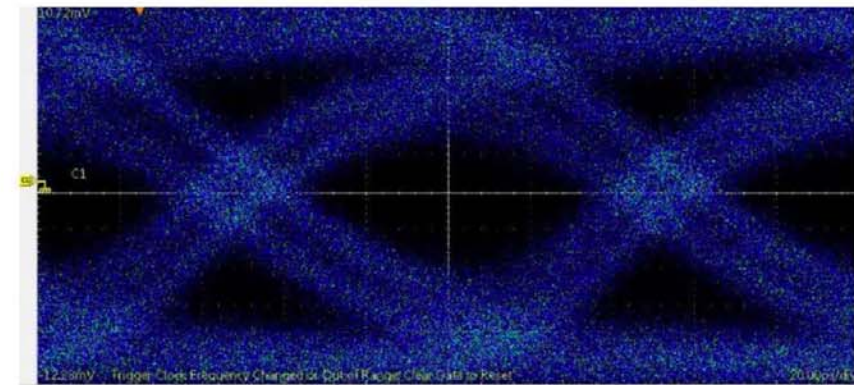


Ge on Si Microstructure Hole PD at 10Gb/s

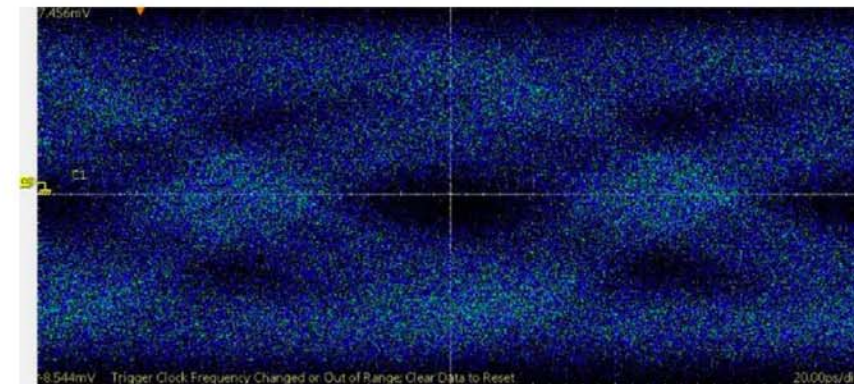
10 Gb/s



PD with holes



PD without holes



Ge on Si Vertical PIN

Compatible with CMOS / BiCMOS

Basic Fab steps

Ge on Si Vertical PIN

1. Starting material SOI



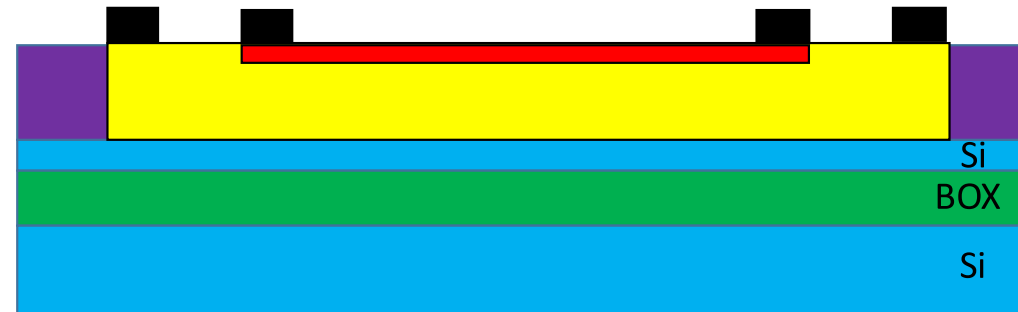
2. P and N wells

PMOS / NMOS retrograde implant



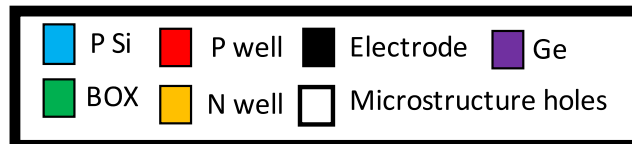
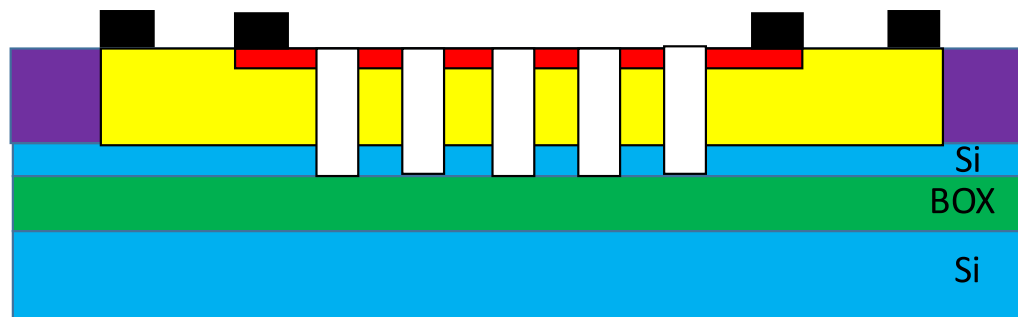
3. Interdigitated Electrodes

Interconnect metals



4. Etch microstructure holes

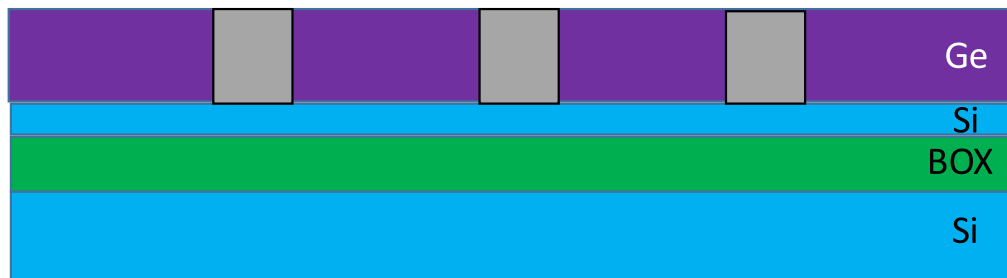
Trench etch



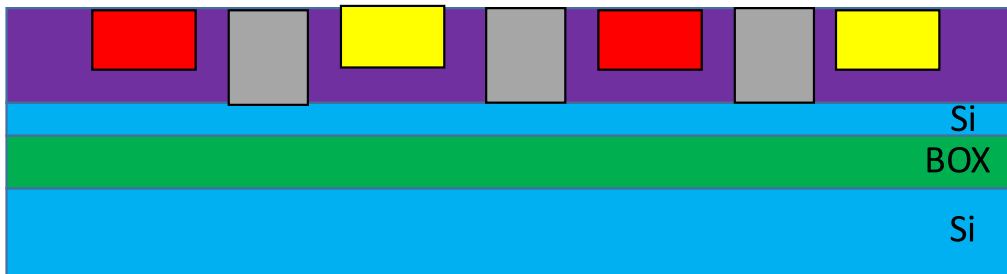
Ge on Si Lateral PIN with Microstructure Holes Basic Fab Steps

Ge on Si Lateral PIN

1. Selective area growth Ge on SOI / planarize

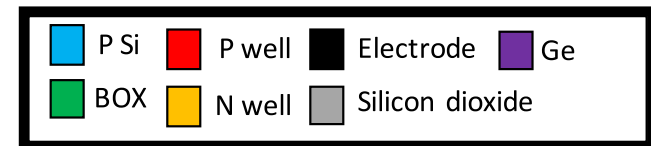
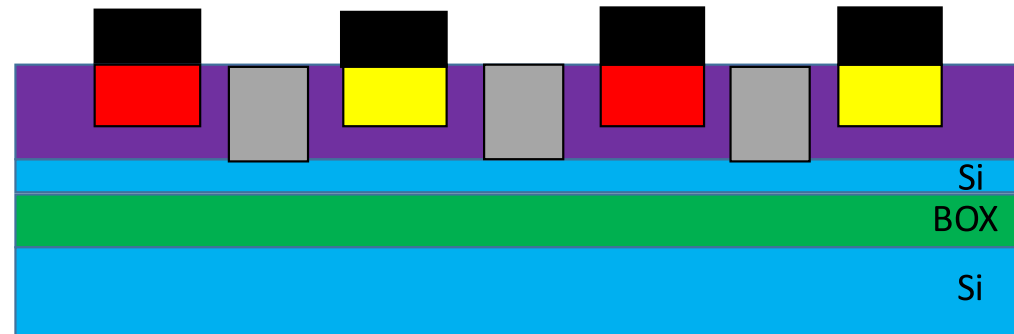


2. P and N wells
PMOS / NMOS



3. Interdigitated Electrodes

Interconnect metals



IBM Lateral Ge on SOI PD Results

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JOURNAL OF LIGHTWAVE TECHNOLOGY, VOL. 25, NO. 1, JANUARY 2007

Ge-on-SOI-Detector/Si-CMOS-Amplifier Receivers for High-Performance Optical-Communication Applications

Steven J. Koester, *Senior Member, IEEE*, Clint L. Schow, Laurent Schares, *Member, IEEE*, Gabriel Dehlinger, Jeremy D. Schaub, *Member, IEEE*, Fuad E. Doany, and Richard A. John

Abstract—In this paper, an overview and assessment of high-performance receivers based upon Ge-on-silicon-on-insulator (Ge-on-SOI) photodiodes and Si CMOS amplifier ICs is provided. Receivers utilizing Ge-on-SOI lateral p-i-n photodiodes paired with high-gain CMOS amplifiers are shown to operate at 15 Gb/s with a sensitivity of -7.4 dBm ($\text{BER} = 10^{-12}$) while utilizing a single supply voltage of only 2.4 V. The 5-Gb/s sensitivity of similar receivers is constant up to 93°C , and 10-Gb/s operation is demonstrated at 85°C . Error-free ($\text{BER} < 10^{-12}$) operation of receivers combining a Ge-on-SOI photodiode with a single-ended high-speed receiver front end is demonstrated at 19 Gb/s, using a supply voltage of 1.8 V. In addition, receivers utilizing Ge-on-SOI photodiodes integrated with a low-power CMOS IC are shown to operate at 10 Gb/s using a single 1.1-V supply while consuming only 11 mW of power. A perspective on the future technological capabilities and applications of Ge-detector/Si-CMOS receivers is also provided.

Index Terms—CMOS, germanium, optical receivers, photodetectors.

suggesting that the improved absorption properties of SiGe [5] and Ge [6] can be exploited for use in high-performance detectors. These facts, combined with the cost advantages of Si-based technology compared with III-Vs, suggest that CMOS-based high-performance optical receivers could have a dramatic impact on the wide-spread adoption of optical solutions for applications such as local-area networks [7], and could help to displace electrical links for short-distance high-speed network computing [8]. Additionally, CMOS-compatible integrated receivers are likely to be critical for the realization of future inter and intrachip optical communications [9].

In this paper, we provide an overview of our results on optical receivers that combine Ge-on-silicon-on-insulator (Ge-on-SOI) infrared detectors with CMOS IC amplifier circuits. We review the state-of-the-art Ge-detector research in Section II, specifically describing the advantages of our Ge-on-SOI detector approach, and also provide an overview of

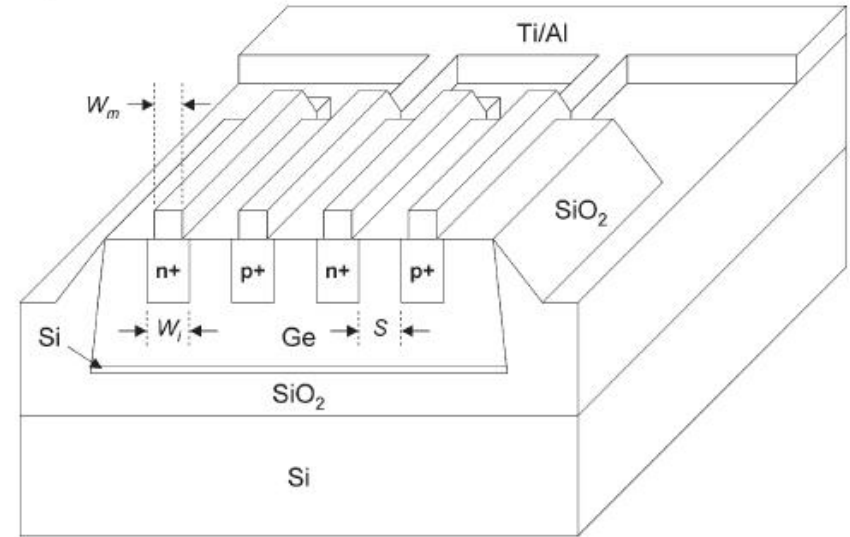


Fig. 1. Schematic diagram of Ge-on-SOI photodetector structure (not drawn to scale).

TABLE I
SIMULTANEOUS PERFORMANCE METRICS FOR Ge-on-SOI LATERAL p-i-n PHOTODIODES

Finger spacing (μm)	Bias voltage (V)	External QE at $\lambda = 850$ nm (%)	Responsivity at $\lambda = 850$ nm (A/W)	-3dB bandwidth (GHz)	Dark current (nA)	Detector area (μm^2)
0.4	-0.5	30	0.21	27	8	10×10
"	-1.0	"	"	29	85	"
0.6	-0.5	33	0.23	25	7	10×10
"	-1.0	"	"	27	24	"

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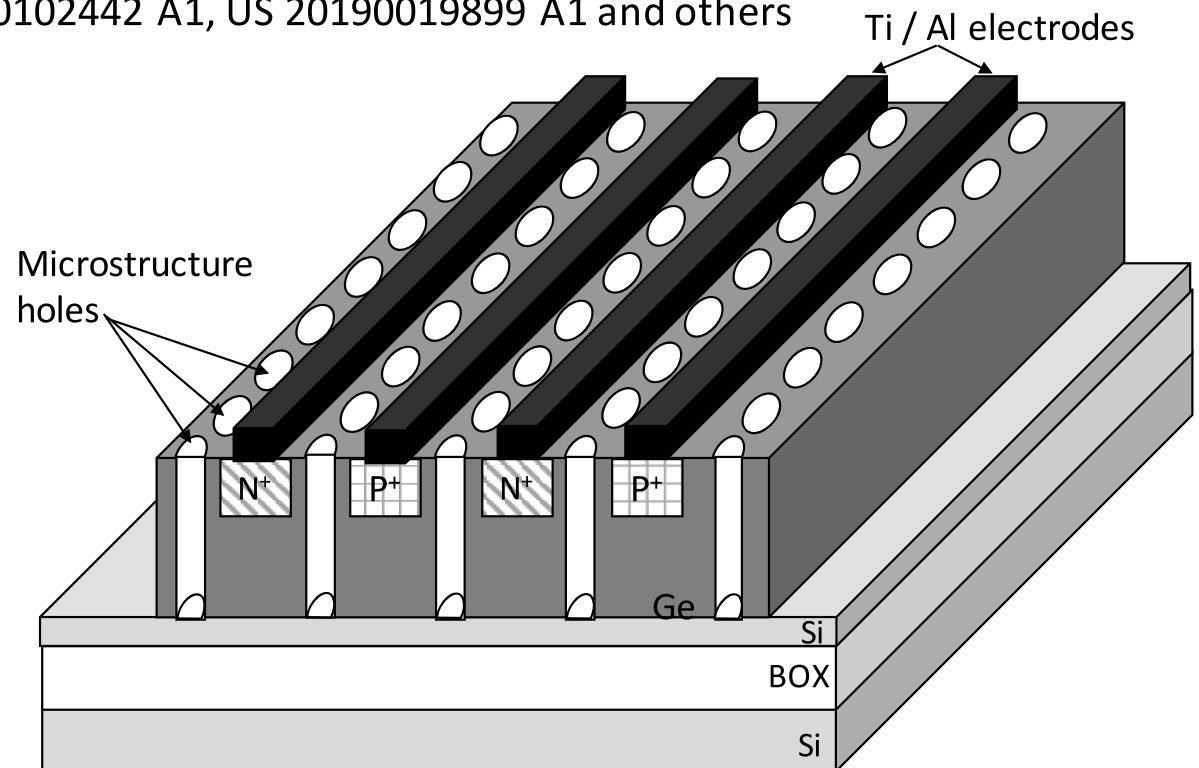
W&Wsens Devices

Lateral Ge on Si PIN Photodiode with Microstructure Holes

Covered by US 2018/0102442 A1, US 20190019899 A1 and others

250 nm Ge on SOI [same as IBM]
Estimated 70% EQE @ 1310 nm
Estimated 50% EQE @ 1550 nm
BW 43 – 58 Gb/s per channel
Wavelength 800 – 1650 nm

Ge on bulk Si
Wavelength 1100 nm – 1650 nm

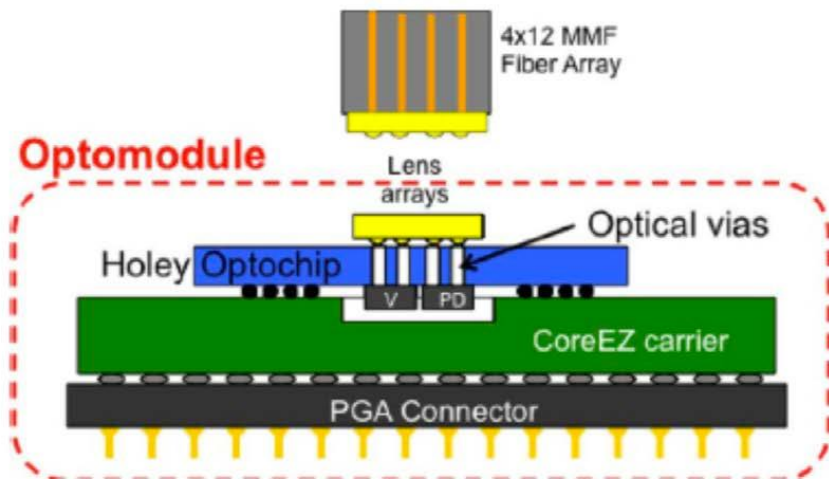


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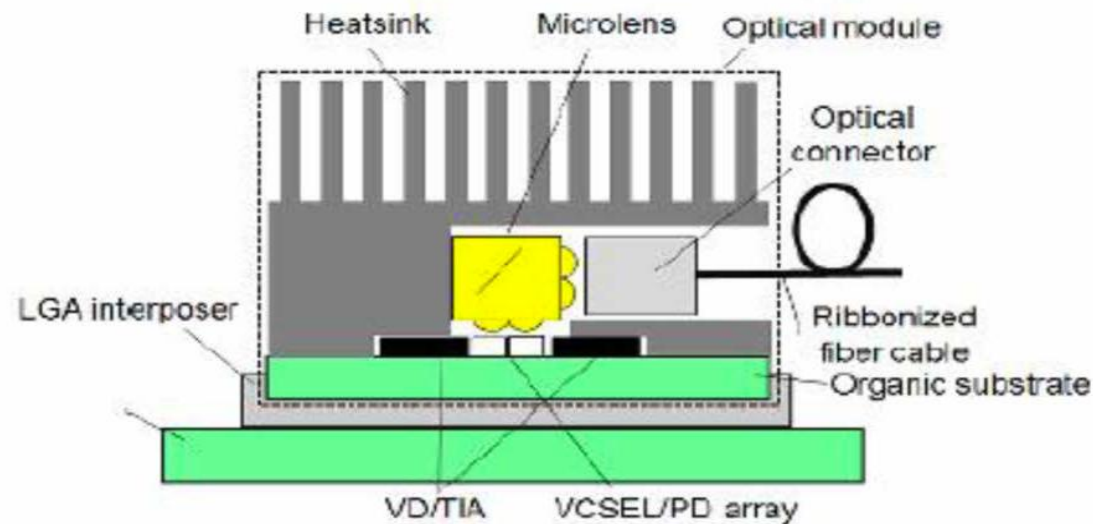
Appendix 2 – Optical Modules

Current Rx + Tx On Board Optical Module Assembly

IBM On Board Optical Module
48 Channels, 10 Gb/s per channel



Furukawa / Finisar On Board Optical Module
24 Channels, 28Gb/s per channel



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Tx + Rx SoCoB Final Step

W&Wsens Devices On Board Optical Module

Monolithically Integration Si PD Array with CMOS Electronics
Mounted Directly on PCB

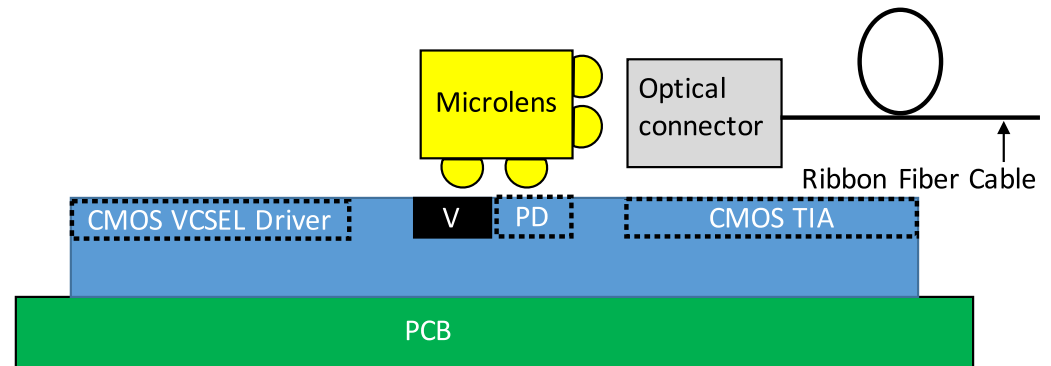
> 48 Channels

10 – 28 Gb/s per Channel

Aggregated Data Rate 480 Gb/s – greater than 1 Tb/s

VCSEL Array Self Assembly Wafer Scale Level

(1 Component)



Appendix 3 – Next Steps

W&Wsens Devices Inc.

Next Step – Monolithic Integration

- Significant cost reduction
- Improve performance with reduced parasitics
- Tower Jazz in discussion
- IHP in discussion
- Global Foundries next

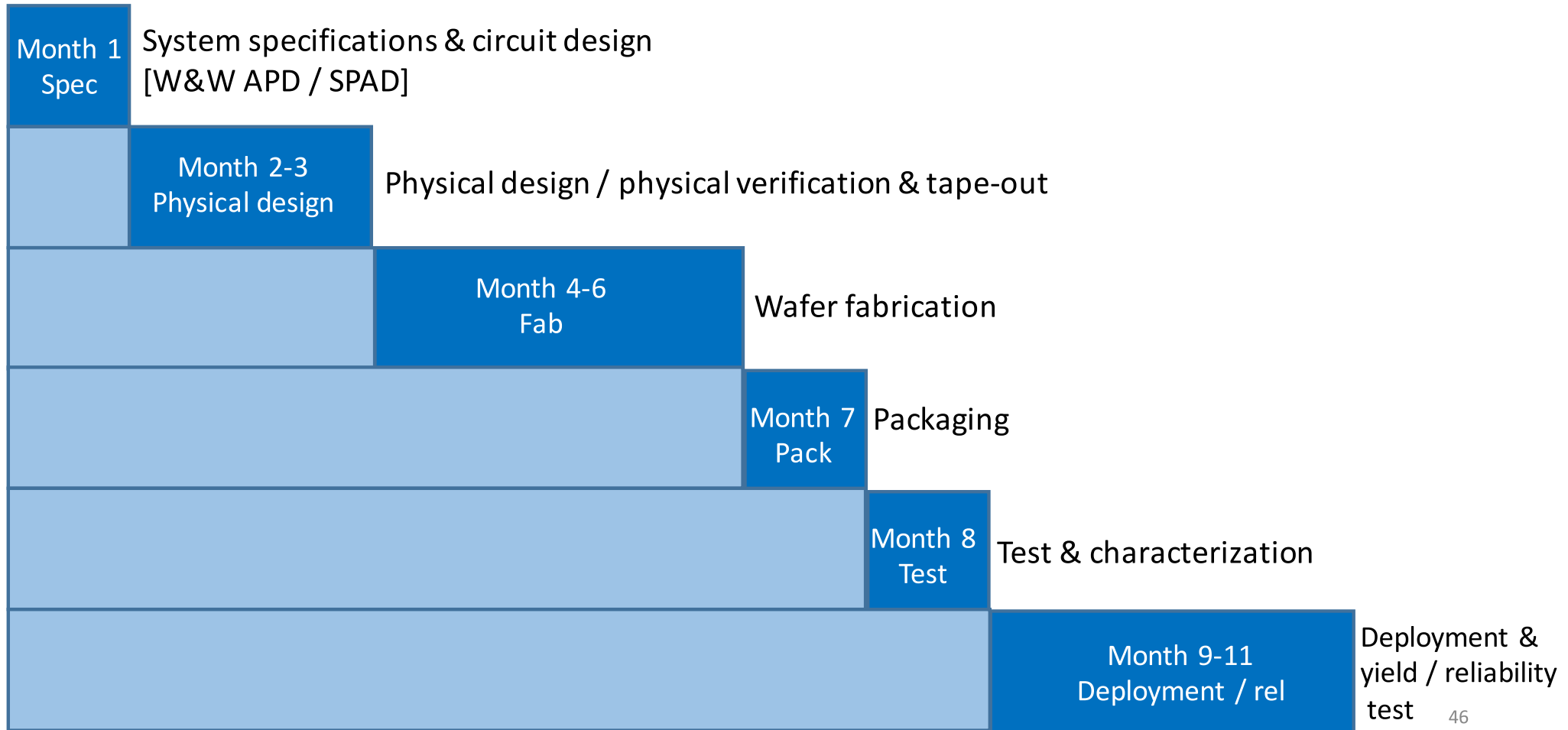
Time-to-Prototype

Single chip APD / SPAD Array & ASICs



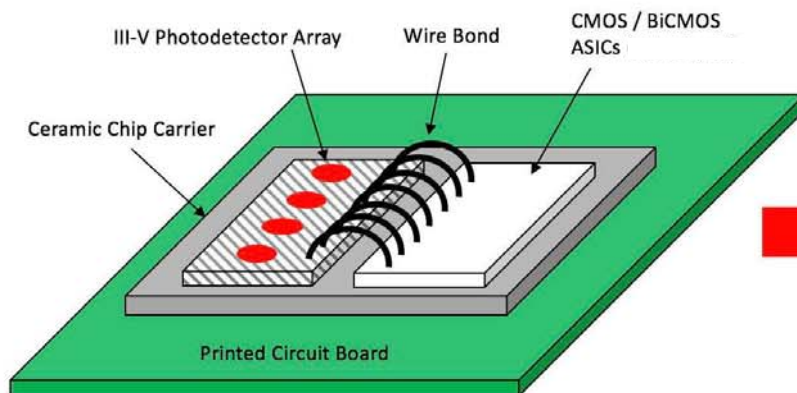
Time-to-Prototype

Monolithic Integrated APD / SPAD + ASICs

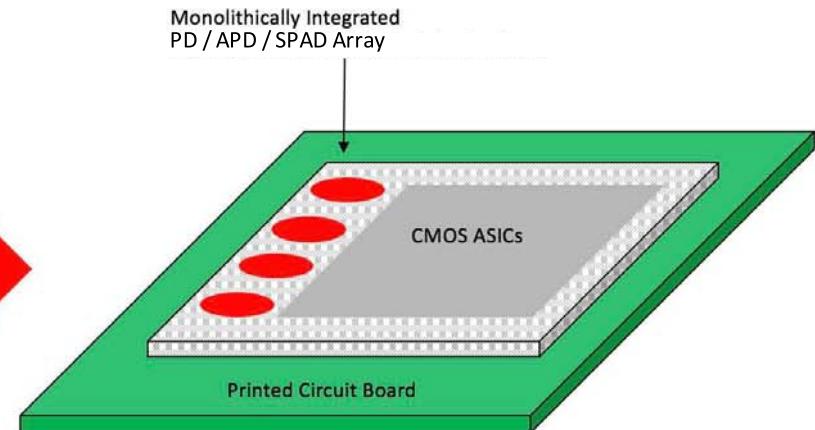


PD Array Integrated with ASICs

Existing Optical Receiver
3 components



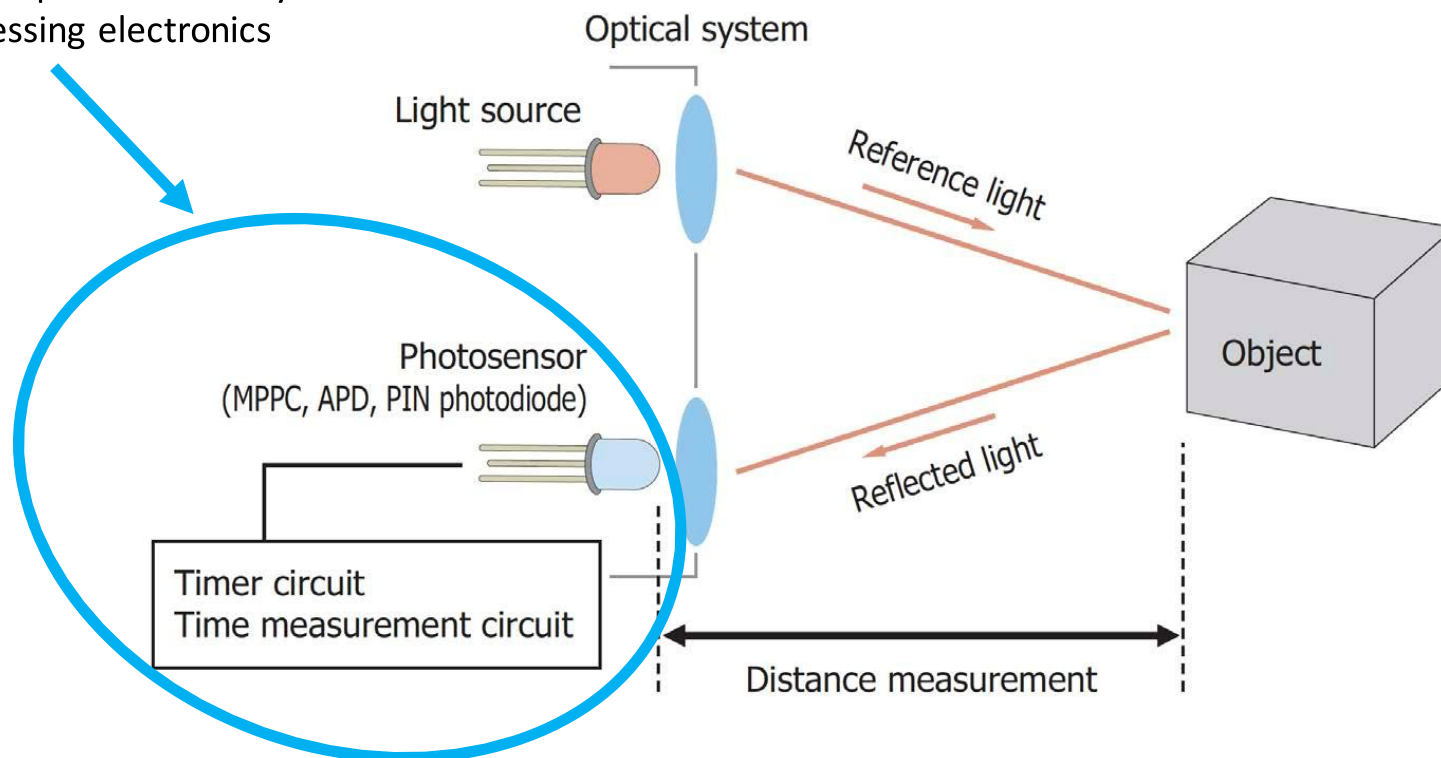
**Optical Receiver
with W&Wsens PD**
1 component



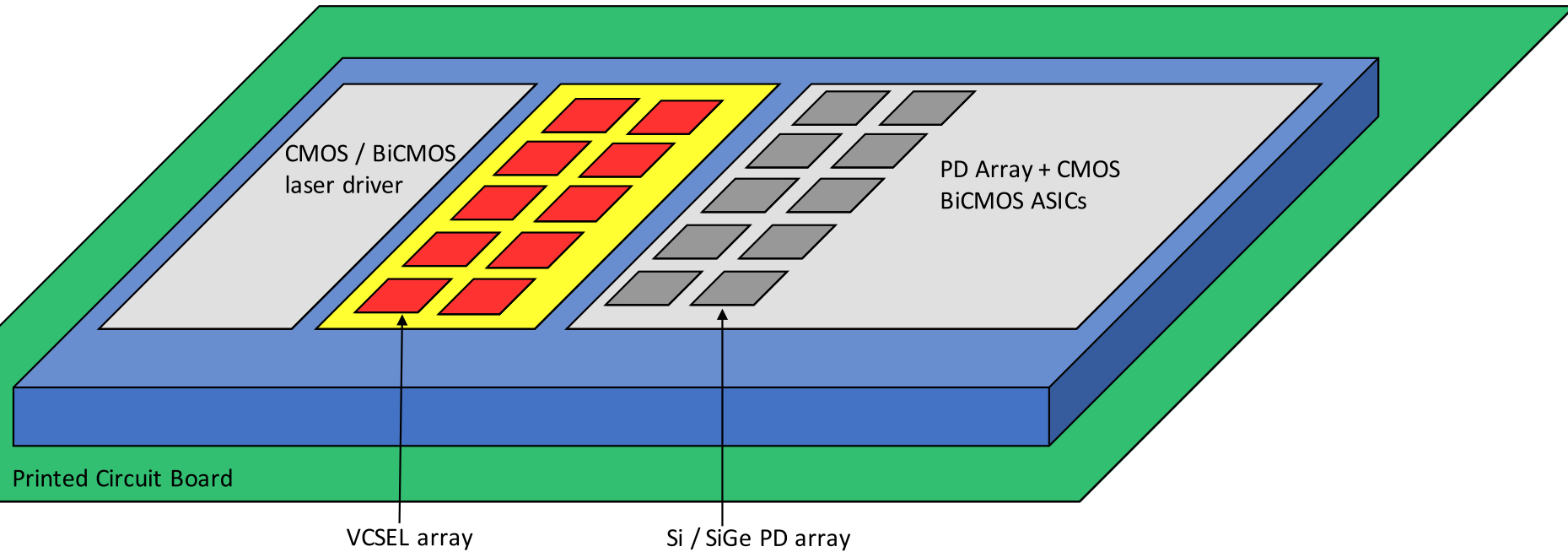
Wavelength Range: 850 nm – 1650 nm
Array Size: 100s – 1,000,000 channels
Cost Reduction & Improved Performance

W&W single chip solution

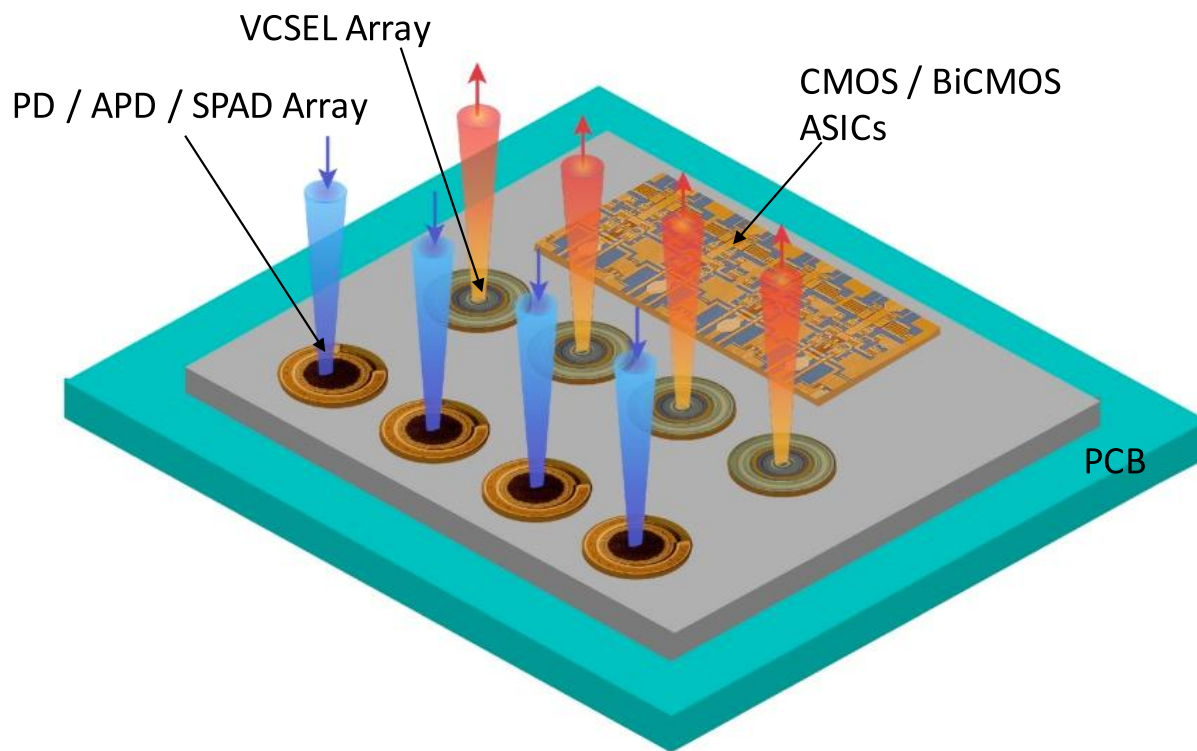
W&W single chip T-o-F PD array +
timing / processing electronics



W&Wsens Devices Inc. Disruptive Technology System-on-Chip-on-Board (SoCoB)



LiDAR Chip on PCB – Flash LiDAR with VCSEL array & high density PD / APD/ SPAD array



LiDAR applications using W&W technology

- W&W wavelength 850 nm, 905 nm , 940 nm, 1550 nm
- Flash LiDAR – short / medium range
- Scanning LiDAR / long range