

Petition for *Inter Partes* Review
U.S. Patent No. 7,557,788

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

Hisense USA Corporation
Petitioner

v.

Phenix Longhorn LLC
Patent Owner

Patent No. 7,557,788
Filing Date: May 1, 2007
Issue Date: July 7, 2009
Title: Gamma Reference Voltage Generator

Inter Partes Review No. IPR2025-01004

PETITION FOR *INTER PARTES* REVIEW

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EXHIBIT	DESCRIPTION
1001	U.S. Patent No. 7,557,788 (“the ’788 Patent”)
1002	Prosecution History of U.S. Patent No. 7,557,788
1003	Declaration of Rafael Betancourt
1004	Curriculum Vitae of Rafael Betancourt
1005	JP H06217239 to Nonomura (“Nonomura”)
1006	Certified Translation of Nonomura
1007	U.S. 2002/0063666 to Kang (“Kang”)
1008	JP H07152347 to Uehara (“Uehara”)
1009	Certified Translation of Uehara
1010	U.S. 2002/0036646 to Tobiya (“Tobiya”)
1011	<i>Phenix Longhorn, LLC v. AU Optronics Corporation et al.</i> , No. 2:23-cv-00477, Dkt. 67 (E.D. Tex.) – Docket Control Order
1012	<i>Phenix Longhorn, LLC v. AU Optronics Corporation et al.</i> , No. 2:23-cv-00477, Dkt. 120 (E.D. Tex.) – Joint Claim Construction and Prehearing Statement and Associated Exhibits

U.S. PATENT NO. 7,557,788 CLAIM LISTING

No.	Element
[1PRE]	1. A method of calibrating a liquid crystal display to a desired gamma curve to compensate for panel to panel manufacturing variations comprising the steps:
[1A]	a. providing said display with gamma reference control capability which is electrically reprogrammable and non-volatile;
[1B]	b. testing said display with at least one sensor with optical input, wherein said sensor is separate from said display;
[1C]	c. varying gamma reference voltage levels on columns of said display by a control circuit, wherein said control circuit is separate from said display;
[1D]	d. optimizing said gamma reference voltage levels using means for executing a predetermined algorithm according to a predetermined criteria and data sensed by said at least one sensor, wherein said means for executing said predetermined algorithm is separate from said display to achieve the desired gamma curve; and
[1E]	e. storing said gamma reference voltage levels in said gamma reference control capability.
2	2. The method of claim 1 wherein the method is repeated more than once under different ambient display conditions to generate at least one different set of gamma reference voltage levels stored in said gamma reference control capability.
[3PRE]	3. A method of programming one or more gamma reference voltage generator integrated circuits attached to a liquid crystal display comprising the steps:
[3A]	a. selecting one or more columns on said liquid crystal display;
[3B]	b. applying one or more different gamma voltages to said liquid crystal display columns;
[3C]	c. storing said applied gamma voltages in reprogrammable, nonvolatile cells in said gamma reference voltage generator integrated circuits appropriate to said selected columns;
[3D]	d. operating means for executing one or more optimization criteria algorithms based on optical emission corresponding to said selected columns, wherein said means for executing said one or more optimization criteria algorithms is separate from said liquid crystal display;

No.	Element
[3E]	e. modifying said one or more different applied gamma voltages based on said one or more optimization criteria algorithms
[3F]	f. programming said applied gamma voltages in storage cells in said gamma reference voltage generator integrated circuits appropriate to said selected columns; and
[3G]	g. repeating steps (d) through (f) until said one or more optimization criteria have been satisfied.
[5PRE]	5. A method for a liquid crystal display, comprising:
[5A]	providing said liquid crystal display with gamma reference control capability which is electrically reprogrammable and non-volatile;
[5B]	calibrating said liquid crystal display comprising: a. testing said liquid crystal display with at least one sensor with optical input;
[5C]	b. varying gamma reference voltage levels on columns of said liquid crystal display
[5D]	c. optimizing said gamma reference voltage levels using means for executing a predetermined algorithm according to a predetermined criteria and data sensed by said at least one sensor; and
[5E]	d. storing said gamma reference voltage levels in said gamma reference control capability
[5F]	retrieving said gamma reference voltage levels from said gamma reference control capability; and
[5G]	displaying an image on said liquid crystal display based on said gamma reference voltage levels.
6	The method of claim 5, wherein the calibrating step is repeated more than once under different ambient display conditions to generate at least one different set of gamma reference voltage levels stored in said gamma reference control capability.

I. Mandatory Notices (37 C.F.R. § 42.8(b))

A. Real Party-in-Interest (37 C.F.R. § 42.8(b)(1))

Petitioner Hisense USA Corporation is a subsidiary of the Hisense Group, which is organized under the laws of China. Other privies or real parties in interest of Petitioner include companies within the Hisense Group, including Hisense Visual Technology Co., Ltd and Hisense Mexico, S.A DE C.V.

B. Related Matters (37 C.F.R. § 42.8(b)(2))

U.S. Patent Number 7,557,788 (“the ’788 Patent”) is asserted against Petitioner in *Phenix Longhorn LLC v. AU Optronics Corp. et al.*, 1:23-cv-00477-RWS-RSP (E.D. Tex.) (the “Litigation”). The Litigation was filed by Patent Owner (PO) Phenix Longhorn on October 10, 2023 and Phenix served the Complaint on Hisense Visual Technology Corp. Ltd. on December 5, 2024, Hisense USA Corporation on October 16, 2024, and Hisense Mexico S.A. DE C.V. on May 15, 2024. The current schedule in the Litigation is attached as Exhibit 1011.

Past and/or pending IPRs against the ’788 Patent include:

- *Innolux Corporation v. Phenix Longhorn LLC*, IPR2025-00044 filed October 15, 2024 (pending)

Other related matters besides the Litigation involving the ’788 Patent include:

- *Phenix Longhorn, LLC v. Innolux Corporation*, No. 2:23-cv-00478 (E.D. Tex. Filed Oct. 10, 2023)

- *Phenix Longhorn, LLC v. Samsung Electronics Co. Ltd et al.*, No. 2:24-cv-01077 (E.D. Tex. Filed Dec. 30, 2024)

C. Designation of Lead and Backup Counsel (37 C.F.R. § 42.8(b)(3)) and Service Information (37 C.F.R. § 42.8(b)(4)).

<u>Lead Counsel</u>	<u>Backup Counsel</u>
Matias Ferrario Reg. No. 51,082 1001 W. 4 th Street Winston-Salem, NC 27101 Office: 336.607.7475 Fax: 336.734.2651 MFerrario@kilpatricktownsend.com	Michael T. Morlock Reg. No. 62,245 1100 Peachtree St. NE, Suite 2800 Atlanta, GA 30309-4528 Office: 404.815.6003 Fax: 336.734.2756 MMorlock@kilpatricktownsend.com

Petitioner may be served at the email addresses above.

II. Introduction

The '788 Patent's claims recite little more than routine methods for calibrating liquid crystal displays commonly used well before the earliest priority date of the '788 Patent. Gamma correction, the process that adjusts brightness of a display to provide a more pleasing picture, was employed in display technology for years. And although PO relies on the fact that its purported invention used novel *analog* gamma reference voltage levels, PO never claimed such "analog" signals. Moreover, analog gamma correction was known in the art as evidenced by one of the primary references here, which teaches both analog and digital gamma correction. Ex. 1006, ¶¶6-11; Ex. 1003, ¶38.

III. IPR Requirements

A. Standing (37 C.F.R. § 42.104(a))

Petitioner certifies that the '788 Patent is available for IPR and that Petitioner is not barred or estopped from requesting IPR. The '788 Patent issued on July 7, 2009, and this Petition is filed within one year of service of the Complaint against Petitioner alleging infringement of the '788 Patent and is not barred under 35 U.S.C. §315(b).

B. Fees (37 C.F.R. § 42.103)

This Petition requests review of five (5) claims of the '788 Patent and is accompanied by a payment of \$51,875, which includes the \$23,750 IPR request fee, and the \$28,125 post-institution fee. This Petition meets the fee requirements under 35 U.S.C. § 312(a)(1). The Board is hereby authorized to charge any additional fees required by this action to Deposit Account No. 20-1430.

C. Challenge Under 37 C.F.R. § 42.104(b)

This petition requests cancellation of claims 1-3 and 5-6 as obvious under 35 U.S.C. § 103 based on the following:

- JP H06217239A to Nonomura (“Nonomura”) (Exs. 1005-1006)
- JP H07152347A to Uehara (“Uehara”) (Exs. 1008-1009)
- US 20020063666A1 to Kang (“Kang”) (Ex. 1007)
- US20020036646A1 to Tobiya (“Tobiya”) (Ex. 1010)

The statutory grounds for the challenge are set forth below:

Ground	35 U.S.C.	Claims	References
1	103	1-3 and 5-6	Nonomura in view of Kang
2	103	1-3 and 5-6	Uehara in view of Kang
3	103	1 and 3	Tobiya in view of Kang

IV. Background

A. '788 Patent

The '788 Patent was filed on May 1, 2007 and issued on July 7, 2009. The '788 Patent describes a method for calibrating LCDs to achieve a target gamma curve purportedly to address manufacturing inconsistencies between different displays. Ex. 1001, Abstract. This method incorporates gamma reference control functionality that is both electrically reprogrammable and non-volatile. Ex. 1001, 2:17-28.

The '788 patent purports to describe testing the display using an external optical sensors that is separate from the display. Ex. 1001, 6:38-56, Fig. 2. A control circuit, distinct from the display, manipulates gamma reference voltage levels on the display columns. Ex. 1001, 3:6-12, Fig. 2. The method fine-tunes these voltage levels by employing a predetermined algorithm that processes sensor data and predefined criteria. Ex. 1001, 6:48-56, Fig. 2. Once optimized, the gamma reference voltage levels are stored. Ex. 1001, 3:24-28.

B. Prosecution of the '788 Patent.

The '788 application was originally filed with claims 1-6. In a non-final office action, the Examiner rejected claims 1, 3, 4, and 5 under 35 U.S.C. 103(a), citing U.S. Patent No. 6,593,934 ("Liaw"). Ex. 1002, 94. The Examiner rejected claims 2 and 6 under 35 U.S.C. 103(a), citing Liaw and U.S. Patent No. 5,754,150 ("Matsui"). Ex. 1002, 97. The Examiner noted that the only limitation missing from the prior art was the explicit teaching that the storage of the gamma reference voltage levels was not explicitly described as "non-volatile". *Id.*, 96. The Applicant responded by amending independent claim 5 to delete "wherein said means for executing said predetermined algorithm is not required subsequent to the calibrating step." Ex. 1002, 73. On March 5, 2009, the Examiner issued a notice of allowance.

V. Expert Testimony, Level of Skill in the Art, and Claim Construction

A. Declaration Evidence

This petition is supported by the declaration of Rafael Betancourt, Eng. D., an expert with extensive experience in the relevant industry. Exs. 1003-1004. As former Director of Analog Mixed-signal Systems and Verification at Synaptics, Inc., and as outlined in his declaration, Dr. Betancourt has experience in many aspects of LCD display technology, including the design and verification of analog mixed signal electrical circuitry for monolithic touch and LCD display controllers ("TDDI") used in various display technologies (e.g., Amorphous, LTPS, IGZO, etc.). Ex. 1003.

B. Person of Ordinary Skill in the Art (POSITA)

A POSITA would have at least a bachelor of science degree in physics, electrical engineering, or the equivalent thereof and three (3) years of experience in circuit design or display technology ... [and] would have had knowledge of integrated circuits, gamma correction, and storage of gamma correction voltage values within memory, and would have understood how to search available literature for relevant publications.

C. Claim Construction

The '788 Patent does not expressly define any claim term that is of consequence to this Petition. For purposes of this proceeding only, Petitioner believes that each term may be given its plain and ordinary meaning and that no claim term requires construction subject to the discussion below.

Petitioner and PO have taken specific positions on claim construction in the Litigation. *See* Ex. 1012. To the extent not indefinite, Petitioner believes that the alternative constructions proposed by Petitioner and the proposed construction by PO have no bearing on the prior art at issue here and thus that under either proposed constructions, the challenged claim elements are present in the prior art.

More particularly, to the extent not indefinite, Petitioner believes that the term “gamma reference control capability” should be construed according to 35 U.S.C. § 112, ¶6. This term’s function is programming and storing gamma reference voltage

values in storage cells that are used to generate gamma reference voltage outputs and switching between different gamma settings to implement dynamic gamma correction. The corresponding structure is disclosed in Figs. 2, 3, and 5, or Figs. 6 and 5, or equivalents thereof.

To the extent not indefinite, Petitioner believes that the term “control circuit” should be construed according to 35 U.S.C. § 112, ¶6. This term’s function is varying gamma reference voltage levels on columns of a display. The corresponding structure is Figs. 2 and 3, or Fig. 6, or equivalents thereof.

To the extent not indefinite, Petitioner believes that the “means for executing a predetermined algorithm according to a predetermined criteria and data sensed by said at least one sensor” and similar elements in claims 3 and 5 should be construed according to 35 U.S.C. § 112, ¶6. This term’s function is the execution of an algorithm that optimizes gamma reference voltage levels based on (1) data sensed by at least one sensor and (2) the application that is being displayed, external environment such as temperature and ambient light, or the personal preference of the user. Corresponding structure is Fig. 2 or Fig. 6, or the structure disclosed in col. 6:57-64, or equivalents thereof.

Finally, the term “gamma reference voltage level” would be understood by a person of ordinary skill in the art to include both analog and digital signals. As explained, the prior art discloses this claim term.

VI. Prior Art

A. Nonomura

Nonomura was filed on January 15, 1993, and published on August 5, 1994, and thus is prior art under at least 35 U.S.C. §102(a).

Nonomura describes a liquid crystal projector having a gamma correction function that will perform gamma correction according to the correction data based on the results of the measurement of the applied voltage-transmittance characteristics. Ex. 1006, ¶14.

B. Uehara

Uehara was filed on November 29, 1993, and published on June 16, 1995, and thus is prior art under at least 35 U.S.C. §102(a).

Uehara discloses a gamma correction method for a liquid crystal display. Ex. 1009, ¶1. The light transmittance of an LCD panel to which voltage is applied is measured, and the gamma characteristics of the LCD panel are then determined and corrected based on the measured light transmittance. Ex. 1009, ¶7.

C. Kang

Kang was filed on June 28, 2001, and published on May 30, 2003, and thus is prior art under at least 35 U.S.C. §102(a).

Kang describes an LCD that includes the digital video card 81, the multi-mode gamma voltage generator 84, the column driver 83 for supplying data to data lines

of the liquid crystal panel 86, the row driver 85 for sequentially driving gate lines of the liquid crystal panel 86, and the controller 82 for controlling the column driver 83 and the row driver 85. Ex. 1007, ¶48. The multi-mode gamma voltage generator 84 stores therein gamma data and divides, by utilizing the selected gamma data, a gamma voltage into a gray level range to be displayed and applies it to the column driver 83. *Id.*, ¶49.

D. Tobiya

Tobiya was filed on June 18, 2001, and published on March 28, 2002, and thus is prior art under at least 35 U.S.C. §102(a).

Tobiya describes a display characteristic correction system that includes a liquid crystal display 100 and a means for correcting the gray level. Ex. 1010, ¶36. Tobiya explains that the gray level relates to luminance. Ex. 1010, ¶4. The input value of the signal and the gray level value associate with a characteristic inherent to the display device. *Id.* Tobiya converts the input signal by using a “correction characteristic” to allow the device to display a gray level that is linear with the input signal. *Id.*

VII. Full Statement of the Reasons for the Relief Requested

A. Ground 1 – Claims 1-3 and 5-6 are Obvious Under 35 U.S.C. § 103 Over Nonomura in view of Kang and further in view of the Knowledge of a POSITA.

1. Motivation to Combine Nonomura and Kang.

A combination of familiar elements according to known methods which yields no more than predictable results is likely obvious to a POSITA. There are several rationales that can support a conclusion of obviousness, including using a known technique to improve similar methods in the same way (MPEP 2143(C)), modifying a known technique to a known method by finding that the prior art contained a known technique applicable to the base method (MPEP 2143(D)), and substituting one known element for another to obtain a predictable result (MPEP 2143(B)). Each of these rationales, among others, can support a conclusion of obviousness, which are consistent with the “functional approach” to obviousness set forth in the Supreme Court’s precedent. *See, KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 415-421 (2007).

A POSITA would have been motivated to combine Nonomura and Kang. Both Nonomura and Kang are in the same field of endeavor, i.e., gamma correction. Ex. 1003, ¶78. Consequently, a POSITA would have had a reasonable expectation of success in combining their various disclosures to achieve, for example, (i) desired gamma correction in the real state in which an LCD panel has been mounted and (ii) improved display quality. Ex. 1003, ¶78.

Furthermore, it was well within the ability of a POSITA to incorporate the column driver and corresponding column configuration described in Kang into the display described in Nonomura because a POSITA at the time would have known how to arrange an LCD into columns and rows for accessing individual pixels. Ex. 1003, ¶79.

It was also well within the ability of a POSITA to incorporate the multi-mode gamma voltage generator for generating a gamma voltage using Kang's multi-mode gamma data set into Nonomura's liquid crystal projector because (i) using multiple modes was well known to a POSITA as of the earliest claimed priority date in the gamma correction field to accommodate different display conditions and use cases and (ii) a POSITA would be motivated to do so to achieve versatility and functionality within the display. Ex. 1003, ¶80.

It was well within the technical ability of a POSITA to design a display where Nonomura's non-volatile cells correlate to appropriate columns using Kang's teachings of column drivers, which a POSITA would understand correlates non-volatile cells with their corresponding columns. Ex. 1003, ¶81.

Thus, combining Nonomura and Kang would have been obvious to a POSITA. Ex. 1003, ¶81.

2. Independent Claim 1.

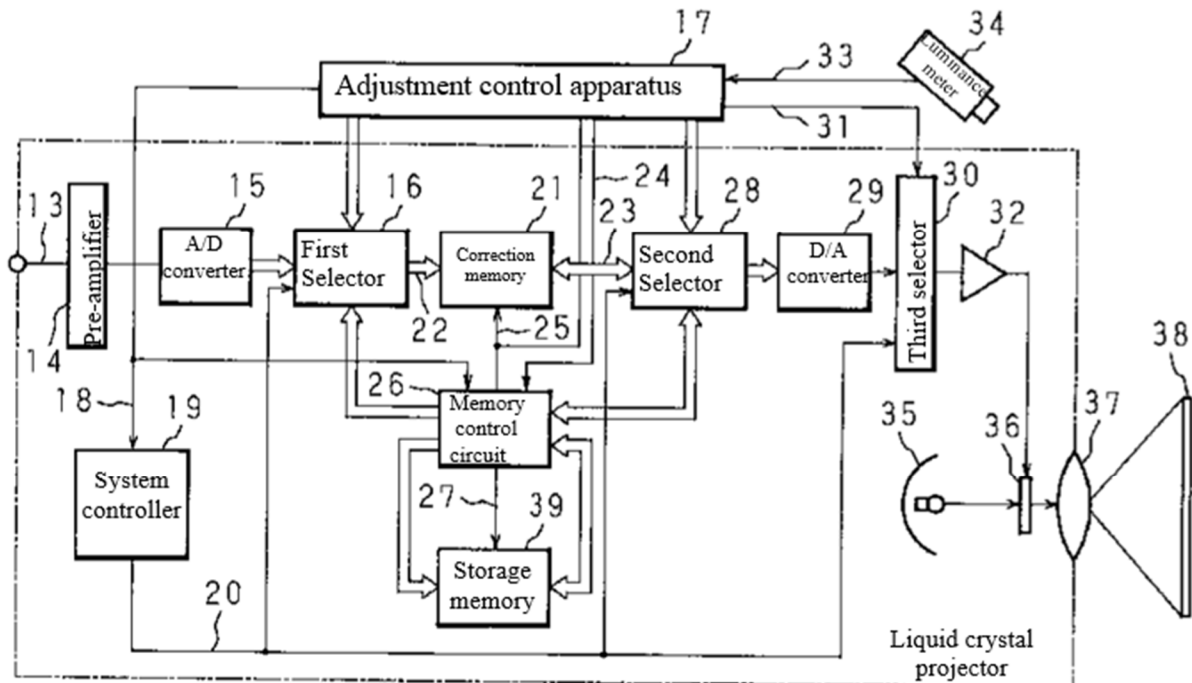
[IPRE]:

Nonomura describes a liquid crystal projector having a gamma correction function that will perform gamma correction according to the correction data based on the results of the measurement of the applied voltage-transmittance characteristics. Ex. 1006, ¶14. As explained in Nonomura, this is generally referred to as gamma correction. Ex. 1006, ¶¶3-4; Ex. 1003, ¶82.1.

Nonomura teaches that the applied voltage-transmittance characteristics of LCD panels depend on various factors that vary panel-to-panel. Ex. 1006, ¶¶12-13. Nonomura highlights the need for performing gamma correction “according to the individual characteristics in the state in which the LCD panel has actually been mounted.” Ex. 1006, ¶13. A POSITA would appreciate that such individualized gamma correction is for compensating for inter-panel manufacturing variations. Ex. 1003, ¶82.2.

[IA]:

Nonomura describes an LCD panel 36 and a screen 38, where the image displayed on the LCD panel 36 is projected by a light source 35 and enlarged by projection lens 37 for projection onto screen 38. Ex. 1006, ¶20, FIG. 1. A POSITA would understand that the operation principles of Nonomura’s system remain the same, regardless of using the projection or not. Ex. 1003, ¶82.3.



Id., Fig. 1.

The memory control circuit 26 is able to exchange data with the non-volatile storage memory 39, and data can be written to or read from the non-volatile storage memory. Ex. 1006, ¶25. The non-volatile storage memory 39 can retain correction data even if the power supply is interrupted. Ex. 1006, ¶34. The correction data stored in the non-volatile storage memory 39 is read for transfer to the correction memory 21 via the second selector 28, and the data is then written to the correction memory 21. Ex. 1006, ¶34.

Thus, a POSITA would appreciate that Nonomura discloses “providing said display with gamma reference control capability” (the basic circuit comprising the non-volatile storage memory 39, the correction memory 21, the memory control

circuit 26, and optionally the D/A converter 29 and the buffer 32), and such gamma reference control capability is electrically reprogrammable (being able to write data to the memory) and non-volatile (non-volatile storage memory). Ex. 1003, ¶82.5.

[1B]:

The adjustment control apparatus 17 is connected to the luminance meter 34, which measures the luminance of the image on the screen 38 and inputs the measurement data 33 to the adjustment control apparatus 17 for calibrating the LCD panel 36. Ex. 1006, ¶23. A POSITA would appreciate that the luminance meter 34 is a sensor and the luminance of the image is the optical input. Ex. 1003, ¶82.6.

The range enclosed by the dashed line in FIG. 1 is a basic circuit, and the adjustment control apparatus 17 and the luminance meter 34 “have been added to this circuit.” Ex. 1006, ¶19. Thus, Nonomura discloses said sensor (the luminance meter 34) is separate from said display (outside the range enclosed by the dashed line). Ex. 1003, ¶82.7.

[1C]:

Nonomura describes three operation modes. Ex. 1006, ¶16. In one mode, the adjustment control device 17 changes the voltage of the DC level voltage signal 31 in a predetermined manner while having the luminance of the screen measured, as the measurement data 33, with the luminance meter 34 at each voltage. *Id.*, ¶27. Consequently, the applied voltage-transmittance characteristics of the LCD panel 36

is obtained by the adjustment control device 17. *Id.* A POSITA would comprehend that this mode is a “display characterization mode” where the applied voltage-transmittance characteristics of the LCD panel is obtained. Ex. 1003, ¶82.8.

In another mode, the adjustment control apparatus 17 prepares the correction data for the output data corresponding to the input data to ensure that the video signal is gamma-corrected based on the measurement data 33. Ex. 1006, ¶28. A POSITA would comprehend that this mode is a “gamma correction mode” where the input video signal is gamma-corrected according to the measured applied voltage-transmittance characteristics in the previous “display characterization mode” and the measurement data 33. Ex. 1003, ¶82.9.

The adjustment control device 17 sends the system control signal 18 to the system controller 19, which generates the mode switching signal 20 to control the operation of the selectors 16, 28, and 30 accordingly. Ex. 1006, ¶¶22-23. During the gamma correction operation, the correction memory 21 and the adjustment control apparatus 17 are connected, and the address signal 22 and the data signal 23 are written in the correction memory 21 according to the first memory control signal 25 received from the adjustment control apparatus 17. *Id.* ¶29. A POSITA would understand that Nonomura discloses a “control circuit” (the adjustment control apparatus 17, which interacts with the system controller 19, sends the system control

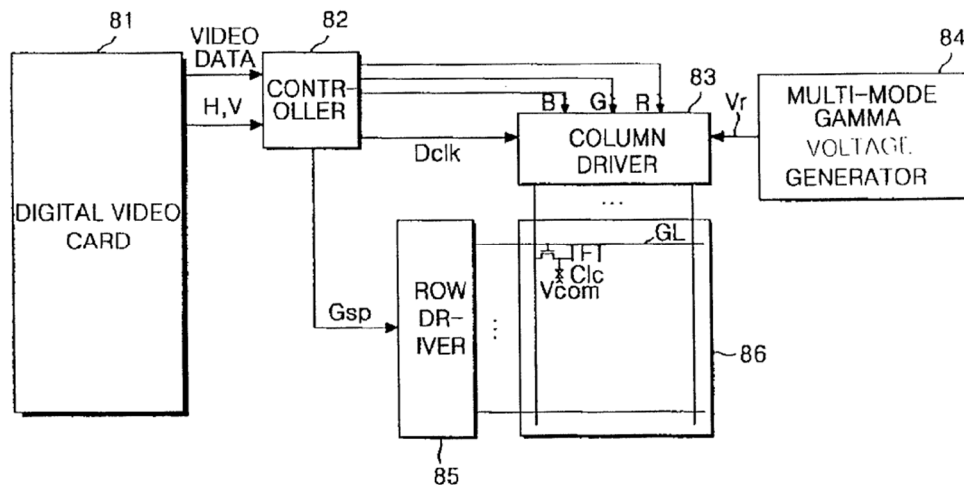
signal 18, and controls the correspondence between the address signal 22 and the data signal 23). Ex. 1003, ¶82.10.

When the writing of the correction data corresponding to *each address* in the correction memory 21 is completed in this way, the adjustment control device 17 outputs the system control signal 18 to change the mode switching signal 20. Ex. 1006, ¶30. The video signal input 13 is converted according to the gamma correction data in the correction memory 21 before being *converted back to an analog signal by the D/A converter 29*, which is input into the LCD panel 36 via the buffer 32. Ex. 1006, ¶31. A POSITA would appreciate that Nonomura discloses “varying gamma reference voltage levels” (varying, across various addresses, the analog signal output by the D/A converter 29) “on ... said display” (applied to the LCD panel via the buffer 32). Ex. 1003, ¶82.11. The gamma-corrected data in the correction memory 21 (and/or the non-volatile storage memory 39), the analog signal output by the D/A converter 29, and the analog signal in the buffer 32 are essentially the same, putting aside the D/A conversion and despite seemingly different representations (digital v. analog) and locations. Ex. 1003, ¶82.11.

To the extent that Nonomura fails to disclose “on columns of” said display, Kang does.

Kang describes an LCD that includes the digital video card 81, the multi-mode gamma voltage generator 84, the column driver 83 for supplying data to data lines

of the liquid crystal panel 86, the row driver 85 for sequentially driving gate lines of the liquid crystal panel 86, and the controller 82 for controlling the column driver 83 and the row driver 85. Ex. 1007, ¶48. The multi-mode gamma voltage generator 84 stores therein gamma data and divides, by utilizing the selected gamma data, a gamma voltage into a gray level range to be displayed and applies it to the column driver 83. *Id.*, ¶49. The column driver 83 latches the digital video data received from the controller 82 and thereafter corrects the latched data based on a gamma voltage from the gamma voltage generator 84. *Id.*, ¶50. The column driver 83 converts the data corrected by the gamma voltage into analog data to apply it to the data lines. Ex. 1007, ¶50.



Id., Fig. 8.

Thus, Kang discloses applying gamma reference voltage levels on columns of the display (the liquid crystal panel 86) by using the column driver 84. Ex. 1003, ¶82.15. A POSITA would be motivated to modify Nonomura's systems to vary the

gamma reference voltage levels on its columns of the LCD panel 36 in light of the teachings of Kang. Ex. 1003, ¶82.15. Arranging an LCD into columns and rows for accessing individual pixels was well known to a POSITA as of the earliest claimed priority date. Ex. 1003, ¶82.15.

[ID]:

As articulated *supra*, in the “gamma correction mode,” the adjustment control apparatus 17 prepares the correction data for the output data corresponding to the input data to ensure that the video signal is gamma-corrected based on the measurement data 33. Ex. 1006, ¶¶14, 28; Ex. 1003, ¶82.16. The input data signal 23 is sent from the correction memory 21 to the D/A converter 29. A POSITA would comprehend the gamma correction process in the “gamma correction mode” is “optimizing said gamma reference voltage levels” (optimizing the output signal of the D/A converter 29). Ex. 1003, ¶82.16. Again, the gamma-corrected data in the correction memory 21 (and/or the non-volatile storage memory 39) and the analog signal output by the D/A converter 29 are different but equivalent representations in different domains (digital v. analog). Ex. 1003, ¶82.16.

A POSITA would appreciate that this optimization process is “using means for executing a predetermined algorithm according to a predetermined criteria and data sensed by said at least one sensor” because (i) the luminance meter 34 is used and (ii) the “gamma count specific to the LCD panel 36” is a predetermined criteria.

Ex. 1006, ¶27, Ex. 1003, ¶82.17. It was well known to a POSITA as of the earliest claimed priority date in this field that the optimization process involves “a predetermined algorithm” (the matching/fitting to a certain desired gamma curve) for the algorithm/software aspect and at least one sensor for the hardware aspect. Ex. 1003, ¶82.17. It is also common knowledge of a POSITA that the “predetermined algorithm” must be executed by “means for executing ...” such as the adjustment control apparatus 17. Ex. 1003, ¶82.17.

Moreover, Nonomura teaches that the adjustment control apparatus 17 and the luminance meter 34 “have been added to this circuit.” Ex. 1006, ¶19. A POSITA would appreciate that this means is separate from said display. Ex. 1003, ¶82.18.

[1E]:

Nonomura describes that the adjustment control apparatus 17 adjusts the gamma correction data, which is then written to the correction memory 21. Ex. 1006, ¶32. The correction data may be modified and rewritten to the correction memory as needed. *Id.* After the “gamma correction mode,” the adjustment control apparatus 17 sends the store signal 24 to the memory control circuit 26, and the memory control circuit 26 provides the address signal to the correction memory 21 to read the gamma correction data and provides the address signal and the second memory control signal 27 to the non-volatile storage memory 39 to write the data to the non-volatile storage memory 39. Ex. 1006, ¶33. Thus, a POSITA would understand that

Nonomura discloses storing the “gamma reference voltage levels” (storing the gamma correction data is equivalent to storing the output signal of the D/A converter 29 as they are simply different representations of the same signal) in the “gamma reference control capability” (the basic circuit comprising, among other components, the non-volatile storage memory 39). Ex. 1003, ¶82.19. Indeed, A/D conversion (sampling and encoding analog signals in essence) and D/A conversion (the reverse process of the A/D conversion in essence) have become well-known in electronics and signal processing since 1940s, and storing the digital representation is equivalent to storing the analog representation. Ex. 1003, ¶82.19.

Alternatively, paragraph 31 of Nonomura discloses storing the “gamma reference voltage levels” (the output signal of the D/A converter 29 transferred to the buffer 32 via the selector 32) in the “gamma reference control capability” (the basic circuit comprising both the non-volatile storage memory 39 and the buffer 32). A POSITA would understand the buffer 32 can be viewed as a part of the “gamma reference control capability” by redrawing the line, which a POSITA would have been well-equipped to achieve as of the earliest claimed priority date. Ex. 1003, ¶82.20.

3. Dependent Claim 2.

Nonomura teaches that the adjustment of gamma correction data may be “repeated until operator believes that there is no need for further correction.” Ex.

1006, ¶32. Thus, a POSITA would understand that Nonomura discloses that the adjustment of gamma correction data may be repeated. Ex. 1003, ¶82.21. Accordingly, a POSITA would appreciate that at least one different set of gamma reference voltage levels can be generated “under different ambient display conditions” and stored in the gamma reference control capability because different ambient conditions result in different gamma correction settings. Ex. 1003, ¶82.21.

To the extent that one would argue Nonomura fails to disclose this element, Kang discloses it. Kang discloses the multi-mode gamma voltage generator 84 for generating a gamma voltage using multi-mode gamma data set. Ex. 1007, ¶48. The memory 92 stores a multi-mode gamma data set, and such gamma data is input to the multi-channel DAC 93 to indicate a gamma reference voltage for each mode. Ex. 1007, ¶53. Notably, an example of gamma reference voltages for each mode is shown in Table 1. Ex. 1007, ¶59.

TABLE 1

Mode Gamma	Mode A	Mode B	Mode C	Mode D
GMA 1	0.1875	0.3750	0.5625	0.7500
GMA 2	1.8750	2.0625	2.2500	2.4375
GMA 3	3.3750	3.5625	3.7500	3.9375
GMA 4	5.0625	5.2500	5.4375	5.6250
GMA 5	6.7500	6.9375	7.1250	7.3125
GMA 6	8.4375	8.6250	8.8125	9.0000
GMA 7	10.1250	10.3125	10.5000	10.6875
GMA 8	11.8125	11.6250	11.4375	11.2500

Id., Table 1.

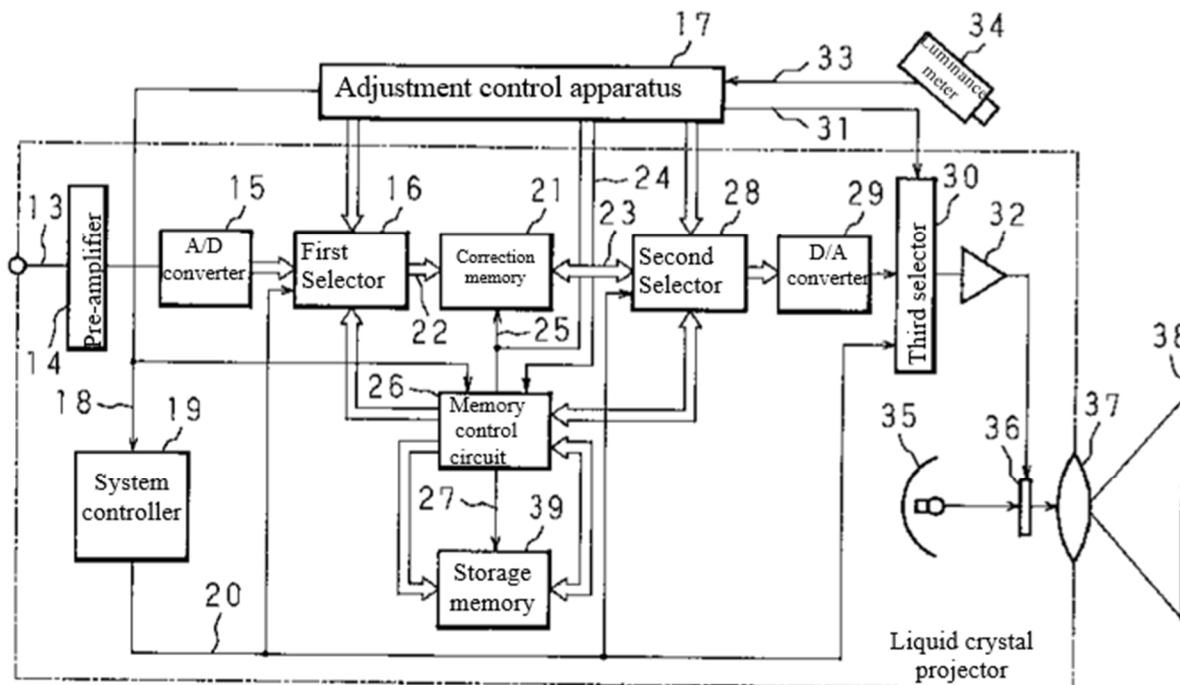
Therefore, a POSITA would understand that Kang discloses “at least one different set of gamma reference voltage levels” (e.g., Mode B data set in addition to Mode A data set) under different ambient display conditions. Ex. 1003, ¶82.23. Such multi-mode arrangement was well known to a POSITA as of the earliest claimed priority date in the gamma correction field to accommodate different display conditions and use cases. Ex. 1003, ¶82.23. A POSITA would be motivated to introduce Kang’s multi-mode gamma voltage generator 84 into the system in Nonomura to achieve versatility. Ex. 1003, ¶82.23.

4. Independent Claim 3.

[3PRE]:

Nonomura describes a liquid crystal projector that will perform gamma correction based on the results of the measurement of the applied voltage-transmittance characteristics. Ex. 1006, ¶14. A POSITA would understand that the non-linear processing of the applied voltage-transmittance characteristics is gamma correction, and the corresponding apparatus is a gamma reference voltage generator. Ex. 1006, ¶¶3-4; Ex. 1003, ¶82.24.

The basic circuit used for the liquid crystal projector is enclosed by the dashed line in FIG. 1. Ex. 1006, ¶19. Thus, a POSITA would understand that the basic circuit, which includes the “gamma reference voltage generator integrated circuits,” can be attached to the liquid crystal display as a natural design choice. 1003, ¶82.25.



Id., Fig. 1.

As articulated in §VII.A.[1E], Nonomura discloses storing gamma correction data in the non-volatile storage memory 39. Ex. 1003, ¶¶82.19-20. A POSITA would understand that Nonomura discloses “programming” (by writing data to the memory) the “gamma reference voltage generator integrated circuits” (a portion of the basic circuit comprising the non-volatile storage memory 39, the correction memory 21, the memory control circuit 26, and optionally the D/A converter 29 and the buffer 32). Ex. 1003, ¶82.26.

[34]:

To the extent Nonomura fails to disclose selecting columns, Kang does. *See*, §VII.A.[1C].

[3B]:

As described in relation to Element [1C], Nonomura teaches “varying gamma reference voltage levels on” and Kang discloses “columns of said display.” Nonomura also describes that if the A/D conversion value of video signal input 13 is n , and the desired corrected value is m , the data of the value m is written to address n of correction memory 21. Ex. 1006, ¶28. A POSITA would comprehend this process establishes a look-up table (video signal input n as address, desired corrected value m as data/result). Ex. 1003, ¶82.32.

Thus, the combination of Nonomura and Kang discloses “applying one or more different gamma voltages” (applying the A/D conversion value of the video signal input 13, which is n in the example above) to “said liquid crystal display columns” (columns of the liquid crystal panel 86). Ex. 1003, ¶82.33-34.

[3C]:

As described *supra*, Nonomura discloses reprogrammable, nonvolatile cells (in relation to Element [1A]) in said gamma reference voltage generator integrated circuits (in relation to Element [3PRE]). Nonomura describes that the A/D conversion value of the video signal input 13 (n in the example above) is input into the correction memory 21 as address signal 22. Ex. 1006, ¶20. A POSITA would appreciate that the correction memory 21, as a memory device designed to store information, at least temporarily stores the A/D conversion value of the video signal

input 13. Ex. 1003, ¶82.35. It was well known to a POSITA as of the earliest claimed priority date that a (non-volatile) memory device is divided into multiple cells, as the minimum storage unit, and different cells are “appropriate to said selected columns.” Ex. 1003, ¶82.35.

[3D]:

Nonomura discloses this element. *See*, §VII.A.[1D].

[3E]:

As described in relation to Element [3B], Nonomura describes that if the A/D conversion value of video signal input 13 is n , and the desired corrected value is m , the data of the value m is written to address n of correction memory 21. Ex. 1006, ¶28. A POSITA would comprehend Nonomura discloses “modifying said one or more different applied gamma voltages” (modifying/transforming from the A/D conversion value of video signal input 13 (n in the example above) to the desired corrected value (m in the example above)). Ex. 1003, ¶82.37. The modification process is the gamma correction process as a result of Element [3d]. Ex. 1003, ¶82.37.

[3F]:

As described in relation to Element [1E], Nonomura discloses “programming said applied gamma voltages” (storing the **corrected** A/D conversion value of video signal input 13, which is the desired corrected value) “in storage cells in said gamma reference voltage generator integrated circuits” (in memory device). Ex. 1003, ¶82.38. It was well known to a POSITA as of the earliest claimed priority date that

a (non-volatile) memory device is divided into multiple cells, as the minimum storage unit, and different cells are “appropriate to said selected columns.” Ex. 1003, ¶82.39.

[3G]:

Nonomura teaches that the adjustment of gamma correction data may be “repeated until operator believes that there is no need for further correction.” Ex. 1006, ¶32. Thus, a POSITA would understand that Nonomura discloses that steps (d) through (f) are being repeated “until said one or more optimization criteria have been satisfied.” ¶82.40.

5. Independent Claim 5.

[5PRE]:

Nonomura discloses this element. *See*, §VII.A.[1PRE].

[5A]:

Nonomura discloses this element. *See*, §VII.A.[1A].

[5B]:

Nonomura discloses this element. *See*, §VII.A.[1B].

[5C]:

Nonomura discloses this element. *See*, §VII.A.[1C].

[5D]:

Nonomura discloses this element. *See*, §VII.A.[1D].

[5E]:

Nonomura discloses this element. *See*, §VII.A.[1E].

[5F]:

Nonomura describes that the video signal input 13 is converted according to the gamma correction data in the correction memory 21 before being converted back to an analog signal by the D/A converter 29, which is input into the LCD panel 36 via the buffer 32. Ex. 1006, ¶31. A POSITA would understand that Nonomura discloses that the gamma reference voltage levels are retrieved “from said gamma reference control capability” (read from the correction memory 21). Ex. 1003, ¶82.47.

[5G]:

Nonomura describes that the video signal input 13 is converted according to the gamma correction data in the correction memory 21 before being converted back to an analog signal by the D/A converter 29, which is input into the LCD panel 36. Ex. 1006, ¶31. A POSITA would understand that Nonomura discloses displaying an image on said liquid crystal display (the LCD panel 36) based on said gamma reference voltage levels (gamma correction data stored in the correction memory). Ex. 1003, ¶82.48.

6. Dependent Claim 6.

Nonomura discloses this element. *See*, §VII.A.[2].

B. Ground 2 – Claims 1-3 and 5-6 are Obvious Under 35 U.S.C. § 103 Over Uehara and Kang in view of the Knowledge of a POSITA.

1. Motivation to Combine Uehara and Kang.

The legal basis for the motivation to combine is the same as set forth in §VII.A.1.

As it relates to this particular combination, a POSITA would have been motivated to combine Uehara and Kang.

Both Uehara and Kang are in the same field of endeavor, i.e., gamma correction. Ex. 1003, ¶84. Consequently, a POSITA would have had a reasonable expectation of success in combining their various disclosures to achieve, for example, (i) desired gamma correction that takes into consideration the gamma characteristics of the image signal for which gamma correction has been performed and (ii) improved display quality. Ex. 1003, ¶84.

Furthermore, it was well within the technical ability of a POSITA at the time to incorporate the column driver and corresponding column configuration described in Kang into the LCD described in Uehara because a POSITA would have known how to arrange an LCD into columns and rows for accessing individual pixels. Ex. 1003, ¶85.

It was also well within the technical ability of a POSITA to incorporate the multi-mode gamma voltage generator for generating a gamma voltage using multi-mode gamma data set described in Kang into Uehara's LCD because (i) multi-mode

arrangements are well-known in the gamma correction field to accommodate different display conditions and use cases and (ii) a POSITA would be motivated to do so to achieve versatility. Ex. 1003, ¶86.

It was well within the technical ability of a POSITA to incorporate the buffer unit that stabilizes the gamma reference voltages discussed in Kang into the gamma correction circuit discussed in Uehara to stabilize the gamma reference voltage levels for a stable image. Ex. 1003, ¶87.

It was well within the technical ability of a POSITA to correlate the storage cells of Uehara's EEPROMs to appropriate columns based on Kang's teachings of using column drivers to correspond non-volatile cells, gamma reference signals, and columns. Ex. 1003, ¶88.

Thus, combining Uehara and Kang would have been obvious to a POSITA. Ex. 1003, ¶89.

2. Independent Claim 1.

[IPRE]:

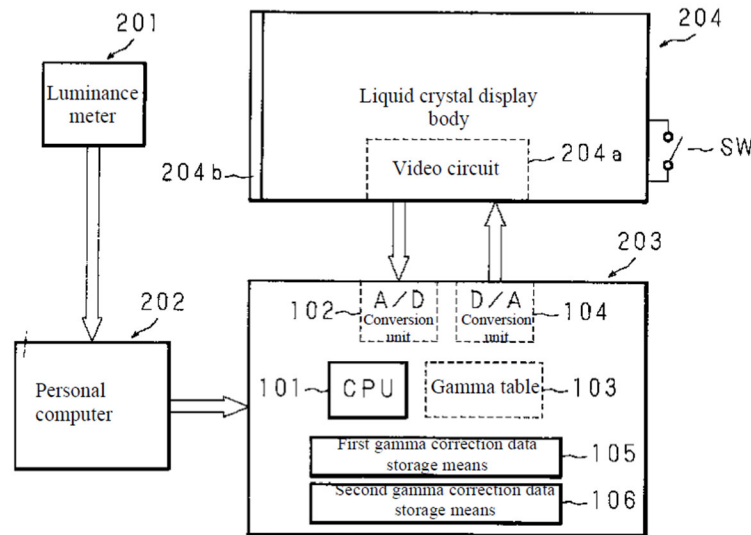
Uehara describes a gamma correction method for a liquid crystal display. Ex. 1009, ¶1. The light transmittance of an LCD panel to which voltage is applied is measured, and the gamma characteristics of the LCD panel are then determined based on the measured light transmittance. Ex. 1009, ¶7. The gamma characteristics are then corrected. *Id.* Uehara explains that the light transmittance in relation to the

input voltage is called the “V-T characteristic,” which is appropriately corrected by the gamma correction data. Ex. 1009, ¶4. A POSITA would understand that correcting the V-T characteristic using the gamma correction data is a process of “calibrating a liquid crystal display to a desired gamma curve.” Ex. 1003, ¶89.1.

Moreover, Uehara highlights that the purpose of gamma correction is to “correct the non-linearity and manufacturing variability of the voltage-light transmission characteristics of the liquid crystal elements.” Ex. 1009, ¶2. Thus, a POSITA would appreciate that Uehara discloses that the method of calibrating is “to compensate for panel to panel manufacturing variations.” Ex. 1003, ¶89.2.

[1A]:

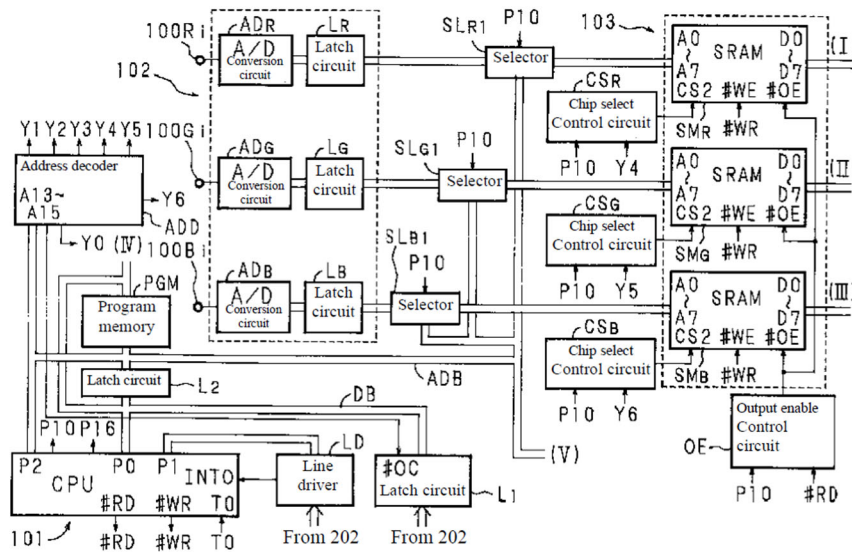
Uehara describes a liquid crystal display that includes an LCD body 204 and a gamma correction circuit 203. Ex. 1009, ¶¶11-12. The LCD body 204 includes a liquid crystal panel 204b and a video circuit 204a built into the LCD body 204. Ex. 1009, ¶11.



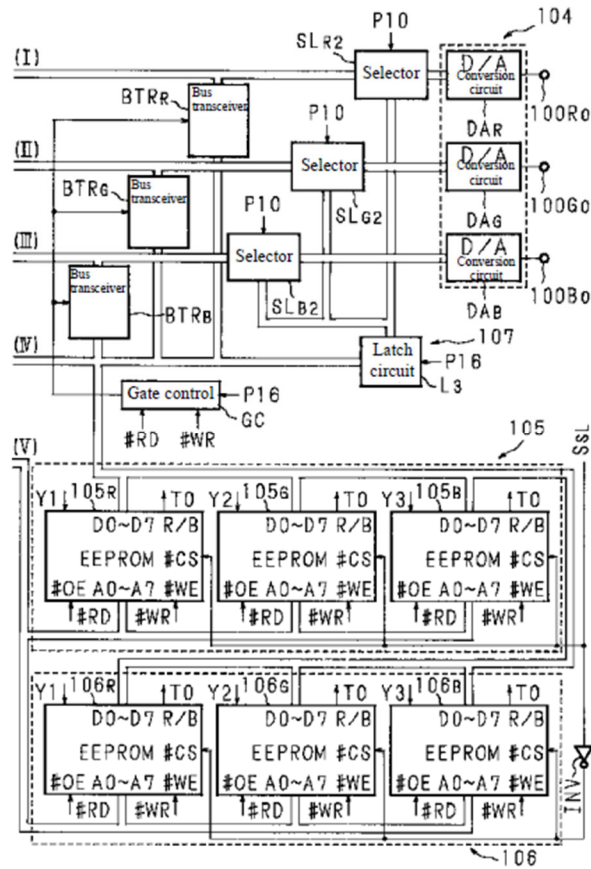
Id., Fig. 1.

The light transmittance of the liquid crystal panel 204b is measured by a luminance meter 201 and sent to a personal computer 202. Ex. 1009, ¶11. The output signal of the personal computer is sent to the gamma correction circuit 203. Ex. 1009, ¶12. The gamma correction circuit 203 includes, among other components, the A/D conversion unit 102, the D/A conversion unit 104, the CPU 101, the gamma table 103, the first gamma correction data storage means 105, and the second gamma correction data storage means 106. Ex. 1009, ¶12. A POSITA would appreciate that the gamma correction circuit 203 is the “gamma reference control capability” because of (i) the components included in the gamma correction circuit 204 and (ii) the feedback loop comprised of the liquid crystal panel 204b, the luminance meter 201, the personal computer 202, and the gamma correction circuit 203. Ex. 1003, ¶89.4.

An example of detailed structures of the gamma correction circuit 203 is shown in FIGS. 2-3. Ex. 1009, ¶13. As shown in FIG. 3, the first gamma correction data storage means 105 stores gamma correction data (image signals not gamma-corrected) and includes, among other components, EEPROMs 105_R, 105_G, and 105_B corresponding to the R, G, and B image signals. Ex. 1009, ¶17. Likewise, the second gamma correction storage means 106 stores gamma correction data (image signals gamma corrected) and includes EEPROMs 106_R, 106_G, and 106_B corresponding to the R, G, and B image signals. *Id.*



Id., Fig. 2.



Id., Fig. 3.

In one operation, after storing the gamma correction data, the control command signal from the personal computer 202 is sent to the gamma correction circuit 203, thus the address signal and write signal #WR from the CPU 101 are provided to EEPROMs 105_R, 105_G, 105_B, 106_R, 106_G, and 106_B. Ex. 1009, ¶28. The personal computer 202 writes the gamma correction data (image signals gamma not corrected) to EEPROMs 105_R, 105_G, 105_B. *Id.* After selecting the EEPROM 106_R, 106_G, and 106_B by switching the switch SW, the personal computer 202 similarly writes the gamma correction data (image signals gamma corrected) to EEPROM

106_R, 106_G, 106_B. Ex. 1009, ¶28. A POSITA would appreciate that the “gamma reference control capability” is electrically reprogrammable (being able to write data to the EEPROMs) and non-volatile (EEPROM was well-known as non-volatile). Ex. 1003, ¶89.6.

[IB]:

Uehara describes the light transmittance of the liquid crystal panel 204b is measured by a luminance meter 201 and sent to a personal computer 202. Ex. 1009, ¶¶11, 23. A POSITA would understand that the luminance meter 201 is a sensor and the luminance of the liquid crystal panel 204b is optical input. Ex. 1003, ¶89.7.

FIG. 1 shows the configuration for gamma correction, while FIG. 4 shows the configuration for image displaying. Ex. 1009, Brief Description of Drawings. A POSITA would comprehend that Uehara discloses that said sensor (the luminance meter 201) “is separate from said display” because the liquid crystal panel 204b operates without the luminance meter 201 in FIG. 4. Ex. 1003, ¶89.8.

[IC]:

Uehara describes that the output signal of the personal computer is sent to the gamma correction circuit 203. Ex. 1009, ¶12. The signal coming out of the gamma correction circuit 203 is sent to the LCD body 204. *Id.*

During a gamma correction process, the personal computer 202 outputs the test signal data, the mode switching signal, the gate control signal, and other control

command signals for generating test signals in response to the voltage applied to the liquid crystal panel 204b, and the gamma correction circuit 203 receives these signals. Ex. 1009, ¶21. The test signal data is then inputted into the gamma correction circuit 203 and the latch circuit L₃ and the CPU 101 of the gamma correction circuit 203 via the latch circuit L₁. *Id.*

As a result of these signals from the personal computer 202, the latch circuit L₃ generates a test signal based on the test signal data, and the test signal is converted to the analog voltage by the D/A conversion unit 104. Ex. 1009, ¶22. The converted analog voltage is sent to the LCD body 204 via output terminals 100R₀, 100G₀, and 100B₀. Ex. 1009, ¶22. The personal computer 202 modifies the test signal data and inputs it to the latch circuit L₃ in order to change the voltage applied to the liquid crystal panel 204b, which changes its light transmittance. Ex. 1009, ¶23. The test signal generation step will sequentially change the voltage to be applied to the liquid crystal panel based on the test signal data. Ex. 1009, ¶41.

Thus, a POSITA would comprehend that the personal computer 202, working in conjunction with the CPU 101 of the gamma correction circuit 203, effectively varies the “gamma reference voltage levels” by sending a group of signals, including the test signal data, the mode switching signal, the gate control signal, and other control command signals for generating test signals in response to the applied voltage. Ex. 1003, ¶89.12.

Similarly, a POSITA would comprehend that Uehara discloses that said control circuit (the personal computer 202 or the personal computer 202 in conjunction with the CPU 101) “is separate from said display” because the liquid crystal panel 204b operates without the personal computer 202 in FIG. 4. Ex. 1003, ¶89.13.

To the extent that Uehara fails to disclose “on columns of said display,” Kang discloses that, as articulated *supra* in §VII.A.[1C].

A POSITA would be motivated to modify the teachings of Uehara to apply the gamma reference voltage levels, which are varied by the personal computer 202 (in conjunction with the CPU 101), to the columns of the liquid crystal panel 204b in light of the teachings of Kang. Ex. 1003, ¶89.15. Arranging an LCD into columns and rows for accessing individual pixels was well known to a POSITA as of the earliest claimed priority date. Ex. 1003, ¶89.15.

[1D]:

Uehara describes that the luminance meter 201 repeatedly measures the light transmittance (luminance) of the liquid crystal panel 204b, as the test signal data is “changed by the personal computer 202.” Ex. 1009, ¶23. The same operation is “repeated in order to sequentially change the applied voltage of liquid crystal panel 204b from, for example, a black level to a white level.” Ex. 1009, ¶23. By measuring all of the light transmission from the black level to the white level, it becomes

“possible to determine the gamma characteristics of liquid crystal panel 204b.” Ex. 1009, ¶24.

The personal computer 202 then reads the measurements values of the light transmission that have been stored in the memory and calculates the inverse function of the gamma characteristics of the liquid crystal and 204b. Ex. 1009, ¶24. The personal computer 202 then calculates the gamma correction data, which is temporarily stored in the personal computer 202 in order to correct the gamma characteristics of liquid crystal panel 204b. *Id.*

Thus, a POSITA would appreciate that the gamma correction data is the “gamma reference voltage levels” and is optimized using this feedback loop (i.e., changing the test signal data, generating light transmission accordingly, measuring the light transmission, calculating the gamma correction data). Ex. 1003, ¶89.18.

A POSITA would appreciate that this optimization process is “using means for executing a predetermined algorithm according to a predetermined criteria and data sensed by said at least one sensor” because (i) the luminance meter 201 is used; (ii) the applied voltage is changed in a predetermined manner (e.g., from a black level to a white level); and (iii) the gamma correction data is calculated using a predetermined algorithm (e.g., calculating the inverse function of the gamma characteristics). Ex. 1003, ¶89.19. It is also well-known in the gamma correction space that the optimization process involves “a predetermined algorithm” for the

software aspect and at least one sensor for the hardware aspect. Ex. 1003, ¶89.19. A POSITA would also comprehend that the optimization process typically involves matching/fitting to a certain desired gamma curve, which is “according to a predetermined criteria.” Ex. 1003, ¶89.19. It is also common knowledge of a POSITA that the “predetermined algorithm” must be executed by “means for executing ...” such as the personal computer 202, which interacts with, among other things, the CPU 101. Ex. 1003, ¶89.19.

As articulated above, a POSITA would appreciate that Uehara discloses that said means for executing said predetermined algorithm (the personal computer 202 or the personal computer 202 in conjunction with the CPU 101) “is separate from said display” because the liquid crystal panel 204b operates without the personal computer 202 in FIG. 4. Ex. 1003, ¶89.20.

[1E]:

As explained *supra*, the gamma correction data calculated in this way is temporarily stored in the personal computer 202 and may be written directly to EEPROMs 105_R, 105_G, 105_B, 106_R, 106_G, and 106_B. Ex. 1009, ¶24, 30.

Moreover, after storing the gamma correction data, the control command signal from the personal computer 202 is sent to the gamma correction circuit 203, thus the address signal and write signal #WR from the CPU 101 are provided to EEPROMs 105_R, 105_G, 105_B, 106_R, 106_G, and 106_B. Ex. 1009, ¶28. The personal

computer 202 writes the gamma correction data (image signals gamma not corrected) to EEPROMs 105_R, 105_G, 105_B. *Id.* Likewise, the personal computer 202 similarly writes the gamma correction data (image signals gamma corrected) to EEPROM 106_R, 106_G, 106_B. Ex. 1009, ¶28.

Thus, a POSITA would comprehend that Uehara discloses storing the “gamma reference voltage levels” (the gamma correction data) in the “gamma reference control capability” (the gamma correction circuit 203). Ex. 1003, ¶89.23.

To the extent that the “gamma reference voltage levels” is interpreted as analog gamma reference voltage levels, Uehara discloses the same.

The gamma correction circuit 203 includes, among other components, the D/A conversion unit 104. Ex. 1009, ¶12. The analog version of the gamma reference voltages, which interfaces with the real world, must exist in the system, and a POSITA at the time was well-equipped to include, for example, a D/A converter and a buffer in the “gamma reference control capability.” Ex. 1003, ¶89.25. Indeed, A/D conversion (sampling an encoding analog signals in essence) and D/A conversion (the reverse process of the A/D conversion in essence) have become well known in electronics and signal processing since 1940s. Ex. 1003, ¶89.25.

In addition, Kang discloses that the buffer unit 94 stabilizes the eight gamma reference voltages and applies them to the gamma voltage output 95. Ex. 1007, ¶54. Thus, a POSITA would be motivated to introduce the buffer unit 94 discussed in

Kang to stabilize the gamma reference voltage levels for a stable image. Ex. 1003, ¶89.26.

3. Dependent Claim 2.

Uehara describes that the same operation is “repeated in order to sequentially change the applied voltage of liquid crystal panel 204b from a black level to a white level.” Ex. 1009, ¶23. Thus, a POSITA would understand that Uehara discloses that the adjustment of gamma correction data may be repetitive as needed. Ex. 1003, ¶89.27. As a result of such repetitive operations, a POSITA would appreciate that at least one different set of gamma reference voltage levels can be generated “under different ambient display conditions” and stored in the gamma reference control capability because different ambient conditions result in different gamma correction setting. Ex. 1003, ¶89.27.

To the extent that one would argue Uehara fails to disclose this element, Kang discloses the same. *See* §VII.A.2. A POSITA would be motivated to introduce Kang’s multi-mode gamma voltage generator 84 into the system in Uehara to achieve versatility. Ex. 1003, ¶89.29.

4. Independent Claim 3.

[3PRE]:

Uehara describes “calibrating an LCD to a desired gamma curve” (*see* §VII.B.[1PRE]) and “storing said gamma reference voltage levels in said gamma

reference control capability” (*see* §VII.B.[1E]). A POSITA would appreciate that the gamma correction circuit 203 is the “one or more gamma reference voltage generator integrated circuits” because of (i) the components included in the gamma correction circuit 204 and (ii) the feedback loop comprised of the liquid crystal panel 204b, the luminance meter 201, the personal computer 202, and the gamma correction circuit 203. Ex. 1003, ¶89.31.

A POSITA would also understand that the gamma correction circuit 203 can be attached to the liquid crystal display as a natural design choice. 1003, ¶89.32.

[3A]:

To the extent that someone would argue that Uehara fails to disclose selecting columns on the LCD, Kang does. *See*, §VII.A.[1C]. A POSITA would be motivated to modify the teachings of Uehara to apply the gamma reference voltage levels, which are varied by the personal computer 202, to the columns of the liquid crystal panel 204b in light of the teachings of Kang. Ex. 1003, ¶89.36. Arranging an LCD into columns and rows for accessing individual pixels was well-known to a POSITA as of the earliest claimed priority date. Ex. 1003, ¶89.36.

[3B]:

As described above, Uehara discloses a gamma correction circuit that applies gamma correction to the liquid crystal display using a personal computer. *See*, §VII.B.[1C]. Moreover, the image signals output from the A/D converters (AD_R,

AD_G, AD_B) are sent to address terminals of the gamma table 103, and the image signals output from the gamma table 103 are sent to D/A converters (DA_R, DA_G, DA_B). Ex. 1009, ¶¶13-14. A POSITA would comprehend that this process is a gamma correction process (image signals output from the ADC as address, image signals output from the gamma table 103 as gamma-corrected data). Ex. 1003, ¶89.38.

Thus, a POSITA would comprehend that the personal computer 202, working in conjunction with the CPU 101 of the gamma correction circuit 203, effectively applies “one or more different gamma voltages to said liquid crystal display” by sending a group of signals, including the test signal data, the mode switching signal, the gate control signal, and other control command signals for generating test signals in response to the applied voltage. Ex. 1003, ¶89.39.

To the extent that Uehara fails to disclose on columns of said liquid crystal display, Kang discloses that, as articulated *supra*. See, §II.B.[1C].

A POSITA would be motivated to modify the teachings of Uehara to apply the gamma reference voltage levels, which are varied by the personal computer 202 (in conjunction with the CPU 101), to the columns of the liquid crystal panel 204b in light of the teachings of Kang because the row-column arrangement is common in the display field. Ex. 1003, ¶89.41.

[3C]:

As described above, Uehara discloses storing applied gamma voltages in reprogrammable nonvolatile cells. *See* §VII.B.[1A](describing programming and storage into EEPROMs). A POSITA would appreciate that the “gamma reference control capability” is electrically reprogrammable (being able to write data to the EEPROMs) and non-volatile (EEPROM is non-volatile). Ex. 1003, ¶89.42. Further, a POSITA would appreciate that the gamma table 103, implemented as the memory device designed to store information, at least temporarily stores the image signals output from the ADC as address. Ex. 1009, ¶¶13-14; Ex. 1003, ¶89.43. It to a POSITA as of the earliest claimed priority date that a (non-volatile) memory device is divided into multiple cells, as the minimum storage unit, and different cells are “appropriate to said selected columns.” *Id.*

[3D]:

Uehara discloses this element. *See*, §VII.B.[1D].

[3E]:

See §VII.B.[1D]. Moreover, as described in relation to Element [3B], Uehara discloses that the image signals output from the A/D converters (AD_R , AD_G , AD_B) are sent to address terminals of the gamma table 103, and the image signals output from the gamma table 103 are sent to D/A converters (DA_R , DA_G , DA_B). Ex. 1009, ¶¶13-14. This process is a gamma correction process (image signals output from the ADC as address, image signals output from the gamma table 103 as gamma-

corrected data). Ex. 1003, ¶89.46. Thus, a POSITA would comprehend that Uehara discloses “modifying said one or more different applied gamma voltages” (modifying/transforming from the image signals output from the ADC to the image signals output from the gamma table 103. *Id.* The modification process is the gamma correction process as a result of Element [3D]. *Id.*

[3F]:

As explained *supra*, the gamma correction data calculated in this way is temporarily stored in the personal computer 202. Ex. 1009, ¶¶13-14 and 24. The gamma correction data temporarily stored in the personal computer 202 is written directly to EEPROMs 105_R, 105_G, 105_B, 106_R, 106_G, and 106_B. Ex. 1009, ¶30.

Moreover, after storing the gamma correction data, the control command signal from the personal computer 202 is sent to the gamma correction circuit 203, thus the address signal and write signal #WR from the CPU 101 are provided to EEPROMs 105_R, 105_G, 105_B, 106_R, 106_G, and 106_B. Ex. 1009, ¶28. The personal computer 202 writes the gamma correction data (image signals gamma not corrected) to EEPROMs 105_R, 105_G, 105_B. *Id.*

Thus, a POSITA would understand that Uehara discloses “programming” (writing) “said applied gamma voltages” (writing the gamma correction data output from the gamma table 103) in “storage cells in said gamma reference voltage generator integrated circuits” (the EEPROMs 105_R, 105_G, 105_B, 106_R, 106_G, and

106_B, and the gamma table 103). Ex. 1003, ¶89.49. Transferring data between different types of memory devices (e.g., EEPROMs and SRAMs) to a POSITA as of the earliest claimed priority date. *Id.*

As articulated *supra*, such storage cells are “appropriate to said selected columns.” Ex. 1003, ¶89.50.

[3G]:

Uehara describes that the luminance meter 201 repeatedly measures the light transmittance (luminance) of the liquid crystal panel 204b, as the test signal data is “changed by the personal computer 202.” Ex. 1009, ¶23. The same operation is “repeated in order to sequentially change the applied voltage of liquid crystal panel 204b from, for example, a black level to a white level.” Ex. 1009, ¶23. By measuring all of the light transmission from the black level to the white level, it becomes “possible to determine the gamma characteristics of liquid crystal panel 204b.” Ex. 1009, ¶24. Thus, a POSITA would comprehend that Uehara discloses that steps (d) through (f) are being repeated “until said one or more optimization criteria have been satisfied.” ¶89.51.

5. Independent Claim 5.

[5PRE]:

Uehara discloses this element. *See*, §II.B.[1PRE].

[5A]:

Uehara discloses this element. *See*, §II.B.[1A].

[5B]:

Uehara discloses this element. *See*, §II.B.[1B].

[5C]:

Uehara discloses this element. *See*, §II.B.[1C].

[5D]:

Uehara discloses this element. *See*, §II.B.[1D].

[5E]:

Uehara discloses this element. *See*, §II.B.[1E].

[5F]:

Uehara describes that the gamma correction circuit 203 includes the gamma table 103 configured to store the gamma correction data. Ex. 1009, ¶12. After storing the gamma correction data, the address signal and write signal #WR from the CPU 101 are provided to EEPROMs 105_R, 105_G, 105_B, 106_R, 106_G, and 106_B. Ex. 1009, ¶28. The personal computer 202 writes the gamma correction data (image signals gamma not corrected) to EEPROMs 105_R, 105_G, 105_B. *Id.* When EEPROMs 105_R, 105_G, and 105_B are provided with the address signal and read signal #RD, the gamma correction data will be read from EEPROMs 105_R (105_G, 105_B), and this data will be sent to the SRAM SM_R (SM_G, SM_B). 1009, ¶34. Thus, a POSITA would understand that Uehara discloses retrieving said gamma reference voltage levels (selecting the EEPROMs 105_R, 105_G, and 105_B and reading the gamma correction data stored therein) from said gamma reference control capability (the gamma

correction circuit 203, which includes the EEPROMs 105_R, 105_G, and 105_B). Ex. 1003, ¶89.58.

[5G]:

Uehara describes that the image signal that was read out will be sent to the D/A conversion circuits, where the image signal is converted to analog image signal, which is applied to the liquid crystal panel 204b in order to display the image on the liquid crystal panel 204b. A POSITA would understand that Uehara discloses displaying an image on said liquid crystal display (on the liquid crystal panel 204b) based on said gamma reference voltage levels because the analog image signal is based on gamma reference voltage levels (gamma correction data). Ex. 1003, ¶89.59.

6. Dependent Claim 6.

Uehara discloses this element. *See*, §II.B.[2].

C. Ground 3 – Claims 1 and 3 are Obvious Under 35 U.S.C. § 103 Over Tobiya and Kang in view of the Knowledge of a POSITA.

1. Motivation to Combine Tobiya with the Knowledge of a POSITA.

The legal basis for the motivation to combine is the same as set forth in §II.A.1. As it relates to this particular combination, a POSITA would have been motivated to combine Tobiya and Kang.

Both Tobiya and Kang are in the same field of endeavor, i.e., gamma correction. Ex. 1003, ¶91. Consequently, a POSITA would have had a reasonable expectation of success in combining their various disclosures to achieve, for example,

(i) a variable gamma correction in addition to a linear type gamma correction and (ii) improved display quality. *Id.*

Furthermore, it was well within the technical ability of a POSITA at the time to incorporate the column driver and corresponding column configuration described in Kang into the LCD described in Tobiya because a POSITA would have known at the time how to arrange an LCD into columns and rows for accessing individual pixels. Ex. 1003, ¶92.

It was also well within the technical ability of a POSITA to incorporate the multi-mode gamma voltage generator for generating a gamma voltage using Kang's multi-mode gamma data set into Tobiya's LCD because (i) multi-mode arrangements are well-known in the gamma correction field to accommodate different display conditions and use cases and (ii) a POSITA would be motivated to do so to achieve versatility. Ex. 1003, ¶93.

It was well within the technical ability of a POSITA to incorporate the buffer unit that stabilizes the gamma reference voltages discussed in Kang into the gamma correction circuit discussed in Tobiya to stabilize the gamma reference voltage levels for a stable image. Ex. 1003, ¶94.

It was well within the technical ability of a POSITA to correspond the storage cells of the LUS memory means described in Tobiya to Kang's columns of the display because it was well known to a POSITA as of the earliest claimed priority

date that a (non-volatile) memory device is divided into multiple cells, as the minimum storage unit, and different cells are appropriate to the selected columns. Ex. 1003, ¶95.

Thus, combining Tobiya and Kang would have been obvious to a POSITA. *Id.*

1. Independent Claim 1.

[IPRE]:

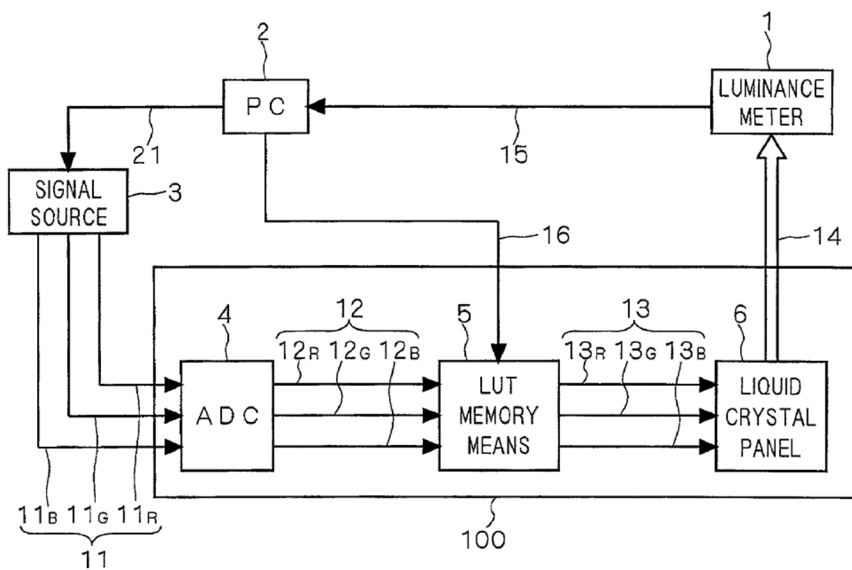
Tobiya describes a display characteristic correction system that includes a liquid crystal display 100 and a means for correcting the gray level thereof. Ex. 1010, ¶36. Tobiya explains that the gray level relates to luminance or light transmittance. Ex. 1010, ¶4. The value of the signal inputted to the display device and the value of the gray level associate with a characteristic (the “ γ -characteristic” or the “display characteristic”) inherent to the display device. *Id.* Converting the input signal by using another characteristic (the “correction characteristic”) allows the display device to display with a gray level that has a linear relationship with the value of the input signal. *Id.* A POSITA would understand that such a display characteristic correction system and the corresponding operation method is “a method of calibrating a liquid crystal display to a desired gamma curve” because converting the input signal by using the correction characteristic (also known as “gamma

correctio data”) is a process to calibrate the LCD to a desired gamma curve (called “display characteristic” in Tobiya). Ex. 1003, ¶96.1.

Tobiya further states that the correction characteristic needs to be set for each of the display devices, and a look-up table (hereinafter, referred to as "LUT") is used so as to make the input signal and the conversion signal associated with each other because there are variations in the display characteristic of individual display devices. Ex. 1010, ¶5. Ex. 1003, ¶96.2.

[1A]:

Tobiya describes that the display characteristic correction system includes, among other components, the signal source 3, the analog/digital converter (ADC) 4, the LUT memory means 5, the liquid crystal panel 6, the computer 2, and the luminance meter 1. Ex. 1010, ¶¶36-37, 39-40.



Id., Fig. 1.

The ADC 4 carries out an analog/digital conversion on a group of analog RGB signals 11 inputted thereto from outside and generates a group of digital RGB signals 12. Ex. 1010, ¶37. The LUT memory means 5 carries out a conversion on the group of RGB signals 12 based upon a predetermined conversion characteristic and generates a group of digital RGB signals 13 as conversion signals. *Id.* Thus, a POSITA would appreciate that Tobiya discloses “providing said display with gamma reference control capability” because the LUT memory means 5 carries out a conversion on the RGB signals 12 based on a predetermined conversion characteristic to generate a group of RGB signals 13 as conversion signals. Ex. 1003, ¶96.4.

Moreover, the application of a rewritable memory (e.g., an EEPROM) as the LUT memory means 5 makes it possible to cancel individual differences in the display characteristic of the liquid crystal panels 6, and consequently to obtain a desired gray level. Ex. 1010, ¶40. Therefore, a POSITA would understand that Tobiya discloses that the gamma reference control capability is “electrically reprogrammable” (rewritable) and “non-volatile” (EEPROM is well known as nonvolatile). Ex. 1003, ¶96.5.

[IB]:

Tobiya describes that the luminance meter 1 measures the gray level (e.g., the luminance 14) displayed by the liquid crystal panel 6. Ex. 1010, ¶39. The data 15

corresponding to the luminance 14 measured by the luminance meter 1 is supplied to the computer 2. *Id.* Thus, Tobiya discloses “testing said display with at least one sensor with optical input” because the luminance meter 1 is the “at least one sensor” and the luminance 14 is the “optical input.” Ex. 1003, ¶96.6.

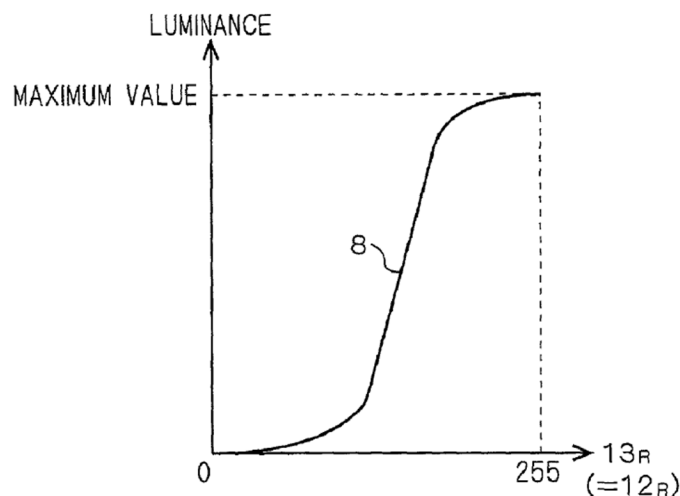
Moreover, as shown in FIG. 1, the luminance meter 1 is separate from the LCD 100. Ex. 1010, FIG. 1. Hence, a POSITA would comprehend that Tobiya discloses “said sensor is separate from said display.” Ex. 1003, ¶96.7.

[IC]:

Tobiya describes that the signal source 3 generates a group of analog RGB signals 11 corresponding to various gradients, based upon a control signal 21 from the computer 2 for setting the LUT memory means 5 and gives them to the ADC 4. Ex. 1010, ¶39. Based on the control signal 21 from the computer 2, the signal 11R having various amplitudes is outputted from the signal source 3 to the ADC 4. Ex. 1010, ¶43. The ADC 4 subjects it to a quantization process with the greatest amplitude being set at 255 to generate a signal 12R, and outputs the resulting signal to the LUT memory means 5. *Id.*

The LUT memory means 5 carries out a conversion on the group of RGB signals 12 based upon a predetermined conversion characteristic and generates a group of digital RGB signals 13 as conversion signals. Ex. 1010, ¶37. Since the LUT memory means 5 stores the conversion characteristic 16R that allows the signals 12R

and 13R to have the same value at the very beginning, the value of the signal 12R is inputted to the liquid crystal panel 6. Ex. 1010, ¶44. The liquid crystal panel 6 emits light with a luminance corresponding to the value of the signal 12R, and the luminance meter 1 measures the luminance 14 at this time and sends data 15 indicating the results to the computer 2. *Id.* This process continues on all the values 0 to 255 of gradients, and the display characteristic of the red color of the liquid crystal panel 6 is obtained. Ex. 1010, ¶45. FIG. 3 shows an exemplary display characteristic 8 of the liquid crystal panel 6. *Id.*



Id., Fig. 3.

Thus, a POSITA would comprehend that Tobiya discloses varying gamma reference voltage levels (changing the digital RGB signals 13 as conversion signals based on the control signal 21 and the conversion characteristic 16) applied to the

display (the liquid crystal panel 6) by a control circuit (the computer 2 that sends the control signal 21 and the conversion characteristic 16). Ex. 1003, ¶96.10.

Moreover, as shown in FIG. 1, the computer 2 is separate from the LCD 100. Ex. 1010, FIG. 1. Hence, a POSITA would comprehend that Tobiya discloses “said control circuit is separate from said display.” Ex. 1003, ¶96.11.

To the extent that Tobiya fails to disclose “on columns of said display,” Kang discloses applying gamma reference voltage levels on columns of the display, as articulated *supra*. Ex. 1003, ¶96.12.

A POSITA would be motivated to modify the teachings of Tobiya to apply the gamma reference voltage levels, which are varied by the computer 2, to the columns of the liquid crystal panel 6 in light of the teachings of Kang because arranging an LCD into columns and rows for accessing individual pixels was well known to a POSITA as of the earliest claimed priority date. *Id.*

[1D]:

Tobiya describes that the signal source 3 generates a group of analog RGB signals 11 corresponding to various gradients, based upon a control signal 21 from the computer 2 for setting the LUT memory means 5 and gives them to the ADC 4. Ex. 1010, ¶39.

Based on the control signal 21 from the computer 2, the signal 11R having various amplitudes is outputted from the signal source 3 to the ADC 4, and the ADC

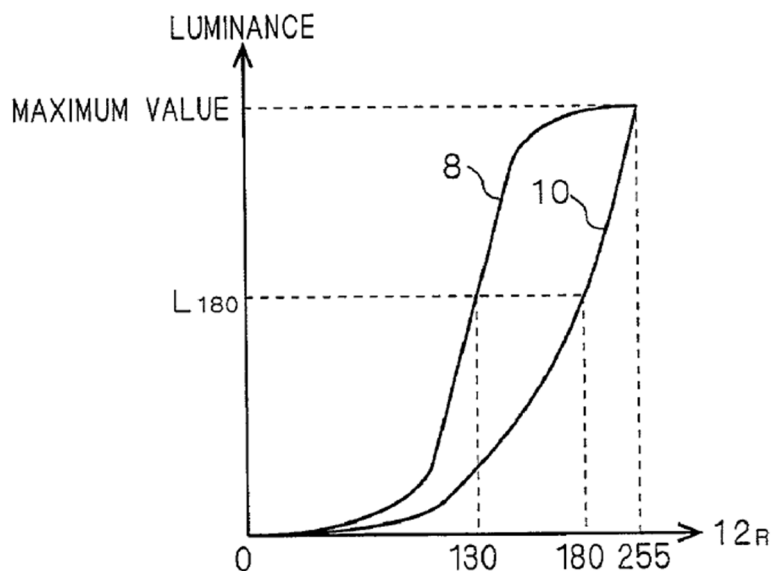
4 subjects it to a quantization process with the greatest amplitude being set at 255 to generate a signal 12R, and outputs the resulting signal to the LUT memory means 5. Ex. 1010, ¶43. The LUT memory means 5 carries out a conversion on the group of RGB signals 12 based upon a predetermined conversion characteristic and generates a group of digital RGB signals 13 as conversion signals. Ex. 1010, ¶37.

The luminance meter 1 measures the gray level (e.g., the luminance 14) displayed by the liquid crystal panel 6, and the data 15 corresponding to the luminance 14 measured by the luminance meter 1 is supplied to the computer 2. Ex. 1010, ¶39. This process continues on all the values 0 to 255 of gradients, and the display characteristic of the red color of the liquid crystal panel 6 is obtained. Ex. 1010, ¶45.

Once the display characteristic has been obtained, the conversion characteristic can be obtained accordingly. Ex. 1010, ¶47. By comparing the actual luminance target characteristic 10 with the actually measured display characteristic 8 of the liquid crystal panel 6, a conversion characteristic is obtained, and the conversion characteristic makes the display characteristic covering the entire liquid crystal display 100 coincident with the actual luminance target characteristic 10. Ex. 1010, ¶48.

As shown in FIG. 6, supposing that the display characteristic of the liquid crystal panel 6 is in conformity with the actual luminance target characteristic 10,

a signal 11_R having a value of gradient 180 is supplied, the luminance of the liquid crystal panel 6 is represented by L_{180} . Ex. 1010, ¶49. In this case, when the value of gradient of the signal 13_R , which gives the luminance L_{180} in accordance with the display characteristic 8 that is the actual display characteristic of the liquid crystal panel, is found, a value of gradient 130 is obtained. Ex. 1010, ¶49. A POSITA would appreciate that a gradient value of 130, instead of a gradient value of 180, should be used as the input to achieve the target luminance value of L_{180} , and a corresponding conversion (i.e., from 180 to 130) can be carried out. Ex. 1003, ¶96.17.



Ex. 1010, Fig. 6.

This process is carried out by the computer 2 with respect to all the values of gradients so as to obtain a conversion characteristic 16 with respect to the red color as well as the green color and the blue color. Ex. 1010, ¶49.

Therefore, a POSITA would understand that Tobiya discloses optimizing (comparing the actual luminance target characteristic 10 with the actually measured display characteristic 8 to obtain the conversion characteristic) said gamma reference voltage levels according to a predetermined criteria (carrying out the conversion based on the predetermined conversion characteristic) and data sensed by said at least one sensor (the luminance meter 1) to “achieve the desired gamma curve” (the desired/target display characteristic). Ex. 1003, ¶96.19.

A POSITA would also comprehend that “means for ...” is needed to execute the predetermined algorithm, and the computer 2 is such “means for executing a predetermined algorithm.” Ex. 1003, ¶96.20.

Moreover, as shown in FIG. 1, the computer 2 is separate from the LCD 100. Ex. 1010, FIG. 1. Hence, a POSITA would comprehend that Tobiya discloses “said means for executing said predetermined algorithm is separate from said display.” Ex. 1003, ¶96.21.

[IE]:

Tobiya describes that the computer 2 compares the values of the group of RGB signals 11 with the values of the data 15 and stores the resulting conversion characteristic 16 in the LUT memory means 5. Ex. 1010, ¶40. This process is realized by storing data corresponding to the value of the group of RGB signals 13 in addresses corresponding to the value of the group of RGB signals 12. *Id.* A

POSITA would appreciate a lookup table (the value of the group of RGB signals 12 as addresses, the value of the group of RGB signals 13 as desired/target data) is established, and that is where the name “look-up table (“LUT”) memory means” comes from. Ex. 1003, ¶96.22. The application of a rewritable memory (e.g., an EEPROM) as the LUT memory means 5 makes it possible to cancel individual differences in the display characteristic of the liquid crystal panels 6, and consequently to obtain a desired gray level. Ex. 1010, ¶40.

Therefore, a POSITA would understand that Tobiya discloses storing said gamma reference voltage levels (storing the resulting conversion characteristic 16 is equivalent to storing the group of RGB signals 13) in said reference control capability (the LUT memory means 5 which is reprogrammable and nonvolatile). Ex. 1003, ¶96.23.

To the extent that the “gamma reference voltage levels” is interpreted as analog gamma reference voltage levels, Kang discloses the same.

Kang discloses that (i) the gamma data is input to the multi-channel DAC 93 to be converted to eight gamma reference voltages and (ii) the buffer unit 94 stabilizes the eight gamma reference voltages and applies them to the gamma voltage output 95. Ex. 1007, ¶54. Thus, a POSITA would be motivated to introduce Kang’s multi-channel DAC 93 and the buffer unit 94 to stabilize the gamma reference voltage levels for digital/analog conversion and image stability. Ex. 1003, ¶96.25.

2. Independent Claim 3.

[3PRE]:

Tobiya describes “calibrating an LCD to a desired gamma curve” (*See*, §II.C.[1PRE]) and “storing said gamma reference voltage levels in said gamma reference control capability” (*See*, §II.C.[1E]). Thus, a POSITA would appreciate that Tobiya discloses “programming one or more gamma reference voltage generator integrated circuits” because (i) the LUT memory means 5 carries out a conversion on the RGB signals 12 based on a predetermined conversion characteristic to generate a group of RGB signals 13 as conversion signals and (ii) storing the resulting conversion characteristic 16 in the LUT memory means 5 is a process of programming. Ex. 1003, ¶96.26.

[3A]:

To the extent that someone would argue that Tobiya fails to disclose selecting columns on the LCD, Kang discloses the same. Ex. 1003, ¶96.27.

A POSITA would be motivated to modify the teachings of Tobiya to apply the gamma reference voltage levels to the columns of the liquid crystal panel 6 in light of the teachings of Kang because arranging an LCD into columns and rows for accessing individual pixels was well known to a POSITA as of the earliest claimed priority date. Ex. 1003, ¶96.28.

[3B]:

As described in §VII.B.[1C], Tobiya uses changing the digital RGB signals 13 as conversion signals to adjust the luminance of the display. Thus, a POSITA would comprehend that Tobiya discloses applying one or more different gamma voltage to said liquid crystal display. Ex. 1003, ¶¶96.29.

To the extent that Tobiya fails to disclose “said liquid crystal display columns,” Kang discloses applying one or more different gamma voltages to the columns of the display, as articulated *supra*. Ex. 1003, ¶¶96.30.

A POSITA would be motivated to modify the teachings of Tobiya to apply the one or more different gamma voltages to the columns of the liquid crystal panel in light of the teachings of Kang because arranging an LCD into columns and rows for accessing individual pixels was well known to a POSITA as of the earliest claimed priority date. Ex. 1003, ¶¶96.31.

[3C]:

Tobiya describes that the ADC 4 subjects it to a quantization process with the greatest amplitude (set at 255) to generate a signal 12R, and outputs the resulting signal to the LUT memory means 5. Ex. 1010, ¶40. A POSITA would understand the signal 12R is a non-programmed or non-gamma-corrected signal, and Tobiya discloses storing said applied gamma voltages (e.g., the signal 12R) in said gamma reference voltage generator integrated circuits (the LUT memory means 5 which is reprogrammable and nonvolatile). Ex. 1003, ¶¶96.32.

A POSITA would also understand that Tobiya discloses that the gamma reference voltage generator integrated circuits include “reprogrammable” (rewritable) and “non-volatile” (EEPROM is nonvolatile) cells. Ex. 1003, ¶96.37. It was well known to a POSITA as of the earliest claimed priority date that a (non-volatile) memory device is divided into multiple cells, as the minimum storage unit, and different cells are “appropriate to said selected columns.” Ex. 1003, ¶96.33.

To the extent that the “applied gamma voltages” are interpreted as analog gamma reference voltages, Kang discloses the same. *See*, §VII.C.[1E].

[3D]:

See §VII.C.[1D].

[3E]:

Tobiya discloses an optimization process for optimizing gamma reference voltage levels (*see* §VII.C.[1D]) and storing the resultant gamma reference voltage levels (*see* §VII.C.[1E]). For the same reasons, Tobiya discloses “modifying said one or more different applied gamma voltages based on said one or more optimization criteria algorithms” because the optimization process, as a trial and error process, involves modifying the applied gamma voltages repeatedly until the optimization criteria have been satisfied. Ex. 1003, ¶96.36.

[3F]:

As articulated in relation to Element [1E], Tobiya discloses “programing said applied gamma voltages” (writing the resulting conversion characteristic 16 is

equivalent to writing the group of RGB signals 13) “in storage cells in said gamma reference voltage generator integrated circuits” (in the LUT memory means 5). Ex. 1003, ¶96.37. It was well known to a POSITA as of the earliest claimed priority date that a (non-volatile) memory device is divided into multiple cells, as the minimum storage unit, and different cells are “appropriate to said selected columns.” *Id.*

As articulated in relation to Element [1E], to the extent that the “gamma reference voltage levels” is interpreted as analog gamma reference voltage levels, Kang discloses it. Ex. 1003, ¶96.38.

[3G]:

Tobiya describes that the setting of the conversion characteristic 16 is also carried out on each of the green and blue colors individually in actual cases. Ex. 1010, ¶40.

A POSITA would comprehend that the optimization process is repetitive in essence to achieve “a gray level that has a linear relationship with the value of the input signal,” as stated in paragraph 4 of Tobiya. Ex. 1003, ¶96.40.

VIII. Any Secondary Considerations Cannot Overcome the Clear Evidence of Obviousness.

Evidence of secondary considerations presented by the PO should be addressed in a trial where the parties may develop, and the Board may consider, a full record. *See, e.g., Tristar Products, Inc. v. Choon’s Design, LLC*, IPR2015-01883, Paper No. 6 at 26 (PTAB Mar. 9, 2016).

IX. Discretionary Denial is Inappropriate.

The Litigation does not warrant discretionary denial under 35 U.S.C. § 314(a). Although current Patent Office guidance provides for specific briefing on this issue (*see, Interim Process for PTAB Workload Management*, March 25, 2025), Petitioner herein provides a succinct statement of the reasons why denial under Section 314(a) is not warranted.

First, the Fintiv Factors do not mandate denial of institution. *See Apple Inc. v. Fintiv, Inc.*, IPR2020-00019, Paper 11 at 6 (PTAB Mar. 20, 2020). Here, the Petition has been timely filed. Although this case has been pending for some time, the party filing this Petition (Hisense USA Corporation) has only recently been added to the Litigation, having been served on October 16, 2024.

Entities that are related to the Petitioner are not responsible for the alleged infringement as they only either assemble or sell the accused TV models or sell completed units; thus their earlier inclusion in the lawsuit should not be a factor in considering the timeliness of the Petition. Additionally, the Petition presents compelling merits. Although trial may potentially be held in January 2026, which would be before the statutory deadline for the completion of this IPR, the reality is that trial will likely be delayed. Plaintiff only filed its Fourth Amended Complaint just days ago and in so doing added additional counts of infringement. *Phenix Longhorn, LLC v. AU Optronics Corporation et al.*, No. 2:23-cv-00477, Dkt. 123

(E.D. Tex. May 12, 2025). Plaintiff has yet to update its infringement contentions. Fact discovery is still ongoing. Depositions in foreign countries still need to be scheduled and conducted.

Further, the Litigation only reflects a portion of the liability the current Petitioner is exposed to as that case involves only certain components. *See, e.g., Phenix Longhorn, LLC v. Innolux Corporation*, No. 2:23-cv-00478 (E.D. Tex. Filed Oct. 10, 2023). Thus, the trial in the Litigation will not resolve all issues between the parties. Additionally, there is no risk of injunction here as the patent has expired. That aside, PO does not participate in the commercial market and is a small shell corporation with two members/employees.

Second, although the parties have made some investment in the litigation, much is left to be completed. And although stays in the instant jurisdiction where the co-pending litigations have been filed are unlikely, there are good reasons why a stay in this case would be appropriate, including because the '788 Patent is expired.

Petitioner reserves the right to make these and additional arguments in any additional briefing regarding discretionary denials.

X. Denial Under Section 325(d) is Inappropriate.

This Petition does not present “the same or substantially the same prior art or arguments [that were] previously ... presented to the Office.” 35 U.S.C. §325(d). None of the prior art references used herein were cited in a substantive rejection

during prosecution. This is the first Petition Petitioner has filed against the '788 Patent. Petitioner again reserves the right to make these and additional arguments in any additional briefing regarding discretionary denials.

XI. Conclusion

Claims 1-3 and 5-6 are invalid.

Respectfully submitted,

By: /s/ Matias Ferrario
Matias Ferrario
Registration No. 51,082

CERTIFICATE OF WORD COUNT

The undersigned certifies pursuant to 37 C.F.R. § 42.24(d) that the foregoing **Petition for Inter Partes Review** excluding any table of contents, mandatory notices, certificates of service or word count, or appendix of exhibits or claim listing, contains 12,763 words according to the word-processing program used to prepare this paper (Microsoft Word). Petitioner certifies that this **Petition for Inter Partes Review** does not exceed the applicable type-volume limit of 37 C.F.R. § 42.24(a).

Dated: May 14, 2025

By: /s/ Matias Ferrario
Matias Ferrario
Registration No. 51,082

CERTIFICATE OF SERVICE

The undersigned hereby certifies that on the date below a copy of this **Petition for *Inter Partes* Review** has been served upon the following:

26895 Aliso Creek Road
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Aliso Viejo, CA 92656
UNITED STATES

With a courtesy copy sent via email to litigation counsel in *Phenix Longhorn LLC v. AU Optronics Corp. et al.*, 1:23-cv-00477-RWS-RSP (E.D. Tex.).

Dated: May 14, 2025

By: /s/ Matias Ferrario
Matias Ferrario
Registration No. 51,082