



**SD Specifications
Part E1
SDIO Simplified Specification**

**Version 2.00
February 8, 2007**

**Technical Committee
SD Card Association**

Revision History

Date	Version	Changes compared to previous issue
April 3, 2006	1.10	Simplified Version Initial Release
February 8, 2007	2.00	(1) Added method to change bus speed (Normal Speed up to 25MHz and High Speed up to 50 MHz) (2) Operational Voltage Requirement is extended to 2.7-3.6V (3) Combine sections 12 (Physical Properties) and 13 (Mechanical Extensions) and add miniSDIO to the new section 13 (Physical Properties) (4) Add Embedded SDIO ATA Standard Function Interface Code (5) Reference of Physical Ver2.00 supports SDHC combo card. (6) Some typos in Ver1.10 are fixed.

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Conventions Used in This Document

Naming Conventions

Some terms are capitalized to distinguish their definition from their common English meaning. Words not capitalized have their common English meaning.

Numbers and Number Bases

Hexadecimal numbers are written with a lower case "h" suffix, e.g., FFFFh and 80h.

Binary numbers are written with a lower case "b" suffix (e.g., 10b).

Binary numbers larger than four digits are written with a space dividing each group of four digits, as in 1000 0101 0010b.

All other numbers are decimal.

Key Words

May: Indicates flexibility of choice with no implied recommendation or requirement.

Shall: Indicates a mandatory requirement. Designers shall implement such mandatory requirements to ensure interchangeability and to claim conformance with the specification.

Should: Indicates a strong recommendation but not a mandatory requirement. Designers should give strong consideration to such recommendations, but there is still a choice in implementation.

Application Notes

Some sections of this document provide guidance to the host implementers as follows:

Application Note:

This is an example of an application note.

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1. General Description

The SDIO (SD Input/Output) card is based on and compatible with the SD memory card. This compatibility includes mechanical, electrical, power, signaling and software. The intent of the SDIO card is to provide high-speed data I/O with low power consumption for mobile electronic devices. A primary goal is that an SDIO card inserted into a non-SDIO aware host shall cause no physical damage or disruption of that host or its software. In this case, the SDIO card should simply be ignored. Once inserted into an SDIO aware host, the detection of the card proceeds via the normal means described in this specification with some extensions. In this state, the SDIO card is idle and draws a small amount of power (15 mA averaged over 1 second). During the normal initialization and interrogation of the card by the host, the card identifies itself as an SDIO card. The host software then obtains the card information in a tuple (linked list) format and determines if that card's I/O function(s) are acceptable to activate. This decision is based on such parameters as power requirements or the availability of appropriate software drivers. If the card is acceptable, it is allowed to power up fully and start the I/O function(s) built into it.

1.1 SDIO Features

- Targeted for portable and stationary applications
- Minimal or no modification to SD Physical bus is required
- Minimal change to memory driver software
- Extended physical form factor available for specialized applications
- Plug and play (PnP) support
- Multi-function support including multiple I/O and combined I/O and memory
- Up to 7 I/O functions plus one memory supported on one card.
- Allows card to interrupt host
- Operational Voltage range: 2.7-3.6V (Operational Voltage is used for Initialization)
- Application Specifications for Standard SDIO Functions.
- Multiple Form Factors:
 - Full-Size SDIO
 - miniSDIO

1.2 Primary Reference Document

This specification is based on and refers extensively to the SDA document:

SD Memory Card Specifications

Part 1 PHYSICAL LAYER SPECIFICATION Version 2.00 May 9, 2006

The reader is directed to this document for more information on the basic operation of SD cards. In addition, other documents are referenced in this specification. A complete list can be found in appendix B.1.

This specification can apply to any released versions of Physical Layer Specification after Version 2.00.

1.3 Standard SDIO Functions

Associated with the base SDIO specification, there are several Application Specifications for Standard SDIO Functions. These common functions such as cameras, Bluetooth cards and GPS receivers have a standard register interface, a common operation method and a standard CIS extension. Implementation of the standard interfaces are optional for any card vendor, but compliance with the standard allows the use of standard drivers and applications which will increase the appeal of these cards to the consumer. Full information on these standard interfaces can be found in the Application Specifications for Standard SDIO Functions maintained by the SDA.

2. SDIO Signaling Definition

2.1 SDIO Card Types

This specification defines two types of SDIO cards. The Full-Speed card supports SPI, 1-bit SD and the 4-bit SD transfer modes at the full clock range of 0-25MHz. The Full-Speed SDIO cards have a data transfer rate of over 100 Mb/second (10 MB/Sec). A second version of the SDIO card is the Low-Speed SDIO card. This card requires only the SPI and 1-bit SD transfer modes. 4-bit support is optional. In addition, Low-Speed SDIO cards shall support a full clock range of 0-400 KHz. The intended use of Low-Speed cards is to support low-speed I/O capabilities with a minimum of hardware. The Low-Speed cards support such functions as modems, bar-code scanners, GPS receivers etc. If a card is a 'Combo card' (memory plus SDIO) then Full-Speed and 4-bit operation is mandatory for both the memory and SDIO portions of the card.

2.2 SDIO Card modes

There are 3 signaling modes defined for SD memory cards that also apply to SDIO Card:

2.2.1 SPI (Card mandatory support)

The SPI bus topology is defined in section 3.5.2 and the protocol is defined in sections 3.6.2 and 7 of the SD Physical Specification Version 2.00. In this mode pin 8, which is undefined for memory, is used as the interrupt pin. All other pins and signaling protocols are identical to the SD Physical Specification.

2.2.2 1-bit SD Data Transfer Mode (Card Mandatory Support)

This mode is identical to the 1 data bit (narrow) mode defined for SD Memory in section 3.6.1 of the SD Physical Specification. In this mode, data is transferred on the DAT[0] pin only. In this mode pin 8, which is undefined for memory, is used as the interrupt pin. All other pins and signaling protocols are identical to the SD Memory specification.

2.2.3 4-bit SD Data Transfer Mode (Mandatory for High-Speed Cards, Optional for Low-Speed)

This mode is identical to the 4 data bit mode (wide) defined for SD Memory in section 3.6.1 of the SD Physical Specification. In this mode, data is transferred on all 4 data pins (DAT[3:0]). In this mode the interrupt pin is not available for exclusive use as it is utilized as a data transfer line. Thus, if the interrupt function is required, a special timing is required to provide interrupts. See section 8.1.2 for details of this operation. The 4-bit SD mode provides the highest data transfer possible, up to 100 Mb/sec.

2.3 SDIO Host Modes

If a SDIO aware host supports the SD transfer mode, it is recommended that both the 1-bit and 4-bit modes be supported. While a SDIO host that supports *only* the 4-bit transfer mode is possible, its performance with a Low-Speed SDIO card may be reduced. This is because the only means to transfer data to and from a Low-Speed card would be the single byte per command transfer (using the IO_RW_DIRECT command (CMD52) see 5.1).

2.4 Signal Pins

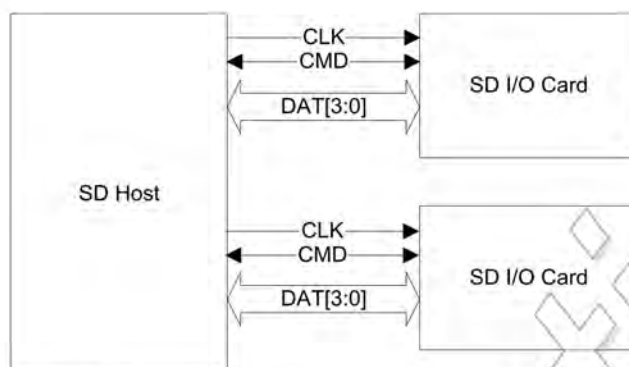


Figure 2-1 Signal connection to two 4-bit SDIO cards

The rest of this chapter is not included in the Simplified Specification.

3. SDIO Card Initialization

3.1 Differences in I/O card Initialization

A requirement for the SDIO specification is that an SDIO card shall not cause non-I/O aware hosts to fail when inserted. In order to prevent operation of I/O functions in non-I/O aware hosts, a change to the SD card identification mode flowchart is needed. A new command (IO_SEND_OP_COND, CMD5) is added to replace the ACMD41 for SDIO initialization by I/O aware hosts (see 3.2).

After reset or power-up, all I/O functions on the card are disabled and the I/O portion of the card shall not execute any operation except CMD5 or CMD0 with CS=low. If there is SD memory installed on the card (also called a combo card), that memory shall respond normally to all normal mandatory memory commands.

An I/O only card shall not respond to the ACMD41 and thus appear initially as an MMC card (See appendix B.1 for information on the MMC specification). The I/O only card shall also not respond to the CMD1 used to initialize the MMC cards and appear as a non-responsive card. The host then gives up and disables this card. Thus, the non-aware host receives no response from an I/O only card and force it to the inactive state. The operation of an I/O card with a non-I/O aware host is shown in Figure 3-1. Note that the solid lines are the actual paths taken while the dashed lines are not executed.

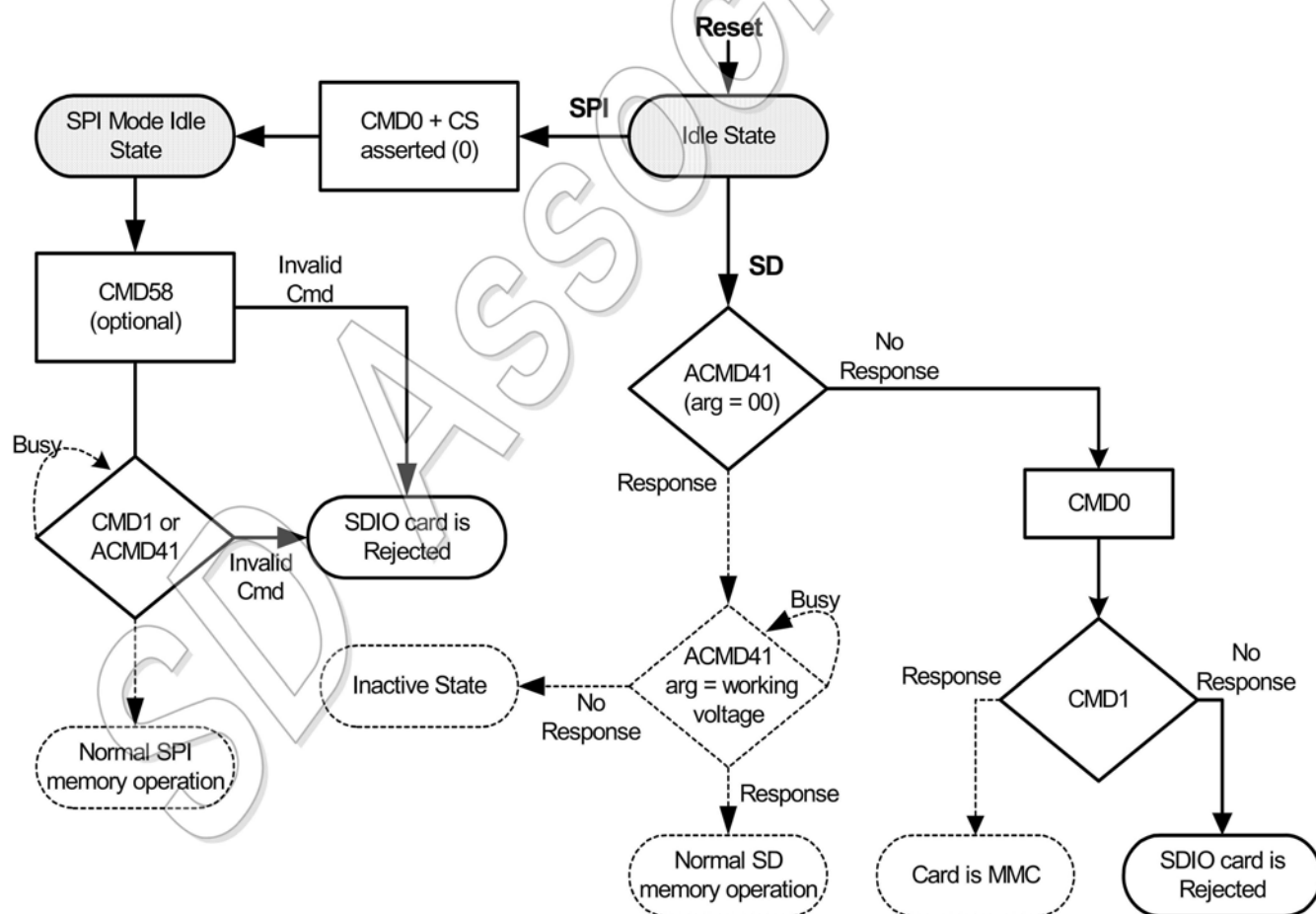


Figure 3-1 SDIO response to non-I/O aware initialization

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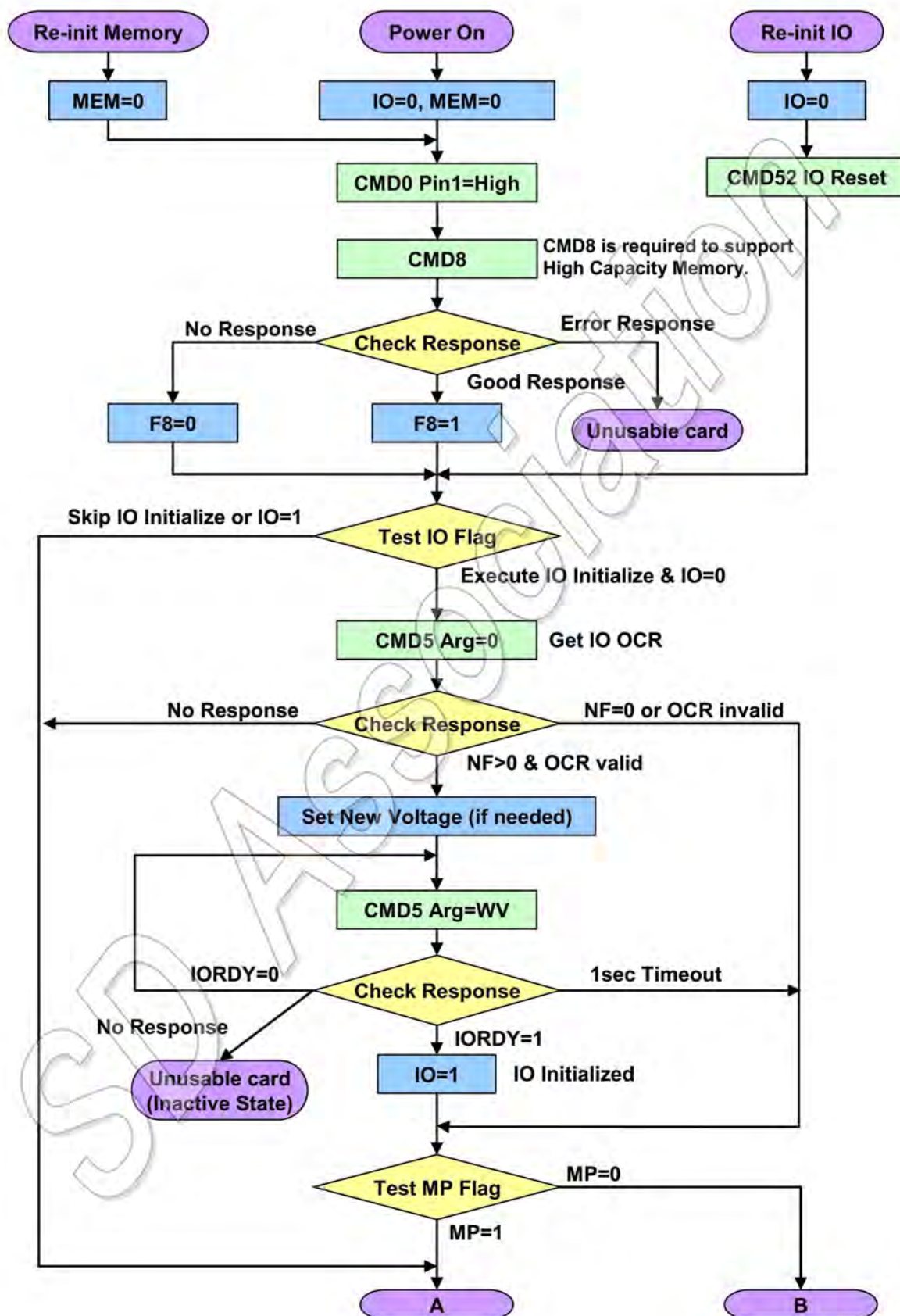
An SDIO aware host sends CMD5 prior to the CMD55/ACMD41 pair, and thus would receive a valid OCR in the R4 response to CMD5 and continue to initialize the card. Figure 3-2 shows the operation of an SDIO aware host operating in the SD modes and Figure 3-3 shows the same operation for a host that operates in the SPI mode.

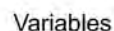
If the I/O portion of a card has received no CMD5, the I/O section remains inactive and shall not respond to any command except CMD5. A combo card stays in the memory-only mode. If no memory is installed on the card (i.e. an I/O only card in a non-SDIO aware host) the card would not respond to any memory command. This satisfies the condition where a user uses some I/O function on the card such as Ethernet to load a music file to the memory function of that card. The card is then removed and inserted into a non-SDIO aware host. That host would not enable the I/O function (no CMD5) so would appear to the player as a memory-only card. If the host were I/O aware, it would send the CMD5 to the card and the card would respond with R4. The host reads that R4 value and knows the number of available I/O functions and about the existence of any SD memory.

After the host has initialized the I/O portion of the card, it then reads the Common Information Area (CIA) of the card (see 6.8). This is done by issuing a read command, starting with the byte at address 0x00, of I/O function 0. The CIA contains the Card Common Control Registers (CCCR) and the Function Basic Registers (FBR). Also included in the CIA are pointers to the card's common Card Information Structure (CIS) and each individual function's CIS. The CIS structure is defined in section 16. The CIS includes information on power, function, manufacturer and other things the host needs to determine if the I/O function(s) is appropriate to power-up. If the host determines that the card should be activated, a register in the CCCR area enables the card and each individual function. At this time, all functions of the I/O card are fully available. In addition, the host can control the power consumption and enable/disable interrupts on a function-by-function basis. This access to I/O does not interfere with memory access to the card if present.

Combo Cards can accept CMD15 with RCA=0000, as described in, but there is an exception for SD memory only cards. Memory only cards require a non-zero RCA before the host may issue CMD15. Thus, CMD15 shall be issued after CMD3 in the Standby state. In the case of ACMD41, it shall accept RCA=0x0000.

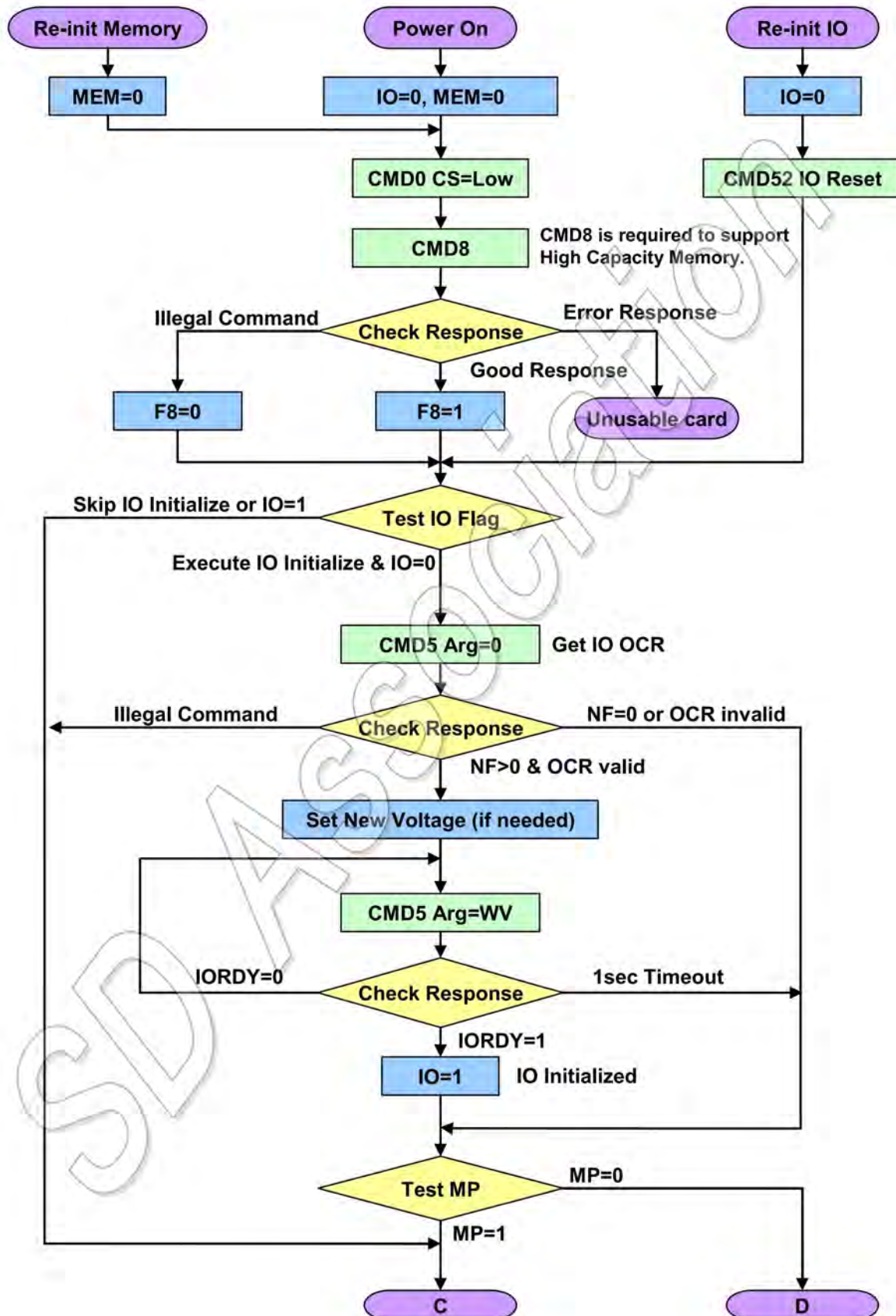
As shown in Figure 3-2 and Figure 3-3, an SDIO aware host shall send CMD5 arg=0 as part of the initialization sequence after either Power On or a CMD 52 with write to I/O Reset. Sending CMD5 arg=0 that has not been preceded by one of these two reset conditions shall not result in either the host or card entering the initialization sequence.

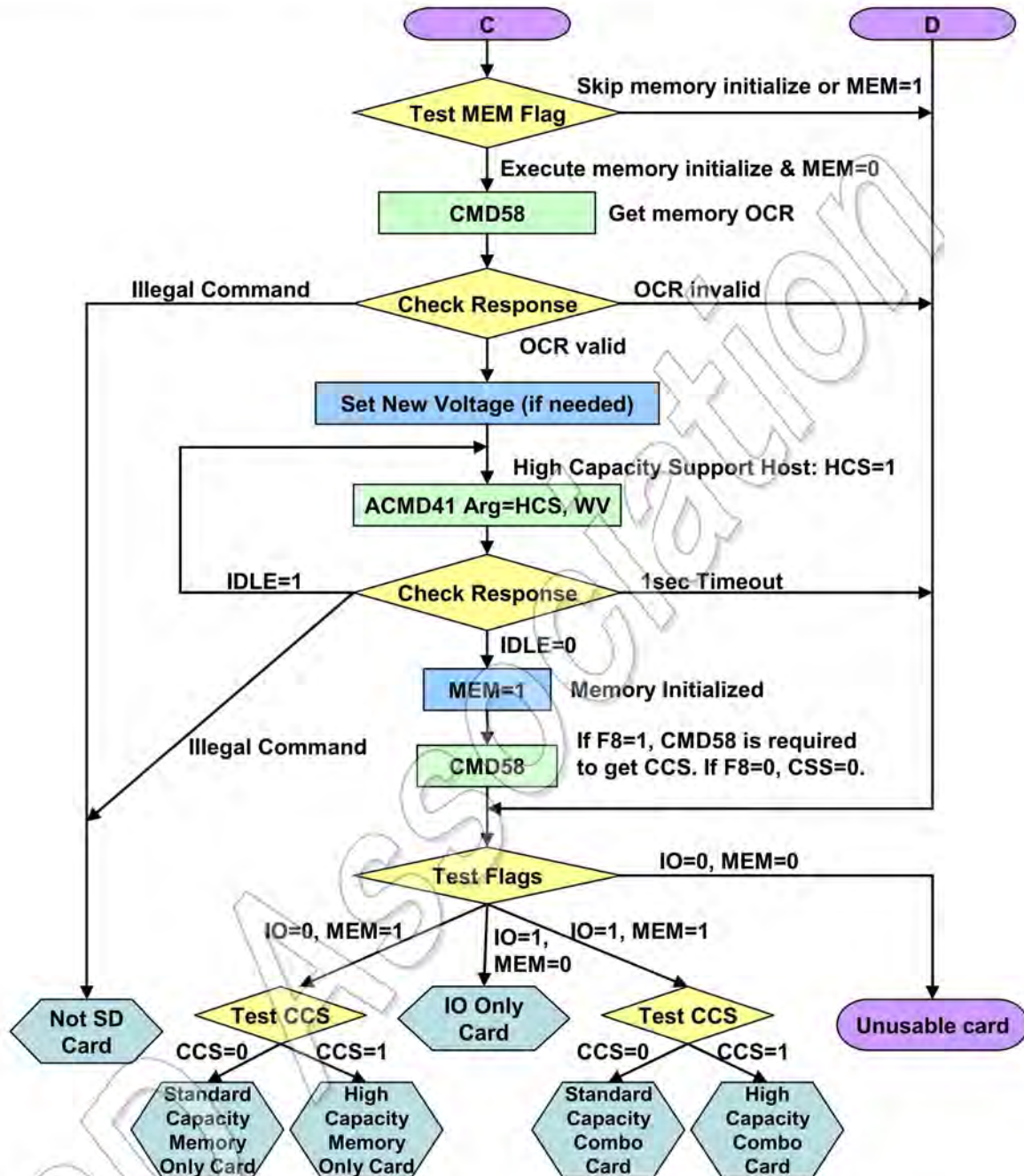




CCS:	Card Capacity Status (ACMD41 Response)
<u>Flags</u>	
IO:	I/O Functions Initialized Flag
MEM:	Memory Initialized Flag
F8:	CMD8 Flag

7



Variables

NF: Number of I/O Functions (CMD5 Response)
 MP: Memory Present Flag (CMD5 Response)
 IORDY: I/O Power-up Status (C bit in the CMD5 response)
 MRDY: Memory Power-up Status (OCR Bit31)
 HCS: Host Capacity Support (ACMD41 Argument)

CCS: Card Capacity Status (ACMD41 Response)
Flags
 IO: I/O Functions Initialized Flag
 MEM: Memory Initialized Flag
 F8: CMD8 Flag

Figure 3-3 Card initialization flow in SPI mode (SDIO aware host)

3.2 The IO_SEND_OP_COND Command (CMD5)

Figure 3-4 shows the format of the IO_SEND_OP_COND command (CMD5). The function of CMD5 for SDIO cards is similar to the operation of ACMD41 for SD memory cards. It is used to inquire about the voltage range needed by the I/O card. The normal response to CMD5 is R4 in either SD or SPI format. The R4 response in SD mode is shown in Figure 3-5 and the SPI version is shown in Figure 3-6.

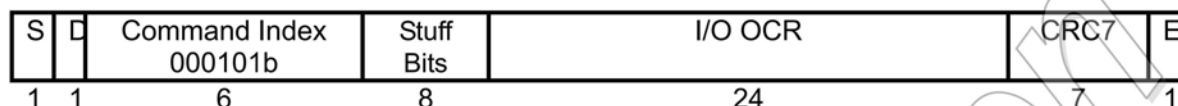


Figure 3-4 IO_SEND_OP_COND Command (CMD5)

The IO_SEND_OP_COND Command contains the following fields:

S(tart bit):	Start bit. Always 0
D(irection):	Direction. Always 1 indicates transfer from host to card.
Command Index:	Identifies the CMD5 command with a value of 000101b
Stuff Bits:	Not used, shall be set to 0.
I/O OCR:	Operation Conditions Register. The supported minimum and maximum values for VDD. The layout of the OCR is shown in Table 3-1. See section 4.10.1 for additional information.
CRC7:	7 bits of CRC data
E(nd bit):	End bit, always 1

I/O OCR bit position	VDD Voltage Window (in Volts)
0-3	Reserved
4	Reserved
5	Reserved
6	Reserved
7	Reserved
8	2.0-2.1
9	2.1-2.2
10	2.2-2.3
11	2.3-2.4
12	2.4-2.5
13	2.5-2.6
14	2.6-2.7
15	2.7-2.8
16	2.8-2.9
17	2.9-3.0
18	3.0-3.1
19	3.1-3.2
20	3.2-3.3
21	3.3-3.4
22	3.4-3.5
23	3.5-3.6

Table 3-1 OCR Values for CMD5

The SDIO Version 2.00 cards shall support the operational voltage range 2.7-3.6V and are not necessary to support the voltage range 2.0-2.7V for basic communication. The hosts, which support SDIO Version 2.00, shall not use voltage range 2.0-2.7V for basic communication.

3.3 The IO_SEND_OP_COND Response (R4)

An SDIO card receiving CMD5 shall respond with a SDIO unique response, R4. The format of R4 for both the SD and SPI modes is:

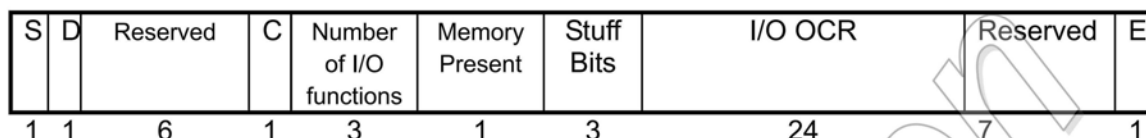


Figure 3-5 Response R4 in SD mode

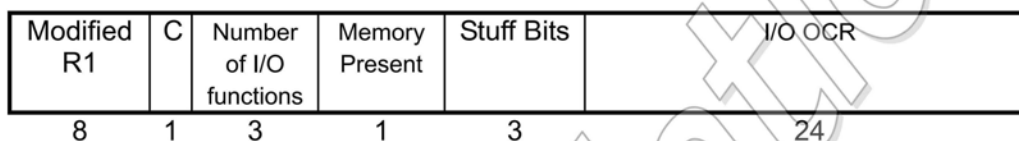


Figure 3-6 Response R4 in SPI mode

The Response, R4 contains the following data:

- S(tart bit): Start bit. Always 0
- D(irection): Direction. Always 0. Indicates transfer from card to host.
- Reserved: Bits reserved for future use. These bits shall be set to 1.
- C: Set to 1 if Card is ready to operate after initialization
- I/O OCR: Operation Conditions Register. The supported minimum and maximum values for VDD. The layout of the OCR is shown in Table 3-1. See section 4.10.1 for additional information.
- Memory Present: Set to 1 if the card also contains SD memory. Set to 0 if the card is I/O only.
- Number of I/O Functions: Indicates the total number of I/O functions supported by this card. The range is 0-7. Note that the common area present on all I/O cards at Function 0 is not included in this count. The I/O functions shall be implemented sequentially beginning at function 1.
- Modified R1: The SPI R1 response byte as described in the SD Physical Specification modified for I/O as follows:

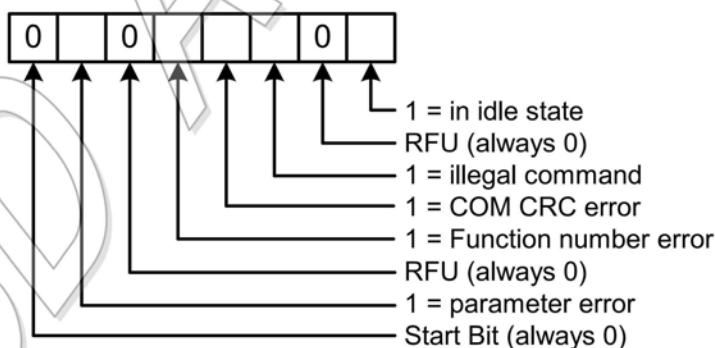


Figure 3-7 Modified R1 Response

Stuff Bits: Not used, shall be set to 0.

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Once an SDIO card has received a CMD5, the I/O portion of that card is enabled to respond normally to all further commands. This I/O enable of the functions within the I/O card shall remain set until a reset, power cycle or CMD52 with write to I/O reset is received by the card. Note that a SD memory only card *may* respond to a CMD5. The proper response for a memory only card would be *Memory Present* = 1 and *Number of I/O Functions* = 0. A memory only card built to SD Memory Card specification version 1.01 would detect the CMD5 as an illegal command and not respond. Note that unlike the similar memory command ACMD41, The SPI response to CMD5 does contain the OCR value from the card.

The I/O aware host sends CMD5. If the card responds with response R4 within the timeout value of Ncr as defined in the SD Physical Specification, the host determines the card's configuration based on the data contained within the R4.

3.4 Special Initialization considerations for Combo Cards

The host must be aware of some special situations when initializing a Combo card (SDIO plus SD Memory on the same card). This is caused because an implementation of the Combo card could actually use 2 separate controllers (Memory and I/O) in the same package and sharing the same bus lines. It is important for the host to both detect and properly configure both parts (controllers) of a Combo card in order to prevent conflicts between the SDIO and the SD memory controller. These concerns are caused due to the different response to a reset (hard or soft) by the two controllers. Another concern is the value of the RCA (Relative Card Address) that exists within the Memory controller.

Note that this consideration is for the SD 1-bit and SD 4-bit modes only. In The SPI mode, card select/de-select is accomplished using the hardware CS line rather than the RCA.

3.4.1 Re-initialize both I/O and Memory

When the host re-initializes both I/O and Memory controllers, it is *strongly* recommended that the host either execute a power reset (power off then on) or issues a reset commands to *both* controllers prior to *any* other operation. If the host chooses to use the reset commands, it shall issue CMD52 (I/O Reset) first, because it cannot issue CMD52 after CMD0 (see 4.4). After the reset, the host shall re-initialize both the I/O and Memory controller as defined in Figure 3-2.

3.4.2 Using a Combo Card as SDIO only or SD Memory only after Combo Initialization

If a host intends to use only the SDIO or the Memory portion of a Combo Card, it is *strongly* recommended that the host power reset (power off then on) or issues reset commands to *both* controllers prior to *any* other operation. If the host chooses to use the reset commands, it shall issue CMD52 (I/O Reset) first, because it cannot issue CMD52 after CMD0 (see 4.4). After the resets, the host re-initializes either the I/O and Memory controller as defined in Figure 3-2.

3.4.3 Acceptable Commands after Initialization

When the host re-initializes a Combo card, the acceptable commands that the host can issue are restricted until the I/O controller is placed into the command state and memory controller enters the transfer state. The kinds of prohibited commands are identified in the next section. Combo cards may not work correctly when the host issues these prohibited commands. The proper command sequence for the I/O controller and the memory controller are shown below. Note that CMD15 (GO_INACTIVE_STATE) can be sent at any time after initialization in order to send any addressed memory controller to the inactive state.

3.4.4 Recommendations for RCA after Reset

Important Note: The RCA specification was not fully defined in SDIO Specification Ver1.0. There are two types of card (SDIO or Combo) with different responses to CMD0 or SDIO reset. The possible responses are:

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The card clears RCA to 0x0000
The card keeps current RCA value

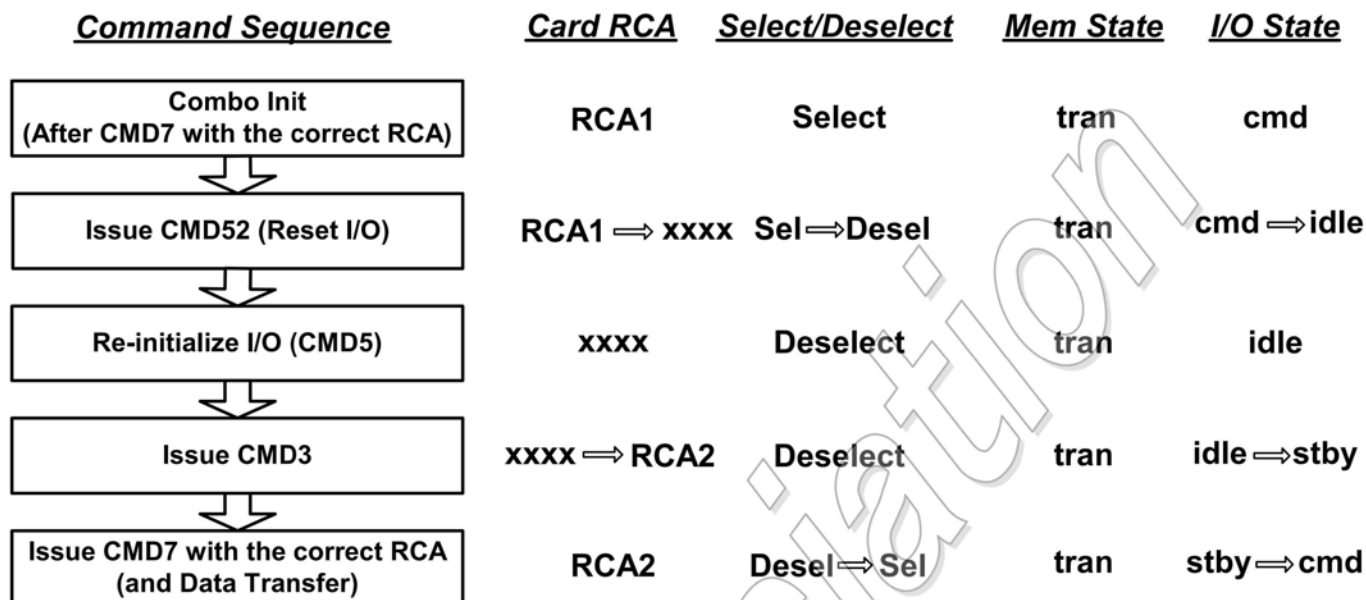


Figure 3-8 Re-Initialization Flow for I/O Controller

Figure 3-8 shows the re-initialization flow for the I/O controller of a Combo card. The flow of commands on the left side is matched with the RCA and controller states on the right side. The RCA value of xxxx denotes an RCA value of either 0x0000 or the prior RCA value. For new controller designs, a reset RCA value of 0x0000 is recommended. The host shall not issue any commands to the Combo Card except for CMD0, CMD5, CMD3 or CMD7 until the I/O controller has transitioned to the cmd state.

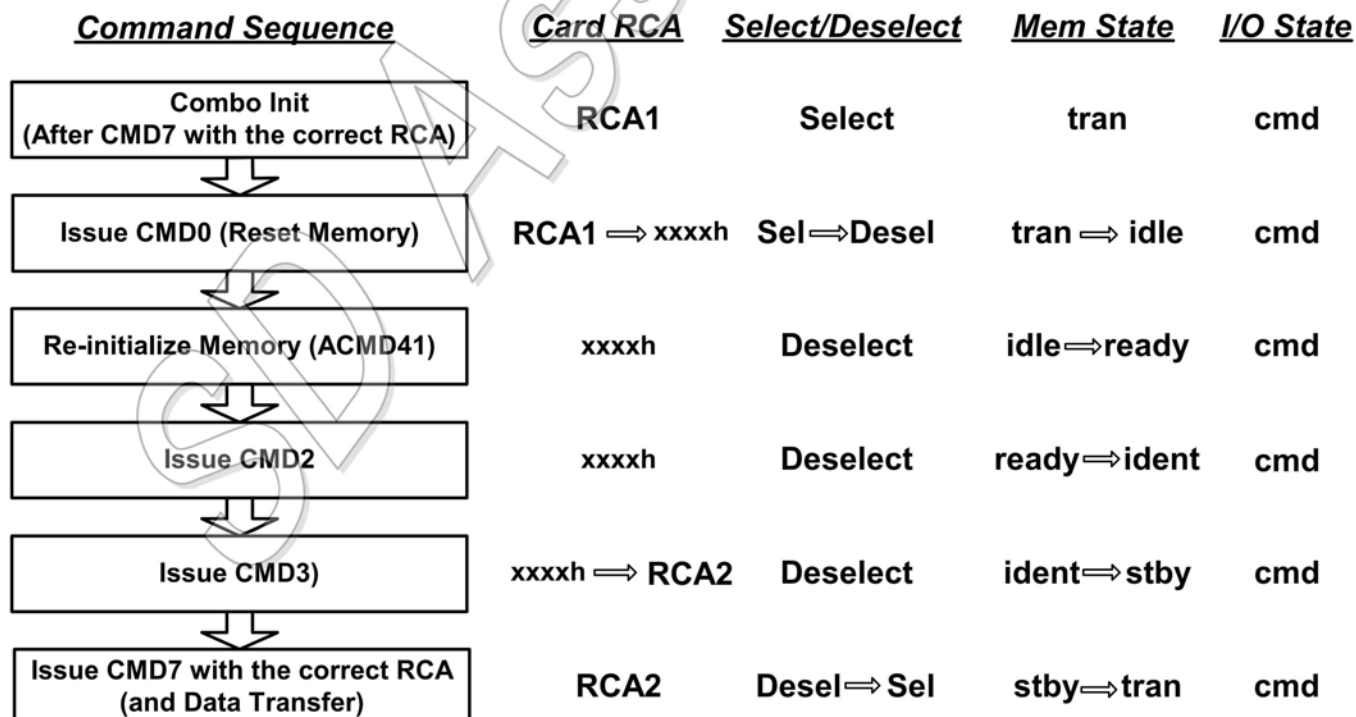


Figure 3-9 Re-Initialization Flow for Memory controller

Figure 3-9 shows the equivalent command flow to re-initialize the memory controller of a Combo card. The RCA value of xxxh denotes an RCA value of either 0x0000 or the prior RCA value. For new controller designs, a reset value of 0x0000 is recommended. The important fact for the host designer to note is that the host shall not issue any commands except for CMD0, ACMD41 (with RCA=0x0000), CMD2, CMD3 or CMD7 to the Combo Card until the memory controller has transitioned to the tran state.

3.4.5 Enabling CRC in SPI Combo Card

When receiving CMD59, Combo cards shall synchronize CRC enable in both SDIO and memory portions of the card. If a host enables CRC using CMD59 and subsequently re-initializes either the I/O or memory controller, the CRC for that controller will be off by default and the host shall issue a CMD59 to re-enable CRC. When CMD59 is received, Combo Cards return the R1 response token while SDIO only cards return the modified R1 response token.

4. Differences with SD Memory Specification

4.1 SDIO Command List

Table A-14 shows the list of commands accepted by SD memory and SDIO cards when using the SD bus interface. Table A-15 shows the list of commands accepted by SD memory and SDIO cards when using the SPI bus interface.

4.2 Unsupported SD Memory Commands

Several commands required for SD Memory cards are not supported by either SDIO-only cards or the I/O portion of Combo cards. Some of these commands have no use in SDIO cards such as Erase commands and thus are not supported in SDIO. In addition, there are several commands for SD memory cards that have different commands when used with the SDIO section of a card. Table 4-1 lists these SD Memory commands and the equivalent SDIO commands. For a complete list of supported and unsupported commands, see Table A-14 and Table A-15.

SD Memory Command	SDIO Command	Comment
CMD0	CMD52 (write to I/O reset in CCCR)	The reset command (CMD0) is only used for memory or the memory portion of Combo cards. In order to reset an I/O only card or the I/O portion of a combo card, use CMD52 to write a 1 to the RES bit in the CCCR (bit 3 of register 6). Note that in the SD mode, CMD0 is only used to indicate entry into SPI mode and shall be supported. An I/O only card or the I/O portion of a combo card is not reset with CMD0
CMD12	CMD52 (write to I/O abort)	In order to abort the block transfer of data, SD memory use CMD12. In order to abort an I/O transaction, use CMD52 to write to the abort register in the CCCR (bits 2:0 of register 6) See 4.8 for details.
CMD16	CMD52 (write to I/O Block Length)	CMD16 sets the block length for SD memory. In order to set the block length for each I/O function, use CMD52 to write the block length in the FBR
CMD2	NONE	The CID register does not exist in an SDIO only card
CMD4	NONE	The DSR register does not exist in an SDIO only card
CMD9	NONE	The CSD register does not exist in an SDIO only card
CMD10	NONE	The CID register does not exist in an SDIO only card
CMD13	NONE	An SDIO only card or the I/O portion of a combo card does not support the same SEND_STATUS (CMD13) protocol the SD memory uses. See 4.10.8.
ACMD6	CMD52 (write to Bus_Width [1:0] in CCCR)	SET_BUS_WIDTH is handled by a write to the CCCR. See 4.4 for details.
ACMD13	NONE	The SD Status register does not exist in an SDIO only card
ACMD41	CMD5	SDIO cards and hosts use the IO_SEND_OP_COND Command (CMD5). See 3.2
ACMD42	CMD52	In the SD mode, the pull-up resistor on DAT[3] is controlled by writing to the CD Disable bit in the CCCR. For Combo Cards, this resistor is enabled unless both the memory and the I/O control registers are set to disable the resistor. For details, see section 4.6
ACMD51	NONE	The SCR register does not exist in an SDIO only card
CMD17,	CMD53	I/O block operations use CMD53, rather than memory block

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SD Memory Command	SDIO Command	Comment
CMD18, CMD24, CMD25		read/write commands.

Table 4-1 Unsupported SD Memory Commands

4.3 Modified R6 Response

The normal response to CMD3 by a memory card is R6 as shown in Table 4-2. The *card status* bits (23-8) are changed when CMD3 is sent to an I/O only card. In this case, the 16 bits of response shall be the SDIO-only values shown in Table 4-3

Bit position	47	46	[45:40]	[39:8] Argument field		[7:1]	0
Width (bits)	1	1	6	16	16	7	1
Value	'0'	'0'	X	X	X	X	'1'
Description	Start bit	Direction bit	Command index ('000011')	New published RCA [31:16] of the card	[15:0] <i>Card status</i> (see Table 4-3)	CRC7	end bit

Table 4-2 R6 response to CMD3

Bits	Identifier	Type	Value	Description	Clear Condition
15	COM_CRC_ERROR	E R	'0' = no error '1' = error	The CRC check of the previous command failed	B
14	ILLEGAL_COMMAND	E R	'0' = no error '1' = error	Command not legal for the card state	B
13	ERROR	E R X	'0' = no error '1' = error	A general or an unknown error occurred during the operation	C
12: 0	Undefined. Should read as 0 for SDIO only cards. Host should ignore these bits.				

Note: Please refer to sections 7.3.4 of the SD Physical Specification for explanation of the entries in the *Type* and *Clear Condition* columns.

Table 4-3 SDIO R6 Status Bits

4.4 Reset for SDIO

In order to reset all functions within an SDIO card or the SDIO portion of a combo card, a method different than that used for SD memory is defined. The reset command (CMD0) is only used for memory or the memory portion of Combo cards. In order to reset an I/O only card or the I/O portion of a combo card, use CMD52 to write a 1 to the RES bit in the CCCR (bit 3 of register 6). Note that in the SD mode, CMD0 is only used to indicate entry into SPI mode and shall be supported. An I/O only card or the I/O portion of a combo card is **not** reset by CMD0.

4.5 Bus Width

For a SD memory card, the bus width for SD mode is set using ACMD6. The SDIO card uses a write to the CCCR using CMD52 to select bus width. In the case of a combo card, both selection methods exist. In this case, the host shall set the bus width in both locations by issuing both the ACMD6 and the CCCR write using CMD52 with the same width before starting any data transfers. For details on changing the bus for an SDIO card, see Table 6-2. . For a Combo Card, changing bus width is handled as shown in Table 4-4.

I/O	Memory	Control Method
Initialized	Not Initialized	CCCR
Not Initialized	Initialized	ACMD6
Initialized	Initialized	CCCR & ACMD6

Table 4-4 Combo Card 4-bit Control

As shown in Table 4-4, if only the I/O function of a combo card is active, only writing to the CCCR is required change the bus width mode. If only memory is active then ACMD6 is all that is needed to change bus widths. If both I/O and Memory are active then both CCCR and ACMD6 are needed to change the bus width. In the combo card, both the memory and I/O controllers shall be set to the same bus width.

Note that Low-Speed SDIO cards support 4-bit transfer as an option. When communicating with a Low-Speed SDIO card, the host shall first determine if the card supports 4-bit transfer prior to attempting to select that mode.

If a Combo card supports the lock/unlock operation, it cannot change bus width of a locked card and returns an illegal command error to a bus width switch command. The host needs to unlock the card by CMD42 before changing bus width. This also implies that the host should not change bus width during initialization before managing a locked card.

4.6 Card Detect Resistor

SD memory and I/O cards use a pull-up resistor on DAT[3] to detect card insertion. The procedure to enable/disable this resistor is different between SD memory and SDIO. SD memory uses ACMD42 to control this resistor while SDIO uses writes to the CCCR using CMD52. In the case of a combo card, both control locations exist and shall be managed by the host. For a combo card, the resistor is enabled only when both the memory and the I/O control registers have the resistor enabled. That is, after a power on, the host shall disable the resistor using ACMD42 to the memory controller or a CCCR write to the SDIO controller since the resistor enable is a logical AND of the two enables. Table 4-5 shows the effect of each resistor enable on the card's resistor. After power-up, both locations default to resistor enabled. Note that after an I/O reset, the I/O resistor enable is not changed. Note that the SDIO Specification Version 1.00 required that both the SDIO and Memory resistor be disabled in order for the resistor to actually be disabled (logical OR of the 2 enables). Combo cards built to that specification require the host to disable both enables. It is recommended the host disable both enables of any combo card to avoid problems with the difference between 1.0 and current specification based cards.

I/O Resistor	Memory Resistor	Card Resistor
Enabled	Enabled	Resistor Connected
Enabled	Disabled	Resistor Disconnected
Disabled	Enabled	Resistor Disconnected
Disabled	Disabled	Resistor Disconnected

Table 4-5 Card Detect Resistor States

4.7 Timings

This section is not included in the Simplified Specification.

4.8 Data Transfer Block Sizes

SDIO cards may transfer data in either a multi-byte (1 to 512 bytes) or an optional block format, while the SD memory cards are fixed in the block transfer mode. The SD Physical Specification limits the block size for data transfer to powers of 2 (i.e. 512, 1024, 2048) unless using partial read and write. The SDIO Specification allows any block size from 1 byte to 2048 bytes in order to accommodate the various natural block sizes for I/O functions. Note that an SDIO card function may define a maximum block size or byte count in the CIS that is smaller than the maximum values described above.

4.9 Data Transfer Abort

A host communicating with a SD memory card uses CMD12 to abort the transfer of read or write data to/from the card. For an SDIO card, CMD12 abort is replaced by a write to the ASx bits in the CCCR. Normally, the abort is used to stop an infinite block transfer (block count=0). If an exact number of blocks are to be transferred, it is recommended that the host issue a block command with the correct block count, rather than using an infinite count and aborting the data at the correct time.

4.9.1 Read Abort

The host may issue an I/O abort by writing to the CCCR at any time during I/O extended read operation. The data transmission stops 2 clocks cycles after the end bit of the I/O abort command, even if the card has already begun transferring an unwanted data block while the host is issuing the abort.

The rest of this section is not included in the Simplified Specification.

4.9.2 Write Abort

The host may issue an I/O abort by writing to the CCCR at any time between data blocks during I/O extended write operation. In this case, the final block transfer (including the CRC response from the card) shall have been completed. This requires that the end bit of the I/O abort command should appear a maximum of two clocks before the end bit of the CRC response to the last data block. Note that the I/O abort command may be sent any time after the CRC response to the last data block. The host shall not abort in the middle of a write block. After the I/O abort is sent to the card, the card signals 'Busy' (by pulling DAT[0] line to '0') until it has finished processing the last transferred data block. During that Busy period, the host may release the bus by writing to the CCCR BR bit. There exist some special cases when the abort is issued near the end of the CRC response to a write multiple command.

The rest of this section is not included in the Simplified Specification.

4.10 Changes to SD Memory Fixed Registers

The SD Physical Specification Version 1.01 defines 7 fixed card registers. They are:

1. OCR Register (32 bits)
2. CID Register (128 bits)
3. CSD Register (128 bits)
4. RCA Register (16 bits)
5. DSR Register (16 bits, optional)
6. SCR Register (64 bits)
7. SD_CARD_STATUS (512 bits)

In addition, within an SD memory card there is a status register whose value is returned to the host in the form of several responses (i.e. the R1b response). An SDIO only card eliminates some registers and changes some of the bits in the remaining registers. The description of these register changes follows:

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4.10.1 OCR Register

All SD cards (memory, I/O and combo) shall have at least one OCR register. If the card is a combo card, it *may* have two OCR's (one for memory and one for I/O). The memory portion of a combo card has an OCR accessed using ACMD41 and CMD58. The I/O portion of a card has an OCR with the same structure that is accessed via CMD5. If there are multiple OCR's the voltage range may not be identical. Some I/O functions may have a wider VDD range than that reflected in the I/O OCR register. The I/O OCR shall be the logical AND of the voltage ranges(s) of all I/O functions. Note that the I/O OCR format is different from the memory version in that it is only 24 bits long. For details, see Table 3-1. The per-function voltage for each I/O function can be read in the CIS for the card.

4.10.2 CID Register

There shall be a *maximum* of one CID register per SD card. If the card contains both memory and I/O, the CID register information is unchanged from the SD 1.01 version and reflects the information from the memory portion of the card. If the card is I/O only, the CID register and the associated access command (CMD10) are **not** supported. If the host attempts to access this register in an I/O only card, a card in SPI mode shall respond with an "Invalid Command" error response and a card in SD mode shall not respond.

4.10.3 CSD Register

There shall be a *maximum* of one CSD register per SD card. If the card contains both memory and I/O, the CSD register information is unchanged from the SD 1.01 version and reflects the information from the memory portion of the card. If the card is I/O only, the CSD register and the associated access command (CMD9) are **not** supported. If the host attempts to access this register in an I/O only card, a card in SPI mode shall respond with an "Invalid Command" error response and a card in SD mode shall not respond.

4.10.4 RCA Register

There shall only be one RCA register per SD card. The RCA value shall apply to the card as a whole. All functions and any memory share the same card address.

4.10.5 DSR Register

SDIO only cards do not support the DSR register. In the case of combo cards, support is optional as defined in the SD Physical Specification.

4.10.6 SCR Register

There shall be a *maximum* of one SCR register per SD card. If the card contains both memory and I/O, the SCR register information is unchanged from the SD 1.01 version and reflects the information from the memory portion of the card. If the card is I/O only, the SCR register and the associated access command (ACMD51) are **not** supported. If the host attempts to access this register in an I/O only card, a card in SPI mode shall respond with an "Invalid Command" error response and a card in SD mode shall not respond.

4.10.7 SD Status

There shall be a *maximum* of one SD Status register per SD card. If the card contains both memory and I/O, the SD Status register information is unchanged from the SD 1.01 version and reflects the information from the memory portion of the card. If the card is I/O only, the SD Status register and the associated access command (ACMD13) are **not** supported. If the host attempts to access this register in an I/O only card, a card in SPI mode shall respond with an "Invalid Command" error response and a card in SD mode shall not respond.

4.10.8 Card Status Register

The structure of the SDIO status register is shown in Table 4-7. For SDIO specific operations in the SD mode that return the card status register contents (i.e. the response to CMD7), some bits are not applicable to I/O operations and shall be returned as 0. These unused bits are identified as type N/A. For combo cards, the values returned shall reflect the memory status. The CURRENT_STATE bits (12:9) shall reflect the memory Controller State. For an I/O only card, the unused bits are 0 and the Current_State bits (12:9) shall be 0xF (15) to

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identify it as an I/O only response.

I/O specific status is reported by I/O response and Memory specific status is reported by Memory response except for the following case: In the SD bus mode, the card shall not respond to an Illegal Command or a command with a CRC error. The indication of those two error cases shall be given by the card in the following command's response. This is true for an I/O only card as well as for combo cards, even in cases where the erroneous command and the command that follows are not targeting the same card module (Memory or I/O).

Bit	Identifier	Type	Value	Description	Clear Condition
31	OUT_OF_RANGE	E R	'0'= no error '1'= error	The command's argument was out of the allowed range for this card.	C
30	ADDRESS_ERROR	N/A	0	Not used with SDIO operation	C
29	BLOCK_LEN_ERROR	N/A	0	Not used with SDIO operation	C
28	ERASE_SEQ_ERROR	N/A	0	Not used with SDIO operation	C
27	ERASE_PARAM	N/A	0	Not used with SDIO operation	C
26	WP_VIOLATION	N/A	0	Not used with SDIO operation	C
25	CARD_IS_LOCKED	N/A	0	Not used with SDIO operation	C
24	LOCK_UNLOCK_FAILED	N/A	0	Not used with SDIO operation	C
23	COM_CRC_ERROR	E R	'0'= no error '1'= error	The CRC check of the previous command failed. (Note 1)	B
22	ILLEGAL_COMMAND	E R	'0'= no error '1'= error	Previous command not legal for the card state. (Note 2)	B
21	CARD_ECC_FAILED	N/A	0	Not used with SDIO operation	C
20	CC_ERROR	N/A	0	Not used with SDIO operation	C
19	ERROR	E R	'0'= no error '1'= error	A general or an unknown error occurred during the operation.	C
18	UNDERRUN	N/A	0	Not used with SDIO operation	C
17	OVERRUN	N/A	0	Not used with SDIO operation	C
16	CID/ CSD_OVERWRITE	N/A	0	Not used with SDIO operation	C
15	WP_ERASE_SKIP	N/A	0	Not used with SDIO operation	C
14	CARD_ECC_DISABLED	N/A	0	Not used with SDIO operation	C
13	ERASE_RESET	N/A	0	Not used with SDIO operation	C
12:9	CURRENT_STATE	S X	15=I/O only	For an I/O only card, the current state shall be fixed at a value of 0x0F. This indicates that it is an I/O only card and the normal memory states do not apply	B
8	READY_FOR_DATA	N/A	0	Not used with SDIO operation	C
7:6	Reserved				
5	APP_CMD	N/A	0	CMD55 not used in SDIO operation	C
4	Reserved				
3	AKE_SEQ_ERROR (SD Memory Card app. spec.)	N/A	0	Not used with SDIO operation	C
2	Reserved for application specific commands				
1, 0	Reserved for manufacturer test mode				

Table 4-7 SDIO Status Register Structure

Note 1: In the SPI mode, if the card detects a CRC error, it returns a com CRC error in the R1 response immediately following the command (see Figure 3-7). In this situation, the note that the CRC error is for the previous command does not apply.

Note 2: In the SPI mode, if the card detects an Illegal Command, it returns an Illegal Command error in the R1 response immediately following the command (see Figure 3-7). In this situation, the note that the Illegal Command error is for the previous command does not apply.

5. New I/O Read/Write Commands

Two additional data transfer instructions have been added to support I/O. IO_RW_DIRECT, a direct I/O command similar to the MMC 'Fast I/O' command, and IO_RW_EXTENDED, which allows fast access with byte or block addresses. Both commands are in class 9 (I/O Commands).

5.1 IO_RW_DIRECT Command (CMD52)

The IO_RW_DIRECT is the simplest means to access a single register within the total 128K of register space in any I/O function, including the common I/O area (CIA). This command reads or writes 1 byte using only 1 command/response pair. A common use is to initialize registers or monitor status values for I/O functions. This command is the fastest means to read or write single I/O registers, as it requires only a single command/response pair.

S	D	Command Index 110100b	R/W flag	Function Number	RAW flag	Stuff	Register Address	Stuff	Write Data or Stuff Bits	CRC7	E
1	1	6	1	3	1	1	17	1	8	7	1

Figure 5-1 IO_RW_DIRECT Command

The IO_RW_DIRECT Command contains the following fields:

S(start bit):	Start bit. Always 0
D(irection):	Direction. Always 1 indicates transfer host to card.
Command Index:	Identifies the "IO_RW_DIRECT" command with a value of 110100b
R/W Flag:	This bit determines the direction of the I/O operation. If this bit is 0, this command shall read data from the SDIO card at the address specified by the Function Number and the Register Address to the host. The data byte is returned in the response, R5. If this bit is set to 1, the command shall write the bytes in the Write Data field to the I/O location addressed by the Function Number and the Register Address. If the RAW flag is 0, then the data in the register that was written shall be read and that value returned in the response.
RAW Flag:	The Read after Write flag. If this bit is set to 1 and the R/W flag is set to 1, then the command shall read the value of the register after the write. This is useful to allow writing to a control register and reading the status at the same address. If this bit is cleared, the value returned in the R5 response shall be the same as the write data in the command. If this bit is set, the data field of the R5 response shall contain the value read from the addressed register after the write operation.
Function Number:	The number of the function within the I/O card you wish to read or write. Note that function 0 selects the common I/O area (CIA).
Register Address:	This is the address of the byte of data inside of the selected function to read or write. There are 17 bits of address available so the register is located within the first 128K (131,072) addresses of that function.
Write Data/Stuff Bits:	For a direct write command (R/W=1), this is the byte that is written to the selected address. For a direct read (R/W=0), this field is not used and shall be set to 0.
CRC7:	7 bits of CRC data
E(nd bit):	End bit, always 1

5.2 IO_RW_DIRECT Response (R5)

The SDIO card's response to CMD52 shall be in one of two formats. If the communication between the card and host is in the 1-bit or 4-bit SD mode, the response shall be in a 48-bit response (R5) as described in 5.2.1. If the communication is using the SPI mode, the response shall be a 16-bit R5 response as described in 5.2.2.

5.2.1 CMD52 Response (SD modes)

The SDIO card's response to CMD52 in the SD mode is shown in Figure 5-2. If the operation was a read command, the data being read is returned as an 8-bit value. In addition, 15 bits of status information is returned. The format of the SD response is as follows:

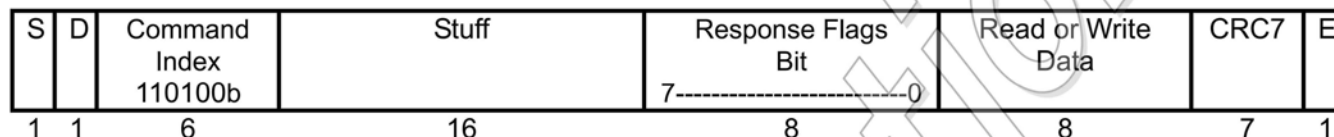


Figure 5-2 R5 IO_RW_DIRECT Response (SD modes)

The IO_RW_DIRECT response (R5) contains the following fields:

S(tart bit):	Start bit. Always 0
D(irection):	Direction. 0 indicates transfer card to host (Response)
Command Index:	Identifies the "IO_RW_DIRECT" command with a value of 110100b
Stuff Bits	Not used, shall be set to 0
Response Flags	8 Bits of flag data indicating the status of the SDIO card. Table 5-1 shows the format of these flag bits.
Read or Write Data:	For an I/O write (R/W=1) with the RAW Flag set (RAW=1) this field shall contain the value read from the addressed register <u>after</u> the write of the data contained in the command. Note that in this case, the read-back data may not be the same as the data written to the register, depending on the design of the hardware. For an I/O write with the RAW bit=0, the SDIO function shall <u>not</u> do a read after write operation, and the data in this field shall be identical to the data byte in the write command. For an I/O read (R/W=0), the actual value read from that I/O location is returned in this field.
CRC7:	7 bits of CRC data
E(nd bit):	End bit, always 1

Bits	Identifier	Type	Value	Description	Clear Condition
7	COM_CRC_ERROR	E R	'0'= no error '1'= error	The CRC check of the previous command failed.	B
6	ILLEGAL_COMMAND	E R	'0'= no error '1'= error	Command not legal for the card State.	B

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Bits	Identifier	Type	Value	Description	Clear Condition
5-4	IO_CURRENT_STATE	S	00=DIS 01=CMD 02=TRN 03=RFU	DIS=Disabled: Initialize, Standby and Inactive States (card not selected) CMD=DAT lines free: 1. Command waiting (No transaction suspended) 2. Command waiting (All CMD53 transactions suspended) 3. Executing CMD52 in CMD State TRN=Transfer: Command executing with data transfer using DAT[0] or DAT[3:0] lines	B
3	ERROR	E R E R X	'0'= no error '1'= error	A general or an unknown error occurred during the operation. Type "E R" shall be used for CMD52 Type "E R X" shall be used for CMD53	C
2	RFU	--	Fixed at 0	Reserved for Future Use	C
1	FUNCTION_NUMBER	E R	'0'= no error '1'= error	An invalid function number was requested	C
0	OUT_OF_RANGE	E R	'0'= no error '1'= error	The command's argument was out of the allowed range for this card.	C

Table 5-1 Flag data for IO_RW_DIRECT SD Response

5.2.2 R5, IO_RW_DIRECT Response (SPI mode)

The SDIO card's response to CMD52 in the SPI mode is shown in Figure 5-3. If the operation was a read command, the data being read is returned as an 8-bit value. In addition, 8 bits of status information is returned in a SPI R1 response byte as described in Fig 47 of the SD Physical Specification modified for I/O as shown in Figure 5-3.

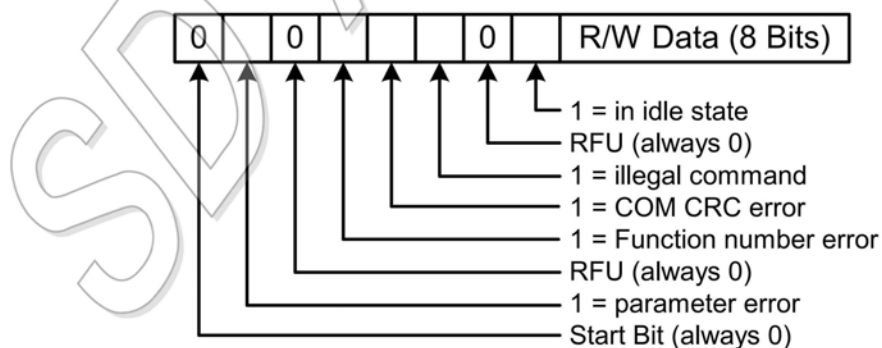


Figure 5-3 IO_RW_DIRECT Response in SPI Mode

Note the read/write (R/W) data is identical to the read/write data described for the SD R5 response (see 5.2.1). Parameter error status in SPI mode corresponds to OUT_OF_RANGE and ERROR in the SD mode response. In the case of CMD53, Data Error Token should also be used to indicate OUT_OF_RANGE and ERROR.

5.3 IO_RW_EXTENDED Command (CMD53)

In order to read and write multiple I/O registers with a single command, a new command, IO_RW_EXTENDED is defined. This command is included in command class 9 (I/O Commands). This command allows the reading or writing of a large number of I/O registers with a single command. Since this is a data transfer command, it provides the highest possible transfer rate.

S	D	Command Index	R/W flag	Function Number	Block Mode	OP Code	Register Address	Byte/Block Count	CRC	E
1	1	6	1	3	1	1	17	9	7	1
		110101b								

Figure 5-4 IO_RW_EXTENDED Command

The IO_RW_EXTENDED Command contains the following fields:

S(tart bit):	Start bit. Always 0
D(irection):	Direction. Always 1 indicates transfer host to card.
Command Index:	Identifies the "IO_RW_EXTENDED" command with a value of 110101b
R/W Flag:	This bit determines the direction of the I/O operation. If this bit is 0, this command reads data from the SDIO card at the address specified by the Function Number and the Register Address to the host. The read data shall be returned on the DAT[x] lines. If this bit is set to 1, the command shall write the bytes from the DAT[x] lines to the I/O location addressed by the Function Number and the Register Address.
Function Number:	The number of the function within the I/O card you wish to read or write. Note that function 0x00 selects the common I/O area (CIA).
Block Mode	(Optional) this bit, if set to 1, indicates that the read or write operation shall be performed on a block basis, rather than the normal byte basis. If this bit is set, the Byte/Block count value shall contain the number of blocks to be read/written. The block size for functions 1-7 is set by writing the block size to the I/O block size register in the FBR (See Table 6-3 and Table 6-4). The block size for function 0 is set by writing to the FN0 Block Size register in the CCCR. Card and host support of the block I/O mode is optional. The host can determine if a card supports block I/O by reading the <i>Card supports MBIO</i> bit (SMB) in the CCCR (see Table 6-2). The block size used when Block Mode = 1 and the maximum byte count per command used when Block Mode = 0 can be read from the CIS in the tuple TPLFE_MAX_BLK_SIZE (see 16.7.4) on a per-function basis.
OP code	Defines the read/write operation as described in Table 5-2

OP code	Command operation
0	Multi byte R/W to fixed address
1	Multi byte R/W to incrementing address

Table 5-2 IO_RW_EXTENDED command Op Code Definition

- OP Code 0 is used to read or write multiple bytes of data to/from a single I/O register address. This command is useful when I/O data is transferred using a FIFO inside of the I/O card. In this case, multiple bytes of data are transferred to/from a single register address. For this operation, the address of the register is set into the Register Address field. Data is transferred on the DAT[0] or DAT[3:0] lines as defined for SD memory cards.
- OP Code 1 is used to read or write multiple bytes of data to/from an I/O register

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address that increment by 1 after each operation. This command is used when large amounts of I/O data exist within the I/O card in a RAM like data buffer. In this operation, the start address is loaded into the Register Address field. The first operation occurs at that address within the I/O card. The next operation shall occur at address+1 with the address incrementing by 1 until the operation has completed. As with OP Code 0, the number of bytes is set in the Byte Count field of the command.

Register Address:
Byte/Block Count

Start Address of I/O register to read or write. Range is [0x1FFFF:0]
If the command is operating on bytes (Block Mode = 0), this field contains the number of bytes to read or write. A value of 0x000 shall cause 512 bytes to be read or written.

Count Value	0x000	0x001	0x002	----	0x1FF
Bytes Transferred	512	1	2		511
Block Transferred	∞	1	2		511

Table 5-3 Byte Count Values

If the command is in block mode (Block Mode=1), the Block Count field specifies the number of Data Blocks to be transferred following this command. A value of 0x000 indicates that the count set to infinite. In this case, the I/O blocks shall be transferred until the operation is aborted by writing to the I/O abort function select bits (ASx) in the CCCR (see Table 6-1 and Table 6-2). Table 5-3 shows the relationship between the value in the command and the actual number of bytes transferred.

CRC7:
E(nd bit):

7 bits of CRC data
End bit, always 1

The response from the SDIO card to CMD53 shall be R5 (the same as CMD52) as defined in 5.2. For CMD53, the 8-bit data field shall be stuff bits and shall be read as 0x00. Also, the ERROR response bit shall be type "E R X" (see Table 5-1).

5.3.1 CMD53 Data Transfer Format

When executing the IO_RW_EXTENDED (CMD53), the multi-byte or multi-block data transfer is similar to the data transfer for memory. For the multi-byte transfer modes (block mode=0) the following applies:

IO_RW_EXTENDED byte read is similar to CMD17 (READ_SINGLE_BLOCK)

IO_RW_EXTENDED byte write is similar to CMD24 (WRITE_BLOCK)

Note that the byte count for this transfer is set in the command, rather than the fixed block size. Thus, the size of the data payload is in the range of 1-512 bytes. The block mode is similar to the following memory commands:

IO_RW_EXTENDED block read is similar to CMD18 (READ_MULTIPLE_BLOCK)

IO_RW_EXTENDED block write is similar to CMD25 (WRITE_MULTIPLE_BLOCK)

For the block mode the only difference is that for a fixed block count, the host does not need to stop the transfer, as it continues until the block count is satisfied. If the block count is set to zero, the operation is identical to the memory mode in that the host must stop the transfer.

5.3.2 Special Timing for CMD53 Multi-Block Read

This section is not included in the Simplified Specification.

6. SDIO Card Internal Operation

I/O access differs from memory in that the registers can be written and read individually and directly without a FAT file structure or the concept of blocks (although block access is supported). These registers allow access to the I/O data, control of the I/O function and report on status or transfer I/O data to/from the host. The SD memory relies on the concept of a fixed block length with commands reading/writing multiples of these fixed size blocks. I/O may or may not have fixed block lengths and the read size may be different from the write size. Because of this, I/O operations may be based on either a length (byte count) or a block size.

6.1 Overview

Each SDIO card may have from 1 to 7 functions plus one memory function built into it. A function is a self contained I/O device. I/O functions may be identical or completely different from each other. All I/O functions are organized as a collection of registers. There is a maximum of 131,072 (2^{17}) registers possible for each I/O function. These registers and their individual bits may be read Only (RO), Write Only (WO) or Read/Write (R/W). These registers can be 8, 16 or 32 bits wide within the card. All addressing is based on byte access. These registers can be written and/or read one at a time, multiply to the same address or multiply to an incrementing address. The single R/W access is often used to initialize the I/O function or to read a single status or data value. The multiple reads to a fixed address are used to read or write data from a data FIFO register in the card. The read to incrementing addresses is used to read or write a collection of data to/from a RAM area inside of the card. Figure 6-1 shows the mapping of the CIA and optional CSA space for an SDIO card.

6.2 Register Access Time

All registers in SDIO only cards and the SDIO portion of Combo cards shall complete read and write data transfer in less than 1 second. This timeout value relates to the time for the requested data to be transferred to/from the host on the DAT[x] lines and not the timing between the command and the response. This wait time is signaled to the host by the card using busy for a write or delaying the start bit for a read operation. The host can use 1 second as the timeout value for a non-responding location. If a functions needs to support an access time greater than 1 second, the card maker may use some function specific method that is not defined in this specification.

6.3 Interrupts

All SDIO hosts should support hardware interrupts. If a host does not support interrupts, it may have difficulties working with SDIO cards that expect fast response to interrupt conditions. Each function within an SDIO or Combo card may implement interrupts as needed. The interrupt used on SDIO functions is a type commonly called "level sensitive". Level sensitive means that any function may signal for an interrupt at any time, but once the function has signaled an interrupt, it shall not release (stop signaling) the interrupt until the cause of the interrupt is removed or commanded to do so by the host. Since there is only 1 interrupt line, it may be shared by multiple interrupt sources. The function shall continue to signal the interrupt until the host responds and clears the interrupt. Since multiple interrupts may be active at once, it is the responsibility of the host to determine the interrupt source(s) and deal with it as needed. This is done on the SDIO function by the use of two bits, the interrupt enable and interrupt pending. Each function that may generate an interrupt has an interrupt enable bit. In addition, the SDIO card has a master interrupt enable that controls all functions. An interrupt shall only be signaled to the SD bus if both the function's enable and the card's master enable are set. The second interrupt bit is called interrupt pending. This read-only bit tells the host which function(s) may be signaling for an interrupt. There is an interrupt pending bit for each function that can generate interrupts. These bits are located in the CCCR area. For more details, see Table 6-1 and Table 6-2. Interrupt operation is described more fully in section 8.

6.4 Suspend/Resume

Within a multi-function SDIO or a Combo card, there are multiple devices (I/O and memory) that share access to the SD bus. In order to allow the sharing of access to the host among multiple devices, SDIO and combo cards can implement the *optional* concept of suspend/resume. If a card supports suspend/resume, the host may temporarily halt a data transfer operation to one function or memory (suspend) in order to free the bus for a higher priority transfer to a different function or memory. Once this higher-priority transfer is complete, the original transfer is re-started where it left off (resume). Support of suspend/resume is optional on a per-card basis. If suspend/resume is implemented, it shall be supported by the memory (if any) of a Combo card and all I/O functions *except* 0 (the CIA). Note that the host can suspend multiple transactions and resume them in any order desired. I/O function 0 does **not** support suspend/resume. Suspend/Resume is described in more detail in section 9. Any card that supports Suspend/Resume shall also support Read Wait and Direct Commands (SRW and SDC = 1) Note that Suspend/Resume is defined only for the SD 1 and 4-bit modes. It does not apply to SPI transfers.

6.5 Read Wait

Host devices built to the SD Physical Specification shall control the SDCLK to stop the read data block output from a card executing a multiple read command whenever the host cannot accept more data. During the time that the host has stopped the SDCLK, a CMD52 cannot be issued. This limitation causes a problem in that a host device built to the SD Physical Specification cannot perform the I/O command during a multiple read cycle.

In order to eliminate this limitation, the SDIO Specification adds the Read Wait control to enable the host to issue CMD52 during a multiple read cycle. Read Wait uses the DAT[2] line to allow the host to signal the card to temporarily halt the sending of read data by a card. This feature is optional for an SDIO or combo card. However, if an SDIO or combo supports Read Wait, all functions and any memory shall support Read Wait. Read Wait is described in more detail in section 10. Any card that supports Suspend/Resume shall also support Read Wait. Note that Read Wait is defined only for the SD 1 and 4-bit modes. It does not apply to SPI transfers.

6.6 CMD52 During Data Transfer

A card may accept CMD52 during data transfer if it supports Direct Commands (see SDC, Table 6-3). For both SD and SPI modes, if an error occurs during data transfer the SDIO card shall accept CMD52 to allow I/O abort and reset regardless of this bit value of the value of SDC.

6.7 SDIO Fixed Internal Map

The SDIO card has a fixed internal register space and a function unique area. The fixed area contains information about the card and certain mandatory and optional registers in fixed locations. The fixed locations allow any host to obtain information about the card and perform simple operations such as enable in a common manner. The function unique area is a per-function area, which is defined either by the Application Specifications for Standard SDIO functions or by the vendor for non-standard functions. Figure 6-1 shows the internal map of an SDIO card with multiple functions.

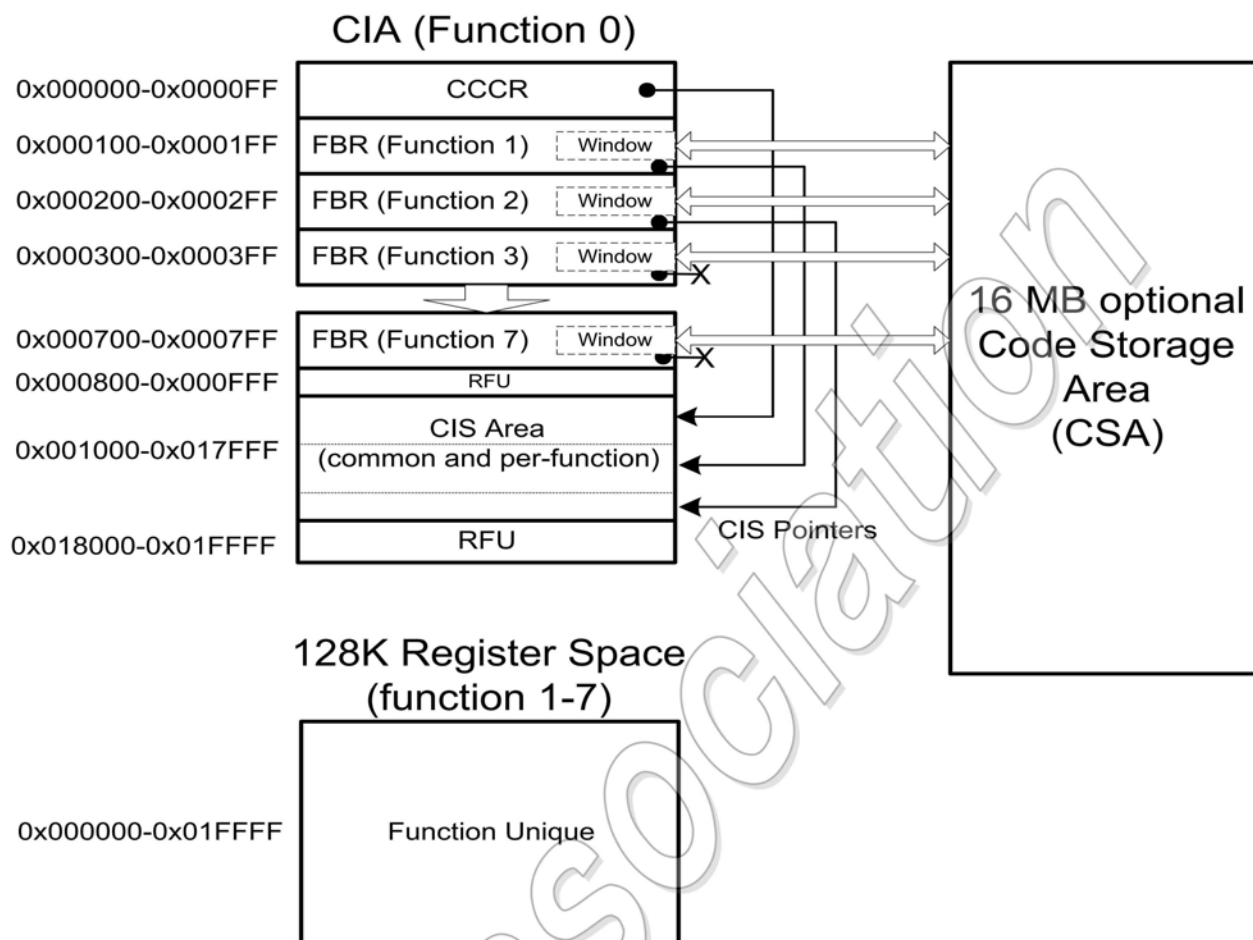


Figure 6-1 SDIO Internal Map

6.8 Common I/O Area (CIA)

The Common I/O Area (CIA) shall be implemented on all SDIO cards. The CIA is accessed by the host via I/O reads and writes to function 0. The registers within the CIA are provided to enable/disable the operation of the I/O function(s), control the generation of interrupts and optionally load software to support the I/O functions. The registers in the CIA also provide information about the function(s) abilities and requirements. There are three distinct register structures supported within the CIA. They are:

1. Card Common Control Registers (CCCR)
2. Function Basic Registers (FBR)
3. Card Information Structure (CIS)

6.9 Card Common Control Registers (CCCR)

The Card Common Control Registers allow for quick host checking and control of an I/O card's enable and interrupts on a per card (master) and per function basis. The bits in the CCCR are mixed Read/Write and read only. If any of the possible 7 functions are not provided on an SDIO card, the bits corresponding to unused functions shall all be read-only and read as 0. All reserved for future use bits (RFU) shall be read-only and return a value of 0. All writeable bits are set to 0 after power-up or reset. Access to the CCCR is possible even after initialization when the I/O functions are disabled. Access is performed using the I/O read and write commands defined in section 5. This allows the host to enable functions after initialization. The CCCR is organized as follows: