

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC. AND
MICRON SEMICONDUCTOR PRODUCTS, INC.,
Petitioner

v.

PALISADE TECHNOLOGIES, LLP,
Patent Owner.

Case No. IPR2025-01009
U.S. Patent No. 9,281,314

**DECLARATION OF DAVID KUAN-YU LIU, PH.D., IN SUPPORT OF
PETITION FOR *INTER PARTES* REVIEW OF U.S. PATENT NO. 9,281,314**

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LIST OF EXHIBITS¹

Ex-1001	U.S. Patent No. 9,281,314 (“the ’314 Patent”)
Ex-1002	Declaration of Dr. David Kuan-Yu Liu
Ex-1003	Curriculum Vitae of Dr. David Kuan-Yu Liu
Ex-1004	Prosecution History of U.S. Patent No. 9,281,314 (App. No. 14/511,834)
Ex-1005	U.S. Patent No. 7,598,564 (“Kang”)
Ex-1006	U.S. Patent App. Pub. No. 2007/0096202 (“Kang-1”)
Ex-1007	U.S. Patent App. Pub. No. 2011/0309425 (“Purayath”)
Ex-1008	U.S. Patent No. 7,759,722 (“Murata”)
Ex-1009	[Intentionally left blank]
Ex-1010	[Intentionally left blank]
Ex-1011	[Intentionally left blank]
Ex-1012	[Intentionally left blank]
Ex-1013	[Intentionally left blank]
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Ex-1020	Claim Mapping Table
Ex-1021	Rino Micheloni et al., <i>Inside NAND Flash Memories</i> (2010)
Ex-1022	Complaint, <i>Palisade Techs, LLP v. Micron Tech., Inc. and Micron Semiconductor Prods., Inc.</i> , No. 7:24-cv-00262 (W.D. Tex. Oct. 16, 2024), ECF No. 1
Ex-1023	First Amended Complaint, <i>Palisade Techs, LLP v. Micron Tech., Inc. and Micron Semiconductor Prods., Inc.</i> , No. 7:24-cv-00262 (W.D. Tex. Dec. 19, 2024), ECF No. 20
Ex-1024	G. Groeseneken et al., <i>Basics of Nonvolatile Semiconductor Memory Devices, in Nonvolatile Semiconductor Memory Technology: A Comprehensive Guide to Understanding and Using NVSM Devices</i> (William D. Brown & Joe Brewer eds., 1997)

¹ Four-digit pin citations that begin with 0 are the page stamps added by Micron in the bottom right corner of the exhibits. All other pin citations are to original page, column, paragraph, or line numbers.

Ex-1025	S. Ahn et al., <i>Influence of the Oxidation in the Metal Silicide/Si₃N₄ Interfaces on the Etching Profile</i> , 77 Microelectronic Eng'g 8 (2005)
Ex-1026	T. Mikolajick et al., <i>The Future of Charge Trapping Memories</i> , 2007 IEEE Int'l Symposium on VLSI Tech., Sys. & Applications (2007)
Ex-1027	U.S. Patent No. 9,589,978 ("Yip")
Ex-1028	Seiichi Aritome, <i>NAND Flash Memory Technologies</i> (2016)
Ex-1029	Jim Handy, <i>3D NAND: Benefits of Charge Traps over Floating Gates</i> , The Memory Guy Blog (Nov. 22, 2013)
Ex-1030	U.S. Patent No. 6,859,397 ("Lutze")
Ex-1031	Silicon Processing for the VLSI Era, Volume 1: Process Technology (2d ed.)
Ex-1032	Mincheol Park et al., <i>Effect of low-k dielectric material on 63nm MLC (multi-level cell) NAND flash cell arrays</i> , IEEE VLSI-TSA International Symposium on VLSI Technology (2005)
Ex-1033	Daewoong Kang et al., <i>The Air Spacer Technology for Improving the Cell Distribution in 1 Giga Bit NAND Flash Memory</i> , 21st IEEE Non-Volatile Semiconductor Memory Workshop (2006)

I. INTRODUCTION

1. Micron Technology, Inc. and Micron Semiconductor Products, Inc. (collectively, “Petitioner”) request *inter partes* review (“IPR”) of Claims 1-7, 13-14, 17-19 of U.S. Patent No. 9,281,314 (“the ’314 Patent”) (Ex-1001), currently assigned to Palisade Technologies, LLP (“PO”).

2. I have been retained by Micron Technology, Inc. and Micron Semiconductor Products, Inc. (collectively, “Petitioner”), as an independent expert in this proceeding before the Patent Trial and Appeal Board (“PTAB” or “Board”). I understand that Petitioner is requesting that the Board institute an *inter partes* review (“IPR”) proceeding of U.S. Patent No. 9,281,314 (“the ’314 Patent”) (Ex-1001), currently assigned to Palisade Technologies, LLP (“Patent Owner” or “PO”).

3. I am not and have never been an employee of Petitioner. I am being compensated at my usual and customary hourly rate of \$600 for time testifying and \$550 for all other time. No part of my compensation depends on the outcome of this proceeding, and I have no other interest in this proceeding.

4. I have been asked to provide my independent analysis of Claims 1-7, 13-14, 17-19 of the ’314 Patent in light of the prior art publications cited below. I have also been asked to consider the state of the art and prior art available as of October 10, 2014. Based on the prior art discussed in this declaration, it is my

opinion that Claims 1-7, 13-14, 17-19 of the '314 Patent are unpatentable for the reasons provided below.

II. BACKGROUND AND QUALIFICATIONS

5. My curriculum vitae (“CV”) is filed concurrently as Ex-1003 and provides an accurate identification of my background and experience. Among other things, my CV includes a list of my issued patents and publications for at least the last 30 years. My CV also includes information about my expert witness experience, with case numbers where available.

6. I received a Bachelor of Science in Electrical Engineering from the University of California, Berkeley, in 1983. I received a Master of Science and Ph.D. in Electrical Engineering from Stanford University in 1985 and 1989, respectively.

7. I worked on a novel Conductivity Modulated Power MOSFET for my Ph.D. thesis. The novel device uses a trench injector to facilitate an optimal tradeoff between the breakdown voltage and ON-Resistance of a Power MOSFET (Vertical DMOS) through the use of a minority carrier injector.

8. From 1989 to 1992, I was a member of technical staff at Texas Instruments, Inc. (“TI”). At TI, my job responsibilities included process integration, device modeling, high-voltage CMOS process integration, and investigating novel source-side injection mechanisms for Flash EPROM channel hot-electron programming.

9. From 1992 to 1995, I was a member of the technical staff at Advanced Micro Devices, Inc. (“AMD”) where I was a key contributor in optimizing Flash cell and periphery devices in AMD’s CMOS-based 0.5μm and 0.35μm Flash EPROM technology. My job responsibilities at AMD also included process integration, device modeling, and development of triple-well process technology to accommodate x-decoder transistors and high-voltage transistors for negative gate erase operations. While at AMD, I was awarded a Spotlight Award for developing a method of manufacturing a self-aligned source (SAS) etch for a NOR flash memory.

10. I spent the next five years of my career in managerial and director roles at several California-based semiconductor companies. I was responsible for increasing yield and for leading teams of engineers working to develop next-generation memory devices.

11. In 2000, I co-founded Progressant Technologies in Fremont, California. Progressant Technologies developed IP for negative differential resistance transistor technology and was eventually acquired by Synopsys, Inc.

12. From 2000 to 2004, I was a Senior Manager at Xilinx, Incorporated, where I was responsible for developing nonvolatile memory process technology for flash and CPLD product applications, as well as advanced CMOS process technology (specifically 75nm CMOS technology node, a half node version between 90nm and 65nm).

13. From 2004 to 2007, I was a Senior Scientist at Maxim Integrated Products where I was responsible for developing Embedded Non-volatile Memory process technology for Power Management product applications.

14. Since 2007, I have served as a technical consultant where I have provided expert advice regarding Flash memory technology, CMOS process technology, and semiconductor device physics. As part of this, I have considered, assessed, and assisted with the design of various different memory devices, including NAND flash and monolithic 3D memory structures.

15. I hold over 99 U.S. patents, a vast majority of which are directly related to Nonvolatile memory device technology. For example, U.S. Patent No. 5,250,464 relates to use of sidewall layers of silicone dioxide and silicon nitride to form a sidewall anti-fuse structure.

16. I am not now and have never been an employee of the Petitioner.

III. INFORMATION CONSIDERED

17. In preparation for this declaration, I have considered the materials discussed in this declaration, including, for example, the '314 Patent, the references cited by the '314 Patent, the prosecution history of the '314 Patent and applications from which it derives (including the references cited therein), various background articles and materials referenced in this declaration, and the prior art references identified in this declaration.

18. In forming the opinions expressed below, I have considered: the documents listed above, any additional documents discussed below, and my education, training, experience, and knowledge in the relevant field of multimedia processing or communications networks.

IV. RELEVANT LEGAL STANDARDS

19. In forming my opinions and considering the subject matter of the '314 Patent and its claim in light of the prior art, I am relying on certain legal principles that counsel in this case explained to me. My understanding of these concepts is summarized below.

A. Claim Interpretation

20. I have been informed and understand that in an IPR proceeding, claims are to be interpreted according to the Phillips claim construction standard. I have been informed and understand that claim construction is a matter of law and that the final claim constructions for this proceeding will be determined by the PTAB.

B. Perspective of One of Ordinary Skill in the Art

21. I have been informed and understand that a patent is to be understood from the perspective of a hypothetical “person of ordinary skill in the art” (“POSITA”). Such an individual is considered to possess normal skills and knowledge in a particular technical field (as opposed to being a genius). I understand that in considering what the claims of a patent require, what was known prior to that

patent, what a prior art reference discloses, and whether an invention is obvious or not, one must use the perspective of such a POSITA.

22. A POSITA at the relevant time would have had a bachelor's degree in electrical engineering, computer engineering, or a related field, and at least two years of experience in the research, design, or development of semiconductor memory device structures, or the equivalent, with additional education substituting for experience and vice versa. I believe that I possessed and exceeded such experience and knowledge before and at the priority date and that I am qualified to opine on the '314 Patent.

C. Obviousness

23. I have been informed and understand that a patent claim is obvious under 35 U.S.C. §103, and therefore invalid, if the claimed subject matter, as a whole, would have been obvious to a POSITA as of the priority date of the patent based on one or more prior art references and/or the knowledge of a POSITA.

24. I understand that an obviousness analysis must consider (1) the scope and content of the prior art, (2) the differences between the claims and the prior art, (3) the level of ordinary skill in the pertinent art, and (4) secondary considerations, if any, of non-obviousness (such as unexpected results, commercial success, long felt but unmet need, failure of others, copying by others, and skepticism of experts).

25. I understand that a prior art reference may be combined with other references to disclose each element of the invention under 35 U.S.C. §103. I understand that a reference may also be combined with the knowledge of a POSITA, and that this knowledge may be used to combine multiple references. I further understand that a POSITA is presumed to know the relevant prior art. I understand that the obviousness analysis may take into account the inferences and creative steps that a POSITA would employ.

26. In determining whether a prior art reference would have been combined with other prior art or other information known to a POSITA, I understand that the following principles may be considered:

- whether the references to be combined involve non-analogous art;
- whether the references to be combined are in different fields of endeavor than the alleged invention in the Patent;
- whether the references to be combined are reasonably pertinent to the problems to which the inventions of the Patent are directed;
- whether the combination is of familiar elements according to known methods that yields predictable results;
- whether a combination involves the substitution of one known element for another that yields predictable results;
- whether the combination involves the use of a known technique to

improve similar items or methods in the same way that yields
predictable results;

- whether the combination involves the application of a known technique to a prior art reference that is ready for improvement, to yield predictable results;
- whether the combination is “obvious to try”;
- whether the combination involves the known work in one field of endeavor prompting variations of it for use in either the same field or a different one based on design incentives or other market forces, where the variations are predictable to a POSITA;
- whether there is some teaching, suggestion, or motivation in the prior art that would have led one of ordinary skill in the art to modify the prior art reference or to combine prior art reference teachings to arrive at the claimed invention;
- whether the combination requires modifications that render the prior art unsatisfactory for its intended use;
- whether the combination requires modifications that change the principle of operation of the reference;
- whether the combination is reasonably expected to be a success; and
- whether the combination possesses the requisite degree of predictability

at the time the invention was made.

27. I understand that in determining whether a combination of prior art references renders a claim obvious, it is helpful to consider whether there is some teaching, suggestion, or motivation to combine the references and a reasonable expectation of success in doing so. I understand, however, that a teaching, suggestion, or motivation to combine is not required.

V. RELIEF REQUESTED

28. I understand that Petitioner challenges the validity of Claims 1-7, 13-14, 17-19 of the '314 Patent. In particular, I understand that Petitioner asserts the following grounds for challenging the claims of the '314 Patent:

Ground	Summary
1	Claims 1, 3-4, 6-7, 13, 17, and 19 are obvious over U.S. Patent No. 7,598,564 ("Kang") (Ex-1005).
2	Claims 1-2, 5-6, 14, and 18 are obvious over Kang in view of U.S. Patent App. Pub. No. 2007/0096202 ("Kang-1") (Ex-1006).
3	Claim 1-2, 4-6, 13-14, 18-19 are obvious over U.S. Patent App. Pub. No. 2011/030942 ("Purayath") (Ex-1007).
4	Claims 3, 7, and 17 are obvious over Purayath in view of U.S. Patent

Ground	Summary
	No. 7,759,722 (“Murata”) (Ex-1008).

VI. THE CHALLENGED PATENT

A. Priority Date

29. The earliest possible priority for the ’314 Patent is October 10, 2014. Ex-1022 ¶21; Ex-1023 ¶22. I take no position on the proper priority date for each claim of the ’314 Patent.

B. The ’314 Patent

30. The ’314 Patent discloses, “[n]on-volatile storage devices and methods for fabricating non-volatile storage device[s].” Ex-1001, code (57). “With the ever decreasing size of features, combating breakdown voltage can be difficult.” *Id.*, 1:51-53. For example, “[a]s the distance between word lines decreases, breakdown voltage may become a greater problem. Moreover, some conventional techniques for combating breakdown voltage lead to other problems, such as undesirably trapping charges in dielectric materials.” *Id.*, 1:54-59. The ’314 Patent describes using silicon oxide to cover the sidewalls of the memory cells and the word line and using silicon nitride to “cover[] the silicon oxide adjacent to the word lines, which may provide protection for the word lines during fabrication.” *Id.*, 1:62-66. The ’314 Patent notes that “silicon nitride can trap charges, which can degrade operation if the trapped charges are near a charge trapping region of a memory cell. Thus, the silicon

nitride does not cover the silicon oxide adjacent to charge storage regions of the memory cells....” *Id.*, 1:66-2:5.

31. Figure 7 “is a flowchart of one embodiment of a process of fabricating memory cells,” and Figures 8A-8F “depict formation after various steps in the process.” *Id.*, 8:8-11.

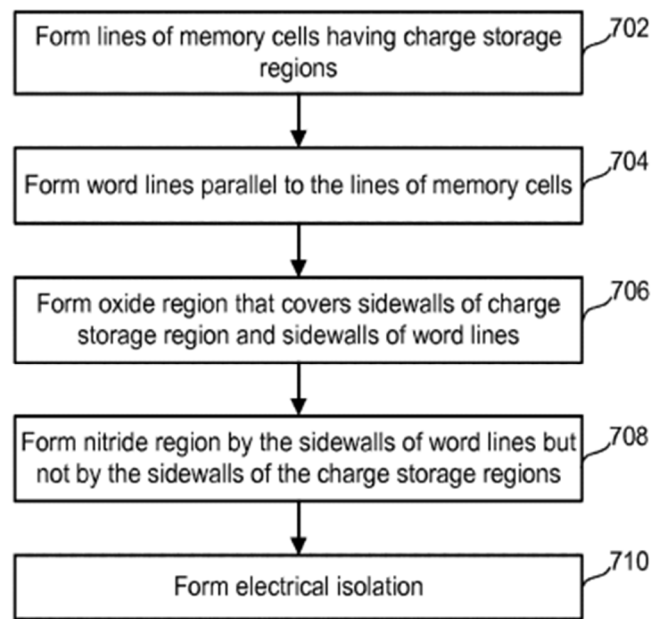


Fig. 7

Id., Fig. 7. For example, Figure 8E (annotated) illustrates lines of memory cell stacks “extend[ing] in the x- or word line-direction,” wherein “[t]he word lines 528 are parallel to the lines of memory cells” and “[e]ach word line 528 [yellow] is coupled to the control gates 526 [blue] of the memory cells.” *Id.*, 9:35-40. “In step 706, oxide is formed that covers the sidewalls 554 [not identified] of the charge storage region and the sidewalls 560 [not identified] of the word lines.” *Id.*, 9:46-48. “Region 532a

of the oxide 532 [green] covers sidewalls of the charge storage region 522 [red], and region 532*b* of oxide 532 covers sidewalls of the word lines 528.” *Id.*, 9:51-56. “The oxide 532 may cover other sidewalls such as sidewalls of the tunnel oxide 520 [not shown], intermediate dielectric 524 and control gate 526.” *Id.*, 9:56-60. And after one embodiment of step 708, “nitride is formed by the sidewalls 566 [not shown] of the word lines 528, but not by the sidewalls 554 [not shown] of the charge storage regions 522.” *Id.*, 10:12-14, 10:4-6. Specifically, “region 532*a* of silicon oxide is not covered by the nitride 534 [purple]. Thus, region 532*a* of silicon oxide is exposed at this point.” *Id.*, 10:16-18.

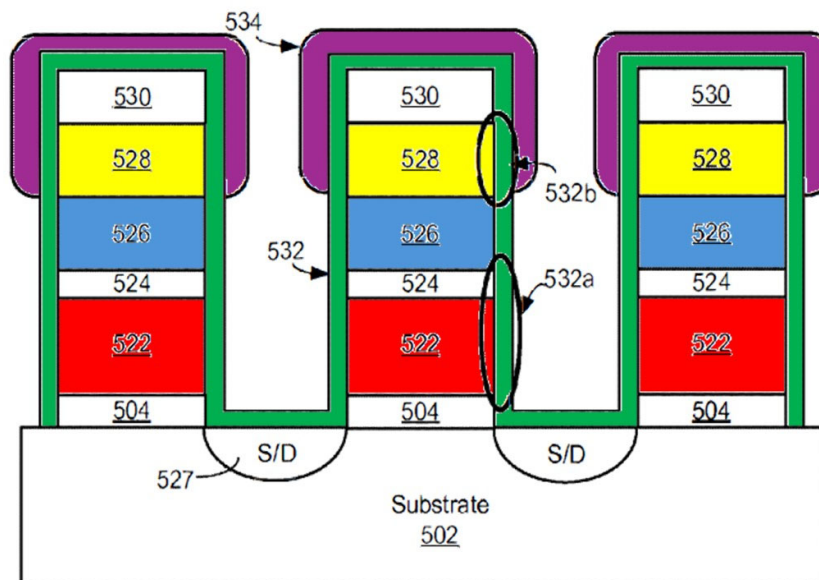


Fig. 8E

Id., Fig. 8E (annotated).

32. Finally, “step 710 forms electrical isolation regions other than silicon nitride adjacent to the oxide regions 532*a* that cover the sidewalls of the charge

storage regions 522. An electrical isolation region may include an air gap and possibly a solid material in contact with the silicon oxide 532.” *Id.*, 10:30-35. And “[s]tep 710 may include forming a capping layer 854 over the word lines 528.” *Id.*, 10:41-42. “Thus, step 710 may include forming air gaps between pairs of neighboring word lines.” *Id.*, 10:36-37. For example, “FIG. 8F [annotated] shows results after one embodiment of step 710, showing air gaps 844 [pink] between pairs of adjacent word lines 528.” *Id.*, 10:39-42.

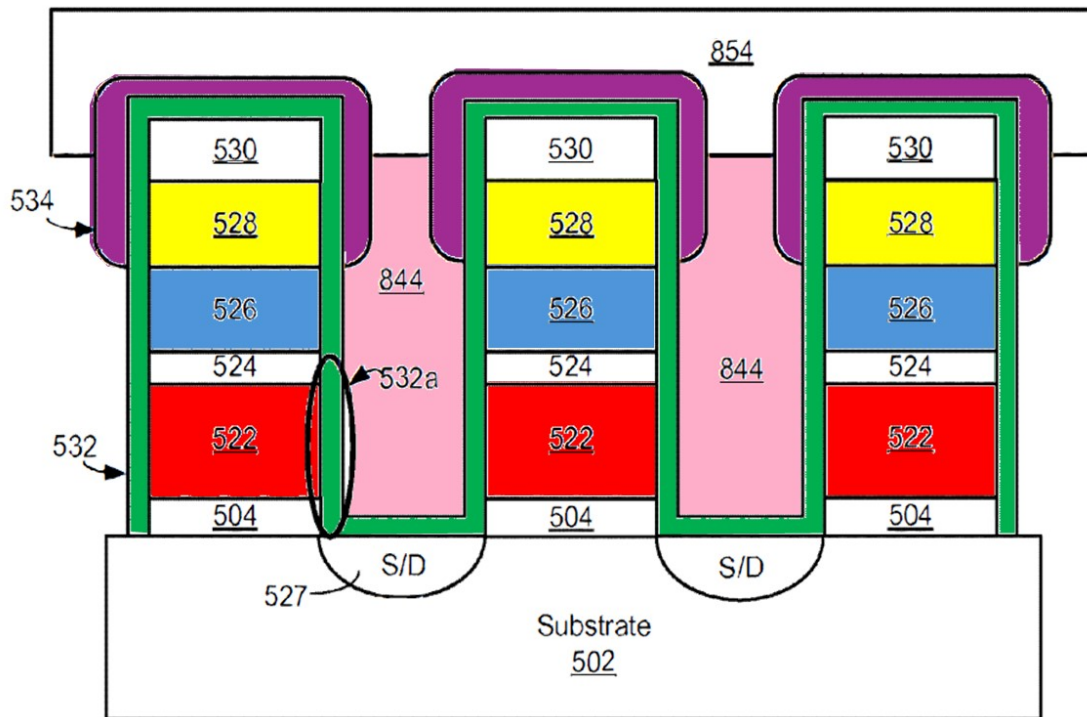


Fig. 8F

Id., Fig. 8F (annotated).

C. Prosecution History of the '314 Patent

33. The '314 file history is submitted as Ex-1004. The Examiner's single Non-Final Office Action presented only a restriction requirement, and the Examiner did not issue any substantive rejections based on prior art. *See* Ex-1004 at 82-87. The Notice of Allowance identifies prior art considered by the Examiner but simply concludes that the prior art did not "teach or suggest an oxide and then a nitride on the sidewalls of the wordlines." *See id.* at 107-13 (citing only U.S. Patent No. 8,492,224 and U.S. Patent Application Pub. Nos. 2015/0318296 and 2015/0340371).

34. None of the four references applied in Petitioner's invalidity grounds were applied to reject a claim during prosecution. *See* Ex-1004. Kang, Kang-1, and Murata were not mentioned during prosecution. *Id.* Although the Examiner cited U.S. Patent No. 8,492,224—which claims priority to one of the same parents as the Purayath reference applied in Petitioner's invalidity grounds (Ex-1007)—in its Notice of Allowance, there is no evidence that the Examiner gave Ex-1007 any consideration and it was not cited during prosecution. Ex-1004 at 110-12, 119.

VII. CLAIM CONSTRUCTION

35. The '314 Patent defines certain terms, including certain terms recited by the claims. For example, the '314 Patent states, "[a]s used herein, the term 'covered' may include direct physical contact, but does not require direct physical contact." Ex-1001, 6:27-29. Similarly, the '314 Patent notes, "[a]s used herein, the

term ‘adjacent’ does not require direct physical contact but could include direct physical contact.” *Id.*, 6:35-37. The ’314 Patent further explains, “[t]he word line and its associated memory cells may be referred to herein as a ‘memory cell stack’ 570.” *Id.*, 6:59-61.

36. However, I do not believe that any term requires explicit construction to resolve the issues presented in the Petition. I ascribe the plain meaning to each claim term, as that plain meaning would have been understood by a POSITA.

37. I reserve the right to offer opinions on any claim constructions proposed in this proceeding or to offer opinions on additional constructions in the district court.

VIII. TECHNOLOGICAL BACKGROUND

38. This section provides technology background to the ’314 Patent.

39. The ’314 Patent and the prior art discussed in the Petition relate generally to NAND flash memory, which represents an example of “non-volatile memory.” Ex-1027, 1:24-26. And “[n]on-volatile memory is memory that can retain its data values for some extended period without the application of power.” *Id.*, 1:26-28.

40. NAND flash has been known and in use for quite some time, having been first developed in 1987. *See* Ex-1028, 22. Like all semiconductor memory, NAND flash includes memory “cells,” with a number of memory cells arranged in

series to form a string. In NAND flash, data is stored in a “cell” formed from a single transistor that is connected with many other memory cell transistors in series. Given that the string of memory cells can only conduct and pass current when each and every memory cell transistor in the string is turned on, this results in the logical equivalent of what a POSITA would have understood to be a “NOT AND” circuit. Ex-1028, 38-39. This is why this type of memory is referred to as “NAND.”

A. It was well known that floating gates and charge-trapping gates were interchangeable

41. A POSITA would have known that floating gates and charge-trapping layers were interchangeable in that they serve the same function of storage of electrons as data state of the memory cell. The storage of charges in the non-volatile memory cell as a MOSFET transistor can be realized in two ways, which has led to the subdivision of nonvolatile semiconductor memory devices into two main classes—floating gate devices and charge-trapping devices. Ex-1024 at 5. Floating gate devices are “based on the storage of charge on a conducting or semiconducting layer that is completely surrounded by a dielectric,...as shown in Fig. 1.5a. Since this layer acts as a completely electrically isolated gate, this type of device is commonly referred to as a floating gate device.” *Id.* at 6. Alternatively, in charge-trapping devices, “the charge is stored in discrete trapping centers of an appropriate dielectric layer.” *Id.*

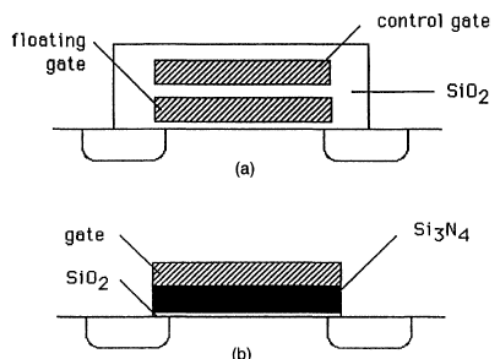


Figure 1.5 Two classes of nonvolatile semiconductor memory devices: (a) floating gate devices; (b) charge-trapping devices (MNOS device).

Id., Fig. 1.5. “Since the early day[s] of nonvolatile memories in the late 1960s, charge trapping transistors using silicon nitride as a charge storage layer have been an alternative to floating gate devices in EPROM, EEPROM, and later Flash memories.” Ex-1026 at 0001.

42. Although a POSITA would have known that the function of the floating gates and charge-trapping layer were interchangeable, there are benefits of each method. For example, “the charge trapping concept has significant advantages when looking into advanced device structure like FinFET or 3D stacked memory cells.” Ex-1026 at 0001. “In floating gate memories,...it becomes more and more difficult to maintain a high gate coupling ratio and keep floating gate interference limited.” *Id.* “Replacing the floating gate cell by a charge trapping cell with Fowler Nordheim programming and erase can help to scale NAND devices further without significant changes in architecture and periphery circuits.” *Id.* at 0002-03 (explaining that charge trapping memory cells can be stacked and share periphery circuits in a NAND architecture); *see also* Ex-1024 at 7 (noting charge trapping devices “in commercial high-density nonvolatile memory circuits”). Ex-1029 (“[C]harge traps consume less

energy during program and erase, so a 3D NAND that is based upon a charge trap is likely to be more energy-efficient than its floating gate counterpart.”).

43. Similarly, “[c]harge traps require a lower programming voltage than do floating gates. This, in turn, reduces the stress on the tunnel oxide.” Ex-1029. Because “stress causes wear in flash memories, the lower programming voltage gives charge trap flash greater endurance than conventional floating gate.” *Id.* “Charge traps are also faster to program than conventional floating gate flash.” *Id.*

44. In addition, in nitride or nanocrystal charge-trapping gate insulators, once the charge is trapped, the charge is far less likely to leak out as compared to a polysilicon layer. *See, e.g.,* Ex-1024 at 7 (“[A]n eventual pinhole in the thin tunneling oxide (I) will not lead to a complete discharge of the cell since the individual traps are isolated from each other by the nitride.”). “3D NAND uses a charge trap because it’s extremely difficult to create features, like a floating gate, sideways—lithography works from the top down.” Ex-1029. “A charge trap, when used to replace a floating gate, doesn’t need to be patterned, since the charge on one bit’s charge trap will not leak through the insulating charge trap layer into an adjacent bit cell.” *Id.* Because “the charge trap is an insulator[,] the charge in the trap can’t flow from one side of the trap to the other, the way it would in a floating gate.” *Id.* “Although stress-induced leakage can drain the charge off a floating gate, the same phenomenon would only drain the charge off of a portion of a charge trap

without disturbing the charge on the remainder of the trap.” *Id.* One potential drawback of the charge-trapping type of memory device is that the charge might be permanently stuck inside the nitride insulator which would lead to failed erase operations.

B. It was well known to form electrical isolation regions between neighboring pairs of word lines

45. A POSITA would have known that forming electrical isolation regions between neighboring word lines introduces parasitic capacitance, causes variation in the threshold voltage, and thereby deteriorates the reliability of memory devices. For example, Kang-1 recognizes a demand for higher density memory devices and “[e]fforts to manufacture devices meeting this demand often involve scaling down the sizes of gate structures and minimizing the space between adjacent gate structures.” Ex-1006 ¶5. “Unfortunately, these efforts often result in increased parasitic capacitance between adjacent structures in the memory cell regions. Such increases in parasitic capacitance reduce the speed of the memory devices.” *Id.*, ¶6. “Also, variation in parasitic capacitance between gate structures causes a variation in the threshold voltage for each gate structure, thereby degrading the reliability of memory devices.” *Id.*

46. Indeed, Kang’s “Equation 2 describes the floating gate voltage (V_{fg}) of one of the memory cells of FIG. 2 as a function of the surrounding voltages and capacitances.” *Id.*, ¶9.

$$V_{fg} = \frac{C_{ono} * V_{cg} + C_{fgx}(V_1 + V_2) + C_{fgy}(V_3 + V_4) + C_{fgcg}(V_5 + V_6)}{C_{ono} + C_{tun} + 2C_{fgx} + 2C_{fgy} + 2C_{fgcg}} \quad (\text{Equation 2})$$

“As shown in Equation 2, decreasing C_{fgy} , results in an increase in V_{fg} . Consequently, the coupling ratio can be increased and the speed performance of the device can be improved.” *Id.* Thus, “one method to improve device performance as device density is increased is to reduce the parasitic capacitance between adjacent floating gates.” *Id.*, ¶10. “Typically, the spaces between adjacent floating gates are filled by an insulating layer whose dielectric constant is a primary factor in determining the capacitance between adjacent floating gates.” *Id.* “An insulating layer formed from a material having a higher dielectric constant will cause increased parasitic capacitance between adjacent gate structures. Consequently, it is desirable to form the dielectric layer from the lowest dielectric constant material possible.” *Id.*; *see id.*, ¶12 (describing additional prior art approaches).

47. Kang-1’s “Table 1 is a list of the approximate dielectric constants of several materials.” *Id.*, ¶11. Although “[t]ypical dielectric layers are formed from silicon oxide or silicon nitride materials,” “these materials have dielectric constants of approximately 3.9 and 7.8, respectively.” *Id.* “Air, on the other hand, has an approximate dielectric constant of 1.005. Consequently, a substantial reduction in the parasitic capacitance between adjacent gate structures can be achieved by

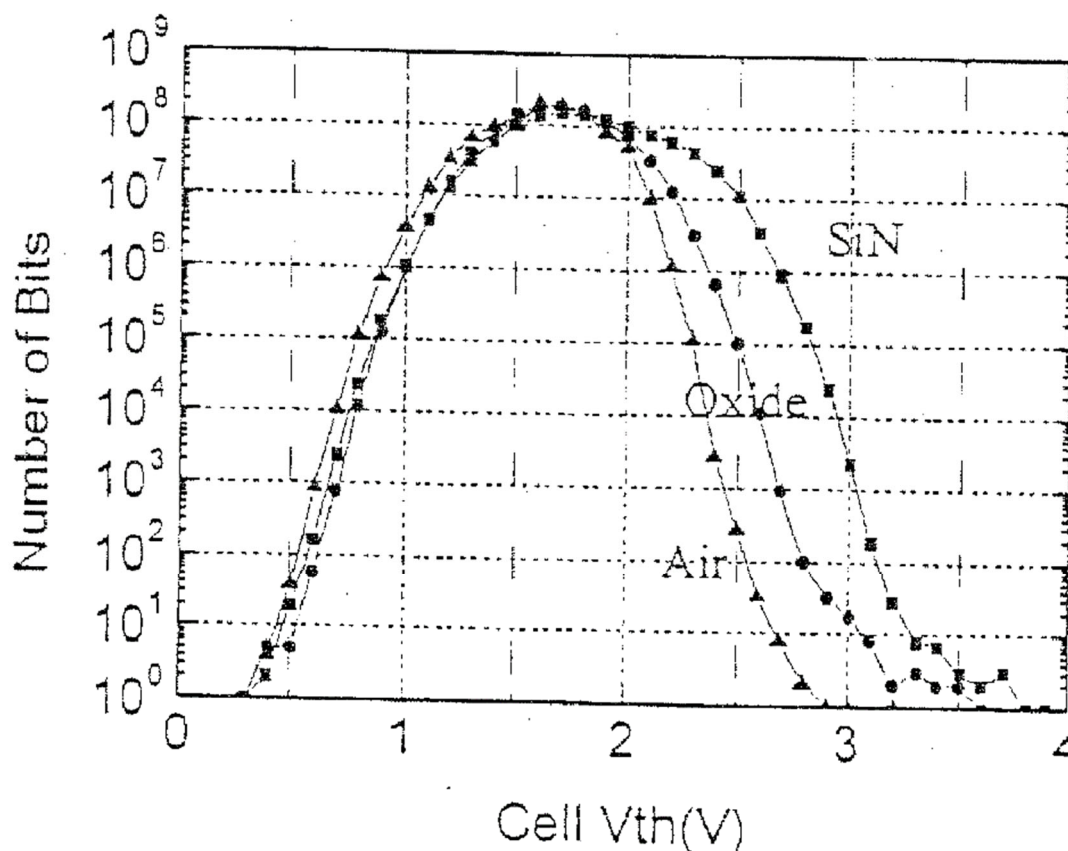
replacing the silicon oxide or nitride dielectric material commonly used in semiconductor, e.g., memory structures with air.” *Id.*

TABLE 1

Material	Dielectric Constant
Vacuum	1 (By definition)
Air	1.005
Polyethylene	2.25
Paper	3
Silicon oxide	3.9
Silicon nitride	7.8
Rubber	7
Silicon	11.68
Methyl alcohol	30
Water	80
Barium Titanate	1200

Id., ¶11, Table 1.

48. For example, Kang-1’s “FIG. 13 is a plot of experimental results showing the threshold voltage distribution in a 1 Gbit NAND flash memory for various dielectric materials.” *Id.*, ¶71. “The plot shows that the V_{th} [cell threshold voltage] distribution is dramatically improved with the cells formed according to some embodiments of [Kang-1’s] invention as opposed to the cells formed using prior art methods having oxide or silicon nitride (SiN) filled between gate structures without air gaps.” *Id.*, ¶72. Indeed, “[t]his improvement in V_{th} distribution is believed to be due to the improved floating gate voltage shift with the air gap.” *Id.*



Id., Fig. 13.

49. Thus, a POSITA would have known that using electrical isolation regions—especially those made of air or another material with a low dielectric constant—would reduce parasitic capacitance between adjacent word lines and gate structures, and thereby improve the reliability of higher density memory devices.

C. It was well known to form word lines from tungsten

50. A POSITA would have known that word lines are connected to the control gate of each memory cell and that the word lines are commonly formed from tungsten or tungsten silicide. Ex-1028, 38-39. For example, Kang teaches, “[t]o enhance an operating speed of a semiconductor device, control gates are made of

metallic substance, e.g., tungsten silicide.” Ex-1005, 1:23-25. “However, with the continuous trend toward higher integration and higher densities of semiconductor devices, line-widths are tending below a nanometer in width. Thus, electrical sheet resistances of the conventional silicon silicide are increasing, causing increases in RC signal delays relative to distance and deterioration of cell threshold voltage distribution.” *Id.*, 1:25-31. “Different approaches for overcoming the foregoing problems have been proposed. One of the approaches proposed forming a control gate from a metal having a low sheet resistance, for example, tungsten.” *Id.*, 1:32-35. And tungsten “may help enhance a speed of a memory device.” *Id.*, 6:14-15. Thus, it was well known to form word lines from either tungsten or tungsten silicide.

D. It was well known to electrically couple word lines to peripheral circuitry

51. In NAND flash memory, the peripheral circuitry refers to the Complementary Metal Oxide Semiconductor (CMOS) components, including mainly low-voltage transistors and high-voltage transistors, that are not part of the cell array itself but form an essential part of the memory device. The peripheral circuitry manages data access and handles various operations like reading, writing, and erasing the memory cells. A POSITA would have understood that a peripheral circuit would include row control circuitry, such as row decoders and word line drivers, connected to the word lines to select one of the word lines, to apply read voltages, to apply program voltages combined with the bit line potential levels

controlled by column control circuit, and to apply an erase voltage, enabling memory access. Thus, a POSITA would have understood that peripheral circuitry is electrically coupled to the word lines of the memory device. Ex-1030, 6:32-36.

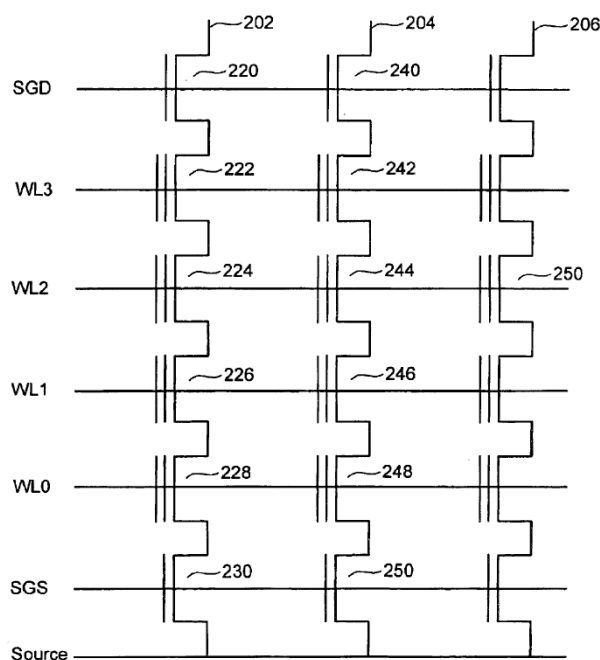
E. It was well known to arrange memory cells as NAND strings perpendicular to word lines

52. In NAND flash memory, memory cells are organized into NAND strings, which are essentially series of connected memory cells. These NAND strings are typically arranged perpendicular to the word lines, which run along the bit lines of the memory array. This arrangement allows for efficient storage and retrieval of data with the bit lines providing a common connection for multiple NAND strings.

See Ex-1030, 2:19-47, Fig. 4.

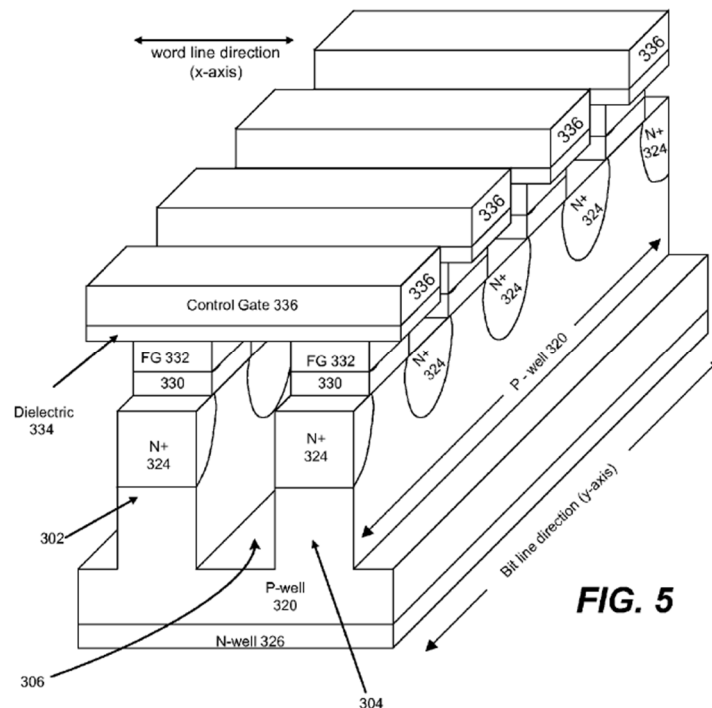
Fig. 4

Prior Art



Id., Fig. 4.

53. For example, Purayath discloses that “FIG. 5 is a three-dimensional block diagram of two exemplary NAND strings 302 and 304 that may be fabricated as part of a larger flash memory array.” Ex-1007 ¶38. “The bit line or y-direction runs along the NAND strings, and the word line or x-direction runs perpendicular to the NAND string or the bit line direction.” *Id.* Thus, a POSITA would have known that it was common to form a plurality of memory cells arranged as NAND strings that are perpendicular to the word lines. *See* Ex-1007 ¶¶8-9, 38-39, 148, Figs. 1-2, 5, 16.



Id., Fig. 5.

IX. BRIEF DESCRIPTION OF THE APPLIED PRIOR ART REFERENCES

54. This petition presents four references, none of which were of record during prosecution. *See* Ex-1004.

A. Kang (Ex-1005)

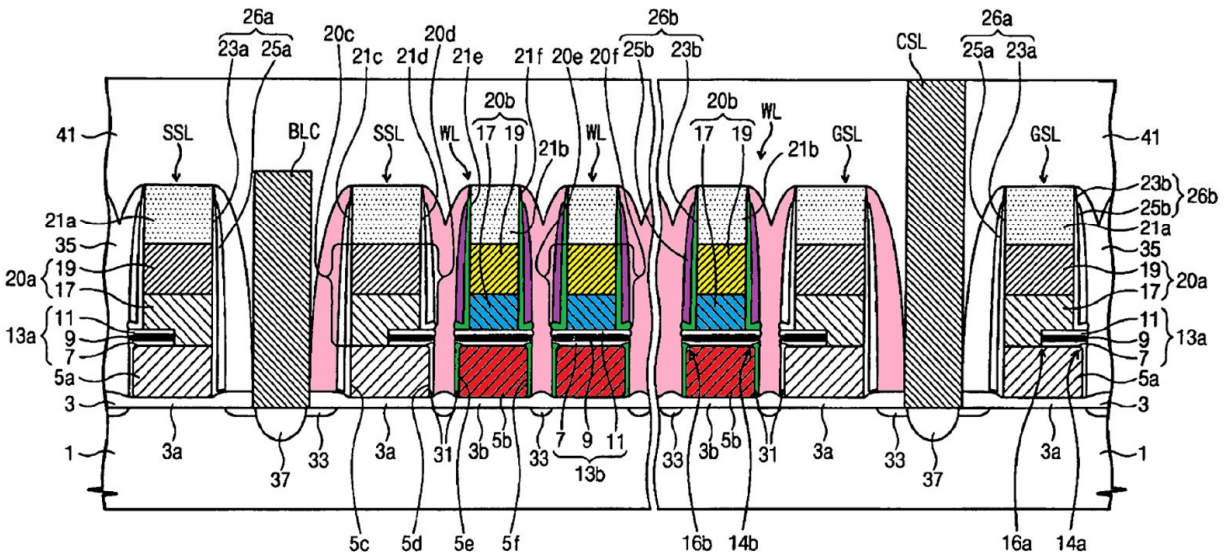
55. Kang was filed May 31, 2006, and issued October 6, 2009. Ex-1005.

56. Kang discloses that “a feature of [the] embodiments of the invention [is] to provide non-volatile memory devices including a barrier spacer that serves to protect a control gate, including a metal layer, from damage that may result from exposure to a cleaning solution and/or oxygen.” Ex-1005, 1:65-2:5. “During formation of the non-volatile memory device, an oxidation process may be formed to cure etch damage of, e.g., an intergate dielectric pattern, a floating gate and a gate insulator. The barrier spacer and/or the oxidation process enable non-volatile memory devices having enhanced speed and reliability to be formed.” *Id.*, 2:5-10. Kang discloses “[a] plurality of wordlines WL may be interposed between respective ones of the string selection lines SSL and the ground selection lines GSL.” *Id.*, 5:13-15. “A string selection line SSL, a ground selection line GSL, and a plurality of wordlines WL interposed therebetween may cross over the active region AR, thereby constituting a cell string.” *Id.*, 5:18-21, Fig. 1.

57. As shown in Figure 2, Kang discloses wordlines WL comprising charge storage regions 5b (red) and control gates 20b with polysilicon layer 17 (blue) and

tungsten layer 19 (yellow). *Id.*, 5:53-57, 6:10-13. “Upper portions of first and second sidewalls of the wordlines WL may be covered with the second barrier spacers 26b and lower portions of the...first and second sidewalls of the word lines WL may be covered with the thermal oxide layer 31 [green]. The second barrier spacers 26b may include a medium-temperature oxide (MTO) layer 23b [green] and a second silicon nitride layer 25b [purple].” *Id.*, 7:47-55. “The second barrier spacers 26b may extend along an entire or substantially entire length of...the upper portions of the first and second sidewalls of the wordlines WL. The second silicon nitride layer 25b...may not extend completely along the length of the upper portions of the second sidewalls of...the first and second sidewalls of the wordlines WL.” *Id.*, 7:56-63.

Fig. 2



Id., Fig. 2 (annotated). Kang further discloses that “[s]pacers 35 [pink] may be formed between adjacent ones of the wordlines WL, the string selection lines SSL,

the ground selection lines GSL and/or the common source lines CSL.” *Id.*, 8:62-65.

“The spacers 35 may cover...the second barrier spacers 26b...and/or the thermal oxide layers 31 covering the sidewalls of the string selection lines SSL, the ground selection lines GSL and the wordlines WL.” *Id.*, 9:1-6.

B. Kang-1 (Ex-1006)

58. Kang-1 was filed October 20, 2006, and published May 3, 2007. Ex-1006.

59. Kang-1 discloses “semiconductor devices such as memory devices having an air gap defined between adjacent gate structures and methods of fabricating the same.” Ex-1006 ¶3. Kang-1 explicitly notes that “[e]fforts to manufacture devices meeting [a demand for ever higher density memory devices] often involve scaling down the sizes of gate structures and minimizing the space between adjacent gate structures.” *Id.*, ¶5. “Unfortunately, these efforts often result in increased parasitic capacitance between adjacent structures in the memory cell regions.” *Id.*, ¶6. “Such increases in parasitic capacitance reduce the speed of the memory devices” and “variation in parasitic capacitance between gate structures causes a variation in the threshold voltage for each gate structure, thereby degrading the reliability of memory devices.” *Id.*

60. Kang-1 discloses that “the spaces between adjacent floating gates are filled by an insulating layer whose dielectric constant is a primary factor in

determining the capacitance between the adjacent floating gates.” *Id.*, ¶10.
“Consequently, it is desirable to form the dielectric layer from the lowest dielectric constant material possible.” *Id.* “Table 1 is a list of the approximate dielectric constants of several materials.” *Id.*, ¶11.

TABLE 1

Material	Dielectric Constant
Vacuum	1 (By definition)
Air	1.005
Polyethylene	2.25
Paper	3
Silicon oxide	3.9
Silicon nitride	7.8
Rubber	7
Silicon	11.68
Methyl alcohol	30
Water	80
Barium Titanate	1200

Id. at 2. Table 1 shows that air “has an approximate dielectric constant of 1.005.” *Id.*, ¶11. “Consequently, a substantial reduction in the parasitic capacitance between adjacent gate structures can be achieved by replacing the silicon oxide or nitride dielectric material commonly used in semiconductor, e.g., memory structures with air.” *Id.*

61. Figures 4-10 illustrate “a method of manufacturing a semiconductor device, e.g., a flash memory structure,” including “a plurality of cell gate structures 126, between the ground select gate structure 127 and the string select gate structure 128.” *Id.*, ¶¶51-52. The gate structures each may include a charge-storage layer 122

(red), control gate 124 (blue), and hard mask 125 (yellow). *Id.* “[A] protection layer 130 [green] may be...formed over the gate structures and the substrate 100, thereby covering the...sidewalls of the gate structures” and “a first insulation layer 132 may be formed over the protection layer 130.” *Id.*, ¶53, Fig. 5. “[A] portion of the first insulation layer 132 is then removed, e.g., etched to form a first insulation layer pattern 133,” which “is thus formed on the sidewalls of the gate structures.” *Id.*, ¶55, Figs. 5-6. “Then, a second insulation layer 136 [purple] is formed over the protection layer 130” and “partially etched or etched back to form the second insulation layer pattern 137,” which “has an opening 131 to expose an upper surface of the first insulation layer pattern 133.” *Id.*, ¶57, Figs. 8-9. “[T]he first insulation layer pattern 133 is then selectively removed by, for example, etching through the opening 131 defined by the second insulation layer pattern 137, to form the air gaps 134 [pink].” *Id.*, ¶58, Fig. 10. Thus, “the protection layer 130 may define the sidewalls and bottoms of the air gaps 134” and “the air gaps 134 may be substantially surrounded by the protection layer 130 and the second insulation layer pattern 137.” *Id.*, ¶59.

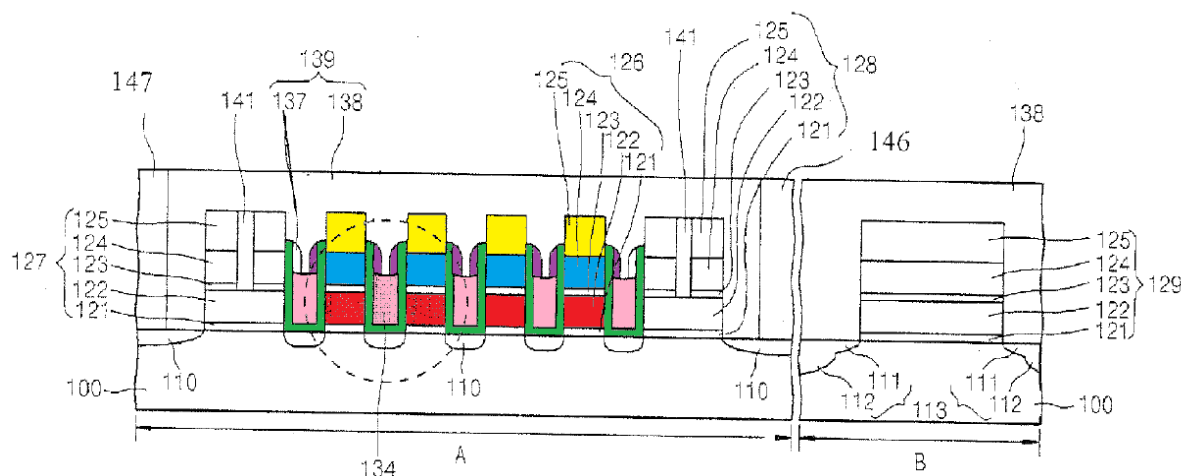


FIG. 3

Id., Fig. 3 (annotated).

C. Purayath (Ex-1007)

62. Purayath was filed June 16, 2011, and published December 22, 2011.

Ex-1007.

63. Purayath relates to “high-density semiconductor memory, and more particularly to electrical isolation between discrete devices in non-volatile memory.”

Ex-1007 ¶31. “Electrical isolation is provided, at least in part, by air gaps that are formed in the column (bit line) direction and/or air gaps that are formed in the row (word line) direction.” *Id.* As shown in Figure 7S, “word line air gap caps are formed to define word line air gaps between the layer stack rows,” wherein each layer stack row includes a charge storage region 466 (red) and a control gate 452 (blue), where “[c]ontrol gates 452 have been silicided to create a metal silicide end portion 453 [yellow cross-hatched region] for each control gate.” *Id.*, ¶¶82, 100, 103-04. Further,

a dielectric “[l]iner [486] (e.g., oxide) [green] is formed along the sidewalls 413 of the layer stack rows, over the upper surface of the control gates 452....” *Id.*, ¶81, Fig. 7S. Then, as shown in Figure 7T, “a capping layer 488 [purple] is formed over the layer stack rows using a non-conformal deposition process,” through which “material 488 will be deposited unequally at the upper portion of the layer stack rows.” *Id.*, ¶83. “Material 488,” which may be a nitride, “quickly accumulates, meeting at a location over the spaces between rows to form air gaps 487 [pink] that are elongated in the x-direction.” *Id.* “Material 488 extends vertically toward the substrate surface along the liner 486 on a portion of vertical sidewalls 413 of the layer stack rows. The amount of this vertical dimension will define an upper endpoint of the air gaps at a lower surface of material 486.” *Id.* In Figure 7T, “it is seen that the air gap extends vertically beyond the level of the upper surface of the control gates.” *Id.*

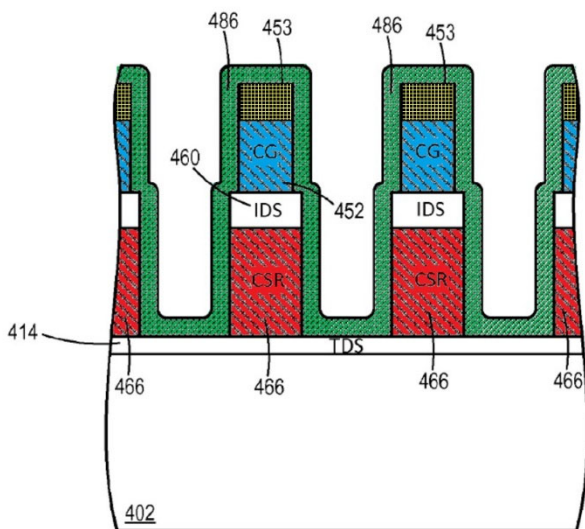


FIG. 7S

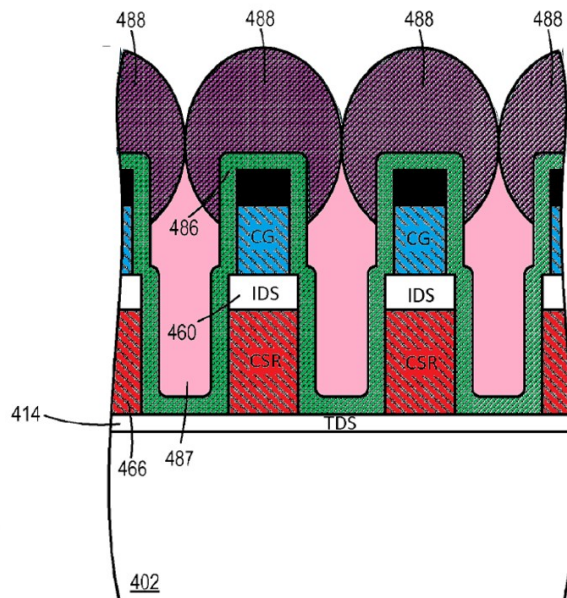


FIG. 7T

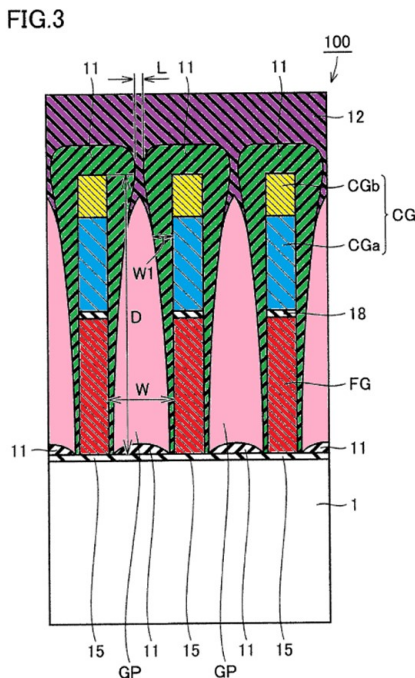
Id., Figs. 7S-7T (annotated).

D. Murata (Ex-1008)

64. Murata was filed June 20, 2007, and issued July 20, 2010. Ex-1008.

65. Murata discloses “[a] semiconductor device...compris[ing]...a plurality of convex patterns formed over a main front surface of the semiconductor substrate so that each might have a floating gate [red] and a control gate [blue], a first insulating film [green] formed so that an upper surface and a side surface of each of the convex patterns might be covered,...and a second insulating film [purple] that covers an upper surface and a side surface of the first insulating film so that a cavity [pink] between the adjacent convex patterns may be occluded.” Ex-1008, 2:29-41, Fig. 3. “Control gate CG is formed, for example of the laminated film of

conductive layer CGa [blue] which consists of polycrystalline silicon of low resistance, and conductive layer CGb [yellow] which consists of high melting point metal silicide films, such as tungsten silicide (WSix), etc. formed in the upper surface.” *Id.*, 6:4-8. A silicon oxide or silicon nitride film may be used for each of the material of first insulating film 11 and second insulating film 12. *See id.*, 6:58-59, 7:7-8, 7:11-12. As shown in Figure 3, “[a] position occluded by the second insulation film of the cavity is a position higher than an upper surface of the floating gate, and a position lower than an upper surface of the control gate.” *Id.*, 2:41-44.



Id., Fig. 3.

X. DETAILED EXPLANATION OF THE UNPATENTABILITY GROUNDS

66. The '314 Patent contains 19 claims. This Petition challenges

independent Claims 1 and 13 and Claims 2-7, 14, and 17-19 that depend either directly or indirectly from Claims 1 and 13. Independent Claim 1 is a “system” claim and Claim 13 is a “method” claim that adapts recitations from system Claim 1. The subject matter of the challenged claims is disclosed by the prior art as shown below.

A. Ground 1: Claims 1, 3-4, 6-7, 13, 17, and 19 are obvious over Kang

67. As shown below, the subject matter of independent Claims 1 and 13 and dependent Claims 3-4, 6-7, 17, and 19 are disclosed by Kang.

1. Claim 1

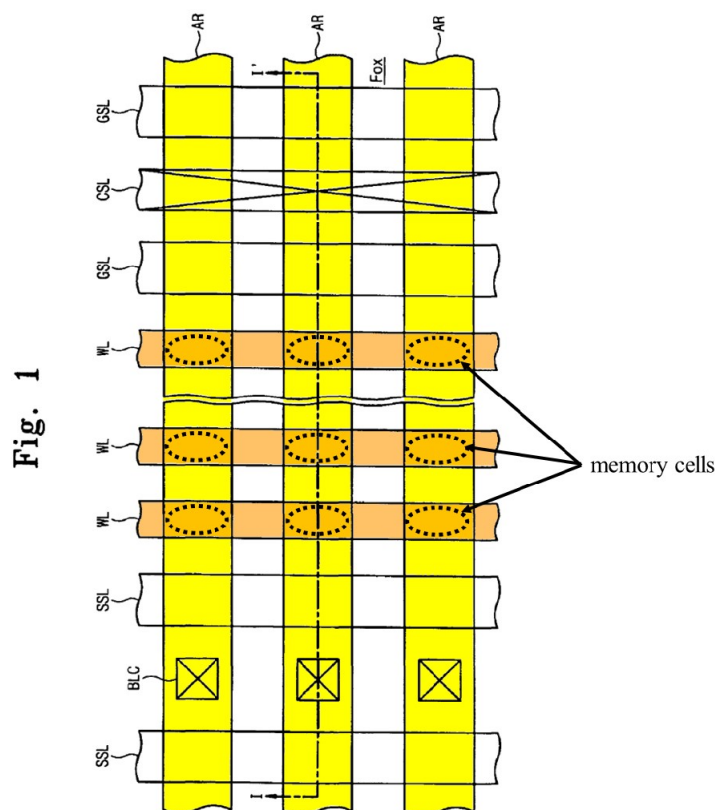
a. Element 1[preamble]: A memory device comprising:

68. If Claim 1’s preamble is limiting, Kang disclose the preamble. Kang states, “the present invention relates to non-volatile memory devices and methods of forming the non-volatile memory devices.” Ex-1005, 1:9-12.

b. Element 1[a]: a plurality of lines of memory cells, the memory cells comprising:

69. Kang states, “[n]on-volatile memory devices, such as flash memory devices, generally include a cell array region and a peripheral circuit region for driving the cell array region.” Ex-1005, 1:14-16. As shown in Figure 1, “[a] plurality of wordlines WL may be interposed between respective ones of the string selection lines SSL and the ground selection lines GSL.” *Id.*, 5:13-15. “A string selection line SSL, a ground selection line GSL, and a plurality of wordlines WL interposed

therebetween may cross over the active region AR, thereby constituting a cell string.” *Id.*, 5:18-21.



Id., Fig. 1 (annotated). A memory cell is formed at each intersection of the wordlines (shown in orange) crossing over the active region AR of the substrate (shown in yellow), forming an array of memory cells that are demarcated as strings extending along the AR direction, with a string selection line and a ground selection line sandwiching each string. *See supra* §VIII.E.

70. This is comparable to the memory cells in the '314 Patent. For example, “FIG. 2A shows three NAND strings 202, 204 and 206 of a memory array having

many more NAND strings.” Ex-1001, 3:1-4. “As can be seen, each bit line and the respective NAND string comprise the columns of the array of memory cells. The word lines (WL3, WL2, WL1 and WL0) comprise the rows of the array.” *Id.*, 3:21-24. And “[t]he lines of memory cell stacks are formed,” wherein “[e]ach stack has a word line and associated memory cells,” so that “[a] line of memory cell stacks 570 extends in the x- or word line-direction.” *Id.*, 2:9-11, 9:35-45, Figs. 5B, 8C; *see id.*, 3:25-26, 3:30-31. “FIG. 2B is a top view of a portion of an array of NAND flash memory cells,” wherein “[t]he array includes NAND strings 300 [shown in yellow] and word lines 528 [shown in orange].” *Id.*, 3:35-37, Fig. 2B.

Fig. 2A

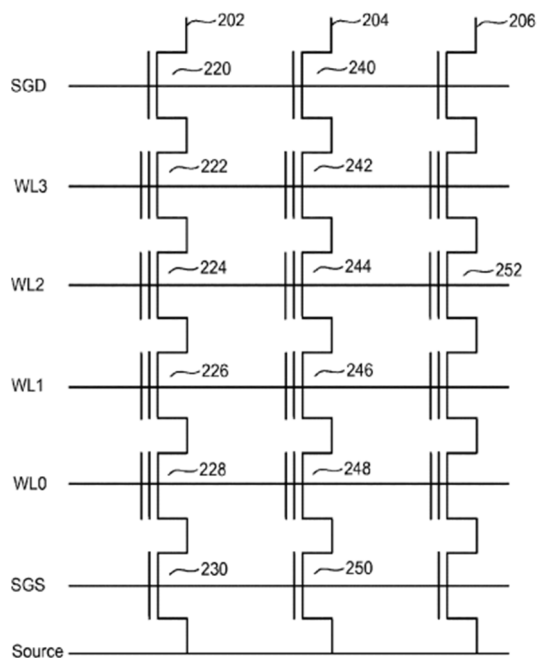
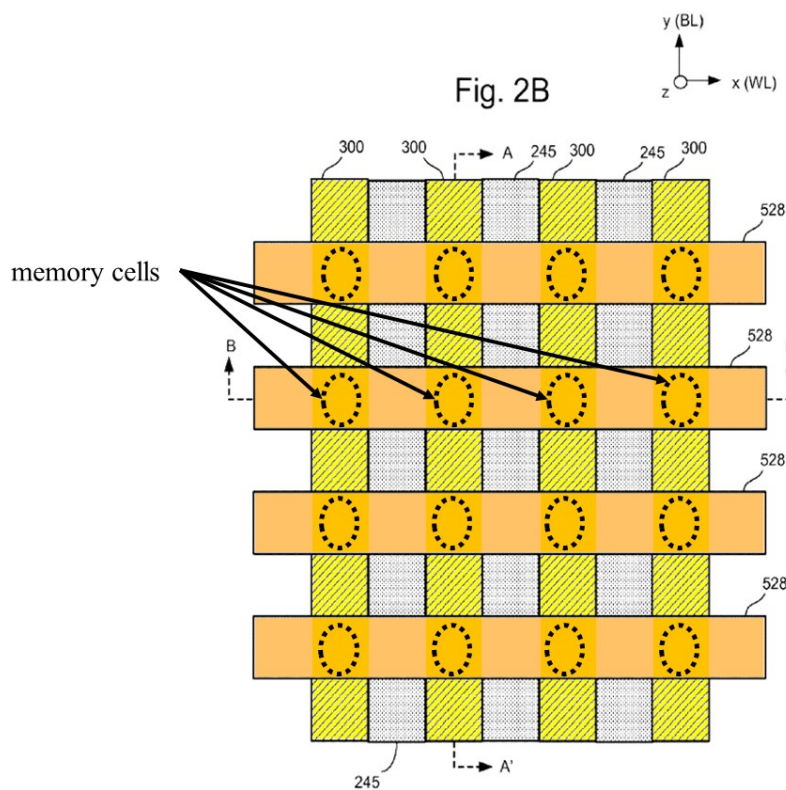


Fig. 2B



Id., Figs. 2A, 2B (annotated).

c. Element 1[a1]: a charge storage region having sidewalls; and

71. Kang discloses a charge storage region. Kang discloses that “[a] cell transistor in the cell array region includes a gate insulator, a floating gate, an intergate dielectric and a control gate sequentially stacked in the order named.” Ex-1005, 1:20-23. A POSITA would have understood that “[t]he storage of charges in...a MOSFET can be realized in two ways, which has led to the subdivision of nonvolatile semiconductor memory devices into two main classes,” i.e., floating gate devices and charge-trapping devices. Ex-1024 at 5-6; *see supra* §VIII.A.

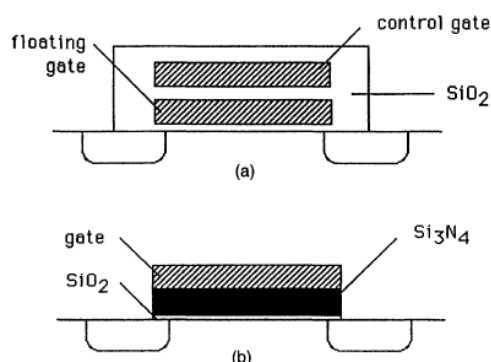


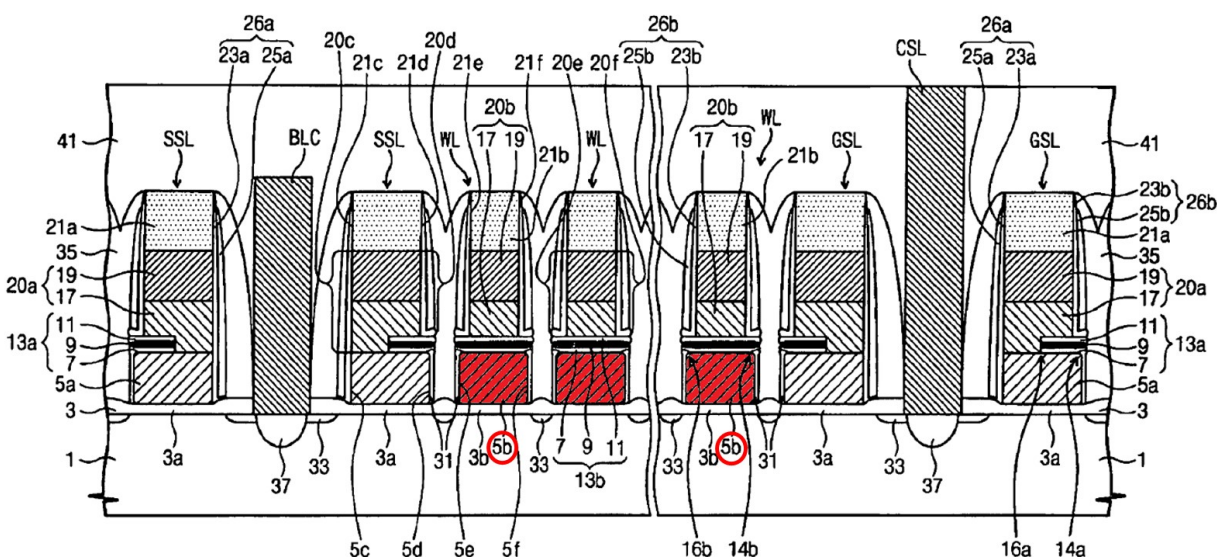
Figure 1.5 Two classes of nonvolatile semiconductor memory devices: (a) floating gate devices; (b) charge-trapping devices (MNOS device).

Ex-1024, Fig. 1.5. Because Kang discloses that “[a] cell transistor in the cell array region includes...a floating gate,” Kang discloses memory cells having a charge storage region. *See supra* §VIII.A.

72. For example, Kang’s Figure 2, which “illustrates a cross-sectional view along the I-I’ of FIG. 1,” shows that “the wordlines WL may each include a second gate insulator 3b, a second floating gate 5b [i.e., a charge storage region shown in red], a second intergate dielectric pattern 13b, a second control gate 20b and a second

mask pattern 21b, which may be stacked on the semiconductor substrate 1 in the order named.” Ex-1005, 5:26-27, 5:53-57, Fig. 2 (emphasis added); *see id.*, 9:43-48, 10:7-33, 11:41-64, Figs. 3-6, 10-12.

Fig. 2



Id., Fig. 2 (annotated). Because each wordline WL includes a floating gate 5b, Kang discloses memory cells having a charge storage region. *See supra* §VIII.A.

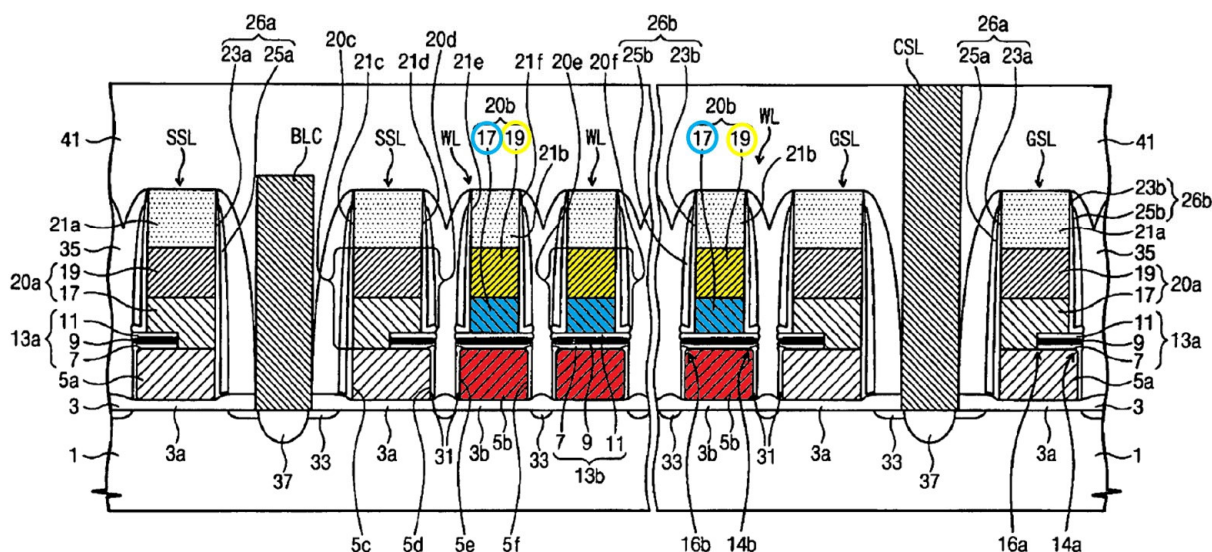
73. And, as shown, “[s]idewalls of the wordlines WL may include upper and lower portions with the first and second sides 14b, 16b....” Ex-1005, 7:31-34. “The lower portion of each of the first sidewalls of the wordlines WL may be defined by a sidewall 5e of the second floating gate 5b and the lower portion of each of the second sidewalls of the wordlines WL may be defined by a sidewall 5f of the second floating gate 5b,” such that “[t]he first sidewalls of the wordlines WL may be opposite to the second sidewalls of the wordlines WL.” *Id.*, 7:41-47. Thus, Kang

discloses that each wordline WL includes a charge storage region (i.e., floating gate 5b) having sidewalls 5e and 5f.

d. Element 1[a2]: a control gate;

74. Kang discloses that “[a] cell transistor in the cell array region includes a gate insulator, a floating gate, an intergate dielectric and *a control gate* sequentially stacked in the order named.” Ex-1005, 1:20-23 (emphasis added). For example, Kang’s Figure 2, which “illustrates a cross-sectional view along the I-I’ of FIG. 1,” shows that “the wordlines WL may each include a second gate insulator 3b, a second floating gate 5b, a second intergate dielectric pattern 13b, *a second control gate 20b* and a second mask pattern 21b, which may be stacked on the semiconductor substrate 1 in the order named.” *Id.*, 5:26-27, 5:53-57, Fig. 2 (emphasis added). The second control gate “20b may include a polysilicon layer 17 [shown in blue], which may be doped with, e.g., N-type-impurities, and a tungsten layer 19 [shown in yellow] having a low electrical resistance.” *Id.*, 6:10-13; *see id.*, 9:66-10:6, 10:7-33, Figs. 5-6.

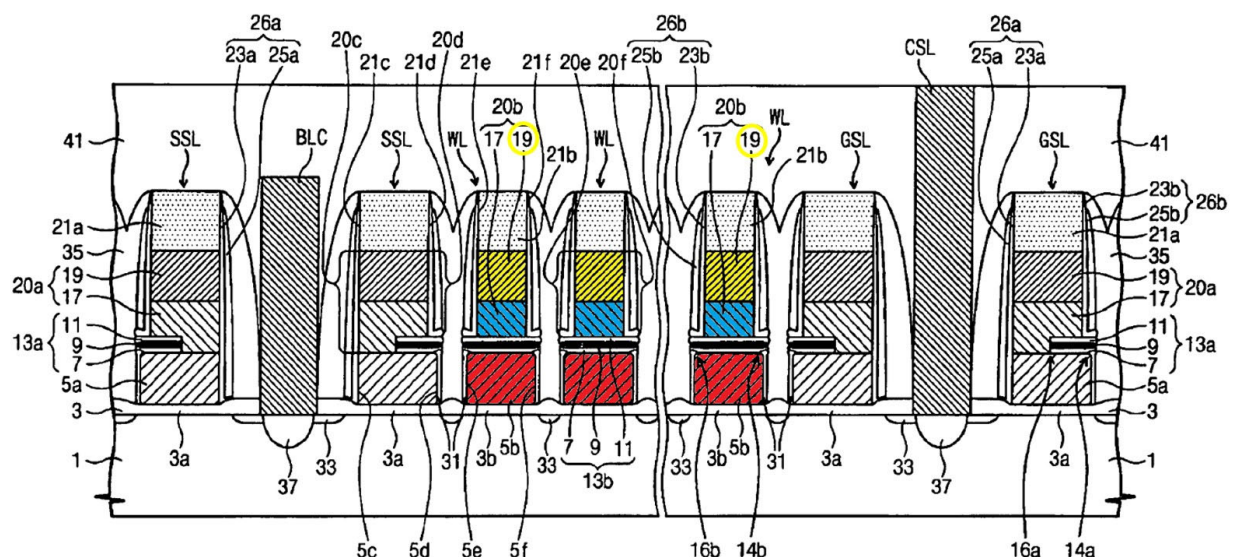
Fig. 2



the control gate of a storage element may be provided as a portion of the word line. *Id.*, 5:9-10. Kang refers to similar structures as “wordlines WL.” For example, “[a]s shown in FIG. 2, the wordlines WL may each include a second gate insulator 3b, a second floating gate 5b, a second intergate dielectric pattern 13b, a second control gate 20b and a second mask pattern 21b, which may be stacked on the semiconductor substrate 1 in the order named.” Ex-1005, 5:53-57, Fig. 2; *see id.*, 1:65-2:2, 2:57-58; *see also id.*, 9:66-10:6, 10:7-33, Figs. 5-6. Kang also discloses word lines in the context of Figure 5A of the ’314 Patent. Kang discloses that control gate may “include a polysilicon layer 17 [shown in blue], which may be doped with, e.g., N-type-impurities, and a tungsten layer 19 [shown in yellow] having a low electrical resistance. *Id.*, 6:11-14, Fig. 2. A POSITA would have known that Kang’s composite control gate of polysilicon and tungsten is the control gate (526) and tungsten word line (528), respectively, of the ’314 Patent.

76. Particularly, a POSITA would have understood that tungsten layer 19 acts as a word line that makes up part of second control gate 20b because tungsten layer 19 forms a conductive path that connects the control gates (i.e., polysilicon layer 17) of memory cells within a string, enabling the selection and control of data access for a specific row of cells, or page, within the NAND flash memory array. *See supra* §VIII.B.

Fig. 2



Ex-1005, Fig. 2 (annotated).

77. Kang further discloses, “[s]idewalls of the wordlines WL may include upper and lower portions with the first and second sides 14b, 16b....” *Id.*, 7:31-34. Specifically, “[t]he upper portion of each of the first sidewalls of the wordlines WL may be defined by a combination of corresponding respective sidewalls 21e and 20e of the second mask pattern 21b and a second control gate 20b” and “[t]he upper portion of each of the second sidewalls of the wordlines WL may be defined by a combination of corresponding respective sidewalls 21f and 20f of the second mask pattern 21b and the second control gate 20b.” *Id.*, 7:34-41. Thus, Kang discloses a plurality of word lines (i.e., tungsten layer 19) each having sidewalls (i.e., 21e, 20e, 21f, and 20f).

78. Further, each of Kang’s word lines is associated with a line of the

memory cells. As discussed above, the '314 Patent describes forming “lines of memory cell stacks,” wherein “[e]ach stack has a word line and associated memory cells,” so that “[a] line of memory cell stacks 570 extends in the x- or word line-direction.” Ex-1001, 2:9-11, 9:35-45, Figs. 5B, 8C; *see id.*, 3:25-26, 3:30-31. Kang similarly discloses that “[a] string selection line SSL, a ground selection line GSL, and a plurality of wordlines WL interposed therebetween may cross over the active region AR, thereby constituting a cell string.” Ex-1005, 5:18-21, Fig. 1. A memory cell is formed at each intersection of the wordlines WL (shown in orange) crossing over the active region AR of the substrate (shown in yellow), and multiple lines of memory cells are formed extending in the word line-direction. Thus, the tungsten layer 19 forms a conductive path that connects the control gates (i.e., polysilicon layer 17) of memory cells within a string in the word line-direction, as shown in Figure 1.



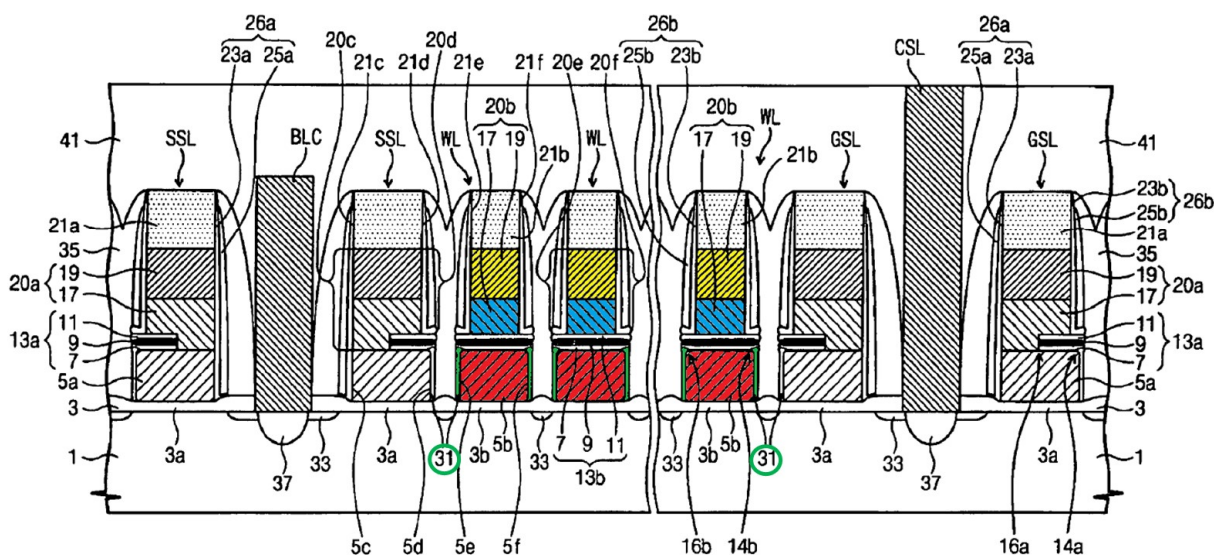
Id., Fig. 1 (annotated).

79. Finally, each of Kang's word lines are coupled to the control gates of the memory cells with which it is associated. *See supra* §VIII.C. As discussed above, Kang's second control gate "20b may include a polysilicon layer 17...and a tungsten layer 19." *Id.*, 6:10-13, Fig. 2. Tungsten layer 19 acts as the word line and polysilicon layer 17 acts as the control gate. These two layers, together, make up Kang's control gate 20b, so a POSITA would have understood that Kang's tungsten layers 19 are coupled to the control gates 20b of the memory cells with which they are associated. *See supra* §VIII.C.

f. Element 1[c]: first oxide regions that cover the charge storage regions;

80. Kang discloses first oxide regions that cover the charge storage regions. Kang describes that “lower portions of the...first and second sidewalls of the word lines WL may be covered with the *thermal oxide layer 31*.” Ex-1005, 7:50-52 (emphasis added); *see also id.*, 9:1-6, 9:33-35, 2:32-34; 10:43-50, 11:65-12:20, Figs. 7-12. Specifically, “[b]y means of the second oxidation process, a thermal oxide layer 31 may be formed on...opposite sidewalls of the second floating gate 5b....” *Id.*, 12:2-7. For example, thermal oxide layer 31 is shown below in Figure 2 in green and covers the sidewalls of each floating gate 5b—i.e., charge storage region—shown in red. *See supra* §VIII.A.

Fig. 2



Ex-1005, Fig. 2 (annotated). A POSITA would have known that an oxide region would cover the charge storage region (floating gate 5b) under the second oxidation process disclosed by Kang. Although Kang discloses that the second oxidation process may be a thermal oxidation process or an In-Situ Stream Generation (ISSG) oxide formation process, under both process options, an oxide layer will be formed on the sidewalls of the floating gate 5b. *See id.*, 11:65-12:20. And a thermal oxide (e.g., SiO₂) refers to a layer of oxide grown on the exposed surface of a silicon wafer, or polysilicon surface, by exposing it to heat and an oxidizing agent (e.g., oxygen or steam). Thus, Kang's thermal oxide layer 31 constitutes an oxide region as required by the claim.

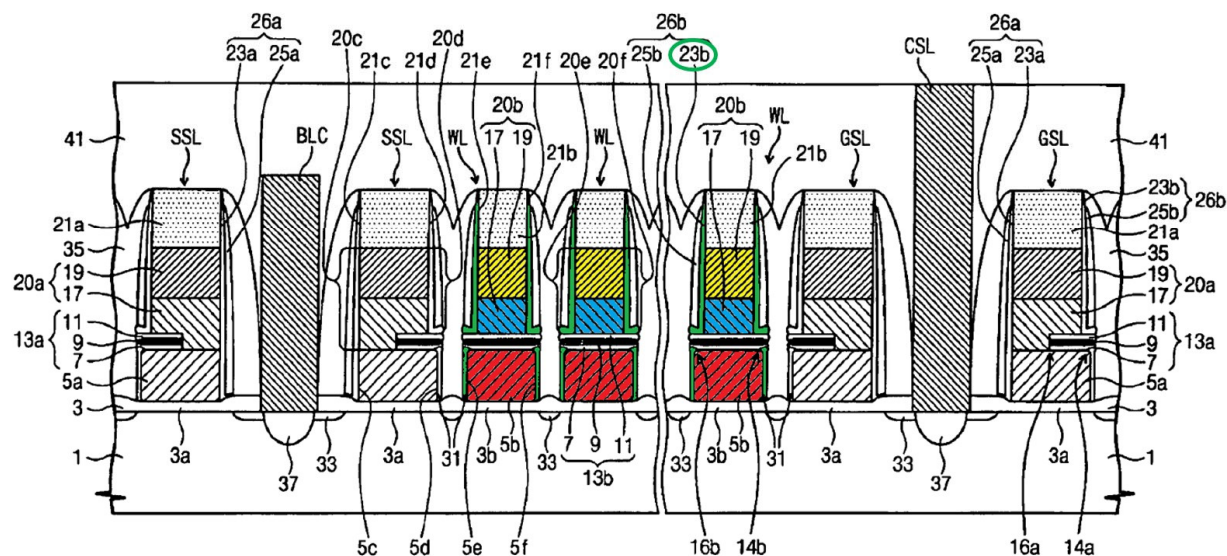
81. Further, Kang's thermal oxide layer 31 "covers" the floating gate 5b—i.e., charge storage region—in accordance with the '314 Specification. The '314 Patent states, "[a]s used herein, the term 'covered' may include direct physical contact, but does not require direct physical contact." Ex-1001, 6:27-29. And Kang's thermal oxide layer 31 directly contacts the sidewalls of floating gate 5b.

g. Element 1[d]: second oxide regions that cover the sidewalls of the word lines;

82. Kang discloses second oxide regions that cover the sidewalls of the word lines. Kang discloses that "[u]pper portions of [the] first and second sidewalls of the wordlines WL may be covered with the second barrier spacers 26b," wherein "[t]he second barrier spacers 26b may include a medium-temperature oxide (MTO)

layer 23b [i.e., second oxide region] and a second silicon nitride layer 25b.” Ex-1005, 7:48-55; *see also id.*, 8:3-10, 8:16-30, 2:39-45, 7:56-63, 10:43-11:27, Figs. 7-12. For example, medium-temperature oxide (MTO) layer 23b is shown below in Figure 2 in green and covers the sidewalls of tungsten layer 19—i.e., word line shown in yellow.

Fig. 2



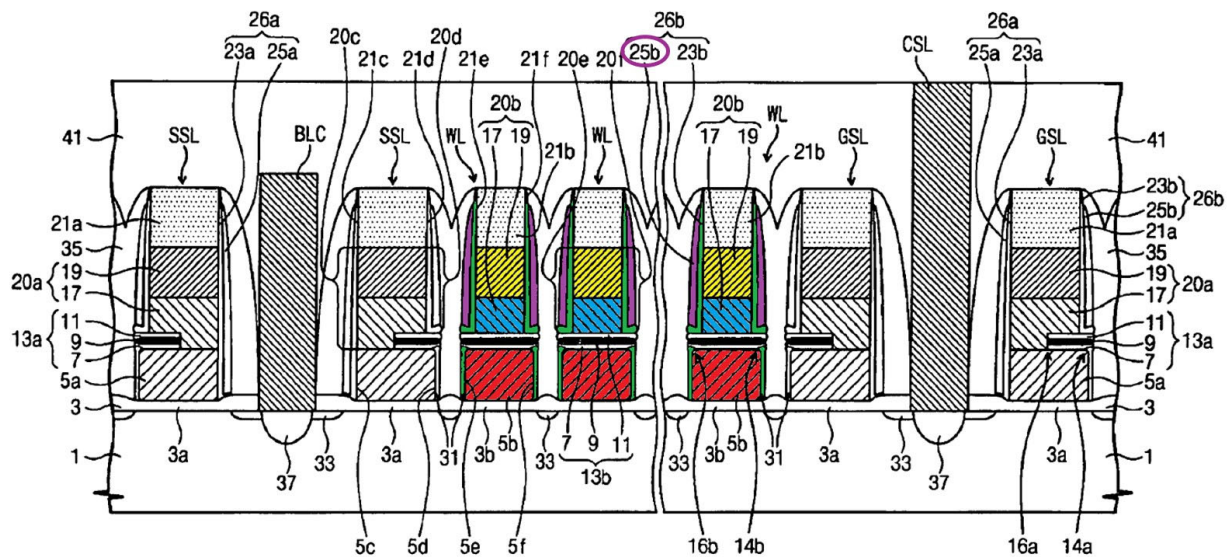
Id., Fig. 2 (annotated). Specifically, a medium-temperature oxide (MTO) layer (e.g., SiO₂) refers to a layer of oxide formed on the exposed surface of a silicon wafer or polysilicon surface by either a thermal growth process or a CVD process at a temperature between 600°C to 800°C, using an oxidizing agent (e.g., oxygen or steam), which is suitable for producing a range of oxide layer thicknesses and properties. Thus, Kang's MTO layer 23b constitutes an oxide region as required by the claim.

83. Further, Kang's MTO layer 23b "covers" the sidewalls of tungsten layer 19—i.e., word lines—in accordance with the '314 Specification. The '314 Patent states, "[a]s used herein, the term 'covered' may include direct physical contact, but does not require direct physical contact." Ex-1001, 6:27-29. And Kang's MTO layer 23b directly contacts the sidewalls of tungsten layer 19.

h. Element 1[e]: nitride regions that cover the second oxide regions; and

84. Kang discloses nitride regions that cover the second oxide regions. Kang discloses that "[u]pper portions of [the] first and second sidewalls of the wordlines WL may be covered with the second barrier spacers 26b," wherein "[t]he second barrier spacers 26b may include a medium-temperature oxide (MTO) layer 23b and a second silicon nitride layer 25b," i.e., nitride region. Ex-1005, 7:48-55; *see id.*, 8:3-10, 8:16-30, 2:39-45, 7:56-63, 10:43-11:40, Figs. 7-12. For example, second silicon nitride layer 25b is shown below in Figure 2 in purple and covers the medium-temperature oxide (MTO) layer 23b—i.e., second oxide region shown in green.

Fig. 2



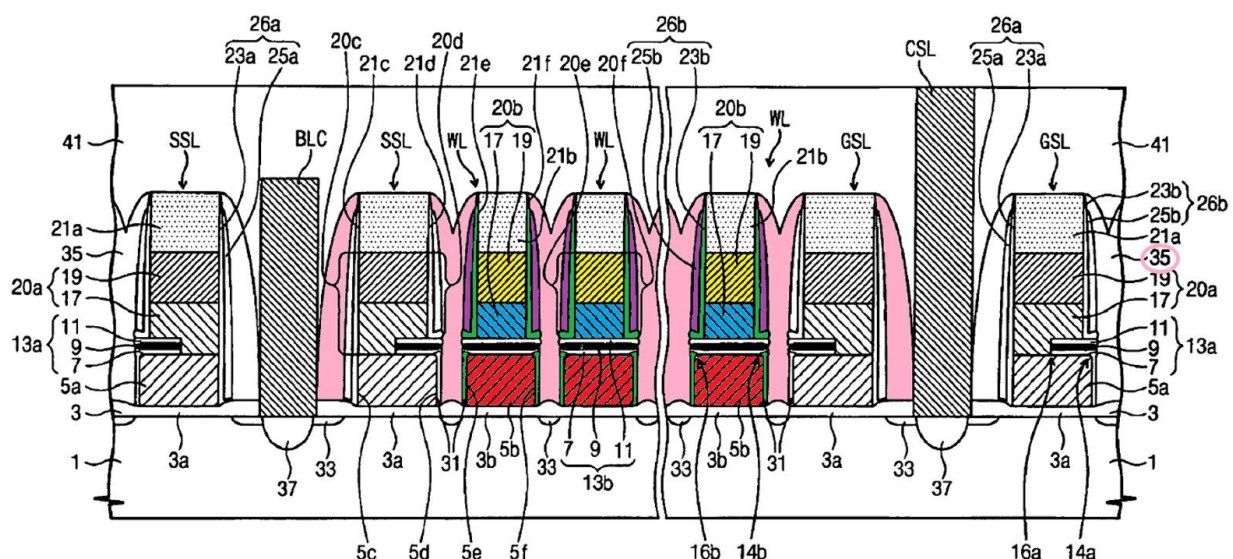
Ex-1005, Fig. 2 (annotated). Specifically, a silicon nitride layer (e.g., Si₃N₄) refers to a layer of nitride that constitutes a nitride region as required by the claim.

85. Further, Kang's silicon nitride layer 25b "covers" the MTO layer 23b—i.e., second oxide region covering the sidewalls of tungsten layer 19—i.e., word lines—in accordance with the '314 Specification. The '314 Patent states, "[a]s used herein, the term 'covered' may include direct physical contact, but does not require direct physical contact." Ex-1001, 6:27-29. And Kang's silicon nitride layer 25b is in direct physical contact with MTO layer 23b that covers the sidewalls of tungsten layer 19.

i. Element 1[f]: electrical isolation regions other than silicon nitride adjacent to the first oxide regions that cover the sidewalls of the charge storage regions.

86. Kang teaches electrical isolation regions that cover the sidewalls of the charge storage regions. Kang discloses that “[s]idewalls of the string selection lines SSL, the ground selection lines GSL and the wordlines WL may be covered with spacers 35.” Ex-1005, 8:66-9:1. As illustrated in Figure 2, “[t]he spacers 35 [shown in pink] may cover the first barrier spacers 26a, the second barrier spacer 26b, the first side 14a of the first intergate dielectric layer 13a and/or the thermal oxide layers 31 covering the sidewalls of the string selection lines SSL, the ground selection lines GSL and the wordlines WL.” *Id.*, 9:1-6; *see id.*, 2:63-3:9, 4:17-32, 12:21-41, Fig. 12. “The spacers 35 may be string-like structures filling the relatively narrow spaces between the string selection lines SSL, the ground selection lines GSL, the wordlines WL, the common source lines CSL and/or the bit line contacts BSL.” *Id.*, 9:6-9.

Fig. 2



Id., Fig. 2 (annotated).

87. Kang's spacers 35 are "adjacent" to thermal oxide layer 31—i.e., first oxide regions—that "cover" the sidewalls of the floating gates 5b—i.e., charge storage regions—in accordance with the '314 Specification. The '314 Patent states, "[a]s used herein, the term 'adjacent' does not require direct physical contact but could include direct physical contact," and "the term 'covered' may include direct physical contact, but does not require direct physical contact." Ex-1001, 6:35-37, 6:27-29. Kang's spacers 35 are in direct physical contact with thermal oxide layer 31 that is in direct physical contact with the sidewalls of floating gate 5b. Thus, a POSITA would have understood that spacers 35 are adjacent to thermal oxide layer 31—i.e., first oxide regions—that cover the sidewalls of floating gate 5b—i.e., charge storage regions. *See supra* §VIII.B.

88. Further, a POSITA would have found it obvious for Kang's spacers 35 to be electrical isolation regions other than silicon nitride because it was well known that using an insulating layer with a low dielectric constant would reduce parasitic capacitance between adjacent gate structures. *See, e.g.*, Ex-1006 ¶¶5-6, 10-11. For example, it was well known to use silicon oxide and other materials with a small dielectric constant (i.e., low-k materials) in the creation of a conformal deposition spacer, as described in Kang, because using a low-k material was a well-known method to reduce the floating gate interference. *See, e.g.*, Ex-1032; Ex-1033. Moreover, a POSITA would have recognized that silicon nitride had a relatively high dielectric constant, especially in comparison to air, which has the lowest dielectric constant. *See, e.g.*, Ex-1006 ¶¶10-11; Ex-1032; Ex-1033. Thus, it would have been obvious to implement Kang's spacers 35—i.e., electrical isolation regions—as a material with a dielectric constant lower than silicon nitride's (e.g., air) to reduce the parasitic capacitance between adjacent floating gates of Kang's memory device. Ex-1006 ¶10.

2. Claim 3: wherein the word lines comprise tungsten.

89. As discussed above, Kang's second control gate 20b "may include...a tungsten layer 19 having a low electrical resistance," which "may help enhance a speed of a memory device." Ex-1005, 6:10-13; *see id.*, 1:23-25, 2:57-58, 4:9-11, 8:19-23, 9:28-33, 10:3-6, 10:17-20, 10:29-31. And a POSITA would have

understood that tungsten layer 19 acts as a word line coupled to the polysilicon layer

17. *See supra* §VIII.C.

3. Claim 4: wherein the charge storage region is a conductive floating gate.

90. As discussed above, Kang discloses that “[a] cell transistor in the cell array region includes a gate insulator, a *floating gate*, an intergate dielectric and a control gate sequentially stacked in the order named.” Ex-1005, 1:20-23 (emphasis added), 5:53-57, Fig. 2. Further, Kang discloses, “[t]he floating gate layer may be made of polysilicon doped with N-type impurities....” *Id.*, 4:12-15, 6:14-16, 9:41-48 (“The floating gate layer 5 may be made of, e.g., polysilicon that may be doped with, e.g., N-type impurities, e.g., phosphorus (P).”). A POSITA would have known that using a polysilicon layer doped with N-type impurities would form a conductive floating gate. *See supra* §VIII.A.

4. Claim 6: further comprising peripheral circuitry, wherein the word lines are electrically coupled to the peripheral circuitry.

91. Kang teaches this limitation. Kang discloses “[n]on-volatile memory devices, such as flash memory devices, generally include a cell array region and a peripheral circuit region for driving the cell array region.” Ex-1005, 1:14-16. A POSITA would have understood that a peripheral circuit “driving the cell array region” would include row decoders and word line drivers connected to the word lines to enable memory access by selectively activating specific rows of memory

cells for reading and writing. *See supra* §VIII.D; Ex-1021 at 346, Fig. 12.13. Thus, a POSITA would have understood that Kang alone describes peripheral circuitry electrically coupled to the word lines of the memory device.

5. Claim 7: wherein the first oxide regions and the second oxide regions comprise silicon oxide and the nitride regions comprise silicon nitride.

92. Kang discloses that “lower portions of the...first and second sidewalls of the word lines WL may be covered with the thermal oxide layer 31,” i.e., first oxide region. Ex-1005, 7:48-52. A POSITA would have understood that a thermal oxide layer typically comprises silicon oxide. This formation of silicon oxide, or silicon dioxide, occurs when the “silicon surface at elevated temperatures is exposed to an oxidizing ambient (such as oxygen or water vapor) and a stable and tenacious oxide forms. The process is known as thermal oxidation. The ability to form an oxide (SiO₂) that is chemically stable at high temperatures and adherent to the silicon is one of the cornerstones of planar silicon processing.” *See* Ex-1031. Thus, Kang discloses that the first oxide region comprises silicon oxide.

93. Further, Kang discloses that “[u]pper portions of [the] first and second sidewalls of the wordlines WL may be covered with the second barrier spacers 26b,” wherein “[t]he second barrier spacers 26b may include a medium-temperature oxide (MTO) layer 23b [i.e., second oxide region] and a second silicon nitride layer 25b,” i.e., nitride region. Ex-1005, 7:48-55; *see also id.*, 9:1-6, 2:32-34, 8:3-10, 8:16-30,

2:39-45. A POSITA would have known that MTO (medium-temperature oxide) is a part of a broader thermal oxidation process that occurs at various temperatures. Thus, Kang discloses nitride regions comprising silicon nitride that cover the second oxide region and renders obvious MTO layer 23b being silicon oxide.

6. Claim 13

a. Previously Addressed Elements

94. Kang meets the following elements of Claim 13 for the reasons discussed in the corresponding sections above.

Element	Addressed in Section:
13[preamble]	§X.A.1.a (1[preamble])
13[a]	§X.A.1.b (1[a])
13[a1]	§X.A.1.c (1[a1])
13[a2]	§X.A.1.d (1[a2])
13[b]	§X.A.1.e (1[b])
13[c]	§X.A.1.f (1[c])
13[d]	§X.A.1.g (1[d])
13[e]	§X.A.1.h (1[e])
13[f]	§X.A.1.i (1[f])

7. Claims 17, 19

95. Claims 17 and 19 replicate recitations of claims 3 and 4, respectively, but in the form of method claims. Kang meets the limitations added by Claims 17 and 19 for the reasons discussed in the corresponding sections above.

Claim(s):	Addressed in Section:
17	§X.A.2 (claim 3)
19	§X.A.3 (claim 4)

B. Ground 2: Claims 1-2, 5-6, 14, and 18 are obvious over Kang in view of Kang-1

96. As shown below, the subject matter of independent Claim 1 and dependent Claims 2, 5-6, 14 and 18 are disclosed by Kang in view of Kang-1.

1. Motivation to combine Kang with Kang-1

97. A POSITA would have been motivated to combine the teachings of Kang and Kang-1 and would have a reasonable expectation of success in doing so at least because they share two of the same named inventors, were filed within months of one another, relate to the same field, and address the same well-known issues. Moreover, Kang and Kang-1 provide complementary solutions for forming non-volatile memory devices with insulators that protect a control gate and “enable a non-volatile memory device having enhanced speed and reliability.” *See, e.g.*, Ex-1005 at Abstract, 1:65-2:10, 9:28-33, 12:42-52; Ex-1006 at Abstract, ¶¶5-6, 45, 68.

A POSITA seeking to decrease the deterioration of cell threshold voltage distribution and/or minimize the parasitic capacitance and any variance between the gate structures would have known of and consulted these proposed solutions. Ex-1005 at 1:25-31; Ex-1006 at Abstract, ¶¶6, 8-14, 17, 44-45, 58, 71-72, Fig. 13.

98. A POSITA would have known that fast and reliable operation of memory cells requires simultaneously minimizing WL RC signal delay and minimizing the window of cell threshold voltage distribution. Both of these efforts involve methods to reduce the R (WL resistance) and C (parasitic capacitance between WL and between adjacent floating gates, including using low-k dielectrics, like air, as a conformal deposition spacer). A POSITA would have known that Kang will address the reduction of WL resistance, while Kang-1 would address the reduction of parasitic capacitance. A POSITA would also recognize that Kang and Kang-1 share similar key process modules such that the combined process would not require additional costly masking steps. Combining Kang and Kang-1 would result in a simple and predictable modification of steps without incurring significant modification in the process flows.

99. Kang discloses “non-volatile memory devices including a barrier spacer that serves to protect a control gate, including a metal layer, from damage that may result from exposure to a cleaning solution and/or oxygen,” and thereby enhance speed and reliability. Ex-1005, 1:65-2:10. Kang further discloses that

“[s]pacers 35 may be formed” to “fill[] the relatively narrow spaces between the string selection lines SSL, the ground selection lines GSL, the wordlines WL, the common source lines CSL and/or the bit line contacts BSL.” *Id.*, 8:62-9:9. Kang-1 discloses structurally similar “semiconductor devices such as memory devices having an air gap defined between adjacent gate structures and methods of fabricating the same.” Ex-1006 ¶3; *see id.*, ¶¶51-59, Figs. 5-10. Kang-1 explicitly notes that “[e]fforts to manufacture devices meeting [a demand for ever higher density memory devices] often involve scaling down the sizes of gate structures and minimizing the space between adjacent gate structures.” *Id.*, ¶5. “Unfortunately, these efforts often result in increased parasitic capacitance between adjacent structures in the memory cell regions,” which “reduce the speed” and “degrad[e] the reliability of the memory devices.” *Id.*, ¶6. A POSITA would have been motivated to implement Kang’s semiconductor memory device using Kang-1’s air gaps because a POSITA would have recognized—as noted in Kang-1—that the “dielectric constant” of the insulating layer filling the spaces between adjacent floating gates “is a primary factor in determining the capacitance between the adjacent floating gates.” *Id.*, ¶10. And a POSITA would have been motivated “to form the dielectric layer from the lowest dielectric constant material possible” and achieve the improvements described in Kang-1, including “a substantial reduction in the parasitic capacitance between adjacent gate structures.” *Id.*, ¶¶10-11, Table 1.

100. In this combination, Kang's semiconductor memory device would have implemented air gaps as spacers 35, as taught by Kang-1, without the need to employ additional photolithographic steps that would significantly modify the process flow. In addition, as the word line spacing—and, thus, the spacing between floating gates—decreases, the more likely it is that the deposition of oxide would leave air gaps because the film would not conform enough to completely fill the gap between word lines. And a POSITA would have had a reasonable expectation of success in achieving the objective of decreasing the deterioration of cell threshold voltage distribution, minimizing the parasitic capacitance and any variance between the gate structures, and enhancing speed and reliability of the memory device by combining the teachings of Kang and Kang-1 with no change in their respective functions because both references solve these problems in similar and predictable ways. *See supra* §§V.A-V.B.

2. Claim 1

a. Previously Addressed Elements

101. Kang and Kang-1 meet the following elements of claim 1 for the reasons discussed in the corresponding sections above.

Element	Addressed in Section:
1[preamble]	§X.A.1.a (1[preamble])
1[a]	§X.A.1.b (1[a])

1[a1]	§X.A.1.c (1[a1])
1[a2]	§X.A.1.d (1[a2])
1[b]	§X.A.1.e (1[b])
1[c]	§X.A.1.f (1[c])
1[d]	§X.A.1.g (1[d])
1[e]	§X.A.1.h (1[e])
1[f]	§X.A.1.i (1[f])

b. Element 1[f]: electrical isolation regions other than silicon nitride adjacent to the first oxide regions that cover the sidewalls of the charge storage regions.

102. In addition to the reasons discussed in Section X.A.1.i (1[f]) above, Kang in view of Kang-1 teaches that it would have been obvious for Kang’s spacers 35 to be electrical isolation regions other than silicon nitride. Kang-1 explicitly notes that “[e]fforts to manufacture devices meeting [a demand for ever higher density memory devices] often involve scaling down the sizes of gate structures and minimizing the space between adjacent gate structures,” and notes that “these efforts often result in increased parasitic capacitance between adjacent structures in the memory cell regions.” Ex-1006 ¶¶5-6. “Such increases in parasitic capacitance reduce the speed of the memory device” and “variation in parasitic capacitance between gate structures causes a variation in the threshold voltage for each gate structure, thereby degrading the reliability of memory devices.” *Id.* Kang-1 further

explains that “one method to improve device performance as device density is increased is to reduce the parasitic capacitance between adjacent floating gates.” *Id.*, ¶10. “Typically, the spaces between adjacent floating gates are filled by an insulating layer whose dielectric constant is a primary factor in determining the capacitance between the adjacent floating gates. An insulating layer formed from a material having a higher dielectric constant will cause increased parasitic capacitance between adjacent gate structures.” *Id.* “Consequently, it is desirable to form the dielectric layer from the lowest dielectric constant material possible.” *Id.* “Table 1 is a list of the approximate dielectric constants of several materials.” *Id.*, ¶11.

TABLE 1

Material	Dielectric Constant
Vacuum	1 (By definition)
Air	1.005
Polyethylene	2.25
Paper	3
Silicon oxide	3.9
Silicon nitride	7.8
Rubber	7
Silicon	11.68
Methyl alcohol	30
Water	80
Barium Titanate	1200

Id. at 2.

103. Table 1 specifically identifies silicon nitride as having a dielectric constant of 7.8. *Id.* And Kang-1 explicitly recognizes, “a substantial reduction in the parasitic capacitance between adjacent gate structures can be achieved by replacing

the silicon oxide or nitride dielectric material commonly used in semiconductor, e.g., memory structures with air.” *Id.*, ¶11. Thus, it would have been obvious to implement Kang’s spacers 35—i.e., electrical isolation regions—as a material with a dielectric constant lower than silicon nitride’s (e.g., paper, polyethylene, air, etc.) to reduce the parasitic capacitance between adjacent floating gates of Kang’s memory device. *Id.*, ¶10; *see supra* §X.A.1. Thus, a POSITA would have applied Kang-1’s specific teaching and implemented Kang’s spacers 35 with a material with a small dielectric constant (i.e., a low-k dielectric material) compatible with semiconductor processing, including air, to achieve Kang-1’s specific benefits.

3. Claim 2: wherein the electrical isolation regions comprise: a plurality of air gaps, each air gap between a neighboring pair of the plurality of word lines, the air gaps being adjacent to first oxide regions.

104. Kang in view of Kang-1 teaches electrical isolation regions comprising a plurality of air gaps between neighboring pairs of word lines and adjacent to first oxide regions. As discussed above, Kang discloses that “[s]idewalls of the string selection lines SSL, the ground selection lines GSL and the wordlines WL may be covered with spacers 35.” Ex-1005, 8:66-9:1. And, specifically, “[t]he spacers 35 may cover...the thermal oxide layers 31 covering the sidewalls of the string selection lines SSL, the ground selection lines GSL and the wordlines WL.” *Id.*, 9:1-6; *see id.*, 2:63-3:9, 4:17-32. Further, Kang-1 recognizes that “the spaces between adjacent floating gates are filled by an insulating layer whose dielectric constant is a primary

factor in determining the capacitance between the adjacent floating gates. An insulating layer formed from a material having a higher dielectric constant will cause increased parasitic capacitance between adjacent gate structures.” Ex-1006 ¶10.

105. Kang-1’s “Table 1 is a list of the approximate dielectric constants of several materials,” showing that air “has an approximate dielectric constant of 1.005.” *Id.*, ¶11.

TABLE 1

Material	Dielectric Constant
Vacuum	1 (By definition)
Air	1.005
Polyethylene	2.25
Paper	3
Silicon oxide	3.9
Silicon nitride	7.8
Rubber	7
Silicon	11.68
Methyl alcohol	30
Water	80
Barium Titanate	1200

Id. at 2. “Consequently, a substantial reduction in the parasitic capacitance between adjacent gate structures can be achieved by replacing the silicon oxide or nitride dielectric material commonly used in semiconductor, e.g., memory structures with air.” *Id.* Thus, it would have been obvious to a POSITA to use air—a material with a low dielectric constant—as Kang’s spacers 35, which are electrical isolation regions—between the neighboring pairs of word lines and adjacent to the thermal

oxide layers 31 covering the sidewalls of the wordlines WL in Kang's memory device. *See supra* §VIII.B.

106. Further, in forming air gaps, a POSITA would have recognized the benefit of enclosing the air gaps using an additional insulation layer. For example, Kang-1 discloses using “[a]n upper insulation layer 138 [brown] [that] covers the gate structures and the air gaps 134” to “seal the air gaps 134.” Ex-1006 ¶¶35, 50, 65, Fig. 3; *see* Ex-1008 at 10:3-20, 6:64-7:6, 7:25-37, 8:7-14, 11:32-43 (using second insulating film 12 to occlude the cavity GP enables control of “the occlusion position of a cavity in a low position as compared with the case where a cavity is simply occluded only by film formation of first insulating film 11” and suppresses “the problem of the corrosion by invasion of cleaning liquid”). Kang similarly discloses that “an interlayer dielectric 41 [brown] may cover the string selection lines SSL, the wordlines WL and the ground selection lines GSL,” so it would have been obvious for interlayer dielectric 41 to form an upper insulation layer that seals the air gap spacers 35 in Kang/Kang-1's memory device. Ex-1005, 9:13-15, Fig. 2.

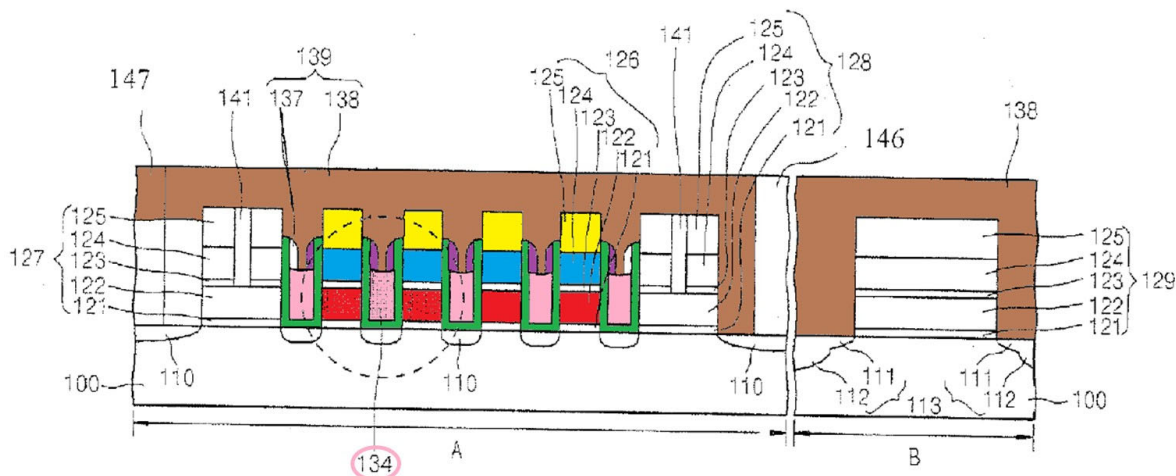
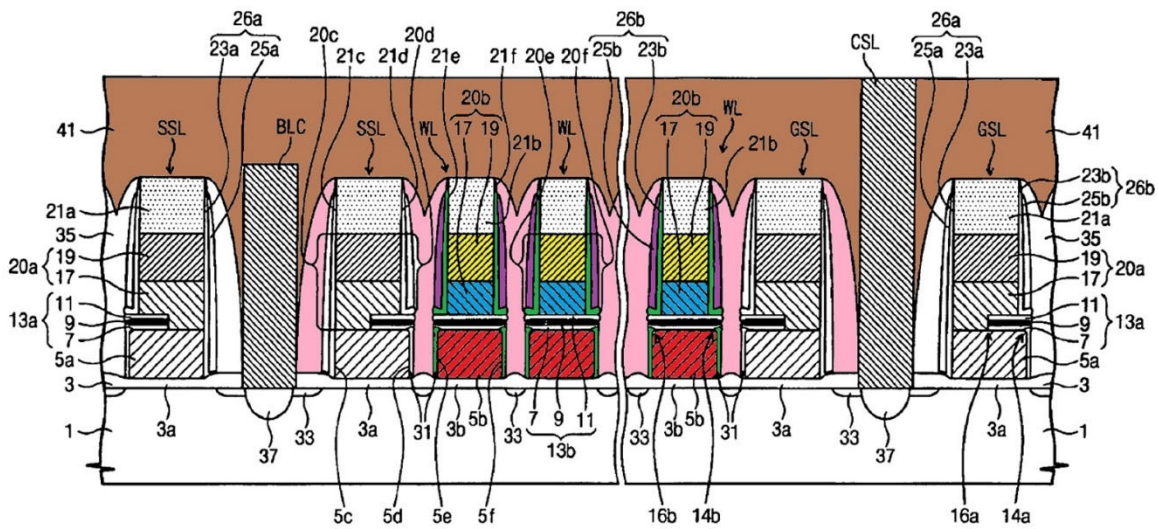


FIG. 3

Ex-1006, Fig. 3 (annotated).

Fig. 2

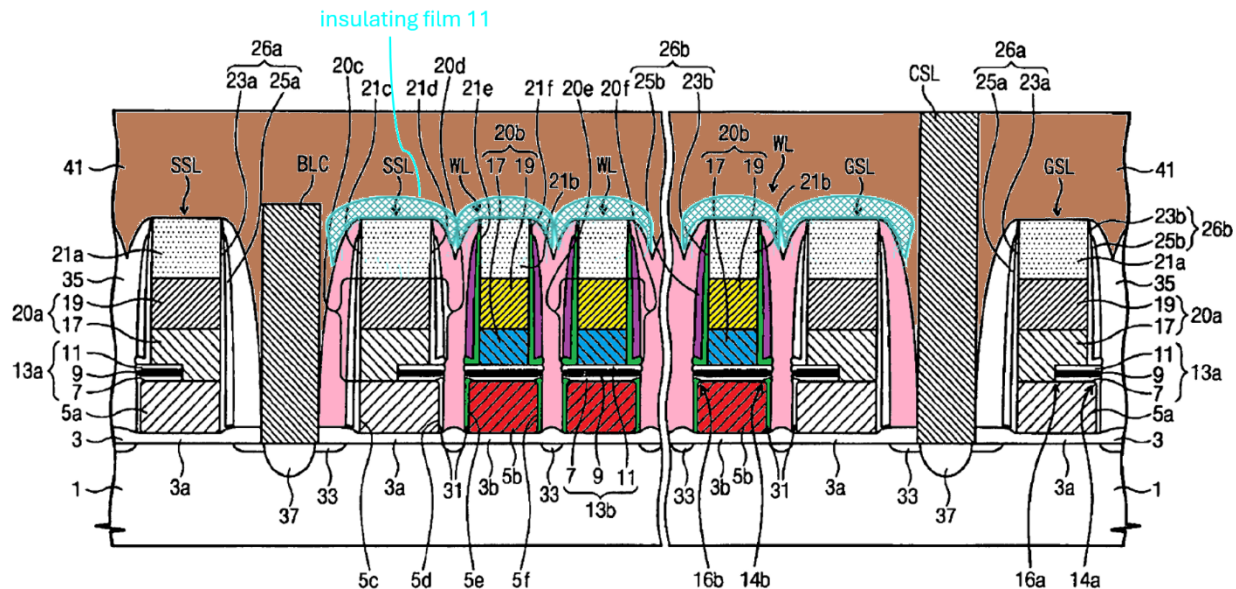


Ex-1005, Fig. 2 (annotated).

107. A POSITA would have known that modifying the process flow of Kang in view of Kang-1 to replace Kang's spacer 35 with an air gap would not require additional critical and expensive photolithographic steps. It would be obvious that,

in addition to simply replacing the spacer layer with air, only an additional dielectric deposition process is required prior to the formation of the interlayer dielectric 41. This additional dielectric deposition process would be one that is similar to the formation of Murata's insulating film 11, *see* Ex-1006 ¶¶65; Ex-1008, Fig. 3, such that each upper surface and side surface of a plurality of convex patterns (such as regions between the signal selection line SSL, the ground selection lines GSL and the word selection lines WL) may be covered. The formation of an insulating film such as the insulating film 11 of Murata, with its profile, would allow the formation of interlayer dielectric 41 in Kang on top of insulating film 11 without filling the air gap cavity with material from layer 41.

Fig. 2



Ex-1005, Fig. 2 (modified and annotated with insulating film 11).

4. Claim 5: wherein the charge storage region is a dielectric charge trapping region.

108. Kang in view of Kang-1 teaches a charge storage region that is a dielectric charge trapping region. As discussed above, Kang discloses that “[a] cell transistor in the cell array region includes a gate insulator, a *floating gate*, an intergate dielectric and a control gate sequentially stacked in the order named.” Ex-1005, 1:20-23 (emphasis added), 5:53-57, Fig. 2. However, a POSITA would have known that “[t]he storage of charges in...a MOSFET can be realized in two ways, which has led to the subdivision of nonvolatile semiconductor memory devices into two main classes,” i.e., floating gate devices and charge-trapping devices. Ex-1024 at 5-6; *See supra* §VIII.A.

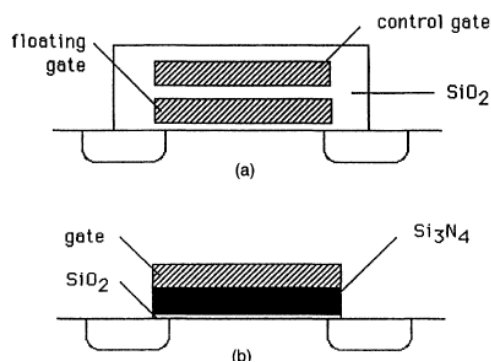


Figure 1.5 Two classes of nonvolatile semiconductor memory devices: (a) floating gate devices; (b) charge-trapping devices (MNOS device).

Ex-1024, Fig. 1.5. Indeed, Kang-1 discloses, “[t]he charge-storage layer 122 may be a polysilicon floating gate or a known charge-trap dielectric layer formed of a material such as silicon nitride or HfAlO.” Ex-1006 ¶¶32, 39 (describing “a nitride (such as silicon nitride) charge-trap layer”). Thus, it would have been obvious over Kang in view of Kang-1 to substitute a dielectric charge trapping region for the

conductive floating gate described in Kang because they are substitutable as a matter of routine design choice for implementing one of two finite choices of classes of non-volatile memory devices as taught by Kang/Kang-1. *See supra* §VIII.A.

5. Claim 6: further comprising peripheral circuitry, wherein the word lines are electrically coupled to the peripheral circuitry.

109. In addition to the reasons discussed in Section X.A.4, this limitation is also obvious over Kang in view of Kang-1. Kang-1 discloses “gate structures...fabricated on a semiconductor substrate 100 with the ground select, cell, and string select gate structures (127, 126, 128, respectively) formed in a cell region A of the substrate 100, and the high voltage gate structures 129 formed in a peripheral region B of the substrate 100.” Ex-1006 ¶32, Fig. 3; *see id.*, ¶¶52, 56, 64.

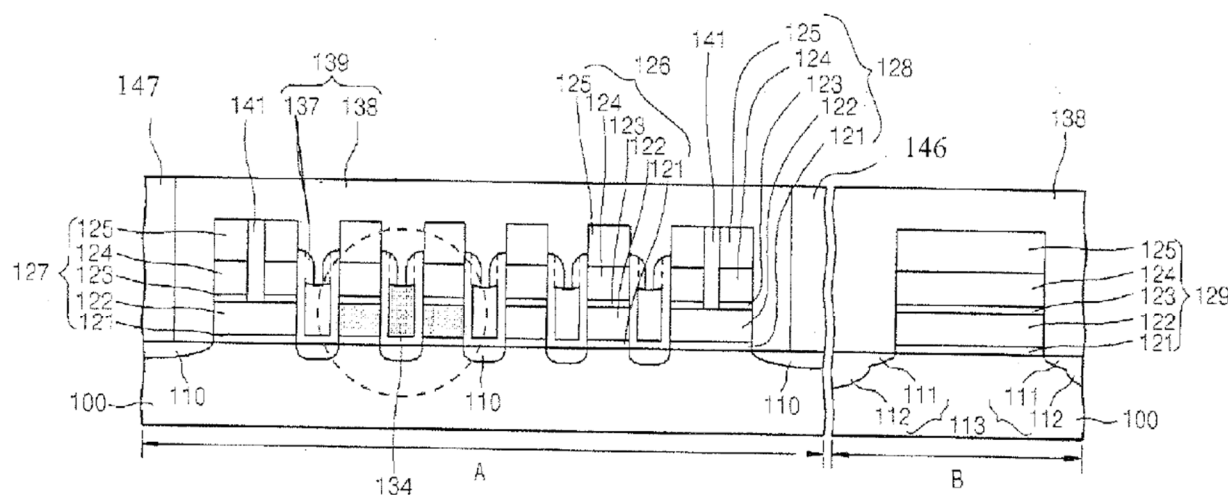


FIG. 3

Ex-1006, Fig. 3.

110. A POSITA would have understood that at least the word lines, string select gate, and other high-voltage gate structures are electrically coupled to peripheral circuitry to enable memory cell selection and operation. One typical application of these high-voltage gate structures is for row decoder transistors to pass the necessary high voltage, such as the programming gate voltage, to the word lines of the memory cell transistors. That is, the high voltage applied to the word line gate enables charge manipulation for data storage and the string select gates control access to the memory cell strings. For example, Figure 12.13 of Micheloni (Ex-1021) illustrates such a typical row decoder circuit with high-voltage transistors. Ex-1021 at 346, Fig. 12.13. The high-voltage transistors enable the pass transistors to connect the high voltages generated from the periphery circuits to the word lines of the memory device. *Id.*

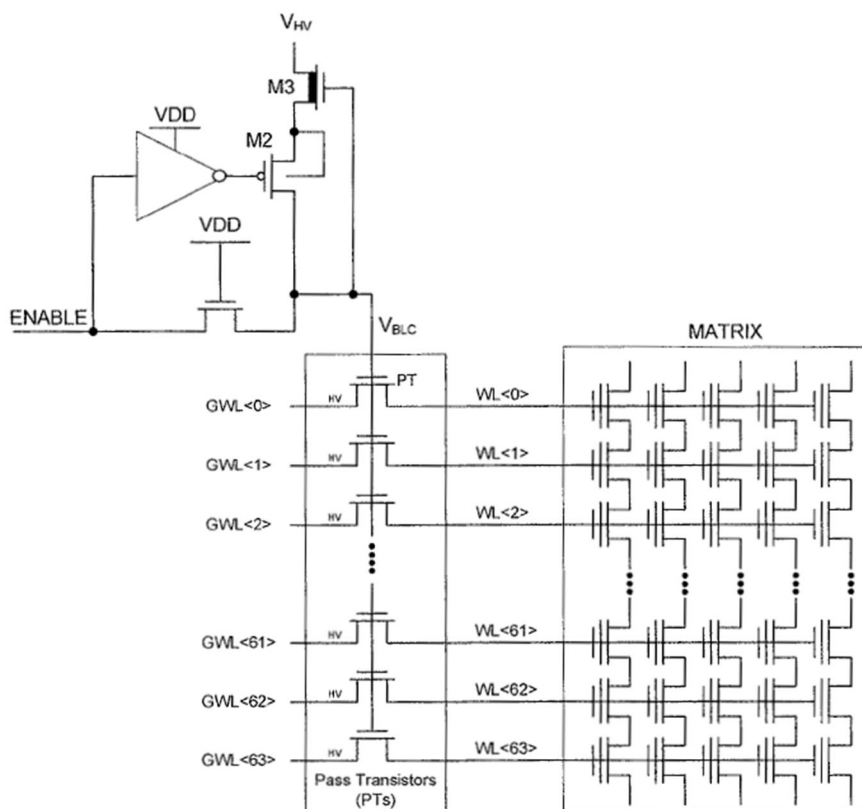


Fig. 12.13. Row decoder with a HV PMOS

Id., Fig. 12.13. Thus, a POSITA would have understood that Kang in view of Kang-1 teaches peripheral circuitry electrically coupled to the word lines of the memory device. *See supra* §VIII.D.

6. Claims 14, 18

111. Claims 14 and 18 replicate recitations of Claims 2 and 5, respectively, but in the form of method claims. Kang meets limitations added by Claims 14 and 18 for the reasons discussed in the corresponding sections above.

Claim(s):	Addressed in Section:
14	§X.B.3 (claim 2)
18	§X.B.4 (claim 5)

C. Ground 3: Claims 1-2, 4-6, 13-14, 18-19 are obvious over Purayath

112. As shown below, the subject matter of independent Claims 1 and 13 and dependent Claims 2, 4-6, 14, and 18-19 are disclosed by Purayath.

1. Claim 1

a. Element 1[preamble]: A memory device comprising:

113. If Claim 1's preamble is limiting, Purayath discloses the preamble. Purayath is "directed to high density semiconductor devices, such as non-volatile storage, and methods of forming the same." *See* Ex-1007 ¶¶5, 7, 31, 162.

b. Element 1[a]: a plurality of lines of memory cells, the memory cells comprising:

114. Purayath discloses, "[o]ne popular flash EEPROM architecture utilizes a NAND array having a large number of strings of memory cells connected through one or more select transistors between individual bit lines and common source lines." Ex-1007 ¶8. "An example of a NAND type of memory array that can be fabricated in accordance with embodiments of the present disclosure is shown in plan view in FIG. 3." *Id.*, ¶37, Fig. 3.

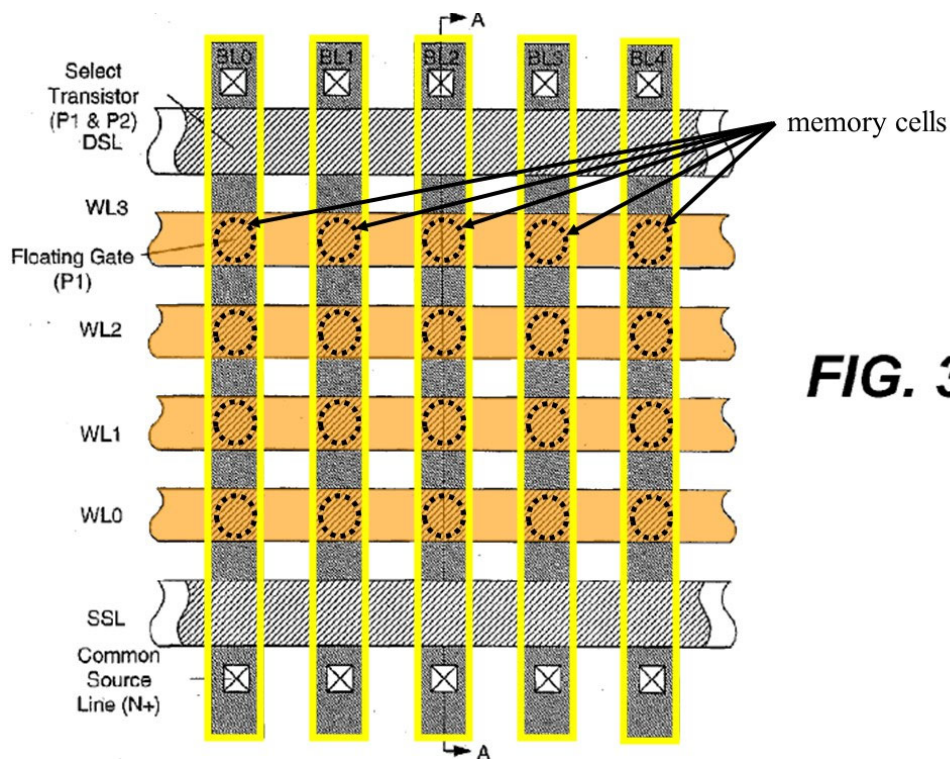


FIG. 3

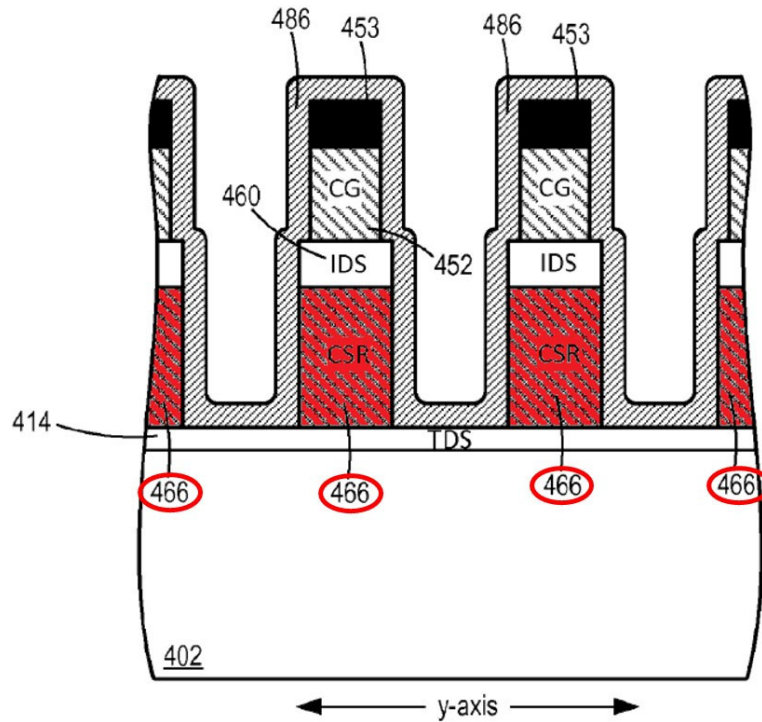
Id., Fig. 3 (annotated). “BL0-BL4 represent bit line connections to global vertical metal bit lines (not shown). Four floating gate memory cells are shown in each string [outlined in yellow] by way of example. Typically, the individual strings include 16, 32 or more memory cells, forming a column of memory cells.” *Id.*, ¶37. “Control gate (word) lines labeled WL0-WL3 [orange] extend across multiple strings over rows of floating gates, often in polysilicon.” *Id.*; *see supra* VIII.E.

c. Element 1[a1]: a charge storage region having sidewalls; and

115. Purayath discloses “a method of fabricating non-volatile storage with air gap isolation,” as shown in the flowchart of Figure 6 and the corresponding cross-sectional views of Figures 7A-7T. *See* Ex-1007 ¶42, Figs. 6, 7A-7T. For example,

“[a]t step 504, an initial layer stack is formed over the substrate surface.” *Id.* As shown in Figure 7A, “a layer stack 401 [is] formed over the surface of a substrate 402” and “includes a tunnel dielectric layer (TDL) 404, a charge storage layer (CSL) 406, a sacrificial layer (SL) 408 and one or more hard masking layer(s) (HML) 410.” *Id.*, ¶44, Fig. 7A. Figure 7B then “depicts the memory array after etching,” wherein “[e]tching forms layer stack columns 403 that are elongated in the direction of the y-axis” that “include[] a tunnel dielectric strip (TDS) 414, a charge storage strip (CSS) 416, a sacrificial strip (SS) 418 and a hard masking strip (HMS) 420.” *Id.*, ¶51. And Figure 7L depicts the result of etching in the “row direction along the x-axis” to “form[] layer stack rows 411.” *Id.*, ¶¶74, 67, Fig. 7L. “Layer 440 [shown in Figure 7K] is etched into intermediate dielectric strips (IDS) 460 and the charge storage strips 416 [shown in Figure 7K] are each etched into a column of charge storage regions (CSR) 466.” *Id.*, ¶74. Thus, each layer stack row 411 includes a hard masking strip 454, a control gate 452, intermediate dielectric strip 460, and *a charge storage region 466*. *See id.*, Figs. 7L-7T, ¶¶74, 100.

116. Purayath further describes the charge storage regions 466 as having vertical sidewalls. *Id.*, ¶81; *see id.*, ¶104. For example, Purayath’s Figure 7S depicts the storage device comprising charge storage regions 466 shown in red, wherein “a dielectric liner is formed along the sidewalls of the layer stack rows,” including the sidewalls of the charge storage regions 466. *Id.*, ¶81; *see supra* §VIII.A.

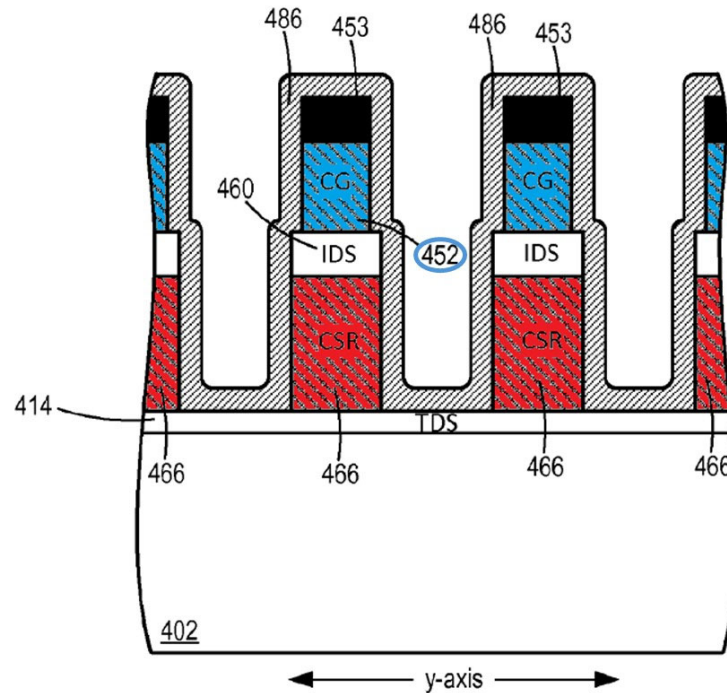


Ex-1007, Fig. 7S (annotated).

d. Element 1[a2]: a control gate;

117. Purayath discloses that each layer stack row 411 includes a hard masking strip 454, a control gate 452, intermediate dielectric strip 460, and a charge storage region 466. See Ex-1007, Figs. 7L-7T, ¶¶70, 72, 76, 81, 100. (It should be noted that the hard masking strip 454 is an intermediate layer used to facilitate the patterning of control gate feature. This intermediate layer is removed, as shown in Figure 7P, to allow the formation of silicide layer 453 on top of control gate 452.) For example, Purayath's Figure 7S depicts the storage device comprising control gates 452 shown in blue, wherein "a dielectric liner is formed along the sidewalls of

the layer stack rows,” including the sidewalls of the control gates 452 and “over the upper surface of the control gates 452.” *Id.*, ¶81. Prior to reaching the process step at Figure 7S, Figure 7Q depicts the result of step 536 in one embodiment where an upper portion 453 of each control gate is transformed into silicide.



Id., Fig. 7S (annotated).

- e. **Element 1[b]: a plurality of word lines each having sidewalls, each of the word lines being associated with a line of the memory cells, each of the word lines being coupled to the control gates of the memory cells with which it is associated;**

118. Purayath teaches a plurality of word lines coupled to the control gates of the memory cells with which it is associated. Purayath discloses that “[a] continuous layer of conductive layer 336 can be formed which is consistent across a

row in order to provide a common word line or control gate for each device on that word line. In such a case, this layer can be considered to form a control gate for each memory cell at the point where the layer overlaps a corresponding floating gate layer 332. In other embodiments, individual control gates can be formed and then interconnected by a separately formed word line.” Ex.-1007 ¶38. Purayath further discloses “[a]n upper portion 453 of each control gate is transformed into silicide.” Ex-1007 ¶¶80, 104, 78-79, 87. “In one example, the control gate layer has a lower portion that is formed from polysilicon and an upper portion that is formed from metal. A barrier layer may be formed between the polysilicon and the metal, to prevent silicidation.” *Id.*, ¶65. “The control gate layer can include, by way of example (from layers to upper layers as move away from substrate surface): a barrier metal and metal; a barrier metal, polysilicon and silicide; a barrier metal and silicide (e.g., FUSI); polysilicon, a barrier metal and metal.” *Id.* “Barrier metals may include, but are not limited to, Ti, TiN, WN and TaN or a combination with related alloys that have a suitable electron work function. Metals may include, but are not limited to, W, WSi₆ or other similar low resistivity metals. Silicides may include, but are not limited to, NiSi, CoSi.” *Id.* A POSITA would have understood that a metal silicide end portion 453 of a control gate may form a word line coupled to the control gate of the memory cell with which it is associated. Ex-1025 at 8-13.

119. Additionally, under the embodiment of Figure 5A of the '314 Patent, word line is associated to the conductive layer formed on top of conductive control gate (526), and that in this particular embodiment, “the word line 528 is formed from tungsten.” Ex-1001, 6:4-5, Fig. 5A. Furthermore, the '314 Patent also indicates that the control gate of a storage element may be provided as a portion of the word line. Ex.1001, 5:9-10. Under this context, again a POSITA would have understood that a control gate layer having an upper portion formed from metal in Purayath would form the word line coupled to the control gate of the memory cell with which it is associated.

120. Purayath teaches that its plurality of word lines each have sidewalls. Purayath's Figure 7S depicts the storage device comprising control gates 452 shown in blue and silicided portions 453 of each control gate shown in the yellow cross-hatched region, wherein “a dielectric liner is formed along the sidewalls of the layer stack rows,” including the sidewalls of the control gates 452 and silicided portions 453 of each control gate and “over the upper surface of the control gates 452.” *Id.*, ¶81.

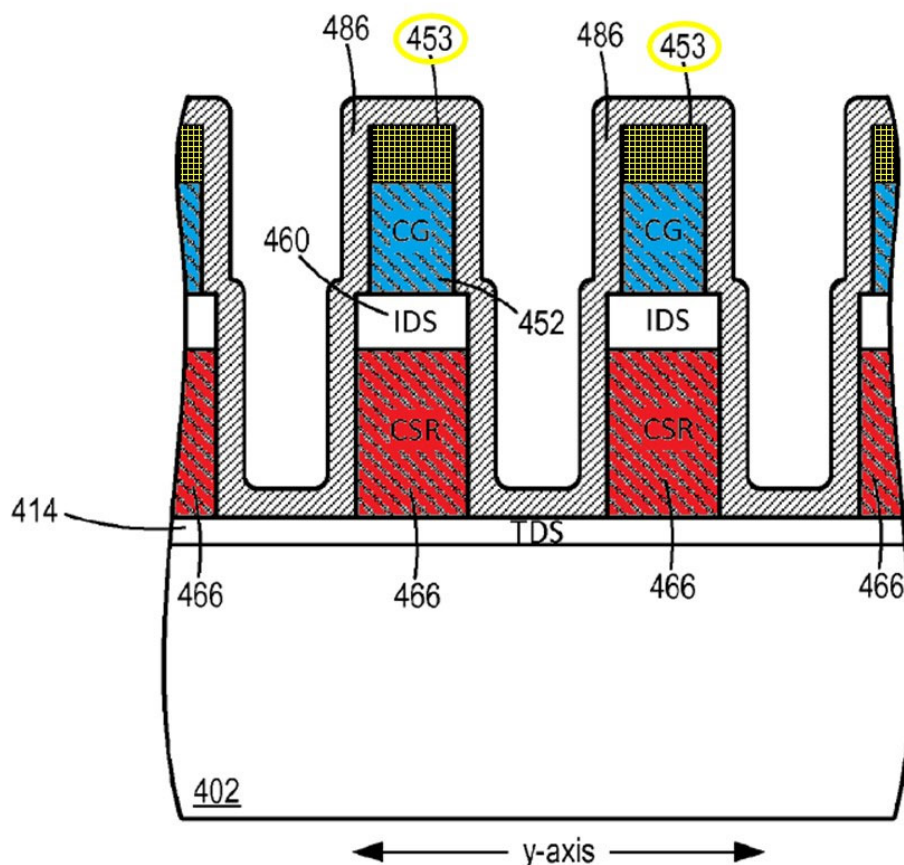
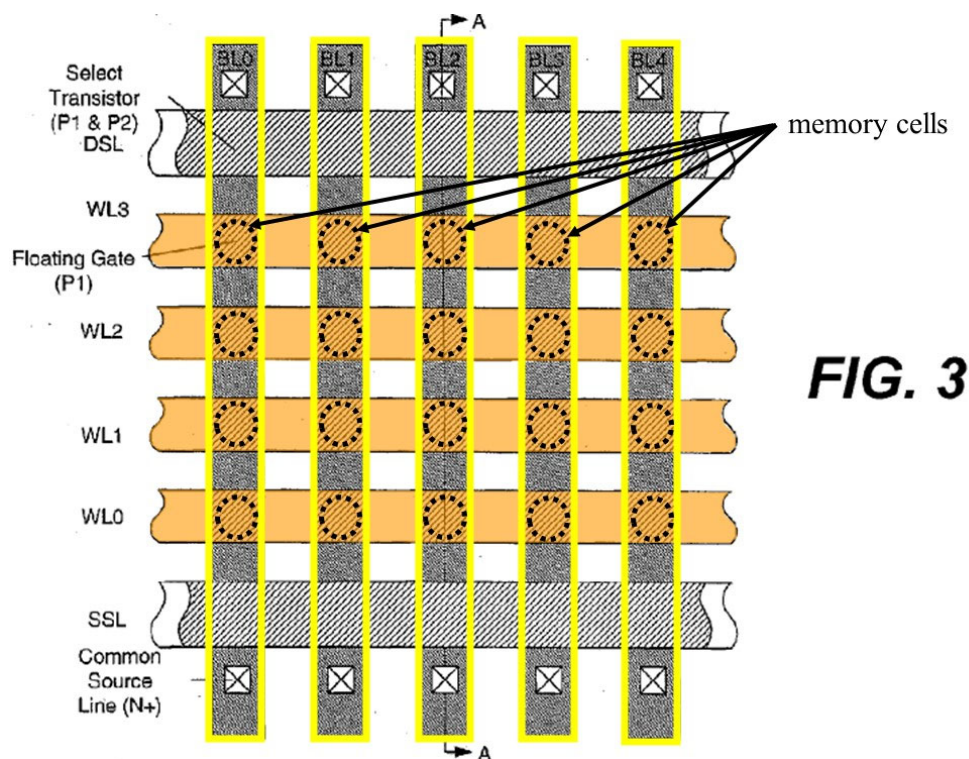


FIG. 7S

Id., Fig. 7S (annotated). Thus, a POSITA would have understood that Purayath's silicided portions 453 have sidewalls.

121. And Purayath discloses that each of the word lines is associated with a line of memory cells. Purayath discloses that “[c]ontrol gate (word) lines labeled WL0-WL3 [shown in orange in Figure 3] extend across multiple strings [outlined in yellow] over rows of floating gates, often in polysilicon.” *See id.*, ¶37, Fig. 3. Thus, a POSITA would have understood that Purayath's silicided portions 453 are coupled to the control gates 452 of the memory cells with which they are associated and are

associated with a line of memory cells. *See supra* §VIII.C.

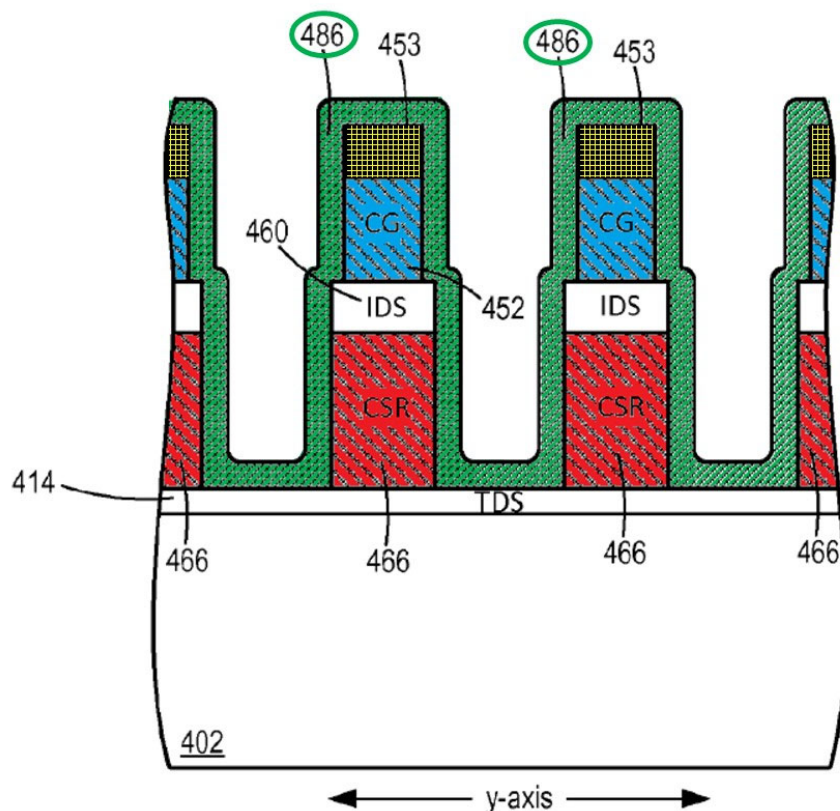


Ex-1007, Fig. 3 (annotated).

f. Element 1[c]: first oxide regions that cover the charge storage regions;

122. Purayath discloses that “[a]t step 540, a dielectric liner is formed along the sidewalls of the layer stack rows. FIG. 7S depicts the results of step 540,” wherein “[l]iner [486] (e.g., oxide) [shown in green] is formed along the sidewalls 413 of the layer stack rows, over the upper surface of the control gates 452, and over the exposed upper surface of the tunnel dielectric strips 414.”² Ex-1007 ¶81, Figs. 7S-7T.

² A POSITA would have understood that the specification mistakenly refers to “liner



Id., Fig. 7S (annotated). Purayath’s liner 486 “covers” the charge storage region 466 in accordance with the ’314 Specification. The ’314 Patent states, “[a]s used herein, the term ‘covered’ may include direct physical contact, but does not require direct physical contact.” Ex-1001, 6:27-29. And Purayath’s liner 486 directly contacts the sidewalls of charge storage region 466. Thus, a POSITA would have understood that liner 486 may be an oxide and cover the charge storage regions 466.

484,” which is correctly identified as liner 486 in Figures 7S-7T. *Compare* Ex-1007 ¶¶77-78, Fig. 7O (discussing oxide spacers 484 that are etched away), *with id.*, ¶81 (discussing liner 484), *and id.*, ¶¶82-83, 88, Figs. 7S-7T (discussing liner 486).

g. Element 1[d]: second oxide regions that cover the sidewalls of the word lines;

123. Purayath discloses that “[a]t step 540, a dielectric liner is formed along the sidewalls of the layer stack rows.” And, as depicted in Figure 7S, “[l]iner [486] (e.g., oxide) is formed along the sidewalls 413 of the layer stack rows.” Ex-1007 ¶81, Figs. 7S-7T. Purayath’s liner 486 is thus formed over both the sidewalls of the charge storage regions and the word line. Although not required, this is the same as the disclosure in the ’314 Patent, where a single silicon oxide layer 532 is formed “over sidewalls of the memory cell, as well as over the sidewalls of the word line 528” and having “a first region 532a adjacent to the charge storage region 522 and a second regions 532b adjacent to the word line 528.” Ex-1001, 6:23-25, 6:29-37, Figs. 5A, 8D-8E.

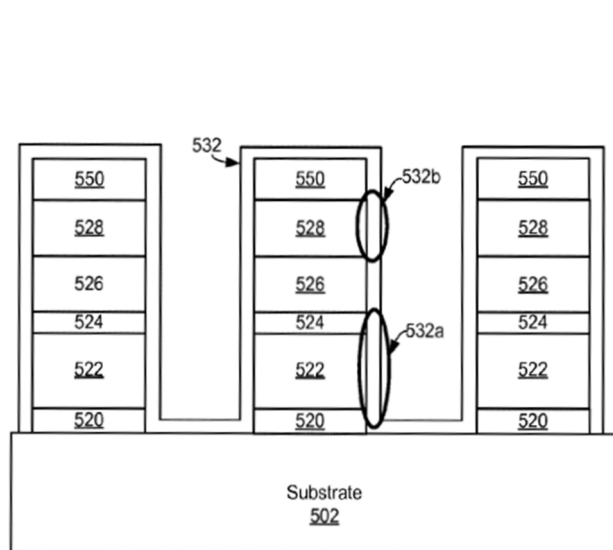


Fig. 8D

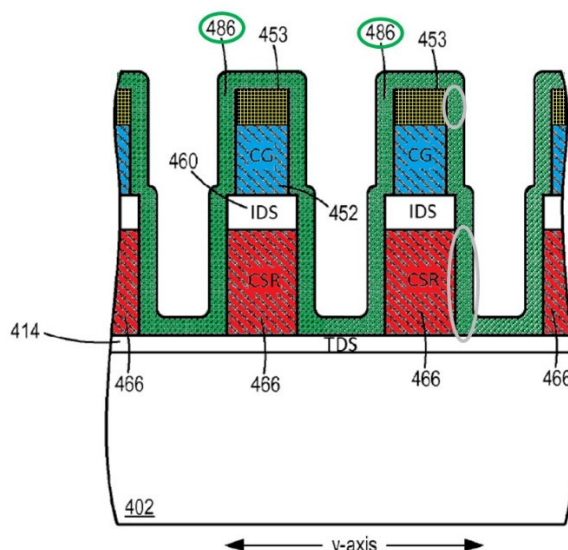


FIG. 7S

Compare id., Fig. 8D, with Ex-1007, Fig. 7S (annotated).

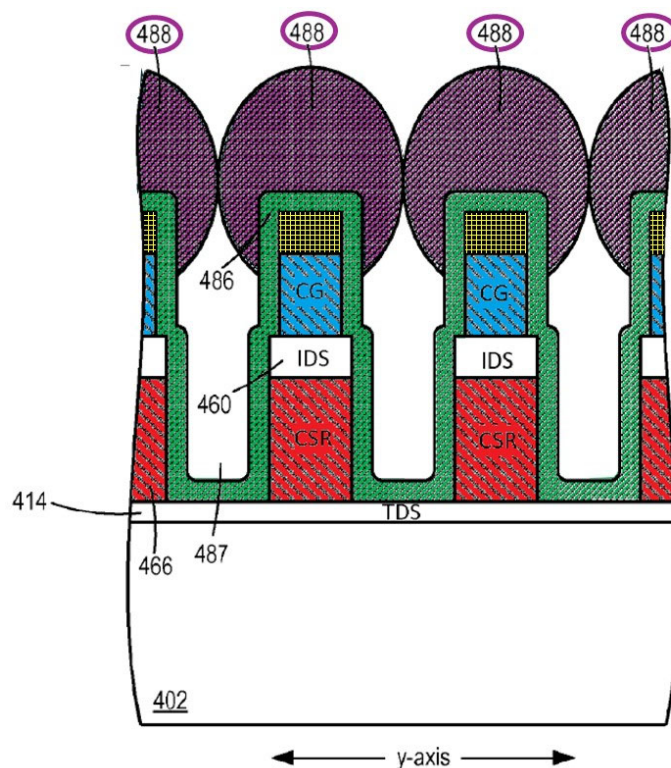
124. Purayath's liner 486 "covers" the sidewalls of the silicided portions 453—i.e., word lines—in accordance with the '314 Specification. The '314 Patent states, "[a]s used herein, the term 'covered' may include direct physical contact, but does not require direct physical contact." Ex-1001, 6:27-29. And Purayath's liner 486 directly contacts the sidewalls of silicided portions 453. Thus, a POSITA would have understood that liner 486 may be an oxide and cover the sidewalls of the word lines 453.

h. Element 1[e]: nitride regions that cover the second oxide regions; and

125. Purayath discloses that "[a]t step 542, word line air gap caps are formed to define word line gaps between the layer stack rows." Ex-1007 ¶82, Fig. 6. "FIG. 7T depicts the results of step 544 in an example where a capping layer 488 is formed over the layer stack rows using a non-conformal deposition process. By using a non-conformal deposition process, material 488 will be deposited unequally at the upper portion of the layer stack rows." *Id.*, ¶83, Fig. 7T.

126. "Material 488 extends vertically toward the substrate surface along the liner 486 on a portion of vertical sidewalls 413 of the layer stack rows. The amount of this vertical dimension will define an upper endpoint of the air gaps at a lower surface of material 486. In this example, it is seen that the air gap extends vertically beyond the level of the upper surface of the control gates." *Id.* For example, Purayath's Figure 7T depicts the result of completing the front end processing of the

non-volatile storage with air gap isolation. *Id.*, ¶83, Fig. 6. As shown in Figure 7T, the storage device comprises layer/material 488 shown in purple.



Id., Fig. 7T (annotated). Purayath’s material 488 “covers” the portions of liner 486 that cover the sidewalls of silicided portions 453—i.e., second oxide regions—in accordance with the ’314 Specification. The ’314 Patent states, “[a]s used herein, the term ‘covered’ may include direct physical contact, but does not require direct physical contact.” Ex-1001, 6:27-29. And Purayath’s material 488 directly contacts the portions of liner 486 that cover the sidewalls of silicided portions 453.

127. “In one embodiment, layer 488 is an oxide (e.g., TEOS, PECVD silane oxide or HDP oxide) but other materials such as nitrides may [be] used in other

implementations.” Ex-1007 ¶83. And a POSITA would have found it obvious to use nitride for dielectric layer 488 because oxide and nitride are typical dielectric layers that are most frequently used in silicon semiconductor processes. Ex-1006 ¶11. Given that this layer of material that covers the second oxide region would need to be removed in the periphery area on the same substrate during the subsequent processing steps, the choice of nitride as a dielectric layer, which is different than the oxide in the second oxide region, would be preferred. The second oxide region would serve as a natural etch stop in the removal of the nitride layer in the periphery circuit regions, so that the removal of the nitride would not damage the periphery circuitry underneath the nitride and the second oxide region. A POSITA would have known that using different materials for two adjacent layers to take advantage of their difference in etch rates is a common scheme employed in removing an upper layer without significantly impacting the underlying layer. Thus, a POSITA would have understood that Purayath discloses a nitride region (i.e., capping layer 488) that covers the second oxide regions (i.e., liner 486) that cover the sidewalls of the word lines (i.e., metal silicide end portion 453 of control gate 452).

i. Element 1[f]: electrical isolation regions other than silicon nitride adjacent to the first oxide regions that cover the sidewalls of the charge storage regions.

128. Purayath discloses that “[a]t step 542, word line air gap caps are formed to define word line gaps between the layer stack rows. The air gaps are elongated in

the x-direction to provide electrical isolation or shielding between elements of adjacent layer stack rows.” Ex-1007 ¶82, Fig. 6. “The vertical dimension and column dimension (along y-axis) of the air gaps can vary to meet the particular requirements of a given implementation. The air gaps extend in the word line direction between adjacent rows of cells.” *Id.* “In one example, the air gaps extend from above the substrate surface (separated therefrom by tunnel dielectric layer 414 and liner 486) to above the upper surface of the control gates 452. The air gaps may be smaller or larger in other examples.” *Id.*

129. “Material 488 quickly accumulates, meeting at a location over the spaces between rows to form air gaps 487 that are elongated in the x-direction.” *Id.*, ¶83. “Material 488 extends vertically toward the substrate surface along the liner 486 on a portion of vertical sidewalls 413 of the layer stack rows. The amount of this vertical dimension will define an upper endpoint of the air gaps at a lower surface of material 486. In this example, it is seen that the air gap extends vertically beyond the level of the upper surface of the control gates.” *Id.* For example, Purayath’s Figure 7T depicts the result of completing the front end processing of the non-volatile storage with air gap isolation. *Id.*, ¶83, Fig. 6. As shown in Figure 7T, the storage device comprises air gaps 487 shown in pink.

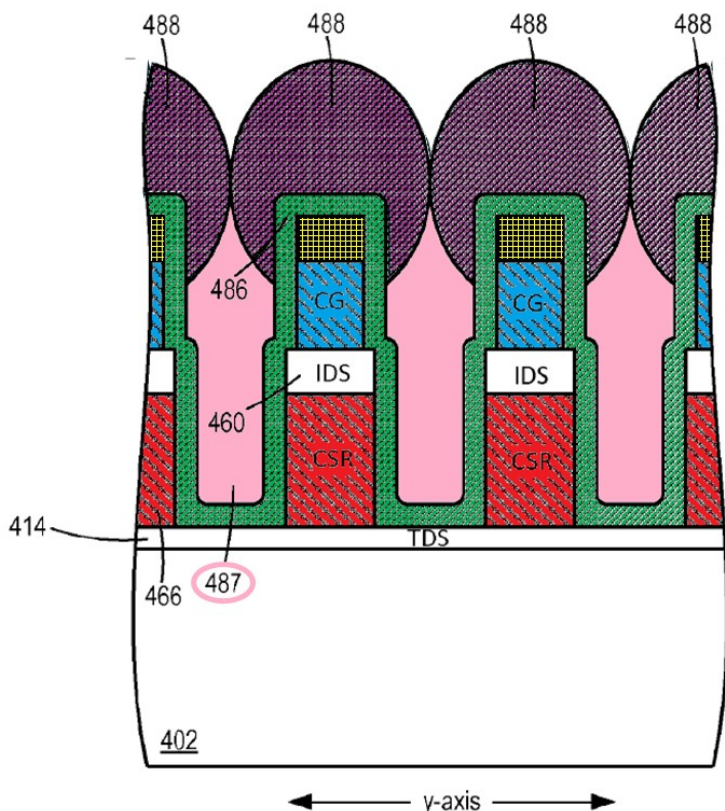


FIG. 7T

Id., Fig. 7T (annotated).

130. Purayath's air gaps 487 are "adjacent" to liner 486—i.e., first oxide regions—that "cover" the sidewalls of the charge storage region 466 in accordance with the '314 Specification. The '314 Patent states, "[a]s used herein, the term 'adjacent' does not require direct physical contact but could include direct physical contact," and "the term 'covered' may include direct physical contact, but does not require direct physical contact." Ex-1001, 6:35-37, 6:27-29. Purayath's air gaps 487 are in direct physical contact with liner 486 that is in direct physical contact with the sidewalls of charge storage region 466. Thus, Purayath discloses air gaps 487 that

are electrical isolation regions—other than silicon nitride—adjacent to the first oxide regions (i.e., liner 486) that cover the sidewalls of the charge storage regions (i.e., charge storage region 466). *See supra* §VIII.B.

2. **Claim 2: wherein the electrical isolation regions comprise: a plurality of air gaps, each air gap between a neighboring pair of the plurality of word lines, the air gaps being adjacent to first oxide regions.**

131. Purayath meets the limitation added by Claim 2 for the reasons discussed above for claim limitation 1[f]. *See supra* §X.C.1.i; *See supra* §VIII.B.

3. **Claim 4: wherein the charge storage region is a conductive floating gate.**

132. Purayath discloses that “[t]he charge storage layer is a polysilicon floating gate layer in one embodiment” but that “[d]ielectric charge storage materials, metal and non-metal nanostructures (e.g., carbon) can also be used for the layer of charge storage material.” Ex-1007 ¶¶46-47, 41. Purayath recognizes that “[t]he charge storage elements of current flash EEPROM arrays are most commonly electrically conductive floating gates, typically formed from a doped polysilicon material.” *Id.*, ¶10; *see* Ex-1024 at 5-7; *See supra* §VIII.A.

4. **Claim 5: wherein the charge storage region is a dielectric charge trapping region.**

133. Purayath discloses that “[t]he charge storage layer is a polysilicon floating gate layer in one embodiment” but that [d]ielectric charge storage materials, metal and non-metal nanostructures (e.g., carbon) can also be used for the layer of

charge storage material.” Ex-1007 ¶¶46-47, 41. Indeed, after discussing conductive floating gates, Purayath recognizes that “[a]nother type of memory cell useful in flash EEPROM systems utilizes a non-conductive floating gate to form a charge storage element capable of storing charge in a non-volatile manner.” *Id.*, ¶10; *see* Ex-1024 at 5-7. For example, “[a] triple layer dielectric formed of silicon oxide, silicon nitride and silicon oxide (‘ONO’) is sandwiched between a conductive control gate and a surface of a semi-conductive substrate above the memory cell channel.” Ex-1007 ¶10. Thus, a POSITA would have recognized that Purayath discloses a dielectric charge trapping region. Ex-1024 at 5-6; *See supra* §VIII.A.

5. Claim 6: further comprising peripheral circuitry, wherein the word lines are electrically coupled to the peripheral circuitry.

134. Purayath discloses, “[a]t step 546 [not shown in Figure 6], front end processing is completed. In one example, step 546 may include interconnecting the floating gate and control gate regions of select and peripheral circuitry transistors.” Ex-1007 ¶85. “Peripheral gate connections can be formed using vias or contact holes, etc. to form contacts to individual gate regions or to connect multiple transistors to a common control line.” *Id.* Further, “[a]rray connections can also be patterned and formed,” and “[a]fter forming contacts, etc., further backend processing to form metal layers, etc. to complete the device according to known techniques can be performed.” *Id.* “For example, a passivation dielectric layer can

be deposited, followed by forming metal conductive lines and vias to connect the lines with source and drain regions at the end of the memory cell strings, etc.” *Id.* Thus, a POSITA would have understood that Purayath describes peripheral circuitry electrically coupled to the word lines of the memory device. *See* Ex-1007 ¶¶85, 151, 45, 49, Fig. 17; *see also supra* §VIII.D; Ex-1021 at 346, Fig. 12.13.

6. Claims 14, 18-19

135. Claims 14, 18-19 replicate recitations of Claims 2, 5, and 4, respectively, but in the form of method claims. Purayath meets the limitations added by Claims 14, 18-19 for the reasons discussed in the corresponding sections above.

Claim(s):	Addressed in Section:
14	§X.C.2 (claim 2)
18	§X.C.4 (claim 5)
19	§X.C.3 (claim 4)

7. Claim 13

a. Previously Addressed Elements

136. Purayath meets the following elements of Claim 13 for the reasons discussed in the corresponding sections above.

Element	Addressed in Section:
13[preamble]	§X.C.1.a (1[preamble])

13[a]	§X.C.1.b (1[a])
13[a1]	§X.C.1.c (1[a1])
13[a2]	§X.C.1.d (1[a2])
13[b]	§X.C.1.e (1[b])
13[c]	§X.C.1.f (1[c])
13[d]	§X.C.1.g (1[d])
13[e]	§X.C.1.h (1[e])
13[f]	§X.C.1.i (1[f])

D. Ground 4: Claims 3, 7, 17 are obvious over Purayath in view of Murata

137. As shown below, the subject matter of dependent Claims 3, 7, and 17 are taught by Purayath in view of Murata.

1. Motivation to combine Purayath with Murata

138. A POSITA would have been motivated to combine the teachings of Purayath and Murata and would have a reasonable expectation of success in doing so at least because they are from the same field and address the same well-known issues. Moreover, Purayath and Murata provide complementary solutions for forming semiconductor memory devices with insulating layers that protect a control gate and electrical isolation regions or cavities between discrete devices that improve device performance as features sizes of circuit elements continuously decrease. *See*,

e.g., Ex-1007 at Abstract, ¶¶12, 31-33, 40; Ex-1008 at Abstract, 1:45-55, 4:18-27. A POSITA seeking to decrease the deterioration of cell threshold voltage distribution and/or minimize the parasitic capacitance would have known of and consulted these proposed solutions. Ex-1007 at Abstract, ¶¶10, 12, 37, 40; Ex-1008 at Abstract, 1:45-55, 4:18-27.

139. From a general perspective, while Purayath attempts to provide a full “electrical isolation between discrete devices in nonvolatile memory and that the electrical isolation is provided, at least in part, by air gaps that are formed in the column (bit line) direction and/or air gaps that are formed in the row (word line) direction.” Ex-1007 ¶31, Purayath would look to solutions that would preserve the integrity of the air gap cavity that is formed both in the bit line direction and/or the word line direction. Murata’s invention addresses the tailoring of the process flow such that “a cavity is occluded in a position lower than the upper surface of a control gate. When CMP is performed after the second insulating film is formed by this, the problem of the corrosion by invasion of the cleaning liquid to a cavity is suppressed.” Ex-1008 ¶19. A POSITA seeking to achieve a reliable electrical isolation by air gaps would have known of and consulted the solution of Murata for forming corrosion free air gaps isolation.

140. Furthermore, Purayath discloses “high-density semiconductor memory, and more particularly...electrical isolation between discrete devices in non-volatile

memory.” Ex-1007 ¶31. Purayath specifically discloses that “word line air caps are formed to define word line air gaps between the layer stack rows,” wherein each layer stack row includes a charge storage region 466 and a control gate 452,” where “[c]ontrol gates 452 have been silicided to create a metal silicide end portion 453 for each control gate.” *Id.*, ¶¶82, 100, 103-04. Further, a dielectric “[l]iner [486] (e.g., oxide) is formed along the sidewalls 413 of the layer stack rows, over the upper surface of the control gates 452” and “a capping layer 488 is formed over the layer stack rows using a non-conformal deposition process.” *Id.*, ¶¶81, 83, Figs. 7S-7T. Murata discloses a structurally similar “semiconductor device...compris[ing]...a plurality of convex patterns formed over a main front surface of the semiconductor substrate so that each might have a floating gate and a control gate, a first insulating film formed so that an upper surface and a side surface of each of the convex patterns might be covered,...and a second insulating film that covers an upper surface and a side surface of the first insulating film so that a cavity between the adjacent convex patterns may be occluded.” Ex-1008, 2:29-41, Fig. 3. Murata explicitly discloses that “[c]ontrol gate CG is formed, for example of the laminated film of conductive layer CGa which consists of polycrystalline silicon of low resistance, and conductive layer CGb which consists of high melting point metal silicide films, such as tungsten silicide (WSix), etc. formed in the upper surface.” *Id.*, 6:4-8. Further, Murata discloses that a silicon oxide or silicon nitride film may be used for each of the

material of first insulating film 11 and second insulating film 12. *See id.*, 6:58-59, 7:7-8, 7:11-12.

141. A POSITA would have been motivated to implement Purayath's semiconductor memory device with Murata's specific materials because a POSITA would have recognized that tungsten is a common material used for word lines and silicon oxide and silicon nitride are common, interchangeable materials used as insulating and protective layers. For example, Kang explains—and a POSITA would have understood—that “[t]o enhance an operating speed of a semiconductor device, control gates are made of metallic substance, e.g., tungsten silicide” which has a “low sheet resistance” and “may help enhance a speed of a memory device.” Ex-1005 at 1:23-25, 1:33-35, 6:11-15, 2:57-58.

142. In this combination, Purayath's semiconductor memory device would have implemented the tungsten word line and silicon oxide and silicon nitride layers discussed in Murata. A POSITA would have had a reasonable expectation of success in achieving the objective of decreasing the deterioration of cell threshold voltage distribution, minimizing the parasitic capacitance, and enhancing speed and reliability by combining the teachings of Purayath and Murata with no change in their respective functions because both references solve these problems in similar and predictable ways. *See supra* §§V.C-V.D.

2. Claims 3, 17: wherein the word lines comprise tungsten.

143. As discussed above, Purayath discloses that “[a]n upper portion 453 of each control gate [452] is transformed into silicide,” as shown in Figure 7S. Ex-1007 ¶¶80, 104, 78-79, 87. Purayath similarly discloses, “[i]n one example, the control gate layer has a lower portion that is formed from polysilicon and an upper portion that is formed from metal.” *Id.*, ¶65.

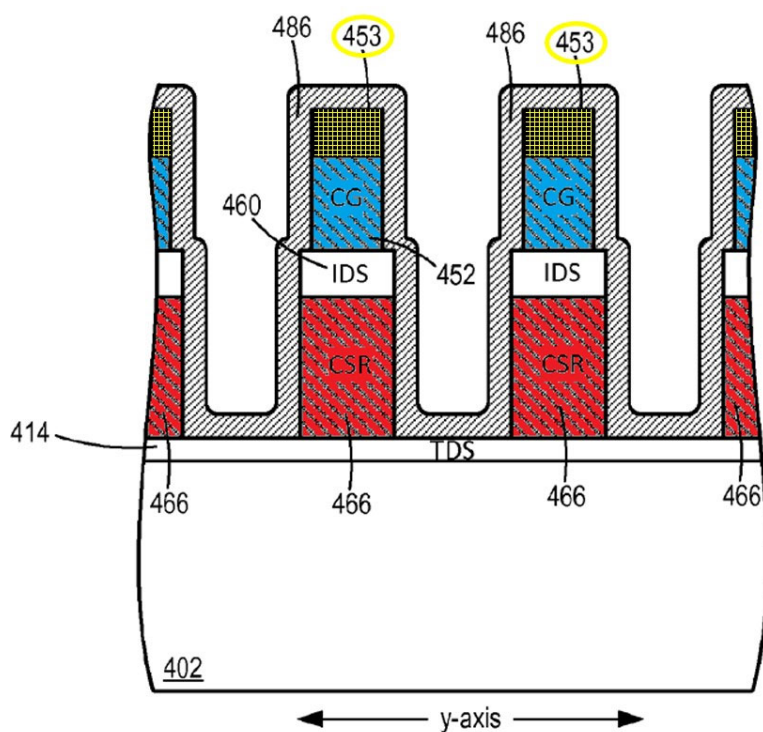


FIG. 7S

Id., Fig. 7S (annotated). For example, “[m]etals may include, but are not limited to, W, WSi_x or other similar low resistivity metals. Silicides may include, but are not limited to, NiSi, CoSi.” *Id.* Thus, a POSITA would have understood that the metal or silicided end portion 453 of a control gate may comprise a word line made from

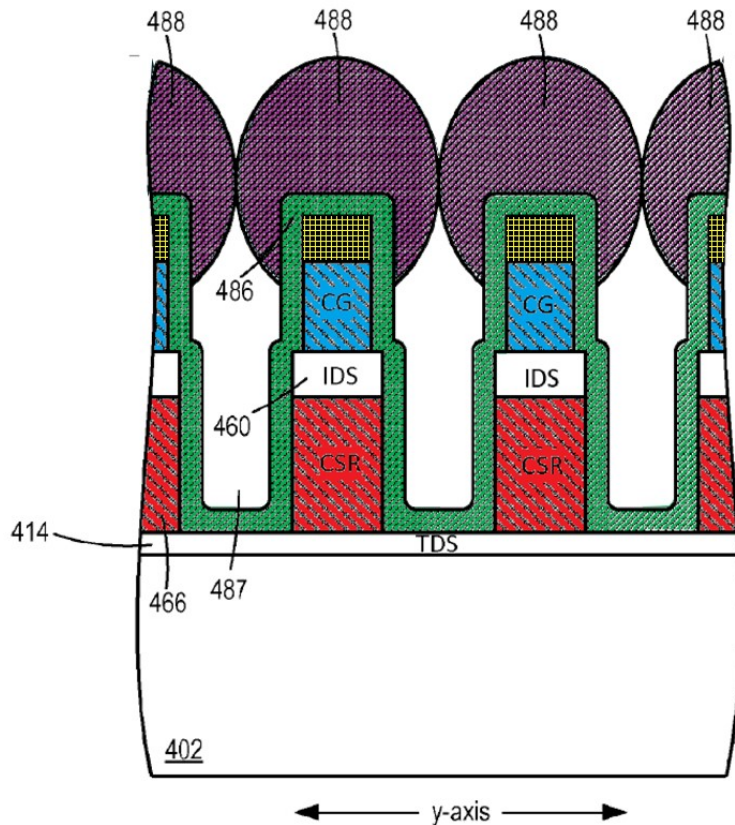
tungsten metal or tungsten silicide. Ex-1025 at 8-13; *see* Ex-1005 at 1:23-25, 1:33-35, 6:11-15, 2:57-58 (“To enhance an operating speed of a semiconductor device, control gates are made of metallic substance, e.g., tungsten silicide” which has a “low sheet resistance” and “may help enhance a speed of a memory device.”); *see supra* §VIII.C.

144. This limitation is also obvious over Purayath in view of Murata. Similar to Purayath, Murata discloses, “[c]ontrol gate CG is formed, for example of the laminated film of conductive layer CGa which consists of polycrystalline silicon of low resistance, and conductive layer CGb which consists of high melting point metal silicide films, such as tungsten silicide (WSix), etc. formed in the upper surface.” Ex-1008 at 6:4-8. Because a POSITA would have understood that tungsten and tungsten silicide made good choices for a conductive layer of a control gate, it would have been obvious to use tungsten metal or tungsten silicide as metal silicide end portions 453 for each control gate 452 in Purayath’s memory device. *See* Ex-1005 at 1:23-25, 1:33-35, 6:11-15, 2:57-58; *see also supra* §VIII.C.

3. Claim 7: wherein the first oxide regions and the second oxide regions comprise silicon oxide and the nitride regions comprise silicon nitride.

145. Purayath discloses that first and second oxide regions comprise silicon oxide. As discussed above, Purayath discloses, “a dielectric liner is formed along the sidewalls of the layer stack rows. FIG. 7T depicts “[I]ner [486] (e.g., **oxide**) [shown

in green]...formed along the sidewalls 413 of the layer stack rows, over the upper surface of the control gates 452, and over the exposed upper surface of the tunnel dielectric strips 414.” Ex-1007 ¶81 (emphasis added), Figs. 7S-7T.



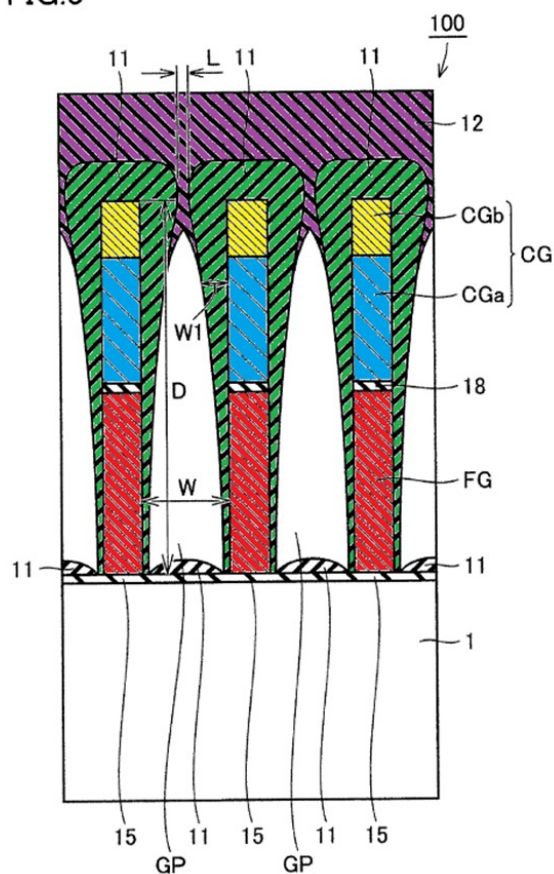
Id., Fig. 7T (annotated). Thus, a POSITA would have understood that liner 486 may be an oxide and cover the charge storage regions 466 and the sidewalls of the silicided end portion 453 of a control gate—i.e., word lines.

146. Further, Purayath discloses that the nitride regions comprise silicon nitride. Specifically, “a capping layer 488 [shown in purple] is formed over the layer stack rows using a non-conformal deposition process,” wherein “material 488 will

be deposited unequally at the upper portion of the layer stack rows.” *Id.*, ¶83. For example, “[m]aterial 488,” which may be “material such as nitrides,” “extends vertically toward the substrate surface along the liner 486 on a portion of vertical sidewalls 413 of the layer stack rows.” *Id.* Thus, a POSITA would have understood that material 488 may comprise nitrides and cover the oxide region covering the sidewalls of the silicided end portion 453 of a control gate—i.e., word lines.

147. Purayath in view of Murata also teaches first and second oxide regions comprising silicon oxide and the nitride regions comprising silicon nitride. Murata discloses a similar structure to Purayath’s, wherein “a plurality of convex patterns which have a layered product of floating gate FG, insulating film 18, and control gate CG...will be formed on semiconductor substrate 1” and in which “[f]irst insulating film 11 is formed so that the upper surface and the side surface of each convex pattern which were mentioned above may be covered,” and “[s]econd insulating film 12 that covers the upper surface and the side surface of first insulating film 11...so that cavity GP between the adjacent convex patterns mentioned above may be occluded.” *See* Ex-1008 at 6:43-7:6, Fig. 3.

FIG.3



Id., Fig. 3 (annotated). Murata discloses that “the first insulating film [11] consists of a silicon oxide film.” Ex-1008 at 4:4-9, 2:45-59, 6:58-59, 11:44-51. Indeed, Murata explains that “when the first insulating film is a silicon oxide film, it can perform dry etching easily in this case” as compared with using a nitride film. *Id.* at 4:7-9, 11:44-51. Murata also discloses that “a silicon nitride film [is] used for the material of second insulating film 12, for example.” *Id.* at 7:7-16. Further, as discussed previously, a POSITA would have found it obvious to use silicon oxide and silicon nitride for these layers because oxide and nitride are typical dielectric layers that are most frequently used in silicon semiconductor processes. Ex-1006

¶11. Indeed, Murata acknowledges that first and second insulating films can each easily be substituted as silicon oxide or silicon nitride. *See* Ex-1008 at 6:58-63, 7:7-16. Thus, a POSITA would have found it obvious in view of Purayath and Murata to use silicon oxide for Purayath's liner 486 and silicon nitride for capping layer 488.

XI. CONCLUSION

148. The unpatentability grounds presented above are reasonably likely to prevail, and IPR should be instituted for Claims 1-7, 13-14, 17-19 of the '314 Patent based on each of the grounds specified in this Petition.

Dated: May 30, 2025

Respectfully submitted,



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