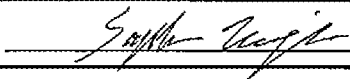


ABSTRACT

Non-volatile storage devices and methods for fabricating non-volatile storage device are described. Sidewalls of the memory cells and their associated word line may be covered with silicon oxide. Silicon nitride covers the silicon oxide adjacent to the word lines, which may provide protection for the word lines during fabrication. However, silicon nitride can trap charges, which can degrade operation if the trapped charges are near a charge trapping region of a memory cell. Thus, the silicon nitride does not cover the silicon oxide adjacent to charge storage regions of the memory cells, which can improve device operation. For example, memory cell current may be increased. Techniques for forming such a device are also disclosed. One aspect includes a method that uses a sacrificial material to control formation of a silicon nitride layer when forming a memory device.

**DECLARATION (37 CFR 1.63) FOR UTILITY OR DESIGN APPLICATION USING AN
APPLICATION DATA SHEET (37 CFR 1.76)**

Title of Invention	Non-Volatile Storage Having Oxide/Nitride Sidewall	
As the below named inventor, I hereby declare that: This declaration is directed to: ☒ The attached application, or ☐ United States application or PCT international application number _____ filed on _____ The above-identified application was made or authorized to be made by me. I believe that I am the original inventor or an original joint inventor of a claimed invention in the application. I hereby acknowledge that any willful false statement made in this declaration is punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both. WARNING: Petitioner/applicant is cautioned to avoid submitting personal information in documents filed in a patent application that may contribute to identity theft. Personal information such as social security numbers, bank account numbers, or credit card numbers (other than a check or credit card authorization form PTO-2038 submitted for payment purposes) is never required by the USPTO to support a petition or an application. If this type of personal information is included in documents submitted to the USPTO, petitioners/applicants should consider redacting such personal information from the documents before submitting them to the USPTO. Petitioner/applicant is advised that the record of a patent application is available to the public after publication of the application (unless a non-publication request in compliance with 37 CFR 1.213(a) is made in the application) or issuance of a patent. Furthermore, the record from an abandoned application may also be available to the public if the application is referenced in a published application or an issued patent (see 37 CFR 1.14). Checks and credit card authorization forms PTO-2038 submitted for payment purposes are not retained in the application file and therefore are not publicly available. LEGAL NAME OF INVENTOR Inventor: <u>Sayako Nagamine</u> Date (Optional): <u>Oct 9th 2014</u> Signature: <u></u> Note: An application data sheet (PTO/SB/14 or equivalent), including naming the entire inventive entity, must accompany this form or must have been previously filed. Use an additional PTO/AIA/01 form for each additional inventor.		

This collection of information is required by 35 U.S.C. 115 and 37 CFR 1.63. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 1 minute to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Electronic Patent Application Fee Transmittal				
Application Number:				
Filing Date:				
Title of Invention:		Non-Volatile Storage Having Oxide/Nitride Sidewall		
First Named Inventor/Applicant Name:		Takashi Kashimura		
Filer:		Ronald Mark Pomerence/Wendy Goy		
Attorney Docket Number:		SAND-01720US0		
Filed as Large Entity				
Utility under 35 USC 111(a) Filing Fees				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Utility application filing	1011	1	280	280
Utility Search Fee	1111	1	600	600
Utility Examination Fee	1311	1	720	720
Pages:				
Claims:				
Claims in Excess of 20	1202	1	80	80
Independent claims in excess of 3	1201	1	420	420
Miscellaneous-Filing:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Miscellaneous:				
Total in USD (\$)				2100

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	SAND-01720US0
		Application Number	
Title of Invention	Non-Volatile Storage Having Oxide/Nitride Sidewall		
The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76. This document may be completed electronically and submitted to the Office in electronic format using the Electronic Filing System (EFS) or the document may be printed and included in a paper filed application.			

Secrecy Order 37 CFR 5.2

☐	Portions or all of the application associated with this Application Data Sheet may fall under a Secrecy Order pursuant to 37 CFR 5.2 (Paper filers only. Applications that fall under Secrecy Order may not be filed electronically.)
--------------------------	---

Inventor Information:

Inventor 1					Remove
Legal Name					
Prefix	Given Name	Middle Name	Family Name	Suffix	
	Takashi		Kashimura		
Residence Information (Select One) ☐ US Residency ☒ Non US Residency ☐ Active US Military Service					
City	Yokkaichi-shi	Country of Residence i	JP		
Mailing Address of Inventor:					
Address 1	951 SanDisk Drive				
Address 2					
City	Milpitas	State/Province	CA		
Postal Code	95035	Country i	US		
Inventor 2					Remove
Legal Name					
Prefix	Given Name	Middle Name	Family Name	Suffix	
	Xiaolong		Hu		
Residence Information (Select One) ☐ US Residency ☒ Non US Residency ☐ Active US Military Service					
City	Yokkaichi-shi	Country of Residence i	JP		
Mailing Address of Inventor:					
Address 1	951 SanDisk Drive				
Address 2					
City	Milpitas	State/Province	CA		
Postal Code	95035	Country i	US		
Inventor 3					Remove
Legal Name					

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	SAND-01720US0
		Application Number	
Title of Invention	Non-Volatile Storage Having Oxide/Nitride Sidewall		

Prefix	Given Name	Middle Name	Family Name	Suffix
	Sayako		Nagamine	
Residence Information (Select One) ☐ US Residency ☒ Non US Residency ☐ Active US Military Service				
City	Yokkaichi-shi	Country of Residence i	JP	

Mailing Address of Inventor:

Address 1	951 SanDisk Drive			
Address 2				
City	Milpitas	State/Province	CA	
Postal Code	95035	Country i	US	

Inventor 4

Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Yusuke		Yoshida	
Residence Information (Select One) ☐ US Residency ☒ Non US Residency ☐ Active US Military Service				
City	Yokkaichi-shi	Country of Residence i	JP	

Mailing Address of Inventor:

Address 1	951 SanDisk Drive			
Address 2				
City	Milpitas	State/Province	CA	
Postal Code	95035	Country i	US	

Inventor 5

Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Hiroaki		Iuchi	
Residence Information (Select One) ☐ US Residency ☒ Non US Residency ☐ Active US Military Service				
City	Nagoya-shi	Country of Residence i	JP	

Mailing Address of Inventor:

Address 1	951 SanDisk Drive			
Address 2				
City	Milpitas	State/Province	CA	
Postal Code	95035	Country i	US	

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	SAND-01720US0
		Application Number	
Title of Invention	Non-Volatile Storage Having Oxide/Nitride Sidewall		

Inventor 6					Remove
Legal Name					
Prefix	Given Name	Middle Name	Family Name	Suffix	
	Akira		Nakada		
Residence Information (Select One) ☐ US Residency ☒ Non US Residency ☐ Active US Military Service					
City	Yokkaichi-shi	Country of Residence i	JP		
Mailing Address of Inventor:					
Address 1	951 SanDisk Drive				
Address 2					
City	Milpitas	State/Province	CA		
Postal Code	95035	Country i	US		

Inventor 7					Remove
Legal Name					
Prefix	Given Name	Middle Name	Family Name	Suffix	
	Kazutaka		Yoshizawa		
Residence Information (Select One) ☐ US Residency ☒ Non US Residency ☐ Active US Military Service					
City	Kuwana-shi	Country of Residence i	JP		
Mailing Address of Inventor:					
Address 1	951 SanDisk Drive				
Address 2					
City	Milpitas	State/Province	CA		
Postal Code	95035	Country i	US		

All Inventors Must Be Listed - Additional Inventor Information blocks may be generated within this form by selecting the **Add** button.

[Add](#)

Correspondence Information:

Enter either Customer Number or complete the Correspondence Information section below. For further information see 37 CFR 1.33(a).			
☐ An Address is being provided for the correspondence Information of this application.			
Customer Number	64948		
Email Address	rpomerenke@vierramagen.com	Add Email	Remove Email

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	SAND-01720US0
		Application Number	
Title of Invention	Non-Volatile Storage Having Oxide/Nitride Sidewall		

Application Information:

Title of the Invention	Non-Volatile Storage Having Oxide/Nitride Sidewall		
Attorney Docket Number	SAND-01720US0	Small Entity Status Claimed	☐
Application Type	Nonprovisional		
Subject Matter	Utility		
Total Number of Drawing Sheets (if any)	16	Suggested Figure for Publication (if any)	

Filing By Reference :

Only complete this section when filing an application by reference under 35 U.S.C. 111(c) and 37 CFR 1.57(a). Do not complete this section if application papers including a specification and any drawings are being filed. Any domestic benefit or foreign priority information must be provided in the appropriate section(s) below (i.e., "Domestic Benefit/National Stage Information" and "Foreign Priority Information").

For the purposes of a filing date under 37 CFR 1.53(b), the description and any drawings of the present application are replaced by this reference to the previously filed application, subject to conditions and requirements of 37 CFR 1.57(a).

Application number of the previously filed application	Filing date (YYYY-MM-DD)	Intellectual Property Authority or Country

Publication Information:

☐ Request Early Publication (Fee required at time of Request 37 CFR 1.219)
☐ Request Not to Publish. I hereby request that the attached application not be published under 35 U.S.C. 122(b) and certify that the invention disclosed in the attached application has not and will not be the subject of an application filed in another country, or under a multilateral international agreement, that requires publication at eighteen months after filing.

Representative Information:

Representative information should be provided for all practitioners having a power of attorney in the application. Providing this information in the Application Data Sheet does not constitute a power of attorney in the application (see 37 CFR 1.32). Either enter Customer Number or complete the Representative Name section below. If both sections are completed the customer Number will be used for the Representative Information during processing.			
Please Select One:	☒ Customer Number	☐ US Patent Practitioner	☐ Limited Recognition (37 CFR 11.9)
Customer Number	64948		

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	SAND-01720US0
		Application Number	
Title of Invention	Non-Volatile Storage Having Oxide/Nitride Sidewall		

Domestic Benefit/National Stage Information:

This section allows for the applicant to either claim benefit under 35 U.S.C. 119(e), 120, 121, or 365(c) or indicate National Stage entry from a PCT application. Providing this information in the application data sheet constitutes the specific reference required by 35 U.S.C. 119(e) or 120, and 37 CFR 1.78.

When referring to the current application, please leave the application number blank.

Prior Application Status		Remove	
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)
Additional Domestic Benefit/National Stage Data may be generated within this form by selecting the Add button.			Add

Foreign Priority Information:

This section allows for the applicant to claim priority to a foreign application. Providing this information in the application data sheet constitutes the claim for priority as required by 35 U.S.C. 119(b) and 37 CFR 1.55(d). When priority is claimed to a foreign application that is eligible for retrieval under the priority document exchange program (PDX) ⁱthe information will be used by the Office to automatically attempt retrieval pursuant to 37 CFR 1.55(h)(1) and (2). Under the PDX program, applicant bears the ultimate responsibility for ensuring that a copy of the foreign application is received by the Office from the participating foreign intellectual property office, or a certified copy of the foreign priority application is filed, within the time period specified in 37 CFR 1.55(g)(1).

Remove			
Application Number	Country ⁱ	Filing Date (YYYY-MM-DD)	Access Code ^j (if applicable)
Additional Foreign Priority Data may be generated within this form by selecting the Add button.			Add

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications

☐ This application (1) claims priority to or the benefit of an application filed before March 16, 2013 and (2) also contains, or contained at any time, a claim to a claimed invention that has an effective filing date on or after March 16, 2013. NOTE: By providing this statement under 37 CFR 1.55 or 1.78, this application, with a filing date on or after March 16, 2013, will be examined under the first inventor to file provisions of the AIA.

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	SAND-01720US0
		Application Number	
Title of Invention	Non-Volatile Storage Having Oxide/Nitride Sidewall		

Authorization to Permit Access:

☒ Authorization to Permit Access to the Instant Application by the Participating Offices

If checked, the undersigned hereby grants the USPTO authority to provide the European Patent Office (EPO), the Japan Patent Office (JPO), the Korean Intellectual Property Office (KIPO), the World Intellectual Property Office (WIPO), and any other intellectual property offices in which a foreign application claiming priority to the instant patent application is filed access to the instant patent application. See 37 CFR 1.14(c) and (h). This box should not be checked if the applicant does not wish the EPO, JPO, KIPO, WIPO, or other intellectual property office in which a foreign application claiming priority to the instant patent application is filed to have access to the instant patent application.

In accordance with 37 CFR 1.14(h)(3), access will be provided to a copy of the instant patent application with respect to: 1) the instant patent application-as-filed; 2) any foreign application to which the instant patent application claims priority under 35 U.S.C. 119(a)-(d) if a copy of the foreign application that satisfies the certified copy requirement of 37 CFR 1.55 has been filed in the instant patent application; and 3) any U.S. application-as-filed from which benefit is sought in the instant patent application.

In accordance with 37 CFR 1.14(c), access may be provided to information concerning the date of filing this Authorization.

Applicant Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.		
Applicant 1		Remove
If the applicant is the inventor (or the remaining joint inventor or inventors under 37 CFR 1.45), this section should not be completed. The information to be provided in this section is the name and address of the legal representative who is the applicant under 37 CFR 1.43; or the name and address of the assignee, person to whom the inventor is under an obligation to assign the invention, or person who otherwise shows sufficient proprietary interest in the matter who is the applicant under 37 CFR 1.46. If the applicant is an applicant under 37 CFR 1.46 (assignee, person to whom the inventor is obligated to assign, or person who otherwise shows sufficient proprietary interest) together with one or more joint inventors, then the joint inventor or inventors who are also the applicant should be identified in this section.		
		Clear
☒ Assignee	☐ Legal Representative under 35 U.S.C. 117	☐ Joint Inventor
☐ Person to whom the inventor is obligated to assign.	☐ Person who shows sufficient proprietary interest	
If applicant is the legal representative, indicate the authority to file the patent application, the inventor is:		
Name of the Deceased or Legally Incapacitated Inventor :		
If the Applicant is an Organization check here. ☒		
Organization Name	SanDisk Technologies Inc.	

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	SAND-01720US0
		Application Number	
Title of Invention	Non-Volatile Storage Having Oxide/Nitride Sidewall		

Mailing Address Information:			
Address 1	Two Legacy Town Center		
Address 2	6900 North Dallas Parkway		
City	Plano	State/Province	TX
Country i	US	Postal Code	75024
Phone Number		Fax Number	
Email Address			
Additional Applicant Data may be generated within this form by selecting the Add button. Add			

Assignee Information including Non-Applicant Assignee Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

Assignee 1				
Complete this section if assignee information, including non-applicant assignee information, is desired to be included on the patent application publication. An assignee-applicant identified in the "Applicant Information" section will appear on the patent application publication as an applicant. For an assignee-applicant, complete this section only if identification as an assignee is also desired on the patent application publication.				
				Remove
If the Assignee or Non-Applicant Assignee is an Organization check here.				☐
Prefix	Given Name	Middle Name	Family Name	Suffix
Mailing Address Information For Assignee including Non-Applicant Assignee:				
Address 1				
Address 2				
City		State/Province		
Country i		Postal Code		
Phone Number		Fax Number		
Email Address				
Additional Assignee or Non-Applicant Assignee Data may be generated within this form by selecting the Add button. Add				

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	SAND-01720US0
		Application Number	
Title of Invention	Non-Volatile Storage Having Oxide/Nitride Sidewall		

Signature:

Remove

NOTE: This form must be signed in accordance with 37 CFR 1.33. See 37 CFR 1.4 for signature requirements and certifications

Signature	/RonaldMPomerence#43009/		Date (YYYY-MM-DD)	2014-10-10	
First Name	Ronald	Last Name	Pomerence	Registration Number	43009

Additional Signature may be generated within this form by selecting the Add button.

Add

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Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these records.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

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**DECLARATION (37 CFR 1.63) FOR UTILITY OR DESIGN APPLICATION USING AN
APPLICATION DATA SHEET (37 CFR 1.76)**

Title of Invention	Non-Volatile Storage Having Oxide/Nitride Sidewall
As the below named inventor, I hereby declare that: This declaration is directed to: ☒ The attached application, or ☐ United States application or PCT international application number _____ filed on _____ The above-identified application was made or authorized to be made by me. I believe that I am the original inventor or an original joint inventor of a claimed invention in the application. I hereby acknowledge that any willful false statement made in this declaration is punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both. WARNING: Petitioner/applicant is cautioned to avoid submitting personal information in documents filed in a patent application that may contribute to identity theft. Personal information such as social security numbers, bank account numbers, or credit card numbers (other than a check or credit card authorization form PTO-2038 submitted for payment purposes) is never required by the USPTO to support a petition or an application. If this type of personal information is included in documents submitted to the USPTO, petitioners/applicants should consider redacting such personal information from the documents before submitting them to the USPTO. Petitioner/applicant is advised that the record of a patent application is available to the public after publication of the application (unless a non-publication request in compliance with 37 CFR 1.213(a) is made in the application) or issuance of a patent. Furthermore, the record from an abandoned application may also be available to the public if the application is referenced in a published application or an issued patent (see 37 CFR 1.14). Checks and credit card authorization forms PTO-2038 submitted for payment purposes are not retained in the application file and therefore are not publicly available. LEGAL NAME OF INVENTOR Inventor: Akira Nakada Date (Optional): 10/10/2014 Signature: Akira Nakada Note: An application data sheet (PTO/SB/14 or equivalent), including naming the entire inventive entity, must accompany this form or must have been previously filed. Use an additional PTO/AIA/D1 form for each additional inventor.	

This collection of information is required by 35 U.S.C. 115 and 37 CFR 1.63. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 1 minute to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

**DECLARATION (37 CFR 1.63) FOR UTILITY OR DESIGN APPLICATION USING AN
APPLICATION DATA SHEET (37 CFR 1.76)**

Title of Invention	Non-Volatile Storage Having Oxide/Nitride Sidewall
As the below named inventor, I hereby declare that: This declaration is directed to: ☒ The attached application, or ☐ United States application or PCT international application number _____ filed on _____ The above-identified application was made or authorized to be made by me. I believe that I am the original inventor or an original joint inventor of a claimed invention in the application. I hereby acknowledge that any willful false statement made in this declaration is punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both. WARNING: Petitioner/applicant is cautioned to avoid submitting personal information in documents filed in a patent application that may contribute to identity theft. Personal information such as social security numbers, bank account numbers, or credit card numbers (other than a check or credit card authorization form PTO-2038 submitted for payment purposes) is never required by the USPTO to support a petition or an application. If this type of personal information is included in documents submitted to the USPTO, petitioners/applicants should consider redacting such personal information from the documents before submitting them to the USPTO. Petitioner/applicant is advised that the record of a patent application is available to the public after publication of the application (unless a non-publication request in compliance with 37 CFR 1.213(a) is made in the application) or issuance of a patent. Furthermore, the record from an abandoned application may also be available to the public if the application is referenced in a published application or an issued patent (see 37 CFR 1.14). Checks and credit card authorization forms PTO-2038 submitted for payment purposes are not retained in the application file and therefore are not publicly available. LEGAL NAME OF INVENTOR Inventor: Xiaolong Hu Date (Optional): 10/9/2014 Signature: <u>Xiaolong Hu</u> Note: An application data sheet (PTO/SB/14 or equivalent), including naming the entire inventive entity, must accompany this form or must have been previously filed. Use an additional PTO/AIA/01 form for each additional inventor.	

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If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Electronic Acknowledgement Receipt

EFS ID:	20386090
Application Number:	14511834
International Application Number:	
Confirmation Number:	8559
Title of Invention:	Non-Volatile Storage Having Oxide/Nitride Sidewall
First Named Inventor/Applicant Name:	Takashi Kashimura
Customer Number:	64948
Filer:	Ronald Mark Pomerence
Filer Authorized By:	
Attorney Docket Number:	SAND-01720US0
Receipt Date:	10-OCT-2014
Filing Date:	
Time Stamp:	16:06:02
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
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Title of Invention	Non-Volatile Storage Having Oxide/Nitride Sidewall
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As the below named inventor, I hereby declare that:

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The above-identified application was made or authorized to be made by me.

I believe that I am the original inventor or an original joint inventor of a claimed invention in the application.

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LEGAL NAME OF INVENTOR

Inventor: Hiroaki Iuchi Date (Optional): 10/10/2014

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NON-VOLATILE STORAGE HAVING OXIDE/NITRIDE SIDEWALL

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BACKGROUND

[0001] This disclosure relates to non-volatile storage.

[0002] Semiconductor memory has become increasingly popular for use in various electronic devices. For example, non-volatile semiconductor memory is used in cellular telephones, digital cameras, personal digital assistants, mobile computing devices, non-mobile computing devices and other devices. Electrically Erasable Programmable Read Only Memory (EEPROM) and flash memory are among the most popular non-volatile semiconductor memories. With flash memory, also a type of EEPROM, the contents of the whole memory array, or of a portion of the memory, can be erased in one step, in contrast to traditional EEPROM.

BRIEF DESCRIPTION OF THE DRAWINGS

[0003] FIG. 1 is a top view of a NAND string.

[0004] FIG. 2A shows three NAND strings of a memory array having many more NAND strings.

[0005] FIG. 2B is a top view of a portion of an array of NAND flash memory cells.

[0006] FIG. 3 depicts a cross-sectional view of an NAND string formed on a substrate.

[0007] FIG. 4 illustrates a non-volatile storage device that may include one or more memory die or chips.

[0008] FIG. 5A is a diagram of a memory cell and portion of a word line of one embodiment.

[0009] FIG. 5B is a perspective view of stacks of memory cell lines of one embodiment.

[0010] FIG. 6 shows an example in which silicon nitride covers the sidewalls of the silicon oxide that are adjacent to the charge trapping region.

[0011] FIG. 7 is a flowchart of one embodiment of a process of fabricating memory cells.

[0012] FIGs. 8A-8F depict formation after various steps in the process of FIG. 7.

[0013] FIG. 9 is a flowchart of one embodiment of a process of fabricating a silicon nitride region.

[0014] FIGs. 10A-10F depict formation after various steps in the process of FIG. 9.

[0015] FIG. 11 depicts a schematic diagram of a portion of one embodiment of a memory array and associated row decoders.

DETAILED DESCRIPTION

[0016] Disclosed herein are non-volatile storage devices and methods for fabricating non-volatile storage devices. With ever decreasing size of features, combating breakdown voltage can be difficult. One type of voltage breakdown occurs between neighboring word lines. As the distance between word lines decreases, breakdown voltage may become a greater problem. Moreover, some conventional techniques for combating breakdown voltage lead to other problems, such as undesirably trapping charges in dielectric materials. These trapped charges can impair device performance. Further details are discussed below.

[0017] One embodiment includes a memory device having memory cells associated with a word line. Sidewalls of the memory cells and the word line may be covered with silicon oxide. Silicon nitride covers the silicon oxide adjacent to the word lines, which may provide protection for the word lines during fabrication. However, silicon nitride can trap charges, which can degrade operation if the trapped charges are near a charge trapping region of a memory cell. Thus, the silicon nitride does not cover the silicon oxide adjacent to charge storage regions of the memory cells, which can improve device operation. For example, memory cell current may be increased. Techniques for forming such a device are also disclosed.

[0018] One embodiment includes a method that uses a sacrificial material to control formation of a silicon nitride layer when forming a memory device. Lines of memory cell stacks are formed. Each stack has a word line and associated memory cells. Silicon oxide is formed on sidewalls of the lines of the memory cell stacks. A sacrificial material is formed between the lines of the memory cell stacks after forming the silicon oxide. The top of the sacrificial material is below the word lines but above charge storage regions of the memory cells. Thus, a portion of the silicon oxide remains exposed after forming the sacrificial material. Silicon nitride is formed on the sidewalls of the exposed silicon oxide. The sacrificial material is removed while leaving the silicon oxide on the sidewalls of the lines of memory cell stacks and the silicon nitride on the sidewalls of the silicon oxide adjacent to the

word lines. Air gaps are formed between neighboring pairs of the lines of memory cell stacks. Advantageously, the location of the silicon nitride can be accurately controlled. Also, the air gap can be formed in the space vacated by the sacrificial material. The air gap provides for good electrical isolation and high voltage breakdown between the word lines.

[0019] The techniques described herein are applicable to wide range of memory arrays having memory cells. The following is one example NAND architecture. However, technology disclosed herein is not limited to this example. One example of a flash memory system uses the NAND structure, which includes arranging multiple floating gate transistors in series between two select gate transistors. The memory cells and select gate transistors in series are referred to as a NAND string. FIG. 1 is a top view showing one NAND string. The NAND string depicted in FIG. 1 includes four memory cell transistors 100, 102, 104 and 106 in series and sandwiched between a first (or drain side) select gate 120 and a second (or source side) select gate 122. Select gate 120 connects the NAND string to a bit line via bit line contact 126. Select gate 122 connects the NAND string to source line 128. Select gate 120 is controlled by applying the appropriate voltages to select line SGD. Select gate 122 is controlled by applying the appropriate voltages to select line SGS. Each of the transistors 100, 102, 104 and 106 has a control gate and a floating gate. For example, transistor 100 has control gate 100CG and floating gate 100FG. Transistor 102 includes control gate 102CG and a floating gate 102FG. Transistor 104 includes control gate 104CG and floating gate 104FG. Transistor 106 includes a control gate 106CG and a floating gate 106FG. Control gate 100CG is connected to word line WL3, control gate 102CG is connected to word line WL2, control gate 104CG is connected to word line WL1, and control gate 106CG is connected to word line WL0.

[0020] A typical architecture for a flash memory system using a NAND structure will include many NAND strings. Each NAND string is connected to the source line by its source select gate controlled by select line SGS and connected to its associated bit line by its drain select gate controlled by select line SGD. Each bit line and the respective NAND string(s) that are connected to that bit line via a bit line contact comprise the columns of the array of memory

cells. Bit lines are shared with multiple NAND strings. Typically, the bit line runs on top of the NAND strings in a direction perpendicular to the word lines and is connected to one or more sense amplifiers.

[0021] FIG. 2A shows three NAND strings 202, 204 and 206 of a memory array having many more NAND strings. Each of the NAND strings of FIG. 2A includes two select transistors and four memory cells. For example, NAND string 202 includes select transistors 220 and 230, and memory cells 222, 224, 226 and 228. NAND string 204 includes select transistors 240 and 250, and memory cells 242, 244, 246 and 248. Each NAND string is connected to the source line by its select transistor (e.g. select transistor 230 and select transistor 250). A selection line SGS is used to control the source side select gates. The various NAND strings are connected to respective bit lines (not depicted in Figure 2A) by select transistors 220, 240, etc., which are controlled by select line SGD. In other embodiments, the select lines do not necessarily need to be in common. Word line WL3 is connected to the control gates for memory cell 222 and memory cell 242. Word line WL2 is connected to the control gates for memory cell 224, memory cell 244, and memory cell 252. Word line WL1 is connected to the control gates for memory cell 226 and memory cell 246. Word line WL0 is connected to the control gates for memory cell 228 and memory cell 248. As can be seen, each bit line and the respective NAND string comprise the columns of the array of memory cells. The word lines (WL3, WL2, WL1 and WL0) comprise the rows of the array.

[0022] Note that a NAND string can have fewer or more memory cells than depicted in FIG. 2A. For example, some NAND strings will include eight memory cells, 16 memory cells, 32 memory cells, 64 memory cells, 128 memory cells, etc. The discussion herein is not limited to any particular number of memory cells in a NAND string. Furthermore, a word line can have more or fewer memory cells than depicted in FIG. 2A. For example, a word line can include thousand or tens of thousands of memory cells. The discussion herein is not limited to any particular number of memory cells in a word line.

[0023] FIG. 2B is a top view of a portion of an array of NAND flash memory cells. The array includes NAND strings 300 and word lines 528. Shallow trench isolation (STI) structures 245 are depicted between the NAND strings 300. The STI structures 245 provide electrical isolation between adjacent NAND strings 300. In one embodiment, the STI structures 245 are formed from silicon oxide. In one embodiment, electrical isolation between adjacent NAND strings 300 is provided by the use of air gaps. These may be referred to a “bit line air gaps” due to their orientation relative to the direction of the bit lines (which may extend in the same direction as the NAND strings 300). A coordinate system is depicted showing: x or word line (WL) direction, y or bit line (BL) direction, and z-direction. It is not required that the word lines and bit lines are perpendicular to each other. Note that FIG. 2B does not show all of the other details of the flash memory cells.

[0024] Note that a NAND string can have fewer or more memory cells than depicted in FIGs. 2A and 2B. For example, some NAND strings will include eight memory cells, 16 memory cells, 32 memory cells, 64 memory cells, 128 memory cells, etc. The discussion herein is not limited to any particular number of memory cells in a NAND string. Furthermore, a word line can be associated with more or fewer memory cells than depicted in FIGs. 2A and 2B. For example, a word line can be associated with thousands or tens of thousands of memory cells. The discussion herein is not limited to any particular number of memory cells in a word line.

[0025] Each memory cell can store data (analog or digital). When storing one bit of digital data, the range of possible threshold voltages of the memory cell is divided into two ranges which are assigned logical data “1” and “0.” In one example of a NAND type flash memory, the threshold voltage is negative after the memory cell is erased, and defined as logic “1.” The threshold voltage after programming is positive and defined as logic “0.” When the threshold voltage is negative and a read is attempted by applying 0 volts to the control gate, the memory cell will turn on to indicate logic one is being stored. When the threshold voltage is positive and a read operation is attempted by applying 0 volts to the control gate, the memory cell will not turn on, which indicates that logic zero is stored.

[0026] In the case of storing multiple levels of data, the range of possible threshold voltages is divided into the number of levels of data. For example, if four levels of information is stored (two bits of data), there will be four threshold voltage ranges assigned to the data values "11", "10", "01", and "00." In one example of a NAND type memory, the threshold voltage after an erase operation is negative and defined as "11". Positive threshold voltages are used for the data states of "10", "01", and "00." If eight levels of information (or states) are stored (e.g. for three bits of data), there will be eight threshold voltage ranges assigned to the data values "000", "001", "010", "011", "100", "101", "110" and "111."

[0027] The specific relationship between the data programmed into the memory cell and the threshold voltage levels of the cell depends upon the data encoding scheme adopted for the cells. In one embodiment, data values are assigned to the threshold voltage ranges using a Gray code assignment so that if the threshold voltage of a floating gate erroneously shifts to its neighboring physical state, only one bit will be affected. In some embodiments, the data encoding scheme can be changed for different word lines, the data encoding scheme can be changed over time, or the data bits for random word lines may be inverted or otherwise randomized to reduce data pattern sensitivity and even wear on the memory cells.

[0028] The discussion herein can also apply to other types of flash memory in addition to NAND as well as other types of non-volatile memory. For example, NOR type flash memories may be used. Also, a so called TANOS structure (consisting of a stacked layer of TaN-Al₂O₃-SiN-SiO₂ on a silicon substrate), which is basically a memory cell using trapping of charge in a nitride layer (instead of a floating gate), can also be used. Another type of memory cell useful in flash EEPROM systems utilizes a non-conductive dielectric material in place of a conductive floating gate to store charge in a non-volatile manner. Such a cell is described in an article by Chan et al., "A True Single-Transistor Oxide-Nitride-Oxide EEPROM Device," IEEE Electron Device Letters, Vol. EDL-8, No. 3, March 1987, pp. 93-95. A triple layer dielectric formed of silicon oxide, silicon nitride and silicon oxide ("ONO") is sandwiched between a conductive control gate and a surface of a semi-conductive substrate above the memory cell channel. The cell is programmed by injecting electrons from the cell channel into the nitride, where they are

trapped and stored in a limited region. This stored charge then changes the threshold voltage of a portion of the channel of the cell in a manner that is detectable. The memory cell is erased by injecting hot holes into the nitride. See also Nozaki et al., "A 1-Mb EEPROM with MONOS Memory Cell for Semiconductor Disk Application," IEEE Journal of Solid-State Circuits, Vol. 26, No. 4, April 1991, pp. 497-501, which describes a similar memory cell in a split-gate configuration where a doped polysilicon gate extends over a portion of the memory cell channel to form a separate select transistor. Other types of memory devices can also be used.

[0029] FIG. 3 depicts a cross-sectional view of a NAND string formed on a substrate. The view is simplified and not to scale. The NAND string 300 includes a source-side select gate 306, a drain-side select gate 324, and eight storage elements 308, 310, 312, 314, 316, 318, 320 and 322, formed on a substrate 502. A number of source/drain regions, one example of which is source drain/region 330, are provided on either side of each storage element and the select gates 306 and 324. In one approach, the substrate 502 employs a triple-well technology which includes a p-well region 392 within an n-well region 394, which in turn is within a p-type substrate region 396. The NAND string and its non-volatile storage elements can be formed, at least in part, on the p-well region 392. A source supply line 304 with a potential of V_{SOURCE} is provided in addition to a bit line 326 with a potential of V_{BL} . Further, the control gate of a storage element may be provided as a portion of the word line. For example, WL0, WL1, WL2, WL3, WL4, WL5, WL6 and WL7 can extend via the control gates of storage elements 308, 310, 312, 314, 316, 318, 320 and 322, respectively.

[0030] Figure 4 illustrates a non-volatile storage device 410 that may include one or more memory die or chips 412. Memory die 412 includes an array (two-dimensional or three dimensional) of memory cells 400, control circuitry 420, and read/write circuits 430A and 430B. In one embodiment, access to the memory array 400 by the various peripheral circuits is implemented in a symmetric fashion, on opposite sides of the array, so that the densities of access lines and circuitry on each side are reduced by half. The read/write circuits 430A and 430B include multiple sense blocks 470 which allow a page of memory cells to be read or programmed in parallel. The memory array 400 is addressable by word lines via row decoders

440A and 440B and by bit lines via column decoders 442A and 442B. In a typical embodiment, a controller 444 is included in the same memory device 410 (e.g., a removable storage card or package) as the one or more memory die 412. Commands and data are transferred between the host and controller 444 via lines 432 and between the controller and the one or more memory die 412 via lines 434. One implementation can include multiple chips 412.

[0031] Control circuitry 420 cooperates with the read/write circuits 430A and 430B to perform memory operations on the memory array 400. The control circuitry 420 includes a state machine 422, an on-chip address decoder 424 and a power control module 426. The state machine 422 provides chip-level control of memory operations. The on-chip address decoder 424 provides an address interface to convert between the address that is used by the host or a memory controller to the hardware address used by the decoders 440A, 440B, 442A, and 442B. The power control module 426 controls the power and voltages supplied to the word lines and bit lines during memory operations. In one embodiment, power control module 426 includes one or more charge pumps that can create voltages larger than the supply voltage.

[0032] In one embodiment, one or any combination of control circuitry 420, power control circuit 426, decoder circuit 424, state machine circuit 422, decoder circuit 442A, decoder circuit 442B, decoder circuit 440A, decoder circuit 440B, read/write circuits 430A, read/write circuits 430B, and/or controller 444 can be referred to as one or more managing circuits.

[0033] Figure 5A is a diagram of a memory cell and portion of a word line of one embodiment. The memory cell is formed on substrate 502 and includes a charge storage region 522. In one embodiment, the charge storage region 522 is a conductive floating gate. For example, the floating gate can be formed from polysilicon. The memory cell also includes a control gate 526, which may be formed from polysilicon. There is a gate or tunnel oxide 520 between the charge storage region 522 and the substrate 502. The tunnel oxide 520 may be formed from silicon oxide. There is an intermediate dielectric 524 between the charge storage region 522 and the control gate 526. In one embodiment, the intermediate dielectric 524 is

formed from multiple layers, such as silicon oxide / silicon nitride / silicon oxide (“ONO”). Such an ONO layer could be referred to as an inter-gate or inter-poly dielectric (IPD). There is a word line 528 over the control gate 526. In one embodiment, the word line 528 is formed from tungsten. The word line 528 could be formed from a different metal. Region 530 comprises SiH₄ in one embodiment. Region 530 could be a different material. In one embodiment, region 530 is used as a mask when etching to form the word line 528 and layers below the word line.

[0034] It is not required that the charge storage region 522 be a conductive floating gate. In one embodiment, the charge storage region 522 includes a dielectric charge trapping region. For example, the dielectric charge trapping region can be formed from silicon nitride. The silicon nitride region may be part of a triple layer dielectric formed of silicon oxide, silicon nitride and silicon oxide (“ONO”) is sandwiched between the conductive control gate 526 and the substrate 502. In such a configuration, intermediate dielectric 524 may be a blocking layer, which could comprise silicon oxide, as one example. Region 520 may be a tunnel oxide of, for example, silicon oxide.

[0035] There is a silicon oxide layer 532 over sidewalls of the memory cell, as well as over the sidewalls of the word line 528. The sidewalls of the memory cell and word line that are covered by the silicon oxide layer 532 may have a surface in the x-y plane. This may be a conformal layer. As used herein, the term “covered” may include direct physical contact, but does not require direct physical contact. The silicon oxide layer 532 has a first region 532a adjacent to the charge storage region 522 and a second region 532b adjacent to the word line 528. These first and second regions 532a, 532b are roughly depicted by the circled areas. The silicon oxide layer 532 may be in direct contact with the sidewalls of the memory cell and word line. As used herein, the term “adjacent” does not require direct physical contact but could include direct physical contact.

[0036] Silicon nitride region 534 covers the sidewalls of the silicon oxide region 532 adjacent to the word line 528. Thus, the silicon nitride region 534 covers the second region

532b of silicon oxide. The silicon nitride region 534 may be in direct contact with silicon oxide region 532b, but direct contact is not required. The silicon nitride region 534 may provide protection for the word line 528 during memory cell formation. For example, tungsten from which the word line may be formed could be damaged during memory cell formation were it not for the protective silicon nitride 534.

[0037] However, silicon nitride region 534 does not cover the sidewalls of the silicon oxide region 532 that is adjacent to the charge trapping region 522. Thus, the silicon nitride region 534 does not cover the first region 532a of silicon oxide. In one embodiment, there is some form of electrical isolation next to region 532a. For example, the electrical isolation may include an air gap next to the first region 532a of silicon oxide 532. The electrical isolation may be in direct contact with the first region 532a of silicon oxide 532.

[0038] Figure 5B depicts a diagram of four memory cells and two word lines to help illustrate the location of the sidewalls of the memory cells and the word lines. The word line and its associated memory cells may be referred to herein as a “memory cell stack” 570. The memory cell stack 570 extends in the word line direction. Thus, each line of memory cell stacks 570 comprises memory cells and a word line. Only two memory cells are shown in each line, but there are typically many more.

[0039] Each memory cell includes tunnel oxide 520, charge storage region 522, intermediate dielectric 524, and control gate 526. The tunnel oxide 520 has sidewall 552, the charge storage region 522 has sidewall 554, the intermediate dielectric 524 has sidewall 556, the control gate 526 has sidewall 558, and the word line 528 has sidewall 560. Each of these sidewalls is a surface in the x-z plane, in this example. Although not labeled, there is another set of sidewalls in the x-z plane on the opposite side of these elements. To simplify Figure 5B, the silicon oxide layer 532 that was depicted in Figure 5A is not depicted. Likewise, the silicon nitride layer 534 that was depicted in Figure 5A is not depicted. The silicon oxide layer 532 may cover each of the sidewalls 552, 554, 556, 558, and 560.

[0040] Figure 5B shows spaces between the memory cells in both the bit line and the word line direction. In one embodiment, the spaces between the memory cell stacks 570 are filled with some form of electrical isolation. A portion of this electrical isolation is the silicon oxide layer 532. Another portion of the electrical isolation may be an air gap. An air gap could be any gasses. This may be referred to as a word line air gap.

[0041] In one embodiment, the spaces beneath the word lines in the word line direction are filled with some form of electrical isolation. Another option is for the control gates 526 to extend downward such that they are near some of the sidewalls of the charge storage regions 522. For example, the control gates 526 can be near the sidewalls of the charge storage regions 522 that have a surface in the y-z plane. Note that the intermediate dielectric 524 should also extend downward to provide a dielectric between the control gate 526 and the charge storage region 522. Figure 8B shows an example in which the control gates 826 extend downward between charge storage regions 822.

[0042] As mentioned above, the silicon nitride 534 can provide protection for the word line 528 during device fabrication. However, silicon nitride 534 can trap charges, which could impair device operation. This is depicted in Figure 6 for an example having memory cells having a tunnel oxide 620, charge storage region 622, intermediate dielectric 624, control gate 626, word line 628, and region 630. The silicon nitride 634 covers the sidewalls of the silicon oxide 632 that are adjacent to the charge storage regions 622. The trapped charges in the silicon nitride 634 can alter the neutral threshold voltage (V_{TH}) of the memory cell. The neutral V_{TH} refers to the V_{TH} when there is no net charge in the charge trapping region. For example, the trapped charges can impact the V_{TH} of the memory cell.

[0043] One possible explanation for the change in neutral V_{TH} is that positive charges may be generated at the edges of the charge storage region 622 near the negative charges in the silicon nitride 634 to cancel the electric field generated by the negative charges. These positive charges may, in effect, be trapped by the edges of the charge storage region 622. Even though there is not a change in net charge on the charge storage region 622 (assuming no leakage), the

change in distribution of the charges in the charge storage region 622 can impact the effective charge in the charge storage region 622. Thus, the neutral V_{TH} may change. For example, the neutral V_{TH} may increase. An increase in the neutral V_{TH} may be consistent with degradation of cell current. Thus, the charges trapped in the silicon nitride may lead to degradation in the cell current.

[0044] However, returning to the embodiment depicted in Figure 5A, there is no silicon nitride by the first region 532a of silicon oxide. Thus, the problem of trapped charges in a silicon nitride region by the charge storage region 522 is avoided.

[0045] It is possible that there may be some trapped charges in the silicon nitride region 534 that is adjacent to the word line 528. However, the word line 528 can be connected to peripheral circuitry such as word line drivers, etc. In other words, the word line 528 is not floating or otherwise surrounded by insulation. Thus, positive charges can be provided (or negative charges removed) by the peripheral circuitry to balance out any negative charges in the silicon nitride region 534 that is adjacent to the word line 528.

[0046] Figure 7 is a flowchart of one embodiment of a process of fabricating memory cells. The process can be used to form a memory cell and word line such as depicted in Figure 5A. Figures 8A-8F depict formation after various steps in the process.

[0047] In step 702, lines of memory cells are formed. In step 704, word lines that extend parallel to the lines of memory cells are formed. Figures 8A – 8C show one embodiment of formation of the lines of memory cells and the word lines. Figure 8A shows a perspective along line A-A' from Figure 2B. This may be referred to as a perspective along the NAND string. Figure 8B shows a perspective along line B-B' from Figure 2B. This may be referred to as a perspective along the word line. Both Figures are for the same step in fabrication.

[0001] Figure 8A is also the line C-C' in Figure 8B. Figure 8A shows a substrate 502, with various layers above that including, tunnel oxide layer 820, charge storage layer 822, intermediate dielectric layer 524, control gate layer 826, and word line layer 828. The tunnel

oxide layer 820 is a thin layer of oxide (e.g., SiO₂) grown in one embodiment, although different materials and processes can be used. Chemical vapor deposition (CVD) processes, metal organic CVD processes, physical vapor deposition (PVD) processes, atomic layer deposition (ALD) processes, thermal oxidation or other suitable techniques can be used. In one example, the tunnel oxide layer is formed to a thickness of about 8 nanometers (nm).

[0002] The charge storage layer 822 is a polysilicon floating gate layer in one embodiment. The vertical dimension (with respect to the substrate surface) or thickness of the charge storage layer can vary by embodiment. In one embodiment, the charge storage layer 822 has a vertical dimension of 10nm. In another embodiment, the charge storage layer has a vertical dimension of 70-80nm. The charge storage layer could have other vertical dimensions.

[0003] Dielectric charge storage materials, metal and non-metal nanostructures (e.g., carbon) can also be used for the charge storage layer 822. In one embodiment, the charge storage layer 822 is a metal layer forming a charge-trap type floating gate layer. A thin metal charge-trap type floating gate can reduce concerns with ballistic charge programming issues that may arise with conventional polysilicon floating gates. In one embodiment, a metal floating gate layer is formed to a thickness of between 5nm and 10nm. In another embodiment, metal thicknesses less than 5nm are used. Thicknesses greater than 10nm might also be used. In one embodiment, the layer of charge storage material comprises nano-particles. In one embodiment, the metal floating gate layer is a high work function metal. In one example, the metal is ruthenium. Other metals such as palladium, platinum, rhodium, titanium, tungsten, tantalum, nickel, cobalt, etc., and their alloys (e.g., TiN, WN, TaN, NiSi, CoSi, WSix) can be used.

[0004] The intermediate dielectric layer 822 is a triple layer of oxide, nitride and oxide (ONO) in one embodiment. In one embodiment, a high-K (dielectric constant) material is used for the intermediate dielectric to reduce or eliminate charge transfer through the intermediate layer while providing enhanced control gate to floating gate coupling.

[0048] Figure 8B shows four memory cells, each of which is on a different NAND string. Region 856 is electrical isolation that is provided between the NAND strings. In one embodiment, this is an air gap. Another option for the electrical isolation is shallow trench isolation (STI) structures, which could be formed from silicon oxide, tetra-ethyl ortho-silicate (TEOS), as examples.

[0049] Figure 8B shows that at this point in fabrication, charge storage layer 822 has been etched into lines that extend in the y- or bit line-direction in accordance with a first pattern. However, etching in the x- or word line-direction has not yet been done (as indicated by Figure 8A). The first pattern corresponds to intended columns of the memory array and may be repetitive in the row or direction of the x-axis. The pattern also corresponds to intended active areas of the substrate 502 which are separated by isolation regions 856. Spacer-assisted patterning, nano-imprint patterning, and other patterning techniques can also be used to form strips at reduced feature sizes. The pattern may define a first direction of etching to form columns of the memory array.

[0050] In this example, the control gate layer 826 extends downward such that it is not only above the charge storage layer 822, but is also adjacent to the sidewalls of the charge storage layer 822. This may improve capacitive coupling between the two regions, but is not a requirement. Also, although the control gate 826 is depicted as a contiguous region, this is not required. For example, each memory cell could have its own separate control gate. Figure 5B depicted an example in which each memory cell has its own separate control gate.

[0051] After etching in the y- or bit line direction, a second etch is performed in the x- or word line direction. This forms the word lines and finalizes the shapes of the memory cells. Figure 8C is a diagram after etching has been performed in the x- or word line-direction. Figure 8C is similar to 8A in that it shows perspective along line A-A' from Figure 2B. In one embodiment, region 550 is used as a mask to etch the word line layers and layers below that to form the structure of Figure 8C.

[0052] Thus, at this point in the fabrication process, lines of memory cell stacks 570 have been formed. A line of memory cell stacks 570 extends in the x- or word line-direction, as depicted in Figure 8B (or Figure 5B). The word lines 528 are parallel to the lines of memory cells. Each word line 528 is coupled to the control gates 526 of the memory cells. A word line 528 may be in direct contact with a control gate 526. The structures in Figure 8C may be referred to as “memory cell stacks”. A memory cell stack may include a line of memory cells and a word line. Note that the structures in Figure 8C may be similar to the structures of Figure 5B.

[0053] In step 706, oxide is formed that covers the sidewalls 554 of the charge storage region and the sidewalls 560 of the word lines. This oxide may cover other sidewalls such as sidewalls 552, 558, 558 of the tunnel oxide 520, intermediate dielectric 524 and control gate 526. In one embodiment, the oxide formed in step 706 is silicon oxide. Figure 8D shows results after one embodiment of step 706, with oxide (e.g., silicon oxide) covering the sidewalls of the memory cell stacks. Region 532a of the oxide 532 covers sidewalls of the charge storage region 522, and region 532b of oxide 532 covers sidewalls of the word lines 528. The oxide 532 may cover other sidewalls such as sidewalls of the tunnel oxide 520, intermediate dielectric 524 and control gate 526. The oxide 532 may also cover a portion of the substrate 502, such as over the source/drain (S/D) regions 827.

[0054] The oxide 532 may be provided using different approaches, including oxidizing the sidewalls, depositing an oxide on the sidewalls, or a combination of these two approaches. For sidewall oxidation, the device may be placed in a furnace at a high temperature (e.g., over 1000 degrees Celsius) and with some fractional percentage of ambient oxygen gas, so that the exposed surfaces oxidize. An alternative to high temperature oxide growth is low temperature (e.g., 400 degrees Celsius) oxide growth in high density Krypton plasma.

[0055] In step 708, nitride is formed by the sidewalls 566 of the word lines 528, but not by the sidewalls 554 of the charge storage regions 552. In one embodiment, this is silicon nitride. In one embodiment, the silicon nitride is formed using low pressure chemical vapor deposition

(LPCVD) technology. In one embodiment, the silicon nitride is formed using plasma-enhanced chemical vapor deposition (PECVD) technology.

[0056] Figure 8E shows results after one embodiment of step 708, with nitride 534 (e.g., silicon nitride) covering the sidewalls of the oxide by the word lines 528. However, the nitride 534 does not cover the sidewalls of the oxide 532 by the charge storage region 522. For example, region 532a of silicon oxide is not covered by the nitride 534. Thus, region 532a of silicon oxide is exposed at this point.

[0057] In one embodiment, silicon nitride 534 is formed by depositing it with poor step coverage. For example, by deliberately having poor step coverage, regions 532b adjacent to the sidewalls of the word lines 528 are covered by the nitride. However, regions 532a of the oxide that is adjacent to the charge storage regions 522 are not covered by the nitride. This provides for the structure depicted in Figure 8E, which shows the nitride 534 covering the silicon oxide 532 by the word line 528. Also, source/drain (S/D) regions 527 have been formed in the substrate 502 by implanting a suitable dopant.

[0058] In step 710, electrical isolation is formed between the word lines and memory cells. In one embodiment, step 710 forms electrical isolation regions other than silicon nitride adjacent to the oxide regions 532a that cover the sidewalls of the charge storage regions 522. An electrical isolation region may include an air gap and possibly a solid material in contact with the silicon oxide 532.

[0059] Thus, step 710 may include forming air gaps between pairs of neighboring word lines. These air gaps may be adjacent to the region 532a of the oxide 532 that is by the charge storage regions 522. Figure 8F shows results after one embodiment of step 710, showing air gaps 844 between pairs of adjacent word lines 528. Step 710 may include forming a capping layer 854 over the word lines 528. In one embodiment, capping layer is silicon oxide. Capping layer 854 may be formed using a plasma SiH₄ process, as one example. Gases such as air and process gases fill the space between the memory cell stacks 570, resulting in the air gaps.

[0060] The air gap 844 is present adjacent to the region 532a of the oxide that itself is adjacent to the charge storage region 522. The air gap 844 may be in direct contact with region 532a of the silicon oxide 532. However, there could be an insulator other than silicon nitride in direct contact with region 532a. For example, there might be a thin layer of an insulator other than silicon nitride in direct contact with region 532a. Thus, it is not required that the air gap 844 occupy the entire space between the memory cells stacks. These air gaps 844 may be referred to as “word line air gaps” due to their orientation being parallel with respect to the word lines.

[0061] Figure 9 is a flowchart of one embodiment of a process of fabricating a silicon nitride region 534. This process is one embodiment of step 708 from Figure 7. Figures 10A-10F show results during one embodiment of this process. In step 902, sacrificial material is formed between lines of memory cells. Prior to step 902, a structure similar to the one depicted in Figure 8D may be formed.

[0062] Figure 10A depicts results after one embodiment of step 902, showing sacrificial material 1002 filled in between the memory cell stacks 570 (which at this point have been covered with silicon oxide 532). In one embodiment, the sacrificial materials is a flowable CVD film. This film can be formed using a high-density plasma CVD system, a plasma enhanced CVD system, and/or a sub-atmospheric CVD system, among other systems. Examples of CVD systems capable of forming a flowable or flow-like layer include the ULTIMA HDP CVD[®] system and ETERNA CVD[®] on the PRODUCER[®] system, both available from Applied Materials, Inc., of Santa Clara, California. Other CVD systems from other manufacturers may also be used.

[0063] In one embodiment, forming the sacrificial material 1002 comprises depositing silicon, nitrogen, and hydrogen. In one embodiment, the sacrificial material 1002 is a material that could be cured by annealing in an oxygen environment to form silicon oxide. However, annealing in an oxygen environment is not performed in one embodiment. Thus, the sacrificial material 1002 is not converted to silicon oxide, in one embodiment.

[0064] The sacrificial material 1002 has a high etch selectivity with respect to silicon oxide in one embodiment. Thus, the sacrificial material 1002 has a high etch selectivity with respect to the silicon oxide 532, in one embodiment. As one example, the etch selectively could be about 10:1, but this is just one example. The sacrificial material 1002 may also have a high etch selectivity with respect to silicon nitride (e.g., silicon nitride 534) in one embodiment.

[0065] In step 904, the sacrificial material 1002 is etched back to a level that at the bottom of or just below the word lines 528. Figure 10B shows results after one embodiment of step 904. The top surface of the sacrificial material 1002 is below the word lines 528. However, the top surface of the sacrificial material 1002 is above the charge storage regions 522. Stated another way, the sacrificial material 1002 covers the sidewalls of the region 532a of the silicon oxide where the silicon oxide itself covers the sidewalls of the charge storage regions 522. However, the sacrificial material 1002 does not cover the sidewalls of the region 532b of the silicon oxide where the silicon oxide itself covers the sidewalls of the word lines 528.

[0066] In step 906, silicon nitride is formed over the exposed silicon oxide. In one embodiment, the silicon nitride is formed using low pressure chemical vapor deposition (LPCVD) technology. In one embodiment, the silicon nitride is formed using plasma-enhanced chemical vapor deposition (PECVD) technology.

[0067] Figure 10C depicts results after one embodiment, showing silicon nitride 1034. The silicon nitride 1034 may be a conformal layer over the exposed silicon oxide 532. The silicon nitride 1034 covers the sidewalls of the regions 532b of the silicon oxide 532 that itself covers the sidewalls of the word lines 528. At this point in the fabrication, there is also some silicon nitride 1034 over the top surface of the sacrificial material 1002. Also, there is also some silicon nitride 1034 over the tops of the memory cell stacks.

[0068] In step 908, the silicon nitride 1034 is etched back. Figure 10D depicts results after one embodiment of step 908. The silicon nitride 534 may now be described as being sidewall spacers. The portions of the silicon nitride that were above the memory cell stacks 570 has

been removed, as well as most of the portions of the silicon nitride 1034 that was over the top surface of the sacrificial material 1002.

[0069] In step 910, the sacrificial material is removed. Figure 10E depicts results after step 910, showing that the sacrificial material is now removed. This step may involve performing a selective etch that etches the sacrificial material but not the silicon oxide 532. Likewise, the silicon nitride 534 is not removed, in one embodiment. Source/drain (S/D) regions 527 have also been formed by implanting a suitable dopant. The S/D regions 527 could be formed at a different point in the process.

[0070] In step 912, air gaps are formed between pairs of neighboring lines of memory cells. Figure 10F depicts results after step 912. A layer of, for example, SiO₂ has been formed as a capping layer 854 over the memory cell stacks. In one embodiment, an SiH₄ plasma process is used to form the capping layer 854. This results in formation of air gaps 844 between the word lines 528. A portion of the air gap 844 is adjacent to the region 532a of the silicon oxide 532 that is adjacent to the charge storage region 522. The air gap 844 may be in direct contact with region 532a of the silicon oxide 532. However, there could be a solid material other than silicon nitride in direct contact with region 532a. For example, there might be a thin layer of an insulator other than silicon nitride in direct contact with region 532a. Thus, it is not required that the air gap 844 occupy the entire space between the memory cells stacks.

[0071] Figure 11 is a diagram of one embodiment of word lines 528 coupled to peripheral circuitry 240A. Because the word lines 528 are coupled to the peripheral circuitry 240A, the peripheral circuitry can provide or remove charges to the portion of the word line that is adjacent to the silicon nitride.

[0072] Figure 11 provides more details of one embodiment of the memory array 400 and associated row decoders 440A of Figure 4. The memory array has blocks 1102(0) - 1102(n). Two blocks are depicted in Figure 11, although there typically may be many more blocks 1102. The word lines (WL0 ... WLn) in a block 1102 are modeled as having some resistance and

some capacitance. The row decoders 440A include a block select transistor connected 1104 to each word line. The voltage VreadH is applied to each block select transistor 1104 in block 1102(n) to select that block 1102(n). The voltage Vss is applied to each block select transistor 104 in other blocks (e.g., block 1102(0)), such that that other blocks are un-selected. Typically, there is one selected block and many unselected blocks. There may be one word line voltage transistor 1106(0) - 1106(n) coupled to each word line. For example, transistor 106(0) is coupled to WL0 of each block 1102 through one of the word line select transistors 1104. Likewise, transistor 106(n) is coupled to WLn of each block 1102 through one of the word line select transistors 1104. Note that a given word line voltage transistor 1106 may be shared by different blocks. For example, if there are 64 word lines per block, there may be 64 word line voltage transistors 1106.

[0073] A reference voltage (Vcgrv) is applied to word line voltage transistor 1106(n) in order to apply Vcgrv to the selected word line (WLn) of the selected block 1102(n). A read pass voltage (Vread) is applied to word line voltage transistor 1106(0) in order to apply Vread to the un-selected word line (WL0) of the selected block 1102(n). The voltage Vread may also be applied to other word line voltage transistors (not depicted in Figure 11) in order to apply Vread to other un-selected word lines of the selected block 1102(n). Because Vss is applied to the block select transistors 1104 in the non-selected blocks, the voltages Vcgrv and Vread do not pass to the word lines in the un-selected blocks. Note that other configurations could be used to provide the voltages to the word lines.

[0074] One embodiment disclosed herein includes a method of forming a memory device comprising the following. A plurality of lines of memory cells are formed. Individual memory cells have a charge storage region and a control gate. The charge storage regions each have sidewalls. A plurality of word lines are formed parallel to the lines of memory cells. Each word line is formed on the control gates of the memory cells in one of the lines. The word lines each have sidewalls. Oxide is formed that covers the sidewalls of the charge storage regions of the memory cells and that covers the sidewalls of the word lines. A nitride region is

formed that is adjacent to the oxide that covers the sidewalls of the word lines but is not adjacent to the oxide that covers the sidewalls of the charge storage regions.

[0075] In one embodiment, the method of the previous paragraph also includes forming air gaps between adjacent pairs of the plurality of word lines. A portion of the air gaps is adjacent to the oxide that covers the sidewalls of the charge storage regions.

[0076] One embodiment disclosed herein includes a memory device comprising a plurality of lines of memory cells and a plurality of word lines each having sidewalls. The memory cells comprise a charge storage region having sidewalls and a control gate. Each of the word lines is associated with a line of the memory cells. Each of the word lines is coupled to the control gates of the memory cells with which it is associated. The memory device also includes first oxide regions that cover the sidewalls of the charge storage regions and second oxide regions that cover the sidewalls of the word lines. The memory device also includes nitride regions that cover the second oxide regions. The memory device also includes electrical isolation regions other than silicon nitride adjacent to the second oxide regions that cover the sidewalls of the charge storage regions.

[0077] In one embodiment, the electrical isolation regions includes air gaps. Each air gap is between a neighboring pair of the plurality of word lines. The air gaps are adjacent to second oxide regions.

[0078] One embodiment includes a method of forming a memory array that comprises the following. Lines of memory cell stacks are formed. Each line comprises a plurality of memory cells and a tungsten word line. Individual memory cells have a charge storage region. The lines of memory cell stacks have sidewalls. Silicon oxide is formed on the sidewalls of the lines of memory cell stacks. The silicon oxide has sidewalls. A sacrificial material is formed between the lines of memory cell stacks after forming the silicon oxide. The sacrificial material has a top surface that is below the word lines but above the charge storage regions. The sacrificial material has an etch selectively with respect to the silicon oxide. A portion of

the silicon oxide remains exposed after forming the sacrificial material. Silicon nitride is formed on the sidewalls of the exposed silicon oxide. The sacrificial material is removed while leaving the silicon oxide on the sidewalls of the lines of memory cell stacks and the silicon nitride on the sidewalls of the silicon oxide adjacent to the word lines. Air gaps are formed between neighboring pairs of the lines of memory cell stacks.

[0079] One embodiment includes a memory device comprising a plurality of lines of memory cell stacks. Each of the lines comprises a plurality of memory cells and a tungsten word line. Individual memory cells have a charge storage region. The lines of memory cell stacks have sidewalls. The device further includes silicon oxide that covers the sidewalls of the memory cell stacks, and silicon nitride that covers portions of the silicon oxide that are adjacent to the tungsten word lines. The device further includes word line air gaps between neighboring pairs of the plurality of lines of memory cell stacks. The word line air gaps are adjacent to portions of the silicon oxide that is adjacent to the charge storage regions.

[0080] Herein, numerous examples of have been presented. However, it will be understood that other semiconductors might be used. The various process flows have the order of steps presented for convenience of discussion. However, it will be appreciated that the steps can be performed in a different order. The flowcharts do not describe all implant steps, forming contacts to bit lines and source lines, metallizations, forming vias, and passivation, as well as other portions of the manufacturing process known in the art. There are many ways to manufacture memory according to embodiments and, thus, the inventors contemplate that various methods other than that described can be used. For example, the charge trapping regions can be formed to have many different shapes.

[0081] The foregoing detailed description of embodiments has been presented for purposes of illustration and description. It is not intended to be exhaustive or to limit embodiments to the precise form disclosed. Many modifications and variations are possible in light of the above teaching. The described embodiments were chosen in order to best explain the principles and practical applications, to thereby enable others skilled in the art to best utilize the

various embodiments and with various modifications as are suited to the particular use contemplated. It is intended that the scope be defined by the claims appended hereto.

Fig. 1

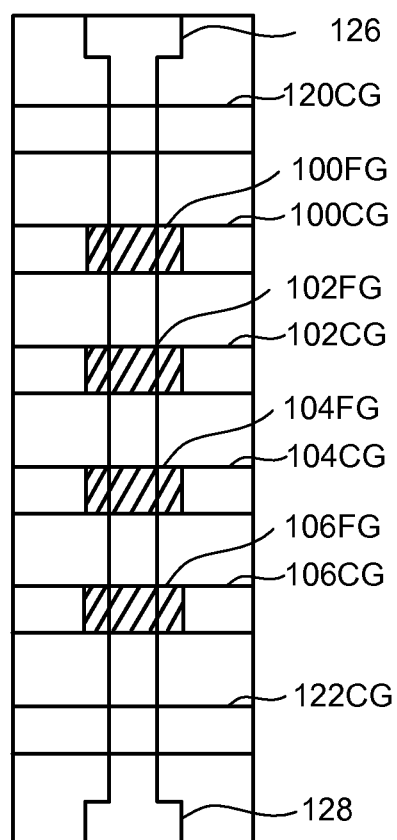


Fig. 2A

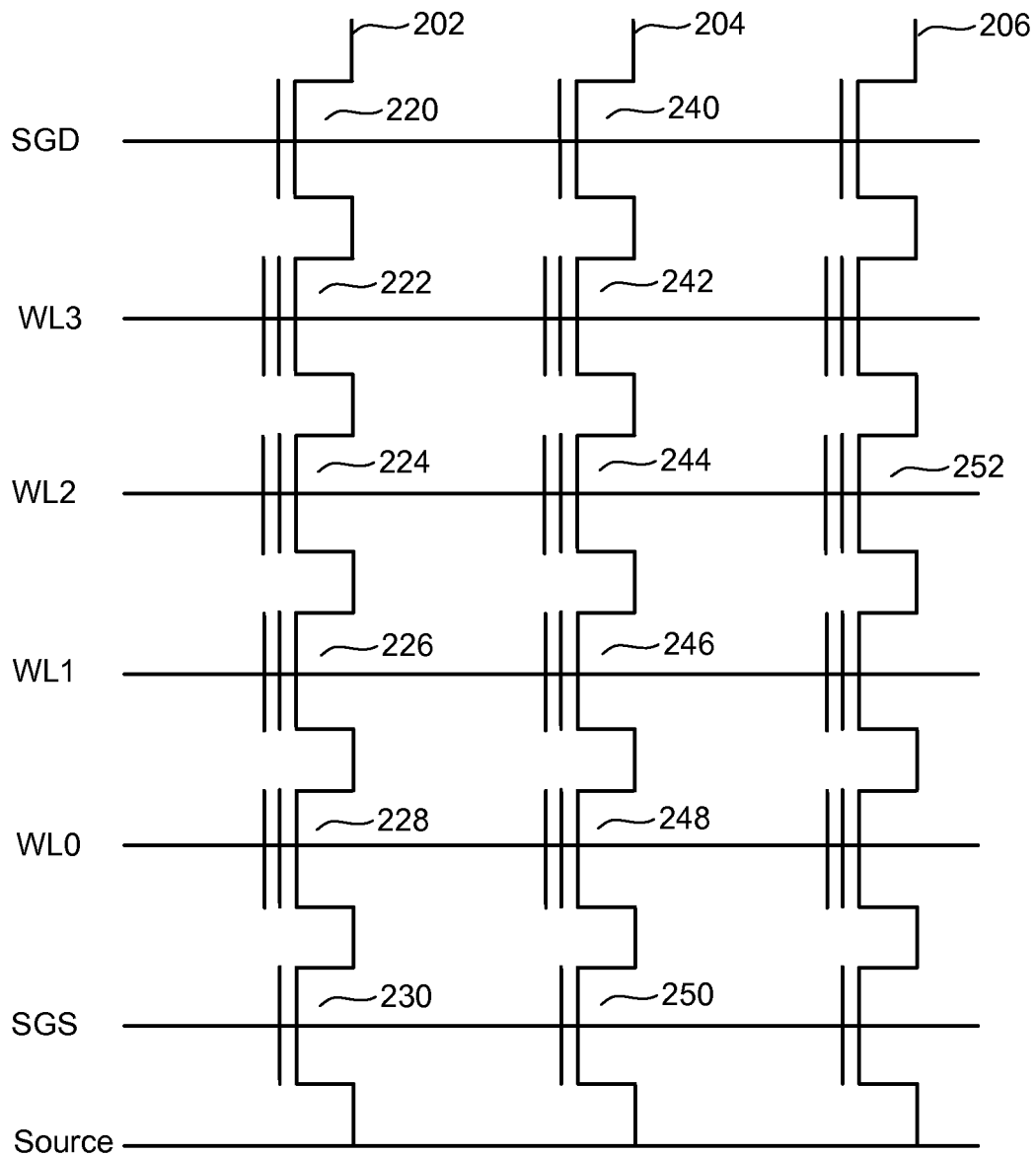
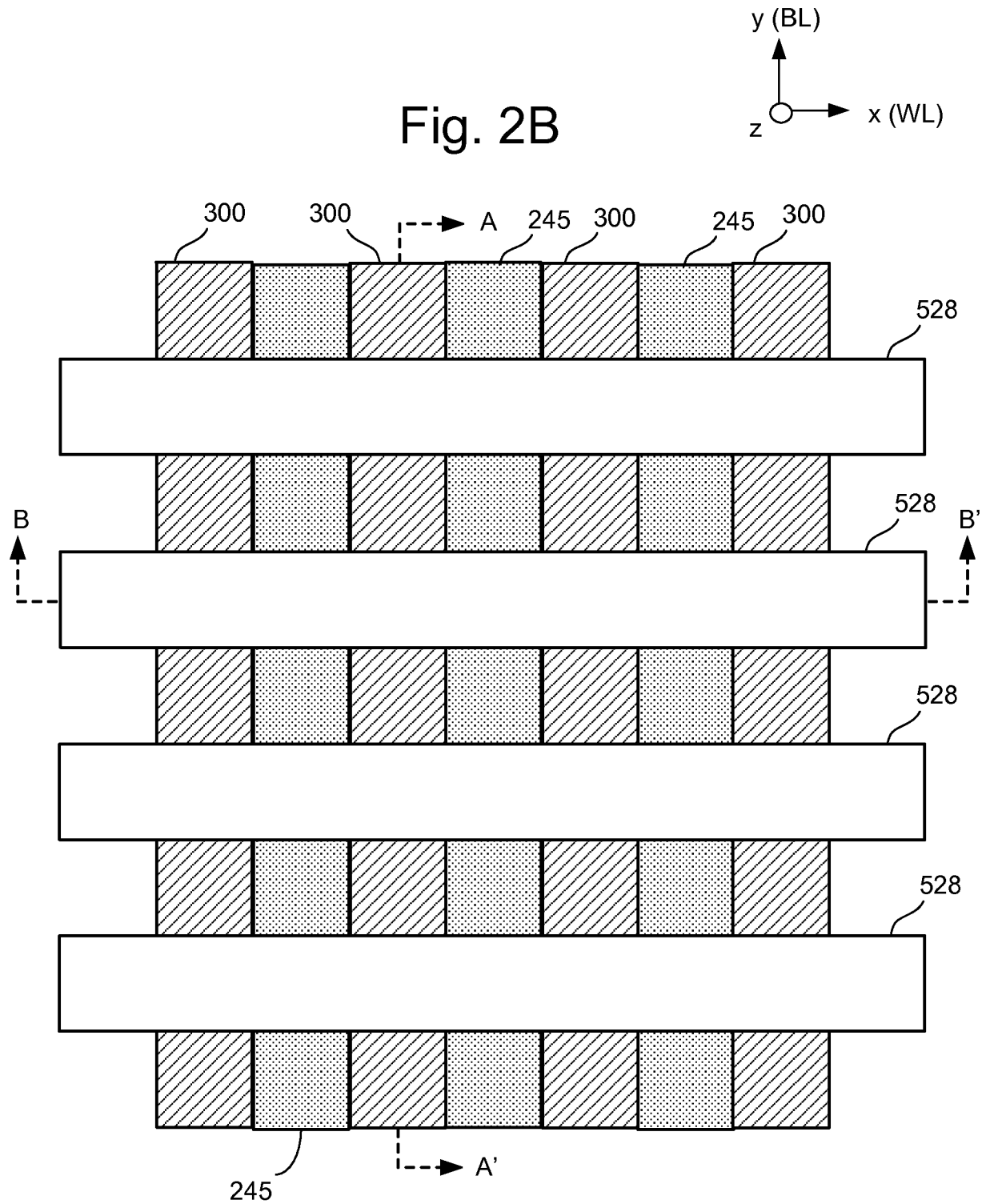


Fig. 2B



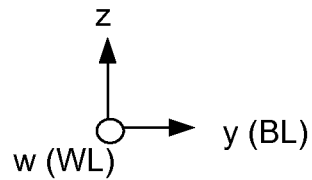
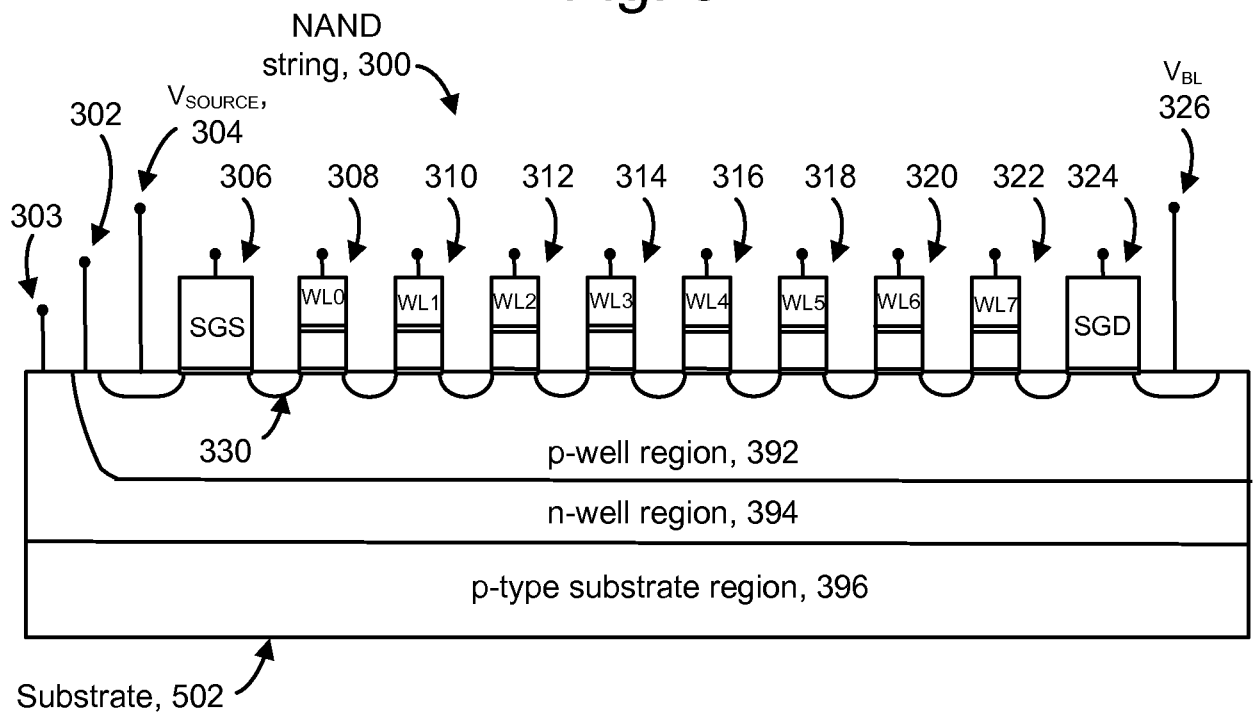


Fig. 3



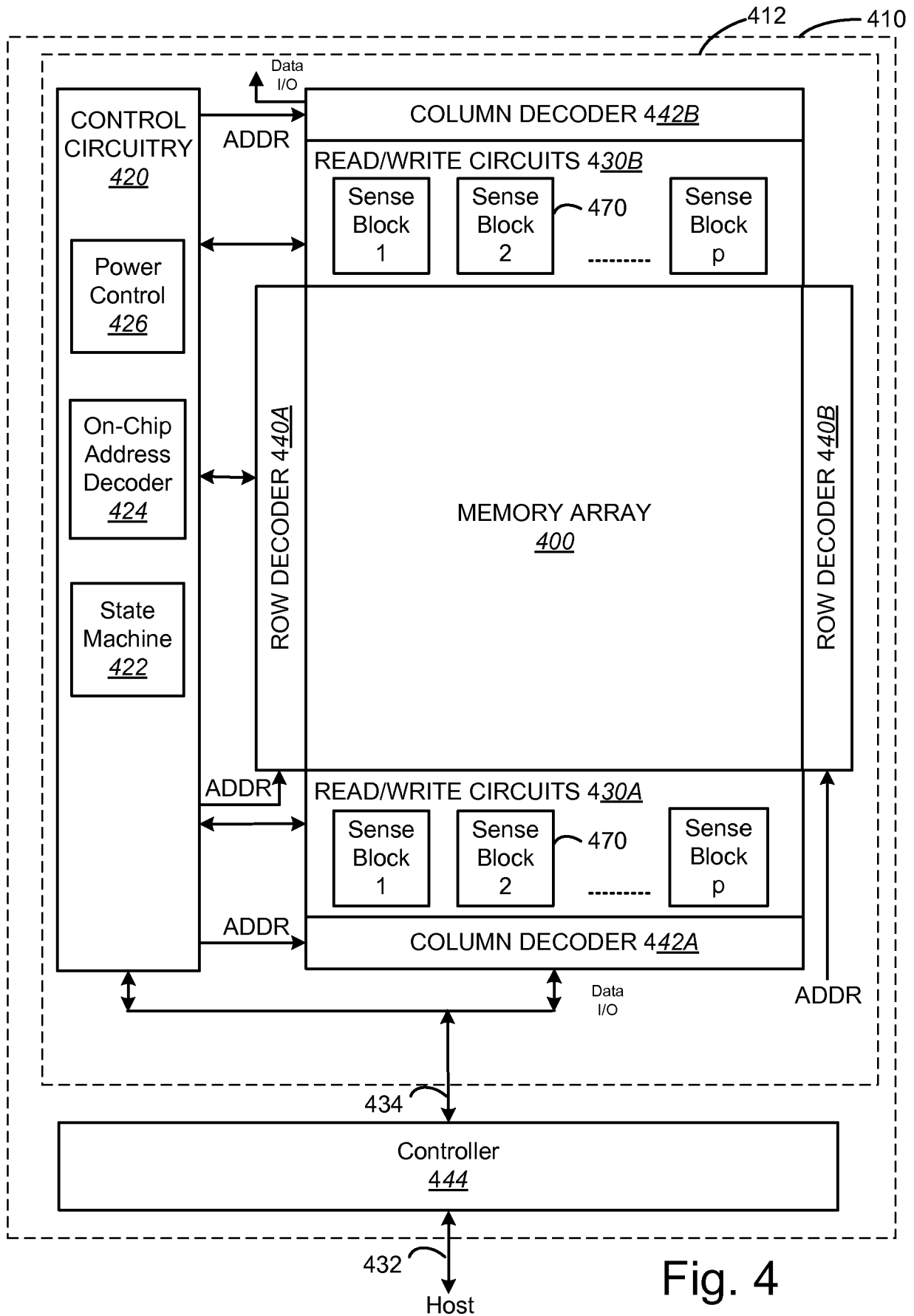


Fig. 4

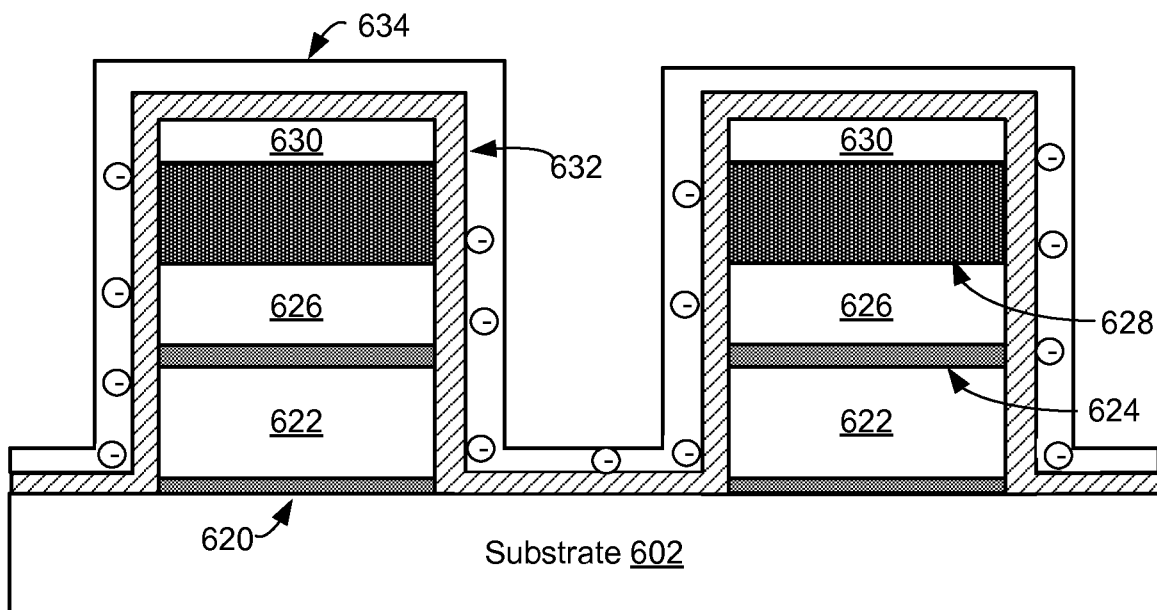
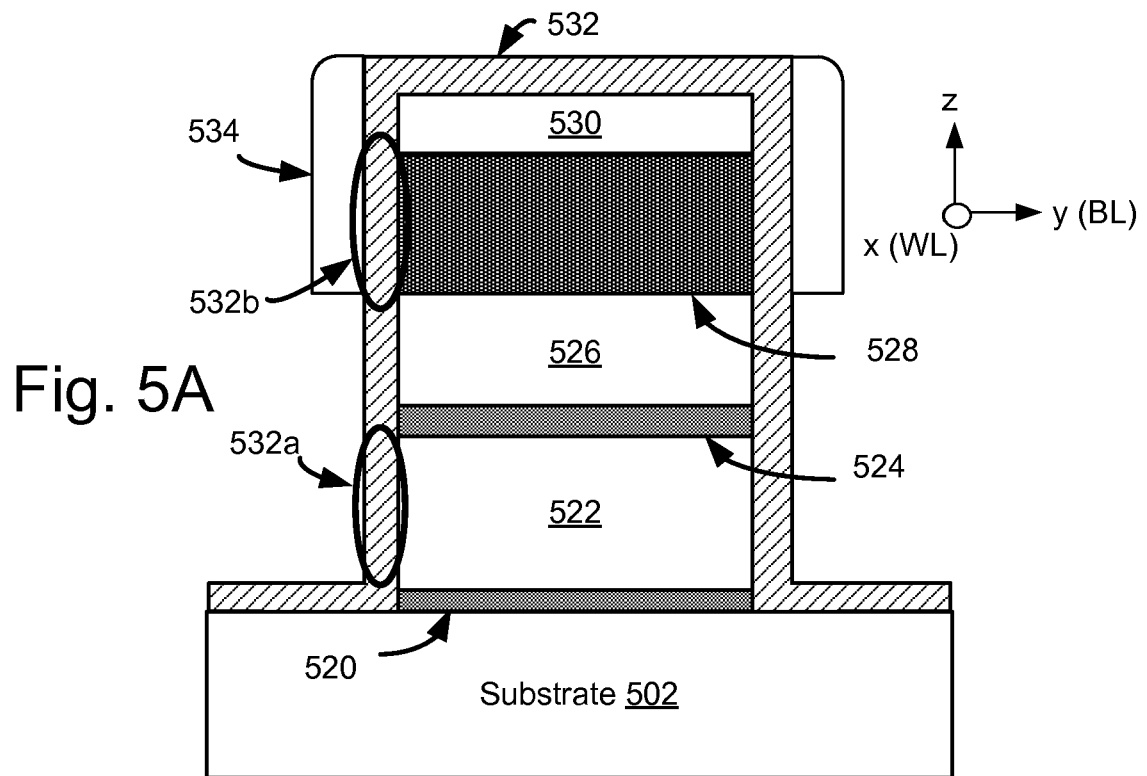


Fig. 6

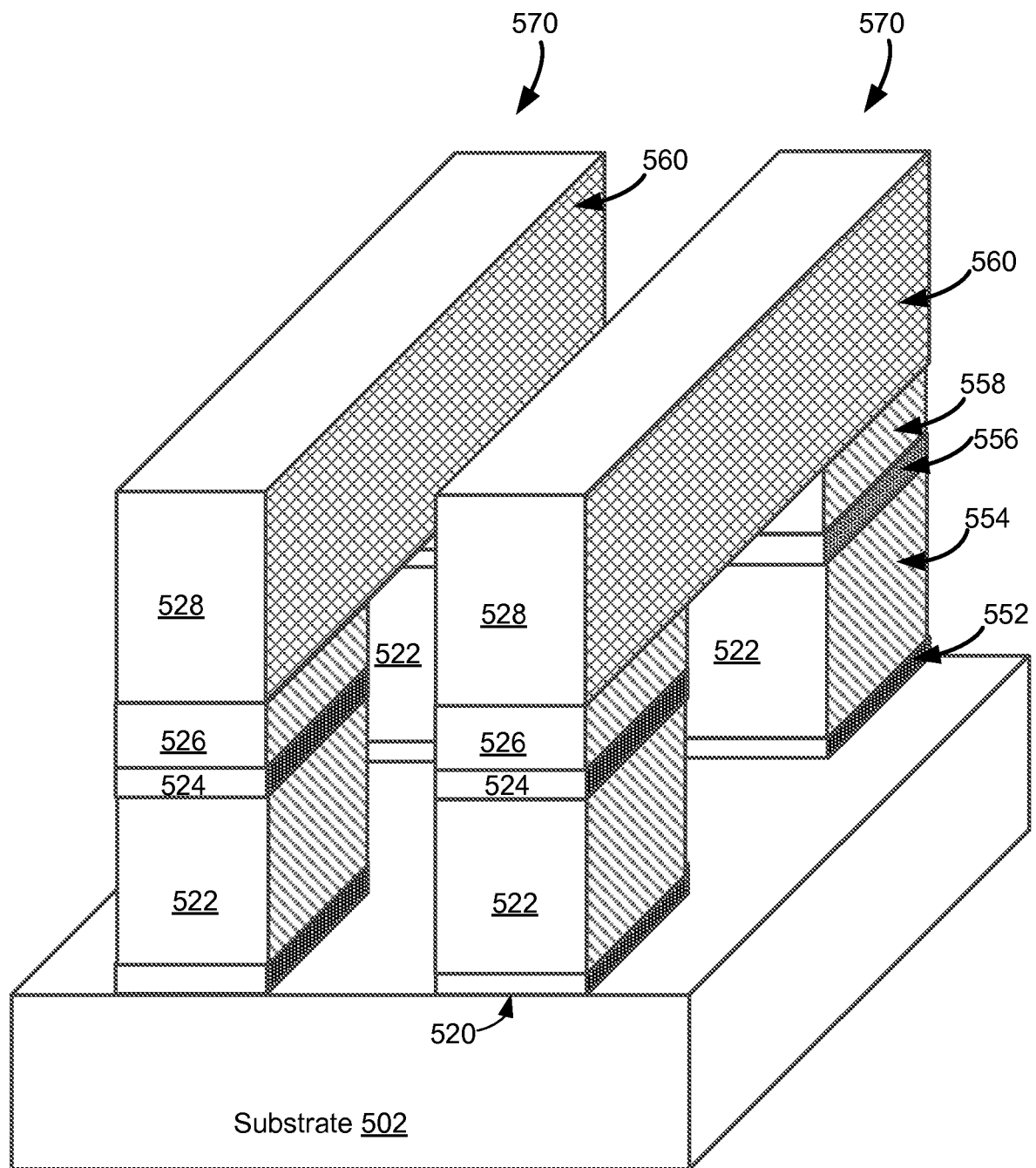


Fig. 5B

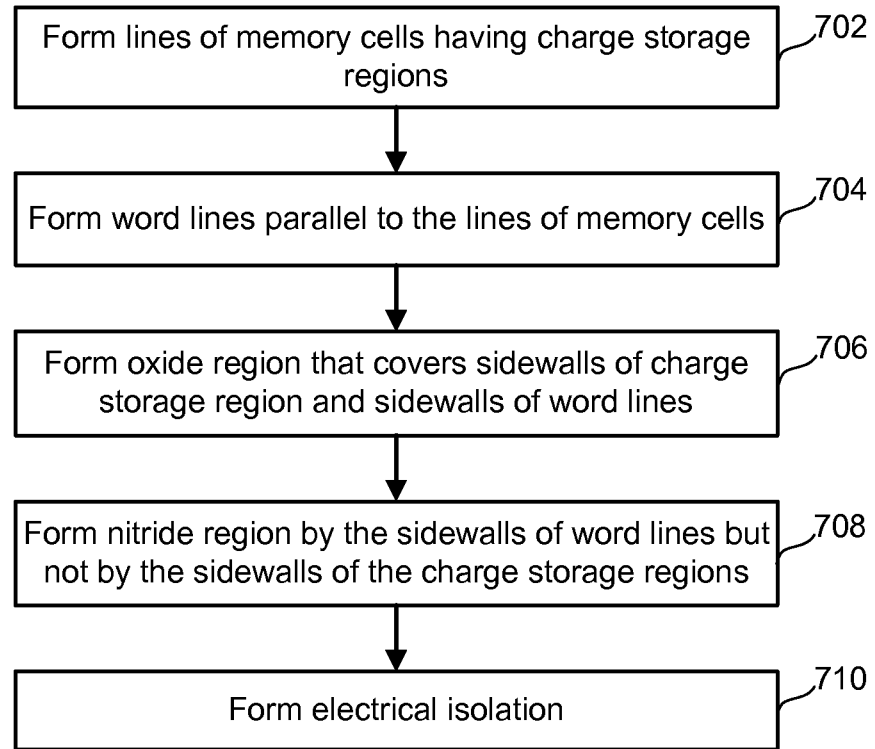


Fig. 7

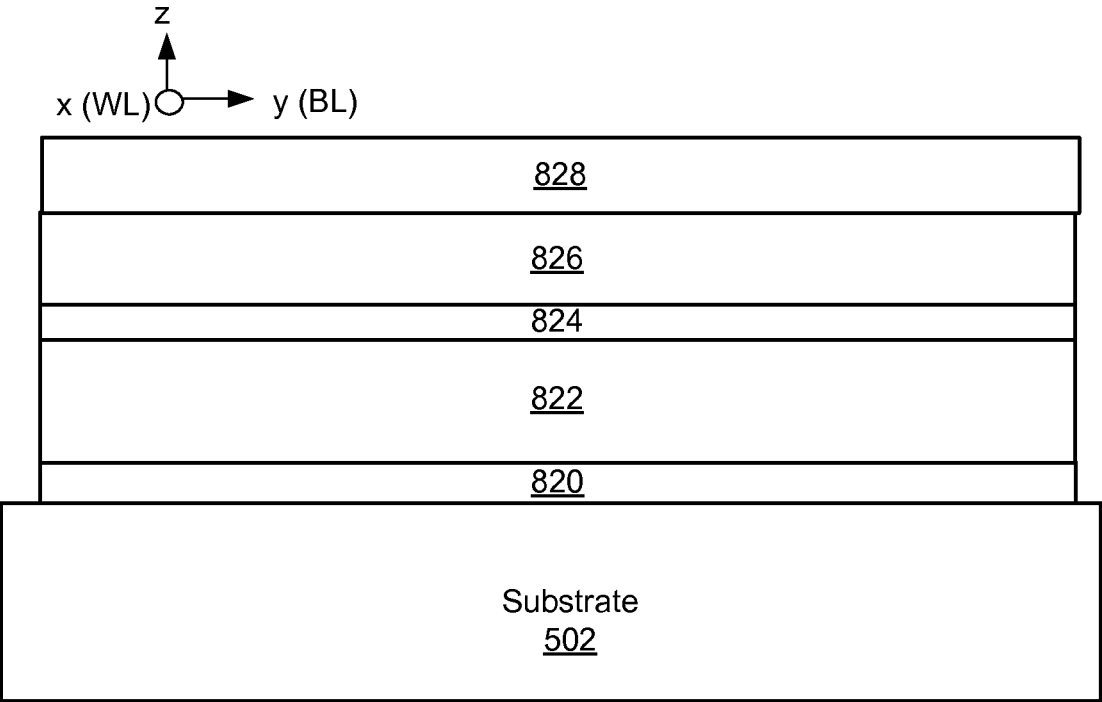


Fig. 8A

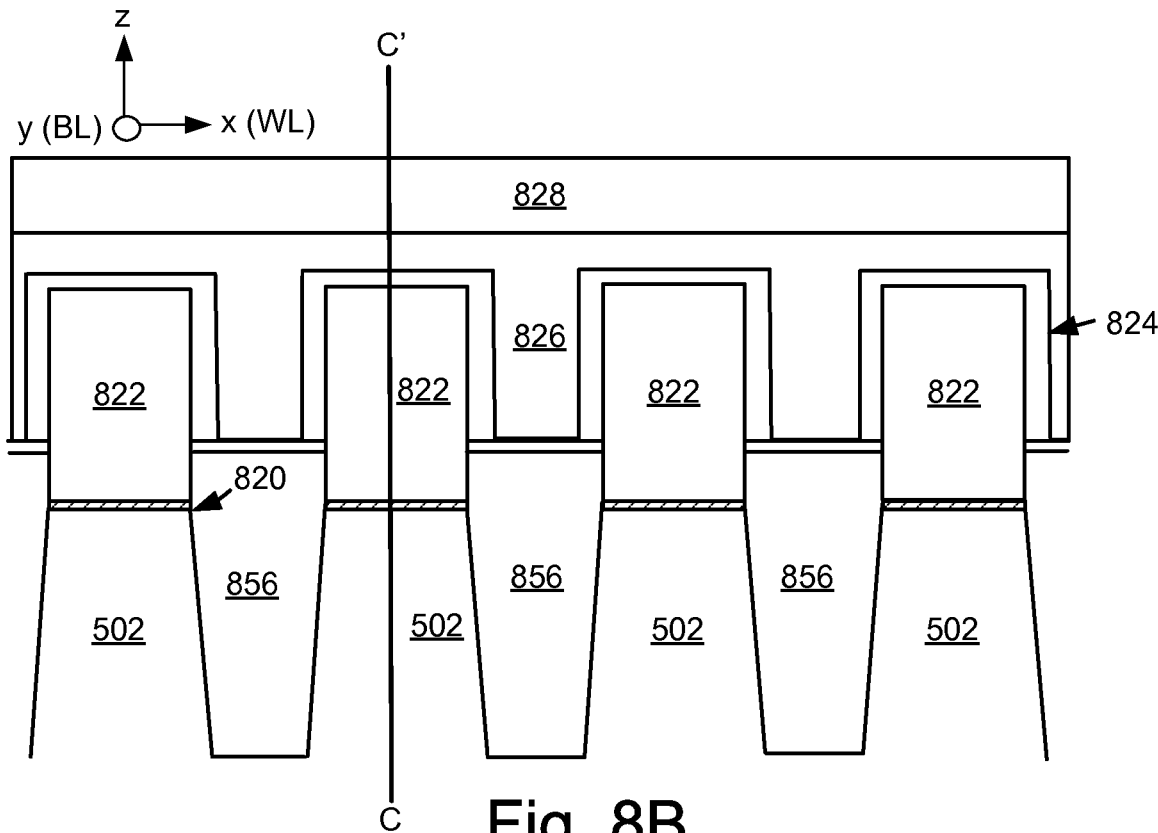


Fig. 8B

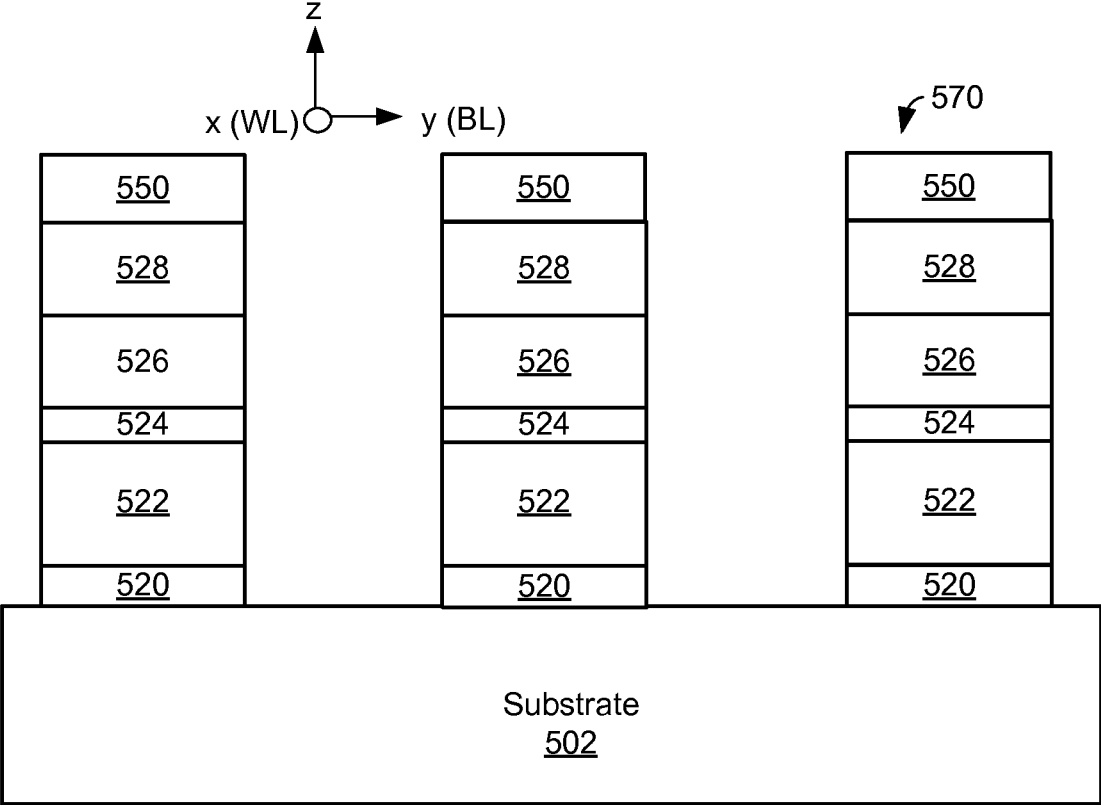


Fig. 8C

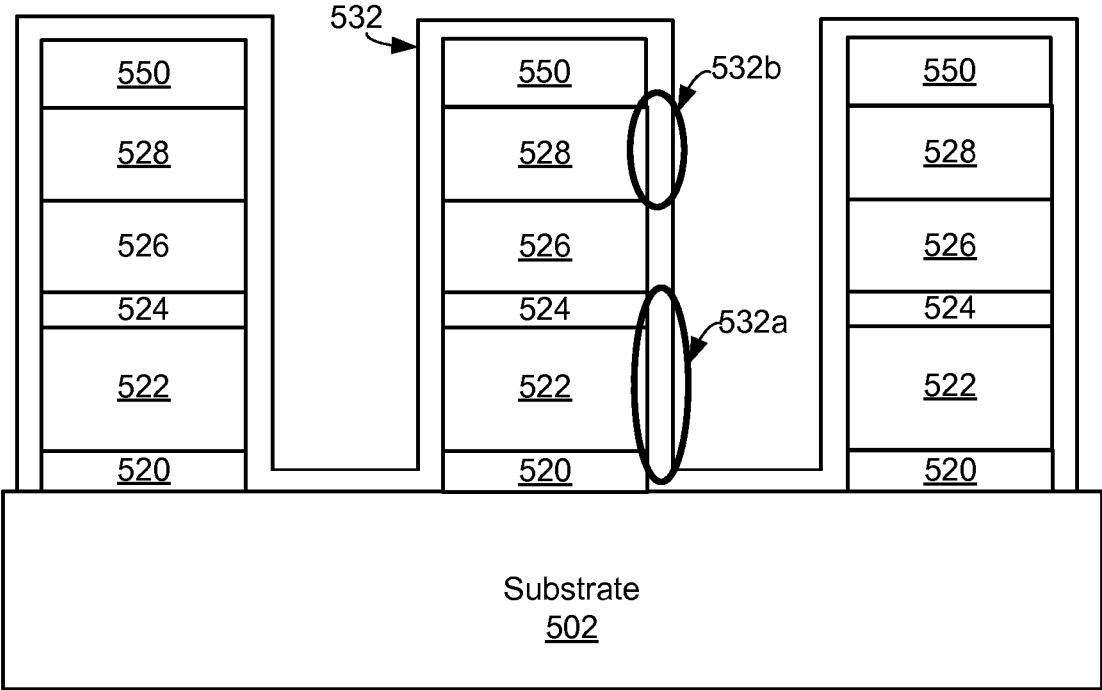


Fig. 8D

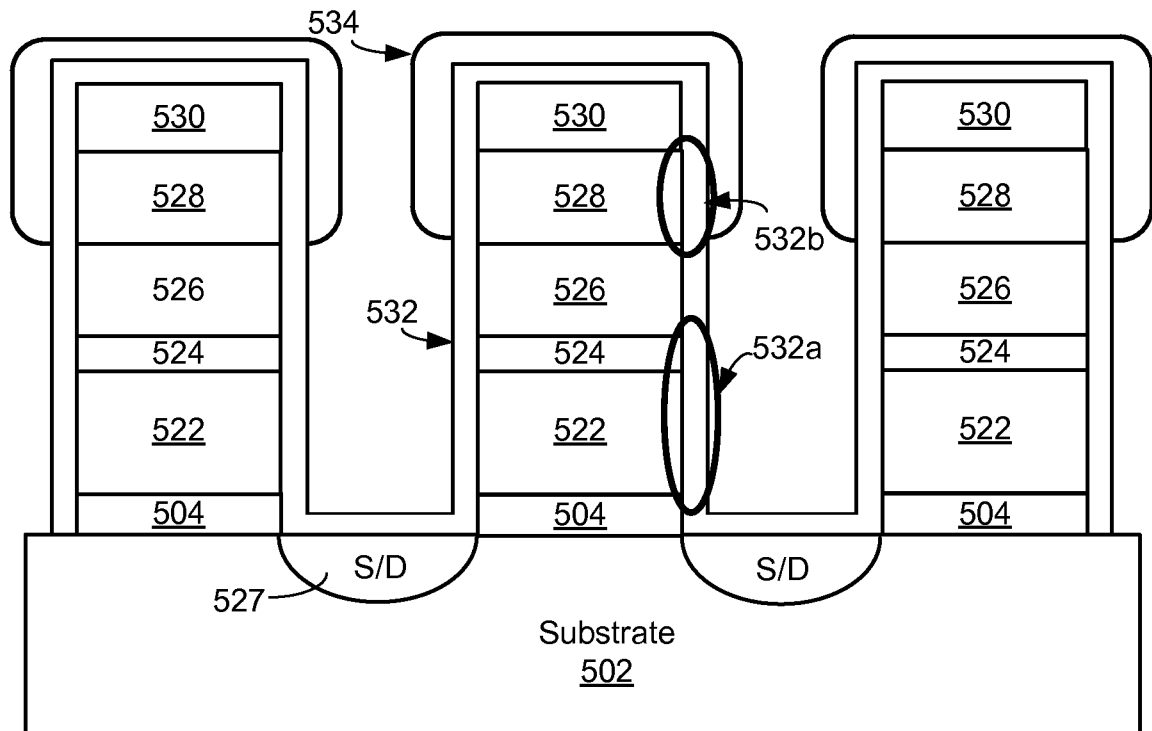


Fig. 8E

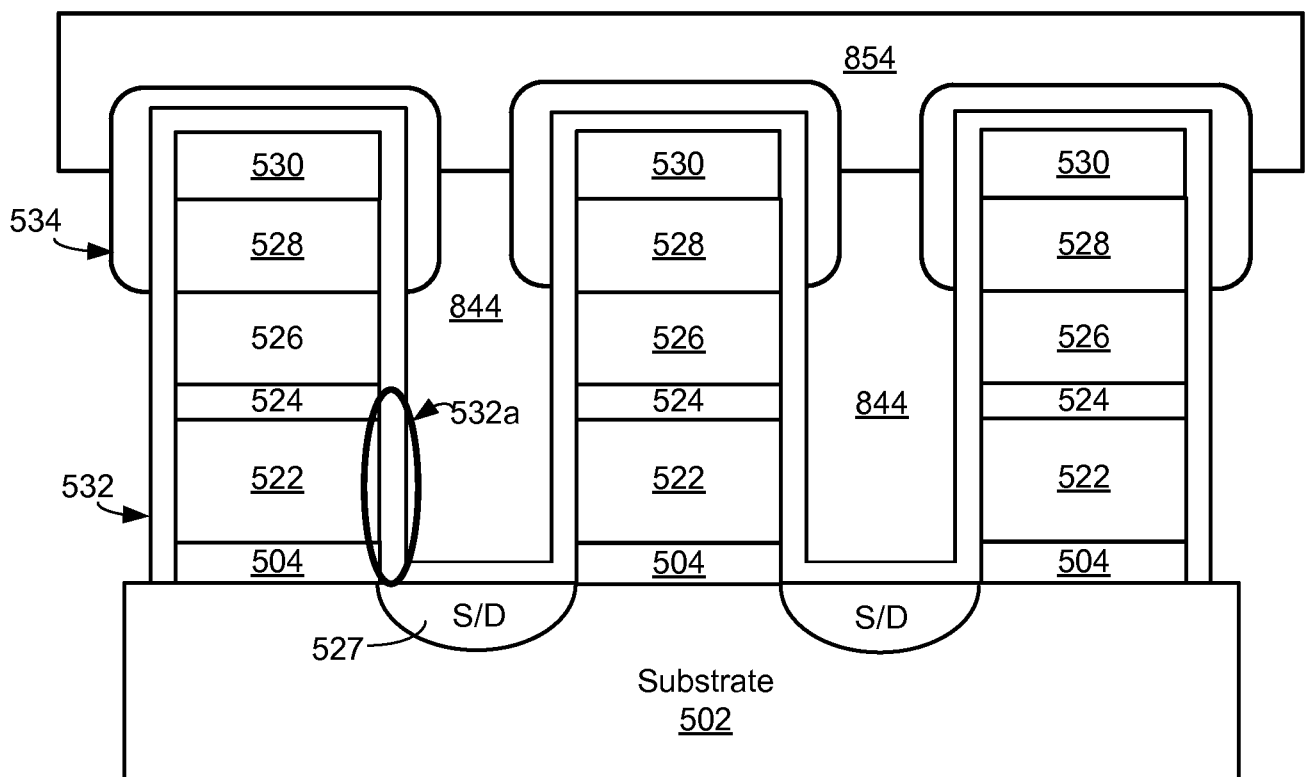


Fig. 8F

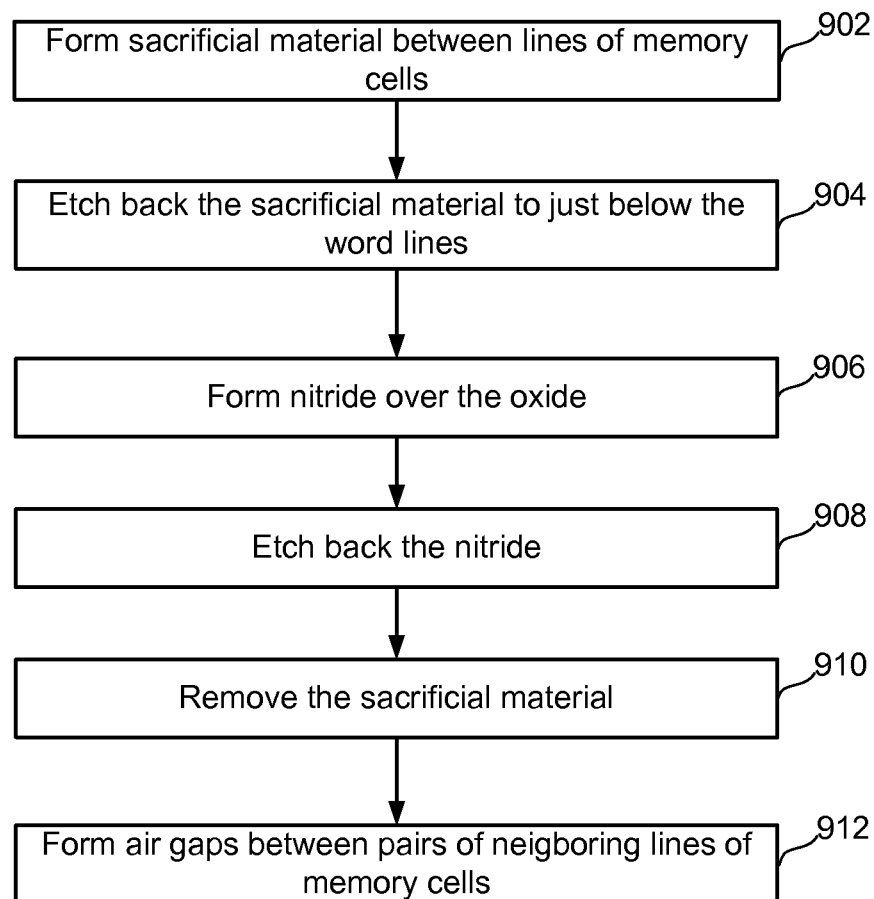


Fig. 9

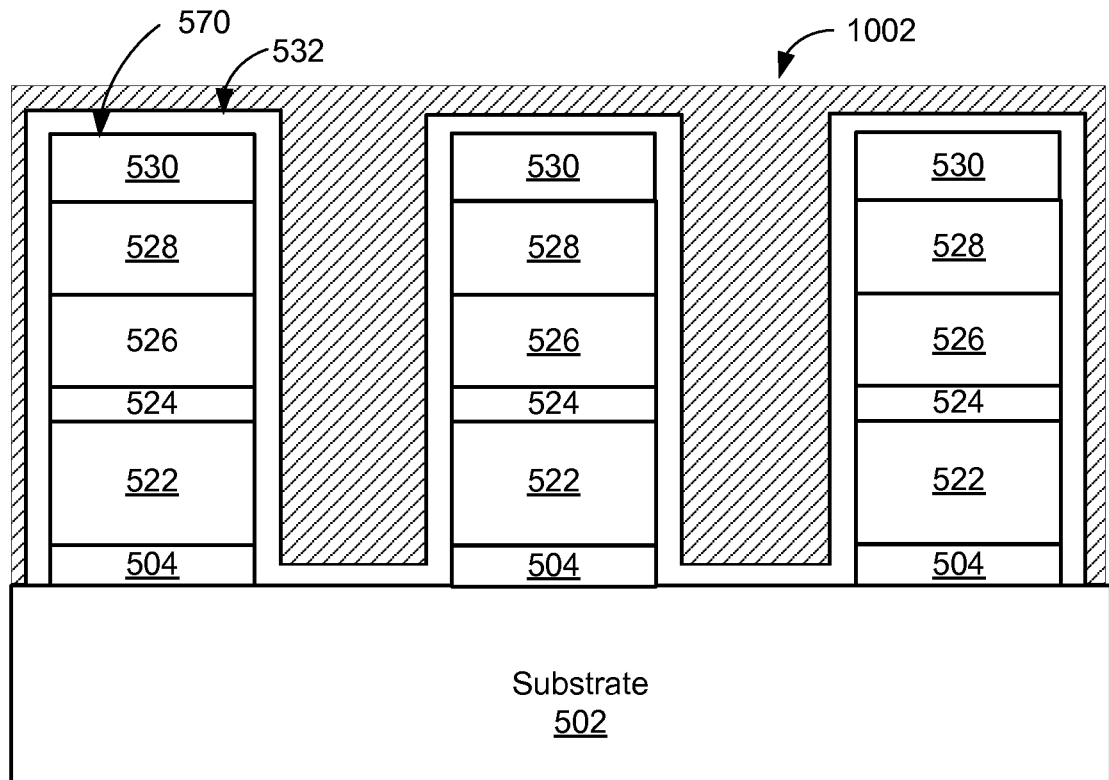


Fig. 10A

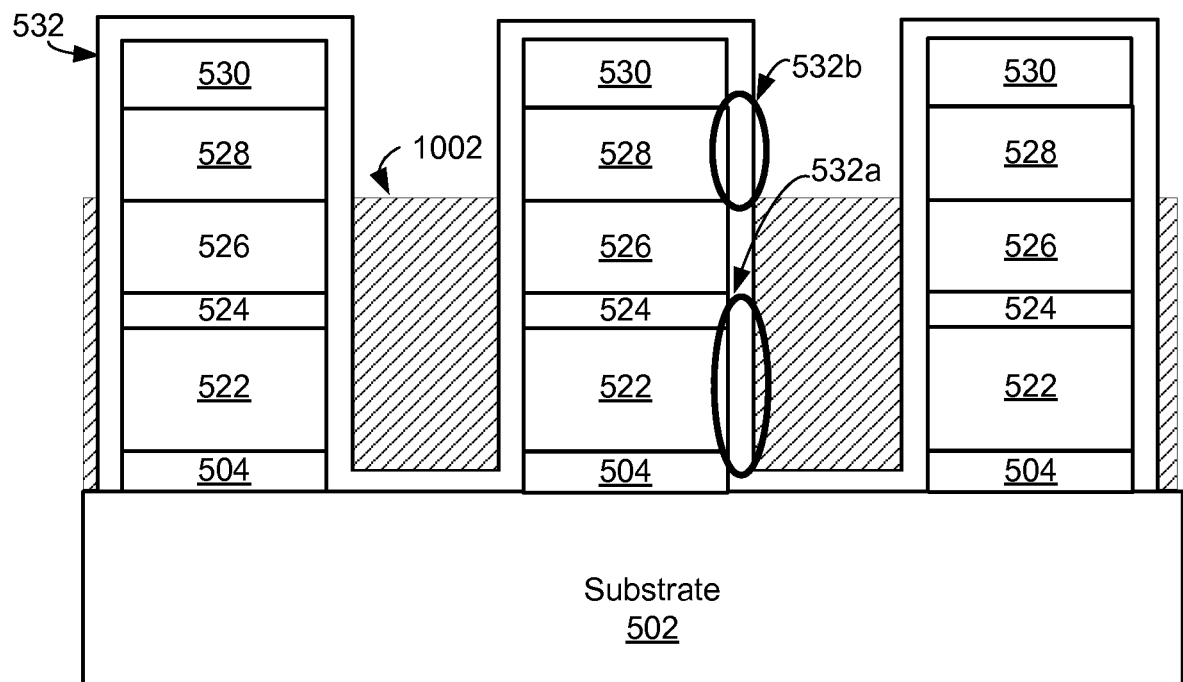


Fig. 10B

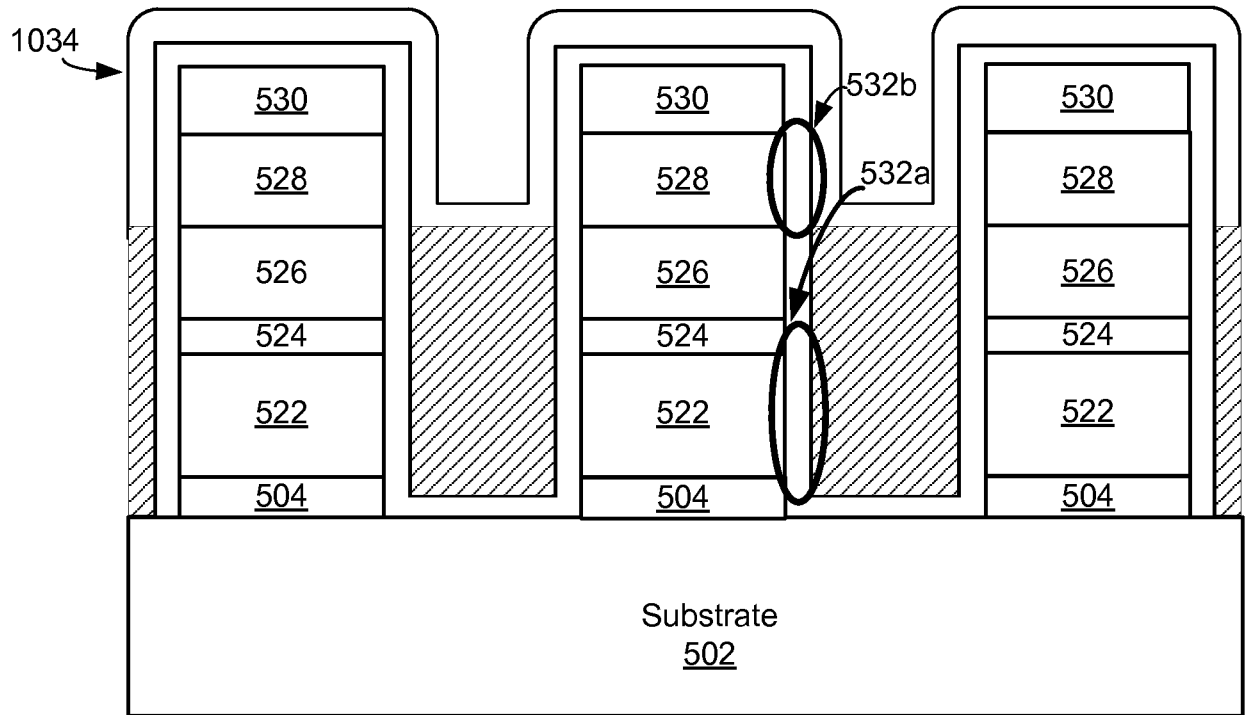


Fig. 10C

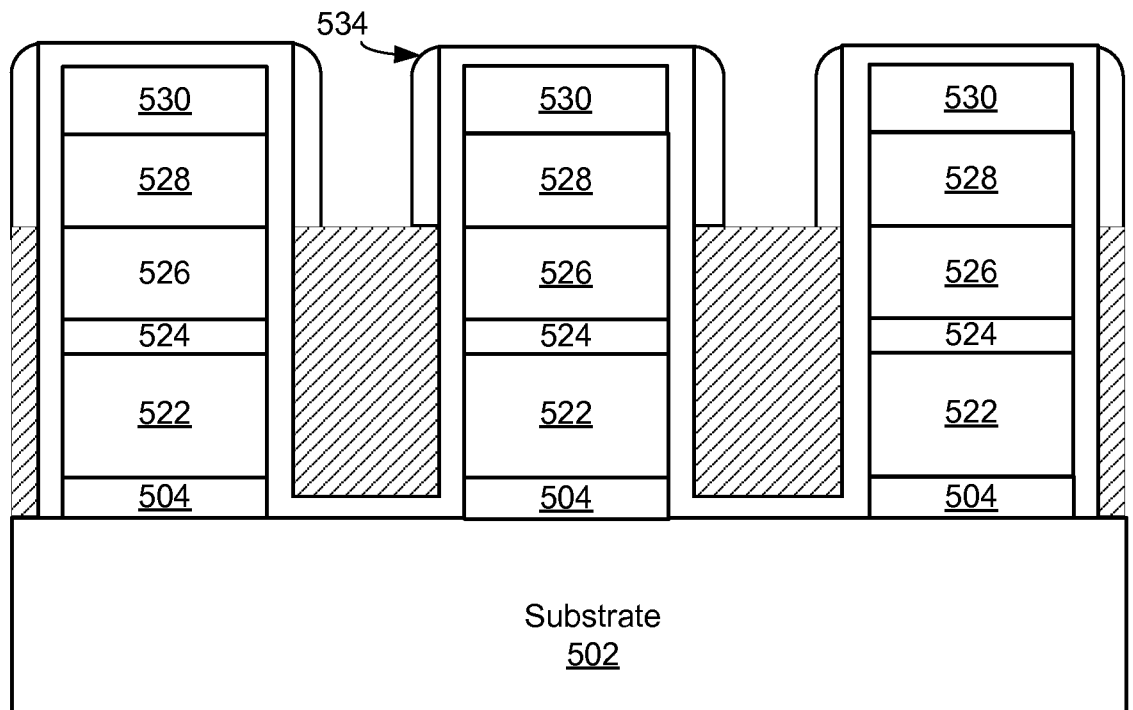


Fig. 10D

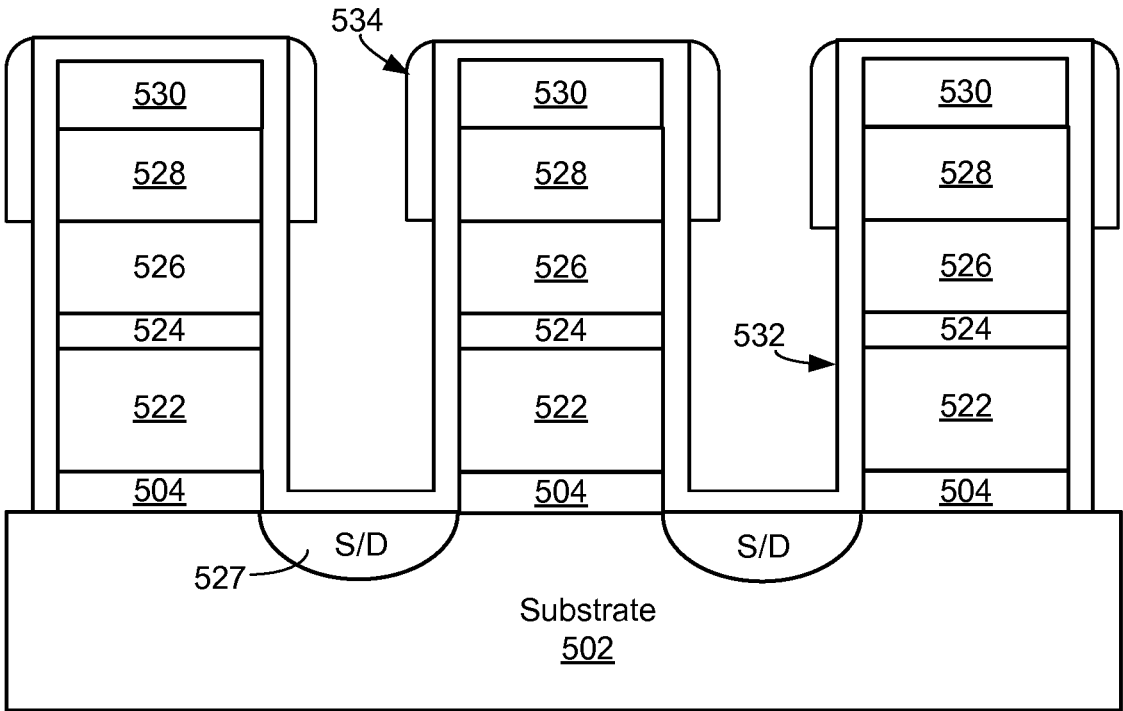


Fig. 10E

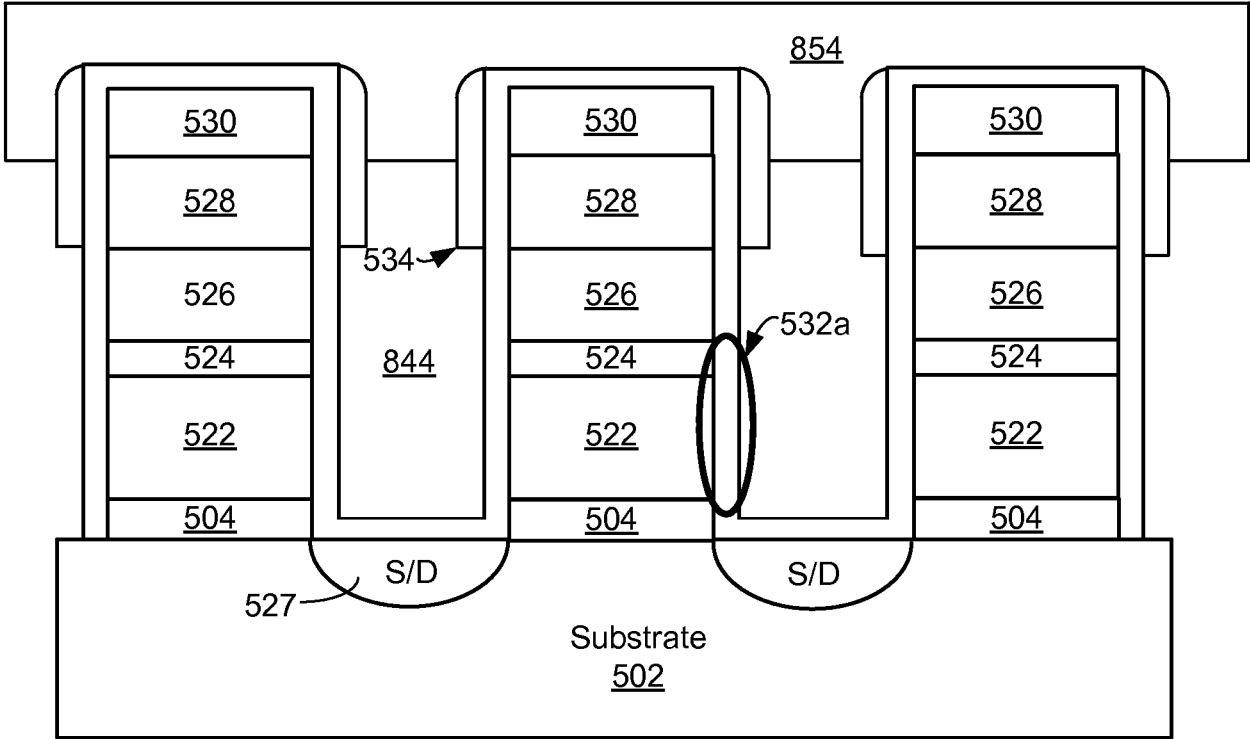


Fig. 10F

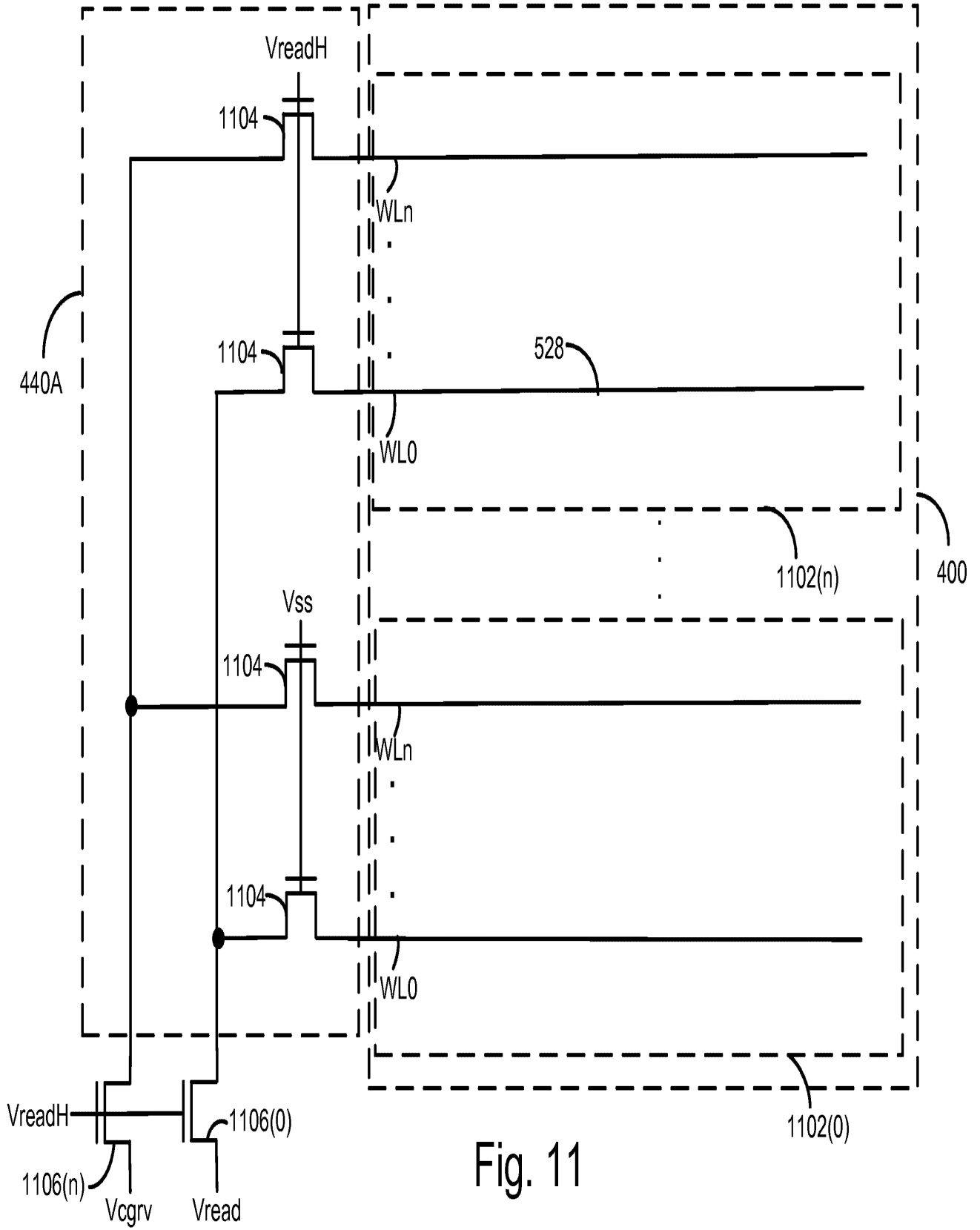
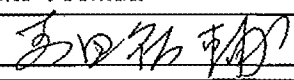


Fig. 11

**DECLARATION (37 CFR 1.63) FOR UTILITY OR DESIGN APPLICATION USING AN
APPLICATION DATA SHEET (37 CFR 1.76)**

Title of Invention	Non-Volatile Storage Having Oxide/Nitride Sidewall
As the below named inventor, I hereby declare that: This declaration is directed to: ☒ The attached application, or ☐ United States application or PCT international application number _____ filed on _____. The above-identified application was made or authorized to be made by me. I believe that I am the original inventor or an original joint inventor of a claimed invention in the application. I hereby acknowledge that any willful false statement made in this declaration is punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both. WARNING: Petitioner/applicant is cautioned to avoid submitting personal information in documents filed in a patent application that may contribute to identity theft. Personal information such as social security numbers, bank account numbers, or credit card numbers (other than a check or credit card authorization form PTO-2038 submitted for payment purposes) is never required by the USPTO to support a petition or an application. If this type of personal information is included in documents submitted to the USPTO, petitioners/applicants should consider redacting such personal information from the documents before submitting them to the USPTO. Petitioner/applicant is advised that the record of a patent application is available to the public after publication of the application (unless a non-publication request in compliance with 37 CFR 1.213(a) is made in the application) or issuance of a patent. Furthermore, the record from an abandoned application may also be available to the public if the application is referenced in a published application or an issued patent (see 37 CFR 1.14). Checks and credit card authorization forms PTO-2038 submitted for payment purposes are not retained in the application file and therefore are not publicly available. LEGAL NAME OF INVENTOR Inventor: <u>Yusuke Yoshida</u> Date (Optional): <u>Oct. 10th, 2014</u> Signature: <u></u> Note: An application data sheet (PTO/SB/14 or equivalent), including naming the entire inventive entity, must accompany this form or must have been previously filed. Use an additional PTO/AIA/01 form for each additional inventor.	

This collection of information is required by 35 U.S.C. 115 and 37 CFR 1.63. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 1 minute to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

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CLAIMS

What is claimed is:

1. A method of forming a memory device comprising:
 - forming a plurality of lines of memory cells, individual memory cells having a charge storage region and a control gate, the charge storage regions each having sidewalls;
 - forming a plurality of word lines parallel to the lines of memory cells, each word line being formed on the control gates of the memory cells in one of the lines, the word lines each having sidewalls;
 - forming oxide that covers the sidewalls of the charge storage regions of the memory cells and that covers the sidewalls of the word lines; and
 - forming a nitride region that is adjacent to the oxide that covers the sidewalls of the word lines but is not adjacent to the oxide that covers the sidewalls of the charge storage regions.
2. The method of claim 1, further comprising:
 - forming air gaps between adjacent pairs of the plurality of word lines, a portion of the air gaps being adjacent to the oxide that covers the sidewalls of the charge storage regions.
3. The method of claim 1, wherein the forming a nitride region that is adjacent to the oxide that covers the sidewalls of the word line but is not adjacent to the oxide that covers the sidewalls of the charge storage regions comprises:
 - forming a sacrificial material between the lines of memory cells after forming the oxide, wherein the sacrificial material covers the oxide that covers the sidewalls of the charge storage regions but does not cover the oxide that covers the sidewalls of the word lines;
 - forming the nitride region on the oxide that covers the sidewalls of the word lines with the sacrificial material in place; and
 - removing the sacrificial material while leaving the nitride region in place.

4. The method of claim 3, wherein the sacrificial material comprises silicon, nitrogen, and hydrogen.
5. The method of claim 1, wherein forming the plurality of word lines comprises forming the plurality of word lines from tungsten.
6. The method of claim 1, wherein forming the plurality of lines of memory cells comprises forming the charge storage regions comprising a dielectric charge trapping region.
7. The method of claim 1, wherein forming the plurality of lines of memory cells comprises forming the charge storage regions comprising a conductive floating gate.
8. A memory device comprising:
 - a plurality of lines of memory cells, the memory cells comprising:
 - a charge storage region having sidewalls; and
 - a control gate;
 - a plurality of word lines each having sidewalls, each of the word lines being associated with a line of the memory cells, each of the word lines being coupled to the control gates of the memory cells with which it is associated;
 - first oxide regions that cover the sidewalls of the charge storage regions;
 - second oxide regions that cover the sidewalls of the word lines;
 - nitride regions that cover the second oxide regions; and
 - electrical isolation regions other than silicon nitride adjacent to the second oxide regions that cover the sidewalls of the charge storage regions.
9. The memory device of claim 8, wherein the electrical isolation regions comprise:
 - a plurality of air gaps, each air gap between a neighboring pair of the plurality of word lines, the air gaps being adjacent to second oxide regions.
10. The memory device of claim 8, wherein the word lines comprise tungsten.

11. The memory device of claim 8, wherein the charge storage region is a conductive floating gate.
12. The memory device of claim 8, wherein the charge storage region is a dielectric charge trapping region.
13. The memory device of claim 8, further comprising peripheral circuitry, wherein the word lines are electrically coupled to the peripheral circuitry.
14. The memory device of claim 8, wherein the first oxide regions and the second oxide regions comprise silicon oxide and the nitride regions comprise silicon nitride.
15. A method of forming a memory array, the method comprising:
 - forming lines of memory cell stacks, each line comprising a plurality of memory cells and a tungsten word line, individual memory cells having a charge storage region, the lines of memory cell stacks having sidewalls;
 - forming silicon oxide on the sidewalls of the lines of memory cell stacks, the silicon oxide having sidewalls;
 - forming a sacrificial material between the lines of memory cell stacks after forming the silicon oxide, the sacrificial material having a top surface that is below the word lines but above the charge storage regions, the sacrificial material having an etch selectively with respect to the silicon oxide, a portion of the silicon oxide remains exposed after forming the sacrificial material;
 - forming silicon nitride on the sidewalls of the exposed silicon oxide;
 - removing the sacrificial material while leaving the silicon oxide on the sidewalls of the lines of memory cell stacks and the silicon nitride on the sidewalls of the silicon oxide adjacent to the word lines; and
 - forming air gaps between neighboring pairs of the lines of memory cell stacks.

16. The method of claim 15, wherein the forming silicon nitride on the sidewalls of the exposed silicon oxide comprises:

depositing silicon nitride over exposed portions of the memory cell stacks with the sacrificial material in place; and

etching the deposited silicon nitride while leaving silicon nitride on the sidewalls of the exposed silicon oxide.

17. The method of claim 15, wherein forming the sacrificial material comprises depositing silicon, nitrogen, and hydrogen.

18. The method of claim 15, wherein forming the sacrificial material includes performing a flowable Chemical Vapor Deposition (CVD) process.

19. A memory device comprising:

a plurality of lines of memory cell stacks, each line comprising a plurality of memory cells and a tungsten word line, individual memory cells having a charge storage region, the lines of memory cell stacks having sidewalls;

silicon oxide that covers the sidewalls of the memory cell stacks;

silicon nitride that covers portions of the silicon oxide that are adjacent to the tungsten word lines; and

word line air gaps between neighboring pairs of the plurality of lines of memory cell stacks, the word line air gaps being adjacent to portions of the silicon oxide that is adjacent to the charge storage regions.

20. The memory device of claim 19, wherein the plurality of memory cells are arranged as NAND strings that are perpendicular to the word lines.

21. The memory device of claim 19, further comprising peripheral circuitry, wherein the word lines are electrically coupled to the peripheral circuitry.

**DECLARATION (37 CFR 1.63) FOR UTILITY OR DESIGN APPLICATION USING AN
APPLICATION DATA SHEET (37 CFR 1.76)**

Title of Invention	Non-Volatile Storage Having Oxide/Nitride Sidewall
As the below named inventor, I hereby declare that: This declaration is directed to: ☒ The attached application, or ☐ United States application or PCT international application number _____ filed on _____. The above-identified application was made or authorized to be made by me. I believe that I am the original inventor or an original joint inventor of a claimed invention in the application. I hereby acknowledge that any willful false statement made in this declaration is punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both. WARNING: Petitioner/applicant is cautioned to avoid submitting personal information in documents filed in a patent application that may contribute to identity theft. Personal information such as social security numbers, bank account numbers, or credit card numbers (other than a check or credit card authorization form PTO-2038 submitted for payment purposes) is never required by the USPTO to support a petition or an application. If this type of personal information is included in documents submitted to the USPTO, petitioners/applicants should consider redacting such personal information from the documents before submitting them to the USPTO. Petitioner/applicant is advised that the record of a patent application is available to the public after publication of the application (unless a non-publication request in compliance with 37 CFR 1.213(a) is made in the application) or issuance of a patent. Furthermore, the record from an abandoned application may also be available to the public if the application is referenced in a published application or an issued patent (see 37 CFR 1.14). Checks and credit card authorization forms PTO-2038 submitted for payment purposes are not retained in the application file and therefore are not publicly available. LEGAL NAME OF INVENTOR Inventor: <u>Takashi Kashimura</u> Date (Optional): <u>10/10/2014</u> Signature: <u>Takashi Kashimura</u> Note: An application data sheet (PTO/SB/14 or equivalent), including naming the entire inventive entity, must accompany this form or must have been previously filed. Use an additional PTO/AIA/01 form for each additional inventor.	

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number		
	Filing Date		2014-10-10
	First Named Inventor	Takashi Kashimura	
	Art Unit		
	Examiner Name		
	Attorney Docket Number	SAND-01720US0	

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**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**
(Not for submission under 37 CFR 1.99)

Application Number	
Filing Date	2014-10-10
First Named Inventor	Takashi Kashimura
Art Unit	
Examiner Name	
Attorney Docket Number	SAND-01720US0

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

☐ See attached certification statement.

☐ The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/RonaldMPomerence#43009/	Date (YYYY-MM-DD)	2014-10-10
Name/Print	Ronald M. Pomerence	Registration Number	43009

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7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.
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**DECLARATION (37 CFR 1.63) FOR UTILITY OR DESIGN APPLICATION USING AN
APPLICATION DATA SHEET (37 CFR 1.76)**

Title of Invention	Non-Volatile Storage Having Oxide/Nitride Sidewall
-------------------------------	--

As the below named inventor, I hereby declare that:

This declaration is directed to: ☒ The attached application, or
☐ United States application or PCT international application number _____
filed on _____

The above-identified application was made or authorized to be made by me.

I believe that I am the original inventor or an original joint inventor of a claimed invention in the application.

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LEGAL NAME OF INVENTOR

Inventor: Kazutaka Yoshizawa Date (Optional): 10/10/2014

Signature: K. Yoshizawa

Note: An application data sheet (PTO/SB/14 or equivalent), including naming the entire inventive entity, must accompany this form or must have been previously filed. Use an additional PTO/AIA/01 form for each additional inventor.

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APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY DOCKET NO	TOT CLAIMS	IND CLAIMS
14/511,834	10/10/2014	2827	2100	SAND-01720US0	21	4

CONFIRMATION NO. 8559

64948
VIERRA MAGEN/SANDISK CORPORATION
575 MARKET STREET
SUITE 3750
SAN FRANCISCO, CA 94105

FILING RECEIPT



OC000000071391451

Date Mailed: 10/17/2014

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Inventor(s)

Takashi Kashimura, Yokkaichi-shi, JAPAN;
Xiaolong Hu, Yokkaichi-shi, JAPAN;
Sayako Nagamine, Yokkaichi-shi, JAPAN;
Yusuke Yoshida, Yokkaichi-shi, JAPAN;
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Akira Nakada, Yokkaichi-shi, JAPAN;
Kazutaka Yoshizawa, Kuwana-shi, JAPAN;

Applicant(s)

SanDisk Technologies Inc., Plano, TX

Power of Attorney: None

Domestic Applications for which benefit is claimed - None.

A proper domestic benefit claim must be provided in an Application Data Sheet in order to constitute a claim for domestic benefit. See 37 CFR 1.76 and 1.78.

Foreign Applications for which priority is claimed (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see <http://www.uspto.gov> for more information.) - None.

Foreign application information must be provided in an Application Data Sheet in order to constitute a claim to foreign priority. See 37 CFR 1.55 and 1.76.

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page 1 of 3

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 14/511,834**

Projected Publication Date: 04/14/2016

Non-Publication Request: No

Early Publication Request: No

Title

Non-Volatile Storage Having Oxide/Nitride Sidewall

Preliminary Class

365

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications: No

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The grant of a license does not in any way lessen the responsibility of a licensee for the security of the subject matter as imposed by any Government contract or the provisions of existing laws relating to espionage and the national security or the export of technical data. Licensees should apprise themselves of current regulations especially with respect to certain countries, of other agencies, particularly the Office of Defense Trade Controls, Department of State (with respect to Arms, Munitions and Implements of War (22 CFR 121-128)); the Bureau of Industry and Security, Department of Commerce (15 CFR parts 730-774); the Office of Foreign Assets Control, Department of Treasury (31 CFR Parts 500+) and the Department of Energy.

NOT GRANTED

No license under 35 U.S.C. 184 has been granted at this time, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" DOES NOT appear on this form. Applicant may still petition for a license under 37 CFR 5.12, if a license is desired before the expiration of 6 months from the filing date of the application. If 6 months has lapsed from the filing date of this application and the licensee has not received any indication of a secrecy order under 35 U.S.C. 181, the licensee may foreign file the application pursuant to 37 CFR 5.15(b).

SelectUSA

The United States represents the largest, most dynamic marketplace in the world and is an unparalleled location for business investment, innovation, and commercialization of new technologies. The U.S. offers tremendous resources and advantages for those who invest and manufacture goods here. Through SelectUSA, our nation works to promote and facilitate business investment. SelectUSA provides information assistance to the international investor community; serves as an ombudsman for existing and potential investors; advocates on behalf of U.S. cities, states, and regions competing for global investment; and counsels U.S. economic development organizations on investment attraction best practices. To learn more about why the United States is the best country in the world to develop technology, manufacture products, deliver services, and grow your business, visit <http://www.SelectUSA.gov> or call +1-202-482-6800.

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875						Application or Docket Number 14/511,834			
APPLICATION AS FILED - PART I									
(Column 1)		(Column 2)		SMALL ENTITY		OR OTHER THAN SMALL ENTITY			
FOR	NUMBER FILED	NUMBER EXTRA		RATE(\$)	FEE(\$)		RATE(\$)		
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A		N/A			N/A		
SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A		N/A			N/A		
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A		N/A			N/A		
TOTAL CLAIMS (37 CFR 1.16(i))	21	minus 20 =	*	1			x 80 =		
INDEPENDENT CLAIMS (37 CFR 1.16(h))	4	minus 3 =	*	1			x 420 =		
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$310 (\$155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						0.00		
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							0.00		
* If the difference in column 1 is less than zero, enter "0" in column 2.				TOTAL			TOTAL 2100		
APPLICATION AS AMENDED - PART II									
(Column 1)		(Column 2)		(Column 3)		SMALL ENTITY		OR OTHER THAN SMALL ENTITY	
AMENDMENT A	CLAIMS REMAINING AFTER AMENDMENT	MINUS	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE(\$)	ADDITIONAL FEE(\$)		RATE(\$)	ADDITIONAL FEE(\$)
	Total (37 CFR 1.16(i))	*	Minus	**	=	x	=	OR	x
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x	=	OR	x
	Application Size Fee (37 CFR 1.16(s))							OR	
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR	
					TOTAL ADD'L FEE			OR	TOTAL ADD'L FEE
AMENDMENT B	CLAIMS REMAINING AFTER AMENDMENT	MINUS	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE(\$)	ADDITIONAL FEE(\$)		RATE(\$)	ADDITIONAL FEE(\$)
	Total (37 CFR 1.16(i))	*	Minus	**	=	x	=	OR	x
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x	=	OR	x
	Application Size Fee (37 CFR 1.16(s))							OR	
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR	
					TOTAL ADD'L FEE			OR	TOTAL ADD'L FEE
* If the entry in column 1 is less than the entry in column 2, write "0" in column 3. ** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20". *** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3". The "Highest Number Previously Paid For" (Total or Independent) is the highest found in the appropriate box in column 1.									

Electronic Acknowledgement Receipt

EFS ID:	21221777
Application Number:	14511834
International Application Number:	
Confirmation Number:	8559
Title of Invention:	Non-Volatile Storage Having Oxide/Nitride Sidewall
First Named Inventor/Applicant Name:	Takashi Kashimura
Customer Number:	64948
Filer:	Ronald Mark Pomerence/Wendy Goy
Filer Authorized By:	Ronald Mark Pomerence
Attorney Docket Number:	SAND-01720US0
Receipt Date:	15-JAN-2015
Filing Date:	10-OCT-2014
Time Stamp:	15:59:29
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no
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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Power of Attorney	1720-poa-signed.pdf	125788 5646c4e5ccf094cadb553fe579c4a6f5f0f55220	no	1

Warnings:

Information:

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application	)	<u>PATENT APPLICATION</u>
Inventors: Kashimura et al.	)	
Application No.: 14/511,834	)	
Filed Date: October 10, 2014	)	
Title: NON-VOLATILE STORAGE HAVING	)	Customer No. 64948
OXIDE/NITRIDE SIDEWALL	)	

POWER OF ATTORNEY (REVOCATION OF PRIOR POWERS)
AND STATEMENT UNDER 37 C.F.R. 3.73(b)

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Assignee hereby revokes all previous powers of attorney given in the above-identified application and appoints all attorneys and agents associated with Customer Number 64948 as our attorneys to prosecute the application identified above, and to transact all business in the United States Patent and Trademark Office connected therewith.

Please recognize or change the correspondence address for the above-identified application to the address associated with **Customer Number 64948** and direct any telephone calls to (415) 489-4100.

SanDisk Technologies Inc., a Texas Corporation, is the assignee of the entire right, title and interest in the above-identified patent application. I, the undersigned, declare that I have reviewed copies of the documentary evidence establishing chain of title to the patent application identified above from the inventors to the assignee which:

_____ is filed for recordation herewith; or
 X was recorded at Reel 033936, Frames 0058-0067; or
_____ a copy is attached herewith.

The undersigned is authorized to sign this document on behalf of the assignee.

Signature: _____
Date: December 10, 2014
Name: Garth Bossow
Title: Director



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
14/511,834	10/10/2014	Takashi Kashimura	SAND-01720US0

CONFIRMATION NO. 8559

POA ACCEPTANCE LETTER



OC000000072985939

64948
VIERRA MAGEN/SANDISK CORPORATION
575 MARKET STREET
SUITE 3750
SAN FRANCISCO, CA 94105

Date Mailed: 01/26/2015

NOTICE OF ACCEPTANCE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 01/15/2015.

The Power of Attorney in this application is accepted. Correspondence in this application will be mailed to the above address as provided by 37 CFR 1.33.

/mabebe/

Office of Data Management, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101

<i>Index of Claims</i> 	Application/Control No. 14511834	Applicant(s)/Patent Under Reexamination KASHIMURA ET AL.
	Examiner DAVID S BLUM	Art Unit 2813

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant			☐ CPA			☐ T.D.			☐ R.1.47		
CLAIM		DATE									
Final	Original	09/16/2015									
	1	÷									
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	3	÷									
	4	÷									
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UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
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Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/511,834	10/10/2014	Takashi Kashimura	SAND-01720US0	8559
64948 7590 09/22/2015 VIERRA MAGEN/SANDISK CORPORATION 575 MARKET STREET SUITE 3750 SAN FRANCISCO, CA 94105			EXAMINER BLUM, DAVID S	
			ART UNIT 2813	PAPER NUMBER
			NOTIFICATION DATE 09/22/2015	DELIVERY MODE ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

patents@vierramagen.com

Office Action Summary	Application No. 14/511,834	Applicant(s) KASHIMURA ET AL.	
	Examiner DAVID S. BLUM	Art Unit 2813	AIA (First Inventor to File) Status Yes

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 2 MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 10/10/14.
☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on ____.
- 2a) ☐ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on ____; the restriction requirement and election have been incorporated into this action.
- 4) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

- 5) ☒ Claim(s) 1-21 is/are pending in the application.
5a) Of the above claim(s) ____ is/are withdrawn from consideration.
- 6) ☐ Claim(s) ____ is/are allowed.
- 7) ☐ Claim(s) ____ is/are rejected.
- 8) ☐ Claim(s) ____ is/are objected to.
- 9) ☒ Claim(s) 1-21 are subject to restriction and/or election requirement.

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

Application Papers

- 10) ☐ The specification is objected to by the Examiner.
- 11) ☐ The drawing(s) filed on ____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

- a) ☐ All b) ☐ Some** c) ☐ None of the:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. ____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) ☐ Notice of References Cited (PTO-892) | 3) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. ____. |
| 2) ☐ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b)
Paper No(s)/Mail Date ____. | 4) ☐ Other: ____. |

This action is in response to the application filed 10/10/14.

Notice of Pre-AIA or AIA Status

1. The present application, filed on or after March 16, 2013, is being examined under the first inventor to file provisions of the AIA.

DETAILED ACTION

Election/Restrictions

2. Restriction to one of the following inventions is required under 35 U.S.C. 121:
 - I. Claims 1-7 and 15-18, drawn to a semiconductor device, classified in H01L27/1157.
 - II. Claims 8-14 and 19-21, drawn to a method of making a semiconductor device, classified in H01L 21/768.

The inventions are distinct, each from the other because of the following reasons:

3. Inventions II and I are related as process of making and product made. The inventions are distinct if either or both of the following can be shown: (1) that the process as claimed can be used to make another and materially different product or (2) that the product as claimed can be made by another and materially different process (MPEP § 806.05(f)). In the instant case the device of claim 8 could be made by fabricating different types of isolation systems, including isolation trenches, air gaps, field oxides, deposition of high k dielectrics, and counter doping wells. The device of

claim 19 could also be made by several methods which include selective deposition of silicon nitride, deposition and removal of silicon nitride, masking and deposition of silicon nitride, and blocking regions and depositing silicon nitride.

4. Restriction for examination purposes as indicated is proper because all these inventions listed in this action are independent or distinct for the reasons given above and there would be a serious search and/or examination burden if restriction were not required because one or more of the following reasons apply:

Because there are several methods to producing the device of claims 8 and 19, simultaneous searching for both inventions would create a search burden.

Applicant is advised that the reply to this requirement to be complete must include (i) an election of an invention to be examined even though the requirement may be traversed (37 CFR 1.143) and (ii) identification of the claims encompassing the elected invention.

The election of an invention may be made with or without traverse. To reserve a right to petition, the election must be made with traverse. If the reply does not distinctly and specifically point out supposed errors in the restriction requirement, the election shall be treated as an election without traverse. Traversal must be presented at the time of election in order to be considered timely. Failure to timely traverse the requirement will result in the loss of right to petition under 37 CFR 1.144. If claims are added after the election, applicant must indicate which of these claims are readable upon the elected invention.

Should applicant traverse on the ground that the inventions are not patentably distinct, applicant should submit evidence or identify such evidence now of record showing the inventions to be obvious variants or clearly admit on the record that this is the case. In either instance, if the examiner finds one of the inventions unpatentable over the prior art, the evidence or admission may be used in a rejection under 35 U.S.C. 103 or pre-AIA 35 U.S.C. 103(a) of the other invention.

5. Applicant is reminded that upon the cancellation of claims to a non-elected invention, the inventorship must be corrected in compliance with 37 CFR 1.48(a) if one or more of the currently named inventors is no longer an inventor of at least one claim remaining in the application. A request to correct inventorship under 37 CFR 1.48(a) must be accompanied by an application data sheet in accordance with 37 CFR 1.76 that identifies each inventor by his or her legal name and by the processing fee required under 37 CFR 1.17(i).

6. The examiner has required restriction between product or apparatus claims and process claims. Where applicant elects claims directed to the product/apparatus, and all product/apparatus claims are subsequently found allowable, withdrawn process claims that include all the limitations of the allowable product/apparatus claims should be considered for rejoinder. All claims directed to a nonelected process invention must include all the limitations of an allowable product/apparatus claim for that process invention to be rejoined.

In the event of rejoinder, the requirement for restriction between the product/apparatus claims and the rejoined process claims will be withdrawn, and the rejoined process claims will be fully examined for patentability in accordance with 37 CFR 1.104. Thus, to be allowable, the rejoined claims must meet all criteria for patentability including the requirements of 35 U.S.C. 101, 102, 103 and 112. Until all claims to the elected product/apparatus are found allowable, an otherwise proper restriction requirement between product/apparatus claims and process claims may be maintained. Withdrawn process claims that are not commensurate in scope with an allowable product/apparatus claim will not be rejoined. See MPEP § 821.04. Additionally, in order for rejoinder to occur, applicant is advised that the process claims should be amended during prosecution to require the limitations of the product/apparatus claims. **Failure to do so may result in no rejoinder.** Further, note that the prohibition against double patenting rejections of 35 U.S.C. 121 does not apply where the restriction requirement is withdrawn by the examiner before the patent issues. See MPEP § 804.01.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to David S. Blum whose telephone number is (571)-272-1687) and e-mail address is David.blum@USPTO.gov .

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, William Kraig, can be reached at (571)-272-8660. Our facsimile number all patent correspondence to be entered into an application is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/David S Blum/

Primary Examiner, Art Unit 2813

September 17, 2015

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application	)	<u>PATENT APPLICATION</u>
Inventor: Kashimura et al.	)	
Application No.: 14/511,834	)	Art Unit: 2813
Filed: October 10, 2014	)	Examiner: Blum, David S.
Title: NON-VOLATILE STORAGE HAVING OXIDE/NITRIDE SIDE WALL	)	<u>Customer No. 64948</u>

RESPONSE A TO OFFICE ACTION/RESTRICTION REQUIREMENT UNDER 37 C.F.R. §
1.111

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

This RESPONSE A is in reply to the Office Action mailed September 22, 2015.

AMENDMENTS to the CLAIMS begin on Page 2 of this paper.

REMARKS begin on Page 6 of this paper.

REMARKS

The above Amendments and these Remarks are in reply to the Office action mailed on September 22, 2015. Claims 1-7 and 15-18 have been cancelled, without prejudice. Claims 8 and 9 have been amended to correct a minor informality. Claims 22-30 have been added. New Claims 24-30 are withdrawn as being directed to a non-elected invention.

The Office has asserted that restriction of the invention in two inventions is warranted:

Invention I – Claims 1-7 and 15-18, drawn to a semiconductor device, classified in H01L27/1157; or

Invention II – Claims 8-14 and 19-21, drawn to a method of making a semiconductor device, classified in H01L21/768.

Applicants elect Invention II claims 8-14 and 19-21 without traverse.

Applicant has added new claims 22-23. These claims depend from elected claim 19. Applicant respectfully asserts that claims 22-23 are directed to the elected invention.

Applicant has added new claims 24-30. These claims are withdrawn as being directed to a non-elected invention. Applicant respectfully asserts that Independent method claim 24 contains all limitations as found in elected apparatus claim 8. As such, upon allowance of claim 8, Applicant respectfully requests that claim 24 be rejoined. Since claims 25-30 depend from claim 24, Applicant also respectfully requests that claims 25-30 be rejoined upon allowance of claim 8.

The Examiner's prompt attention to this matter is greatly appreciated. Should further questions remain, the Examiner is invited to contact the undersigned attorney by telephone.

The Commissioner is authorized to charge any underpayment or credit any overpayment to Deposit Account No. 501826 for any matter in connection with this response, including any fee for extension of time, which may be required.

Respectfully submitted,

Date: November 19, 2015

By: /RonaldMPomerenke#43009/
Ronald M. Pomerenke
Reg. No. 43,009

Vierra Magen Marcus LLP
575 Market Street, Suite 3750
San Francisco, CA 94105
Telephone: (415) 489-4100
Facsimile: (415) 489-4150

AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claim in the application.

- 1-7. (Cancelled)
8. (Currently Amended) A memory device comprising:
a plurality of lines of memory cells, the memory cells comprising:
a charge storage region having sidewalls; and
a control gate;
a plurality of word lines each having sidewalls, each of the word lines being associated with a line of the memory cells, each of the word lines being coupled to the control gates of the memory cells with which it is associated;
first oxide regions that cover the sidewalls of the charge storage regions;
second oxide regions that cover the sidewalls of the word lines;
nitride regions that cover the second oxide regions; and
electrical isolation regions other than silicon nitride adjacent to the first ~~second~~-oxide regions that cover the sidewalls of the charge storage regions.
9. (Currently Amended) The memory device of claim 8, wherein the electrical isolation regions comprise:
a plurality of air gaps, each air gap between a neighboring pair of the plurality of word lines, the air gaps being adjacent to first ~~second~~-oxide regions.
10. (Original) The memory device of claim 8, wherein the word lines comprise tungsten.
11. (Original) The memory device of claim 8, wherein the charge storage region is a conductive floating gate.
12. (Original) The memory device of claim 8, wherein the charge storage region is a dielectric charge trapping region.

13. (Original) The memory device of claim 8, further comprising peripheral circuitry, wherein the word lines are electrically coupled to the peripheral circuitry.

14. (Original) The memory device of claim 8, wherein the first oxide regions and the second oxide regions comprise silicon oxide and the nitride regions comprise silicon nitride.

15-18. (Cancelled)

19. (Original) A memory device comprising:

a plurality of lines of memory cell stacks, each line comprising a plurality of memory cells and a tungsten word line, individual memory cells having a charge storage region, the lines of memory cell stacks having sidewalls;

silicon oxide that covers the sidewalls of the memory cell stacks;

silicon nitride that covers portions of the silicon oxide that are adjacent to the tungsten word lines; and

word line air gaps between neighboring pairs of the plurality of lines of memory cell stacks, the word line air gaps being adjacent to portions of the silicon oxide that is adjacent to the charge storage regions.

20. (Original) The memory device of claim 19, wherein the plurality of memory cells are arranged as NAND strings that are perpendicular to the word lines.

21. (Original) The memory device of claim 19, further comprising peripheral circuitry, wherein the word lines are electrically coupled to the peripheral circuitry.

22. (New) The memory device of claim 19, wherein the charge storage region is a conductive floating gate.

23. (New) The memory device of claim 19, wherein the charge storage region is a dielectric charge trapping region.

24. (New – Withdrawn) A method of forming a memory device, the method comprising:
forming a plurality of lines of memory cells, the memory cells comprising:
a charge storage region having sidewalls; and
a control gate;
forming a plurality of word lines each having sidewalls, each of the word lines being associated with a line of the memory cells, each of the word lines being coupled to the control gates of the memory cells with which it is associated;
forming first oxide regions that cover the sidewalls of the charge storage regions;
forming second oxide regions that cover the sidewalls of the word lines;
forming nitride regions that cover the second oxide regions; and
forming electrical isolation regions other than silicon nitride adjacent to the first oxide regions that cover the sidewalls of the charge storage regions.
25. (New – Withdrawn) The method of claim 24, wherein forming the electrical isolation regions comprises:
forming air gaps between adjacent pairs of the plurality of word lines, a portion of the air gaps being adjacent to the oxide that covers the sidewalls of the charge storage regions.
26. (New – Withdrawn) The method of claim 24, wherein forming the nitride regions that cover the second oxide regions comprises:
forming a sacrificial material between the lines of memory cells after forming the first oxide regions, wherein the sacrificial material covers the first oxide regions that cover the sidewalls of the charge storage regions but does not cover the second oxide regions that cover the sidewalls of the word lines;
forming the nitride regions on the second oxide regions that cover the sidewalls of the word lines with the sacrificial material in place; and
removing the sacrificial material while leaving the nitride regions in place.
27. (New – Withdrawn) The method of claim 26, wherein the sacrificial material comprises silicon, nitrogen, and hydrogen.

28. (New – Withdrawn) The method of claim 24, wherein forming the plurality of word lines comprises forming the plurality of word lines from tungsten.

29. (New – Withdrawn) The method of claim 24, wherein forming the plurality of lines of memory cells comprises forming the charge storage regions comprising a dielectric charge trapping region.

30. (New – Withdrawn) The method of claim 24, wherein forming the plurality of lines of memory cells comprises forming the charge storage regions comprising a conductive floating gate.

Electronic Acknowledgement Receipt

EFS ID:	24131911
Application Number:	14511834
International Application Number:	
Confirmation Number:	8559
Title of Invention:	Non-Volatile Storage Having Oxide/Nitride Sidewall
First Named Inventor/Applicant Name:	Takashi Kashimura
Customer Number:	64948
Filer:	Ronald Mark Pomerence
Filer Authorized By:	
Attorney Docket Number:	SAND-01720US0
Receipt Date:	19-NOV-2015
Filing Date:	10-OCT-2014
Time Stamp:	17:01:42
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no
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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		1720-restrictionresp-001.pdf	111268 82af1ac242af7eb58757645beec3a8d450ce7c1	yes	7

	Multipart Description/PDF files in .zip description		
	Document Description	Start	End
	Response to Election / Restriction Filed	1	1
	Claims	2	5
	Applicant Arguments/Remarks Made in an Amendment	6	7
Warnings:			
Information:			
Total Files Size (in bytes):		111268	
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. <u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. <u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. <u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.			

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 14/511,834	Filing Date 10/10/2014	☐ To be Mailed
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ENTITY: ☒ LARGE ☐ SMALL ☐ MICRO

APPLICATION AS FILED – PART I

FOR	NUMBER FILED	NUMBER EXTRA	RATE (\$)	FEE (\$)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (j), or (m))	N/A	N/A	N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X \$ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X \$ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$310 (\$155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).			
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))				
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL	

APPLICATION AS AMENDED – PART II

AMENDMENT	(Column 1)	(Column 2)	(Column 3)	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)
	11/19/2015	CLAIMS REMAINING AFTER AMENDMENT					
	Total (37 CFR 1.16(i))	* 19	Minus	** 21	= 0	x \$80 =	0
	Independent (37 CFR 1.16(h))	* 3	Minus	***4	= 0	x \$420 =	0
	☐ Application Size Fee (37 CFR 1.16(s))						
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
						TOTAL ADD'L FEE	0

AMENDMENT	(Column 1)	(Column 2)	(Column 3)	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)
		CLAIMS REMAINING AFTER AMENDMENT					
	Total (37 CFR 1.16(i))	*	Minus	**	=	X \$ =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X \$ =	
	☐ Application Size Fee (37 CFR 1.16(s))						
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
						TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
 ** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
 *** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
 The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

LIE
/MARCIA GORDON/

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**
 If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Issue Classification 	Application/Control No. 14511834	Applicant(s)/Patent Under Reexamination KASHIMURA ET AL.
	Examiner DAVID S BLUM	Art Unit 2813

CPC						
Symbol					Type	Version
H01L		27	/	1157	F	2013-01-01
H01L		27	/	11524	I	2013-01-01
H01L		27	/	11526	I	2013-01-01
H01L		27	/	11573	I	2013-01-01
H01L		21	/	768	I	2013-01-01
H01L		23	/	528	I	2013-01-01
H01L		23	/	53257	I	2013-01-01
H01L		21	/	28568	I	2013-01-01
H01L		21	/	28273	I	2013-01-01
H01L		21	/	28282	I	2013-01-01
H01L		21	/	02164	I	2013-01-01
H01L		21	/	0217	I	2013-01-01
H01L		21	/	764	I	2013-01-01
H01L		21	/	31111	I	2013-01-01
H01L		21	/	02271	I	2013-01-01

CPC Combination Sets					
Symbol		Type	Set	Ranking	Version

NONE		Total Claims Allowed: 19	
(Assistant Examiner)	(Date)		
/DAVID S BLUM/ Primary Examiner.Art Unit 2813	12/22/15	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	8D

Issue Classification 	Application/Control No. 14511834	Applicant(s)/Patent Under Reexamination KASHIMURA ET AL.
	Examiner DAVID S BLUM	Art Unit 2813

☐ Claims renumbered in the same order as presented by applicant															
☐ CPA															
☐ T.D.															
☐ R.1.47															
Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
	1		17												
	2		18												
	3	8	19												
	4	9	20												
	5	10	21												
	6	11	22												
	7	12	23												
1	8	13	24												
2	9	14	25												
3	10	15	26												
4	11	16	27												
5	12	17	28												
6	13	18	29												
7	14	19	30												
	15														
	16														

NONE	Total Claims Allowed: 19	
(Assistant Examiner)	(Date)	
/DAVID S BLUM/ Primary Examiner.Art Unit 2813	12/22/15	O.G. Print Claim(s) 1
(Primary Examiner)	(Date)	O.G. Print Figure 8D

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L4	4866	(438/257).CCLS	US-PGPUB; USPAT	OR	OFF	2015/12/22 10:54

EAST Search History (Interference)

< This search history is empty >

12/ 22/ 2015 10:55:41 AM

Notice of References Cited	Application/Control No. 14/511,834		Applicant(s)/Patent Under Reexamination KASHIMURA ET AL.	
	Examiner DAVID S. BLUM		Art Unit 2813	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	CPC Classification	US Classification
*	A	US-2015/0340371 A1	11-2015	LUE; HANG-TING	H01L27/1158	257/324
*	B	US-2015/0318296 A1	11-2015	Kim; Hyun-suk	H01L27/11573	257/296
	C	US-				
	D	US-				
	E	US-				
	F	US-				
	G	US-				
	H	US-				
	I	US-				
	J	US-				
	K	US-				
	L	US-				
	M	US-				

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	CPC Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

64948 7590 01/15/2016
VIERRA MAGEN/SANDISK CORPORATION
575 MARKET STREET
SUITE 3750
SAN FRANCISCO, CA 94105

EXAMINER

BLUM, DAVID S

ART UNIT

PAPER NUMBER

2813

DATE MAILED: 01/15/2016

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
-----------------	-------------	----------------------	---------------------	------------------

14/511,834

10/10/2014

Takashi Kashimura

SAND-01720US0

8559

TITLE OF INVENTION: Non-Volatile Storage Having Oxide/Nitride Sidewall

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	\$960	\$0	\$0	\$960	04/15/2016

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

For purposes of this notice, small entity fees are 1/2 the amount of undiscounted fees, and micro entity fees are 1/2 the amount of small entity fees.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: **Mail** Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or **Fax** (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

64948 7590 01/15/2016
VIERRA MAGEN/SANDISK CORPORATION
575 MARKET STREET
SUITE 3750
SAN FRANCISCO, CA 94105

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/511,834	10/10/2014	Takashi Kashimura	SAND-01720US0	8559

TITLE OF INVENTION: Non-Volatile Storage Having Oxide/Nitride Sidewall

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	\$960	\$0	\$0	\$960	04/15/2016

EXAMINER	ART UNIT	CLASS-SUBCLASS
BLUM, DAVID S	2813	257-316000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

- ☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
- ☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

- (1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
- (2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 _____
2 _____
3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☐ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:

- ☐ Issue Fee
- ☐ Publication Fee (No small entity discount permitted)
- ☐ Advance Order - # of Copies _____

4b. Payment of Fee(s): (Please first reapply any previously paid issue fee shown above)

- ☐ A check is enclosed.
- ☐ Payment by credit card. Form PTO-2038 is attached.
- ☐ The director is hereby authorized to charge the required fee(s), any deficiency, or credits any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. Change in Entity Status (from status indicated above)

- ☐ Applicant certifying micro entity status. See 37 CFR 1.29
- ☐ Applicant asserting small entity status. See 37 CFR 1.27
- ☐ Applicant changing to regular undiscounted fee status.

NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.

NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.

NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature _____

Date _____

Typed or printed name _____

Registration No. _____



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/511,834	10/10/2014	Takashi Kashimura	SAND-01720US0	8559

EXAMINER	
BLUM, DAVID S	

ART UNIT	PAPER NUMBER
2813	

DATE MAILED: 01/15/2016

64948 7590 01/15/2016
VIERRA MAGEN/SANDISK CORPORATION
575 MARKET STREET
SUITE 3750
SAN FRANCISCO, CA 94105

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (Applications filed on or after May 29, 2000)

The Office has discontinued providing a Patent Term Adjustment (PTA) calculation with the Notice of Allowance.

Section 1(h)(2) of the AIA Technical Corrections Act amended 35 U.S.C. 154(b)(3)(B)(i) to eliminate the requirement that the Office provide a patent term adjustment determination with the notice of allowance. See Revisions to Patent Term Adjustment, 78 Fed. Reg. 19416, 19417 (Apr. 1, 2013). Therefore, the Office is no longer providing an initial patent term adjustment determination with the notice of allowance. The Office will continue to provide a patent term adjustment determination with the Issue Notification Letter that is mailed to applicant approximately three weeks prior to the issue date of the patent, and will include the patent term adjustment on the patent. Any request for reconsideration of the patent term adjustment determination (or reinstatement of patent term adjustment) should follow the process outlined in 37 CFR 1.705.

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

OMB Clearance and PRA Burden Statement for PTOL-85 Part B

The Paperwork Reduction Act (PRA) of 1995 requires Federal agencies to obtain Office of Management and Budget approval before requesting most types of information from the public. When OMB approves an agency request to collect information from the public, OMB (i) provides a valid OMB Control Number and expiration date for the agency to display on the instrument that will be used to collect the information and (ii) requires the agency to inform the public about the OMB Control Number's legal significance in accordance with 5 CFR 1320.5(b).

The information collected by PTOL-85 Part B is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450. Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No. 14/511,834	Applicant(s) KASHIMURA ET AL.	
	Examiner DAVID S. BLUM	Art Unit 2813	AIA (First Inventor to File) Status Yes

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to 11/19/15.
☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

3. ☒ The allowed claim(s) is/are 8-14, 19-30. As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:
a) ☐ All b) ☐ Some *c) ☐ None of the:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).
* Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.
Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)
1. ☒ Notice of References Cited (PTO-892)
2. ☒ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
4. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____
5. ☐ Examiner's Amendment/Comment
6. ☒ Examiner's Statement of Reasons for Allowance
7. ☐ Other _____.

/DAVID S BLUM/ Primary Examiner, Art Unit 2813	
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This action is in response to the election filed 11/19/15.

Notice of Pre-AIA or AIA Status

1. The present application, filed on or after March 16, 2013, is being examined under the first inventor to file provisions of the AIA.

Election/Restrictions

2. Applicant's election without traverse of claims 8-23 in the reply filed on 11/19/15 is acknowledged.

3. Claims 8-14 and 19-23, as well as new claims 24-30 are allowable. The restriction requirement regarding method claims , as set forth in the Office action mailed on 9/22/15 , has been reconsidered in view of the allowability of claims to the elected invention pursuant to MPEP § 821.04(a). **The restriction requirement is hereby withdrawn as to any claim that requires all the limitations of an allowable claim.** Specifically, the restriction requirement of different inventions is withdrawn in regard to new claims 24-30. Claims 24-30, directed to a method of making a semiconductor device are no longer withdrawn from consideration because the claim(s) requires all the limitations of an allowable claim (positive step claim limitations merely recite "forming"). In view of the above noted withdrawal of the restriction requirement, applicant is advised that if any claim presented in a continuation or divisional application is anticipated by, or includes all the limitations of, a claim that is allowable in the present application, such

claim may be subject to provisional statutory and/or nonstatutory double patenting rejections over the claims of the instant application.

Once a restriction requirement is withdrawn, the provisions of 35 U.S.C. 121 are no longer applicable. See *In re Ziegler*, 443 F.2d 1211, 1215, 170 USPQ 129, 131-32 (CCPA 1971). See also MPEP § 804.01.

Drawings

4. The drawings were received on 10/10/14. These drawings are accepted.

Reasons for Allowance

5. Claims 8-14 and 19-30 are allowed.
6. The following is an examiner's statement of reasons for allowance:

Claim 8 recites, "A memory device comprising:

a plurality of lines of memory cells, the memory cells comprising:

a charge storage region having sidewalls; and

a control gate;

a plurality of word lines each having sidewalls, each of the word lines being associated with a line of the memory cells, each of the word lines being coupled to the control gates of the memory cells with which it is associated;

first oxide regions that cover the sidewalls of the charge storage regions;

second oxide regions that cover the sidewalls of the word lines;

nitride regions that cover the second oxide regions; and
electrical isolation regions other than silicon nitride adjacent to the first oxide regions
that cover the sidewalls of the charge storage regions.”

This is not taught or suggested by the prior art of record. Kim (US 2015/0318296)
covers the charge storage area with the gate dielectric which is not an oxide and does
not place an oxide on the sidewalls. Purayath (US 8,492,224) does not teach or suggest
an oxide and then a nitride on the sidewalls of the wordlines. Lue (US 2015/0340371)
does not teach or suggest an oxide and then a nitride on the sidewalls of the wordlines.
Claims 9-14 are allowed as being properly dependent upon allowed claim 8.

Claim 19 recites, “A memory device comprising:

a plurality of lines of memory cell stacks, each line comprising a plurality of memory
cells and a tungsten word line, individual memory cells having a charge storage region,
the lines of memory cell stacks having sidewalls;
silicon oxide that covers the sidewalls of the memory cell stacks;
silicon nitride that covers portions of the silicon oxide that are adjacent to the tungsten
word lines; and
word line air gaps between neighboring pairs of the plurality of lines of memory cell
stacks, the word line air gaps being adjacent to portions of the silicon oxide that is
adjacent to the charge storage regions.”

This is not taught or suggested by the prior art of record. Kim (US 2015/0318296) covers the charge storage area with the gate dielectric which is not an oxide and does not place an oxide on the sidewalls. Purayath (US 8,492,224) does not teach or suggest an oxide and then a nitride on the sidewalls of the wordlines. Lue (US 2015/0340371) does not teach or suggest an oxide and then a nitride on the sidewalls of the wordlines. Claims 20-23 are allowed as being properly dependent upon allowed claim 19.

Claim 24 recites, "A method of forming a memory device, the method comprising:
forming a plurality of lines of memory cells, the memory cells comprising:
a charge storage region having sidewalls; and
a control gate;
forming a plurality of word lines each having sidewalls, each of the word lines being associated with a line of the memory cells, each of the word lines being coupled to the control gates of the memory cells with which it is associated;
forming first oxide regions that cover the sidewalls of the charge storage regions;
forming second oxide regions that cover the sidewalls of the word lines;
forming nitride regions that cover the second oxide regions; and
forming electrical isolation regions other than silicon nitride adjacent to the first oxide regions that cover the sidewalls of the charge storage regions.

This is not taught or suggested by the prior art of record. Kim (US 2015/0318296) covers the charge storage area with the gate dielectric which is not an oxide and does

not form an oxide on the sidewalls. Purayath (US 8,492,224) does not teach or suggest forming an oxide and then a nitride on the sidewalls of the wordlines. Lue (US 2015/0340371) does not teach or suggest forming an oxide and then a nitride on the sidewalls of the wordlines.

Claims 25-30 are allowed as being properly dependent upon allowed claim 24.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to David S. Blum whose telephone number is (571)-272-1687) and e-mail address is David.blum@USPTO.gov .

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, William Kraig, can be reached at (571)-272-8660. Our facsimile number all patent correspondence to be entered into an application is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/David S Blum/

Primary Examiner, Art Unit 2813

January 12, 2016

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	0	"14511834"	US-PGPUB; USPAT	ADJ	ON	2015/12/21 13:46
L2	5	("4971655" "6734097" "7821059" "8449942" "8492224").PN.	US-PGPUB; USPAT	ADJ	ON	2015/12/21 13:47
L3	2	L2 and ((charge adj storage) same oxide and nitride)	US-PGPUB; USPAT	ADJ	ON	2015/12/21 13:52
L4	2097	memory and (charge adj storage) and ((word adj line) same oxide same nitride)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2015/12/21 14:06
L5	5549	"L8" and isolation	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2015/12/21 14:07
L6	1336	L4 and isolation	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2015/12/21 14:07
L7	42	L6 and (air adj gap)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2015/12/21 14:16
L8	1497	(Takashi near2 Kashimura).in. or (Xiaolong near2 Hu).in. or (Sayako near2 Nagamine).in. or (Yusuke near2 Yoshida).in. or (Hiroaki near2 Iuchi).in. or (Akira near2 Nakada).in. or (Kazutaka near2 Yoshizawa).in.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2015/12/21 15:11
L9	162	L8 and memory	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2015/12/21 15:11
L10	4108	SanDisk adj Technologies	US-PGPUB; USPAT;	ADJ	ON	2015/12/21 15:20

			USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB			
L11	3696	L10 and memory	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2015/12/21 15:21
L12	833	L11 and (charge adj storage)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2015/12/21 15:22
L13	1633	H01L27/1157.cpc.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2015/12/21 15:52
L14	5787	H01L27/11524.cpc.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2015/12/21 15:53
L15	3474	(257/324).OCLS.	US-PGPUB; USPAT	OR	OFF	2015/12/21 15:54
L16	3312	L15 not L13	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2015/12/21 15:55
L17	5006	L14 not L15 not L13	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2015/12/21 15:55

EAST Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L18	2063	memory and (charge adj storage) and ((word adj line) same oxide same nitride)	US-PGPUB; USPAT	ADJ	ON	2015/12/21 15:56

12/ 21/ 2015 3:57:04 PM

Search Notes 	Application/Control No. 14511834	Applicant(s)/Patent Under Reexamination KASHIMURA ET AL.
	Examiner DAVID S BLUM	Art Unit 2813

CPC- SEARCHED		
Symbol	Date	Examiner
H01L 27/1157, 27/11524	12/21/15	DSB

CPC COMBINATION SETS - SEARCHED		
Symbol	Date	Examiner
12/22/15		

US CLASSIFICATION SEARCHED			
Class	Subclass	Date	Examiner
257	324	12/21/15	DSB
438	257	12/22/15	DSB

SEARCH NOTES		
Search Notes	Date	Examiner
EAST (attached)	12/21/15	DSB
Inventor name search	12/21/15	DSB
Company name search	12/21/15	DSB

INTERFERENCE SEARCH			
US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner
H01L	27/1157, 27/11524	12/21/15	DSB
257	324	12/21/15	DSB
438	257	12/22/15	DSB

	/DAVID S BLUM/ Primary Examiner.Art Unit 2813
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BIB DATA SHEET

CONFIRMATION NO. 8559

SERIAL NUMBER	FILING or 371(c) DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.		
14/511,834	10/10/2014	257	2813	SAND-01720US0		
APPLICANTS SanDisk Technologies Inc., Plano, TX;						
INVENTORS Takashi Kashimura, Yokkaichi-shi, JAPAN; Xiaolong Hu, Yokkaichi-shi, JAPAN; Sayako Nagamine, Yokkaichi-shi, JAPAN; Yusuke Yoshida, Yokkaichi-shi, JAPAN; Hiroaki Iuchi, Nagoya-shi, JAPAN; Akira Nakada, Yokkaichi-shi, JAPAN; Kazutaka Yoshizawa, Kuwana-shi, JAPAN;						
** CONTINUING DATA *****						
** FOREIGN APPLICATIONS *****						
** IF REQUIRED, FOREIGN FILING LICENSE GRANTED ** 10/16/2014						
Foreign Priority claimed ☐ Yes ☒ No 35 USC 119(a-d) conditions met ☐ Yes ☒ No Verified and /DAVID S BLUM/ Acknowledged Examiner's Signature		☐ Met after Allowance Initials	STATE OR COUNTRY JAPAN	SHEETS DRAWINGS 16	TOTAL CLAIMS 21	INDEPENDENT CLAIMS 4
ADDRESS VIERRA MAGEN/SANDISK CORPORATION 575 MARKET STREET SUITE 3750 SAN FRANCISCO, CA 94105 UNITED STATES						
TITLE Non-Volatile Storage Having Oxide/Nitride Sidewall						
FILING FEE RECEIVED 2100	FEES: Authority has been given in Paper No. _____ to charge/credit DEPOSIT ACCOUNT No. _____ for following:			☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit		

Receipt date: 10/10/2014

Doc code: IDS

Doc description: Information Disclosure Statement (IDS) Filed

PTO/SB/08a (01-10)

Approved for use through 07/31/2012. OMB 0651-0031

U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number		14/511834
	Filing Date		2014-10-10
	First Named Inventor	Takashi Kashimura	
	Art Unit	2813	
	Examiner Name	Blum	
	Attorney Docket Number	SAND-01720US0	

U.S.PATENTS						Remove
Examiner Initial*	Cite No	Patent Number	Kind Code ¹	Issue Date	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines where Relevant Passages or Relevant Figures Appear
	1	4971655		1990-11-20	Stefano et al.	
	2	6734097		2004-05-11	Iggulden et al.	
	3	7821059		2010-10-26	Shingu et al.	
	4	8449942		2013-05-28	Liang et al.	
	5	8492224		2013-07-23	Purayath et al.	
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Examiner Initial*	Cite No	Publication Number	Kind Code ¹	Publication Date	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines where Relevant Passages or Relevant Figures Appear
	1					
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ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /D.B./

Receipt date: 10/10/2014 INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number		14/511834	
	Filing Date		2014-10-10	
	First Named Inventor	Takashi Kashimura		
	Art Unit	2813		
	Examiner Name	Blum		
	Attorney Docket Number	SAND-01720US0		

Examiner Initial*	Cite No	Foreign Document Number ³	Country Code ² i	Kind Code ⁴	Publication Date	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines where Relevant Passages or Relevant Figures Appear	T ⁵
	1							☐

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NON-PATENT LITERATURE DOCUMENTS

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Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T ⁵
	1		☐

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EXAMINER SIGNATURE

Examiner Signature	/David S. Blum/	Date Considered	12/21/2015
--------------------	-----------------	-----------------	------------

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

¹ See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. ² Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). ³ For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁴ Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. ⁵ Applicant is to place a check mark here if English language translation is attached.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /D.B./

Electronic Patent Application Fee Transmittal

Application Number:	14511834			
Filing Date:	10-Oct-2014			
Title of Invention:	Non-Volatile Storage Having Oxide/Nitride Sidewall			
First Named Inventor/Applicant Name:	Takashi Kashimura			
Filer:	Ronald Mark Pomerence/Wendy Goy			
Attorney Docket Number:	SAND-01720US0			
Filed as Large Entity				
Filing Fees for Utility under 35 USC 111(a)				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Utility Appl Issue Fee	1501	1	960	960

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Extension-of-Time:				
Miscellaneous:				
Total in USD (\$)				960

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: **Mail** Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or **Fax** (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

64948 7590 01/15/2016
VIERRA MAGEN/SANDISK CORPORATION
575 MARKET STREET
SUITE 3750
SAN FRANCISCO, CA 94105

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/511,834	10/10/2014	Takashi Kashimura	SAND-01720US0	8559

TITLE OF INVENTION: Non-Volatile Storage Having Oxide/Nitride Sidewall

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	\$960	\$0	\$0	\$960	04/15/2016

EXAMINER	ART UNIT	CLASS-SUBCLASS
BLUM, DAVID S	2813	257-316000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

- ☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
- ☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

- (1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
- (2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 Vierra Magen Marcus LLP

2 _____

3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

SanDisk Technologies Inc.

Plano, TX

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☒ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:

- ☒ Issue Fee
- ☐ Publication Fee (No small entity discount permitted)
- ☐ Advance Order - # of Copies _____

4b. Payment of Fee(s): (Please first reapply any previously paid issue fee shown above)

- ☐ A check is enclosed.
- ☐ Payment by credit card. Form PTO-2038 is attached.
- ☒ The director is hereby authorized to charge the required fee(s), any deficiency, or credits any overpayment, to Deposit Account Number 501826 (enclose an extra copy of this form).

5. Change in Entity Status (from status indicated above)

- ☐ Applicant certifying micro entity status. See 37 CFR 1.29
- ☐ Applicant asserting small entity status. See 37 CFR 1.27
- ☐ Applicant changing to regular undiscounted fee status.

NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.

NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.

NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature /RonaldMPomerence#43009/

Date 2/1/16

Typed or printed name Ronald M. Pomerence

Registration No. 43009

Electronic Acknowledgement Receipt

EFS ID:	24779481
Application Number:	14511834
International Application Number:	
Confirmation Number:	8559
Title of Invention:	Non-Volatile Storage Having Oxide/Nitride Sidewall
First Named Inventor/Applicant Name:	Takashi Kashimura
Customer Number:	64948
Filer:	Ronald Mark Pomerence
Filer Authorized By:	
Attorney Docket Number:	SAND-01720US0
Receipt Date:	01-FEB-2016
Filing Date:	10-OCT-2014
Time Stamp:	15:56:51
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Credit Card
Payment was successfully received in RAM	\$ 960
RAM confirmation Number	2540
Deposit Account	
Authorized User	

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

File Listing:					
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Issue Fee Payment (PTO-85B)	1720-IssueFeeTrans.pdf	230664	no	1
			92afa27395b99d82d102b2ee5e8dffbb2ae4dee5		
Warnings:					
Information:					
2	Fee Worksheet (SB06)	fee-info.pdf	30936	no	2
			77da5521de1b31671dbc7135a95ba0076cc4f0ea		
Warnings:					
Information:					
Total Files Size (in bytes):			261600		
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. <u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. <u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. <u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.					



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APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/511,834	03/08/2016	9281314	SAND-01720US0	8559

64948 7590 02/17/2016

VIERRA MAGEN/SANDISK CORPORATION
575 MARKET STREET
SUITE 3750
SAN FRANCISCO, CA 94105

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (application filed on or after May 29, 2000)

The Patent Term Adjustment is 0 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (<http://pair.uspto.gov>).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Data Management (ODM) at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site <http://pair.uspto.gov> for additional applicants):

Takashi Kashimura, Yokkaichi-shi, JAPAN;
SanDisk Technologies Inc., Plano, TX;
Xiaolong Hu, Yokkaichi-shi, JAPAN;
Sayako Nagamine, Yokkaichi-shi, JAPAN;
Yusuke Yoshida, Yokkaichi-shi, JAPAN;
Hiroaki Iuchi, Nagoya-shi, JAPAN;
Akira Nakada, Yokkaichi-shi, JAPAN;
Kazutaka Yoshizawa, Kuwana-shi, JAPAN;

The United States represents the largest, most dynamic marketplace in the world and is an unparalleled location for business investment, innovation, and commercialization of new technologies. The USA offers tremendous resources and advantages for those who invest and manufacture goods here. Through SelectUSA, our nation works to encourage and facilitate business investment. To learn more about why the USA is the best country in the world to develop technology, manufacture products, and grow your business, visit SelectUSA.gov.

PATENT ASSIGNMENT COVER SHEET

Electronic Version v1.1
Stylesheet Version v1.2

Assignment ID: PATI432478

SUBMISSION TYPE:	NEW ASSIGNMENT	
NATURE OF CONVEYANCE:	ASSIGNMENT	
CONVEYING PARTY DATA		
Name		Execution Date
SanDisk Technologies LLC		08/12/2024
RECEIVING PARTY DATA		
Company Name:	Palisade Technologies, LLP	
Street Address:	1468 James Rd.	
City:	Gardnerville	
State/Country:	NEVADA	
Postal Code:	89460	
PROPERTY NUMBERS Total: 14		
Property Type	Number	
Patent Number:	9530716	
Patent Number:	8148962	
Patent Number:	9501398	
Patent Number:	9448876	
Patent Number:	9454448	
Patent Number:	8327051	
Patent Number:	9466383	
Patent Number:	9281314	
Patent Number:	8996838	
Patent Number:	9373408	
Patent Number:	9524974	
Patent Number:	9349458	
Patent Number:	7743258	
Patent Number:	8135961	
CORRESPONDENCE DATA		
Fax Number:		
<i>Correspondence will be sent to the e-mail address first; if that is unsuccessful, it will be sent using a fax number, if provided; if that is unsuccessful, it will be sent via US Mail.</i>		
Phone:	3129194254	
Email:	dave@gerasimowlaw.com	

Correspondent Name:	David Gerasimow
Address Line 1:	FL3 PMB1717
Address Line 2:	211 W Wacker Dr
Address Line 4:	Chicago, ILLINOIS 60606
NAME OF SUBMITTER:	David Gerasimow
SIGNATURE:	David Gerasimow
DATE SIGNED:	08/15/2024
	This document serves as an Oath/Declaration (37 CFR 1.63).
Total Attachments: 2 source=SDTL Palisade Assignment#page1.tiff source=SDTL Palisade Assignment#page2.tiff	

SDTL PALISADE ASSIGNMENT

For good and valuable consideration, the receipt of which is hereby acknowledged, **SanDisk Technologies LLC**, with a registered address at 7501 N Capital of Texas Hwy, Building A, Suite #100, Austin, TX 78731, ("Assignor"), does hereby assign, transfer and convey unto **Palisade Technologies, LLP**, with an office at 1468 James Rd., Gardnerville, NV 89460, USA, ("Assignee"), all of Assignor's entire right, title and interest in and to all patents and patent applications listed in the attached Schedule A (collectively "Patent Rights").

In addition, Assignor agrees to and hereby does sell, assign, transfer and convey unto Assignee all rights (i) in and to causes of action and enforcement rights for the Patent Rights including all rights to pursue damages, injunctive relief and other remedies for past, present and future infringement of the Patent Rights, (ii) the right to apply (or continue prosecution) in any and all countries of the world for patents, design patents, utility models, certificates of invention or other governmental grants for the Patent Rights, including under the Paris Convention for the Protection of Industrial Property, the International Patent Cooperation Treaty, or any other convention, treaty, agreement or understanding, and (iii) the rights, if any, to revive prosecution of any abandoned Patent Rights.

Assignor also hereby authorizes the respective patent office or governmental agency in each jurisdiction to issue any and all patents or certificates of invention or equivalent which may be granted upon any of the Patent Rights in the name of Assignee, as the assignee to the entire interest therein.

The terms and conditions of this Assignment shall inure to the benefit of Assignee, its successors, assigns and other legal representatives, and shall be binding upon Assignor, its successor, assigns and other legal representatives.

This assignment is made effective as of: August 7, 2024.

IN WITNESS WHEREOF, this Assignment of Patent Rights is executed at Sandy, UT, USA
on 8/12/24.

ASSIGNOR SanDisk Technologies LLC,

By:

Name: David Dutcher

Title: VP, Chief IP and Licensing Counsel

STATE OF Utah)
COUNTY OF Salt Lake) ss.

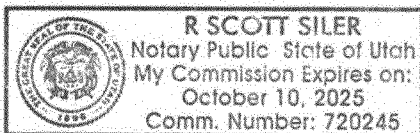
On 08-12-2024 before me,

R. Scott Siler Notary Public

Personally appeared David Dutcher, who proved to me on the basis of satisfactory evidence to be the person whose name is subscribed to the within instrument and acknowledged to me that she executed the same in her authorized capacity, and that by her signature on the instrument the person, or the entity upon behalf of which the person acted, executed the instrument.

I certify under PENALTY OF PERJURY under the laws of the State of Utah that the foregoing paragraph is true and correct.

WITNESS my hand and official seal.



R. Scott Siler
Notary Public

SCHEDULE TO ASSIGNMENT

Country	Patent/Publication Number	Application Number
US	9,530,716	13/452,767
KR	10-1774059	2011-7028490
US	8,148,962	12/464,301
CN	ZL201380072287.2	201380072287.2
US	9,501,398	13/831,218
US	9,448,876	14/454,667
US	9,454,448	14/454,672
US	8,327,051	11/986,389
US	9,466,383	14/144,056
US	9,281,314	14/511,834
US	8,996,838	14/273,031
TW	TW201606496	104112604
CN	ZL201510626779.2	201510626779.2
DE	102015116905	102015116905.3
US	9,373,408	14/508,274
US	9,524,974	14/806,111
US	9,349,458	14/515,762
US	7,743,258	11/511,766
US	8,135,961	12/760,359

UNITED STATES
PATENT AND TRADEMARK OFFICEP.O. Box 1450
Alexandria, VA 22313 - 1450
www.uspto.gov**ELECTRONIC ACKNOWLEDGEMENT RECEIPT**APPLICATION #
14/511,834RECEIPT DATE / TIME
08/29/2024 04:31:14 PM Z ETATTORNEY DOCKET #
SAND-01720USO**Title of Invention**

Non-Volatile Storage Having Oxide/Nitride Sidewall

Application InformationAPPLICATION TYPE Utility - Nonprovisional Application
under 35 USC 111(a)

PATENT # 9281314

CONFIRMATION # 8559

FILED BY David Gerasimow

PATENT CENTER # 66982497

FILING DATE 10/10/2014

CUSTOMER # 64948

FIRST NAMED
INVENTOR Takashi KashimuraCORRESPONDENCE
ADDRESS -

AUTHORIZED BY -

Documents**TOTAL DOCUMENTS: 2**

DOCUMENT	PAGES	DESCRIPTION	SIZE (KB)
POA9281314.pdf	2	Power of Attorney	265 KB
Warning: The PDF file has been signed with a digital signature and the legal effect of the document will be based on the contents of the file not the digital signature.			
POA9281314 3.73c.pdf	3	Assignee showing of ownership per 37 CFR 3.73	119 KB

Digest

DOCUMENT	MESSAGE DIGEST(SHA-512)
POA9281314.pdf	FBC71906849ED13B2E0F3C9485C5DEAD5B572DA6498E4AF8 A8F114AD140701C81208203C1C26BCB95A3249C6C6F9B9489 4E418390DEC2935DE01970074ED9C29

POA9281314 3.73c.pdf

DFDDC149DD84FB74242923B77457506D0A58A06EE119B4054
6FB44FE3ACAB8730AACC281BF6C43CD536C3890F936A9218
1BF7437E0FE2E9174DA3AF2A072DC7B

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

STATEMENT UNDER 37 CFR 3.73(c)Applicant/Patent Owner: PALISADE TECHNOLOGIES, LLPApplication No./Patent No.: 9281314Filed/Issue Date: 3/8/2016Titled: NON-VOLATILE STORAGE HAVING OXIDE/NITRIDE SIDEWALLPALISADE TECHNOLOGIES, LLP, a LIMITED LIABILITY PARTNERSHIP

(Name of Assignee)

(Type of Assignee, e.g., corporation, partnership, university, government agency, etc.)

states that, for the patent application/patent identified above, it is (choose one of options 1, 2, 3 or 4 below):

1. ☒ The assignee of the entire right, title, and interest.
2. ☐ An assignee of less than the entire right, title, and interest (check applicable box):
- ☐ The extent (by percentage) of its ownership interest is _____%. Additional Statement(s) by the owners holding the balance of the interest must be submitted to account for 100% of the ownership interest.
- ☐ There are unspecified percentages of ownership. The other parties, including inventors, who together own the entire right, title and interest are:

Additional Statement(s) by the owner(s) holding the balance of the interest must be submitted to account for the entire right, title, and interest.

3. ☐ The assignee of an undivided interest in the entirety (a complete assignment from one of the joint inventors was made). The other parties, including inventors, who together own the entire right, title, and interest are:

Additional Statement(s) by the owner(s) holding the balance of the interest must be submitted to account for the entire right, title, and interest.

4. ☐ The recipient, via a court proceeding or the like (e.g., bankruptcy, probate), of an undivided interest in the entirety (a complete transfer of ownership interest was made). The certified document(s) showing the transfer is attached.

The interest identified in option 1, 2 or 3 above (not option 4) is evidenced by either (choose one of options A or B below):

- A. ☐ An assignment from the inventor(s) of the patent application/patent identified above. The assignment was recorded in the United States Patent and Trademark Office at Reel _____, Frame _____, or for which a copy thereof is attached.
- B. ☒ A chain of title from the inventor(s), of the patent application/patent identified above, to the current assignee as follows:

1. From: TAKASHI KASHIMURA, ET AL. To: SANDISK TECHNOLOGIES INC.The document was recorded in the United States Patent and Trademark Office at
Reel 033936, Frame 0058, or for which a copy thereof is attached.2. From: SANDISK TECHNOLOGIES INC. To: SANDISK TECHNOLOGIES LLCThe document was recorded in the United States Patent and Trademark Office at
Reel 038807, Frame 0948, or for which a copy thereof is attached.

[Page 1 of 2]

This collection of information is required by 37 CFR 3.73(b). The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

STATEMENT UNDER 37 CFR 3.73(c)3. From: SANDISK TECHNOLOGIES LLC To: PALISADE TECHNOLOGIES, LLP

The document was recorded in the United States Patent and Trademark Office at
 Reel 068301, Frame 0100, or for which a copy thereof is attached.

4. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at
 Reel _____, Frame _____, or for which a copy thereof is attached.

5. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at
 Reel _____, Frame _____, or for which a copy thereof is attached.

6. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at
 Reel _____, Frame _____, or for which a copy thereof is attached.

☐ Additional documents in the chain of title are listed on a supplemental sheet(s).

☒ As required by 37 CFR 3.73(c)(1)(i), the documentary evidence of the chain of title from the original owner to the assignee was, or concurrently is being, submitted for recordation pursuant to 37 CFR 3.11.

[NOTE: A separate copy (i.e., a true copy of the original assignment document(s)) must be submitted to Assignment Division in accordance with 37 CFR Part 3, to record the assignment in the records of the USPTO. See MPEP 302.08]

The undersigned (whose title is supplied below) is authorized to act on behalf of the assignee.

/David Gerasimow/

Signature

David Gerasimow

Printed or Typed Name

08-29-2024

Date

57,512

Title or Registration Number

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Under the Paperwork Reduction Act of 1995 no persons are required to respond to a collection of information unless it displays a valid OMB control number

PATENT - POWER OF ATTORNEY OR REVOCATION OF POWER OF ATTORNEY WITH A NEW POWER OF ATTORNEY AND CHANGE OF CORRESPONDENCE ADDRESS	Patent Number	9281314
	Issue Date	03/08/2016
	First Named Inventor	Takashi KASHIMURA
	Title	Non-volatile storage having oxide/nitride sidewall
	Attorney Docket No.	9062-0014

I hereby revoke all previous powers of attorney given in the above-identified patent.

☐ A Power of Attorney is submitted herewith.

OR

☒ I hereby appoint Practitioner(s) associated with the Customer Number identified in the box at right as my/our attorney(s) or agent(s) with respect to the patent identified above, and to transact all business in the United States Patent and Trademark Office connected therewith:

174899

OR

☐ I hereby appoint Practitioner(s) named below as my/our attorney(s) or agent(s) with respect to the patent identified above, and to transact all business in the United States Patent and Trademark Office connected therewith:

Practitioner(s) Name	Registration Number

Please recognize or change the correspondence address for the above-identified patent to:

☒ The address associated with the above-identified Customer Number.

OR

☐ The address associated with the Customer Number identified in the box at right:

OR

☐ Firm or
Individual Name

Address

City

State

Zip

Country

Telephone

Email

I am the:

☐ Applicant.

OR

☒ Patent owner.

Statement under 37 CFR 1.95(c) (Form PTO/AIA/96) submitted herewith or filed on _____.

Signature	<i>Peter Hardigan</i>	SIGNATURE of Applicant or Patent Owner	8/29/2024
Name	Peter Hardigan	Date	
Title and Company	Manager, Palisade Technologies, LLP	Telephone	(917) 622-0926

NOTE: Signatures of all the applicants or patent owners of the entire interest or their representative(s) are required. If more than one signature is required, submit multiple forms, check the box below, and identify the total number of forms submitted in the blank below.

☐ A total of _____ forms are submitted.

This collection of information is required by 37 CFR 1.31, 1.32, and 1.33. The information is required to obtain or retain a benefit by the public, which is to update (and by the USPTO to process) the file of a patent or reexamination proceeding. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
14/511,834	10/10/2014	Takashi Kashimura	SAND-01720US0

CONFIRMATION NO. 8559

64948
VIERRA MAGEN/WESTERN DIGITAL
4104 24th Street, Suite 390
San Francisco, CA 94114

POWER OF ATTORNEY NOTICE



OC000000077831254

Date Mailed: 09/13/2024

NOTICE REGARDING CHANGE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 08/29/2024.

- The Power of Attorney to you in this application has been revoked by the assignee who has intervened as provided by 37 CFR 3.71. Future correspondence will be mailed to the new address of record(37 CFR 1.33).

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at (571) 272-4000 or (571) 272-4200 or 1-888-786-0101.

/ytdemisse/



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
14/511,834	10/10/2014	Takashi Kashimura	9062-0014

CONFIRMATION NO. 8559

POA ACCEPTANCE LETTER



OC00000077831299

174899
The Law Offices of David A. Gerasimow, P.C.
211 W. Wacker Dr.
Ste. 1717
Chicago, IL 60606

Date Mailed: 09/13/2024

NOTICE OF ACCEPTANCE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 08/29/2024.

The Power of Attorney in this application is accepted. Correspondence in this application will be mailed to the above address as provided by 37 CFR 1.33.

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at (571) 272-4000 or (571) 272-4200 or 1-888-786-0101.

/ytdemisse/