

Ex-1020: U.S. Patent No. 9,281,314 Claim Comparison Table

1[preamble]: A memory device comprising:	13[preamble]: A method of forming a memory device, the method comprising:
1[a]: a plurality of lines of memory cells, the memory cells comprising:	13[a]: forming a plurality of lines of memory cells, the memory cells comprising:
1[a1]: a charge storage region having sidewalls; and	13[a1]: a charge storage region having sidewalls; and
1[a2]: a control gate;	13[a2]: a control gate;
1[b]: a plurality of word lines each having sidewalls, each of the word lines being associated with a line of the memory cells, each of the word lines being coupled to the control gates of the memory cells with which it is associated;	13[b]: forming a plurality of word lines each having sidewalls, each of the word lines being associated with a line of the memory cells, each of the word lines being coupled to the control gates of the memory cells with which it is associated;
1[c]: first oxide regions that cover the sidewalls of the charge storage regions;	13[c]: forming first oxide regions that cover the sidewalls of the charge storage regions;
1[d]: second oxide regions that cover the sidewalls of the word lines;	13[d]: forming second oxide regions that cover the sidewalls of the word lines;
1[e]: nitride regions that cover the second oxide regions; and	13[e]: forming nitride regions that cover the second oxide regions; and
1[f]: electrical isolation regions other than silicon nitride adjacent to the first oxide regions that cover the sidewalls of the charge storage regions	13[f]: forming electrical isolation regions other than silicon nitride adjacent to the first oxide regions that cover the sidewalls of the charge storage regions.
2. The memory device of claim 1, wherein the electrical isolation regions comprise: a plurality of air gaps, each air gap between a neighboring pair of the plurality of word lines, the air gaps being adjacent to first oxide regions.	14. The method of claim 13, wherein forming the electrical isolation regions comprises: forming air gaps between adjacent pairs of the plurality of word lines, a portion of the air gaps being adjacent to the oxide that covers the sidewalls of the charge storage regions.
3. The memory device of claim 1, wherein the word lines comprise tungsten.	17. The method of claim 13, wherein forming the plurality of word lines comprises forming the plurality of word lines from tungsten.
4. The memory device of claim 1, wherein the charge storage region is a conductive floating gate.	19. The method of claim 13, wherein forming the plurality of lines of memory cells comprises forming the charge storage regions comprising a conductive floating gate.

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5. The memory device of claim 1, wherein the charge storage region is a dielectric charge trapping region.	18. The method of claim 13, wherein forming the plurality of lines of memory cells comprises forming the charge storage regions comprising a dielectric charge trapping region.
6. The memory device of claim 1, further comprising peripheral circuitry, wherein the word lines are electrically coupled to the peripheral circuitry.	
7. The memory device of claim 1, wherein the first oxide regions and the second oxide regions comprise silicon oxide and the nitride regions comprise silicon nitride.	