UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC. and
MICRON SEMICONDUCTOR PRODUCTS, INC.,
Petitioner

v.

PALISADE TECHNOLOGIES, LLP,
Patent Owner.

Case No. IPR2025-01009
U.S. Patent No. 9,281,314

PETITIONER'S UPDATED LIST OF EXHIBITS

LIST OF EXHIBITS[1]

Ex-1001	U.S. Patent No. 9,281,314 ("the '314 Patent")
Ex-1002	Declaration of Dr. David Kuan-Yu Liu
Ex-1003	Curriculum Vitae of Dr. David Kuan-Yu Liu
Ex-1004	Prosecution History of U.S. Patent No. 9,281,314 (App. No. 14/511,834)
Ex-1005	U.S. Patent No. 7,598,564 ("Kang")
Ex-1006	U.S. Patent App. Pub. No. 2007/0096202 ("Kang-1")
Ex-1007	U.S. Patent App. Pub. No. 2011/0309425 ("Purayath")
Ex-1008	U.S. Patent No. 7,759,722 ("Murata")
Ex-1009	[Intentionally left blank]
Ex-1010	[Intentionally left blank]
Ex-1011	[Intentionally left blank]
Ex-1012	[Intentionally left blank]
Ex-1013	[Intentionally left blank]
Ex-1014	[Intentionally left blank]
Ex-1015	[Intentionally left blank]
Ex-1016	[Intentionally left blank]
Ex-1017	[Intentionally left blank]
Ex-1018	[Intentionally left blank]
Ex-1019	[Intentionally left blank]
Ex-1020	Claim Mapping Table
Ex-1021	Rino Micheloni et al., *Inside NAND Flash Memories* (2010)
Ex-1022	Complaint, *Palisade Techs, LLP v. Micron Tech., Inc. and Micron Semiconductor Prods., Inc.*, No. 7:24-cv-00262 (W.D. Tex. Oct. 16, 2024), ECF No. 1
Ex-1023	First Amended Complaint, *Palisade Techs, LLP v. Micron Tech., Inc. and Micron Semiconductor Prods., Inc.*, No. 7:24-cv-00262 (W.D. Tex. Dec. 19, 2024), ECF No. 20
Ex-1024	G. Groeseneken et al., *Basics of Nonvolatile Semiconductor Memory Devices, in Nonvolatile Semiconductor Memory Technology: A Comprehensive Guide to Understanding and Using NVSM Devices* (William D. Brown & Joe Brewer eds., 1997)
Ex-1025	S. Ahn et al., *Influence of the Oxidation in the Metal Silicide/Si3N4*

[1] Four-digit pin citations that begin with 0 are the page stamps added by Micron in the bottom right corner of the exhibits. All other pin citations are to original page, column, paragraph, or line numbers.

	Interfaces on the Etching Profile, 77 Microelectronic Eng'g 8 (2005)
Ex-1026	T. Mikolajick et al., *The Future of Charge Trapping Memories*, 2007 IEEE Int'l Symposium on VLSI Tech., Sys. & Applications (2007)
Ex-1027	U.S. Patent No. 9,589,978 ("Yip")
Ex-1028	Seiichi Aritome, *NAND Flash Memory Technologies* (2016)
Ex-1029	Jim Handy, *3D NAND: Benefits of Charge Traps over Floating Gates*, The Memory Guy Blog (Nov. 22, 2013)
Ex-1030	U.S. Patent No. 6,859,397 ("Lutze")
Ex-1031	Silicon Processing for the VLSI Era, Volume 1: Process Technology (2d ed.)
Ex-1032	Mincheol Park et al., *Effect of low-k dielectric material on 63nm MLC (multi-level cell) NAND flash cell arrays*, IEEE VLSI-TSA International Symposium on VLSI Technology (2005)
Ex-1033	Daewoong Kang et al., *The Air Spacer Technology for Improving the Cell Distribution in 1 Giga Bit NAND Flash Memory*, 21st IEEE Non-Volatile Semiconductor Memory Workshop (2006)
Ex-1034	Notice of Defendants' Stipulation Regarding Invalidity Challenges, *Palisade Techs., LLP v. Micron Tech., Inc. et al*, No. 7:24-cv-00262-DC-DTG (E.D. Tex. 2024), ECF No. 74.

Respectfully submitted,

Dated: August 13, 2025

By: */s/ John Kappos*
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CERTIFICATE OF SERVICE

I hereby certify that on August 13, 2025, I caused a true and correct copy of the foregoing PETITIONER'S UPDATED LIST OF EXHIBITS was served in its entirety by filing these documents through the PTAB P-TACTS System, as well as by email, on the counsel of record for the Patent Owner:

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