**IN THE UNITED STATES DISTRICT COURT**
**FOR THE WESTERN DISTRICT OF TEXAS**
**MIDLAND DIVISION**

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| PALISADE TECHNOLOGIES, LLP,<br><br>Plaintiff,<br><br>v.<br><br>MICRON TECHNOLOGY, INC., MICRON SEMICONDUCTOR PRODUCTS, INC., AND MICRON TECHNOLOGY TEXAS LLC,<br><br>Defendants. | §<br>§<br>§<br>§<br>§<br>§<br>§<br>§<br>§<br>§<br>§<br>§<br>§<br>§<br>§ | CIVIL ACTION NO. 7:24-cv-00262<br><br>**JURY TRIAL DEMANDED** |

**PLAINTIFF'S COMPLAINT FOR PATENT INFRINGEMENT**

Plaintiff Palisade Technologies, LLP ("Palisade") files this Complaint against Defendants Micron Technology, Inc., Micron Semiconductor Products, Inc., and Micron Technology Texas LLC (collectively "Micron" or "Defendants") and alleges as follows:

**NATURE OF THE ACTION**

1. This is a civil action for patent infringement (hereinafter the "Action"), brought under the patent laws of the United States, 35 U.S.C. § 1 et seq., seeking damages and other relief arising out of Defendants' infringement of United States Patent Nos. 8,148,962 ("'962 patent"); 8,996,838 ("'838 patent"); 8,327,051 ("'051 patent"); 9,281,314 ("'314 patent"); and 9,524,974 ("'974 patent") (collectively, the "Asserted Patents"). Palisade owns the entire right, title, and interest in and to each of the Asserted Patents.

2. Palisade asserts that Defendants infringe each Asserted Patent by, without Palisade's authorization, making, using, offering to sell, and selling in, and/or importing into the

United States certain semiconductor memory devices, including DRAM and NAND flash memory devices.

**THE PARTIES**

3. Plaintiff Palisade is a corporation organized and existing under the laws of Nevada, with its principal place of business in Gardnerville, Nevada.

4. On information and belief, Defendant Micron Technology Inc. ("MTI") is a corporation organized and existing under the laws of the State of Delaware. MTI is registered to do business in Texas. MTI has a regular and established place of business located at 101 West Louis Henna Boulevard, Suite 210, Austin, Texas 78728. *See, e.g.*, https://www.micron.com/about/locations. MTI can be served with process through its registered agent for service of process, Corporation Service Company, at 211 E. 7th Street, Suite 620, Austin, Texas 78701-3128.

5. On information and belief, Defendant Micron Semiconductor Products, Inc. ("MSP") is a corporation organized and existing under the laws of the State of Idaho. MSP is registered to do business in the State of Texas. MSP has a regular and established place of business located at 101 West Louis Henna Boulevard, Suite 210, Austin, Texas 78728. MSP can be served with process through its registered agent of process, Corporation Service Company, at 211 E. 7th Street, Suite 620, Austin, Texas 78701-3128. MSP is a wholly owned subsidiary of MTI. MTI does not separately report revenue from MSP in its public filings submitted to the Securities and Exchange Commission ("SEC").

6. On information and belief, Defendant Micron Technology Texas LLC ("MTT") is a corporation organized and existing under the laws of Idaho. MTT has a regular and established place of business located at 101 West Louis Henna Boulevard, Suite 210, Austin, Texas 78728.

MTT is registered with the Texas Secretary of State to do business in Texas. MTT can be served through its registered agent, The Corporation Service Company, 211 E. 7th Street, Suite 620, Austin, Texas, 78701-3218.

7. On information and belief, MSP and MTT are wholly owned subsidiaries of MTI. MTI does not separately report revenue from Micron Semiconductor or Micron Texas in its filings to the Securities Exchange Commission, but rather reports combined revenue from its various products and subsidiaries.

8. On information and belief, Defendants have semiconductor fabrication plants in the United States and other countries throughout the world and manufacture memory products such as DRAM, NAND Flash, and NOR Flash at those plants. Defendants also use, sell, and offer for sale in the United States, import into the United States and/or export from the United States memory products, including solid state storage devices and memory modules, such as LPDDR5 ("Accused Products"). Defendants have at least imported, advertised, distributed, used, sold, or offered to sell products and services, including the Accused Products, in this judicial district, e.g., through sales and distribution channels managed by MTT.

9. On information and belief, Defendants place, have placed, and contributed to placing Accused Products into the stream of commerce via an established distribution channel knowing or understanding that such products would be sold and used in the United States, including in this judicial district. Defendants have also derived substantial revenues from infringing acts in this judicial district, including from the sale and use of the Accused Products.

## JURISDICTION AND VENUE

10. This is an action for patent infringement arising under the patent laws of the United States, 35 U.S.C. §§ 1, *et seq*. This Court has jurisdiction over this action pursuant to 28 U.S.C. §§ 1331, 1338(a) and 1367.

11. This Court has specific and personal jurisdiction over Micron consistent with the requirements of the Due Process Clause of the United States Constitution and the Texas Long Arm Statute because, *inter alia*, (i) Micron has done and continues to do business in Texas, and (ii) Micron has committed and continues to commit, directly or through intermediaries (including subsidiaries, distributors, affiliates, retailers, suppliers, integrators, customers, and others), acts of patent infringement in this State. Such acts of infringement include making, using, offering to sell, and/or selling Accused Products (as more particularly identified and described throughout this Complaint, below) in this State and this District and/or importing Accused Products into this State and/or inducing others to commit acts of patent infringement in this State. Indeed, Micron has purposefully and voluntarily placed, and is continuing to place, one or more Accused Products into the stream of commerce through established distribution channels (including the Internet) with the expectation and intent that such products will be sold to and purchased by consumers in the United States, this State, and this District; and with the knowledge and expectation that such products (whether in standalone form or as integrated in downstream products) will be imported into the United States, this State, and this District.

12. Micron has derived substantial revenues from its infringing acts occurring within this State and this District. It has substantial business in this State and this District, including: (i) at least part of its infringing activities alleged herein; and (ii) regularly doing or soliciting business, engaging in other persistent conduct, and/or deriving substantial revenue from infringing goods

offered for sale, sold, and imported, and services provided to Texas residents vicariously through and/or in concert with its alter egos, intermediaries, agents, distributors, importers, customers, subsidiaries, and/or consumers.

13. This Court has personal jurisdiction over Micron, Micron regularly conducts business and has committed acts of patent infringement and/or has induced acts of patent infringement by others in this District and/or has contributed to patent infringement by others in this District, the State of Texas, and elsewhere in the United States. Further, this Court has personal jurisdiction over Micron through intermediaries (including subsidiaries, distributors, affiliates, retailers, suppliers, integrators, customers, and others). Through direction and control of such intermediaries, Micron has committed acts of direct and/or indirect patent infringement within this State and elsewhere within the United States giving rise to this action and/or has established minimum contacts with this forum such that the exercise of personal jurisdiction over Micron would not offend traditional notions of fair play and substantial justice.

14. In addition, Micron has knowingly induced, and continues to knowingly induce, infringement within this District by advertising, marketing, offering for sale and/or selling Accused Products (such as solid state storage devices and DRAM memory) that incorporate the fundamental technologies covered by the Asserted Patents. Such advertising, marketing, offering for sale and/or selling of Accused Products is directed to consumers, customers, manufacturers, integrators, suppliers, distributors, resellers, partners, and/or end users, and this includes providing instructions, user manuals, advertising, and/or marketing materials facilitating, directing and/or encouraging use of infringing functionality with Micron's knowledge thereof.

15. Micron has, thus, in the multitude of ways described above, availed itself of the benefits and privileges of conducting business in this State and willingly subjected itself to the

exercise of this Court's personal jurisdiction over it. Indeed, Micron has sufficient minimum contacts with this forum through its transaction of substantial business in this State and this District and its commission of acts of patent infringement as alleged in this Complaint that are purposefully directed towards this State and District.

16. Micron has infringed or caused infringement in Texas, including in this Judicial District, by, among other things, promoting, offering for sale, distributing, and/or selling infringing products. Defendants have various physical locations in Texas, including within this Judicial District, at which Defendants transact business, conduct office and research operations, and recruit and hire employees. For example, Micron tests semiconductor memory devices, including at least NAND memory chips, in Austin, TX. Defendants also have authorized sellers and sales representatives that offer for sale and sell infringing products to consumers at various locations throughout Texas and this Judicial District and Division, including but not limited to: Best Buy at 2511 W Loop 250 N in Midland, TX; Walmart Supercenter at 2450 NW Loop 338 State Rte W, Odessa, TX; and Amazon.com (which delivers infringing products throughout this Judicial District). On information and belief, Defendants intend for customers to use their products within this Judicial District. Therefore, the exercise of jurisdiction over Defendants is appropriate under the applicable jurisdictional statutes and would not offend traditional notions of fair play and substantial justice.

17. Venue is proper in this district for Defendants pursuant to 28 U.S.C. § 1400(b). Each of the Defendants committed and continues to commit acts of patent infringement in this District, including making, using, offering to sell, and/or selling accused products in this District, and/or importing accused products into this District, including by Internet sales and sales via retail and wholesale stores, inducing others to commit acts of patent infringement in Texas, and/or

committing at least a portion of any other infringements alleged herein in this District. Each of the Defendants has a regular and established places of business in this district, including at least at 101 West Louis Henna Boulevard, Suite 210, Austin, Texas 78728. *See, e.g.*, https://www.micron.com/about/locations.

**THE ASSERTED PATENTS**

18. Palisade is the sole and exclusive owner of all right, title, and interest in the ’962 patent, ’838 patent, ’051 patent, ’314 patent, and ’974 patent and holds the exclusive right to take all actions necessary to enforce its rights in, and to, the Asserted Patents, including the filing of this patent infringement lawsuit. Palisade also has the right to recover all damages for past, present, and future infringements of the Asserted Patents and to seek injunctive relief as appropriate under the law.

19. The ’962 patent is titled “Transient Load Voltage Regulator.” The ’962 patent lawfully issued on April 3, 2012, and stems from U.S. Patent Application No. 12/464,301, which was filed on May 12, 2009.

20. The ’838 patent is titled “Structure Variation Detection for a Memory Having a Three-Dimensional Memory Configuration.” The ’838 patent lawfully issued on March 31, 2015, and stems from U.S. Patent Application No. 14/273,031, which was filed on May 8, 2014.

21. The ’051 patent is titled “Portable Handheld Memory Card and Methods for Use Therewith.” The ’051 patent lawfully issued on December 4, 2012, and stems from U.S. Patent Application No. 11/986,389, which was filed on November 20, 2007.

22. The ’314 patent is titled “Non-Volatile Storage Having Oxide/Nitride Sidewall.” The ’314 patent lawfully issued on March 8, 2016, and stems from U.S. Patent Application No. 14/511,834, which was filed on October 10, 2014.

23. The ’974 patent is titled “Alternating Sidewall Assisted Patterning.” The ’974 patent lawfully issued on December 20, 2016, and stems from U.S. Patent Application No. 14/806,111, which was filed on July 22, 2015.

24. Palisade and its predecessors complied with the requirements of 35 U.S.C. § 287, to the extent necessary, such that Palisade may recover pre-suit damages.

25. The claims of the Asserted Patents are directed to patent eligible subject matter under 35 U.S.C. § 101. They are not directed to an abstract idea, and the technologies covered by the claims comprise devices, systems and/or consist of ordered combinations of features and functions that, at the time of invention, were not, alone or in combination, well-understood, routine, or conventional.

**COUNT I**

(INFRINGEMENT OF U.S. PATENT NO. 8,148,962)

26. Plaintiff incorporates the preceding paragraphs herein by reference.

27. This cause of action arises under the patent laws of the United States, and, in particular, 35 U.S.C. §§ 271, *et seq*.

28. Palisade is the owner of all substantial rights, title, and interest in and to the ’962 patent including the right to exclude others and to enforce, sue, and recover damages for past infringements.

29. The ’962 patent is valid, enforceable, and was duly and legally issued by the United States Patent and Trademark Office on April 3, 2012, after full and fair examination.

30. Defendants directly and/or indirectly infringed (by inducing infringement) one or more claims of the ’962 patent in this District and elsewhere in Texas and the United States by making, using, selling, offering to sell, and/or importing, and by actively inducing others to make, use, sell, offer to sell, and/or import products containing voltage regulators, such as DRAM, and/or

products containing the same that incorporate the fundamental technologies covered by the ’962 patent, including, but not limited to, the Micron MT62F1G64D4ZV-026 WT:B (the “’962 Accused Products”).

***Direct Infringement (35 U.S.C. § 271(a))***

31. Defendants directly infringed one or more claims of the ’962 Patent in this District and elsewhere in Texas and the United States.

32. Defendants directly infringed, either by itself or via its agent(s), at least Claim 1 of the ’962 patent[1] as set forth under 35 U.S.C. § 271(a) by making, using, offering for sale, selling, and/or importing the ’962 Accused Products. Furthermore, Defendants made and sold the ’962 Accused Products outside of the United States and either delivered those products to its customers, distributors, and/or subsidiaries in the United States, or, in the case that it delivered the ’962 Accused Products outside of the United States, it did so intending and/or knowing that those products were destined for the United States and/or designed and designated for sale in the United States, thereby directly infringing the ’962 Patent. *See, e.g., Lake Cherokee Hard Drive Techs., L.L.C. v. Marvell Semiconductor, Inc.*, 964 F. Supp. 2d 653, 658 (E.D. Tex. 2013).

33. By way of illustration only, the ’962 Accused Products comprise each and every element of claim 1 of the ’962 patent. On information and belief, the ’962 Accused Products comprise “a voltage regulator circuit integrated in an integrated circuit (IC) and adapted to provide a voltage from a power supply to a load under varying load conditions.” The ’962 Accused Products comprise voltage regulators.

[1] Throughout this Complaint, wherever Palisade identifies specific claims of the Asserted Patents infringed by Defendants, Palisade expressly reserves the right to identify additional claims and products in its infringement contentions in accordance with applicable local rules and the Court’s case management orders. Specifically identified claims throughout this Complaint are provided for notice pleading only.

34. On information and belief, the voltage regulators in the ’962 Accused Products comprise “an input adapted to receive a voltage from the power supply.” For example, the voltage regulators are configured to receive an input, Vdd, from a power supply.

35. On information and belief, the voltage regulators in the ’962 Accused Products comprise “an output adapted to be coupled to said load.” For example, the voltage regulators are configured to provide an output, Vout, that is coupled to the load.

36. On information and belief, the voltage regulators in the ’962 Accused Products comprise “a feedback circuit coupled to a first current path and including a feedback transistor, wherein said feedback circuit is constructed to maintain a voltage at a gate of said feedback transistor substantially constant.” For example, the voltage regulators comprise a feedback circuit that includes a feedback transistor that is constructed so that the voltage at the gate of the feedback transistor is substantially constant. A current path goes through the feedback transistor into a programmable resistor divider. The resistor divider is coupled to an input of a differential amplifier. The output of the differential amplifier is coupled to the gate of the feedback transistor. As a result, the differential amplifier maintains the voltage at the gate of the feedback transistor at a substantially constant value.

37. On information and belief, the voltage regulators in the ’962 Accused Products comprise “a first current supply circuit constructed to supply to a second current path a first current that is substantially constant.” For example, the first current supply circuit comprises a diode connected transistor that is connected on one end to Vdd and coupled to a second transistor. The gate of the second transistor is connected to the output of the feedback circuit. The diode connected transistor and second transistor supply a first current that is substantially constant. The circuitry in

the ’962 Accused Products is configured such that the first current feeds into a resistor that provides a second path.

38. On information and belief, the voltage regulators in the ’962 Accused Products comprise “a second current supply circuit coupled to said first current supply circuit, said gate of said feedback transistor, and said output of said voltage regulator circuit and constructed to supply a second current to said second current path with a magnitude based on said voltage at said gate of said feedback transistor and a voltage at said output of said voltage regulator circuit.” For example, the second current supply circuit comprises a diode connected transistor that is connected on one end to Vdd and coupled to a second transistor. The gate of the second transistor is connected to the output of the voltage regulator circuit. The diode connected transistor and second transistor supply a second current. The circuitry in the ’962 Accused Products is configured such that the second current feeds into the same resistor that the first current feeds into via a second path. The first and second current supply circuits are coupled via a feedback path.

39. On information and belief, the voltage regulators in the ’962 Accused Products comprise “a pass device including a gate coupled to said second current path and adapted to receive a signal based on said current of said second current path and supply a load current to said load via said output of said voltage regulator circuit with a magnitude based on said signal.” For example, the pass device comprises a transistor that is connected to Vdd and coupled to the second current path such that its gate is adjusted by a signal based on the second current. The pass device supplies a current for the output of the voltage regulator dependent on the signal.

40. On information and belief, the voltage regulators in the ’962 Accused Products comprise “wherein said second current supply circuit is adapted to, via said pass device, cause an increase in magnitude of said load current supplied to said output if a voltage at said output

decreases and cause a decrease in magnitude of said load current supplied to said output if a voltage at said output increases." For example, the feedback circuit is configured to maintain a substantially constant output such that it causes an increase in magnitude if the voltage at the output decreases and causes a decrease in magnitude if the voltage at the output increases. The feedback circuit maintains this substantially constant output via the second current supply circuit and pass device.

41. On information and belief, the voltage regulators in the '962 Accused Products comprise "wherein said feedback circuit, said first current supply circuit, said second current supply circuit, and said pass device are integrated in an integrated circuit and referenced to said input of said voltage regulator circuit." For example, the feedback circuit, the first current supply circuit, the second current supply circuit, and the pass device are all on an integrated circuit and referenced to Vdd, as detailed above.

***Indirect Infringement (Inducement – 35 U.S.C. § 271(b))***

42. In addition and/or in the alternative to its direct infringements, Defendants have indirectly infringed one or more claims of the '962 patent by knowingly and intentionally inducing others, including its subsidiaries, distributors, affiliates, retailers, suppliers, integrators, importers, customers, and/or consumers, to directly infringe by making, using, offering to sell, selling and/or importing into the United States the '962 Accused Products.

43. At a minimum, Defendants had knowledge of the '962 patent since the filing of this suit. Since receiving notice of its infringements, Defendants actively induced the direct infringements of its subsidiaries, distributors, affiliates, retailers, suppliers, integrators, importers, customers, and/or consumers as set forth under U.S.C. § 271(b). For example, on information and belief, Defendants induce subsidiaries such as Micron Semiconductor Asia PTE and Micron

Technology Taiwan Inc. to import the ’962 Accused Products into the United States. Such inducements have been committed with the knowledge, or with willful blindness to the fact, that the acts induced constitute infringement of the ’962 Patent. On information and belief, Defendants intended to cause and took affirmative steps to induce infringement by, among other things, creating and disseminating advertisements and instructive materials that promote the infringing use of the ’962 Accused Products; creating and/or maintaining established distribution channels for the ’962 Accused Products into and within the United States; manufacturing the ’962 Accused Products in conformity with U.S. laws and regulations; distributing or making available datasheets supporting use of the ’962 Accused Products that promote their features, specifications, and applications; providing technical documentation and tools for the ’962 Accused Products, such as white papers, brochures, and/or manuals; promoting the incorporation of the ’962 Accused Products into end-user products, testing and certifying features related to initializing a dynamic semiconductor memory device of a random access in the ’962 Accused Products; and/or by providing technical support and/or related services for these products to purchasers in the United States.

***Damages***

44. On information and belief, despite having knowledge of the ’962 patent and knowledge that it is directly and/or indirectly infringing one or more claims of the ’962 patent, Micron has nevertheless continued its infringing conduct and disregarded an objectively high likelihood of infringement. Micron’s infringing activities relative to the ’962 patent have been, and continue to be, willful, wanton, malicious, in bad-faith, deliberate, consciously wrongful, flagrant, and an egregious case of misconduct beyond typical infringement such that Palisade is entitled to enhanced damages under 35 U.S.C. § 284 up to three times the amount found or assessed.

45. Palisade has been damaged as a result of Micron's infringing conduct described in this Count. Micron is, thus, liable to Palisade in an amount that adequately compensates Palisade for Micron's infringements, which, by law, cannot be less than a reasonable royalty, together with interest and costs as fixed by this Court under 35 U.S.C. § 284.

**COUNT II**

(INFRINGEMENT OF U.S. PATENT NO. 8,996,838)

46. Plaintiff incorporates the preceding paragraphs herein by reference.

47. This cause of action arises under the patent laws of the United States, and, in particular, 35 U.S.C. §§ 271, *et seq*.

48. Palisade is the owner of all substantial rights, title, and interest in and to the '838 patent including the right to exclude others and to enforce, sue, and recover damages for past infringements.

49. The '838 patent is valid, enforceable, and was duly and legally issued by the United States Patent and Trademark Office on March 31, 2015, after full and fair examination.

50. Micron directly and/or indirectly infringed (by inducing infringement) one or more claims of the '838 patent in this District and elsewhere in Texas and the United States by making, using, selling, offering to sell, and/or importing, and by actively inducing others to make, use, sell, offer to sell, and/or import products containing 3D NAND with 176 or more layers, such as packages laser marked as NV046, and/or products containing the same, such as the Micron 7450 Pro (collectively, the "'838 Accused Products").

***Direct Infringement (35 U.S.C. § 271(a))***

51. Micron directly infringed one or more claims of the '838 patent in this District and elsewhere in Texas and the United States.

52. Micron directly infringed, either by itself or via its agent(s), at least Claim 1 of the ’838 patent as set forth under 35 U.S.C. § 271(a) by making, using, offering for sale, selling, and/or importing the ’838 Accused Products, including by testing the ’838 Accused Products in configurations as in the exemplary implementations discussed further below. Furthermore, Micron made and sold the ’838 Accused Products outside of the United States and either delivered those products to its customers, distributors, and/or subsidiaries in the United States, or, in the case that it delivered the ’838 Accused Products outside of the United States, it did so intending and/or knowing that those products were destined for the United States and/or designed and designated for sale in the United States, thereby directly infringing the ’838 patent. *See, e.g., Lake Cherokee Hard Drive Techs., L.L.C. v. Marvell Semiconductor, Inc.*, 964 F. Supp. 2d 653, 658 (E.D. Tex. 2013).

53. By way of illustration only, the ’838 Accused Products perform a method comprising each and every step of claim 1 of the ’838 patent. On information and belief, the ’838 Accused Products performed the claimed steps in a data storage device that includes a memory having a three-dimensional (3D) memory configuration and including a structure extending through multiple layers of the memory. The ’838 Accused Products comprise a 3D memory configuration that includes a structure extending through multiple layers of the memory. For example, the annotated image below of a representative ’838 Accused Product demonstrates this:

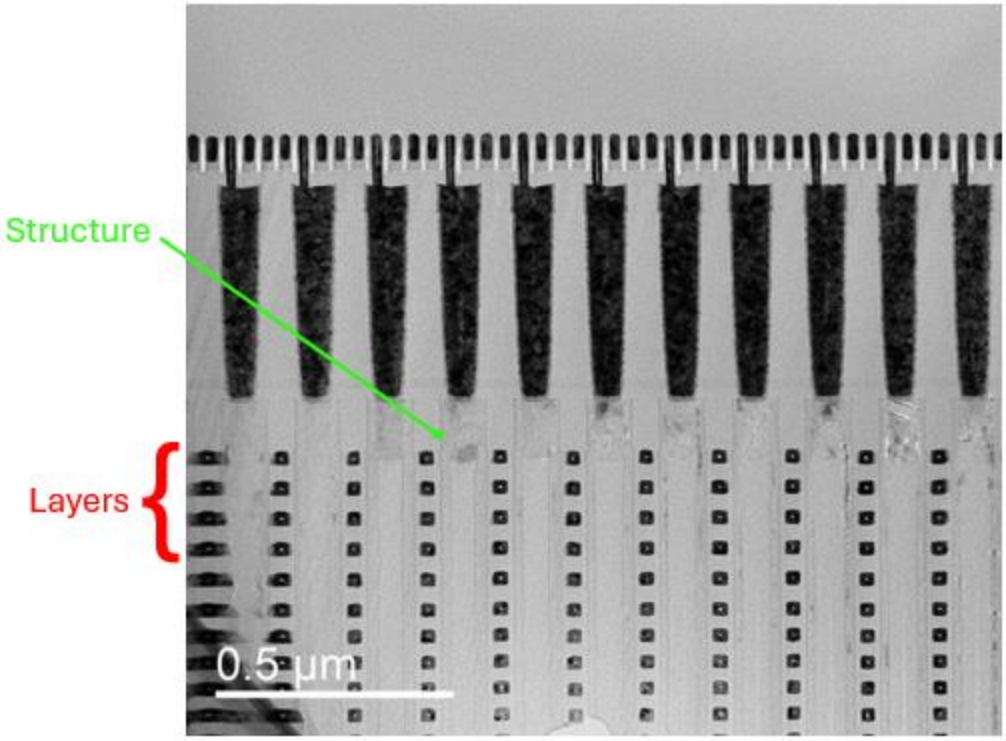



*Figure 1 - TEM Image of Micron 7450*

54. On information and belief, the '838 Accused Products store information at the data storage device, the information identifying a location associated with a variation of the structure. For example, the '838 Accused Products store information identifying a location associated with a variation of the structure. As described by Micron's Akira Goda in a paper titled "Recent Progress on 3D NAND Flash Technologies," "[i]n the latest achievement, 176-layer stacked 3D NAND has been demonstrated in both publication and mass production."[2]

[2] Ex. A – Akira Goda, *Recent Progress on 3D NAND Flash Technologies*, at 5 (*available at* https://www.mdpi.com/2079-9292/10/24/3156).

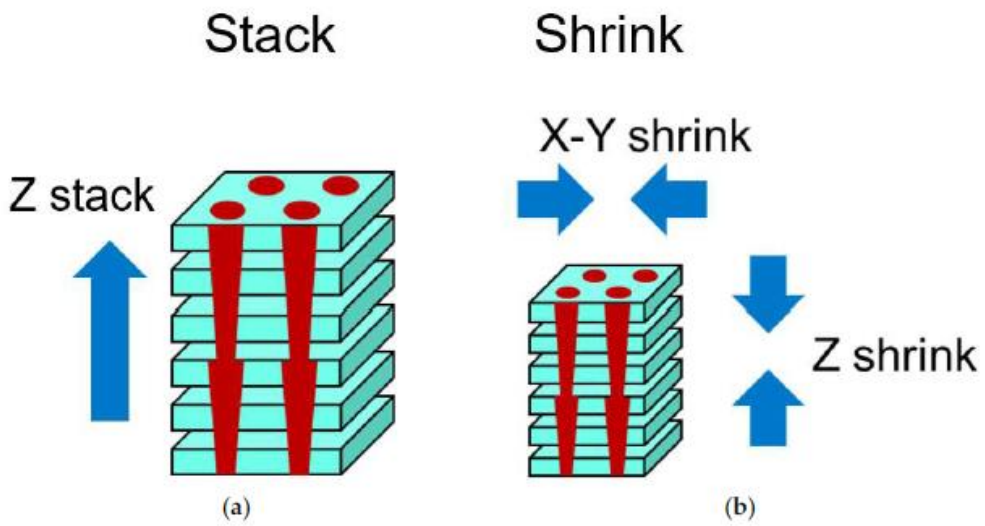



**Figure 9.** XYZ scaling of 3D NAND. (**a**) Layer stacking in Z-direction. (**b**) Footprint shrink of XY dimensions and layer pitch reduction as Z-shrink. Z-shrink is often combined with Z-stack to minimize the increase in the pillar height.

As Micron's Mr. Goda notes, "[w]ith the WL [word line] pitch scaling, the trapped charge migration between the neighboring cells would raise the reliability concern."[3] And, "large write parallelism (= page size × number of planes) and short tProg are critical to achieve high write bandwidth."[4] "The improvements in tProg are realized by combinations of WL and BL bias time reduction, *fine tuning of the programming voltage compensating cell characteristics' variability across the pillar* and the reduction in the program verify operations."[5]

55. On information and belief, the '838 Accused Products access the information. For example, the '838 Accused Products access the information (i.e., the information identifying a location associated with a variation of the structure) in order to determine the finely tuned programming voltage noted above.

[3] *Id*. at 7.
[4] *Id*. at 9.
[5] *Id*. (emphasis added).

***Indirect Infringement (Inducement – 35 U.S.C. § 271(b))***

56. In addition and/or in the alternative to its direct infringements, Defendants have indirectly infringed one or more claims of the ’838 patent by knowingly and intentionally inducing others, including its subsidiaries, distributors, affiliates, retailers, suppliers, integrators, importers, customers, and/or consumers, to directly infringe by making, using, offering to sell, selling and/or importing into the United States the ’838 Accused Products.

57. At a minimum, Defendants had knowledge of the ’838 patent since the filing of this suit. Since receiving notice of its infringements, Defendants actively induced the direct infringements of its subsidiaries, distributors, affiliates, retailers, suppliers, integrators, importers, customers, and/or consumers as set forth under U.S.C. § 271(b). For example, on information and belief, Defendants induce subsidiaries such as Micron Semiconductor Asia PTE and Micron Technology Taiwan Inc. to import the ’838 Accused Products into the United States. Such inducements have been committed with the knowledge, or with willful blindness to the fact, that the acts induced constitute infringement of the ’838 Patent. On information and belief, Defendants intended to cause and took affirmative steps to induce infringement by, among other things, creating and disseminating advertisements and instructive materials that promote the infringing use of the ’838 Accused Products; creating and/or maintaining established distribution channels for the ’838 Accused Products into and within the United States; manufacturing the ’838 Accused Products in conformity with U.S. laws and regulations; distributing or making available datasheets supporting use of the ’838 Accused Products that promote their features, specifications, and applications; providing technical documentation and tools for the ’838 Accused Products, such as white papers, brochures, and/or manuals; promoting the incorporation of the ’838 Accused Products into end-user products, testing and certifying features related to initializing a dynamic

semiconductor memory device of a random access in the ’838 Accused Products; and/or by providing technical support and/or related services for these products to purchasers in the United States.

***Damages***

58. On information and belief, despite having knowledge of the ’838 patent and knowledge that it is directly and/or indirectly infringing one or more claims of the ’838 patent, Micron has nevertheless continued its infringing conduct and disregarded an objectively high likelihood of infringement. Micron’s infringing activities relative to the ’838 patent have been, and continue to be, willful, wanton, malicious, in bad-faith, deliberate, consciously wrongful, flagrant, and an egregious case of misconduct beyond typical infringement such that Palisade is entitled to enhanced damages under 35 U.S.C. § 284 up to three times the amount found or assessed.

59. Palisade has been damaged as a result of Micron’s infringing conduct described in this Count. Micron is, thus, liable to Palisade in an amount that adequately compensates Palisade for Micron’s infringements, which, by law, cannot be less than a reasonable royalty, together with interest and costs as fixed by this Court under 35 U.S.C. § 284.

**COUNT III**

(INFRINGEMENT OF U.S. PATENT NO. 8,327,051)

60. Plaintiff incorporates the preceding paragraphs herein by reference.

61. This cause of action arises under the patent laws of the United States, and, in particular, 35 U.S.C. §§ 271, *et seq*.

62. Palisade is the owner of all substantial rights, title, and interest in and to the ’051 patent including the right to exclude others and to enforce, sue, and recover damages for past and future infringements.

63. The ’051 patent is valid, enforceable, and was duly and legally issued by the United States Patent and Trademark Office on December 4, 2012, after full and fair examination.

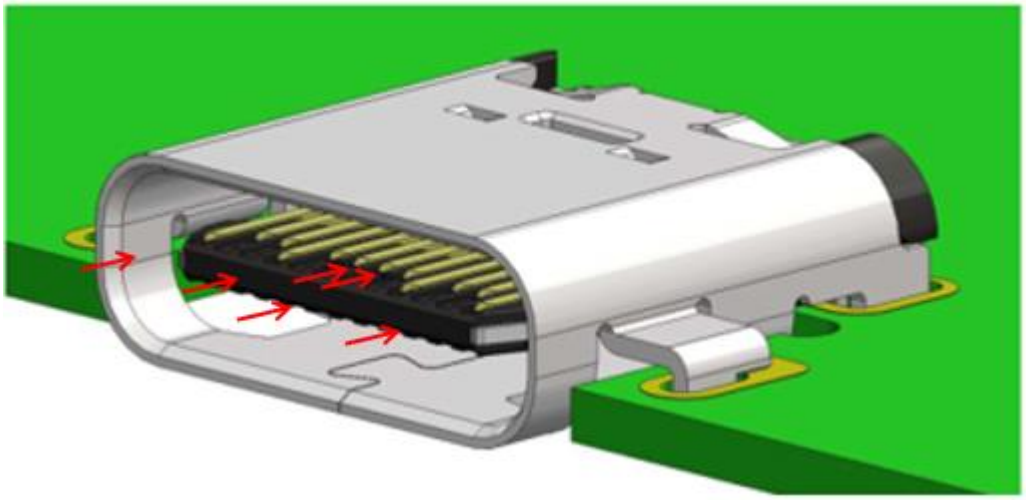
64. Micron has and continues to directly and/or indirectly infringe (by inducing infringement) one or more claims of the ’051 patent in this District and elsewhere in Texas and the United States by making, using, selling, offering to sell, and/or importing, and by actively inducing others to make, use, sell, offer to sell, and/or import, Micron products, their components and processes, and/or products containing the same that incorporate the fundamental technologies covered by the ’051 patent, including, but not limited to, SSDs comprising a USB-C port, such as the Crucial X9 portable SSD (collectively, the “’051 Accused Products”).

***Direct Infringement (35 U.S.C. § 271(a))***

65. Micron has directly infringed and continues to directly infringe one or more claims of the ’051 patent in this District and elsewhere in Texas and the United States.

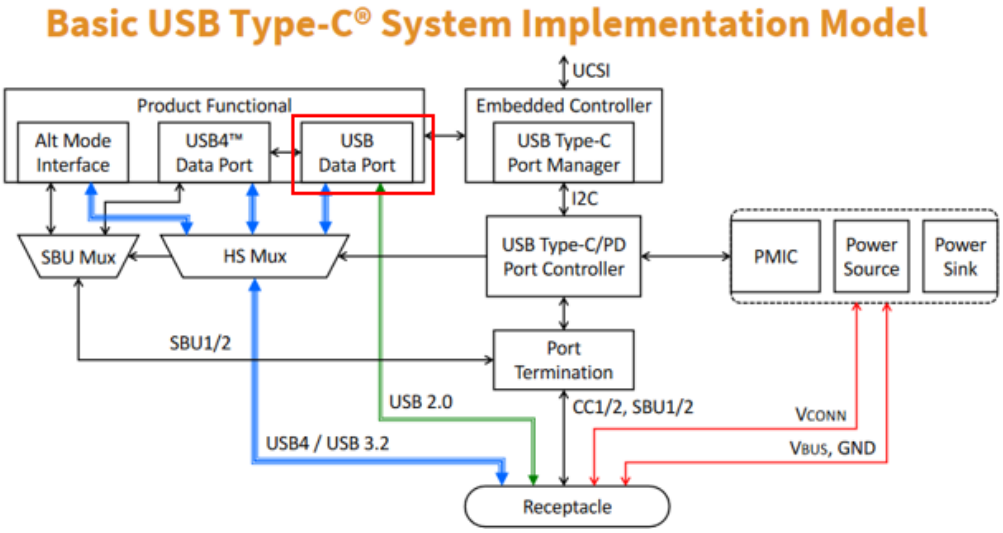
66. Micron has directly infringed and continues to directly infringe, either by itself or via its agent(s), at least Claim 1 of the ’051 patent as set forth under 35 U.S.C. § 271(a) by making, using, offering for sale, selling, and/or importing the ’051 Accused Products, including by testing the ’051 Accused Products in configurations as in the exemplary implementation discussed further below. Furthermore, Micron makes and sells the ’051 Accused Products outside of the United States and either delivers those products to its customers, distributors, and/or subsidiaries in the United States, or, in the case that it delivers the ’051 Accused Products outside of the United States, it does so intending and/or knowing that those products are destined for the United States and/or designed and designated for sale in the United States, thereby directly infringing the ’051 patent. *See, e.g., Lake Cherokee Hard Drive Techs., L.L.C. v. Marvell Semiconductor, Inc.*, 964 F. Supp. 2d 653, 658 (E.D. Tex. 2013).

67. By way of illustration only, the ’051 Accused Products comprise each and every element of claim 1 of the ’051 patent. On information and belief, the ’051 Accused Products comprise “Universal Serial Bus (USB) port comprising a first set of pins.” For example, the port shown below comprises a USB port comprising a first set of pins that allow for communication with a USB Type-A device.

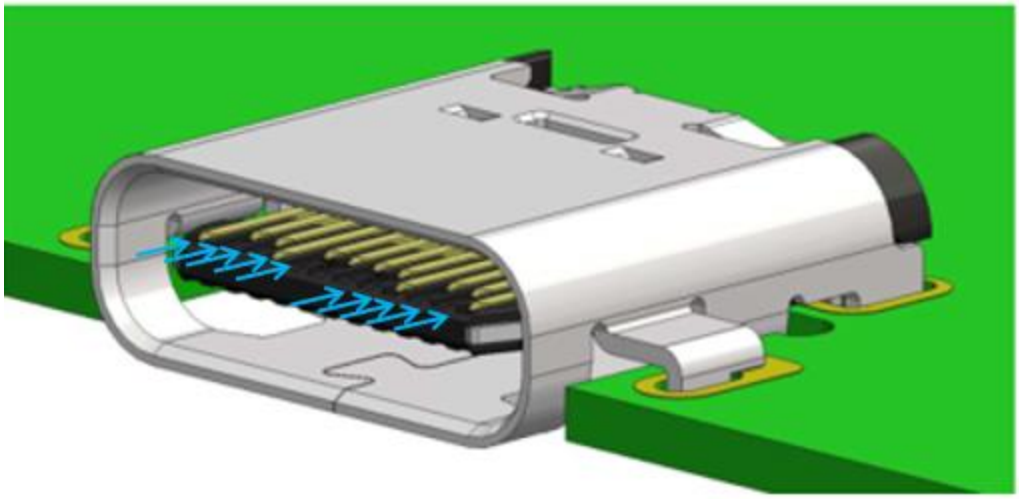


68. On information and belief, the ’051 Accused Products comprise “USB controller circuitry electrically connected with the first set of pins of the USB port.” For example, first set of

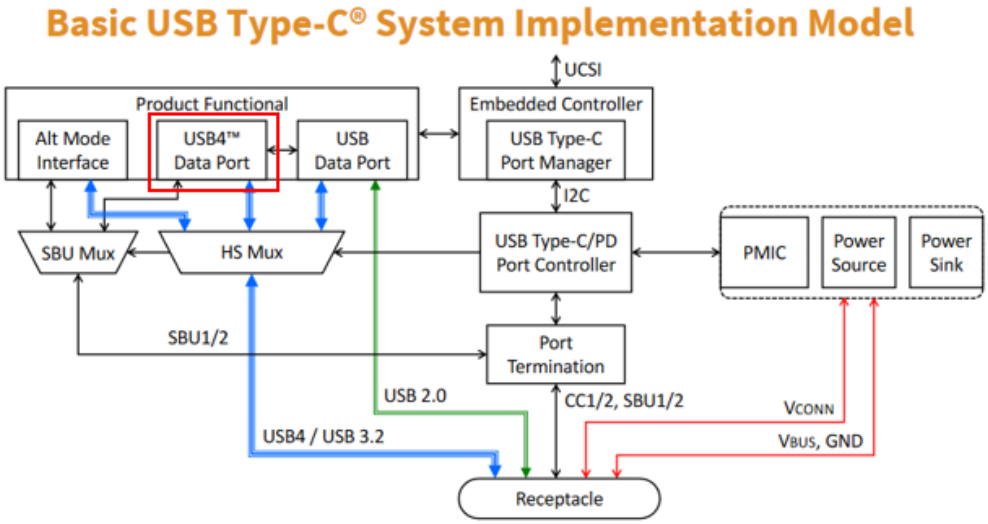
pins is electrically connected with a USB controller that controls the port functionality noted below in red.




69. On information and belief, the '051 Accused Products comprise "an input/output (I/O) port comprising a second set of pins." For example, the port shown below comprises an I/O port comprising a second set of pins that allow for communication with a USB Type-C device.



70. On information and belief, the ’051 Accused Products comprise “I/O controller circuitry electrically connected with the second set of pins of the I/O port.” For example, second set of pins is electrically connected with an I/O controller that controls the port functionality noted below in red.




71. On information and belief, the ’051 Accused Products comprise “a memory in communication with the USB port and the I/O port.” For example, the ’051 Accused Products comprise NAND flash memory that is in communication with both ports as evidenced by the fact the ’051 Accused Products can deliver data stored on the memory via either port.

72. On information and belief, the ’051 Accused Products comprise “a housing storing the memory and exposing the USB port and the I/O port.” For example, the ’051 Accused Products comprise a housing that stores the memory and exposes the USB port and the I/O port.

73. On information and belief, the ’051 Accused Products are configured such that “the USB port and the I/O port are positioned on a same end to allow a same card-insertion direction irrespective of whether a host device comprises a mating USB port or a mating I/O port.” For example, the ’051 Accused Products are configured such that the USB port and the I/O port are located on the same end. Further the ports are configured to allow for same card-insertion.

74. On information and belief, the ’051 Accused Products are configured such that “the USB port and the I/O port are positioned such that when the I/O port is electrically connected with the host device, at least one of the first set of pins of the USB port is not electrically connected to the host device, and when the USB port is electrically connected to the host device, at least one of the second set of pins of the I/O port is not electrically connected to the host device.” For example, the ’051 Accused Products are configured such that when the port is connected to a USB Type-A device, the first set of pins is electronically connected to the host device and at least one of the second set of pins is not electronically connected to the host device. Similarly, when the port is

connected to a USB Type-C device, the second set of pins is electronically connected to the host device and at least one of the first set of pins, such as the DP/DN pin, is not electronically connected to the host device.

***Indirect Infringement (Inducement – 35 U.S.C. § 271(b))***

75. In addition and/or in the alternative to its direct infringements, Defendants have indirectly infringed one or more claims of the ’051 patent by knowingly and intentionally inducing others, including its subsidiaries, distributors, affiliates, retailers, suppliers, integrators, importers, customers, and/or consumers, to directly infringe by making, using, offering to sell, selling and/or importing into the United States the ’051 Accused Products.

76. At a minimum, Defendants had knowledge of the ’051 patent since the filing of this suit. Since receiving notice of its infringements, Defendants actively induced the direct infringements of its subsidiaries, distributors, affiliates, retailers, suppliers, integrators, importers, customers, and/or consumers as set forth under U.S.C. § 271(b). For example, Defendants supply data sheets that encourage the use of the USB port on the ’051 Accused Products. *See, e.g.*, Ex. B – Crucial X9 Data Sheet, p. 2. Such inducements have been committed with the knowledge, or with willful blindness to the fact, that the acts induced constitute infringement of the ’051 Patent. On information and belief, Defendants intended to cause and took affirmative steps to induce infringement by, among other things, creating and disseminating advertisements and instructive materials that promote the infringing use of the ’051 Accused Products; creating and/or maintaining established distribution channels for the ’051 Accused Products into and within the United States; manufacturing the ’051 Accused Products in conformity with U.S. laws and regulations; distributing or making available datasheets supporting use of the ’051 Accused Products that promote their features, specifications, and applications; providing technical

documentation and tools for the ’051 Accused Products, such as white papers, brochures, and/or manuals; promoting the incorporation of the ’051 Accused Products into end-user products, testing and certifying features related to initializing a dynamic semiconductor memory device of a random access in the ’051 Accused Products; and/or by providing technical support and/or related services for these products to purchasers in the United States.

***Damages***

77. On information and belief, despite having knowledge of the ’051 patent and knowledge that it is directly and/or indirectly infringing one or more claims of the ’051 patent, Micron has nevertheless continued its infringing conduct and disregarded an objectively high likelihood of infringement. Micron’s infringing activities relative to the ’051 patent have been, and continue to be, willful, wanton, malicious, in bad-faith, deliberate, consciously wrongful, flagrant, and an egregious case of misconduct beyond typical infringement such that Palisade is entitled to enhanced damages under 35 U.S.C. § 284 up to three times the amount found or assessed.

78. Palisade has been damaged as a result of Micron’s infringing conduct described in this Count. Micron is, thus, liable to Palisade in an amount that adequately compensates Palisade for Micron’s infringements, which, by law, cannot be less than a reasonable royalty, together with interest and costs as fixed by this Court under 35 U.S.C. § 284.

## COUNT IV

(INFRINGEMENT OF U.S. PATENT NO. 9,281,314)

79. Plaintiff incorporates the preceding paragraphs herein by reference.

80. This cause of action arises under the patent laws of the United States, and, in particular, 35 U.S.C. §§ 271, *et seq*.

81. Palisade is the owner of all substantial rights, title, and interest in and to the ’314 patent including the right to exclude others and to enforce, sue, and recover damages for past and future infringements.

82. The ’314 patent is valid, enforceable, and was duly and legally issued by the United States Patent and Trademark Office on March 8, 2016, after full and fair examination.

83. Micron has and continues to directly and/or indirectly infringe (by inducing infringement) one or more claims of the ’314 patent in this District and elsewhere in Texas and the United States by making, using, selling, offering to sell, and/or importing, and by actively inducing others to make, use, sell, offer to sell, and/or import products containing 3D NAND, such as packages laser marked as NV046, and/or products containing the same, such as the Micron 7450 Pro (collectively, the “’314 Accused Products”).

***Direct Infringement (35 U.S.C. § 271(a) and (g))***

84. Micron has directly infringed and continues to directly infringe one or more claims of the ’314 patent in this District and elsewhere in Texas and the United States.

85. Micron has directly infringed and continues to directly infringe, either by itself or via its agent(s), at least Claim 13 of the ’314 patent as set forth under 35 U.S.C. § 271(a) by making, using, offering for sale, selling, and/or importing the ’314 Accused Products, including by testing the ’314 Accused Products in configurations as in the exemplary implementation discussed further below. Further, Micron has infringed certain claims of the ’314 patent under 35 U.S.C. § 271(g) by among other things, making, selling, offering for sale, and/or importing products the ’314 Accused Products that were made in a manner that satisfied the limitations of claim 13. Furthermore, Micron makes and sells the ’314 Accused Products outside of the United States and either delivers those products to its customers, distributors, and/or subsidiaries in the United States,

or, in the case that it delivers the ’314 Accused Products outside of the United States, it does so intending and/or knowing that those products are destined for the United States and/or designed and designated for sale in the United States, thereby directly infringing the ’314 patent. *See, e.g., Lake Cherokee Hard Drive Techs., L.L.C. v. Marvell Semiconductor, Inc.*, 964 F. Supp. 2d 653, 658 (E.D. Tex. 2013).

86. By way of illustration only, on information and belief, the ’314 Accused Products are made using a method of manufacturing that infringes claim 13 of the ’314 patent. For example, the method of manufacturing of the ’314 Accused Products comprises “forming a plurality of lines of memory cells.” This is illustrated by the purple boxes in the below cross section of a ’314 Accused Product:

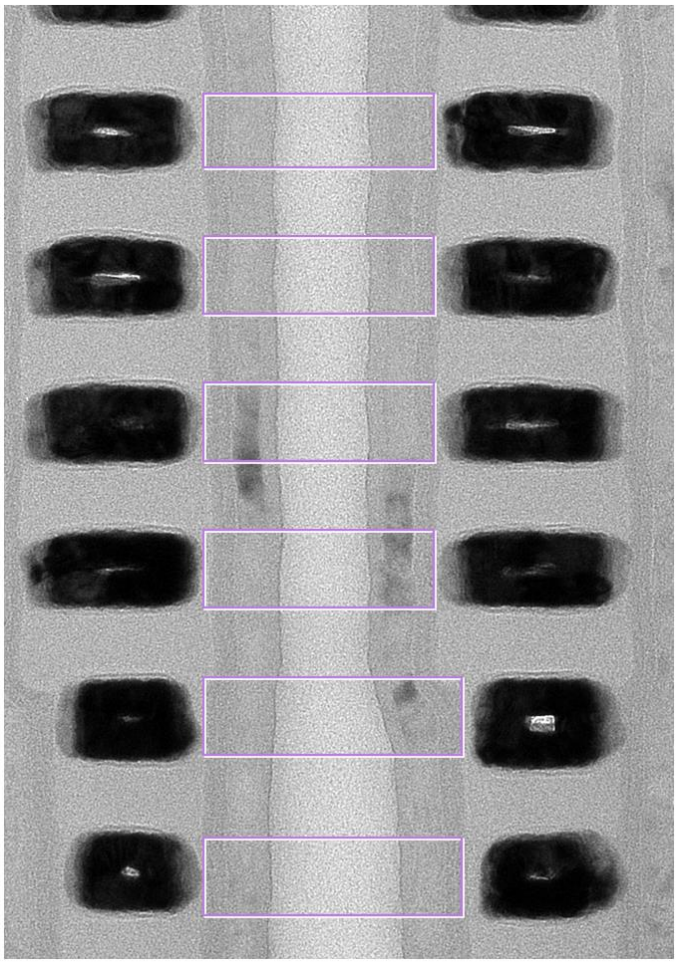


*Figure 2 - TEM Image of Micron 7450*

Further, the memory cells comprise "a charge storage region having sidewalls" and "a control gate." For example, a top down view of the '314 Accused Products shows a charge storage region having sidewalls and a control gate that consists of 1.5-2 nm TiN:

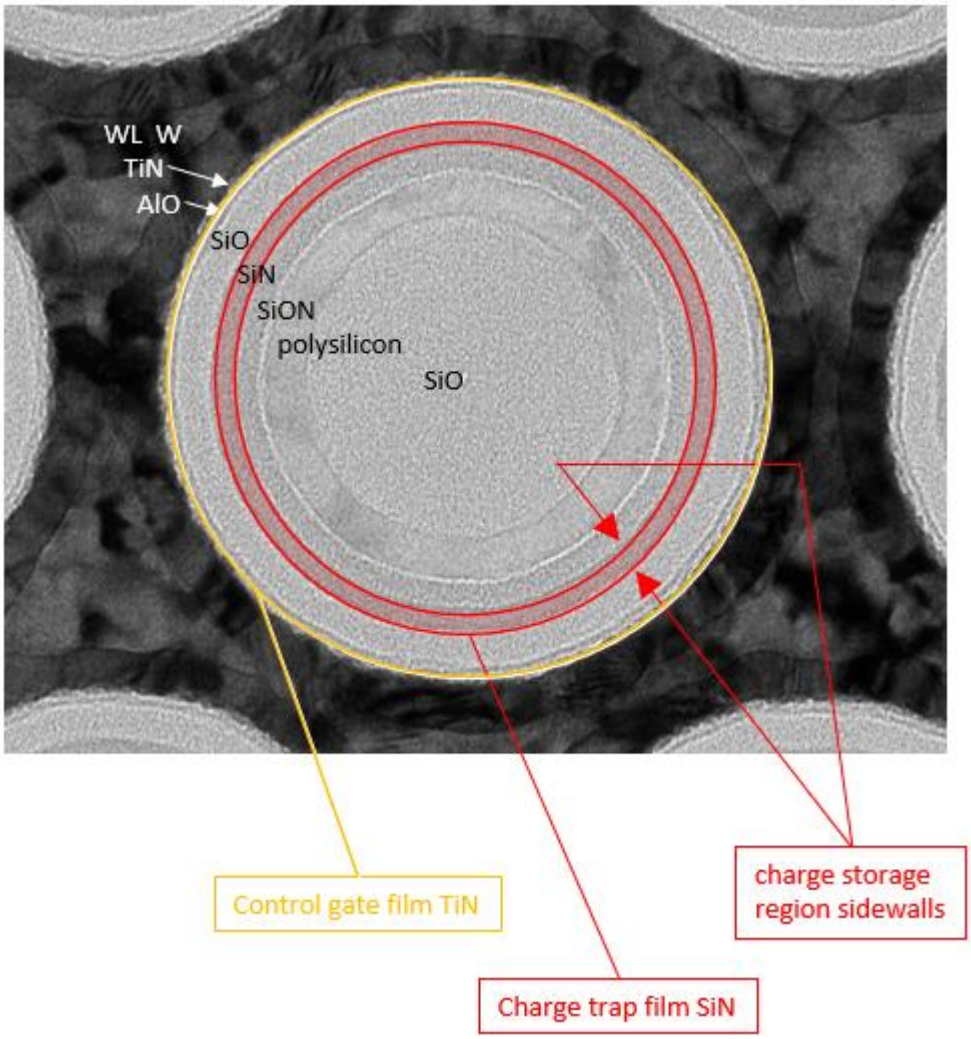



*Figure 3 - TEM Image of Micron 7450*

87. On information and belief, the method of manufacturing of the ’314 Accused Products comprises “forming a plurality of word lines each having sidewalls, each of the word lines being associated with a line of the memory cells, each of the word lines being coupled to the control gates of the memory cells with which it is associated.” This is illustrated by the top down view of a’314 Accused Product showing the word lines are coupled to the control gate:

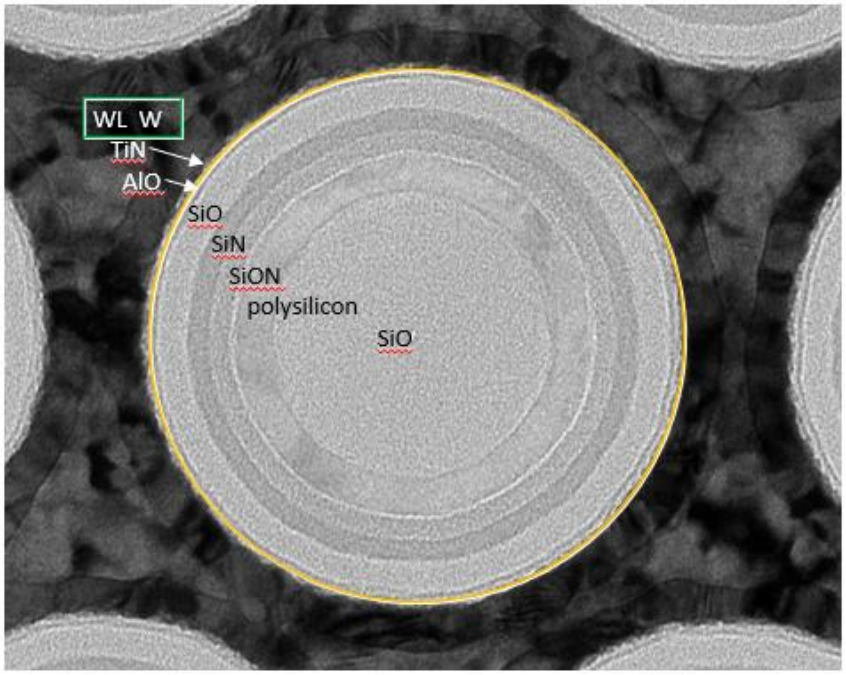



*Figure 4 - TEM Image of Micron 7450*

And the below cross section of a '314 Accused Product showing tungsten word lines that have side walls and are each coupled to the control gates of the memory cells:

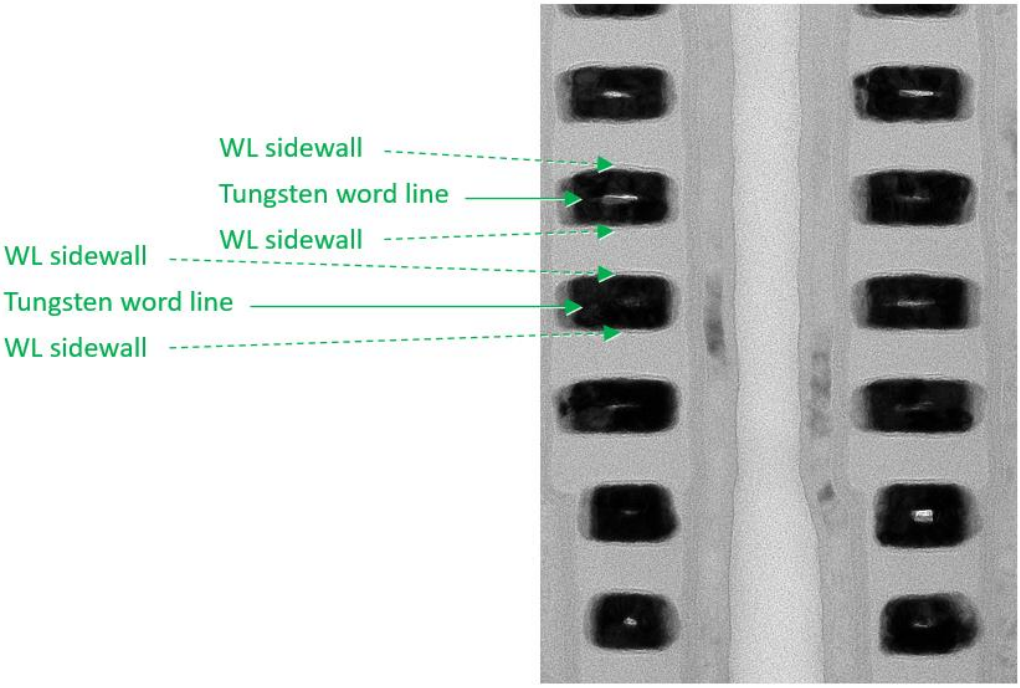



*Figure 5 - TEM Image of Micron 7450*

88. On information and belief, the method of manufacturing of the ’314 Accused Products comprises “forming first oxide regions that cover the sidewalls of the charge storage regions.” For example, in the below cross section, the sidewalls of the charge storage regions are covered by a silicon oxide layer.

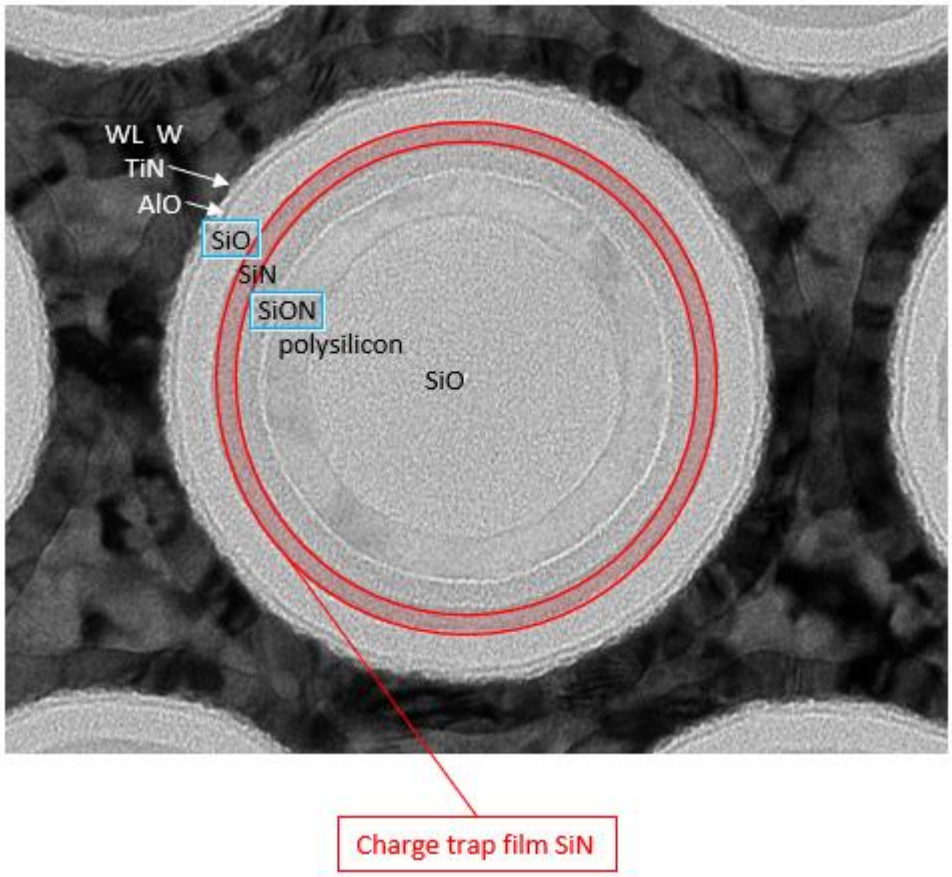



*Figure 6 - TEM Image of Micron 7450*

89. On information and belief, the method of manufacturing of the ’314 Accused Products comprises “forming second oxide regions that cover the sidewalls of the word lines” and “forming nitride regions that cover the second oxide regions.” For example, the below cross section of a ’314 Accused Product shows a second oxide region of aluminum oxide or silicon oxide that covers the sidewalls of the word lines and the second oxide region is covered in 1.5-2nm TiN.

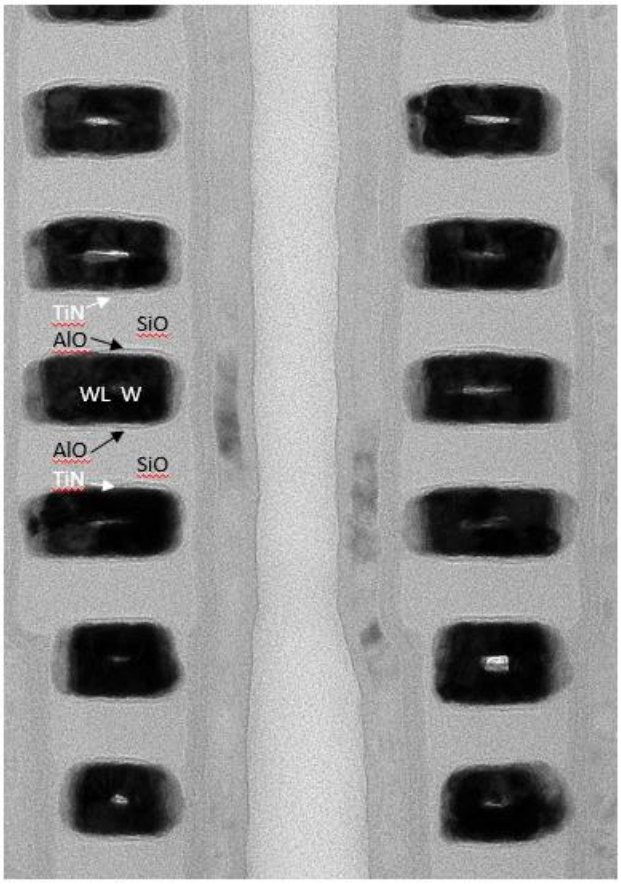



*Figure 7 - TEM Image of Micron 7450*

90. On information and belief, the method of manufacturing of the ’314 Accused Products comprises “forming electrical isolation regions other than silicon nitride adjacent to the first oxide regions that cover the sidewalls of the charge storage regions.” For example, the below cross section of a ’314 Accused Product shows a separate polysilicon region that is adjacent to the first oxide region and covers the charge storage region:

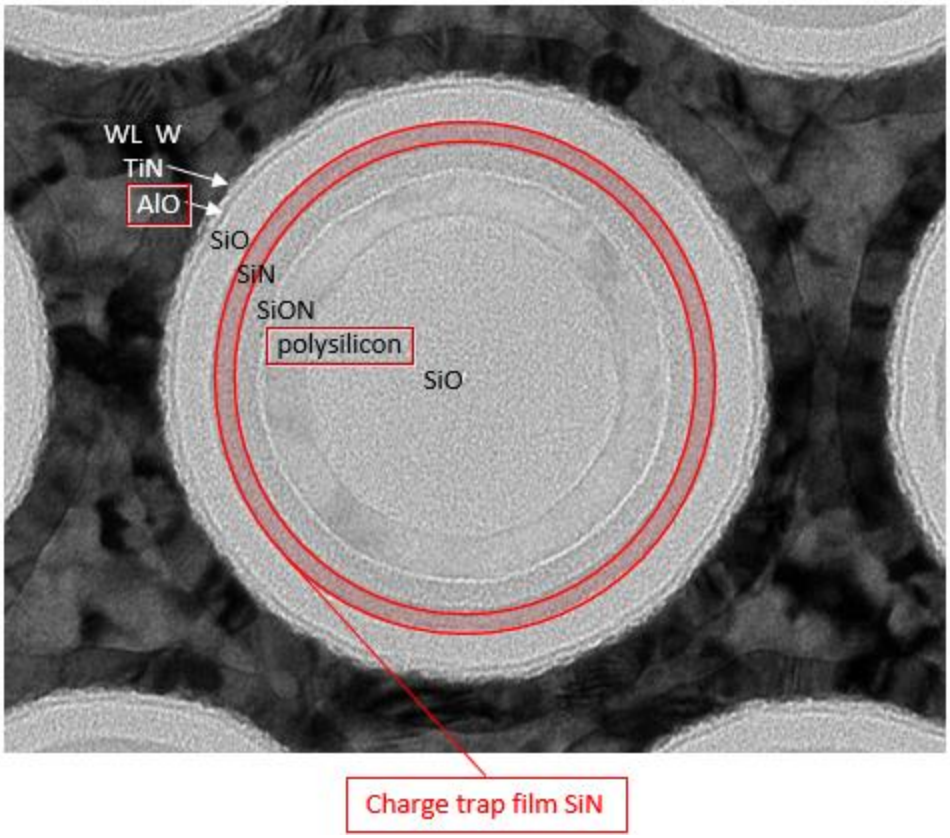



*Figure 8 - TEM Image of Micron 7450*

***Indirect Infringement (Inducement – 35 U.S.C. § 271(b))***

91. In addition and/or in the alternative to its direct infringements, Defendants have indirectly infringed one or more claims of the ’314 patent by knowingly and intentionally inducing others, including its subsidiaries, distributors, affiliates, retailers, suppliers, integrators, importers, customers, and/or consumers, to directly infringe by making, using, offering to sell, selling and/or importing into the United States the ’314 Accused Products.

92. At a minimum, Defendants had knowledge of the ’314 patent since the filing of this suit. Since receiving notice of its infringements, Defendants actively induced the direct infringements of its subsidiaries, distributors, affiliates, retailers, suppliers, integrators, importers, customers, and/or consumers as set forth under U.S.C. § 271(b). For example, on information and belief, Defendants induce subsidiaries such as Micron Semiconductor Asia PTE and Micron

Technology Taiwan Inc. to import the ’314 Accused Products into the United States. Such inducements have been committed with the knowledge, or with willful blindness to the fact, that the acts induced constitute infringement of the ’314 Patent. On information and belief, Defendants intended to cause and took affirmative steps to induce infringement by, among other things, creating and disseminating advertisements and instructive materials that promote the infringing use of the ’314 Accused Products; creating and/or maintaining established distribution channels for the ’314 Accused Products into and within the United States; manufacturing the ’314 Accused Products in conformity with U.S. laws and regulations; distributing or making available datasheets supporting use of the ’314 Accused Products that promote their features, specifications, and applications; providing technical documentation and tools for the ’314 Accused Products, such as white papers, brochures, and/or manuals; promoting the incorporation of the ’314 Accused Products into end-user products, testing and certifying features related to initializing a dynamic semiconductor memory device of a random access in the ’314 Accused Products; and/or by providing technical support and/or related services for these products to purchasers in the United States.

***Damages***

93. On information and belief, despite having knowledge of the ’314 patent and knowledge that it is directly and/or indirectly infringing one or more claims of the ’314 patent, Micron has nevertheless continued its infringing conduct and disregarded an objectively high likelihood of infringement. Micron’s infringing activities relative to the ’314 patent have been, and continue to be, willful, wanton, malicious, in bad-faith, deliberate, consciously wrongful, flagrant, and an egregious case of misconduct beyond typical infringement such that Palisade is entitled to enhanced damages under 35 U.S.C. § 284 up to three times the amount found or assessed.

94. Palisade has been damaged as a result of Micron's infringing conduct described in this Count. Micron is, thus, liable to Palisade in an amount that adequately compensates Palisade for Micron's infringements, which, by law, cannot be less than a reasonable royalty, together with interest and costs as fixed by this Court under 35 U.S.C. § 284.

**COUNT V**

(INFRINGEMENT OF U.S. PATENT NO. 9,524,974)

95. Plaintiff incorporates the preceding paragraphs herein by reference.

96. This cause of action arises under the patent laws of the United States, and, in particular, 35 U.S.C. §§ 271, *et seq*.

97. Palisade is the owner of all substantial rights, title, and interest in and to the '974 patent including the right to exclude others and to enforce, sue, and recover damages for past and future infringements.

98. The '974 patent is valid, enforceable, and was duly and legally issued by the United States Patent and Trademark Office on December 20, 2016, after full and fair examination.

99. Micron has and continues to directly and/or indirectly infringe (by inducing infringement) one or more claims of the '974 patent in this District and elsewhere in Texas and the United States by making, using, selling, offering to sell, and/or importing, and by actively inducing others to make, use, sell, offer to sell, and/or import products containing NAND, such as packages laser marked as NV046, and/or products containing the same, such as the Micron 7450 Pro (collectively, the "'974 Accused Products").

***Direct Infringement (35 U.S.C. § 271(a) and (g))***

100. Micron has directly infringed and continues to directly infringe one or more claims of the '974 patent in this District and elsewhere in Texas and the United States.

101. Micron has directly infringed and continues to directly infringe, either by itself or via its agent(s), at least Claim 1 of the ’974 patent as set forth under 35 U.S.C. § 271(a) by making, using, offering for sale, selling, and/or importing the ’974 Accused Products, including by testing the ’974 Accused Products in configurations as in the exemplary implementation discussed further below. Further, Micron has infringed certain claims of the ’974 patent under 35 U.S.C. § 271(g) by among other things, making, selling, offering for sale, and/or importing products the ’974 Accused Products that were made in a manner that satisfied the limitations of claim 12. Furthermore, Micron makes and sells the ’974 Accused Products outside of the United States and either delivers those products to its customers, distributors, and/or subsidiaries in the United States, or, in the case that it delivers the ’974 Accused Products outside of the United States, it does so intending and/or knowing that those products are destined for the United States and/or designed and designated for sale in the United States, thereby directly infringing the ’974 patent. *See, e.g., Lake Cherokee Hard Drive Techs., L.L.C. v. Marvell Semiconductor, Inc.*, 964 F. Supp. 2d 653, 658 (E.D. Tex. 2013).

102. By way of illustration only, the ’974 Accused Products comprise each and every element of claim 1 of the ’974 Patent. On information and belief, the ’974 Accused Products are NAND flash memory that comprise a semiconductor substrate. For example, as the below annotated cross section of a representative ’974 Accused Product illustrates, the ’974 Accused Products comprise a “semiconductor substrate,” a “dielectric layer extending over the semiconductor substrate,” “a plurality of first trenches in the dielectric layer, each first trench being elongated along a first direction and having a first shape in cross section along a plane that is perpendicular to the first direction,” “a plurality of second trenches in the dielectric layer, each second trench being elongated along the first direction and having a second shape in cross section

along the plane, the second shape being different from the first shape, the first and second trenches arranged in an alternating pattern that alternates from first trench to second trench along a second direction that is perpendicular to the first direction," and "a plurality of bit lines located in the first trenches."

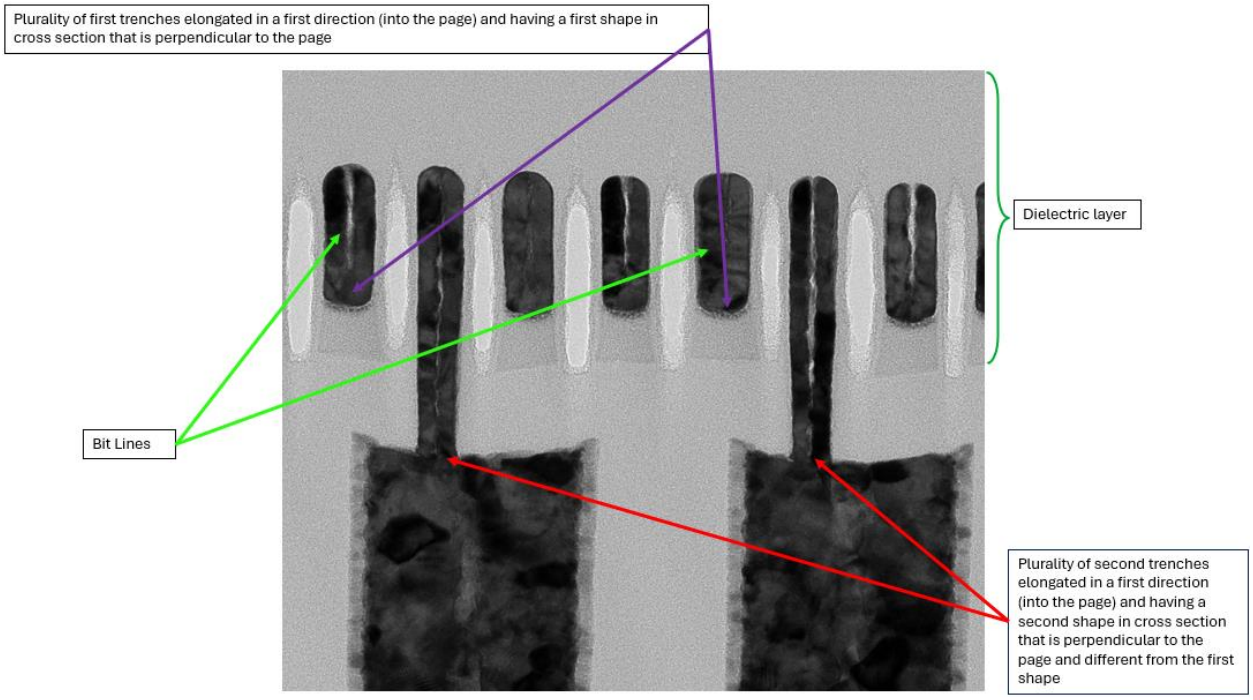



*Figure 9 - TEM Image of Micron 7450*

For example, the plurality of first trenches (pointed to in purple above) are elongated into the page. The '974 Accused Products also comprise a plurality of second trenches (pointed to in red above). The second trenches have a different height/from the first trenches. The first and second trenches are arranged in an alternating pattern. Bit lines are located in the plurality of first trenches.

***Indirect Infringement (Inducement – 35 U.S.C. § 271(b))***

103. In addition and/or in the alternative to its direct infringements, Defendants have indirectly infringed one or more claims of the '974 patent by knowingly and intentionally inducing others, including its subsidiaries, distributors, affiliates, retailers, suppliers, integrators, importers,

customers, and/or consumers, to directly infringe by making, using, offering to sell, selling and/or importing into the United States the ’974 Accused Products.

104. At a minimum, Defendants had knowledge of the ’974 patent since the filing of this suit. Since receiving notice of its infringements, Defendants actively induced the direct infringements of its subsidiaries, distributors, affiliates, retailers, suppliers, integrators, importers, customers, and/or consumers as set forth under U.S.C. § 271(b). For example, on information and belief, Defendants induce subsidiaries such as Micron Semiconductor Asia PTE and Micron Technology Taiwan Inc. to import the ’974 Accused Products into the United States. Such inducements have been committed with the knowledge, or with willful blindness to the fact, that the acts induced constitute infringement of the ’974 Patent. On information and belief, Defendants intended to cause and took affirmative steps to induce infringement by, among other things, creating and disseminating advertisements and instructive materials that promote the infringing use of the ’974 Accused Products; creating and/or maintaining established distribution channels for the ’974 Accused Products into and within the United States; manufacturing the ’974 Accused Products in conformity with U.S. laws and regulations; distributing or making available datasheets supporting use of the ’974 Accused Products that promote their features, specifications, and applications; providing technical documentation and tools for the ’974 Accused Products, such as white papers, brochures, and/or manuals; promoting the incorporation of the ’974 Accused Products into end-user products, testing and certifying features related to initializing a dynamic semiconductor memory device of a random access in the ’974 Accused Products; and/or by providing technical support and/or related services for these products to purchasers in the United States.

***Damages***

105. On information and belief, despite having knowledge of the ’974 patent and knowledge that it is directly and/or indirectly infringing one or more claims of the ’974 patent, Micron has nevertheless continued its infringing conduct and disregarded an objectively high likelihood of infringement. Micron’s infringing activities relative to the ’974 patent have been, and continue to be, willful, wanton, malicious, in bad-faith, deliberate, consciously wrongful, flagrant, and an egregious case of misconduct beyond typical infringement such that Palisade is entitled to enhanced damages under 35 U.S.C. § 284 up to three times the amount found or assessed.

106. Palisade has been damaged as a result of Micron’s infringing conduct described in this Count. Micron is, thus, liable to Palisade in an amount that adequately compensates Palisade for Micron’s infringements, which, by law, cannot be less than a reasonable royalty, together with interest and costs as fixed by this Court under 35 U.S.C. § 284.

## CONCLUSION

107. Palisade is entitled to recover from Defendants the damages sustained by Palisade as a result of Defendants’ wrongful acts, and willful infringements, in an amount subject to proof at trial, which, by law, cannot be less than a reasonable royalty, together with interest and costs as fixed by this Court.

108. Palisade has incurred and will incur attorneys’ fees, costs, and expenses in the prosecution of this action. The circumstances of this dispute may give rise to an exceptional case within the meaning of 35 U.S.C. § 285, and Palisade is entitled to recover its reasonable and necessary attorneys’ fees, costs, and expenses.

## JURY DEMAND

109. Palisade hereby requests a trial by jury pursuant to Rule 38 of the Federal Rules of Civil Procedure.

## PRAYER FOR RELIEF

110. Palisade respectfully requests that the Court find in its favor and against Defendants, and that the Court grant Palisade the following relief:

(i) A judgment that one or more claims of the Asserted Patents have been infringed, either literally and/or under the doctrine of equivalents, by Defendants;

(ii) A judgment that one or more claims of the Asserted Patents have been willfully infringed, either literally and/or under the doctrine of equivalents, by Defendants;

(iii) A judgment that Defendants account for and pay to Plaintiff all damages and costs incurred by Plaintiff because of Defendants' infringing activities and other conduct complained of herein, including an accounting for any sales or damages not presented at trial;

(iv) A judgment that Defendants account for and pay to Plaintiff a reasonable, ongoing, post judgment royalty because of Defendants' infringing activities, including continuing infringing activities, and other conduct complained of herein;

(v) A judgment that Plaintiff be granted pre-judgment and post judgment interest on the damages caused by Defendants' infringing activities and other conduct complained of herein;

(vi) A judgment that this case is exceptional under the provisions of 35 U.S.C. § 285 and award enhanced damages; and

(vii) Such other and further relief as the Court deems just and equitable.

Dated: October 16, 2024

Respectfully submitted,

*/s/ Patrick J. Conroy*

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# Exhibit A

electronics

IMPACT FACTOR 2.6

CITESCORE 5.3

Review

# Recent Progress on 3D NAND Flash Technologies

Akira Goda

Special Issue
High-Density Solid-State Memory Devices and Technologies

Edited by
Prof. Dr. Christian Monzio Compagnoni and Prof. Dr. Riichiro Shirota

MDPI

https://doi.org/10.3390/electronics10243156

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Palisade Technologies' Exhibit 2001
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electronics

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*Review*

# Recent Progress on 3D NAND Flash Technologies

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**Abstract:** Since 3D NAND was introduced to the industry with 24 layers, the areal density has been successfully increased more than ten times, and has exceeded 10 Gb/mm$^2$ with 176 layers. The physical scaling of XYZ dimensions including layer stacking and footprint scaling enabled the density scaling. Logical scaling has been successfully realized, too. TLC (triple-level cell, 3 bits per cell) is now the mainstream in 3D NAND, while QLC (quad-level cell, 4 bits per cell) is increasing the presence. Several attempts and partial demonstrations were made for PLC (penta-level cell, 5 bits per cell). CMOS under array (CuA) enabled the die size reduction and performance improvements. Program and erase schemes to address the technology challenges such as short-term data retention of the charge-trap cell and the large block size are being investigated.

**Keywords:** 3D NAND; floating gate cell; charge-trap cell; CMOS under array

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**Citation:** Goda, A. Recent Progress on 3D NAND Flash Technologies. *Electronics* **2021**, *10*, 3156. https://doi.org/10.3390/electronics10243156

Academic Editor: Changhwan Shin

Received: 30 November 2021
Accepted: 13 December 2021
Published: 18 December 2021

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## 1. Introduction

After 2D NAND reached the scaling limit around 15 nm in process node, 3D NAND was proposed as a solution for the continuous NAND scaling [1]. The 3D NAND was introduced into production with 24 layers and MLC technology [2]. The scaling trend of the areal density of 2D NAND and 3D NAND is summarized based on the NAND publications in IEEE ISSCC conferences, (Figure 1). As seen in Figure 1, 3D NAND successfully replaced 2D NAND and has achieved more than 10 Gb/mm$^2$ areal density [2–31].

At the early stage of the 3D NAND development, various types of 3D NAND technologies were proposed. A comprehensive survey can be found in [32]. After extensive research on various technology options, vertical NAND string architecture with gate-all-around (GAA) cells was introduced to the industry for floating gate (FG) cells and charge-trap cells [2,33].

In this paper, the status of 3D NAND scaling is reviewed and discussed by using the ISSCC conference publications as a reference. This review mainly focuses on the vertical 3D NAND technology adopted in the industry. The physical and logical scaling of 3D NAND will be discussed. The recent progress and topics since the prior review of 3D NAND [34] will be reviewed, including progress on the QLC technology and beyond.

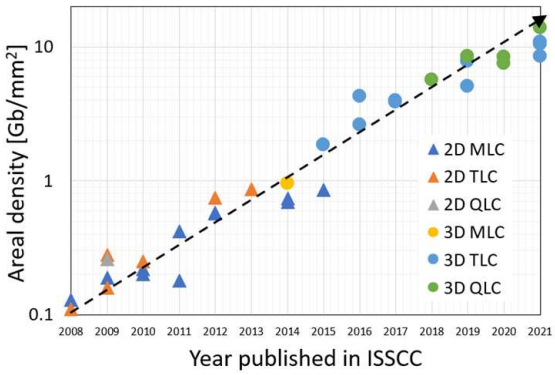


**Figure 1.** Areal density trend of NAND flash chip presented in ISSCC conferences since 2008 [2–31]. Adapted with permission from ref. [34], Copyright 2020 IEEE.



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## 2. 3D NAND Architecture and Operations

Figure 2 shows the 3D NAND cell array architectures. The strings are placed in the vertical direction. Word lines (WLs) have a plate-like shape and are stacked vertically for 3D cell stacking. There are multiple select gates at the drain side (SGDs) in a block. The channel of the NAND string has a cylinder shape.

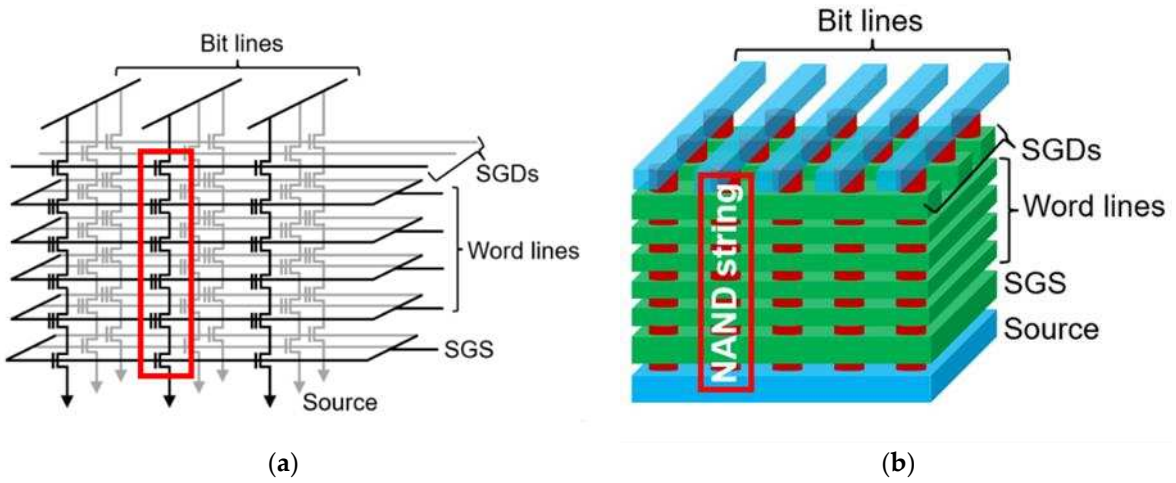



**Figure 2.** 3D NAND array architecture [35]. (**a**) Schematics of 3 × 3 NAND strings and (**b**) bird's eye view of 3 × 5 NAND strings. Only 4 word lines (WLs) in a string are shown for visibility. The actual 3D NAND has more than 128 WLs in a string.

A block is a unit of the erase operation. As shown in Figure 3, there are two types of erase methods in 3D NAND—the body erase (Figure 3a) and the GIDL erase (Figure 3b) [1,36]. In the body erase, NAND strings are connected to the Si-substrate, and holes are supplied to the NAND string from the Si-substrate, enabling the positive body potential required for erase. In the GIDL erase, the NAND strings are de-decoupled from the Si-substrate and formed on the N+ source layer instead. During erase, the electron-hole pairs are generated at source and drain N+ junctions by GIDL mechanism to supply holes to the NAND strings. The GIDL erase is used for the CMOS under Array (CuA) technology, which will be discussed later [33].

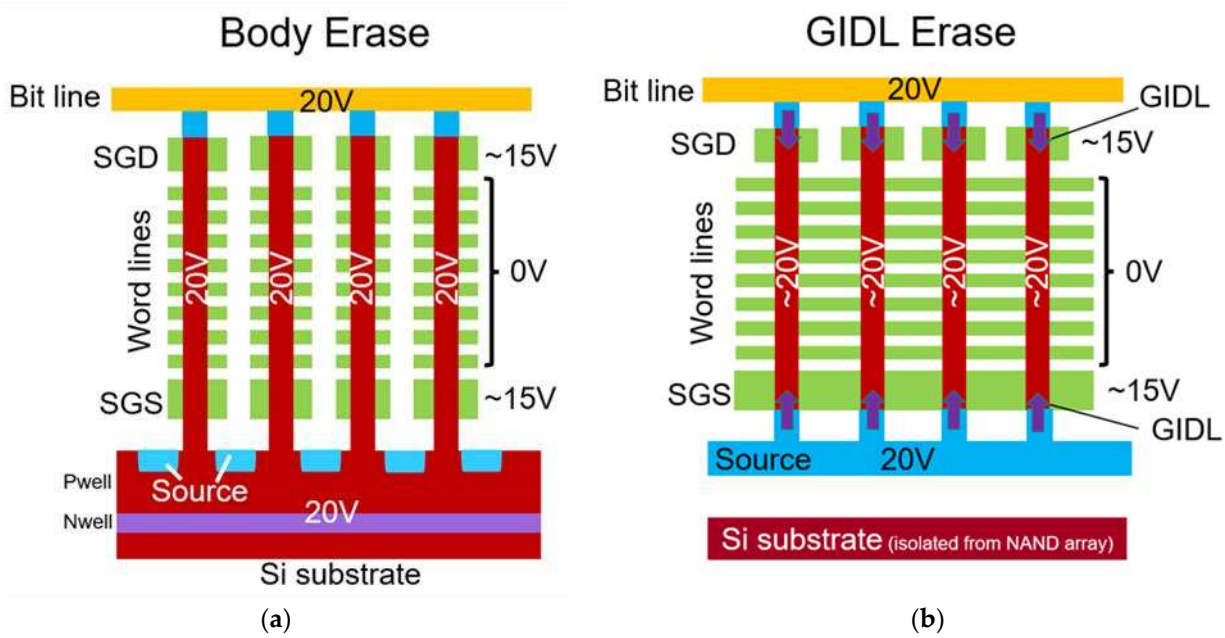



**Figure 3.** Erase schemes of 3D NAND [35]. (**a**) Body erase scheme directly biases the channels at erase voltage. Holes are supplied from the Si-substrate. (**b**) GIDL erase scheme generates electron-hole pairs at the source and drain junctions. The generated holes are supplied to the channels to boost the potential to around the erase voltage.

During program and read, one of the SGDs is selected in a block so that one NAND string can be selected per bit line (Figure 4).

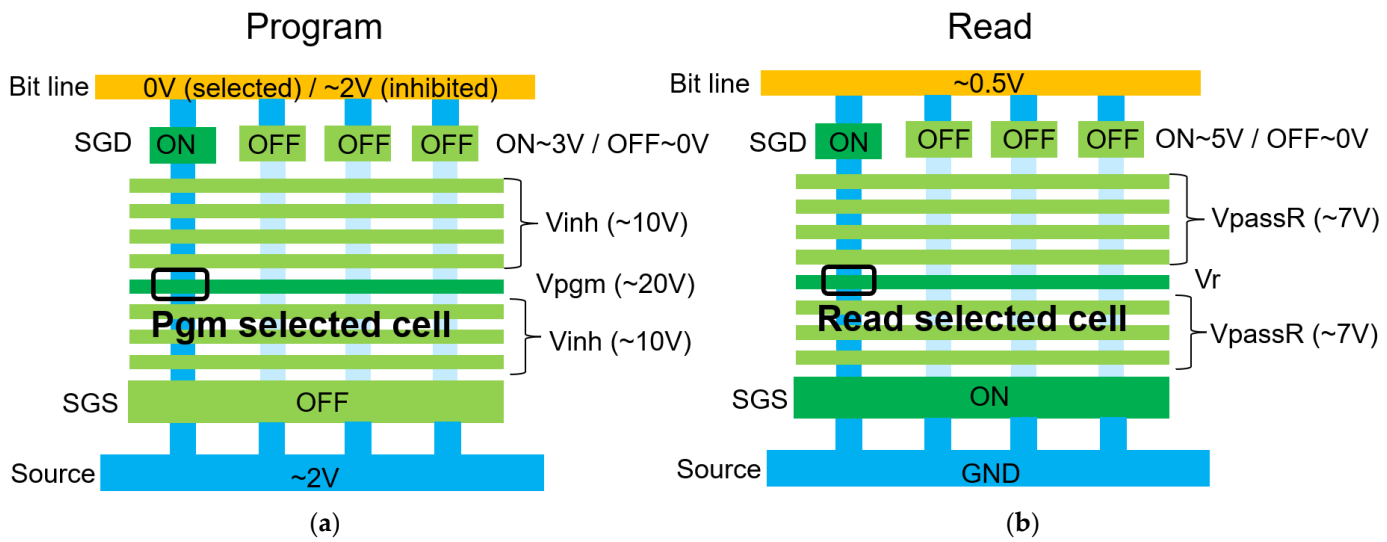



**Figure 4.** (**a**) Program and (**b**) read operations of 3D NAND. One cell per bit line is selected by selecting one SGD and one WL [35].

## 3. Floating Gate NAND and Replacement Gate NAND

### *3.1. Architectures of FG NAND and RG NAND*

The floating gate (FG) cell technology was used in 2D NAND. In 3D NAND, in addition to the FG technology (FG NAND), replacement gate cell technology (RG NAND) is also utilized [33,36]. Figure 5 compares the cross-sections of the NAND strings for FG NAND and RG NAND.

In FG NAND, the FG storages are separated between cells because the FG is made of the conductive polysilicon material. The advanced cell integration scheme is adopted to realize the FG separation [33]. In this scheme, the cells are formed outside the pillar holes. Therefore, the diameter of the pillar etching needs to be aligned with the final channel diameter of the NAND string.

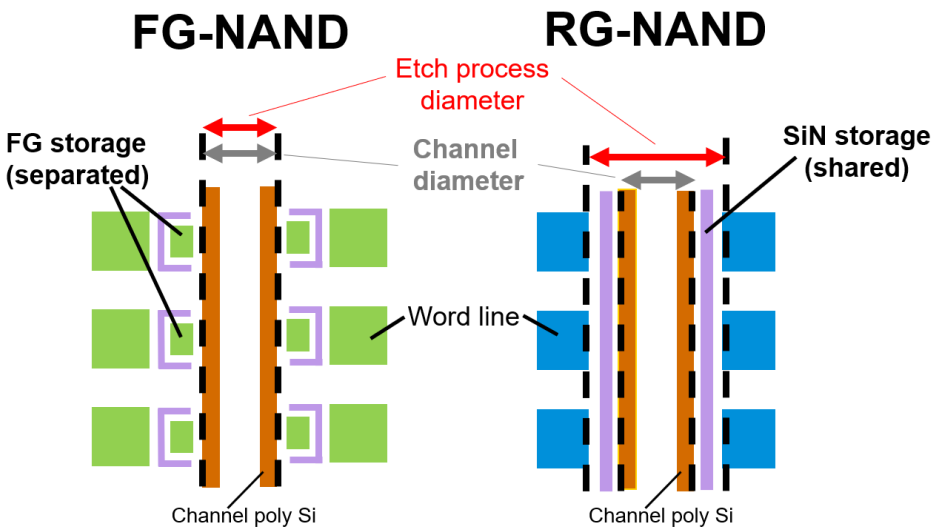



**Figure 5.** Cross-section comparison of NAND strings between floating gate (FG) NAND and replacement gate (RG) NAND. RG NAND has a larger diameter for the memory hole etching which is advantageous for the pillar height scaling.

In RG NAND, charge-trap cells with a silicon-nitride (SiN) storage layer are employed [2]. Because the SiN storage is a dielectric material which can trap charges, the storage layer can be shared and continuous among the cells. The SiN storage film and other films composing the charge-trap cells are formed after the dry etching of the pillar holes. Therefore, the diameter of the pillar holes for etching can be larger than that of the final channel diameter by the thicknesses of the cell dielectrics. This is advantageous for the pillar etching, especially for the very tall pillar when many cells are stacked vertically. The word line is formed by tungsten metal by replacing the SiN films stacked originally [36]. Therefore, the technology is called replacement gate NAND. RG NAND is the combination of the replacement gate technology and the charge-trap cell technology.

### *3.2. Band-Engineered Tunneling Dielectrics of the Charge-Trap Cell*

In the FG cell, electrons are injected to or emitted from the FG by Fowler–Nordheim (FN) Tunneling (Figure 6a). In the charge-trap cells, the programming is similar to FG cells, where the electrons are injected to the SiN storage by modified FN tunneling. For erase, holes are injected to the SiN storage by direct tunneling (DT) (DT erase) (Figure 6b). In the charge-trap cell, in order to enhance erase efficiently, the cell stack is engineered as shown in Figure 7a. First, the band engineered (BE) tunnel directrices has been introduced [37]. As BE-tunnel dielectrics, an ONO stacked film or a film with an engineered nitrogen profile can be used instead of the $SiO_2$ tunnel layer. With BE-tunnel dielectrics, holes can tunnel only the thin oxide layer during the erase, while the full ONO thickness can be utilized during the retention. Second, the High-k/Metal gate is used to reduce the unwanted electron injection from the control gate [38]. By combining the BE-tunnel layer and the High-k/Metal gate, good erase characteristics can be achieved with the charge-trap cell (Figure 7b).

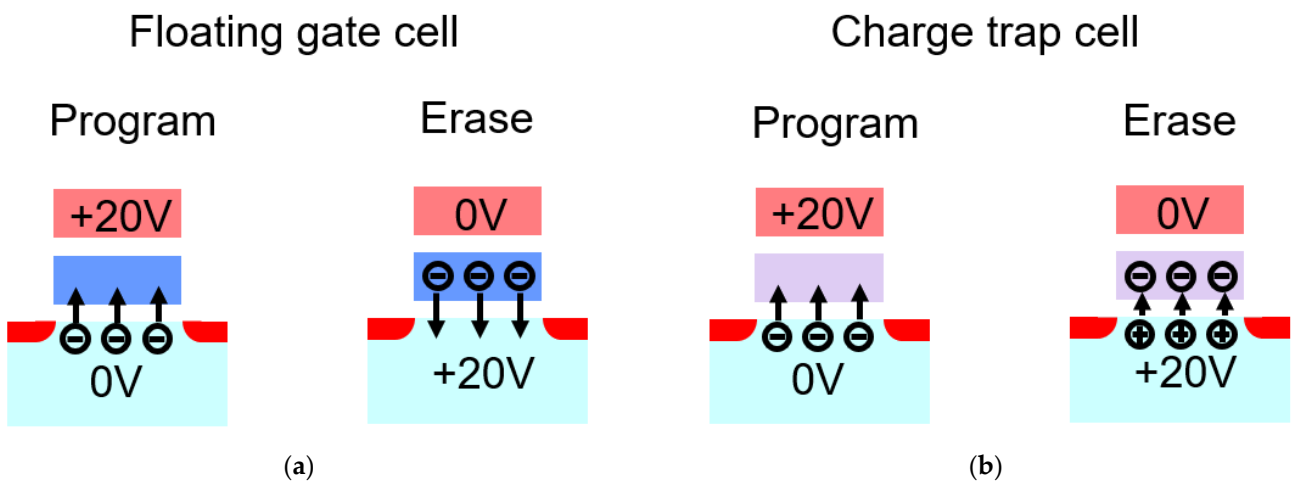



**Figure 6.** Program and erase operations for (**a**) floating gate cell and (**b**) charge-trap cell. In the charge-trap cell, holes are injected to the storage layer by direct tunneling.

### *3.3. Data Retention Mechanisms of the Charge-Trap Cell*

The short-term data retention has been a challenge for the charge-trap cell [38]. Figure 8 shows various mechanisms potentially causing the short-term data retention [39]. The first mechanism is charge migration and relaxation. After the programming, the trapped charge in SiN storage could move both laterally (lateral migration, LM) or vertically (vertical relaxation, VR). The second mechanism is detrapping from the SiN storage layer by trap-assisted tunneling (TAT). On top of these, there is trapping at the BE-tunnel oxide as it includes SiN or a nitrogen-rich layer. Due to the very short distance between the trapping sites at BE and the poly Si channel, the detrapping can occur in a very short time.

The impacts on the Vth distribution and programming algorithms solutions for the short-term data retention will be discussed in a later section.

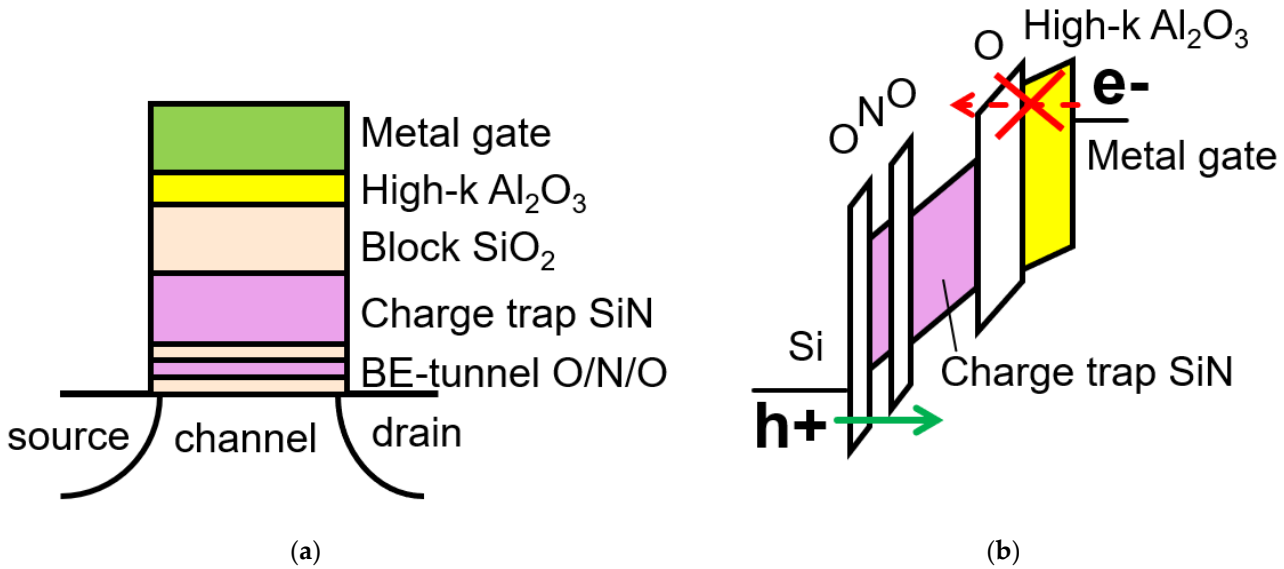



**Figure 7.** (**a**) Cell film stack of the charge-trap cell. (**b**) Band diagram during erase of charge-trap cell. Band-engineered (BE) tunnel dielectrics enhances hole injections while High-k/Metal gate prevents electron back tunneling [35].

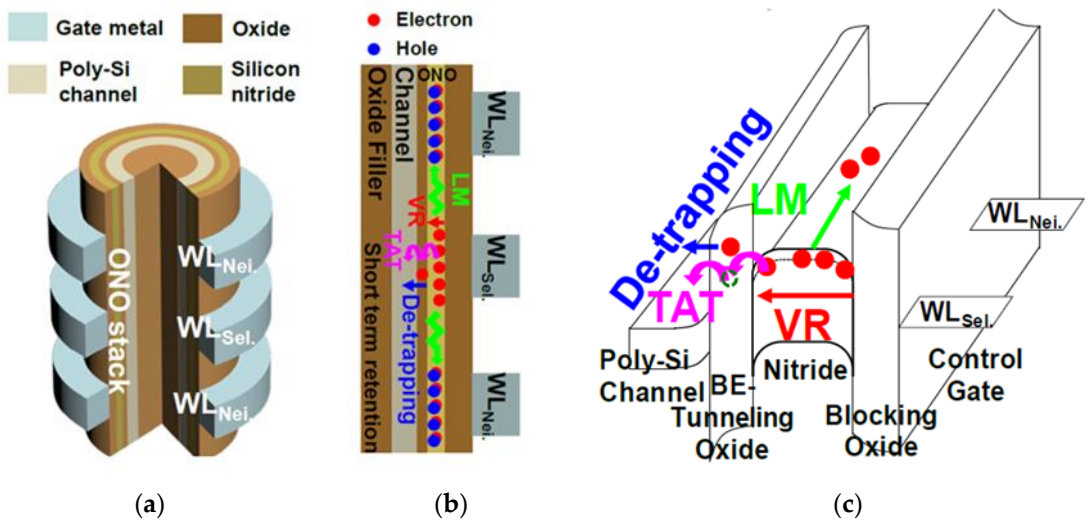



**Figure 8.** (**a**) The bird's eye view and (**b**) cross-sectional view of 2D NAND with charge-trap cells. (**c**) Energy band diagram schematic for short-term retention and possible retention mechanisms. Reprinted with permission from ref. [40], copyright 2020 IEEE.

## 4. 3D NAND Array Physical Scaling by Process Integration

### *4.1. Conventional Scaling*

The physical scaling of the 3D NAND array can be described as XYZ scaling, as shown in Figure 9. XY scaling means reducing the cell footprint. Z scaling means stacking more layers, which is often done together with layer pitch shrink (Z shrink) in order to minimize the increase in the physical height. Z scaling (stacking) has been the main scaling enabler so far. In the ISSCC publications, the steady progress of the layer stacking has been shown, except for in 2020, when the focus was on circuit design technologies for single-level-cells (SLC) and quad-level-cells (QLC) rather than the physical array scaling. In the latest achievement, 176-layer stacked 3D NAND has been demonstrated in both publication and mass production (Figure 10).

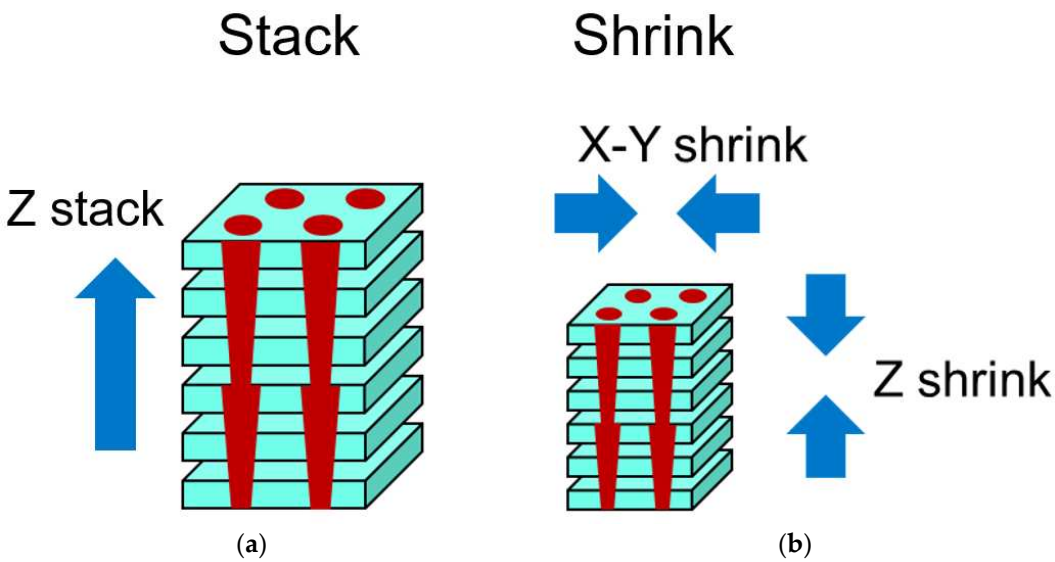



**Figure 9.** XYZ scaling of 3D NAND. (**a**) Layer stacking in Z-direction. (**b**) Footprint shrink of XY dimensions and layer pitch reduction as Z-shrink. Z-shrink is often combined with Z-stack to minimize the increase in the pillar height.

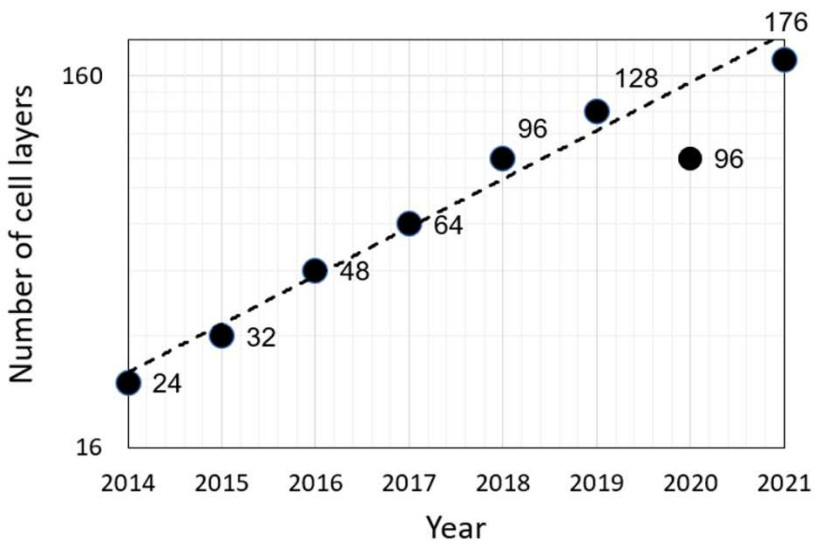



**Figure 10.** The year-by-year trend of cell layer stacking in 3D NAND published in ISSCC conferences. The reverse trend in 2020 is because the publications are about SLC and QLC technologies on the 96-layer NAND baseline.

The effort for XYZ scaling has been focused on efficiency improvement of the pillar (memory hole) layout [41]. Due to the various layout space requirements such as source line contacts, SGD-to-SGD separations, block-to-block separations, the pillar layout is far from the ideal hexagonal close-packed (HCP) layout. There have been continuous improvements in the array layout so that the pillar arrangement has become closer to HCP, enabling XY scaling (Figure 11).

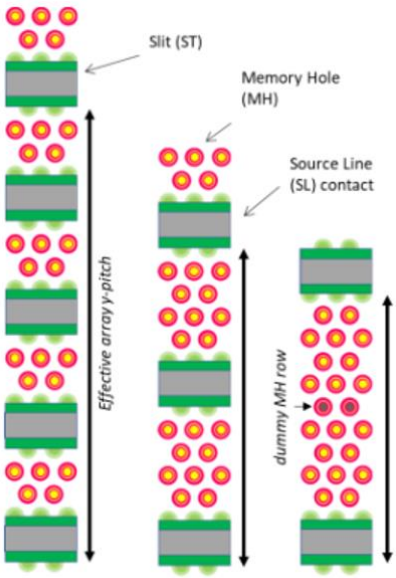
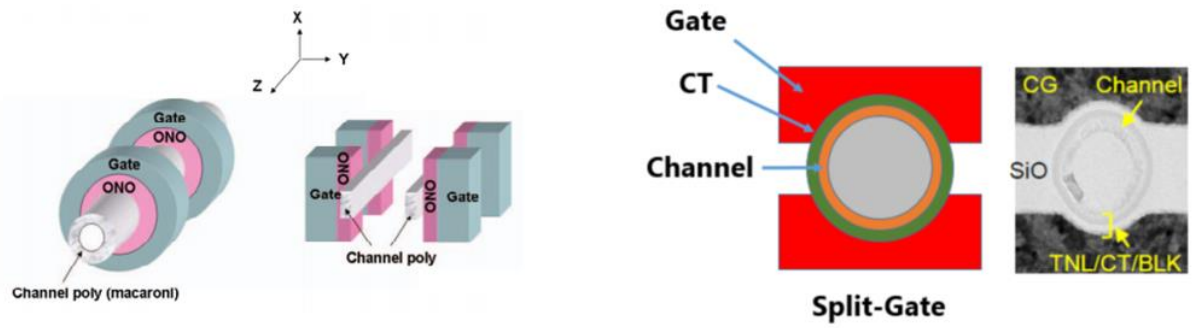



**Figure 11.** XY scaling by pillar (memory hole) layout efficiency improvement. The pillar layout approaches HPC configuration. Reprinted with permission from ref. [41], Copyright 2020 IEEE.

### *4.2. Disruptive Scaling*

As a disruptive XY scaling, the split cells have been investigated (Figure 12). In the conventional 3D NAND, the cell has a cylinder shape. In the split cell, the cell is split into two parts so that the cell density increases. There are two different types of the split cell proposals. One is a planar-like split cell [42] and the other is a half-cylindrical cell [43,44]. The planar-like cell is similar to the 2D NAND cell, while the half-cylindrical cell can be seen as an evolution of the 3D NAND cylindrical cell. For both split cells, the challenges are the process integration of the cell split, the increased cell-to-cell interference and the reduced gate-coupling ratio.




(**a**) (**b**)

**Figure 12.** Split cells with (**a**) planar cell and (**b**) semicylindrical cell. Both of these achieve physical density scaling. The extra cell-to-cell interference needs to be managed to achieve good cell characteristics and high reliability. Reprinted with permission from refs. [42,44], Copyright 2015 and 2019 IEEE, respectively.

As discussed earlier, the pitch shrink of the WL layer is critical to manage the pillar height with layer stacking. In the charge-trap cell, the SiN storage layer is continuous between neighboring cells. With the WL pitch scaling, the trapped charge migration between the neighboring cells would raise the reliability concern. In order to overcome this issue, the SiN storage separation has been proposed (Figure 13) [45]. The process flow is similar to that of 3D FG NAND where the diameter of the pillar etching is smaller

compared to the conventional 3D RG NAND. Therefore, the process integration needs to be well-managed for the successful implementation of the SiN storage separation.

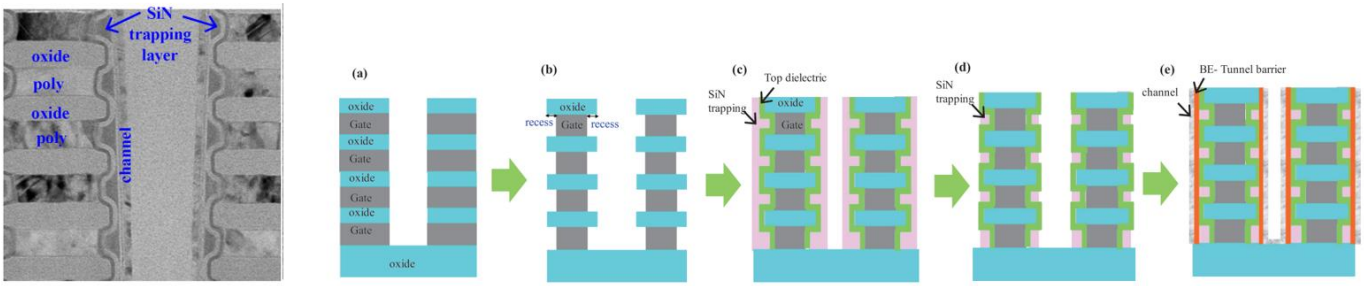



**Figure 13.** Charge-trap cell with the confined SiN storage layer and the process flow. The SiN storage is successfully separated between cells. The pillar etching diameter needs to be smaller compared to the conventional charge-trap cell. Reprinted with permission from ref. [45], Copyright 2019 IEEE.

## 5. 3D NAND Array Logical Scaling by Cell Device Engineering

In addition to the physical cell density scaling, the logical density scaling (i.e., more bits per cell scaling) has been actively pursued in 3D NAND.

Figure 14 shows the number of 3D NAND publications in ISSCC conferences. 3D NAND started as MLC technology and rapidly transitioned to TLC, owing to the excellent cell characteristics and reliability. Recently, QLC technology has been introduced to mass production and the presence of the QLC technology has also been increasing in the publications. Currently, TLC is the mainstream for high-performance and high-endurance usages. QLC is becoming mainstream for the high-density and low-cost usages.

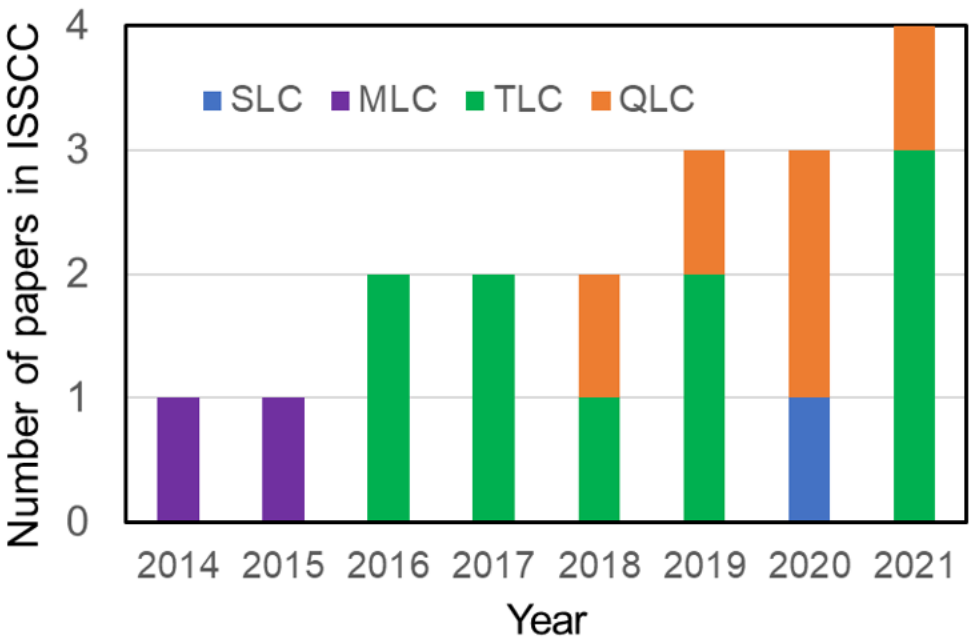
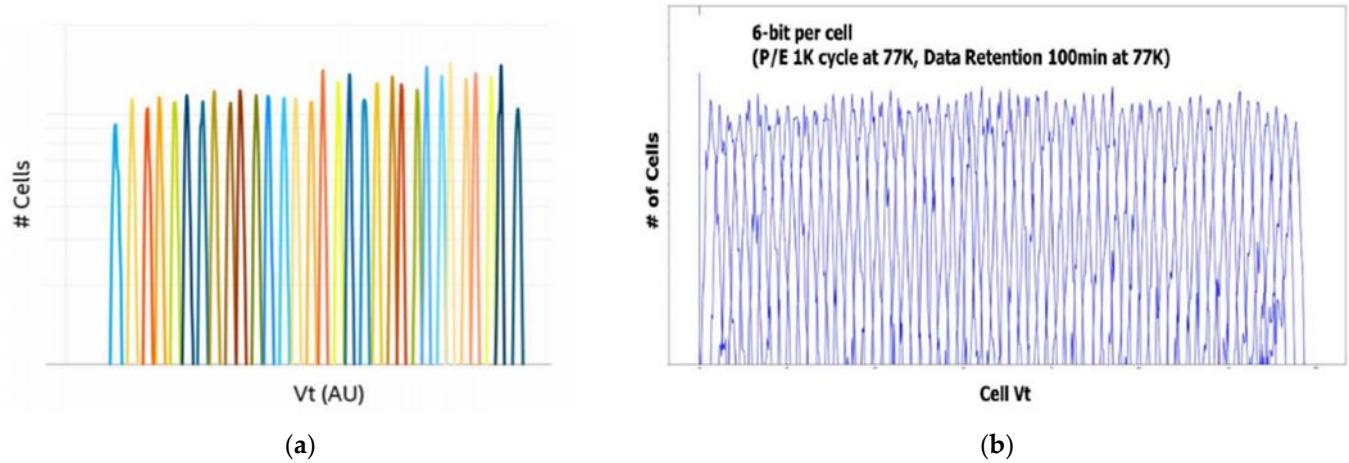



**Figure 14.** 3D NAND publications in ISSCC for SLC, MLC, TLC and QLC technologies. TLC has been the mainstream for 3D NAND. The interest in QLC is rapidly increasing.

Recently, "beyond QLC" efforts have been reported for both FG and charge-trap cells. PLC (5 bits per cell) distributions were shown with FG cells (Figure 15a) [46]. In this work, the excellent data-retention properties of the FG cell were identified as critical to enable PLC. HLC (6 bits per cell) Vth distributions were experimentally shown at a cryogenic temperature of 77 K for charge-trap cells (Figure 15b) [47]. In that work, it was shown that random telegraph noise (RTN) improves at the 77 K while it degrades at 300 K relative

to 358 K. Performance and reliability characteristics as well as the operational conditions warrant further study to enable further bit-per-cell scaling beyond QLC.




(**a**) (**b**)

**Figure 15.** (**a**) PLC (5 bits per cell) Vth distribution with FG cell. (**b**) HLC (6 bits per cell) Vth placement with charge-trap cell at cryogenic temperature of 77 K. Reprinted with permission from refs. [46,47], Copyright 2020 and 2021 IEEE, respectively.

## 6. 3D NAND Performance Scaling by Design and Algorithms

### *6.1. Write Bandwidth for TLC*

Write bandwidth is provided by

$$\textit{Page size} \times \textit{number of planes}/\textit{tProg} \tag{1}$$

Therefore, the large write parallelism (= *page size* × *number of planes*) and short *tProg* are critical to achieve high write bandwidth. Figure 16 shows the trend of TLC write bandwidth from the ISSCC publications. There has been incremental improvement over the years and a steep increase in recent years.

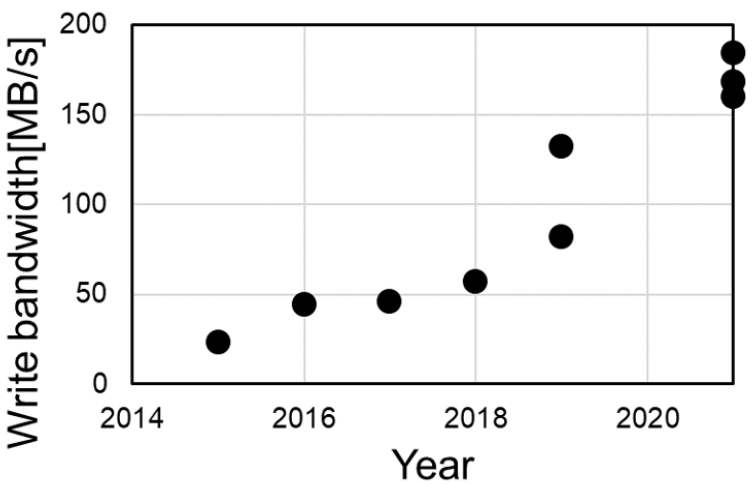



**Figure 16.** TLC write bandwidth trend reported in ISSCC conferences.

The former is due to the continuous improvement of TLC tProg. Figure 17 is the TLC tProg trend published or estimated from ISSCC publications. In TLC RG NAND, all seven programmed states are programmed in a single programming pass. The improvements in tProg are realized by combinations of WL and BL bias time reduction, fine tuning of the programming voltage compensating cell characteristics' variability across the pillar and the reduction in the program verify operations. Figure 18 shows the center XDEC (WL-driver) architecture which shortens the time for WL loading [31].

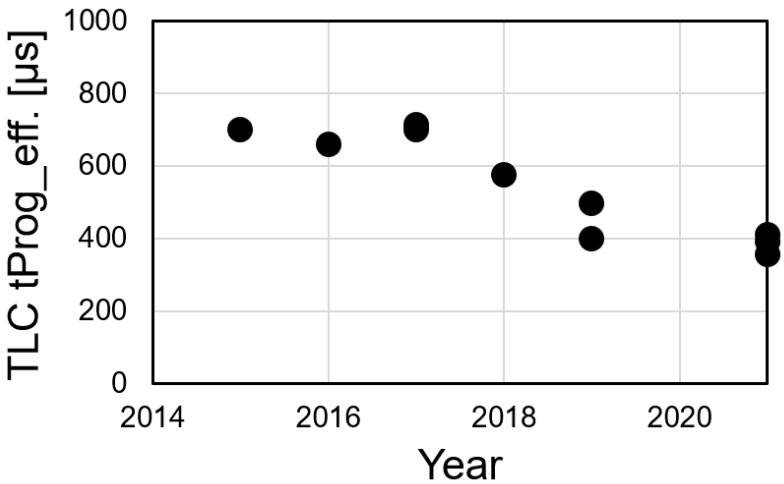



**Figure 17.** TLC effective tProg reported or calculated from ISSCC publications.

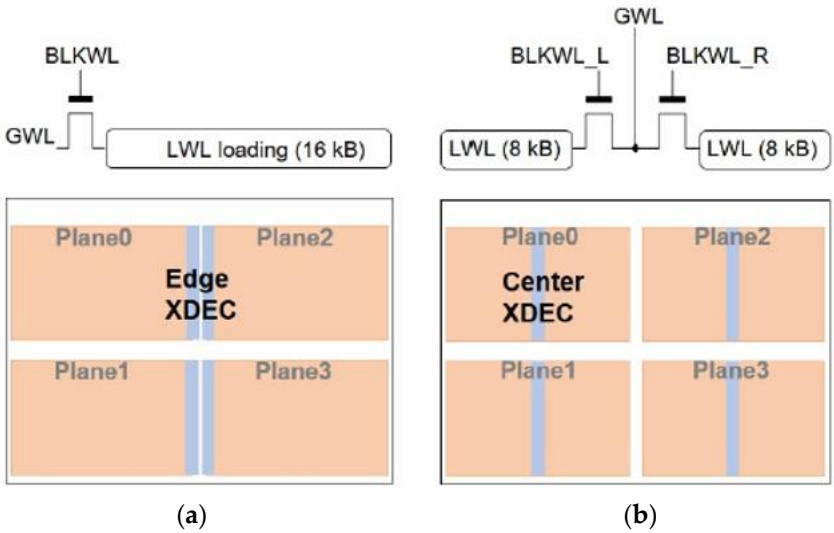



**Figure 18.** XDEC (WL driver) architecture. (**a**) XDEC is placed at the edge of the local WL. (**b**) XDEC is placed at the center of the local WL, reducing the LWL load to a half for faster operations. Reprinted with permission from ref. [31], Copyright 2021 IEEE.

The latter (the steep increase in the write bandwidth) is realized by the increased number of planes owing to the CMOS under Array (CuA) architecture. Figure 19 shows three different CMOS architectures utilized in 3D NAND. In CMOS outside array (CoA), the CMOS circuits are placed next to the array. Therefore, the die size increases if the CMOS area increases. To increase the parallelism, a larger amount of CMOS circuits such as page buffer circuits need to be placed, which results in the increase in the die size. In the CMOS under Array (CuA), the CMOS circuits are placed under the array. More parallelism (more planes) can be realized with CuA because the larger area is available for CMOS circuits. Another variation is to place the CMOS over array by using wafer bonding technologies (Wafer on wafer, WoW) [48]. With this architecture, CMOS is processed separately from the array processing by using a dedicated wafer for CMOS. Therefore, the process flow can be optimized for CMOS devices and interconnect.

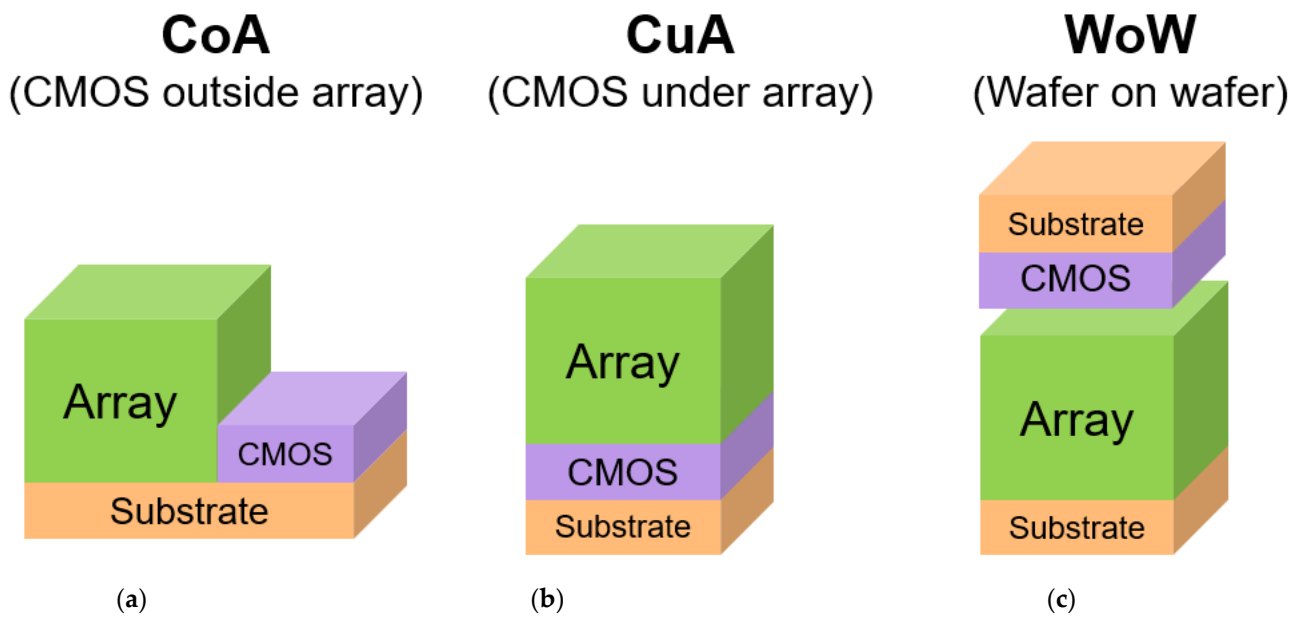



**Figure 19.** 3D NAND architectures for CMOS placement. (**a**) CMOS outside array (CoA); (**b**) CMOS under Array (CuA), (**c**) Wafer on wafer bonding (WoW).

Figure 20 shows the number of publications in ISSCC for CNA and CuA. After CuA was presented in 2016 for the first time in an ISSCC conference, publications with CuA have been increasing, and most of the recent 3D NAND publications are for CuA. CuA technology is now the mainstream for 3D NAND.

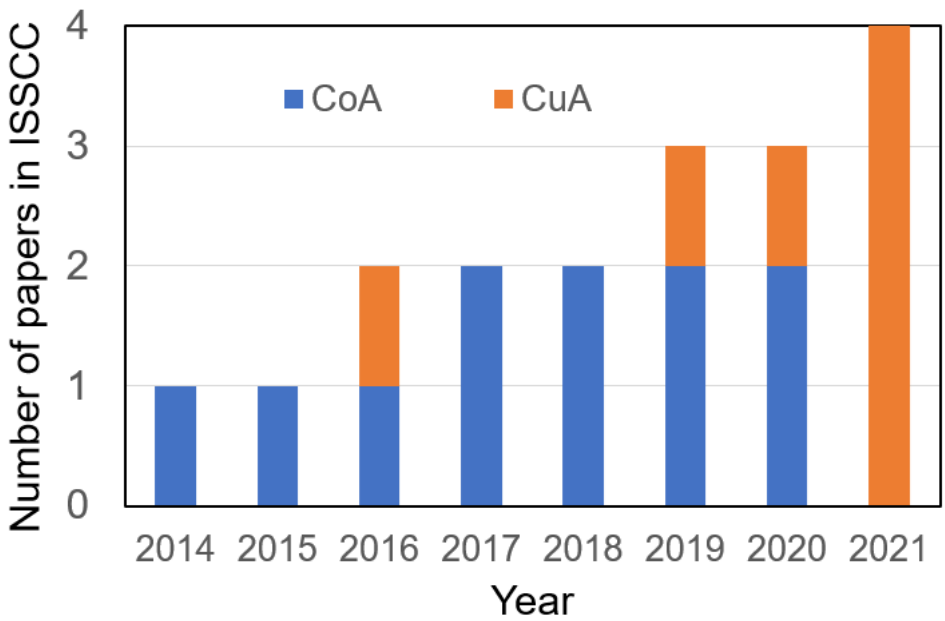



**Figure 20.** 3D NAND publications in ISSCC for CMOS outside array (CoA) and CMOS under array (CuA) architectures. All publications in 2021 are for CuA.

### *6.2. QLC Program Schemes*

QLC tProg is much longer than TLC tProg (as shown in Figure 21), in order to realize the tight Vth distributions. As discussed earlier, in RG NAND with the charge-trap cells, there is a phenomenon known as short-term data retention. This causes shift and widening of Vth distributions right after programming. To realize the tight Vth distributions for QLC, it is important to manage the short-term data retention effects.

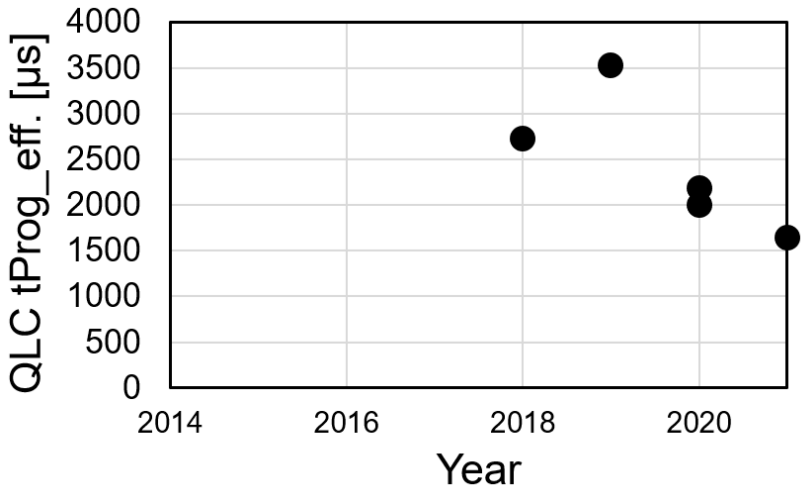



**Figure 21.** QLC effective tProg reported or calculated from ISSCC publications.

The coarse–fine programming scheme has been introduced for QLC RG NAND [26]. As shown in Figure 22a, all 16 levels are programmed in the first pass with relatively wide distribution widths. Due to the short-term data retention, the Vth distributions shift and widen right after the coarse programming. The fine programming is performed as the second programming path, which tightens the Vth distributions by touching up the distribution tails caused by the short-term data retention. This scheme can be called the 16-16 scheme as the 16-level programming is performed twice. To reduce QLC tProg, an 8-16 scheme was proposed (Figure 22b). With the 8-16 scheme, eight levels are programmed at the coarse programming pass, contributing to the tProg reduction.

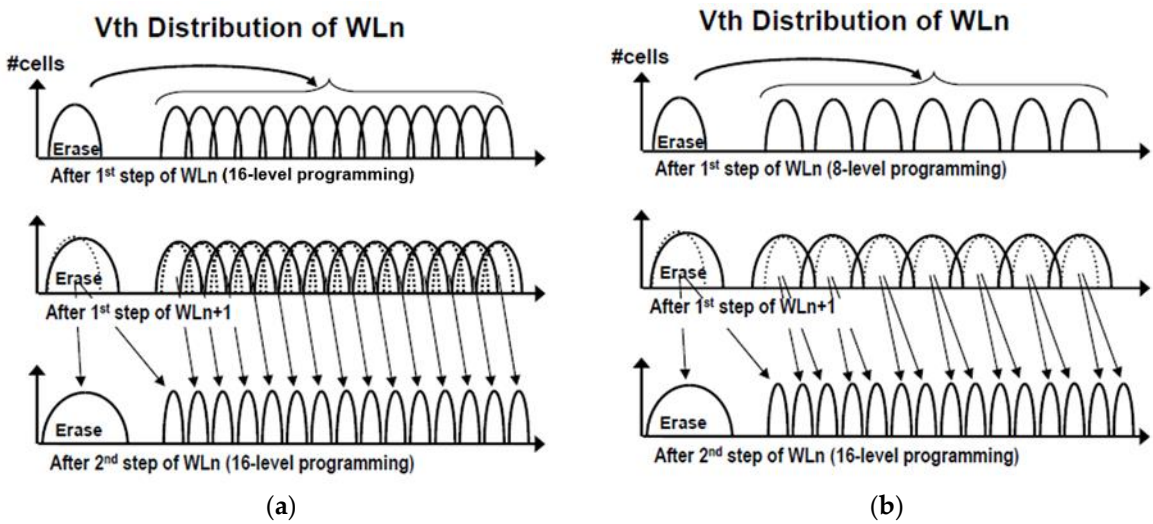


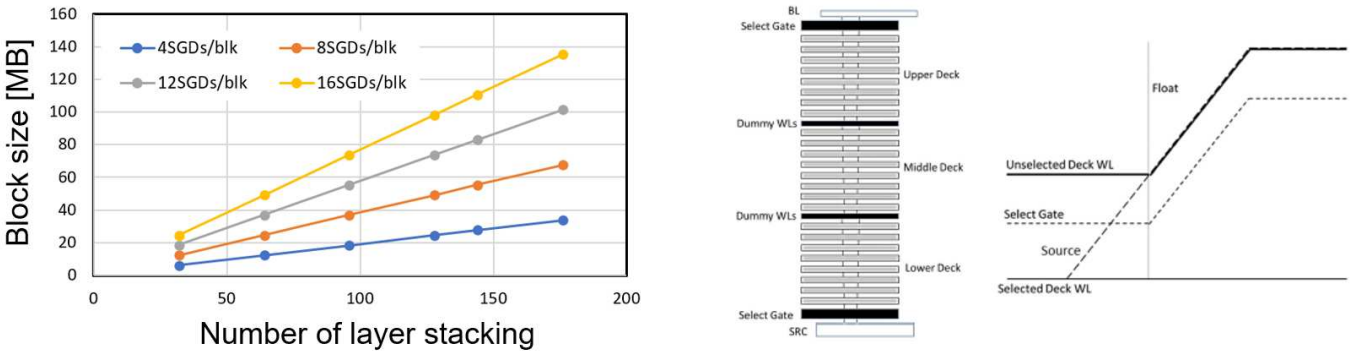

**Figure 22.** QLC coarse–fine programming schemes with (**a**) 16-16 scheme and (**b**) 8-16 scheme. 16-16 is more efficient to compensate the short-term retention while the 8-16 scheme would have tProg advantage. Reprinted with permission from ref. [26], Copyright 2019 IEEE.

In the FG NAND, the first programming pass only has four levels. The 16 levels are then completed at the second pass [30] because the short-term retention is much smaller in the FG cell and does not require the touch-up operation.

So far, 1.6–2 msec tProg has been reported for QLC and ~0.4 msec tProg has been reported for TLC. For the further enhancement of QLC tProg, solving the short-term data retention by programming scheme and cell improvement is critical.

### 6.3. Block Size Scaling

With the WL stacking increasing, the block size increases. Figure 23a shows the TLC block size as a function of number of WL stacking. The number of SGDs per block is chosen as a parameter. Typically, FG NAND runs 12–16 SGDs/block, while RG NAND has 4–8 SGDs/blocks. Given that the block size is the minimum granularity of erase, the increase in the block size could increase the system burden of the data management and would degrade system performance. In order to mitigate this problem, the block-by-deck scheme was proposed (Figure 23b) [30]. In this scheme, the NAND string is divided into multiple segments (three segments in this example) and each segment is treated as a different block. During erase operation, the entire pillar is biased to the erase voltage. The WLs of the selected deck block are grounded while the WLs of the unselected deck blocks are ramped to the channel potential. In this way, the cells in the unselected deck blocks can be inhibited for erase.




(**a**) (**b**)

**Figure 23.** (**a**) Block size scaling as a function of number of layer stacking. (**b**) Block-by-deck erase scheme. The conventional physical block is divided into three logical blocks [30]. Reprinted with permission from ref. [23], Copyright 2021 IEEE.

## 7. Conclusions

3D NAND scaling has been successfully achieved. The layer stacking has reached 176 layers. QLC has been introduced in both FG NAND and RG NAND. Research on PLC is active, with partial demonstrations for cell capability. CMOS under array (CuA) has been widely adopted and enables performance enhancement by increasing the number of planes. For future scaling, on top of the continuous XYZ physical scaling, disruptive technologies such as split cells are proposed. Program and erase schemes are being developed further to solve cell reliability challenges and block size scaling challenges.

**Funding:** This research received no external funding.

**Conflicts of Interest:** The author declares no conflict of interest.

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# Exhibit B

# Crucial X9 Portable SSD

## Hard days are over

### Get durable storage wherever you need it

Dependable storage for your favorite devices, wherever you go — that's what the Crucial® X9 Portable SSD offers. With speedy file transfers up to 1,050MB/s[1] and up to 4TB[2] of storage for all your favorite photos, videos, games and more, the Crucial X9 is up to 7.5x faster[3] than portable hard drives, drop proof[4] up to 7.5 feet (2 meters) and compatible[5] with PCs, Macs, tablets, gaming consoles, Android™ phones, and more, making it the perfect plug-and-play storage solution.

| 4TB | 2TB | 1TB |
|---|---|---|
| Up to 20,000 photos, 50 hours of family video, 10 AAA game titles, and 100GB of documents, with 400GB to spare[6] | Up to 10,000 photos, 25 hours of family video, 5 AAA game titles, and 50GB of documents, with 200GB to spare[6] | Up to 5,000 photos, 15 hours of family video, 2 AAA game titles, and 50GB of documents, with 100GB to spare[6] |

## Best For

Affordable added storage for typical consumer workloads and backups

## Key Features

- Read speeds up to 1,050MB/s[1]
- Capacities of 4, 2 and 1TB[2]
- Drop proof[4] up to 7.5 feet/2 meters without data loss, and extreme temperature, shock and vibration proof
- Mini 65 x 50 mm enclosure
- Lanyard hole
- Plug-and-play compatibility[5] with Windows, Mac, Android™, iPad, Xbox®, PlayStation® and more
- USB Type-C to C connection[7]
- Ships in exFAT format; can be reformatted into NTFS, APFS and more[8]
- 3-year limited warranty[9]

## Expand your storage

Skip the monthly cloud storage fee and save more of the games, photos, videos and files you love with read speeds up to 1,050MB/s[1]. Load files up to 7.5x faster[3] than portable hard drives and 100x faster[3] than USB flash drives.

## Plug-and-play compatibility

With an easy USB-C connection[7], the Crucial X9 Portable SSD is the perfect compatible[5] storage solution for your PC, Mac, tablet, gaming console, Android™ and more.

## On-the-go durability

Unlike fragile portable hard drives, the Crucial X9 Portable SSD is durable and dependable. Shock, vibration and drop proof[4] up to 7.5 feet, the X9 is also built to withstand fluctuations in temperature.

## Back up everything that matters

Never lose another file, photo or video. Instead, back up all your favorite things to your Crucial X9 Portable SSD, available in capacities up to 4TB. The X9 works with Windows File History, Apple Time Machine and Acronis True Image.

## Trusted quality, practical design

Engineered by Micron®, the Crucial X9 Portable SSD is lightweight yet durable in a 65 x 50 mm polycarbonate design that includes an integrated lanyard hole for ultimate portability.

| Crucial® X9 Portable SSD | | | |
|---|---|---|---|
| **Capacity** | **Part number** | **Box contents** | **Sequenatial read** |
| 4TB | CT4000X9SSD9 | Crucial X9 Portable SSD<br>USB Type-C to Type-C USB cable<br>Quick-Start Guide | Up to<br>1,050MBs |
| 2TB | CT2000X9SSD9 | | |
| 1TB | CT1000X9SSD9 | | |

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1. MB/s speed measured by Crucial as maximum sequential performance of device on a high-performance desktop computer with Crystal Disk Mark (version 8.0.4 for x64). Your performance may vary.
2. Some of the storage capacity is used for formatting and other purposes and is not available for data storage. 1GB equals 1 billion bytes.
3. Comparative speed claims measured against maximum reported speeds from mainstream portable HDD manufacturers. Your performance may vary.
4. Up to 7.5 ft/2 meters without impact to data on a carpeted floor.
5. Compatibility may vary and may be contingent on device formatting and host capabilities. Compatible Android devices must be able to work with USB Mass Storage over OTG. Operating system updates and reformatting may be required.
6. Based on average photo size of 6MB, video at 4K/60fps in H264 format at 24GB/hr and 200GB for AAA games.
7. Best speeds available with USB Type-C to C cable on USB 3.2 Gen2 supported devices. Use USB Type-A adapter for older devices.
8. Ships in exFAT format. Can be reformatted into NTFS, APFS or other formats. Reformatting will result in loss of data from the drive.
9. Warranty valid for 3 years from the original date of purchase by an authorized seller, or before writing the maximum total bytes written (TBW) as published in the product datasheet and as measured in the product's SMART data, whichever comes first.

JS 44 (Rev. 10/20)

# CIVIL COVER SHEET

The JS 44 civil cover sheet and the information contained herein neither replace nor supplement the filing and service of pleadings or other papers as required by law, except as provided by local rules of court. This form, approved by the Judicial Conference of the United States in September 1974, is required for the use of the Clerk of Court for the purpose of initiating the civil docket sheet. *(SEE INSTRUCTIONS ON NEXT PAGE OF THIS FORM.)*

**I. (a) PLAINTIFFS**

Palisade Technologies, LLP

**(b)** County of Residence of First Listed Plaintiff _____
*(EXCEPT IN U.S. PLAINTIFF CASES)*

**(c)** Attorneys *(Firm Name, Address, and Telephone Number)*

See attached.

**DEFENDANTS**

Micron Technology, Inc; Micron Semiconductor Products, Inc.; and Micron Technology Texas LLC

County of Residence of First Listed Defendant _____
*(IN U.S. PLAINTIFF CASES ONLY)*

NOTE: IN LAND CONDEMNATION CASES, USE THE LOCATION OF THE TRACT OF LAND INVOLVED.

Attorneys *(If Known)*

## II. BASIS OF JURISDICTION *(Place an "X" in One Box Only)*

- [ ] 1 U.S. Government Plaintiff
- [x] 3 Federal Question *(U.S. Government Not a Party)*
- [ ] 2 U.S. Government Defendant
- [ ] 4 Diversity *(Indicate Citizenship of Parties in Item III)*

## III. CITIZENSHIP OF PRINCIPAL PARTIES *(Place an "X" in One Box for Plaintiff and One Box for Defendant)*
*(For Diversity Cases Only)*

| | PTF | DEF | | PTF | DEF |
|---|---|---|---|---|---|
| Citizen of This State | [ ] 1 | [ ] 1 | Incorporated *or* Principal Place of Business In This State | [ ] 4 | [ ] 4 |
| Citizen of Another State | [ ] 2 | [ ] 2 | Incorporated *and* Principal Place of Business In Another State | [ ] 5 | [ ] 5 |
| Citizen or Subject of a Foreign Country | [ ] 3 | [ ] 3 | Foreign Nation | [ ] 6 | [ ] 6 |

## IV. NATURE OF SUIT *(Place an "X" in One Box Only)*

Click here for: Nature of Suit Code Descriptions.

**CONTRACT**
- [ ] 110 Insurance
- [ ] 120 Marine
- [ ] 130 Miller Act
- [ ] 140 Negotiable Instrument
- [ ] 150 Recovery of Overpayment & Enforcement of Judgment
- [ ] 151 Medicare Act
- [ ] 152 Recovery of Defaulted Student Loans (Excludes Veterans)
- [ ] 153 Recovery of Overpayment of Veteran's Benefits
- [ ] 160 Stockholders' Suits
- [ ] 190 Other Contract
- [ ] 195 Contract Product Liability
- [ ] 196 Franchise

**REAL PROPERTY**
- [ ] 210 Land Condemnation
- [ ] 220 Foreclosure
- [ ] 230 Rent Lease & Ejectment
- [ ] 240 Torts to Land
- [ ] 245 Tort Product Liability
- [ ] 290 All Other Real Property

**TORTS**

**PERSONAL INJURY**
- [ ] 310 Airplane
- [ ] 315 Airplane Product Liability
- [ ] 320 Assault, Libel & Slander
- [ ] 330 Federal Employers' Liability
- [ ] 340 Marine
- [ ] 345 Marine Product Liability
- [ ] 350 Motor Vehicle
- [ ] 355 Motor Vehicle Product Liability
- [ ] 360 Other Personal Injury
- [ ] 362 Personal Injury - Medical Malpractice

**PERSONAL INJURY**
- [ ] 365 Personal Injury - Product Liability
- [ ] 367 Health Care/ Pharmaceutical Personal Injury Product Liability
- [ ] 368 Asbestos Personal Injury Product Liability

**PERSONAL PROPERTY**
- [ ] 370 Other Fraud
- [ ] 371 Truth in Lending
- [ ] 380 Other Personal Property Damage
- [ ] 385 Property Damage Product Liability

**CIVIL RIGHTS**
- [ ] 440 Other Civil Rights
- [ ] 441 Voting
- [ ] 442 Employment
- [ ] 443 Housing/ Accommodations
- [ ] 445 Amer. w/Disabilities - Employment
- [ ] 446 Amer. w/Disabilities - Other
- [ ] 448 Education

**PRISONER PETITIONS**

**Habeas Corpus:**
- [ ] 463 Alien Detainee
- [ ] 510 Motions to Vacate Sentence
- [ ] 530 General
- [ ] 535 Death Penalty

**Other:**
- [ ] 540 Mandamus & Other
- [ ] 550 Civil Rights
- [ ] 555 Prison Condition
- [ ] 560 Civil Detainee - Conditions of Confinement

**FORFEITURE/PENALTY**
- [ ] 625 Drug Related Seizure of Property 21 USC 881
- [ ] 690 Other

**LABOR**
- [ ] 710 Fair Labor Standards Act
- [ ] 720 Labor/Management Relations
- [ ] 740 Railway Labor Act
- [ ] 751 Family and Medical Leave Act
- [ ] 790 Other Labor Litigation
- [ ] 791 Employee Retirement Income Security Act

**IMMIGRATION**
- [ ] 462 Naturalization Application
- [ ] 465 Other Immigration Actions

**BANKRUPTCY**
- [ ] 422 Appeal 28 USC 158
- [ ] 423 Withdrawal 28 USC 157

**PROPERTY RIGHTS**
- [ ] 820 Copyrights
- [x] 830 Patent
- [ ] 835 Patent - Abbreviated New Drug Application
- [ ] 840 Trademark
- [ ] 880 Defend Trade Secrets Act of 2016

**SOCIAL SECURITY**
- [ ] 861 HIA (1395ff)
- [ ] 862 Black Lung (923)
- [ ] 863 DIWC/DIWW (405(g))
- [ ] 864 SSID Title XVI
- [ ] 865 RSI (405(g))

**FEDERAL TAX SUITS**
- [ ] 870 Taxes (U.S. Plaintiff or Defendant)
- [ ] 871 IRS—Third Party 26 USC 7609

**OTHER STATUTES**
- [ ] 375 False Claims Act
- [ ] 376 Qui Tam (31 USC 3729(a))
- [ ] 400 State Reapportionment
- [ ] 410 Antitrust
- [ ] 430 Banks and Banking
- [ ] 450 Commerce
- [ ] 460 Deportation
- [ ] 470 Racketeer Influenced and Corrupt Organizations
- [ ] 480 Consumer Credit (15 USC 1681 or 1692)
- [ ] 485 Telephone Consumer Protection Act
- [ ] 490 Cable/Sat TV
- [ ] 850 Securities/Commodities/ Exchange
- [ ] 890 Other Statutory Actions
- [ ] 891 Agricultural Acts
- [ ] 893 Environmental Matters
- [ ] 895 Freedom of Information Act
- [ ] 896 Arbitration
- [ ] 899 Administrative Procedure Act/Review or Appeal of Agency Decision
- [ ] 950 Constitutionality of State Statutes

## V. ORIGIN *(Place an "X" in One Box Only)*

- [x] 1 Original Proceeding
- [ ] 2 Removed from State Court
- [ ] 3 Remanded from Appellate Court
- [ ] 4 Reinstated or Reopened
- [ ] 5 Transferred from Another District *(specify)*
- [ ] 6 Multidistrict Litigation - Transfer
- [ ] 8 Multidistrict Litigation - Direct File

## VI. CAUSE OF ACTION

Cite the U.S. Civil Statute under which you are filing ***(Do not cite jurisdictional statutes unless diversity)***:
35 USC 271

Brief description of cause:
Patent infringement

## VII. REQUESTED IN COMPLAINT:

[ ] CHECK IF THIS IS A **CLASS ACTION** UNDER RULE 23, F.R.Cv.P.

**DEMAND $**

CHECK YES only if demanded in complaint:
**JURY DEMAND:** [x] Yes [ ] No

## VIII. RELATED CASE(S) IF ANY

*(See instructions):* JUDGE _____ DOCKET NUMBER _____

DATE
10/16/2024

SIGNATURE OF ATTORNEY OF RECORD
/s/ Mark D. Siegmund

**FOR OFFICE USE ONLY**

RECEIPT # _____ AMOUNT _____ APPLYING IFP _____ JUDGE _____ MAG. JUDGE _____

# INSTRUCTIONS FOR ATTORNEYS COMPLETING CIVIL COVER SHEET FORM JS 44

Authority For Civil Cover Sheet

The JS 44 civil cover sheet and the information contained herein neither replaces nor supplements the filings and service of pleading or other papers as required by law, except as provided by local rules of court. This form, approved by the Judicial Conference of the United States in September 1974, is required for the use of the Clerk of Court for the purpose of initiating the civil docket sheet. Consequently, a civil cover sheet is submitted to the Clerk of Court for each civil complaint filed. The attorney filing a case should complete the form as follows:

**I.(a)** **Plaintiffs-Defendants.** Enter names (last, first, middle initial) of plaintiff and defendant. If the plaintiff or defendant is a government agency, use only the full name or standard abbreviations. If the plaintiff or defendant is an official within a government agency, identify first the agency and then the official, giving both name and title.

**(b)** **County of Residence.** For each civil case filed, except U.S. plaintiff cases, enter the name of the county where the first listed plaintiff resides at the time of filing. In U.S. plaintiff cases, enter the name of the county in which the first listed defendant resides at the time of filing. (NOTE: In land condemnation cases, the county of residence of the "defendant" is the location of the tract of land involved.)

**(c)** **Attorneys.** Enter the firm name, address, telephone number, and attorney of record. If there are several attorneys, list them on an attachment, noting in this section "(see attachment)".

**II.** **Jurisdiction.** The basis of jurisdiction is set forth under Rule 8(a), F.R.Cv.P., which requires that jurisdictions be shown in pleadings. Place an "X" in one of the boxes. If there is more than one basis of jurisdiction, precedence is given in the order shown below.
United States plaintiff. (1) Jurisdiction based on 28 U.S.C. 1345 and 1348. Suits by agencies and officers of the United States are included here.
United States defendant. (2) When the plaintiff is suing the United States, its officers or agencies, place an "X" in this box.
Federal question. (3) This refers to suits under 28 U.S.C. 1331, where jurisdiction arises under the Constitution of the United States, an amendment to the Constitution, an act of Congress or a treaty of the United States. In cases where the U.S. is a party, the U.S. plaintiff or defendant code takes precedence, and box 1 or 2 should be marked.
Diversity of citizenship. (4) This refers to suits under 28 U.S.C. 1332, where parties are citizens of different states. When Box 4 is checked, the citizenship of the different parties must be checked. (See Section III below**; NOTE: federal question actions take precedence over diversity cases.**)

**III.** **Residence (citizenship) of Principal Parties.** This section of the JS 44 is to be completed if diversity of citizenship was indicated above. Mark this section for each principal party.

**IV.** **Nature of Suit.** Place an "X" in the appropriate box. If there are multiple nature of suit codes associated with the case, pick the nature of suit code that is most applicable. Click here for: Nature of Suit Code Descriptions.

**V.** **Origin.** Place an "X" in one of the seven boxes.
Original Proceedings. (1) Cases which originate in the United States district courts.
Removed from State Court. (2) Proceedings initiated in state courts may be removed to the district courts under Title 28 U.S.C., Section 1441.
Remanded from Appellate Court. (3) Check this box for cases remanded to the district court for further action. Use the date of remand as the filing date.
Reinstated or Reopened. (4) Check this box for cases reinstated or reopened in the district court. Use the reopening date as the filing date.
Transferred from Another District. (5) For cases transferred under Title 28 U.S.C. Section 1404(a). Do not use this for within district transfers or multidistrict litigation transfers.
Multidistrict Litigation – Transfer. (6) Check this box when a multidistrict case is transferred into the district under authority of Title 28 U.S.C. Section 1407.
Multidistrict Litigation – Direct File. (8) Check this box when a multidistrict case is filed in the same district as the Master MDL docket.
**PLEASE NOTE THAT THERE IS NOT AN ORIGIN CODE 7.** Origin Code 7 was used for historical records and is no longer relevant due to changes in statue.

**VI.** **Cause of Action.** Report the civil statute directly related to the cause of action and give a brief description of the cause. **Do not cite jurisdictional statutes unless diversity.** Example: U.S. Civil Statute: 47 USC 553 Brief Description: Unauthorized reception of cable service.

**VII.** **Requested in Complaint.** Class Action. Place an "X" in this box if you are filing a class action under Rule 23, F.R.Cv.P.
Demand. In this space enter the actual dollar amount being demanded or indicate other demand, such as a preliminary injunction.
Jury Demand. Check the appropriate box to indicate whether or not a jury is being demanded.

**VIII.** **Related Cases.** This section of the JS 44 is used to reference related pending cases, if any. If there are related pending cases, insert the docket numbers and the corresponding judge names for such cases.

**Date and Attorney Signature.** Date and sign the civil cover sheet.

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