

**IN THE UNITED STATES DISTRICT COURT
FOR THE WESTERN DISTRICT OF TEXAS
MIDLAND/ODESSA DIVISION**

PALISADE TECHNOLOGIES, LLP,

Plaintiff

v.

MICRON TECHNOLOGY, INC. and
MICRON SEMICONDUCTOR
PRODUCTS, INC.,

Defendants.

Case No. 7:24-cv-00262-DC-DTG

Jury Trial Demanded

**DEFENDANTS' PRELIMINARY INVALIDITY CONTENTIONS FOR
U.S. PATENT NOS. 8,148,962; 8,327,051; AND 9,281,314**

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I. Introduction

Defendants Micron Technology, Inc. and Micron Semiconductor Products, Inc. (collectively, “Defendants” or “Micron”) submit its Preliminary Invalidity Contentions for U.S. Patent Nos. 8,148,962; 8,327,051; and 9,281,314 (“Invalidity Contentions”) to Plaintiff Palisade Technologies, LLP (“Plaintiff” or “Palisade”) pursuant to the Court’s Order Governing Proceedings in Patent Cases.¹

In Plaintiff’s Preliminary Infringement Contentions (“Infringement Contentions”), served April 16, 2025, Plaintiff asserted the following claims of each patent against Micron.

U.S. Patent No.	Asserted Claim(s)
8,148,962	1, 7-11, 14
8,327,051	1-2, 4-6, 8, 16-17, 21, 23-25, 27
9,281,314	1, 3, 5-6, 13, 17-18

Micron’s Invalidity Contentions address only those claims asserted in Plaintiff’s Infringement Contentions. Micron provides these Invalidity Contentions without waiving any argument about the sufficiency or substance of Plaintiff’s Infringement Contentions.

Based on its investigation to date, Micron hereby: (a) identifies each item of prior art that anticipates each asserted claim or renders it obvious; (b) specifies whether each such item of prior art anticipates each asserted claim or renders it obvious and, if a combination of items of

¹ On May 14, 2025, the Court granted Defendants’ unopposed motion to extend the service deadline for invalidity contentions for U.S. Patent Nos. 8,996,838 and 9,524,974 to July 3, 2025. ECF No. 48.

prior art makes a claim obvious, identifies each such combination and the motivation to combine such items; (c) provides a chart identifying where specifically in each item of prior art each element of each asserted claim is found, including for each element that is governed by pre-AIA 35 U.S.C. § 112 ¶ 6 and/or 35 U.S.C. § 112(f), the identity of the structure(s), act(s), or material(s) in each item of prior art that performs the claimed function; (d) identifies any grounds of invalidity of the asserted claims based on indefiniteness under pre-AIA 35 U.S.C. § 112 ¶ 2 and/or 35 U.S.C. § 112(b), or enablement or written description under pre-AIA 35 U.S.C. § 112 ¶ 1 and/or 35 U.S.C. § 112(a); and (e) identifies any grounds of invalidity of the asserted claims directed to ineligible subject matter under 35 U.S.C. § 101.

In addition, based on its investigation to date, Micron has produced or is producing documents concurrently with these Invalidity Contentions.

II. Reservations

Defendants reserve the right to amend these Invalidity Contentions. The information and documents that Defendants produce are based on information available to date and are subject to further revision.

The information and documents that Defendants produce are based on Defendants' present understanding of Plaintiff's infringement theories as advanced by Plaintiff in its Infringement Contentions. Plaintiff's Infringement Contentions are deficient in numerous respects. For example, although Plaintiff lists hundreds of product models as accused products in its Infringement Contentions, the accompanying claim charts include analysis for only four models. Thus, Plaintiff has failed to identify specifically where each element of each asserted claim is found within each accused instrumentality. If Plaintiff attempts or is permitted to cure such deficiencies, amends its contentions, or provides additional information regarding its

- Claim 23: “at least two pins of the USB port are parallel to at least two pins of the I/O port.”
- Claim 24: “layout for the USB port is different from layout of the I/O port.”
- Claim 27: “wherein all of the multiple data pins are not electrically connected to the I/O controller circuitry”

V. U.S. Patent No. 9,281,314 (“’314 Patent”)

A. Invalidity Contentions Under 35 U.S.C. §§ 102 And 103

1. Identification of Prior Art

In addition to the prior art cited on the face of the ’314 Patent and related patents, the admitted prior art in the specifications of the ’314 Patent and related patents, the prior art cited in any file histories, reexaminations, *inter partes* review proceedings, reissue proceedings, or other examination or post-grant proceedings of the ’314 Patent and related patents, and the prior art cited in any invalidity contentions or expert reports submitted in any action or proceedings involving the ’314 Patent or related patents, Defendants identify the following prior art that anticipates each asserted claim or renders it obvious.

a) Prior Art Patents

The following patents and patent publications are prior art to the asserted claims under at least 35 U.S.C. §§ 102(a)(1), (a)(2), and/or 35 U.S.C. § 103. The identification of any patent or patent publication shall be deemed to include any counterpart patent or application filed, published, or issued anywhere in the world.

Patent or Publication Number	Country of Origin	Filing Date	Date of Issue or Publication
U.S. Patent App. Pub. No. 2014/0159132 (“Daycock”)	U.S.	12/6/2012	6/12/2014
U.S. Patent App. Pub. No. 2007/0096202 (“Kang ’202”)	U.S.	10/20/2006	5/3/2007

Patent or Publication Number	Country of Origin	Filing Date	Date of Issue or Publication
U.S. Patent No. 7,598,564 ("Kang '564")	U.S.	5/31/2006	10/6/2009
U.S. Patent App. Pub. No. 2013/0193504 ("Kinoshita")	U.S.	1/24/2013	8/1/2013
U.S. Patent No. 7,759,722 ("Murata")	U.S.	6/20/2007	7/20/2010
U.S. Patent App. Pub. No. 2011/0309425 ("Purayath")	U.S.	6/16/2011	12/22/2011
U.S. Patent No. 7,705,392 ("Yonemochi")	U.S.	4/13/2006	4/27/2010
U.S. Patent App. Pub. No. 2006/0205148 ("Deppe")	U.S.	3/11/2005	9/14/2006
U.S. Patent App. Pub. No. 2015/0014762 ("Ohnuki")	U.S.	2/11/2014	1/15/2015
U.S. Patent App. Pub. No. 2015/0380431 ("Kanamori")	U.S.	3/9/2015; (Claims priority to Korean Application No. 10-2014-0078205, filed on June 25, 2014)	12/31/2015
U.S. Patent App. Pub. No. 2010/0117141 ("Shin")	U.S.	11/12/2009	5/13/2010
U.S. Patent No. 8,492,797 ("Hwang")	KR	4/7/2011	7/23/2013

b) Prior Art Non-Patent Publications

The following non-patent publications are prior art to the asserted claims under at least 35 U.S.C. §§ 102(a)(1), (a)(2), and/or 35 U.S.C. § 103.

Title	Author/Publisher	Date of Publication
<i>Memory Detailed Structural Analysis of the Toshiba TC58NVG3D4CTG00 70nm 8Gb MLC NAND Flash</i> , SAR-3843 ("TechInsights SAR-3843")	Xu Chang, TechInsights	May 31, 2006

Title	Author/Publisher	Date of Publication
<i>Full Electrical Reverse and Reliability Characterization on 8Gb MLC 70nm NAND Toshiba</i>	Dario Romio, Guglielmo Russo & Angelo Visconti, STMicroelectronics	July 2006
<i>Toshiba and SanDisk Develop 8-Gigabit NAND Flash Memory Chip With 70 nm Process Technology (“Toshiba”)</i>	Toshiba, https://www.global.toshiba/ww/news/corporate/2005/02/pr0802.html	Feb. 8, 2005
<i>Toshiba and SanDisk Develop 8-Gigabit NAND Flash Memory Chip (“EETimes”)</i>	EETime, https://www.eetimes.com/toshiba-and-sandisk-develop-8-gigabit-nand-flash-memory-chip/	Mar. 1, 2005
<i>SanDisk, Toshiba to Ship High-Performance NAND Flash Chips (“Channel Insider”)</i>	Channel Insider, https://www.channelinsider.com/news-and-trends/sandisk-toshiba-to-ship-high-performance-nand-flash-chips/	Jan. 23, 2007

c) Prior Art Systems

The following systems are prior art under at least 35 U.S.C. §§ 102(a):

1. Products, components, systems, and methods invented, designed, developed, reduced to practice, and/or in public use or on sale related to Toshiba and SanDisk’s 70nm 8Gb MLC NAND Flash (“**Toshiba/SanDisk’s NAND**”), as exemplified in the claim chart in Exhibit C9. As part of these Invalidity Contentions, Defendants have produced documents relating to Toshiba/SanDisk’s NAND. Based on information available to Defendants, Defendants believes that Toshiba/SanDisk’s NAND was conceived and/or reduced to practice by engineers at Toshiba Corporation and SanDisk® Corporation, including those identified in the claim chart and its cited publications, at least before May 2006, without being abandoned, suppressed, or concealed, and it was in public use or on sale by the dates identified in the claim chart, which are no later than May 2006.

Defendants’ investigation into publicly-available prior art systems that teach and/or render obvious each element of any asserted claims is ongoing. Fact discovery is at an early stage, and Defendants may require discovery from third parties regarding publicly-available prior art systems. Defendants reserve the right to amend its identification of prior art systems as Defendants become aware of the existence, functionality, and/or characteristics of prior art

systems as a result of their investigation and forthcoming discovery.

2. Primary References

Defendants contend that the primary prior art references identified below and described in the charts attached as Exhibits C1 to C9 by themselves, anticipate the asserted claims of the '314 Patent. To the extent that a primary reference is deemed not to anticipate a claim for failing to teach one or more limitations of that claim, Defendants contend that the claim would nonetheless have been obvious to a person of ordinary skill in the art at the time of the invention in view of the prior art reference itself and the knowledge of a person of ordinary skill in the art, as described in the attached charts. Defendants' prior art charts (attached as Exhibits C1 to C9) set forth the particular claims that are anticipated under 35 U.S.C. § 102 and/or rendered obvious under 35 U.S.C. § 103 by each item of prior art and identify where specifically in each item of prior art each element of each asserted claim is found.

Exhibit	Primary References
C1	U.S. Patent App. Pub. No. 2014/0159132 ("Daycock")
C2	U.S. Patent App. Pub. No. 2007/0096202 ("Kang '202")
C3	U.S. Patent No. 7,598,564 ("Kang '564")
C4	U.S. Patent App. Pub. No. 2013/0193504 ("Kinoshita")
C5	U.S. Patent No. 7,759,722 ("Murata")
C6	U.S. Patent App. Pub. No. 2011/0309425 ("Purayath")
C7	U.S. Patent No. 7,705,392 ("Yonemochi")
C8	U.S. Patent App. Pub. No. 2006/0205148 ("Deppe")
C9	Toshiba and SanDisk's 70nm 8Gb MLC NAND Flash ("Toshiba/SanDisk's NAND")

3. Obvious Combinations

To the extent that a primary reference is deemed, by itself, not to anticipate or render obvious a claim for failing to teach one or more limitations, the claim would nonetheless have been obvious to a person of ordinary skill in the art at the time of the invention by the combination of the primary reference with one or more other primary references and/or the knowledge of someone skilled in the art. For example, a person of ordinary skill in the art would have been motivated to combine any reference in Exhibits C1 to C9 with any other reference(s) in Exhibits C1 to C9. Such combinations would be achieved, for example, by merely combining the disclosures described in the respective claim charts for each reference.

The obviousness combinations are provided in the alternative to Defendants' anticipation contentions and are not to be construed to suggest that any reference included in the combinations is not itself anticipatory.

a) Exemplary Combinations

Below are examples of prior art references that would have been combined by one of ordinary skill in the art at the time of the alleged invention. These combinations are merely examples. The asserted claims of the '314 Patent are rendered obvious by:

- Daycock alone or in combination with one or more of Kang '202, Kang '564, Kinoshita, Murata, Purayath, Yonemochi, Deppe, and Toshiba/SanDisk's NAND.

For example:

- Independent claims 1 and 13 are obvious over Daycock; Daycock in view of Kang '564; Daycock in view of Yonemochi; Daycock in view of Murata; Daycock in view of Purayath; Daycock in view of Kang '202; Daycock in view of Kinoshita; Daycock in view of Toshiba/SanDisk's NAND.

- Dependent claims 3 and 17 are obvious over any of the obviousness grounds listed for independent claims 1 and 13 alone and/or further in view of Murata, Kang '564, Kinoshita, Yonemochi, Deppe, and/or Toshiba/SanDisk's NAND.
- Dependent claims 5 and 18 are obvious over any of the obviousness grounds listed for independent claims 1 and 13 alone and/or further in view of Purayath, Kang '202, and/or Deppe.
- Dependent claim 6 is obvious over any of the obviousness grounds listed for independent claims 1 and 13 alone and/or further in view of Yonemochi, Purayath, Kinoshita, Kang '564, Kang '202, and/or Toshiba/SanDisk's NAND.
- Kang '202 alone or in combination with one or more of Kang '564, Daycock, Kinoshita, Murata, Purayath, Yonemochi, Deppe, and Toshiba/SanDisk's NAND.

For example:

- Independent claims 1 and 13 are obvious over Kang '202; Kang '202 in view of Kang '564; Kang in view of Daycock; Kang '202 in view of Yonemochi; Kang '202 in view of Murata; Kang '202 in view of Purayath; Kang '202 in view of Kinoshita; Kang '202 in view of Toshiba/SanDisk's NAND.
- Dependent claims 3 and 17 are obvious over any of the obviousness grounds listed for independent claims 1 and 13 alone and/or further in view of Murata, Kang '564, Kinoshita, Yonemochi, Deppe, and/or Toshiba/SanDisk's NAND.

- Dependent claims 5 and 18 are obvious over any of the obviousness grounds listed for independent claims 1 and 13 alone and/or further in view of Purayath, Daycock, and/or Deppe.
- Dependent claim 6 is obvious over any of the obviousness grounds listed for independent claims 1 and 13 alone and/or further in view of Yonemochi, Purayath, Kinoshita, Kang '564, Daycock, and/or Toshiba/SanDisk's NAND.
- Kang '564 alone or in combination with one or more of Kang '202, Daycock, Kinoshita, Murata, Purayath, Yonemochi, Deppe, and Toshiba/SanDisk's NAND.

For example:

- Independent claims 1 and 13 are obvious over Kang '564; Kang '564 in view of Daycock; Kang '564 in view of Yonemochi; Kang '564 in view of Murata; Kang '564 in view of Purayath; Kang '564 in view of Kang '202; Kang '564 in view of Kinoshita; Kang '564 in view of Toshiba/SanDisk's NAND.
- Dependent claims 3 and 17 are obvious over any of the obviousness grounds listed for independent claims 1 and 13 alone and/or further in view of Murata, Kinoshita, Yonemochi, Deppe, and/or Toshiba/SanDisk's NAND.
- Dependent claims 5 and 18 are obvious over any of the obviousness grounds listed for independent claims 1 and 13 alone and/or further in view of Purayath, Daycock, Kang '202, and/or Deppe.

- Dependent claim 6 is obvious over any of the obviousness grounds listed for independent claims 1 and 13 alone and/or further in view of Yonemochi, Purayath, Kinoshita, Daycock, Kang '202, and/or Toshiba/SanDisk's NAND.
- Kinoshita alone or in combination with one or more of Kang '202, Kang '564, Daycock, Murata, Purayath, Yonemochi, Deppe, and Toshiba/SanDisk's NAND.

For example:

- Independent claims 1 and 13 are obvious over Kinoshita; Kinoshita in view of Kang '564; Kinoshita in view of Yonemochi; Kinoshita in view of Murata; Kinoshita in view of Purayath; Kinoshita in view of Kang '202; Kinoshita in view of Daycock; Kinoshita in view of Toshiba/SanDisk's NAND.
- Dependent claims 3 and 17 are obvious over any of the obviousness grounds listed for independent claims 1 and 13 alone and/or further in view of Murata, Kang '564, Yonemochi, Deppe, and/or Toshiba/SanDisk's NAND.
- Dependent claims 5 and 18 are obvious over any of the obviousness grounds listed for independent claims 1 and 13 alone and/or further in view of Purayath, Daycock, Kang '202, and/or Deppe.
- Dependent claim 6 is obvious over any of the obviousness grounds listed for independent claims 1 and 13 alone and/or further in view of Yonemochi, Purayath, Kang '564, Daycock, Kang '202, and/or Toshiba/SanDisk's NAND.

- Murata alone or in combination with one or more of Kang '202, Kang '564, Kinoshita, Daycock, Purayath, Yonemochi, Deppe, and Toshiba/SanDisk's NAND. For example:

- Independent claims 1 and 13 are obvious over Murata; Murata in view of Kang '564; Murata in view of Yonemochi; Murata in view of Daycock; Murata in view of Purayath; Murata in view of Kang '202; Murata in view of Kinoshita; Murata in view of Toshiba/SanDisk's NAND.
- Dependent claims 3 and 17 are obvious over any of the obviousness grounds listed for independent claims 1 and 13 alone and/or further in view of Kinoshita, Kang '564, Yonemochi, Deppe, and/or Toshiba/SanDisk's NAND.
- Dependent claims 5 and 18 are obvious over any of the obviousness grounds listed for independent claims 1 and 13 alone and/or further in view of Purayath, Daycock, Kang '202, and/or Deppe.
- Dependent claim 6 is obvious over any of the obviousness grounds listed for independent claims 1 and 13 alone and/or further in view of Yonemochi, Purayath, Kinoshita, Kang '564, Daycock, Kang '202, and/or Toshiba/SanDisk's NAND.

- Purayath alone or in combination with one or more of Kang '202, Kang '564, Kinoshita, Murata, Daycock, Yonemochi, Deppe, and Toshiba/SanDisk's NAND.

For example:

- Independent claims 1 and 13 are obvious over Purayath; Purayath in view of Kang '564; Purayath in view of Yonemochi; Purayath in view of

Murata; Purayath in view of Daycock; Purayath in view of Kang '202; Purayath in view of Kinoshita; Purayath in view of Toshiba/SanDisk's NAND.

- Dependent claims 3 and 17 are obvious over any of the obviousness grounds listed for independent claims 1 and 13 alone and/or further in view of Murata, Kinoshita, Kang '564, Yonemochi, Deppe, and/or Toshiba/SanDisk's NAND.
- Dependent claims 5 and 18 are obvious over any of the obviousness grounds listed for independent claims 1 and 13 alone and/or further in view of Daycock, Kang '202, and/or Deppe.
- Dependent claim 6 is obvious over any of the obviousness grounds listed for independent claims 1 and 13 alone and/or further in view of Yonemochi, Kinoshita, Kang '564, Daycock, Kang '202, and/or Toshiba/SanDisk's NAND.
- Yonemochi alone or in combination with one or more of Kang '202, Kang '564, Kinoshita, Murata, Purayath, Daycock, Deppe, and Toshiba/SanDisk's NAND.

For example:

- Independent claims 1 and 13 are obvious over Yonemochi; Yonemochi in view of Kang '564; Yonemochi in view of Daycock; Yonemochi in view of Murata; Yonemochi in view of Purayath; Yonemochi in view of Kang '202; Yonemochi in view of Kinoshita; Yonemochi in view of Toshiba/SanDisk's NAND.

- Dependent claims 3 and 17 are obvious over any of the obviousness grounds listed for independent claims 1 and 13 alone and/or further in view of Murata, Kinoshita, Kang '564, Deppe, and/or Toshiba/SanDisk's NAND.
- Dependent claims 5 and 18 are obvious over any of the obviousness grounds listed for independent claims 1 and 13 alone and/or further in view of Purayath, Daycock, Kang '202, and/or Deppe.
- Dependent claim 6 is obvious over any of the obviousness grounds listed for independent claims 1 and 13 alone and/or further in view of Purayath, Kinoshita, Kang '564, Daycock, Kang '202, and/or Toshiba/SanDisk's NAND.
- Deppe alone or in combination with one or more of Kang '202, Kang '564, Kinoshita, Murata, Purayath, Yonemochi, Deppe, and Toshiba/SanDisk's NAND.

For example:

- Independent claims 1 and 13 are obvious over Deppe; Deppe in view of Kang '564; Deppe in view of Yonemochi; Deppe in view of Murata; Deppe in view of Purayath; Deppe in view of Daycock; Deppe in view of Kang '202; Deppe in view of Kinoshita; Deppe in view of Toshiba/SanDisk's NAND.
- Dependent claims 3 and 17 are obvious over any of the obviousness grounds listed for independent claims 1 and 13 alone and/or further in view of Murata, Kinoshita, Kang '564, Yonemochi, and/or Toshiba/SanDisk's NAND.

- Dependent claims 5 and 18 are obvious over any of the obviousness grounds listed for independent claims 1 and 13 alone and/or further in view of Purayath, Daycock, and/or Kang '202.
- Dependent claim 6 is obvious over any of the obviousness grounds listed for independent claims 1 and 13 alone and/or further in view of Yonemochi, Purayath, Kinoshita, Kang '564, Daycock, Kang '202, and/or Toshiba/SanDisk's NAND.
- Toshiba/SanDisk's NAND alone or in combination with one or more of Kang '202, Kang '564, Kinoshita, Murata, Purayath, Yonemochi, Deppe, and Daycock.

For example:

- Independent claims 1 and 13 are obvious over Toshiba/SanDisk's NAND; Toshiba/SanDisk's NAND in view of Kang '564; Toshiba/SanDisk's NAND in view of Yonemochi; Toshiba/SanDisk's NAND in view of Murata; Toshiba/SanDisk's NAND in view of Purayath; Toshiba/SanDisk's NAND in view of Kang '202; Toshiba/SanDisk's NAND in view of Kinoshita; Toshiba/SanDisk's NAND in view of Daycock.
- Dependent claims 3 and 17 are obvious over any of the obviousness grounds listed for independent claims 1 and 13 alone and/or further in view of Murata, Kinoshita, Kang '564, Yonemochi, and/or Deppe.
- Dependent claims 5 and 18 are obvious over any of the obviousness grounds listed for independent claims 1 and 13 alone and/or further in view of Purayath, Daycock, Kang '202, and/or Deppe.

- Dependent claim 6 is obvious over any of the obviousness grounds listed for independent claims 1 and 13 alone and/or further in view of Yonemochi, Purayath, Kinoshita, Kang '564, Daycock, and/or Kang '202.

b) Motivations to Combine and Expectation of Success

To the extent a finder of fact finds that a primary prior art reference does not disclose one or more limitations of an asserted claim, the asserted claim is nevertheless obvious because the alleged missing limitations contain nothing beyond ordinary improvements. In other words, the asserted claim combines known elements to achieve predictable results or chooses between clear alternatives known to those of skill in the art, particularly in view of the state of the art as reflected in the relevant prior art.

Moreover, as explained above, it would have been obvious to a person of skill in the art at the time of the alleged invention of the asserted claims to combine any primary reference with any combination of other primary references so as to practice the asserted claims. To the extent that Plaintiff argues that any concept claimed in the asserted claims is not disclosed in a primary reference, it would, at a minimum, have been obvious to adapt the primary reference to include the concept or combine it with other primary references that disclose the concept. Each concept described and claimed in the Asserted Patents was known to those of skill in the art as available design choices for semiconductor memory design and fabrication.

The Supreme Court has held that “[t]he combination of familiar elements according to known methods is likely to be obvious when it does no more than yield predictable results.” *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 416 (2007). “When a work is available in one field of endeavor, design incentives and other market forces can prompt variations of it, either in the same field or a different one.” *Id.* at 417. As the Supreme Court made clear, “[f]or the same reason, if a technique has been used to improve one device, and a person of ordinary skill in the

art would recognize that it would improve similar devices in the same way, using the technique is obvious unless its actual application is beyond his or her skill.” *Id.*

To determine whether there is an apparent reason to combine the known elements in the fashion claimed by the patent at issue, a court can “look to interrelated teachings of multiple patents; the effects of demands known to the design community or present in the marketplace; and the background knowledge possessed by a person having ordinary skill in the art.” *Id.* at 418. For example, obviousness can be demonstrated by showing “there existed at the time of invention a known problem for which there was an obvious solution encompassed by the patent’s claims.” *Id.* at 420. “[A]ny need or problem known in the field of endeavor at the time of invention and addressed by the patent can provide a reason for combining the elements in the manner claimed.” *Id.* Common sense also teaches that “familiar items may have obvious uses beyond their primary purposes, and in many cases a person of ordinary skill will be able to fit the teachings of multiple patents together like pieces of a puzzle.” *Id.*

However, the Supreme Court in *KSR* held that a claimed invention can be obvious even if there is no explicit teaching, suggestion, or motivation for combining the prior art to produce that invention. In summary, *KSR* holds that patents that are based on new combinations of elements or components already known in a technical field may be found to be obvious. *See, generally, KSR*, 550 U.S. 398. Specifically, the Court in *KSR* rejected a rigid application of the “teaching, suggestion, or motivation [to combine]” test. *Id.* at 418. “In determining whether the subject matter of a patent claim is obvious, neither the particular motivation nor the avowed purpose of the patentee controls. What matters is the objective reach of the claim.” *Id.* at 419. “Under the correct analysis, any need or problem known in the field of endeavor at the time of invention and addressed by the patent can provide a reason for combining the elements in the

manner claimed.” *Id.* at 420. A key inquiry is whether the “improvement is more than the predictable use of prior art elements according to their established functions.” *Id.* at 417.

The rationale to combine or modify prior art references is significantly stronger when, as here, the references seek to solve the same problem, come from the same field, and correspond well to each other. *In re Inland Steel Co.*, 265 F.3d 1354, 1362 (Fed. Cir. 2001). The Federal Circuit has held that two references may be combined as invalidating art under similar circumstances, namely “[the prior art] focus[es] on the same problem that the . . . patent addresses: enhancing the magnetic properties of . . . steel. Moreover, both [prior art references] come from the same field Finally, the solutions to the identified problems found in the two references correspond well.” *Id.* at 1364 (concerning patents and prior art relating to improving the magnetic and electrical properties of steel).

In view of the Supreme Court’s *KSR* decision, the PTO issued a set of Examination Guidelines. Examination Guidelines for Determining Obviousness Under 35 U.S.C. § 103 in view of the Supreme Court Decision in *KSR International Co. v. Teleflex, Inc.*, 72 Fed. Reg. 57526 (October 10, 2007). Those Guidelines summarized the *KSR* decision and identified various rationales for finding a claim obvious, including those based on other precedents. Those rationales include:

- (A) Combining prior art elements according to known methods to yield predictable results;
- (B) Simple substitution of one known element for another to obtain predictable results;
- (C) Use of known technique to improve similar devices (methods, or products) in the same way;
- (D) Applying a known technique to a known device (method, or product) ready for improvement to yield predictable results;
- (E) “Obvious to try” – choosing from a finite number of identified, predictable solutions, with a reasonable expectation of success;

(F) Known work in one field of endeavor may prompt variations of it for use in either the same field or a different one based on design incentives or other market forces if the variations would have been predictable to one of ordinary skill in the art;

(G) Some teaching, suggestion, or motivation in the prior art that would have led one of ordinary skill to modify the prior art reference or to combine prior art reference teachings to arrive at the claimed invention.

Id. at 57529. The above rationales likewise apply in rendering obvious the asserted claims of the Asserted Patents.

The references disclosed herein, alone or in combination, contain an explicit and/or implicit teaching or motivation to combine them due to the following: (1) the knowledge generally available to a person of ordinary skill in the art; (2) the prior art references as understood by a person of ordinary skill in the art; (3) the nature of the problem to be solved; (4) the fact that each prior art reference addresses similar problems; and (5) the knowledge of those skilled in the art that the disclosed elements had been or could be used together.

As an example of those reasons and motivations to combine the references Kang '202, Kang '564, Daycock, Kinoshita, Murata, Daycock, Yonemochi, Deppe, and Toshiba/SanDisk's NAND all generally relate to semiconductor memory design and, in particular, structures and manufacturing methods for enhancing the speed and reliability and decreasing the parasitic capacitance of semiconductor memory devices including flash/non-volatile memory with minimal space between adjacent gate structures. *See, e.g.*, Daycock ¶ 6; Kang '564 at Abstract, ¶ 6; Kang '202 at Abstract, ¶¶ 5-6; Purayath ¶¶ 7, 12. The references disclose using similar components and techniques, such as using air gaps or other electrical isolation regions between adjacent structures. *See, e.g.*, Daycock at Abstract, ¶¶ 1, 15-17; Kang '202 at Abstract, ¶¶ 3, 14; Purayath at Abstract, ¶¶ 31-33. Thus, combining one or more such references merely involves combining prior art elements according to known methods to yield predictable results, the

substitution of one known element for another to obtain predictable results, the use of a known technique to improve similar devices in the same way, or applying a known technique to a known device ready for improvement to yield predictable results.

In addition, below are additional motivations to combine prior art for particular claim limitations. The following discussion of specific claim limitations merely provides examples, which are not limiting.

For example, to the extent that any primary reference is deemed not to anticipate a claim for failing to teach limitations 1[e] and 13[e] (“[forming] nitride regions that cover the second oxide regions”), it would have been obvious to a person of ordinary skill in the art at the time of the invention to combine the primary reference with any of the prior art that discloses limitation 1[e] and 13[e] in Exhibits C1 to C9. For example, the charted prior art references explicitly describe or implicitly suggest using barrier spacers, such as nitride, to protect a control gate—including a wordline—during cell formation. *See, e.g.,* Kang ’564 at Abstract, 1:65-2:65. It would have been obvious to combine any primary reference with any of Kang ’202, Kang ’564, Daycock, Kinoshita, Murata, Daycock, Yonemochi, Deppe, and Toshiba/SanDisk’s NAND to satisfy limitations 1[e] and 13[e]. A person skilled in the art would have recognized that having a nitride region covering a control gate and wordline was an effective technique to protect a control gate and wordline during formation of a memory cell. Indeed, using a dielectric layer such as nitride to insulate control gates and wordlines in a semiconductor was a common practice. Further, a person of ordinary skill in the art would have recognized that using a dielectric such as nitride has several benefits. For example, nitride, especially silicon nitride (SiN), has a moderate dielectric constant, which helps in minimizing capacitive coupling between adjacent wordlines. This reduction in capacitive coupling is crucial for preventing interference between

neighboring cells, leading to better data integrity and preventing disturb effects (e.g., unintentional programming or erasing of nearby cells). In addition, using nitride as part of the insulating layers in memory devices can enhance reliability by improving etch resistance and serving as a barrier layer. Further, nitride can facilitate advanced patterning schemes in three-dimensional memory architectures, improving device density and performance. Thus, a person of ordinary skill in the art would have been motivated to modify any of the primary references to include the claimed features, to the extent it is not disclosed. A person of ordinary skill in the art would also have had a reasonable expectation of success given that, by the alleged priority date of the '314 Patent, millions of semiconductor devices were manufactured each year using dielectric layers for insulation and protection of control gates and wordlines. A person of ordinary skill in the art would have understood that these references disclose interrelated teachings based on routine technologies and would have been amenable to various well-understood and predictable combinations.

In addition, to the extent that any primary reference is deemed not to anticipate a claim for failing to teach limitations 1[f] and 13[f] (“[forming] electrical isolation regions other than silicon nitride adjacent to the first oxide regions that cover the sidewalls of the charge storage regions”), it would have been obvious to a person of ordinary skill in the art at the time of the invention to combine the primary reference with any of the prior art that discloses limitation 1[f] and 13[f] in Exhibits C1 to C9. For example, the charted prior art references explicitly describe or implicitly suggest a semiconductor device including electrical isolation regions—other than silicon nitride—that are adjacent to the first oxide regions that cover the sidewalls of the charge storage regions. *See, e.g.*, Daycock at Abstract, ¶¶ 1, 15-17; Kang '202 at Abstract, ¶¶ 3, 14; Purayath at Abstract, ¶¶ 31-33. A person skilled in the art would have recognized that the

dielectric constant of an insulating material is a primary factor in determining the capacitance between adjacent floating gates. Kang '202 ¶ 10. For example, “[a]n insulating layer formed from a material having a higher dielectric constant will cause increased parasitic capacitance between adjacent gate structures.” *Id.* And increases in parasitic capacitance reduce the speed of the memory devices while variations in parasitic capacitance between gate structures may cause a variation in the threshold voltage for each gate structure, thereby degrading the reliability of memory devices. *Id.* ¶ 6. A person skilled in the art would, therefore, have recognized that it is desirable to use a dielectric layer from the lowest dielectric constant material possible and that, for example, silicon nitride had a much higher dielectric constant than silicon oxide or air. *See id.* ¶¶ 10, 11. Thus, a person of ordinary skill in the art would have been motivated to modify any of the primary references to include this feature. A person of ordinary skill in the art would also have had a reasonable expectation of success given the well-known uses of electrical isolation regions in semiconductor processing. A person of ordinary skill in the art would have understood that these references disclose interrelated teachings based on routine technologies and would have been amendable to various well-understood and predictable combinations. It would, therefore, have been obvious to combine any primary reference with any of Kang '202, Kang '564, Daycock, Kinoshita, Murata, Daycock, Yonemochi, Deppe, and Toshiba/SanDisk's NAND to satisfy limitations 1[f] and 13[f].

In addition, to the extent that any primary reference is deemed not to anticipate a claim for failing to teach claims 3 (“wherein the word lines comprise tungsten”) and 17 (“forming the plurality of word lines from tungsten”) it would have been obvious to a person of ordinary skill in the art at the time of the invention to combine the primary reference with any of the prior art that discloses this limitation in Exhibits C1 to C9. For example, the charted prior art references

explicitly describe or implicitly suggest a semiconductor device including having a tungsten word line. *See, e.g.*, Kang '564 at 1:12-57, 6:11-22; Kinoshita ¶¶ 23, 119; Yonemochi at 3:52-64; Deppe ¶ 87. A person skilled in the art would have recognized that tungsten has a low electrical resistance, so forming a word line from tungsten may enhance the speed of a memory device. *See* Kang '564 at 6:10-13, 1:12-30, 6:11-22. Thus, a person of ordinary skill in the art would have been motivated to modify any of the primary references to include this feature. A person of ordinary skill in the art would also have had a reasonable expectation of success given the well-known uses of tungsten word lines in memory devices. A person of ordinary skill in the art would have understood that these references disclose interrelated teachings based on routine technologies and would have been amendable to various well-understood and predictable combinations. It would, therefore, have been obvious to combine any primary reference with any of Kang '202, Kang '564, Daycock, Kinoshita, Murata, Daycock, Yonemochi, Deppe, and Toshiba/SanDisk's NAND to satisfy claims 3 and 17.

In addition, to the extent that any primary reference is deemed not to anticipate a claim for failing to teach claims 5 ("wherein the charge storage region is a dielectric charge trapping region") and 18 ("wherein forming the charge storage regions comprising a dielectric charge trapping region") it would have been obvious to a person of ordinary skill in the art at the time of the invention to combine the primary reference with any of the prior art that discloses this limitation in Exhibits C1 to C9. For example, the charted prior art references explicitly describe or implicitly suggest a semiconductor device wherein the charge storage region is a dielectric charge trapping region. *See, e.g.*, Daycock ¶¶ 3, 29, 34; Kang '202 ¶ 32; Purayath ¶¶ 10, 47; Deppe at Abstract, ¶¶ 2, 9. A person skilled in the art would have known that charge-trapping layers store electrons as data state of the memory cell. A person of skill in the art would also

have known that there were advantages to using charge trapping as opposed to other, largely interchangeable methods of storing electrons as a data state of the memory cell (i.e., floating gates), including greater data retention, better scalability to smaller process nodes, and ease of manufacturing. Thus, a person of ordinary skill in the art would have been motivated to modify any of the primary references to include this feature. A person of ordinary skill in the art would also have had a reasonable expectation of success given the well-known uses of charge trapping regions in non-volatile memory. A person of ordinary skill in the art would have understood that these references disclose interrelated teachings based on routine technologies and would have been amendable to various well-understood and predictable combinations. It would, therefore, have been obvious to combine any primary reference with any of Kang '202, Kang '564, Daycock, Kinoshita, Murata, Daycock, Yonemochi, Deppe, and Toshiba/SanDisk's NAND to satisfy claims 5 and 18.

In addition, to the extent that any primary reference is deemed not to anticipate a claim for failing to teach claim 6 ("wherein the word lines are electrically coupled to the peripheral circuitry") it would have been obvious to a person of ordinary skill in the art at the time of the invention to combine the primary reference with any of the prior art that discloses this limitation in Exhibits C1 to C9. For example, the charted prior art references explicitly describe or implicitly suggest a semiconductor device wherein the word lines are electrically coupled to the peripheral circuitry. *See, e.g.*, Kang '202 ¶¶ 32, 56, 64; Kang '564 at 1:12-30; Kinoshita ¶¶ 14, 99; Purayath ¶¶ 85, 151, 45, 49, Fig. 17; Toshiba/SanDisk's NAND at 53-56, 63-64, 66-68. A person skilled in the art would have known that connecting peripheral circuitry to wordlines plays a crucial role in enabling various functionalities and optimizing performance of memory devices. For example, peripheral circuitry manages data access and handles various operations like

reading, writing, and erasing the memory cells. A person of skill in the art would also have understood that a peripheral circuit would include row control circuitry, such as row decoders and word line drivers, connected to the word lines to select one of the word lines, to apply read voltages, to apply program voltages combined with the bit line potential levels controlled by column control circuit, and to apply an erase voltage, enabling memory access. Accordingly, peripheral circuitry allows for the controlled application of various voltages to wordlines during read, program, and erase operations, which is essential for reducing power consumption through low-power operations, reducing read select delays, reducing wordline-to-wordline interference, and improving data reliability. Thus, a person of ordinary skill in the art would have been motivated to modify any of the primary references to include the claimed features, to the extent it is not disclosed. A person of ordinary skill in the art would also have had a reasonable expectation of success given that, by the alleged priority date of the '314 Patent, millions of semiconductor devices were manufactured each year using word lines electrically coupled to peripheral circuitry. A person of ordinary skill in the art would have understood that these references disclose interrelated teachings based on routine technologies and would have been amendable to various well-understood and predictable combinations. It would, therefore, have been obvious to combine any primary reference with any of Kang '202, Kang '564, Daycock, Kinoshita, Murata, Daycock, Yonemochi, Deppe, and Toshiba/SanDisk's NAND to satisfy claim 6.

B. Invalidity Contentions Under 35 U.S.C. § 112

Defendants include below the grounds on which Defendants contend the asserted claims are invalid for failure to meet the requirements of the first two paragraphs of 35 U.S.C. § 112.

Plaintiff has not yet provided a claim construction for many of the terms and phrases that Defendants anticipate will be in dispute. Defendants, therefore, cannot provide a complete list

of its § 112 defenses because Defendants do not know whether Plaintiff will proffer a construction for certain terms and phrases that is broader than, or inconsistent with, the construction that would be supportable by the disclosure set forth in the specification.

To the extent the following contentions reflect constructions of claim limitations consistent with or implicit in Plaintiff's Infringement Contentions, no inference is intended nor should any be drawn that Defendants agree with Plaintiff's claim constructions, and Defendants expressly reserve the right to contest such claim constructions. Defendants offer these contentions in response to Plaintiff's Infringement Contentions and without prejudice to any position it may ultimately take as to any claim construction issues.

Accordingly, Defendants reserve the right to amend or supplement these § 112 Invalidity Contentions as discovery progresses.

1. Indefiniteness Under 35 U.S.C. § 112(b)

35 U.S.C. § 112(b) requires that a patent claim "particularly point[] out and distinctly claim[] the subject matter which the inventor or a joint inventor regards as the invention." 35 U.S.C. § 112(b). Claim terms that fail to inform those skilled in the art "with reasonable certainty . . . about the scope of the invention" fail the definiteness requirement of 35 U.S.C. § 112(b). *Nautilus, Inc. v. Biosig Instruments, Inc.*, 572 U.S. 898, 901 (2014).

Each of the asserted claims are invalid as indefinite under 35 U.S.C. § 112 because they fail to particularly point out and distinctly claim the subject matter which the applicant regards as his invention. In particular, the following limitations, read in light of the intrinsic evidence, fail to inform those skilled in the art with reasonable certainty about the scope of the claimed inventions:

- Claim 1: “each of the word lines being associated with a line of the memory cells, each of the word lines being coupled to the control gates of the memory cells with which it is associated;”
- Claim 1: “first oxide regions that cover the sidewalls of the charge storage regions;”
- Claim 1: “second oxide regions that cover the sidewalls of the word lines;”
- Claim 1: “nitride regions that cover the second oxide regions;”
- Claim 1: “and electrical isolation regions other than silicon nitride adjacent to the first oxide regions that cover the sidewalls of the charge storage regions.”
- Claim 3: “wherein the word lines comprise tungsten.”
- Claim 13: “each of the word lines being associated with a line of the memory cells, each of the word lines being coupled to the control gates of the memory cells with which it is associated;”
- Claim 13: “forming first oxide regions that cover the sidewalls of the charge storage regions;”
- Claim 13: “forming second oxide regions that cover the sidewalls of the word lines;”
- Claim 13: “forming nitride regions that cover the second oxide regions;”
- Claim 13: “forming electrical isolation regions other than silicon nitride adjacent to the first oxide regions that cover the sidewalls of the charge storage regions.”
- Claim 17: “wherein the plurality of word lines comprises forming the plurality of word lines from tungsten.”
- Claim 18: “wherein forming the plurality of lines of memory cells comprises forming the charge storage regions comprising a dielectric charge trapping region.”

2. Lack of Enablement/Lack of Written Description Under 35 U.S.C. § 112(a)

The asserted claims of the '314 Patent are further invalid under 35 U.S.C. § 112(a) because the specifications do not contain an adequate written description of the subject matter of these claims and would not enable one of skill in the relevant art to make and use the alleged invention.

For a claim to be valid, the specification must contain a written description of the invention. 35 U.S.C. § 112(a). To fulfill the written description requirement, it “must clearly allow persons of ordinary skill in the art to recognize that the inventor invented what is claimed.” *Ariad Pharm., Inc. v. Eli Lilly & Co.*, 598 F.3d 1336, 1351 (Fed. Cir. 2010) (citation and internal quotation marks omitted). “[T]he applicant must ‘convey with reasonable clarity to those skilled in the art that, as of the filing date sought, he or she was in possession of the invention,’ and demonstrate that by disclosure in the specification of the patent.” *Carnegie Mellon Univ. v. Hoffmann-La Roche Inc.*, 541 F.3d 1115, 1122 (Fed. Cir. 2008) (quoting *Vas-Cath Inc. v. Mahurkar*, 935 F.2d 1555, 1563–64 (Fed. Cir. 1991)).

The specification must also describe “the manner and process of making and using [the invention], in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains . . . to make and use the” invention. *Ariad*, 598 F.3d at 1343; *see also* 35 U.S.C. § 112(a). “The enablement requirement is satisfied when one skilled in the art, after reading the specification, could practice the claimed invention without undue experimentation.” *AK Steel Corp. v. Sollac & Ugine*, 344 F.3d 1234, 1244 (Fed. Cir. 2003) (citation omitted). “[T]he scope of the claims must be less than or equal to the scope of the enablement.” *Nat’l Recovery Tech., Inc. v. Magnetic Separation Sys., Inc.*, 166 F.3d 1190, 1196 (Fed. Cir. 1999).

Each of the asserted claims below are invalid because the specifications fail to provide written description and/or an enabling disclosure of at least the following limitations:

- Claim 1: “each of the word lines being associated with a line of the memory cells, each of the word lines being coupled to the control gates of the memory cells with which it is associated;”
- Claim 1: “first oxide regions that cover the sidewalls of the charge storage regions;”
- Claim 1: “second oxide regions that cover the sidewalls of the word lines;”
- Claim 1: “nitride regions that cover the second oxide regions;”
- Claim 1: “and electrical isolation regions other than silicon nitride adjacent to the first oxide regions that cover the sidewalls of the charge storage regions.”
- Claim 3: “wherein the word lines comprise tungsten.”
- Claim 5: “wherein the charge storage region is a dielectric charge trapping region.”
- Claim 6: “further comprising peripheral circuitry, wherein the word lines are electrically coupled to the peripheral circuitry.”
- Claim 13: “each of the word lines being associated with a line of the memory cells, each of the word lines being coupled to the control gates of the memory cells with which it is associated;”
- Claim 13: “forming first oxide regions that cover the sidewalls of the charge storage regions;”
- Claim 13: “forming second oxide regions that cover the sidewalls of the word lines;”
- Claim 13: “forming nitride regions that cover the second oxide regions;”
- Claim 13: “forming electrical isolation regions other than silicon nitride adjacent to the first oxide regions that cover the sidewalls of the charge storage regions.”

- Claim 17: “wherein the plurality of word lines comprises forming the plurality of word lines from tungsten.”
- Claim 18: “wherein forming the plurality of lines of memory cells comprises forming the charge storage regions comprising a dielectric charge trapping region.”

VI. Document Production

Pursuant to the Court’s Standing Order Governing Patent and Scheduling Order (Dkt. No. 38), Defendants are concurrently producing the prior art identified in these Invalidity Contentions.

In addition, based on its investigations to date, Defendants are concurrently producing technical documents, sufficient to show the operation of the Accused Instrumentalities identified by Plaintiff in its Infringement Contentions. Defendants further make available source code for inspection at Micron’s facilities in Boise, Idaho, as soon as a protective Order is entered.

Defendants reserve the right to supplement these productions with additional documentation, in accordance with the Federal Rules of Civil Procedure, the Local Rules, the Court’s Orders and other applicable rules and statutes.

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Respectfully submitted,

/s/ John Kappos

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CERTIFICATE OF SERVICE

Pursuant to the Federal Rules of Civil Procedure, I hereby certify that, on June 11, 2025, all counsel of record who have appeared in this case are being served with a copy of the foregoing via the electronic mail.

/s/ John Kappos

John Kappos

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