

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

ADVANCED MICRO DEVICES, INC.

Petitioner

v.

COLLABO INNOVATIONS, INC.

Patent Owner

Case IPR2019-01523
Patent 7,930,575 B2

PATENT OWNER'S PRELIMINARY RESPONSE

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PATENT OWNER'S EXHIBIT LIST

Exhibit No.	Description
2001	Excerpts from The Authoritative Dictionary of IEEE Standard Terms, 7th Ed. © 2000
2002	Excerpts from Modern Dictionary of Electronics, 7th Ed. © 1999
2003	Excerpts from Microsoft Computer Dictionary, 4th Ed. © 1999

Pursuant to 35 U.S.C. § 313, 37 C.F.R. § 42.107 and the Notice of Filing Date Accorded to Petition, Paper No. 4, Patent Owner Collabo Innovations, Inc. (“Collabo”) timely submits this preliminary response to Petitioner Advanced Micro Devices, Inc.’s (“Petitioner”) petition for *inter partes* review (the “Petition”) of U.S. Patent No. 7,930,575 (the “’575 patent”).

“In an IPR, the petitioner has the burden from the onset to show with particularity why the patent it challenges is unpatentable.” *Harmonic Inc. v. Avid Tech., Inc.*, 815 F.3d 1356, 1363 (Fed. Cir. 2016); 35 U.S.C. § 312(a)(3) (requiring IPR petitions to identify “with particularity . . . the evidence that supports the grounds for the challenge to each claim”). “[T]hat burden never shifts to the patentee.” *In re Magnum Oil Tools Int’l, Ltd.*, 829 F.3d 1364, 1375 (Fed. Cir. 2016) (citation omitted).

This is one of two petitions for *inter partes* review filed by Petitioner on the same day regarding certain claims of the ’575 patent. Petitioner has not met its burden in showing any of the challenged claims of the ’575 patent obvious in light of the alleged prior art. For the reasons stated herein, the Petition should be denied.

I. THE MICROCONTROLLER OF THE ’575 PATENT.

The ’575 patent, entitled “Microcontroller for Controlling Power Shutdown Process,” discloses various embodiments of an inventive microcontroller that is capable of preserving the state of a Central Processing Unit (“CPU”) when the

CPU goes into standby, or sleep, or another low-power state. Ex. 1001 at 2:26-31.

In contrast to the technology that existed prior to the '575 patent, the main object of the invention of the '575 patent is in providing a “microcontroller capable of easily and rapidly evacuating and restoring information necessary in proceeding with a program when realizing a standby state in which internal operation voltage is lowered, or the like.” *Id.* The '575 patent does this through the specific requirements of the microcontroller as detailed in the specification and claims.

A. The Claims Of The '575 Patent.

Independent claims 1 and 17 of the '575 patent describe the required elements of the claimed microcontroller.

Claim 1 begins by listing the physical requirements of the microcontroller.

What is claimed is

[1.Preamble] A microcontroller comprising:

[1.A] a CPU;

[1.B] a power supply unit arranged between the CPU and
a power supply device for supplying power to the
CPU;

[1.C] a power supply control unit for controlling the CPU
and the power supply unit;

[1.D] an information holding unit for holding information
evacuated from the CPU, the information being
necessary in proceeding with a program; and

[1.E] a clock generator; wherein:

Ex. 1001 at 18:45-55.

Claim 1 recites limitations directed at the process undertaken by the components of the claimed microcontroller. *See id.* at 18:56-19:24. Included within that process are seven distinct signals:

- (a) Shutdown request signal
- (b) Evacuation completed signal
- (c) Power shutdown control signal
- (d) Clock stop control signal
- (e) Power supply control signal
- (f) Restoration request signal
- (g) Clock supply control signal

See id. Claim 1 describes where each signal originates and terminates, the signal's effect, as well as the requisite sequencing of those signals for the claimed operation of the microcontroller. *See id.*

Origin	Signal	Terminus
Power Supply Control Unit	Shutdown request signal	CPU
CPU	Evacuation completed signal	Power Supply Control Unit
Power Supply Control Unit	Power shutdown control signal	Power Supply Unit
Power Supply Control Unit	Clock stop control signal	Clock Generator
Power Supply Control Unit	Power supply control signal	Power Supply Unit
Power Supply Control Unit	Restoration request signal	CPU
Power Supply Control Unit	Clock supply control signal	Clock Generator

These specific interconnections are essential and specific aspects of the claims of the '575 patent.

Claim 1 of the '575 patent puts all of these elements together to teach a microcontroller that produces a new solution to a problem that existing solutions did not provide. As an example, claim 1 requires that “the *CPU*, upon receiving the *shutdown request signal*, executes a *power shutdown microprogram*, evacuates the *information necessary in proceeding with the program* to the *information holding unit*, and outputs an *evacuation completed signal* to the *power supply control unit* after evacuation is completed[.]” *Id.* at 18:59-64 (emphasis added).

FIG. 1

The microcontroller of independent claim 17 largely mirrors that of claim 1, except it does not require a clock generator and it differs in some of the requisite sequencing of processes. *Compare id.* at 18:46-19:24 with 20:49-21:13; *see also* Ex. 1003 at Appendix A (Claim Comparison). For example, claim 17 covers a scenario when a microcontroller is preparing to shut down power to the processor, but aborts that effort just prior to removing power. *See* Ex. 1001 at 20:59-21:8. In that case, restoring the state is unnecessary because it has not yet been lost by the removal of power. *See id.* at 21:1-8. This requires that “the CPU, upon receiving the restoration request signal, executes a power supply restoration microprogram which does not restore the evacuated information, and continues program execution[.]” *Id.* at 21:5-8.

The '575 patent contains twenty-nine dependent claims—claims 2 through 16 depend from claim 1, and claims 18 through 31 depend from claim 17. Claims 18 through 31 largely mirror claims 2 through 16. *Compare id.* at 19:25-20:48 with 21:14-22:47; *see also* Ex. 1003 at Appendix A. The dependent claims cover different variations to the components and operation of the claimed microcontroller.

B. Claim Construction.

Claims in an *inter partes* review proceeding “shall be construed using the same claim construction standard that would be used to construe the claim in a

civil action under 35 U.S.C. 282(b), including construing the claim in accordance with the ordinary and customary meaning of such claim as understood by one of ordinary skill in the art and the prosecution history pertaining to the patent.” 37 C.F.R. § 42.100(b). “A petition for an *inter partes* review must ‘[p]rovide a statement of the precise relief requested for each claim challenged,’ which ‘statement must identify . . . [h]ow the challenged claim is to be construed’ and ‘[h]ow the construed claim is unpatentable.’” *Hologic v. Enzo*, 2018 Pat. App. LEXIS 5855, *8 (PTAB April 18, 2018) (quoting 37 C.F.R. § 42.104(b)(3)-(4)).

Petitioner takes a dubious approach to claim construction in this proceeding. First, it argues that “no construction may be necessary for this proceeding,” Petition at 13, but it includes claim construction arguments for ten terms of the ’575 patent. Second, in the related district court proceeding,¹ Petitioner argued that many of these terms are means-plus-function terms and indefinite. However here, Petitioner adopts Collabo’s constructions of those terms, *see, e.g.*, Petition at 19, and in contrast to its arguments before the district court, Petitioner appears to be able to ascertain the scope of the limitations in the Petition. Finally, when Petitioner does offer a construction, it repeatedly argues that the alleged prior art

¹ As of the date of this filing, the district court has not yet issued its order regarding claim construction for the ’575 patent. *See* 37 C.F.R. § 42.100(b).

“teaches or suggests either [Petitioner’s or Collabo’s] construction.” *See, e.g.*,
Petition at 14.

Because the failings of the Petition do not turn on the construction of all ten terms identified by Petitioner, Collabo submits that the only term that should be construed is “restores the information necessary in proceeding with the program and evacuated in the information holding unit in time of power shutdown.” *See Wellman, Inc. v. Eastman Chem. Co.*, 642 F.3d 1355, 1361 (Fed. Cir. 2011) (“claim terms need only be construed to the extent necessary to resolve the controversy”) (internal quotation marks omitted).

Claim 1, limitation [1.O], requires that “the CPU, upon receiving the restoration request signal, executes a power supply restoration microprogram, *restores the information necessary in proceeding with the program and evacuated in the information holding unit in time of power shutdown*, and then branches a process to an address indicated by a program counter to continue program execution from a shutdown state.” Ex. 1001 at 19:18-24 (emphasis added).

Petitioner argues that this term should be construed as the CPU . . . “restores *from the information holding unit* the information necessary to proceed with the program, *the information was stored in the information holding unit during power shut down*.” Petition at 21 (emphasis added). That construction adds an

unnecessary element not found in the claims or specification: that the information evacuated from the CPU is restored *from* the information holding unit. Nothing in the claims and specification requires that the information be restored from the information holding unit. Instead, the specification discloses that the information restored during the restoration process be the information that “had been evacuated” during the shutdown process. *See, e.g.*, Ex. 1001 at 9:28-22, 10:18-20. Claim 1 similarly describes the information to be restored. The focus of the claim is the information, not the source from which the information is restored.

The proper construction of this term is that the CPU “restores the information necessary to proceed with the program, the information was evacuated from the CPU in the information holding unit in the power shut down process.”

II. THE ALLEGED BASES OF INVALIDITY.

Petitioner challenges twenty-one claims of the ’575 patent, claims 1-7, 11-12, 15-22, 26-27, and 30-31. Petitioner alleges four grounds of invalidity:

Ground 1—Claims 1-3, 5-7, 11, 15, and 16 are obvious over the combination of U.S. Pub. No. 2007/0157036 to Jahagirdar et al. (“Jahagirdar”) and “Advanced Configuration and Power Interface Specification,” Revision 2.0 (“ACPI”);

Ground 2—Claims 4, 17-22, 26, 30, and 31 are obvious over the combination of Jahagirdar, ACPI, and JP Pat. Appl. No.: S58-169218 to Saito

(“Saito”);

Ground 3—Claim 12 is obvious over the combination of Jahagirdar, ACPI, and U.S. Pat. No. 5,390,350 to Chung *et al.* (“Chung”); and

Ground 4—Claim 27 is obvious over the combination of Jahagirdar, ACPI, Saito, and Chung.

III. THE BOARD SHOULD EXERCISE ITS DISCRETION TO DENY INSTITUTION OF THIS REDUNDANT PETITION.

Petitioner filed a separate petition for *inter partes* review of the same claims of the same patent on the same day. This is exactly the type of case over which the director should exercise his discretion to deny institution. *See* 35 U.S.C. § 314(a); *Cuozzo Speed Techs., LLC v. Lee*, 136 S. Ct. 2131, 2140 (2016) (“the agency’s decision to deny a petition is a matter committed to the Patent Office’s discretion”).

“Two or more petitions filed against the same patent at or about the same time (e.g., before the first preliminary response by the patent owner) may place a substantial and unnecessary burden on the Board and the patent owner and could raise fairness, timing, and efficiency concerns. *See* 35 U.S.C. § 316(b).” TRIAL PRACTICE GUIDE UPDATE (JULY 2019) at 26.

Petitioner argues that it should be able to file two petitions for *inter partes* review of the ’575 patent because it was unable to meet the word limitations imposed by the PTAB rules due to the number of claims it wished to challenge.

Paper 3 (Petitioner’s Notice of Ranking Petitions) at 1.² But Petitioner has created its own word-count problem. Collabo has asserted only *six* claims of the ’575 patent in litigation, *see* Ex. 1015 at 2, while Petitioner challenges *twenty-one* claims in this proceeding. Notably, two of the four grounds for invalidity in this Petition do not involve any claims that have been asserted by Collabo (Ground 2 and Ground 4). *See* Paper 2 at 5. Petitioner states that it “seeks to challenge additional claims” in this proceeding because “Patent Owner may assert additional claims in the future.” Paper 3 at 1. That is rank speculation. Because Petitioner has admittedly sought review of fifteen unasserted claims, this is not the “rare” case when a second petition may be needed because “the patent owner has asserted a large number of claims in litigation[.]” *See* TRIAL PRACTICE GUIDE UPDATE (JULY 2019) at 26.

In addition, speculating further, Petitioner argues that “Collabo may try to antedate Jahagirdar by attempting to swear behind it.” Paper 3 at 4. This also is not the other “rare” case “when there is a dispute about priority date requiring arguments under multiple prior art references.” *See* TRIAL PRACTICE GUIDE UPDATE (JULY 2019) at 26. Petitioner can point to no swear behind dispute that

² Collabo responds to Petitioner’s Notice of Ranking Petitions herein rather than in a separate document. *See* TRIAL PRACTICE GUIDE UPDATE (JULY 2019) at 28.

would justify a second petition.

The only difference Petitioner contends separates Petition 1 from Petition 2 is that Petitioner asserted different references in the two petitions. *See* Paper 3 at 4. But the primary reference on which Petition 2 relies was asserted in Petition 1.

Petition 1 (IPR2019-01523)	Petition 2 (IPR2019-01524)	Similarities
Claims 1, 2, 3, 4, 5, 6, 7, 11, 12, 15, 16, 17, 18, 19, 20, 21, 22, 26, 27, 30, and 31 of the '575 Patent	Claims 1, 4, 5, 7, 12, 15, 16, 17, 20, 22, 27, 30, and 31 of the '575 Patent	All claims challenged in Petition 2 are already challenged in Petition 1
§ 103 combinations over Jahagirdar ACPI Saito Chung	§ 103 combination over Chung Crump	Chung is asserted in both petitions.

Petitioner states that the petitions “challenge different claims,” Paper 3 at 4, but as demonstrated in the chart above, *all* of the claims asserted in the second petition were asserted in the first petition. Next, Petitioner concedes that the “claims are challenged in both petitions,” but argues that the “grounds” are distinct. *Id.* Petitioner does not attempt to explain why the issues addressed by the differences are material, or why two petitions should be instituted even if the Board finds that one petition satisfies petitioner’s burden under 35 U.S.C. § 314(a). All that Petitioner offers is that “the manner in which the primary references disclose the independent claim elements varies,” and the petitions “combine

different³ references in different ways to show that the challenged claims would have been obvious to a person of ordinary skill in the art.” Paper 3 at 4-5. But Petitioner does not explain why that is material and why two petitions and two separate proceedings are warranted. Tellingly, the expert declaration and all other exhibits submitted by Petitioner in support of both petitions are *identical*, so the evidence on which Petitioner relies for the two proceedings does not differ. *Compare* Case IPR2019-01523, Ex. 1003 (Albonesi Declaration) *with* Case IPR2019-01524, Ex. 1003 (Albonesi Declaration); *compare* IPR2019-01523, Paper 2 at v-vi (Petitioner’s Exhibit List) *with* IPR2019-01524, Paper 2 at iv-v (Petitioner’s Exhibit List).

Petitioner admittedly exceeded the word count, and accordingly decided to split its petition into two. Petitioner should not be able to hedge its bets and take two bites at the apple because it was not able to fit its duplicative obviousness combinations into one petition. Petitioner has placed a large burden on the PTAB’s resources and on the Patent Owner in having to defend its patent in two separate proceedings. The PTAB must assess the potential impacts on both the efficiency of the *inter partes* review process and the fundamental fairness of the process for all parties. Petitioner’s serial and duplicative attacks on the ’575 patent negate the

³ The Chung reference is alleged as prior art in both proceedings.

AIA’s goal of a quick and cost effective alternative to litigation by compounding the proceedings. The similarities between the petitions, including the verbatim expert testimony and exhibits warrant denial of this petition.

IV. THE PETITION DOES NOT ESTABLISH THAT EXHIBIT 1006 IS A “PRINTED PUBLICATION.”

An *inter partes* review may only be requested based on “prior art consisting of patents or printed publications.” 35 U.S.C. § 311(b). The petitioner has the burden of production of evidence establishing that the asserted references are applicable as prior art. *Dynamic Drinkware LLC v. Nat’l Graphics, Inc.*, 800 F.3d 1375, 1379 (Fed. Cir. 2015). The Petition does not establish that Exhibit 1006 qualifies as a “printed publication” under 35 U.S.C. § 102. See *Hulu, LLC v. Sound View Innovations, Inc.*, IPR2018-01039, Paper No. 29 (PTAB Dec. 20, 2019) (precedential).

To qualify as a prior art printed publication, a reference “must have been sufficiently accessible to the public interested in the art.” *Blue Calypso, LLC v. Groupon, Inc.*, 815 F.3d 1331, 1348 (Fed. Cir. 2016) (internal quotation marks removed). “‘Because there are many ways in which a reference may be disseminated to the interested public, ‘public accessibility’ has been called the touchstone in determining whether a reference constitutes a ‘printed publication’ bar under 35 U.S.C. § 102(b).’” *Id.* (quoting *In re Hall*, 781 F.2d 897, 898–99 (Fed. Cir. 1986)). “A reference will be considered publicly accessible if it was

“disseminated or otherwise made available to the extent that persons interested and ordinarily skilled in the subject matter or art exercising reasonable diligence, can locate it.” *Blue Calypso*, 815 F.3d at 1348 (quoting *Kyocera Wireless Corp. v. Int’l Trade Comm’n*, 545 F.3d 1340, 1350 (Fed. Cir. 2008)). At this stage, the Petition must “identify, with particularity, evidence sufficient to establish a reasonable likelihood that the reference was publicly accessible before the critical date of the challenged patent and therefore that there is a reasonable likelihood that it qualifies as a printed publication.” *Hulu*, IPR2018-01039, Paper No. 29, slip op. at *13.

Petitioner relies on Exhibit 1006, with cover page stating Advanced Configuration and Power Interface Specification (Revision 2.0), as part of its obviousness case. Petitioner contends that the document comprising Exhibit 1006 was “published and publicly available at least as early as May 4, 1999.” Petition at 5. Specifically, Petitioner argues that “ACPI 2.0 was released July 27, 2000, and was publically available more than one year before the ’575 patent’s earliest possible effective filing date.” *Id.* at 6. As purported support for this statement, the only “evidence” argued in the Petition is that (1) “Intel filed several patent applications that refer to ACPI 2.0 and that were filed more than one year before September 12, 2006” and (2) “[t]he Wayback Machine also shows that the public had access to a webpage containing a link to the ACPI 2.0 document by at least May 4, 1999.” *See id.*

Petitioner's first argument does not show how the legal standard for "public accessibility" is met. That Intel Corporation, one of the five names listed on the cover of the document that is Exhibit 1006, filed patent applications referring to a document it helped create does not establish that the document itself was accessible to the public interested and ordinarily skilled in the art. *See* Ex. 1006 at 0001. The Petition offers no evidence how the filing of such Intel patent applications proves the document was publicly available.

As to Petitioner's second argument, Exhibit 1016 does not "show" that the "public had access to a webpage containing a link to the ACPI 2.0 document[.]" The links in the supporting declaration appear to access compressed ZIP files that were purportedly crawled by the "Wayback Machine." The declaration is unadorned with any of the attachments, or a "webpage containing a link to the ACPI 2.0 document[.]" *See* Ex. 1016.

All grounds for invalidity asserted in the Petition rely on Exhibit 1006 (which Petitioner abbreviates as "ACPI"). *See* Petition at 5. Petitioner has made no effort to demonstrate how the "public accessibility" standard is met by its proffered evidence, and thus how Exhibit 1006 qualifies as a "printed publication." For this reason, the Petition should be denied.

V. NONE OF THE ASSERTED COMBINATIONS RENDER ANY CLAIM OF THE '575 PATENT OBVIOUS.

Jahagirdar, Petitioner's primary reference asserted in this Petition, does not disclose several of the requisite elements of the claims of the '575 patent.

Consequently, Petitioner relies on various combinations with ACPI, Saito, and Chung for a handful of claim elements. For the elements where Petitioner relies solely on Jahagirdar, Petitioner does not show how Jahagirdar teaches or suggests the limitations at issue in the '575 patent. Petitioner's main problem is that Jahagirdar does not teach that its system resides on a single chip. Thus, it does not teach a "microcontroller." Jahagirdar discloses a multi-chip PC (personal computer) system.

Petitioner's other big problem is that, even assuming Petitioner's blanket statement that "[p]ower management has been a longstanding concern in the computer industry" is true, *see* Petition at 7, Jahagirdar does not teach the requisite sequencing or many of the requisite signals claimed by the '575 patent. Therefore, it is not surprising that Jahagirdar operates in a manner much different from the technology claimed in the '575 patent.

The expert testimony that Petitioner cites in arguing that Jahagirdar renders certain claim elements obvious is largely a copy and paste of what Petitioner argues in the Petition. *See, e.g.*, 37 C.F.R. § 42.65(a) ("Expert testimony that does not disclose the underlying facts or data on which the opinion is based is entitled to

little or no weight.”). Conclusory expert testimony such as Petitioner’s cannot support a case for obviousness. Petitioner is left with no disclosure of numerous elements required by the ’575 patent, as detailed below.

When Petitioner does rely on the combinations of Jahagirdar with the ACPI, Saito, and Chung, Petitioner’s bare conclusions do not support a motivation to combine the two references to arrive at the claimed invention. “[O]bviousness concerns whether a skilled artisan not only could have made but would have been motivated to make the combinations or modifications of prior art to arrive at the claimed invention.” *Belden Inc. v. Berk-Tek LLC*, 805 F.3d 1064, 1073 (Fed. Cir. 2015). Petitioner’s motivation to combine arguments that use the ’575 patent as a roadmap are the result of classic hindsight. As such, the Petition does not demonstrate how any of the challenged claims are obvious over the asserted references and should be denied.

A. The Combination Of Jahagirdar And ACPI Does Not Render Claims 1-3, 5-7, 11, 15, Or 16 Of The ’575 Patent Obvious [Ground 1].

1. Limitation [1.Preamble].

A microcontroller comprising:

Petitioner relies solely on Jahagirdar for the claimed “microcontroller” but does not show how Jahagirdar teaches or suggests the “microcontroller” required by the ’575 patent.

As an initial matter, the parties agree that the preamble of claim 1 of the '575 patent is limiting, but disagree over the construction. *See* Ex. 1001 at 18:46 (“A microcontroller comprising:”). Petitioner argues that the term “microcontroller” should be construed as “a chip designed for control applications rather than data-processing that has a complete CPU, semiconductor memory sufficient for control applications, and input/output capability[, that chip includes].” *See* Ex. 1018 at 7; Petition at 14.⁴ In the district court, Collabo’s construction of “microcontroller” was “an integrated circuit.” Ex. 1018 at 7. Regardless of which construction is used in this proceeding, both constructions require the microcontroller to be on a single integrated chip.⁵ *See also* Ex. 2001 (The Authoritative Dictionary of IEEE Standard Terms, 7th Ed. © 2000) (listing “integrated circuit” as a synonym for “chip”). Jahagirdar does not meet either

⁴ In the Petition, Petitioner curiously omits language from its proffered claim construction in the district court: “[, that chip includes].” *Compare* Petition at 14 with Ex. 1018 at 7.

⁵ Petitioner’s omitted language “[, that chip includes],” further demonstrates that that Petitioner contends that the claimed “microcontroller” requires everything to reside on a single chip.

party's proffered construction of "microcontroller."⁶

In describing how this limitation is met, Petitioner argues that "Jahagirdar's system 200" is a microcontroller. Petition at 27. Petitioner then argues that Jahagirdar discloses "a processor 205 (i.e., CPU), a memory 220 which may comprise one or more of random access memory (RAM), flash memory and/or another type of memory (i.e., semiconductor memory), and an input/output (I/O) control hub 225 (i.e., input/output capability)." *Id.* at 27-28. According to Petitioner, because these components allegedly "can be located on the same chip," its proposed construction of the claimed "microcontroller" is met. *See id.* Petitioner's simplistic argument overlooks the biggest problem with Jahagirdar—that it discloses a PC (personal computer) system and *not* a microcontroller.

Numerous disclosures throughout Jahagirdar confirm Jahagirdar's system 200 does not teach a "microcontroller," but rather a PC system with numerous different components that both lay persons and persons of ordinary skill in the art alike would understand to be separate. *See* Ex. 1005 at [0024] ("The system **200** may be a notebook or laptop computer system, or may be any different type of

⁶ Collabo submits that because the reference does not teach the claimed "microcontroller" under either party's construction, no construction is necessary for this term. *Wellman*, 642 F.3d at 1361.

mobile electronic system such as a mobile device, personal digital assistant, wireless telephone/handset or may even be a non-mobile system such as a desktop or enterprise computing system.”); *id.*, Figure 2; *id.* at [0038] (“The mass storage device **230** may include one or more compact disc read-only memory (CD-ROM) drive(s) and associated disc(s), one or more hard drive(s) and associated disk(s) and/or one or more mass storage devices accessible by the computing system **200** over a network.”); *id.* at [0040] (“Also, it should be appreciated that system **200** may include a display device, such as a cathode ray tube (CRT) or liquid crystal display (LCD), for displaying information to a user. Further, system **200** may include an alphanumeric input device (e.g., a keyboard), including alphanumeric and other keys, for communicating information and command selections to processor **205**.”); *id.* at [0041] (“Another device that may included with system [sic] is a hard copy device, which may be used for printing instructions, data, or other information on a medium such as paper, film, or similar types of media. Furthermore, a Sound recording and playback device, such as a speaker and/or microphone (not shown) may optionally be included in system **200** for audio interfacing.”); *id.* at [0042] (“Where the system **200** is a mobile or portable system, a battery or battery connector **255** may be included to provide power to operate the system **200** either exclusively or in the absence of another type of power source.

Additionally, for some embodiments, an antenna **260** may be included and coupled to the system **200** via, for example, a wireless local area network (WLAN) device **261** to provide for wireless connectivity for the system **200**.”).

Additionally, Jahagirdar teaches that its system 200 comprises a “chipset,” not a “chip.” *Id.* at [0034]. Jahagirdar states that its processor 205 “may be an Intel® architecture microprocessor[.]” *Id.* at [0026]. The exhibits attached to the Petition show that the Intel architecture referenced in Jahagirdar is implemented in computer systems having multiple chips on a motherboard, such as the evaluation board depicted in Exhibit 1024, “a full-featured system board with two Pentium III processors . . . and the Intel 840 Chipset. . . . The 840 chipset includes the [Memory Controller Hub] MCH, [I/O Controller Hub] ICH, [PCI 64 Hub] P64H and the [Firmware Hub] FWH.” *See* Ex. 1024 at 2.1, 2.1.1, 3.3 (reproduced below).

2.1 Overview

The evaluation board consists of a baseboard with two Intel Pentium III processors, the 840 chipset, and other system board components and peripheral connectors.

Note: The evaluation board is shipped as an open system, allowing for maximum flexibility in changing hardware configuration and peripherals. Because the board is not in a protective chassis, the user must observe extra precautions when handling and operating the system.

2.1.1 Baseboard Features

The evaluation board features are summarized below:

- Full support for two Intel® Pentium® III processors with 256 Kbytes of on-die L2 Cache at up to 866 MHz core bus speed. The baseboard supports a 100 or 133 MHz Processor System Bus.
- Intel® 840 chipset:
 - 82840 Memory Controller Hub (MCH)
 - 82801AA I/O Controller Hub (ICH)
 - 82802AB/82802AC Firmware Hub (FWH)
 - 82806AA PCI 64 Hub (P64H)

3.3 System Operation

The Intel® Pentium® III processor/840 evaluation board is a full-featured system board with two Pentium III processors with 256 Kbytes of on-die L2 cache in a PGA370 socket, and the Intel 840 Chipset. The supported core and processor side bus frequencies are up to 866 MHz/133 MHz. The 840 chipset includes the MCH, ICH, P64H and the FWH. The board also supports RDRAM and other system and I/O peripherals.

See also *id.* at Figure 2-1 (reproduced and annotated below) (Evaluation board with the two processors shaded red, and the I/O Controller Hub (ICH) on the 840 chipset shaded blue).

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Consistent with this Intel architecture, Jahagirdar teaches that its input/output (I/O) control hub 225 is located on a different chip than that of the CPU. Jahagirdar states that its “chipset” contains a “graphics and memory control hub (G/MCH),” the North bridge, and the “I/O control hub **225** which may be referred to as a South bridge[.]” Ex. 1005 at [0034]. The “chipset features may be partitioned in a different manner and/or may be implemented using a different number of integrated circuit chips.” *Id.* As an example, Jahagirdar states that its “graphics and memory control applications may be provided using separate integrated circuit devices.” *Id.* at [0035]. As shown above, the Intel Pentium III microprocessor is implemented in a system that has separate North bridge (MCH) and South bridge (ICH) chips on its evaluation baseboard. *See* Ex. 1024 at 2.1, 2.1.1, 3.3, Figure 2-1. It is clear that Jahagirdar teaches a system 200 comprising of multiple chips. Because Jahagirdar’s multi-chip system is not integrated on a single chip, it does not teach a “microcontroller” under either party’s construction.

Petitioner argues that “Jahagirdar’s components can be located on the same chip.” Petition at 28 (citing Ex. 1005, [0102]). The cited portion of Jahagirdar, however, states that various embodiments “*may be applied* to different power management configurations and/or for different types of integrated circuits.” Ex. 1005 at [0102]. That the teachings of Jahagirdar “may be applied” to other types of configurations or for different types of integrated circuits does not mean that

Jahagirdar's system 200, which Petitioner relies on as the claimed "microcontroller," is or can be itself located on a single chip.

The declaration of David H. Albonesi (Ex. 1003 at ¶ 147) that Petitioner cites as purported support for this conclusion is just a verbatim recitation of what is stated in the Petition and is not evidence that Jahagirdar's system 200 teaches the claimed "microcontroller." See *InfoBionic, Inc. v. Braemer Manufacturing, LLC*, IPR2015-01704, Paper 11 slip op. at 14-15 (PTAB Feb. 16, 2016) ("Ppetitioner's arguments and Dr. Stone's testimony repeating the same (with the addition of the phrase 'in my opinion') are too conclusory to persuade us that Petitioner has met its burden at this stage of the case.") (citing 37 C.F.R. § 42.65(a) ("Expert testimony that does not disclose the underlying facts or data on which the opinion is based is entitled to little or no weight."))).

Lastly, Petitioner argues that Jahagirdar teaches that its "*processor* could be an embedded processor, which is synonymous with a microcontroller." See Petition at 28 (citing Ex. 1005, [0027]) (emphasis added); see Ex. 1005 at [0027] ("In other embodiments, the processor **205** may be a different type of processor such as a digital signal processor, an embedded processor, or a microprocessor from a different source."). This is irrelevant. Petitioner is not relying on Jahagirdar's processor 205 (CPU) as the claimed "microcontroller." Moreover, Petitioner cites no evidence (apart from the verbatim paragraph 147 of Dr.

Albonesi's declaration) to support its conclusion that an "embedded processor" is synonymous with a "microcontroller." And the Petition does not argue that the processor 205 contains a power supply unit, power supply control unit, or a clock generator, which Petitioner's construction requires to be integrated on the same chip. In arguing that "an embedded processor" is synonymous with "microcontroller," Petitioner asks the Board to ignore its proffered construction of "microcontroller."

There is no disclosure within Jahagirdar that teaches a "microcontroller." 37 C.F.R. § 42.104(b) requires a petitioner to "identify how each challenged claim is to be construed," and "specify where each element of the claim is found" in the references. Petitioner has not shown how a "microcontroller," either under its own construction or under Collabo's, is taught in Jahagirdar.

2. Limitation [1.C].

a power supply control unit for controlling the CPU and the power supply unit;

The microcontroller of claim 1 requires a "power supply control unit for controlling the CPU and the power supply unit." Ex. 1001 at 18:50-51. In the related district court proceeding, Petitioner argued the term "power supply control unit" was indefinite. Ex. 1018 at 12-13. However here, Petitioner adopts Collabo's construction, Petition at 19, which Collabo argued was the plain and ordinary

meaning and that no construction was required. Ex. 1018 at 12. Petitioner concludes, without citation, that it “understands” the plain and ordinary meaning to be “logic/circuitry for controlling the CPU and power supply unit.” Petition at 19. Petitioner’s construction (which was not Collabo’s), merely substitutes the words “logic/circuitry” into the language in which the term “power supply control unit” appears in claim 1. See Ex. 1001 at 18:50-51 (“a power supply control unit for controlling the CPU and power supply unit”). Nonetheless, Jahagirdar does not teach or suggest the claimed “power supply control unit.”

Petitioner argues that “Jahagirdar’s I/O control hub, clock/power management unit 350, and zero voltage entry/exit logic 354 together teach or suggest the recited ‘power supply control unit.’” Petition at 32. Petitioner contends the microcontroller chip “has a complete CPU, semiconductor memory sufficient for control applications, and input/output capability.” *Id.* at 14. Collabo’s construction also requires the “microcontroller” to be an single chip. See *id.* (“integrated circuit”). As explained above, Jahagirdar’s input/output (I/O) control hub 225 resides on a different chip than that of the CPU. See *supra*, V.A.1 (Limitation [1.Preamble]). Jahagirdar’s I/O control hub 225 cannot be part of the claimed “power supply control unit” since it must reside on the same chip as all of the other components including the CPU, and without it, the clock/power management unit 350 and zero voltage entry/exit logic 354 (depicted as inside

Jahagirdar's CPU 205, *see* Ex. 1005 at Figure 2A), admittedly do not perform all of the requisite functions of the "power supply control unit" in claim 1. Jahagirdar, which does not teach a microcontroller, does not teach the required "power supply control unit."

3. Limitation [1.F].

the power supply control unit outputs a shutdown request signal to the CPU in response to an occurrence of a power shutdown factor,

Claim 1 (limitations [1.F] and [1.G], as well as claim 17 limitations [17.E] and [17.F]) requires a "shutdown request signal." Ex. 1001 at 18:56-59, 20:59-62. Petitioner does not precisely identify any particular signal that teaches the claimed "shutdown request signal" that is output by the "power supply control unit" to the CPU in response to an occurrence of a power shutdown factor.

First, Petitioner argues that "Jahagirdar's I/O control hub outputs multiple shutdown request signals (i.e., signals that control transitions between at least a subset of the C-states) at different stages as the CPU transitions between various known C-states to conserve power and reduce thermal load (i.e., power shutdown factors)." Petition at 38. But Petitioner does not identify which of the unspecified "signals" is the "shutdown request signal" required by the '575 patent. Petitioner also states that Jahagirdar's "power management state control logic 242" "use[s] one or more of" five different signals, "stop clock (STPCLK#), processor sleep

(SLP#), deep sleep (DPSLP#), deeper stop (DPRSTP#), and/or stop processor (STPCPU#) signals.” *Id.* at 38-39. Which signal is the claimed “shutdown request signal”? Which signal is output in response to a “power shutdown factor”? Petitioner does not state. The Petition is silent as to these essential requirements, and merely quoting that Jahagirdar discloses “one or more signals” does not satisfy Petitioner’s burden of “specify[ing] where each element of the claim is found in the prior art or printed publications relied upon.” 37 C.F.R. § 42.104(b)(4).

4. Limitation [1.G].

the CPU, upon receiving the shutdown request signal, executes a power shutdown microprogram, evacuates the information necessary in proceeding with the program to the information holding unit, and outputs an evacuation completed signal to the power supply control unit after evacuation is completed,

The ’575 patent requires that after receiving the “shutdown request signal” from the “power supply control unit,” the CPU executes a “power shutdown microprogram” and “evacuates the information necessary in proceeding with the program to the information holding unit[.]” Ex. 1001 at 18: 59-62, 20:62-65.

This limitation is not met because Petitioner has not identified a “shutdown request signal.” *See supra*, V.A.3 (Limitation [1.F]).

Additionally, a “power shut down microprogram” and “evacu[at]ion [of] the information necessary in proceeding with the program to the information holding unit” is not performed by the CPU in response to any signal from the alleged “power supply control unit” in Jahagirdar. Petitioner incorrectly asserts that Jahagirdar’s CPU transitions “to a lower power state, in response to (i.e., upon receiving) a shutdown request signal from the I/O control hub.” See Petition at 39-40. Jahagirdar’s CPU shuts down after it executes an MWAIT instruction. Jahagirdar states that “the entry into the zero voltage processor sleep state may be initiated via an MWAIT instruction.” Ex. 1005 at [0065]; *see also id.* at [0045]. The MWAIT instruction is executed by CPU core 320 or 322. *Id.* at [0066-0067]. As Petitioner previously argued with respect to a different limitation, “Jahagirdar discloses an event where its CPU ‘may be transitioned to a lower power state... in response to firmware, such as microcode, or software, such as the operating system 245, or even ACPI software in some cases, executing a HALT or MWAIT instruction (not shown), the processor 205 may transition to the C1 or Auto-HALT state.’” Petition at 38 (citing Ex. 1005 at [0045]). This confirms that there is no “signal” sent from Jahagirdar’s I/O control hub (or clock/power management unit 350, or zero voltage entry/exit logic 354) (together, Petitioner’s alleged “power supply control unit”) to the CPU in order for it to begin the transition into a lower power state or to evacuate the necessary information to the information holding

unit. In other words, the CPU decides that it will enter a lower power state and then does so by initiating a “sleep or MWAIT instruction” executed by either of its cores that it received from firmware/software or its operating system. This is not done in response to receiving any “signal” from the I/O control hub.

Figure 4, which Petitioner relies on as purported support for its erroneous argument, confirms that no “signal” from either of Jahagirdar’s I/O control hub, clock/power management unit 350, or zero voltage entry/exit logic 354 (together, the alleged “power supply control unit”) is what initiates power shut down and state saving of the CPU.

Looking particularly at FIG. 4, an illustration of entry into the zero voltage processor sleep state is provided. As shown in FIG. 4, each core *independently performs a state save* when the zero voltage processor sleep state is initiated. Particularly, looking at CPU core #0320, the first CPU core #0 is active (circle 402) and then *a command for a zero voltage sleep state is initiated (e.g. via a sleep or MWAIT instruction)* (circle 404). Responsive to this, *the state of CPU core 320 is saved at circle 406* to dedicated cache memory 340. This includes the dedicated state 325 and the shared state 324. CPU core 320 then goes into a first sleep state 408 (e.g. CC6) in which it waits for the other core to get into the CC6 state as well, before the whole package can transition into the overall package sleep state (e.g. C6).

Id. at [0068] (emphasis added); *see also id.* at Figure 4.

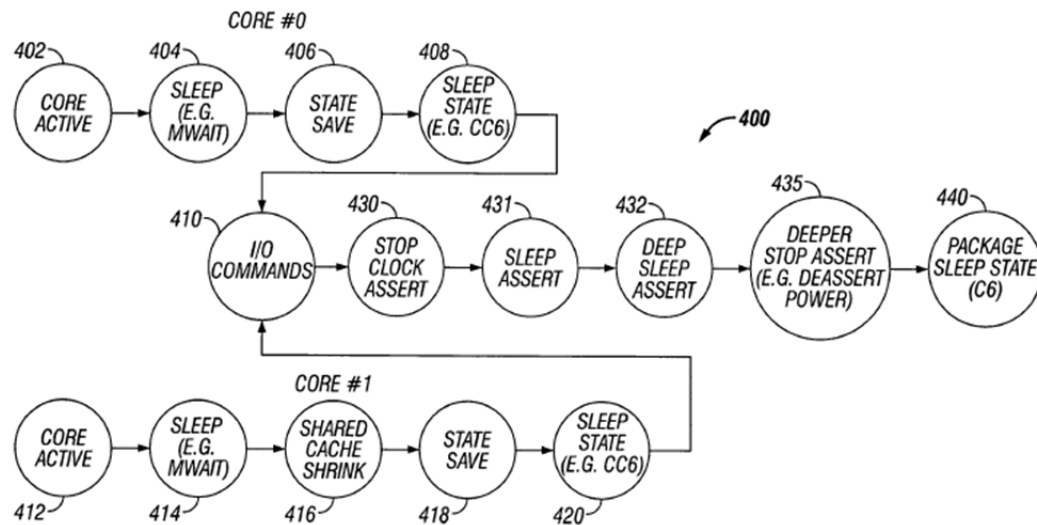


FIG. 4

The fact that Jahagirdar’s power shut down process is initiated by a sleep/MWAIT instruction at the CPU core further exemplifies how none of Petitioner’s unspecified “signals” output from the I/O control hub or any of the five signals used by power management state control logic 242 (“stop clock (STPCLK#), processor sleep (SLP#), deep sleep (DPSLP#), deeper stop (DPRSTP#), and/or stop processor (STPCPU#) signals”) could be the claimed “shutdown request signal” sent from the “power supply control unit.” See Petition at 38-39. Each of those alleged “signals” is transmitted much later in Jahagirdar’s process, *after and not before* Jahagirdar’s CPU state was saved (circle 406) and power reduction began (circle 408). See Ex. 1005 at [0071], [0073-0074]; *id.* at Figure 4 (circles 410, 430, 431, 432, 435).

The '575 patent requires that after (1) receiving the “shutdown request signal” from the “power supply control unit,” (2) executing a “power shutdown microprogram,” and (3) “evacuat[ing] the information necessary in proceeding with the program to the information holding unit,” the CPU then (4) outputs an “evacuation completed signal” to the “power supply control unit” after the evacuation is completed. Ex. 1001 at 18:59-64, 20:62-67.⁷ Since Jahagirdar’s CPU sleep (e.g. MWAIT instruction) (circle 404) and state save (circle 408) do not occur in response to a signal from the “power supply control unit,” Jahagirdar does not teach steps (1) through (3). See Ex. 1005 at [0068], Figure 4. Similarly, Jahagirdar does not teach the last step of this limitation—that the CPU output an “evacuation completed signal” to the “power supply control unit.”

The fact that Jahagirdar’s CPU initiates power shutdown on its own, and not in response to a signal from the I/O control hub, clock/power management unit 350, or zero voltage entry/exit logic 354 alleged to be the “power supply control unit,” further exemplifies why there is no “evacuation completed signal” sent from Jahagirdar’s CPU to the “power supply control unit.” Jahagirdar’s CPU does not

⁷ Claim 1 limitations [1.H] and [1.J], as well as claim 17 limitations [17.F] and [17.G] also require the claimed “evacuation completed signal.” See Ex. 1001 at 18:65-67, 19:4-6, 20:62-67, 21:1-4.

need to communicate with either of the I/O control hub, clock/power management unit 350, or zero voltage entry/exit logic 354 in order to begin entering into a lower power state. Jahagirdar is clear that the saving of the CPU state (circle 406) occurs immediately after the sleep/MWAIT instruction (circle 404), and not after receiving any signal from the I/O control hub. *See id.*, Figure 4; *id.* at [0068]. The CPU core “then goes into a first sleep state **408** (e.g., CC6) in which *it waits* for the other core to get into the CC6 state as well, before the whole package can transition into the overall package sleep state (e.g. C6).” *Id.* Jahagirdar’s CPU is in control of these processes, *not* the I/O control hub, clock/power management unit 350, or zero voltage entry/exit logic 354.

Petitioner argues that because Jahagirdar’s “sleep states are not entered[] until the required CPU state information has been saved[,]” “it would have been obvious to a POSITA that clock/power management logic 350 would have initiated the sleep state transition in response to an indication that the state data has been saved.” Petition at 41. This, Petitioner argues, “could be in the form of an internal signal or setting a flag.” *Id.* Petitioner points to no disclosure in Jahagirdar of a need for any “internal signal” or “setting [of] a flag” for the CPU to indicate to the alleged “power supply control unit.” Petitioner’s argument is a hindsight-based attempt to create a signal where one does not exist.

Petitioner’s expert Dr. Albonesi argues that Jahagirdar’s CPU cores

“coordinate in order to simultaneously enter the deep sleep state.” See Ex. 1003 at ¶ 177 (citing Ex. 1005 at [0068-0069]). Thus, he suggests, a “POSITA would know that that coordination would require a signal to be sent from Core #1 to Core #0 . . . to affect the transition from state 406 to 408, and some form of internal signaling or flag setting would have to occur within Core #1 to affect transition from state 418 to 420.” *Id.* No signal sent “from Core #1 to Core #0” meets the requirement that it go “to the power supply control unit.” Ex. 1001 at 18:62-64. Dr. Albonesi’s hindsight conclusions are further exposed by turning to the material cited.

Jahagirdar states that “each core *independently* performs a state save when the zero voltage processor sleep state is initiated.” Ex. 1005 at [0068] (emphasis added). The CPU core then “waits for the other core to get into the CC6 state as well, before the whole package can transition into the overall package sleep state (e.g. C6).” *Id.* The only waiting that occurs by the first CPU core is *after it has entered sleep state CC6*. Thus, if anything “internal” were to happen between one CPU core to the other, it would not be after the CPU core saves its state, but after it entered into sleep state CC6. See *id.* Additionally, any “coordination” between the two CPU cores would be *between the two CPU cores* after they had entered sleep state CC6 and before they transition into sleep state C6, and not from the CPU to the alleged “power supply control unit” after the information had been evacuated as required by the ’575 patent. This shows that Petitioner’s, and its expert’s,

conclusions are nothing more than impermissible hindsight. “[R]ejections on obviousness grounds cannot be sustained by mere conclusory statements; instead, there must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness.” *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 418 (2007) (quoting *In re Kahn*, 441 F.3d 977, 988 (Fed. Cir. 2006)); see also *TQ Delta, LLC v. Cisco Sys.*, 942 F.3d 1352, 1361 (Fed. Cir. 2019) (explaining that the Federal Circuit has “repeatedly expressed concerns that crediting such testimony risks allowing the challenger to use the challenged patent as a roadmap to reconstruct the claimed invention using disparate elements from the prior art—i.e., the impermissible ex post reasoning and hindsight bias that *KSR* warned against.”).

Jahagirdar’s system 200 and the microcontroller of the ’575 patent operate in different ways in preserving the state of a CPU and in shutting down power to the CPU. The ’575 patent’s “evacuation completed signal” output from the CPU tells the “power supply control unit” that the evacuation of the information necessary in proceeding with the program has been completed, so that the “power supply control unit” can continue from there in the power shut down process.

[T]he CPU . . . outputs an evacuation completed signal to the power supply control unit after evacuation is completed,
the power supply control unit, upon receiving the

evacuation completed signal, outputs a power shutdown control signal to the power supply unit, the power supply unit shuts down power supply to the CPU upon receiving the power shutdown control signal from the power supply control unit[.]

Ex. 1001 at 18:59-19-3. No “internal” signal between the CPU cores in Jahagirdar after the cores have entered a sleep state can teach what is required of the ’575 patent.

5. Limitation [1.H].

the power supply control unit, upon receiving the evacuation completed signal, outputs a power shutdown control signal to the power supply unit,

The ’575 patent requires that once the “power supply control unit” receives the “evacuation completed signal,” it output a “power shutdown control signal” to the “power supply unit.” Ex. 1001 at 18:65-67. Petitioner has not shown this limitation to be obvious because Jahagirdar does not teach or suggest an “evacuation completed signal” that is sent from the CPU to the “power supply control unit.” *See supra*, V.A.4 (Limitation [1.G]). Thus, there is no teaching that “upon receiving the evacuation completed signal,” the “power supply control unit” “outputs a power shutdown control signal to the power supply unit.”

Even assuming Petitioner’s alleged “evacuation completed signal” discloses that of the ’575 patent, the alleged “power supply control unit” in Jahagirdar does

not output a “power shutdown control signal” to the “power supply unit” upon receipt of that “evacuation completed signal.” The Petition is silent as to how Jahagirdar’s alleged “power supply control unit” receives the “evacuation completed signal” and then “outputs a power shutdown control signal.” See Petition at 42-43. For this reason, Petitioner has failed to show how the limitation is met.

Petitioner alleges that a “CPU VID signal” once it is switched to a zero voltage level is the claimed “power shutdown control signal.” *Id.* at 42. “VID” stands for a “voltage identification.” See Ex. 1005 at [0031]. The plain language of Jahagirdar, however, confirms that the “CPU VID” cannot be the claimed “power shutdown control signal” that is sent from the “power supply control unit” to the “power supply unit.” Jahagirdar states that the “CPU 205” “switches its VID to a zero voltage level” “in order to tell the voltage regulator 212 to remove power and that it is safe to do so”—*not* from the alleged “power supply control unit” (I/O control hub, clock/power management unit 350, or zero voltage entry/exit logic 354) as is required by the ’575 patent. *Id.* at [0074]. Jahagirdar teaches that its “voltage regulator **212** is coupled to *receive VID signals from the processor 205* over a bus **235** and, responsive to the VID signals, provides an associated operating voltage to the processor **205** over a signal line **240**.” *Id.* at [0033]; see also *id.* at Figure 2A (showing VID code being sent from CPU 205 to voltage regulator 212

over a bus 235). Jahagirdar does not teach or suggest that the “power supply control unit” outputs a “power shutdown control signal” to the “power supply unit” “upon receiving the evacuation completed signal.”

Petitioner alleges that Jahagirdar’s clock/power management unit 350 “switch[es] the CPU VID to a zero voltage level” after “Jahagirdar’s I/O control hub outputs a DPRSTP# command.” Petition at 42-43. Setting aside the fatal fact that the switching of the CPU VID originates at CPU 205 and not clock/power management unit 350, Petitioner did not allege that DPRSTP# is the claimed “evacuation completed signal,” nor could it because it occurs much later down the line in the sequencing of events after the CPU’s state is saved. See Ex. 1005 at Figure 4 (annotated below) (“state save” at circle 406, and “deeper stop assert” at circle 435).

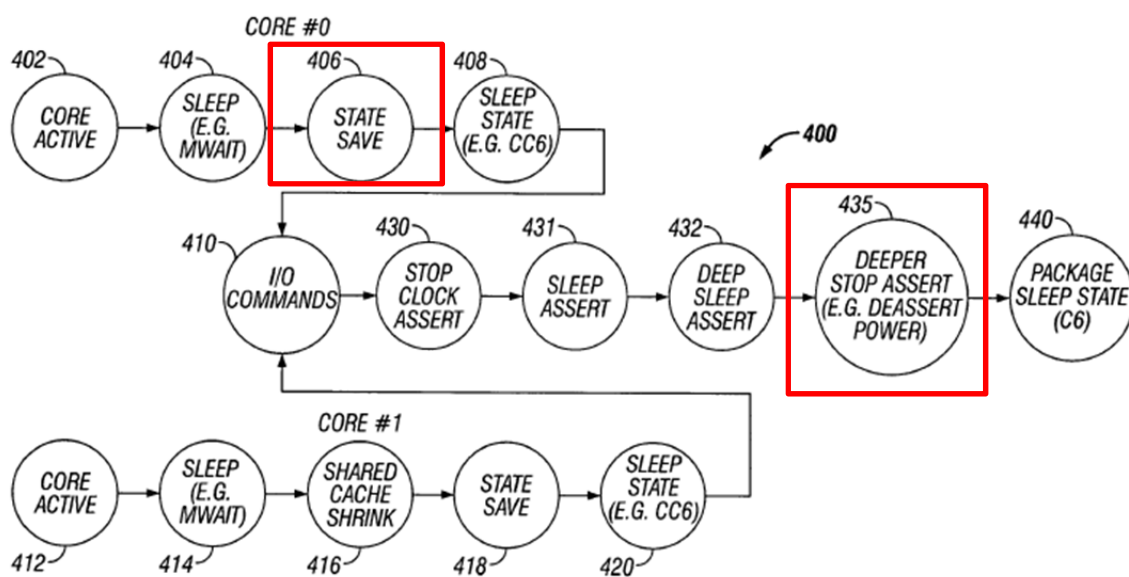


FIG. 4

Petitioner's omission of this critical detail is telling. In explaining the requisite "series of operations" for its process of entering the zero voltage processor sleep state, Jahagirdar states that the DPRSTP# signal is asserted at circle 435. *Id.* at [0065], [0074], Figure 4. Jahagirdar teaches the following series of operations:

The I/O commands **410** may be issued from the ICH **225**/MCH **215**. Particularly, a stop clock signal may be asserted at circle **430** (e.g. STPCLK#). Then, a sleep signal may be asserted. (circle **431**) (e.g. SLPH). Further, at circle **432**, a deep sleep signal may be asserted (DPSLP#). *These commands are issued in the previously-described order such that the CPU 205 responds by shutting off its internal clock distribution and then the PLLs. When at circle 435, a deeper stop signal is asserted (e.g., DPRSTP#), the CPU 205 switches its VID to a zero voltage level in order to tell the voltage regulator 212 to remove power and that it is safe to do so.*

Id. at [0073-0074] (emphasis added). No argument by Petitioner can counter the fact that Jahagirdar's commands are "issued" in the described "order" such that the CPU responds by first "shutting off its internal clock distribution and then the PLLs" ("phase lock loops" in the processor). Then, "when at circle 435" the deeper stop (DPTSTP#) signal is asserted and "CPU **205** switches its VID to a zero voltage level" (the alleged "power shutdown control signal"). This is nearly at the end of Jahagirdar's CPU shutdown process, and not possibly "upon receiving" the

alleged “evacuation completed signal” (albeit by the CPU core and not the alleged “power supply control unit”). Jahagirdar’s disclosed sequencing is in a completely different order than that required of the ’575 patent, and thus cannot render it obvious.

6. Limitation [1.I].

the power supply unit shuts down power supply to the CPU upon receiving the power shutdown control signal from the power supply control unit,

The compounding nature of the Petition’s problems are shown when continuing on through the limitations of claim 1. As explained with respect to limitation [1.H], *see supra* V.A.5, the alleged “power supply unit” in Jahagirdar does not “receiv[e] the power shutdown control signal from the power supply control unit” as required by claim 1. *See* Ex. 1001 at 19:1-3. Thus, Jahagirdar’s “power supply unit” cannot “shut[] down power supply to the CPU *upon receiving the power shutdown control signal from the power supply control unit.*” *Id.* (emphasis added).

Petitioner relies on the same arguments and signals in Jahagirdar as it did with respect to limitation [1.H]. As explained above, Jahagirdar’s “CPU 205 switches its VID to a zero voltage level in order to tell the voltage regulator 212 to remove power and that it is safe to do so.” Ex. 1005 at [0074] (emphasis added). Jahagirdar’s CPU is in charge of controlling the power shut down. It is the CPU

that communicates with the voltage regulator 212. *Id.* Thus, Jahagirdar’s shutting down of power to the CPU is not done upon receipt of a “power shutdown control signal” from the “power supply control unit” to the “power supply unit” as required by the ’575 patent.

7. Limitation [1.J].

the power supply control unit, upon receiving the evacuation completed signal, outputs a clock stop control signal to the clock generator,

The microcontroller of the ’575 patent requires that its “power supply control unit” output a “clock stop control signal to the clock generator” “upon receiving the evacuation completed signal.” Ex. 1001 at 19:4-6. Petitioner has not shown this limitation to be obvious because Jahagirdar does not teach or suggest an “evacuation completed signal” received by the “power supply control unit.” See *supra*, V.A.4 (Limitation [1.G]). There is thus no teaching in Jahagirdar that “upon receiving the evacuation completed signal,” the “power supply control unit” “outputs a clock stop control signal to the clock generator.”

8. Limitation [1.K].

the power supply control unit outputs a power supply control signal to the power supply unit in response to an occurrence of a power supply restoration factor,

Claim 1 of the '575 patent (limitations [1.K] and [1.L]) requires a “power supply control signal” that is output from the “power supply control unit” to the “power supply unit” “in response to an occurrence of a power supply restoration factor.” Ex. 1001 at 19:7-11. Petitioner relies solely on Jahagirdar for the claimed “power supply control signal,” but Jahagirdar does not teach this signal that is output from the “power supply control unit.”

Petitioner argues that “Jahagirdar’s exit sequence ‘may be considered the reverse of what happens during the previously-described entry phase.’” Petition at 46 (citing Ex. 1005 at [0077]). For the “previously-described entry phase,” Petitioner argued that Jahagirdar’s “CPU VID signal,” once it is switched to a zero voltage level, was the claimed “power shutdown control signal.” See Petition at 42. As pointed out above, Jahagirdar’s plain language states that “[w]hen at circle **435**, a deeper stop signal is asserted (e.g., DPRSTP#), *the CPU 205 switches its VID* to a zero voltage level in order to tell the voltage regulator **212** to remove power and that it is safe to do so”—*not* from the “power supply control unit” as is required by the '575 patent. Ex. 1005 at [0074] (emphasis added); *see also id.* at Figure 2A

(showing VID code 235 being sent from CPU 205 to voltage regulator 212); *see supra*, V.A.5 (Limitation [1.H]).

For the claimed “power supply control signal,” Petitioner again relies on a “VID.” Petitioner argues that “Jahagirdar teaches an exit sequence from the zero voltage processor sleep state that typically occurs when an interrupt event (i.e., a power supply restoration factor) necessitates waking up the CPU, which causes *a low frequency mode VID* (i.e., power supply control signal) to be sent to the voltage regulator (i.e., power supply unit).” Petition at 45 (citing Ex. 1005 at [0077-0078]) (emphasis added).

As the “reverse” of what happened at power shutdown, Jahagirdar explains that after “deeper stop signal (DRPSTP#) is deasserted (circle **502**) which is detected by the CPU **205** and the zero voltage entry/exit logic **354** of the clock/power management logic **350**,” the “low frequency mode (LFM) VID is sent to the voltage regulator 212.” Ex. 1005 at [0078]. Jahagirdar also confirms that this “low frequency mode VID” (as with the “VID” that was switched to a “zero voltage level”) is sent from Jahagirdar’s CPU 205 to voltage regulator 212—*not* from the alleged “power supply control unit” (I/O control hub, clock/power management unit 350, or zero voltage entry/exit logic 354) as is required by the ’575 patent. *Id.* at [0078]. Jahagirdar teaches that its “voltage regulator **212** is coupled to *receive VID signals from the processor 205* over a bus **235** and,

responsive to the VID signals, provides an associated operating voltage to the processor **205** over a signal line **240**.” *Id.* at [0033]; *see also id.*, Figure 2A (showing VID code being sent from CPU 205 to voltage regulator 212 over a bus 235); *see also id.* at [0074]. Jahagirdar does not teach or suggest that the “power supply control unit” outputs a “power supply control signal” to the “power supply unit” in response to an occurrence of a power supply restoration factor.

9. Limitation [1.L].

the power supply unit, upon receiving the power supply control signal, starts to supply power to the CPU,

Limitation [1.L] similarly requires the “power supply control signal” described in limitation [1.K]. Ex. 1001 at 19:7-11. As explained with respect to limitation [1.K], *see supra* V.A.8, the alleged “power supply control signal” in Jahagirdar is not output from the “power supply control unit” to the “power supply unit” as is required by claim 1. *See* Ex. 1001 at 19:7-11. Rather, it is output from Jahagirdar’s CPU 205. *See* Ex. 1005 at [0033], [0074], [0078]; *see also id.*, Figure 2A. Since Jahagirdar’s “power supply unit” did not receive the low frequency mode VID (the alleged “power supply control signal”) from the “power supply control unit,” it cannot “start[] to supply power to the CPU” “*upon receiving the power supply control signal.*” Ex. 1001 at 19:10-11 (emphasis added).

10. Limitation [1.M].

the power supply control unit outputs a restoration request signal to the CPU and outputs a clock supply control signal to the clock generator when a supplied power supply voltage is stabilized,

The '575 patent requires that the “power supply control unit” output (1) a “restoration request signal” to the CPU and (2) a “clock supply control signal” to the “clock generator” when a supplied power supply voltage is stabilized. Ex. 1001 at 19:12-15. Claim 1 limitations [1.M] and [1.O] as well as claim 17 limitations [17.G] and [17.H] require the claimed “restoration request signal,” and claim 1 limitations [1.M] and [1.N] require the claimed “clock supply control signal.” See *id.* at 19:12-15, 19:18-24, 21:1-8.

Petitioner argues that “when Jahagirdar’s control hub *de-asserts* the DPRSTP# signal, it acts as the restoration request signal.” Petition at 47. From that, Petitioner simply concludes that “Jahagirdar teaches outputting a state restore signal (i.e., a restoration request signal) to the CPU.” This conclusion is not supported.

Petitioner does not explain how the deassertion of deeper stop (DPRSTP#) is a “signal” output from the “power supply control unit” to the CPU, and Jahagirdar does not teach that it operates as a “restoration request signal.” Petitioner also omits many of the steps described in Jahagirdar’s “exit sequence” from the zero

voltage processor sleep state to obscure Jahagirdar’s shortcomings. Jahagirdar’s “exit sequence” as written confirms that the “deassertion” of deeper stop (DPRSTP#) is not a “signal” to the CPU that causes the “restoration” of the CPU state.

From the package sleep state (C6) (circle **440**) in one embodiment, *the deeper stop signal (DPRSTP#) is deasserted (circle 502)* which is detected by the CPU **205** and the zero voltage entry/exit logic **354** of the clock/power management logic **350** such that the low frequency mode (LFM) VID is sent to the voltage regulator **212**. This indicates to the voltage regulator **212** to drive the core operational voltage back up to the required VID.

Ex. 1005 at [0078] (emphasis added); *see also id.* at Figure 5 (deassertion of DPRSTP# outlined in red).

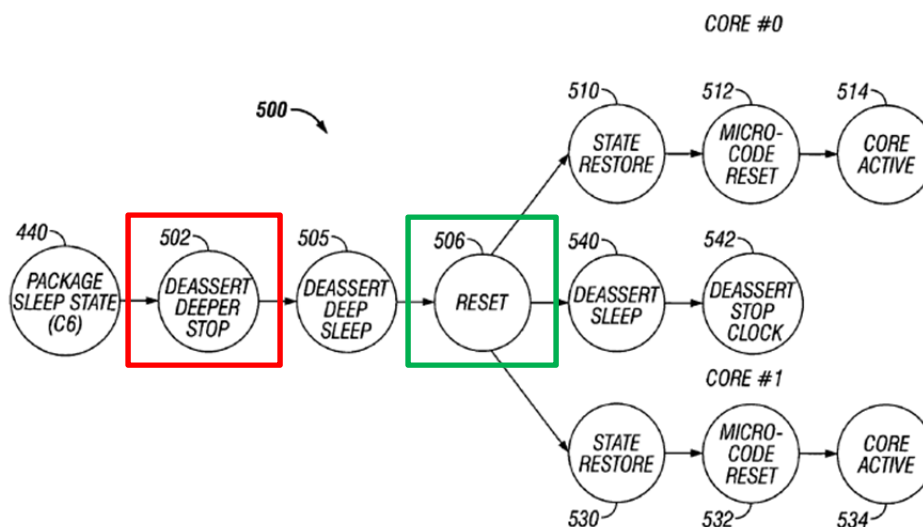


FIG. 5

The “deassertion” of the line where deeper stop (DPRSTP#) was active does not cause the CPU to restore. Only later down the line in Jahagirdar’s process (at circle 506) does the CPU “RESET” occur. *See id.*, Figure 5 (CPU RESET outlined in green). Indeed, Petitioner cites this latter part of the process, which starts from circle 505 as purported support for the “deassertion” of the DPRSTP# signal being a “restoration request signal.” *See* Petition at 47 (citing Ex. 1005 at [0079]).

Paragraph [0079] of Jahagirdar states:

At a predetermined time (e.g. controlled by timers in the ICH 225), a signal to assert the clocks back on is asserted and the *deep sleep (DPSLP#)* signal is de-asserted (circle **505**), which initiates the PLLS of the clock/power management logic **350**. *After this*, CPU **305** initiates an internal RESET (circle **506**). *After this reset is complete*, CPU **205** has the power and clocks engaged and *is ready to restore the critical state variables associated with the CPU 205*.

Ex. 1005 at [0079] (emphasis added). As shown by the plain language, Petitioner has attempted to distort Jahagirdar’s process. Moreover, Petitioner does not contend that the “deassertion” of the “deep sleep (DPSLP#) signal” is the “restoration request signal,” nor could it because the deassertion of DPSLP# “initiates the PLLs of the clock/power management logic **350**” (which Petitioner argued was part of the “power supply control unit”) and not the CPU as required

by claim 1. *See* Petition at 32; *see* Ex. 1001 at 19:12-15. Also, “deeper stop (DPTSPT#)” first had to be deasserted from the zero voltage sleep state C6 (circle 440). Ex. 1005 at [0078], Figure 5.

Petitioner offers no evidence for how the “deassertion” of any signal can itself be a “signal.” Nor does its expert, Dr. Albonesi, when the cited paragraphs 194 through 199 of his declaration are a mere copy and paste of the Petition. *Compare* Petition at 47-49 with Ex. 1003 at ¶¶ 194-199; *see* 37 C.F.R § 42.65(a); *see also InfoBionic*, IPR2015-01704, Paper 11 slip op. at 14-15. Petitioner has not shown how the claimed “restoration request signal” is taught or suggested in Jahagirdar.

Petitioner has also not shown how the claimed “clock supply control signal” is taught in Jahagirdar because Petitioner points to no signal from the “power supply control unit” to the “clock generator.” Petitioner obscures Jahagirdar’s disclosure by arguing that “‘at a predetermined time (e.g., controller by timers)’ Jahagirdar generates a clock supply control signal to assert the clocks back on.” *See* Petition at 48 (citing Ex. 1005 at [0079]). But all that Jahagirdar discloses is that at that undisclosed predetermined time, “a signal to assert the clocks back on is asserted[.]” Ex. 1005 at [0079]. Neither Petitioner, nor Jahagirdar itself, explains what that “signal” is, where it comes from, or where it goes. Petitioner’s generic conclusion that “Jahagirdar generates a clock supply control signal to assert the

clocks back on” does not provide these critical requirements.

Petitioner also oddly argued that Jahagirdar teaches “de-asserting a deep sleep signal (i.e., a clock supply control signal) which powers and engages the clocks.” See Petition at 47. But Petitioner did not bother to justify or further explain this conclusion, so it does not appear Petitioner is actually relying on the “deassertion” of the deep sleep (DPSLP#) signal as the claimed “clock supply control signal.” It is also unclear why Petitioner shades circle 505 (deassert deep sleep) of Jahagirdar’s Figure 5 in red, since Jahagirdar states that, at a predetermined time, (1) “a signal to assert the clocks back on is asserted” and (2) “the *deep sleep (DPSLP#)* signal is de-asserted (circle **505**),” Ex. 1005 at [0079]. Circle 505 does depict the “signal to assert the clocks back on,” but rather the deassertion of the deep sleep (DPSLP#) signal. See *id.* Petitioner has not shown how the claimed “clock supply control signal” is taught or suggested in Jahagirdar.

Finally, Petitioner has not shown how both the “restoration request signal” and the “clock supply control signal” are output by the “power supply control unit” “*when a supplied power voltage is stabilized*” as required by claim 1. See Ex. 1001 at 19:12-15. Petitioner argues that “Jahagirdar’s use of the timer and the [analog-to-digital converter] ARC ensures that the power supply voltage is stabilized before the clocks are turned on.” Petition at 48. Petitioner also concludes that “it would have been obvious to wait for the power supply voltage to stabilize before

advancing from circle 502 to 505 in Figure 5. EX1003, ¶201 [*sic*]. And a POSITA would expect the clock restoration signal to be output before the CPU restoration signal because the CPU must wait until the clocks are restored.” *Id.* at 49. Again, Petitioners conclusions are not sufficiently supported by credible expert testimony.

Claim 1 requires that the power supply voltage be stabilized, but Jahagirdar does not explicitly mention that the power supply voltage is stabilized. Jahagirdar only describes a timer that is used to space the two events appearing at circles 502 and 505 of Figure 5. *See* Ex. 1005 at [0079]. Jahagirdar’s system 200 is a personal computer, and the clock generator is outside of the CPU in the chipset. *See id.* at [0025]; *see id.*, Figure 2A; *see also* Ex. 1024 at 3.3.21 – 3.3.21.1 (describing Intel Pentium III microprocessor’s “Clock Generation” as “CK113W devices on the baseboard generate and distribute the clocks used by the entire system” where “[t]he CK113W, clock synthesizer is the primary source of clock generation for most of the clocks on the baseboard.”). Petitioner does not offer any rationale for why Jahagirdar’s clock generator cannot start before the power supplied by the “power supply unit” to the CPU is stabilized. This is not the “articulated reasoning with some rational underpinning to support the legal conclusion of obviousness” that the Supreme Court requires. *KSR*, 550 U.S. at 418 (internal quotation mark omitted). Petitioner’s citation to the verbatim paragraphs in Dr. Albonesi’s declaration also does not meet this standard. *See* Ex. 1003 at ¶¶ 106-199, 201.

Petitioner has not demonstrated how this limitation is taught or suggested by Jahagirdar.

11. Limitation [1.N].

the clock generator, upon receiving the clock supply control signal, restarts to supply an operation clock, and

As was the case with respect to claim 1 limitation [1.M], limitation [1.N] also requires the “clock supply control signal.” Ex. 1001 at 19:16-17. Petitioner did not demonstrate how the “clock supply control signal” is taught or suggested in Jahagirdar, *see supra* V.A.10 (Limitation [1.M]), and does not offer any additional arguments or evidence with respect to this limitation. *See* Petition at 49. Jahagirdar thus does not teach or suggest that its “clock generator, *upon receiving the clock supply control signal*, restarts to supply an operation clock” as required by claim 1. *See* Ex. 1001 at 19:16-17.

12. Limitation [1.O].

the CPU, upon receiving the restoration request signal, executes a power supply restoration microprogram, restores the information necessary in proceeding with the program and evacuated in the information holding unit in time of power shutdown, and then branches a process to an address indicated by a program counter to continue program execution from a shutdown state.

Claim 1 requires that after the CPU receives the “restoration request signal,” the CPU (1) executes a “power supply restoration microprogram,” (2) “restores the information necessary in proceeding with the program and evacuated in the information holding unit in time of power shutdown,” and then (3) “branches a process to an address indicated by a program counter to continue program execution from a shutdown state.” Ex. 1001 at 19:18-24.

As an initial matter, this limitation [1.O] requires the “restoration request signal” described in limitation [1.M]. Ex. 1001 at 19:18. Petitioner has not shown how Jahagirdar teaches or suggests the claimed “restoration request signal” that is output from the claimed “power supply control unit” to the CPU. *See supra*, V.A.10 (Limitation [1.M]). Petitioner has not demonstrated how “the CPU, *upon receiving the restoration request signal*, executes a power supply restoration

microprogram, restores the information necessary in proceeding with the program and evacuated in the information holding unit in time of power shutdown, and then branches a process to an address indicated by a program counter to continue program execution from a shutdown.” Ex. 1001 at 19:18-24 (emphasis added).

Petitioner also does not explain how the remaining requisite elements of this limitation are rendered obvious over the asserted references.

Petitioner does not argue that a “microprogram” for restoring power supply is taught in the asserted references. *See* Petition at 49-52. A microprogram is a special program that runs at the lowest level of the hardware. *See, e.g.*, Ex. 2002 (Modern Dictionary of Electronics, 7th Ed. © 1999) (**microprogram**: “1. A computer program written in the most basic instructions or subcommands that can be executed by the computer.”; **microprogramming**: “1. The setting up of basic suboperations for a computer to handle, after which the programmer combines them, and they are presented to the computer again in a higher-level program.”). To clarify, a computer runs a program made up of instructions, also called macro-instructions. *See* Ex. 2003 (Microsoft Computer Dictionary 4th Ed. © 1999) (**program**: “A sequence of instructions that can be executed by a computer.... *Also called* software.”). These instructions are held in the main memory of the computer system until executed by the CPU. In many CPUs, these individual instructions are performed by executing a microprogram or microcode comprised of

microinstructions. The microcode is held entirely within the CPU. The microcode directs and coordinates the lowest-level hardware resources within the CPU to effect the specific semantics of the macro-level instructions. *See* Exs. 2002-2003 (definitions of microprogram and program).

Next, Petitioner argued that the phrase “restores the information necessary in proceeding with the program and evacuated in the information holding unit in time of power shutdown” should be construed to mean “restores from the information holding unit the information necessary to proceed with the program, the information was stored in the information holding unit during power shut down.” Petition at 21. But Petitioner does not apply its proposed construction, nor does it apply Collabo’s construction which it knows from the district court proceedings, in arguing that the limitation is met. Petitioner points to a disclosure in Jahagirdar that once “the states of the cores 320 and 322 are restored, CPU 205 is ready to continue from where it stopped.” *Id.* at 49-50 (citing Ex. 1005 at [0080]). Petitioner also argues that “Jahagirdar expressly states that the architectural state is saved.” Petition at 52. But that does not explain how the “information necessary in proceeding with the program and evacuated in the information holding unit in time of power shutdown” is restored. Pointing to Jahagirdar’s end result is not sufficient to demonstrate how it got there, when how it got there is claimed in the ’575

patent.⁸

13. Dependent Claims 2, 3, 5, 7, 11, 15, And 16.

Claims 2, 3, 5, 7, 11, 15, and 16 all depend from “the microcontroller according to claim 1[.]” *See* Ex. 1001 at 19:25-20:48. Since Petitioner has not demonstrated that claim 1 is rendered obvious over the combination of Jahagirdar and ACPI, *see supra* V.A.1-V.A.12, the Petition fails as to these claims that depend from claim 1.

B. The Combination Of Jahagirdar, ACPI, And Saito Does Not Render Claims 4, 17-22, 26, 30 Or 31 Of The ’575 Patent Obvious [Ground 2].

1. Limitations [17.Preamble], [17.C], [17.E], And [17.F].

Because claim 17 limitations [17.Preamble]-[17.F] “are identical to limitations [1.Preamble]-[1.D],[1.F]-[1.G],” Petitioner presents no additional arguments for claim 17 limitations [17.P] through [17.F]. Petition at 53-54. As such, Petitioner’s invalidity challenge regarding independent claim 17 limitations

⁸ Petitioner does not argue a motivation to combine Jahagirdar with ACPI for this element. Petitioner simply states that “Jahagirdar teaches or suggests claim elements [1.O].” Petition at 52. So, it is unclear Petitioner’s purpose in citing ACPI for this limitation. *See* Petition at 50-51 (“ACPI also discloses a process for restoring information necessary in proceeding with the program.”).

[17.Preamble] through [17.F] suffers from the same problems described above with respect to claim 1 limitations [1. Preamble], [1.C], [1.F], and [1.G]. *See supra*, V.A.1-V.A.4. Petitioner has not demonstrated how claim 17 limitations [17.Preamble] (“microcontroller”), [17.C] (“a power supply control unit for controlling the CPU and the power supply unit”), [17.E] (“the power supply control unit outputs a shutdown request signal to the CPU in response to an occurrence of a power shutdown factor”), and [17.F] (“the CPU, upon receiving the shutdown request signal, executes a power shutdown microprogram, evacuates the information necessary in proceeding with the program to the information holding unit, and outputs an evacuation completed signal to the power supply control unit after evacuation is completed”) are obvious over the combination of Jahagirdar and ACPI. *See id.*

2. Limitation [17.G].

the power supply control unit, upon receiving an occurrence of a power supply restoration factor after receiving the evacuation completed signal, outputs a restoration request signal to the CPU,

Independent claim 17 of the '575 patent requires that “the power supply control unit, upon receiving an occurrence of a power supply restoration factor after receiving the evacuation completed signal, outputs a restoration request signal to the CPU[.]” Ex. 1001 at 21:1-4.

As an initial matter, this limitation [17.G] requires the receipt of the “evacuation completed signal” described in limitations [17.F]/[1.G]. *See supra*, V.A.4 (Limitation [1.G]). Limitation [17.G] also requires that a “restoration request signal” be output from the “power supply control unit” to the CPU, as with the “restoration request signal” described in claim 1. *See supra*, V.A.10 (Limitation [1.M]). Petitioner relies on the same arguments it presented with respect to limitations [1.G] and [1.M]. Petition at 68. Petitioner’s arguments with respect to this limitation also fail because Petitioner has not shown how Jahagirdar teaches or suggests the claimed “evacuation completed signal” or the claimed “restoration request signal.” Petitioner has not demonstrated how the “*the power supply control unit*, upon receiving an occurrence of a power supply restoration factor *after receiving the evacuation completed signal*, outputs a restoration request signal to the CPU” Ex. 1001 at 21:1-4 (emphasis added).

Next, Petitioner appears to be attempting to prove obviousness by inherency with respect to this limitation’s requirement that the “restoration request signal” be output from the “power supply control unit” after it receives “an occurrence of a power supply restoration factor after receiving the evacuation completed signal[.]” *See* Petition at 68 (citing Ex. 1003 at ¶ 256) (“A POSITA would have understood that Jahagirdar’s evacuation complete signal would have been received before receiving an occurrence of the power supply restoration factor.”). If that is the

case, Petitioner has failed to meet the “high standard” of proving obviousness by inherency.

“[T]he use of inherency, a doctrine originally rooted in anticipation, must be carefully circumscribed in the context of obviousness.” *Par Pharm., Inc. v. TWi Pharm., Inc.*, 773 F.3d 1186, 1195 (Fed. Cir. 2014). “The mere fact that a certain thing *may* result from a given set of circumstances is not sufficient [to establish inherency]. [M]ere recitation of a newly discovered function or property, inherently possessed by things in the prior art, does not distinguish a claim drawn to those things from the prior art.” *Id.* (internal citations and quotation marks omitted). “A party must, therefore, meet a high standard in order to rely on inherency to establish the existence of a claim limitation in the prior art in an obviousness analysis—the limitation at issue necessarily must be present, or the natural result of the combination of elements explicitly disclosed by the prior art. *Id.* at 1195-96.

The only evidence cited in support of Petitioner’s argument that “[a] POSITA would have understood that Jahagirdar’s evacuation complete signal would have been received before receiving an occurrence of the power supply restoration factor” is paragraph 256 of the declaration of its expert, Dr. Albonesi. However, paragraph 256 is merely a verbatim repetition of the petition. *Compare* Petition at 68 *with* Ex. 1003 at ¶ 359; 37 C.F.R. § 42.65(a); *InfoBionic*, IPR2015-

01704, Paper 11 slip op. at 14-15. Neither Petitioner nor its expert Dr. Albonesi offers anything more. This is insufficient to prove obviousness by inherency.

3. Limitation [17.H].

the CPU, upon receiving the restoration request signal, executes a power supply restoration microprogram which does not restore the evacuated information, and continues program execution, and

Claim 17 of the '575 patent requires that after the CPU receives the “restoration request signal,” the CPU executes a “power supply restoration microprogram which does not restore the evacuated information, and continues program execution[.]” Ex. 1001 at 21: 5-8. Petitioner does not explain how all of the requisite elements of this limitation are rendered obvious over the asserted references.

First, this limitation [17.H] requires the “restoration request signal” that was output from the “power supply control unit” to the CPU that was described in limitation [17.G] (and also in claim 1 limitation [1.M]). As was the case with respect to those limitations, Petitioner did not show how Jahagirdar teaches or suggests the claimed “restoration request signal.” *See supra*, V.A.10 (Limitation [1.M], V.B.2 (Limitation [17.G])). Petitioner’s bare conclusion that “Jahagirdar discloses a power supply restoration microprogram that is executed upon receiving

a restoration request signal” is not supported. *See* Petition at 69. Petitioner has not demonstrated how the “the CPU, *upon receiving the restoration request signal*, executes a power supply restoration microprogram which does not restore the evacuated information, and continues program execution[.]” Ex. 1001 at 21:5-8 (emphasis added).

Second, Petitioner does not explain how the claimed “power supply restoration microprogram which does not restore the evacuated information” is taught. *See supra*, V.A.12 (definitions of “microprogram”). Jahagirdar does not teach that its system 200 is capable of restoring power to the CPU where the CPU state is not restored. *See* Ex. 1005 at [0077-0080] (repeatedly discussing the “state restore” of the CPU cores). Instead, Petitioner concludes that “if an interrupt [in Jahagirdar] occurred during any of states C1-C3, the evacuated information necessary in proceeding with the program would still be stored at the CPU and therefore would not need to be restored.” *See* Petition at 69. The only way Petitioner can reach this assumption is by pointing to teachings from ACPI, *see id.* at 69-70, but Petitioner presents *no argument* for a motivation to combine said teachings from ACPI into Jahagirdar for this purpose. Petitioner simply refers to a discussion related to the ’575 patent’s dependent claim 7, *see* Petition at 70, where Petitioner argued that “[i]t would have been obvious for a POSITA to enhance the C-states of Jahagirdar and ACPI, with the power-on reset of ACPI’s S-states.” *Id.*

at 60. But Petitioner has not pointed to any need for “enhancement” in Jahagirdar. Petitioner’s motivation to combine argument that uses the ’575 patent as a roadmap is the result of classic hindsight. “[A] conclusory assertion with no explanation is inadequate to support a finding that there would have been a motivation to combine because this type of finding, without more, tracks the *ex post* reasoning” the Supreme Court has “warned of and fails to identify any actual *reason* why a skilled artisan would have combined the elements in the manner claimed.” *TQ Delta*, 942 F.3d at 1359 (citation omitted); *see also id.* at 1361 (collecting cases).

Petitioner has not met its burden of demonstrating that the claimed “power supply restoration microprogram” of claim limitation [17.H] is taught or suggested by the combination of Jahagirdar and ACPI.

4. Limitation [17.I] / Dependent Claim 4.

the power shutdown microprogram evacuates the information necessary in proceeding with the program to a stack region in the information holding unit, and then evacuates to a specific place only a value of a stack pointer for pointing to an evacuation place.

Independent claim 17 of the ’575 patent (as well as the substantially identical dependent claim 4 that depends from the microcontroller according to

claim 1), requires that the “power shutdown microprogram” first described in limitation [17.F] (as well as in claim 1 limitation [1.G]) “evacuates the information necessary in proceeding with the program to a *stack region in the information holding unit*, and then evacuates to a *specific place only a value of a stack pointer for pointing to an evacuation place*.” Ex. 1001 at 21:9-13 (emphasis added).

This is the only element at issue where Petitioner’s asserts a combination of Jahagirdar and ACPI with the Saito reference. See Petition at 67-68. At this juncture, it is not necessary to discuss the Petition’s failures with respect to the proposed combination with Jahagirdar, ACPI, and Saito for this element because Petitioner has not shown how independent claim 17 is obvious. See *supra*, V.B.1-V.B.3. Additionally, Dependent claim 4 is not taught or suggested over the asserted references because it depends from “[t]he microcontroller according to claim 1,” and Petitioner has not shown how claim 1 is obvious. Ex. 1001 at 19:34; see *supra*, V.A.1-V.A.12.

5. Dependent Claims 18, 19, 20, 21, 22, 26, 30 And 31.

Claims 18, 19, 20, 21, 22, 26, 30, and 31 all depend from “the microcontroller according to claim 17[.]” See Ex. 1001 at 21:14-22:47. Since Petitioner has not demonstrated that claim 17 are rendered obvious over the combination of Jahagirdar, ACPI, and Saito, see *supra* V.B.1-V.B.3, the Petition fails as to these claims that depend from claim 17.

C. The Combination Of Jahagirdar, ACPI, And Chung Does Not Render Claim 12 Of The '575 Patent Obvious [Ground 3].

Ground 3 of the Petition, where only dependent claim 12 is at issue, asserts a combination of Jahagirdar, ACPI, and the Chung references. *See* Petition at 73-75. Claim 12 depends from “the microcontroller according to claim 1[.]” Ex. 1001 at 20:16-18. At this juncture, it is not necessary to discuss the Petition’s failures with respect to the proposed combination with Jahagirdar, ACPI, and Chung for dependent claim 12 because Petitioner has not shown how independent claim 1 is obvious. *See supra*, V.A.1-V.A.12.

D. The Combination Of Jahagirdar, ACPI, Saito, And Chung Does Not Render Claim 27 Of The '575 Patent Obvious [Ground 4].

Ground 4 of the Petition, where only dependent claim 27 is at issue, asserts a combination of Jahagirdar, ACPI, Saito, and the Chung references. *See* Petition at 75. Claim 27 is “substantially identical to claim 12,” *see id.*, but depends from “the microcontroller according to claim 17[.]” Ex. 1001 at 22:16-18. At this juncture, it is not necessary to discuss the Petition’s failures with respect to the proposed combination with Jahagirdar, ACPI, Saito, and Chung for dependent claim 27 because Petitioner has not shown how independent claim 17 is obvious. *See supra*, V.B.1-V.B.3.

VI. THE BOARD LACKS AUTHORITY TO RULE ON THE PATENTABILITY OF THE CHALLENGED CLAIMS OF THE '575 PATENT.

The Board should not institute trial because Administrative Patent Judges (APJs) are unconstitutionally appointed. *See Lucia v. SEC*, 138 S. Ct. 2044, 2049 (2018); *Masias v. Sec'y of HHS*, 634 F.3d 1283, 1294–95 (Fed. Cir. 2011); *Free Enter. Fund v. Pub. Co. Accounting Oversight Bd.*, 561 U.S. 477, 489, 496-498 (2010); *Edmond v. United States*, 520 U.S. 651, 662–65 (1997); *Freytag v. Commissioner*, 501 U.S. 868, 873 (1991); *see also Arthrex, Inc. v. Smith & Nephew, Inc.*, 941 F.3d 1320, 1325 (Fed. Cir. 2019).

APJs have the power to revoke patent rights, but there is no review of their decisions by constitutionally appointed principal officers. The Federal Circuit, in *Arthrex*, attempted to cure this constitutional defect by severing a provision of the Patent Act that applied Title 5's removal protections to APJs. *Arthrex*, 941 F.3d at 1325. Supreme Court and Federal Circuit precedent, however, demonstrates that the solution advanced in *Arthrex* is insufficient because it does not give a constitutionally appointed principal officer the power to review APJ decisions. *See, e.g., Lucia*, 138 S. Ct. at 2049; *Masias*, 634 F.3d at 1294–95; *Free Enter.*, 561 U.S. at 489, 496-498; *Edmond*, 520 U.S. at 662–65; *Freytag*, 501 U.S. at 873. Thus, APJs remain unconstitutionally appointed.

Congress has the power to remedy the constitutional defect, not the courts. Congress could give a constitutionally appointed principal officer the power to review APJ decisions or require that APJs be appointed by the President, with the advice and consent of the Senate. *See Arthrex*, 941 F.3d at 1327. Regardless of the path forward chosen by the legislative branch, *inter partes* review remains unconstitutional. The petition must be dismissed.

VII. CONCLUSION.

For the foregoing reasons, the Petition should be denied.

Date: January 3, 2020

/Jing H. Cherng/

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