

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

ADVANCED MICRO DEVICES, INC.,
Petitioner,

v.

COLLABO INNOVATIONS, INC.,
Patent Owner.

IPR2019-01523
Patent 7,930,575 B2

Before DAVID C. McKONE, GREGG I. ANDERSON, and
GARTH D. BAER, *Administrative Patent Judges*.

BAER, *Administrative Patent Judge*.

DECISION
Denying Institution of *Inter Partes* Review
35 U.S.C. § 314

I. INTRODUCTION

Advanced Micro Devices, Inc. (“Petitioner”) filed a Petition to institute an *inter partes* review of claims 1–7, 11, 12, 15–22, 26, 27, 30, and 31 of U.S. Patent No. 7,930,575 B2 (Ex. 1001, the “’575 patent”) pursuant to 35 U.S.C. § 311 *et seq.* Paper 2 (“Pet.”). Collabo Innovations, Inc. (“Patent Owner”) filed a Preliminary Response to the Petition. Paper 9 (“Prelim. Resp.”). Petitioner then filed a Reply to Patent Owner’s Preliminary Response, addressing whether Exhibit 1006, one of the asserted prior-art references, is a printed publication. Paper 14, 1. Petitioner also filed a Motion to Expunge and Replace Exhibit 1016, which is an affidavit relating to Exhibit 1006’s status as a printed publication. Paper 15, 1. Patent Owner filed a Sur-Reply (Paper 16) and an Opposition to Petitioner’s Motion to Expunge and Replace Exhibit 1016 (Paper 17).

We have authority under 35 U.S.C. § 314, which provides that an *inter partes* review may not be instituted unless the information presented in the Petition and the Preliminary Response shows that “there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition.” 35 U.S.C. § 314(a) (2018); *see also* 37 C.F.R. § 42.4(a) (2019) (“The Board institutes the trial on behalf of the Director.”). For the reasons that follow, we do not institute an *inter partes* review as to the challenged claims of the ’575 patent on the grounds of unpatentability presented. Because we do not institute an *inter partes* review, we dismiss Petitioner’s Motion to Expunge and Replace Exhibit 1016 as moot.

A. Related Matters

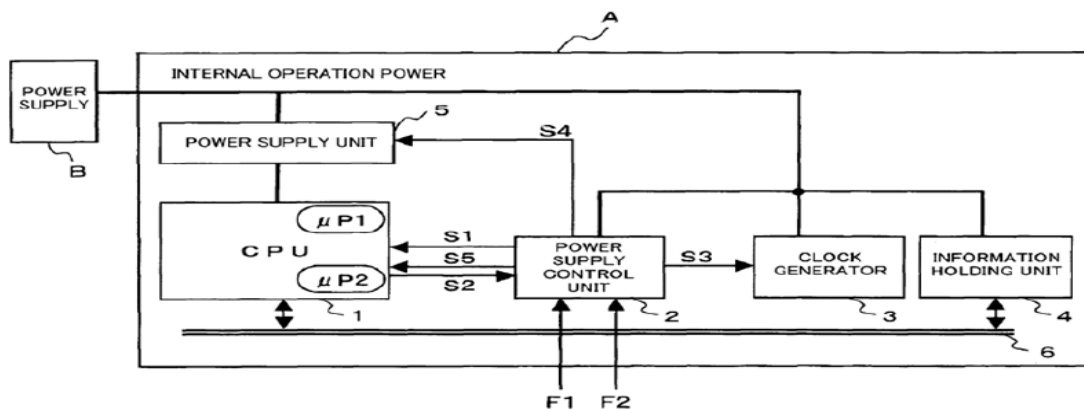
The parties indicate that the '575 patent has been asserted in *Collabo Innovations, Inc. v. Advanced Micro Devices, Inc.*, Case No. 1:18-cv-00552-LY (W.D. TX.). Pet. 3; Paper 5, 2. The '575 patent is also the subject of co-pending IPR2019-01524.¹

B. The '575 Patent

The '575 patent is titled “Microcontroller for Controlling Power Shutdown Process.” Ex. 1001, code (54). The invention’s object is “to provide a microcontroller capable of easily and rapidly evacuating and restoring information necessary in proceeding with a program when realizing a standby state in which internal operation voltage supply is shutdown, a state in which an internal operation voltage is lowered, or the like.” *Id.* at 2:26–31.

Figure 1 of the '575 patent is reproduced below.

FIG. 1



¹ Patent Owner requests that we exercise our discretion to deny institution under 35 U.S.C. 314(a) because Petitioner challenged many of the same claims based on different prior art in IPR2019-01524. Prelim. Resp. 9–12. Because we determine that the merits of the Petition in this case do not support institution, we do not reach Patent Owner’s arguments that we should exercise our discretion under § 314(a) to deny institution in this case.

Figure 1 “is a block diagram showing a configuration of a microcontroller according to a first embodiment of the present invention.” *Id.* at 7:22–24.

According to the ’575 patent,

The microcontroller A includes a CPU 1, a power supply control unit 2, a clock generator 3, an information holding unit (built-in RAM) 4, a power supply unit 5, an internal bus 6, and peripheral circuits (not shown) such as a timer circuit and serial interface. Power is externally supplied to the microcontroller A. The power supply unit 5 is arranged between the power supply B and the CPU 1, and has a function of performing a control so that the voltage to be supplied to the CPU 1 is constant and a function of controlling supply/shutdown of power to the CPU 1 in response to a power supply/power shutdown control signal S4 from the power supply control unit 2. The power supply control unit 5 is configured by a general voltage regulator. The clock generator 3 supplies or stops an operation clock in response to a clock supply/clock stop control signal S3 from the power supply unit 2.

Id. at 8:39–54.

C. Challenged Claims

Petitioner challenges claims 1–7, 11, 12, 15–22, 26, 27, 30, and 31 of the ’575 patent. Pet. 1. Of the challenged claims, claims 1 and 17 are independent. Claim 1 is illustrative and recites:

1. A microcontroller comprising:
 - a CPU;
 - a power supply unit arranged between the CPU and a power supply device for supplying power to the CPU;
 - a power supply control unit for controlling the CPU and the power supply unit;
 - an information holding unit for holding information evacuated from the CPU, the information being necessary in proceeding with a program; and

a clock generator; wherein:

the power supply control unit outputs a shutdown request signal to the CPU in response to an occurrence of a power shutdown factor,

the CPU, upon receiving the shutdown request signal, executes a power shutdown microprogram, evacuates the information necessary in proceeding with the program to the information holding unit, and outputs an evacuation completed signal to the power supply control unit after evacuation is completed,

the power supply control unit, upon receiving the evacuation completed signal, outputs a power shutdown control signal to the power supply unit,

the power supply unit shuts down power supply to the CPU upon receiving the power shutdown control signal from the power supply control unit,

the power supply control unit, upon receiving the evacuation completed signal, outputs a clock stop control signal to the clock generator,

the power supply control unit outputs a power supply control signal to the power supply unit in response to an occurrence of a power supply restoration factor,

the power supply unit, upon receiving the power supply control signal, starts to supply power to the CPU,

the power supply control unit outputs a restoration request signal to the CPU and outputs a clock supply control signal to the clock generator when a supplied power supply voltage is stabilized,

the clock generator, upon receiving the clock supply control signal, restarts to supply an operation clock, and

the CPU, upon receiving the restoration request signal, executes a power supply restoration microprogram, restores the information necessary in proceeding with the program and evacuated in the information holding unit in time of power shutdown, and then branches a process to an address

indicated by a program counter to continue program execution from a shutdown state.

Ex. 1001, 18:45–19:24.

D. Asserted Grounds of Unpatentability

Petitioner asserts the following grounds of unpatentability. Pet. 5.

Challenged Claim(s)	35 U.S.C. §	References/Basis
1–3, 5–7, 11, 15, 16	103 ²	Jahagirdar ³ , ACPI ⁴
4, 17–22, 26, 30, 31	103	Jahagirdar, ACPI, Saito ⁵
12	103	Jahagirdar, ACPI, Chung ⁶
27	103	Jahagirdar, ACPI, Saito, Chung

II. ANALYSIS

A. Claim Construction

“In an *inter partes* review proceeding, a claim of a patent . . . shall be construed using the same claim construction standard that would be used to construe the claim in a civil action under 35 U.S.C. § 282(b), including

² The Leahy-Smith America Invents Act (“AIA”) amended 35 U.S.C. § 103. *See* Pub. L. No. 112-29, 125 Stat. 284, 285–88 (2011). As the application that issued as the ’575 patent was filed before the effective date of the relevant amendments, the pre-AIA version of § 102 applies.

³ U.S. Pub. No. 2007/0157036, filed Dec. 30, 2005, Published July 5, 2007 (Ex. 1005, “Jahagirdar”).

⁴ Compaq Computer Corp., Intel Corp., Microsoft Corp., Phoenix Techs. Ltd., Toshiba Corp., *Advanced Configuration and Power Interface Specification*, Revision 2.0 (1999) (Ex. 1006, “ACPI”).

⁵ Japanese Pat. Appl. No. S58-169218, published October 5, 1983 (certified English translation) (Ex. 1010, “Saito”).

⁶ U.S. Patent No. 5,390,350, Feb. 14, 1995 (Ex. 1007, “Chung”).

construing the claim in accordance with the ordinary and customary meaning of such claim as understood by one of ordinary skill in the art and the prosecution history pertaining to the patent.” 37 C.F.R. § 42.100(b). In applying a district court-type claim construction, we are guided by the principle that the words of a claim “are generally given their ordinary and customary meaning,” as understood by a person of ordinary skill in the art at the time of the invention. *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312–13 (Fed. Cir. 2005) (en banc) (citation omitted).

Microcontroller

The preambles of claims 1 and 17 recite a “microcontroller.” The parties agree that the preambles are limiting, but disagree over the construction. *See* Pet. 27 n.10; Prelim. Resp. 18. Petitioner asserts we should construe “microcontroller” as “a chip designed for control applications rather than data-processing that has a complete CPU, semiconductor memory sufficient for control applications, and input/output capability.” Pet. 14. Patent Owner notes that its proffered construction for “microcontroller” in the related district court case is “an integrated circuit.” Prelim. Resp. 18. However, Patent Owner explains, for purposes of this Decision, we need not choose between the parties’ constructions because “[r]egardless of which construction is used in this proceeding, both constructions require the microcontroller to be on a single integrated chip.” *Id.* (citing Ex. 2001 (Authoritative Dictionary of IEEE Standard Terms listing “integrated circuit” as a synonym for “chip”)).

We agree with Patent Owner that, as both parties’ constructions reflect, a microcontroller must be a single, integrated chip. *Id.*; *see* Pet. 14 (asserting that a “microcontroller” is “*a chip* designed for control

applications . . .”) (emphasis added). Our construction is consistent with the term’s ordinary meaning. *See, e.g.*, <https://www.merriam-webster.com/dictionary/microcontroller> (defining “microcontroller” as an “*integrated circuit* that contains a microprocessor along with memory and associated circuits . . .”) (emphasis added). We decline to construe “microprocessor” beyond requiring a single, integrated chip because that construction is enough to determine whether to institute an *inter partes* review. *See, e.g., Wellman, Inc. v. Eastman Chem. Co.*, 642 F.3d 1355, 1361 (Fed. Cir. 2011) (“[C]laim terms need only be construed ‘to the extent necessary to resolve the controversy.’”) (*quoting Vivid Techs., Inc. v. Am. Sci. & Eng’g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999)). We likewise decline to construe the parties’ additional asserted claim terms, *see* Prelim. Resp. 5–8; Pet. 13–24, because no additional claim construction is necessary to determine whether to institute an *inter partes* review.

B. Petitioner Fails to Show Obviousness for Any Challenged Claim

Our decision not to institute is based on our conclusion that Jahagirdar does not disclose a “microcontroller” as recited in the preamble of independent claims 1 and 17. Because Petitioner does not show Jahagirdar teaches this required element, or argue that such a feature is shown in any other reference, Petitioner has not established a reasonable likelihood of prevailing as to any challenged claim.

1. Jahagirdar

Jahagirdar is titled “Method and Apparatus for a Zero Voltage Processor Sleep State.” Ex. 1005, code (54). According to Jahagirdar, during a transition to the disclosed zero voltage power management state, the “operational voltage applied to the processor by the voltage regulator

may be reduced to approximately zero and the state variables associated with the processor may be saved to the dedicated cache memory.” *Id.* at code (57). Upon waking and restoring power to Jahagirdar’s CPU, the system can continue where the CPU left off. *Id.* at ¶ 54.

Jahagirdar’s Figures 2A and 2B are reproduced below.

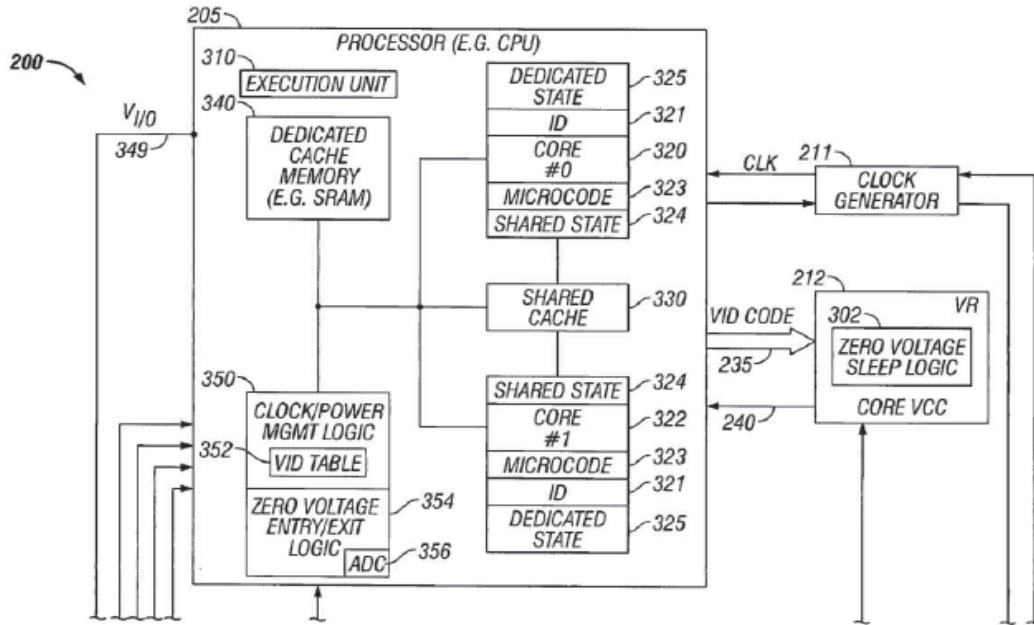


FIG. 2A

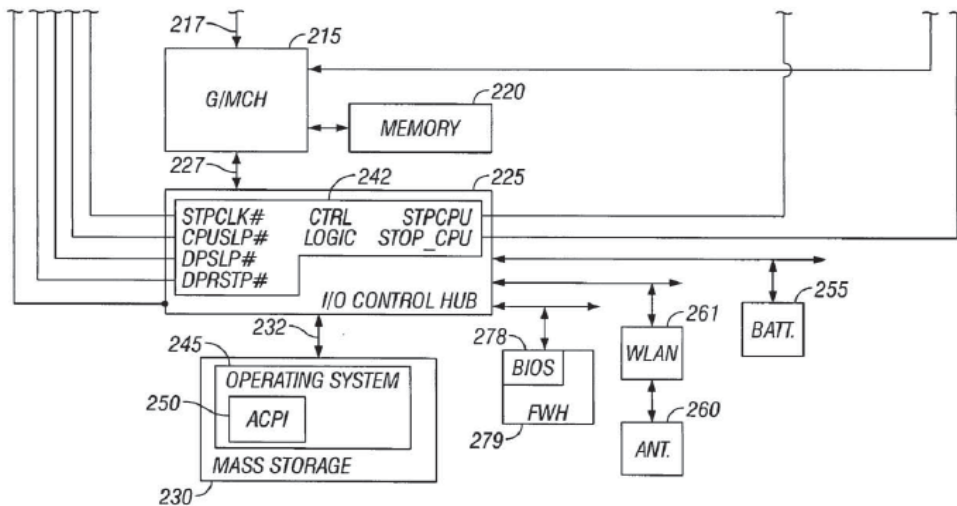


FIG. 2B

Jahagirdar states as follows:

FIG 2 is a block diagram of an exemplary system 200 that may implement the zero voltage power management state transition approach of one or more embodiments. It should be noted that FIG 2 is divided into 2A and 2B. The system 200 may be a notebook or laptop computer system, or may be any different type of mobile electronic system

Ex. 1005 ¶ 24.

2. *ACPI*

Petitioner relies on ACPI for teaching implementation details related to transitioning processors into sleeping states that consume less power. *See* Pet. 26–27 (citing Ex. 1006 ¶¶ 37, 225, 228, 229).

3. *The Asserted Prior Art Does Not Teach or Suggest the Claimed Microcontroller*

The preamble for claims 1 and 17 recites “[a] microcontroller comprising” The parties agree that the preamble is limiting. Pet. 27 n.10; Prelim. Resp. 17. Petitioner relies solely on Jahagirdar for the claimed microcontroller. *See* Pet. 27–28. According to Petitioner, “Jahagirdar’s system 200” is a microcontroller. *See id.* at 27. Petitioner further asserts that Jahagirdar discloses “a processor 205 (i.e., CPU), a memory 220 which may comprise one or more of random access memory (RAM), flash memory and/or another type of memory (i.e., semiconductor memory), and an input/output (I/O) control hub 225 (i.e., input/output capability).” *Id.* at 27–28. According to Petitioner, because Jahagirdar teaches that “various embodiments may be applied to different types of power management configurations and/or for different types of integrated circuits,” *id.* at 28 (quoting Ex. 1005 ¶ 102), these components “can be located on the same chip.” *Id.*

We agree with Patent Owner that Petitioner has not shown sufficiently that Jahagirdar's system resides on a single chip, as Petitioner's claim construction requires. *See* Prelim Resp. 17–26. Specifically, as Patent Owner explains, Jahagirdar's "system 200" is not a single-chip microcontroller, but rather a "system" with multiple separate components. Ex. 1005 ¶ 25; *see id.* ¶ 24 ("The system 200 may be a notebook or laptop computer system, or may be any different type of mobile electronic system such as a mobile device, personal digital assistant, wireless telephone/handset or may even be a non-mobile system such as a desktop or enterprise computing system."); *id.* ¶ 40 ("[I]t should be appreciated that system 200 may include a display device, such as a cathode ray tube (CRT) or liquid crystal display (LCD), for displaying information to a user. Further, system 200 may include an alphanumeric input device (e.g., a keyboard), including alphanumeric and other keys, for communicating information and command selections to processor 205.").

In addition, the record evidence does not show sufficiently that Jahagirdar teaches its components "can be located on the same chip," as Petitioner asserts. Pet. 28. Jahagirdar's teaching that "various embodiments *may be applied* to different types of power management configurations and/or for different types of integrated circuits," Ex. 1005 ¶ 102 (emphasis added), does not establish that Jahagirdar's system might be a single-chip system. Testimony from Petitioner's expert, Dr. Albonesi, merely repeats Petitioner's conclusory argument. *See* Ex. 1003 ¶ 147. For the reasons noted above, Dr. Albonesi's conclusory statement does not persuade us Petitioner has met its burden to show Jahagirdar teaches or suggests a single-chip system. *See* 37 C.F.R. § 42.65(a) ("Expert testimony that does not

disclose the underlying facts or data on which the opinion is based is entitled to little or no weight.”).

Last, Petitioner argues that “Jahagirdar teaches that the processor could be an embedded processor, which is synonymous with a microcontroller.” Pet. 28 (citing Ex. 1005 ¶ 27). Jahagirdar’s disclosure related to its *processor* 205 is not relevant, however, because Petitioner relies on Jahagirdar’s system 200—not its processor 205—as the claimed “microcontroller.” See Pet. 29–39. Petitioner does not argue, for example, that Jahagirdar’s processor 205 contains a power supply unit, a power supply control unit, and a clock generator, which it would have to for it to be the microprocessor recited in claim 1. See *id.*

Based on the current record, we are not persuaded that Petitioner has shown Jahagirdar teaches or suggests the “microprocessor” recited in claims 1 and 17. Absent such a disclosure, Petitioner has not explained why it would have been obvious to one skilled in the art to implement the asserted prior-art teachings as a single-chip system. Petitioner also does not contend that any other reference teaches the single chip requirement of its microcontroller construction.

C. Conclusion

For the foregoing reasons, we conclude that Petitioner has not demonstrated a reasonable likelihood of prevailing with respect to any of the claims challenged in the Petition. Given our decision not to institute an *inter partes* review based on Jahagirdar’s deficiency, Petitioner’s Motion to Expunge and Replace Exhibit 1016, which is an affidavit relating to Exhibit 1006’s status as a printed publication, is moot.

III. ORDER

In consideration of the foregoing, it is hereby:

ORDERED that, pursuant to 35 U.S.C. § 314(a), no *inter partes* review as to any claim of US Patent No. 7,930,575 B2 is instituted; and

ORDERED that Petitioner's Motion to Expunge and Replace Exhibit 1016 (Paper 15) is dismissed as moot.

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