

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

ADVANCED MICRO DEVICES, INC.

Petitioner

v.

COLLABO INNOVATIONS, INC.

Patent Owner

Case IPR2019-01524
Patent 7,930,575 B2

PATENT OWNER'S PRELIMINARY RESPONSE

TABLE OF CONTENTS

	Page
I. THE MICROCONTROLLER OF THE '575 PATENT	1
A. The Claims Of The '575 Patent.....	2
B. Claim Construction	5
II. THE ALLEGED BASES OF INVALIDITY	8
III. THE BOARD SHOULD EXERCISE ITS DISCRETION TO DENY INSTITUTION OF THIS REDUNDANT PETITION	8
IV. THE COMBINATION OF CHUNG AND CRUMP DOES NOT RENDER ANY CLAIM OF THE '575 PATENT OBVIOUS	13
1. Limitation [1.Preamble].....	14
2. Limitation [1.F].....	20
3. Limitation [1.G]	27
4. Limitation [1.H]	30
5. Limitation [1.I].....	34
6. Limitation [1.J].....	35
7. Limitation [1.K]	37
8. Limitation [1.L].....	40
9. Limitation [1.M].....	41
10. Limitation [1.N]	44
11. Limitation [1.O]	45
12. Limitations [17.Preamble], [17.E], And [17.F]	48
13. Limitation [17.G]	49

TABLE OF CONTENTS
(continued)

	Page
14. Limitation [17.H]	52
15. Limitation [17.I] / Dependent Claim 4	54
16. Dependent Claims 5, 7, 12, 15, 16, 20, 22, 27, 30, And 31.....	57
V. THE BOARD LACKS AUTHORITY TO RULE ON THE PATENTABILITY OF THE CHALLENGED CLAIMS OF THE '575 PATENT.....	57
VI. CONCLUSION.....	59

TABLE OF AUTHORITIES

	Page(s)
Cases	
<i>ActiveVideo Networks, Inc. v. Verizon Communs., Inc.</i> , 694 F.3d 1312 (Fed. Cir. 2012)	24
<i>Apotex Inc. v. Wyeth LLC</i> , IPR2014-00115, Paper 94 (PTAB Apr. 20, 2015).....	21
<i>Arthrex, Inc. v. Smith & Nephew, Inc.</i> , 941 F.3d 1320 (Fed. Cir. 2019)	57, 58
<i>Belden Inc. v. Berk-Tek LLC</i> , 805 F.3d 1064 (Fed. Cir. 2015)	14
<i>Cuozzo Speed Techs., LLC v. Lee</i> , 136 S. Ct. 2131 (2016).....	9
<i>Edmond v. United States</i> , 520 U.S. 651 (1997).....	57, 58
<i>Free Enter. Fund v. Pub. Co. Accounting Oversight Bd.</i> , 561 U.S. 477 (2010).....	57, 58
<i>Freytag v. Commissioner</i> , 501 U.S. 868 (1991).....	57, 58
<i>Harmonic Inc. v. Avid Tech., Inc.</i> , 815 F.3d 1356 (Fed. Cir. 2016)	1
<i>Hologic v. Enzo</i> , 2018 Pat. App. LEXIS 5855 (PTAB April 18, 2018).....	6
<i>InfoBionic, Inc. v. Braemer Manufacturing, LLC</i> , IPR2015-01704, Paper 11 (PTAB Feb. 16, 2016).....	<i>passim</i>
<i>KSR Int’l Co. v. Teleflex Inc.</i> , 550 U.S. 398 (2007).....	<i>passim</i>
<i>Lucia v. SEC</i> , 138 S. Ct. 2044 (2018).....	57, 58

<i>In re Magnum Oil Tools Int’l, Ltd.</i> , 829 F.3d 1364 (Fed. Cir. 2016)	1
<i>Masias v. Sec’y of HHS</i> , 634 F.3d 1283 (Fed. Cir. 2011)	57, 58
<i>Par Pharm., Inc. v. TWi Pharm., Inc.</i> , 773 F.3d 1186 (Fed. Cir. 2014)	50, 51
<i>PersonalWeb Techs., LLC v. Apple, Inc.</i> , 848 F.3d 987 (Fed. Cir. 2017)	24, 56
<i>Stryker Corp. v. Karl Storz Endoscopy America, Inc.</i> , IPR2015-00764, Paper 13 (Sept. 2, 2015)	56
<i>TQ Delta, LLC v. Cisco Sys.</i> , 942 F.3d 1352 (Fed. Cir. 2019)	26, 39, 48, 53
<i>Wellman, Inc. v. Eastman Chem. Co.</i> , 642 F.3d 1355 (Fed. Cir. 2011)	7, 16

Statutes

35 U.S.C. § 282(b)	6
35 U.S.C. § 312(a)(3)	1
35 U.S.C. § 313	1
35 U.S.C. § 314(a)	9, 11
35 U.S.C. § 316(b)	9

Other Authorities

37 C.F.R. § 42.65(a)	<i>passim</i>
37 C.F.R. § 42.100(b)	6
37 C.F.R. § 42.104(b)	19
37 C.F.R. § 42.107	1

PATENT OWNER'S EXHIBIT LIST

Exhibit No.	Description
2001	Excerpts from The Authoritative Dictionary of IEEE Standard Terms, 7th Ed. © 2000
2002	Excerpts from Modern Dictionary of Electronics, 7th Ed. © 1999
2003	Excerpts from Microsoft Computer Dictionary, 4th Ed. © 1999
2004	Excerpts from Comprehensive Dictionary of Electrical Engineering, 2nd Ed. © 2005

Pursuant to 35 U.S.C. § 313, 37 C.F.R. § 42.107 and the Notice of Filing Date Accorded to Petition, Paper No. 4, Patent Owner Collabo Innovations, Inc. (“Collabo”) timely submits this preliminary response to Petitioner Advanced Micro Devices, Inc.’s (“Petitioner”) petition for *inter partes* review (the “Petition”) of U.S. Patent No. 7,930,575 (the “’575 patent”).

“In an IPR, the petitioner has the burden from the onset to show with particularity why the patent it challenges is unpatentable.” *Harmonic Inc. v. Avid Tech., Inc.*, 815 F.3d 1356, 1363 (Fed. Cir. 2016); 35 U.S.C. § 312(a)(3) (requiring IPR petitions to identify “with particularity . . . the evidence that supports the grounds for the challenge to each claim”). “[T]hat burden never shifts to the patentee.” *In re Magnum Oil Tools Int’l, Ltd.*, 829 F.3d 1364, 1375 (Fed. Cir. 2016) (citation omitted).

This is one of two petitions for *inter partes* review filed by Petitioner on the same day regarding certain claims of the ’575 patent. Petitioner has not met its burden in showing any of the challenged claims of the ’575 patent obvious in light of the alleged prior art. For the reasons stated herein, the Petition should be denied.

I. THE MICROCONTROLLER OF THE ’575 PATENT.

The ’575 patent, entitled “Microcontroller for Controlling Power Shutdown Process,” discloses various embodiments of an inventive microcontroller that is capable of preserving the state of a Central Processing Unit (“CPU”) when the

CPU goes into standby, or sleep, or another low-power state. Ex. 1001 at 2:26-31.

In contrast to the technology that existed prior to the '575 patent, the main object of the invention of the '575 patent is in providing a “microcontroller capable of easily and rapidly evacuating and restoring information necessary in proceeding with a program when realizing a standby state in which internal operation voltage is lowered, or the like.” *Id.* The '575 patent does this through the specific requirements of the microcontroller as detailed in the specification and claims.

A. The Claims Of The '575 Patent.

Independent claims 1 and 17 of the '575 patent describe the required elements of the claimed microcontroller.

Claim 1 begins by listing the physical requirements of the microcontroller.

What is claimed is

[1.Preamble] A microcontroller comprising:

[1.A] a CPU;

[1.B] a power supply unit arranged between the CPU and
a power supply device for supplying power to the
CPU;

[1.C] a power supply control unit for controlling the CPU
and the power supply unit;

[1.D] an information holding unit for holding information
evacuated from the CPU, the information being
necessary in proceeding with a program; and

[1.E] a clock generator; wherein:

Ex. 1001 at 18:45-55.

Claim 1 recites limitations directed at the process undertaken by the components of the claimed microcontroller. *See id.* at 18:56-19:24. Included within that process are seven distinct signals:

- (a) Shutdown request signal
- (b) Evacuation completed signal
- (c) Power shutdown control signal
- (d) Clock stop control signal
- (e) Power supply control signal
- (f) Restoration request signal
- (g) Clock supply control signal

See id. Claim 1 describes where each signal originates and terminates, the signal's effect, as well as the requisite sequencing of those signals for the claimed operation of the microcontroller. *See id.*

Origin	Signal	Terminus
Power Supply Control Unit	Shutdown request signal	CPU
CPU	Evacuation completed signal	Power Supply Control Unit
Power Supply Control Unit	Power shutdown control signal	Power Supply Unit
Power Supply Control Unit	Clock stop control signal	Clock Generator
Power Supply Control Unit	Power supply control signal	Power Supply Unit
Power Supply Control Unit	Restoration request signal	CPU
Power Supply Control Unit	Clock supply control signal	Clock Generator

The microcontroller of independent claim 17 largely mirrors that of claim 1, except it does not require a clock generator and it differs in some of the requisite sequencing of processes. *Compare id.* at 18:46-19:24 with 20:49-21:13; *see also* Ex. 1003 at Appendix A (Claim Comparison). For example, claim 17 covers a scenario when a microcontroller is preparing to shut down power to the processor, but aborts that effort just prior to removing power. *See* Ex. 1001 at 20:59-21:8. In that case, restoring the state is unnecessary because it has not yet been lost by the removal of power. *See id.* at 21:1-8. This requires that “the CPU, upon receiving the restoration request signal, executes a power supply restoration microprogram which does not restore the evacuated information, and continues program execution[.]” *Id.* at 21:5-8.

The '575 patent contains twenty-nine dependent claims—claims 2 through 16 depend from claim 1, and claims 18 through 31 depend from claim 17. Claims 18 through 31 largely mirror claims 2 through 16. *Compare id.* at 19:25-20:48 with 21:14-22:47; *see also* Ex. 1003 at Appendix A. The dependent claims cover different variations to the components and operation of the claimed microcontroller.

B. Claim Construction.

Claims in an *inter partes* review proceeding “shall be construed using the same claim construction standard that would be used to construe the claim in a

civil action under 35 U.S.C. 282(b), including construing the claim in accordance with the ordinary and customary meaning of such claim as understood by one of ordinary skill in the art and the prosecution history pertaining to the patent.” 37 C.F.R. § 42.100(b). “A petition for an *inter partes* review must ‘[p]rovide a statement of the precise relief requested for each claim challenged,’ which ‘statement must identify . . . [h]ow the challenged claim is to be construed’ and ‘[h]ow the construed claim is unpatentable.’” *Hologic v. Enzo*, 2018 Pat. App. LEXIS 5855, *8 (PTAB April 18, 2018) (quoting 37 C.F.R. § 42.104(b)(3)-(4)).

Petitioner takes a dubious approach to claim construction in this proceeding. First, it argues that “no construction may be necessary for this proceeding,” Petition at 12, but it includes claim construction arguments for ten terms of the ’575 patent. Second, in the related district court proceeding,¹ Petitioner argued that many of these terms are means-plus-function terms and indefinite. However here, Petitioner adopts Collabo’s constructions of those terms, *see, e.g.*, Petition at 19, and in contrast to its arguments before the district court, Petitioner appears to be able to ascertain the scope of the limitations in the Petition. Finally, when Petitioner does offer a construction, it repeatedly argues that the alleged prior art

¹ As of the date of this filing, the district court has not yet issued its order regarding claim construction for the ’575 patent. *See* 37 C.F.R. § 42.100(b).

“teaches or suggests either [Petitioner’s or Collabo’s] construction.” *See, e.g.*, Petition at 14.

Because the failings of the Petition do not turn on the construction of all ten terms identified by Petitioner, Collabo submits that the only term that should be construed is “restores the information necessary in proceeding with the program and evacuated in the information holding unit in time of power shutdown.” *See Wellman, Inc. v. Eastman Chem. Co.*, 642 F.3d 1355, 1361 (Fed. Cir. 2011) (“claim terms need only be construed ‘to the extent necessary to resolve the controversy’”) (quoting *Vivid Techs., Inc. v. Am. Sci. & Eng’g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999)).

Claim 1, limitation [1.O], requires that “the CPU, upon receiving the restoration request signal, executes a power supply restoration microprogram, *restores the information necessary in proceeding with the program and evacuated in the information holding unit in time of power shutdown*, and then branches a process to an address indicated by a program counter to continue program execution from a shutdown state.” Ex. 1001 at 19:18-24 (emphasis added).

Petitioner argues that this term should be construed as the CPU . . . “restores *from the information holding unit* the information necessary to proceed with the program, *the information was stored in the information holding unit during power shut down*.” Petition at 20 (emphasis added). That construction adds an

unnecessary element not found in the claims or specification: that the information evacuated from the CPU is restored *from* the information holding unit. Nothing in the claims and specification requires that the information be restored from the information holding unit. Instead, the specification discloses that the information restored during the restoration process be the information that “had been evacuated” during the shutdown process. *See, e.g.*, Ex. 1001 at 9:28-22, 10:18-20. Claim 1 similarly describes the information to be restored. The focus of the claim is the information, not the source from which the information is restored.

The proper construction of this term is that the CPU “restores the information necessary to proceed with the program, the information was evacuated from the CPU in the information holding unit in the power shut down process.”

II. THE ALLEGED BASES OF INVALIDITY.

The Petition alleges one ground of invalidity—that claims 1, 4, 5, 7, 12, 15-17, 20, 22, 27, 30, and 31 are obvious over the combination of U.S. Pat. No. 5,390,350 to Chung *et al.* (“Chung”) and U.S. Pat. No. 5,530,879 to Crump *et al.* (“Crump”). Claims 1 and 17 are the independent claims, claims 4-5, 7, 12, and 15-16 depend from claim 1, and claims 20, 22, 27, 30, and 31 depend from claim 17.

III. THE BOARD SHOULD EXERCISE ITS DISCRETION TO DENY INSTITUTION OF THIS REDUNDANT PETITION.

Petitioner filed a separate petition for *inter partes* review of the same claims of the same patent on the same day. This is exactly the type of case over which the

director should exercise his discretion to deny institution. *See* 35 U.S.C. § 314(a); *Cuozzo Speed Techs., LLC v. Lee*, 136 S. Ct. 2131, 2140 (2016) (“the agency’s decision to deny a petition is a matter committed to the Patent Office’s discretion”).

“Two or more petitions filed against the same patent at or about the same time (e.g., before the first preliminary response by the patent owner) may place a substantial and unnecessary burden on the Board and the patent owner and could raise fairness, timing, and efficiency concerns. *See* 35 U.S.C. § 316(b).” TRIAL PRACTICE GUIDE UPDATE (JULY 2019) at 26.

Petitioner argues that it should be able to file two petitions for *inter partes* review of the ’575 patent because it was unable to meet the word limitations imposed by the PTAB rules due to the number of claims it wished to challenge. Paper 3 (Petitioner’s Notice of Ranking Petitions) at 1.² But Petitioner has created its own word-count problem. Collabo has asserted only six claims of the ’575 patent in litigation, *see* Ex. 1015 at 2, while Petitioner challenges *twenty-one*

² Collabo responds to Petitioner’s Notice of Ranking Petitions herein rather than in a separate document. *See* TRIAL PRACTICE GUIDE UPDATE (JULY 2019) at 28.

claims.³ Notably, two of the four grounds for invalidity in Petition 1 do not involve any claims that have been asserted by Collabo (Ground 2 and Ground 4). *See* IPR2019-01523, Paper 2 at 5. Petitioner states that it “seeks to challenge additional claims” in this proceeding because “Patent Owner may assert additional claims in the future.” Paper 3 at 1. That is rank speculation. Because Petitioner has admittedly sought review of fifteen unasserted claims, this is not the “rare” case when a second petition may be needed because “the patent owner has asserted a large number of claims in litigation[.]” *See* TRIAL PRACTICE GUIDE UPDATE (JULY 2019) at 26.

In addition, speculating further, Petitioner argues that “Collabo may try to antedate Jahagirdar by attempting to swear behind it.” Paper 3 at 4. This also is not the other “rare” case “when there is a dispute about priority date requiring arguments under multiple prior art references.” *See* TRIAL PRACTICE GUIDE UPDATE (JULY 2019) at 26. Petitioner can point to no “swear behind” dispute that would justify a second petition.

The only difference Petitioner contends separates Petition 1 from Petition 2 is that Petitioner asserted different references in the two petitions. *See* Paper 3 at 4.

³ Thirteen claims are the subject of this petition, and those same thirteen claims plus an additional eight are the subject of IPR2019-01523 (Petition 1).

But the primary reference on which Petition 2 relies was asserted in Petition 1.

Petition 1 (IPR2019-01523)	Petition 2 (IPR2019-01524)	Similarities
Claims 1, 2, 3, 4, 5, 6, 7, 11, 12, 15, 16, 17, 18, 19, 20, 21, 22, 26, 27, 30, and 31 of the '575 Patent	Claims 1, 4, 5, 7, 12, 15, 16, 17, 20, 22, 27, 30, and 31 of the '575 Patent	All claims challenged in Petition 2 are already challenged in Petition 1
§ 103 combinations over Jahagirdar ACPI Saito Chung	§ 103 combination over Chung Crump	Chung is asserted in both petitions.

Petitioner states that the petitions “challenge different claims,” Paper 3 at 4, but as demonstrated in the chart above, *all* of the claims asserted in the second petition were asserted in the first petition. Next, Petitioner concedes that the “claims are challenged in both petitions,” but argues that the “grounds” are distinct. *Id.* Petitioner does not attempt to explain why the issues addressed by the differences are material, or why two petitions should be instituted even if the Board finds that one petition satisfies petitioner’s burden under 35 U.S.C. § 314(a). All that Petitioner offers is that “the manner in which the primary references disclose the independent claim elements varies,” and the petitions “combine different⁴ references in different ways to show that the challenged claims would have been obvious to a person of ordinary skill in the art.” Paper 3 at 4-5. But

⁴ The Chung reference is alleged as prior art in both proceedings.

Petitioner does not explain why that is material and why two petitions and two separate proceedings are warranted. Tellingly, the expert declaration and all other exhibits submitted by Petitioner in support of both petitions are *identical*, so the evidence on which Petitioner relies for the two proceedings does not differ.

Compare Case IPR2019-01523, Ex. 1003 (Albonesi Declaration) *with* Case IPR2019-01524, Ex. 1003 (Albonesi Declaration); *compare* IPR2019-01523, Paper 2 at v-vi (Petitioner's Exhibit List) *with* IPR2019-01524, Paper 2 at iv-v (Petitioner's Exhibit List).

Petitioner admittedly exceeded the word count, and accordingly decided to split its petition into two. Petitioner should not be able to hedge its bets and take two bites at the apple because it was not able to fit its duplicative obviousness combinations into one petition. Petitioner has placed a large burden on the PTAB's resources and on Collabo in having to defend its patent in two separate proceedings. The PTAB must assess the potential impacts on both the efficiency of the *inter partes* review process and the fundamental fairness of the process for all parties. Petitioner's serial and duplicative attacks on the '575 patent negate the AIA's goal of a quick and cost effective alternative to litigation by compounding the proceedings. The similarities between the petitions, including the verbatim expert testimony and exhibits warrant denial of this petition.

IV. THE COMBINATION OF CHUNG AND CRUMP DOES NOT RENDER ANY CLAIM OF THE '575 PATENT OBVIOUS.

Chung, Petitioner's primary reference asserted in this Petition, does not disclose several of the requisite elements of the claims of the '575 patent. Consequently, Petitioner relies on a combination with Crump for a handful of claim elements. For the elements where Petitioner relies solely on Chung, Petitioner does not show how Chung teaches or suggests the limitations at issue in the '575 patent. Petitioner's main problem is that Chung does not teach that its system resides on a single chip. Thus, it does not teach a "microcontroller." Chung teaches a multi-chip system that includes a system controller for use in a computer.

Petitioner's other big problem is that, even assuming its blanket statement that "[p]ower management has been a longstanding concern in the computer industry" is true, *see* Petition at 6, Chung does not teach many of the requisite the signals claimed by the '575 patent. Therefore, it is not surprising that Chung, which dates back to 1991, operates in a manner much different from the newer technology claimed in the '575 patent.

The expert testimony that Petitioner cites in arguing that Chung renders certain claim elements obvious is simply a copy and paste of what Petitioner argues in the Petition. *See, e.g.*, 37 C.F.R. § 42.65(a) ("Expert testimony that does not disclose the underlying facts or data on which the opinion is based is entitled to little or no weight."). Conclusory expert testimony such as Petitioner's cannot

support a case for obviousness. Petitioner is left with no disclosure of numerous elements required by the '575 patent, as detailed below.

When Petitioner does rely on the combination of Chung and Crump, Petitioner's bare conclusions do not support a motivation to combine the two references to arrive at the claimed invention. "[O]bviousness concerns whether a skilled artisan not only could have made but would have been motivated to make the combinations or modifications of prior art to arrive at the claimed invention." *Belden Inc. v. Berk-Tek LLC*, 805 F.3d 1064, 1073 (Fed. Cir. 2015). Petitioner concludes, for example, that one of ordinary skill in the art would have simply looked to Crump "for additional details," when there is no reason in the primary reference to even look elsewhere for such alleged "details." Petitioner's motivation to combine arguments that use the '575 patent as a roadmap are the result of classic hindsight. As such, the Petition does not demonstrate how any of the asserted claims are obvious over the alleged prior art and should be denied.

1. Limitation [1.Preamble].

A microcontroller comprising:

Petitioner relies solely on Chung for the claimed "microcontroller" but makes no attempt to argue how Chung teaches or suggests the "microcontroller" required by the '575 patent.

As an initial matter, the parties agree that the preamble of claim 1 of the '575 patent is limiting, but disagree over the construction. *See* Ex. 1001 at 18:46 (“A microcontroller comprising:”). Petitioner argues that the term “microcontroller” should be construed as “a chip designed for control applications rather than data-processing that has a complete CPU, semiconductor memory sufficient for control applications, and input/output capability[, that chip includes].” *See* Ex. 1018 at 7; Petition at 13.⁵ In the district court, Collabo’s construction of “microcontroller” was “an integrated circuit.” Ex. 1018 at 7. Regardless of which construction is used in this proceeding, both constructions require the microcontroller to be on a single integrated chip.⁶ *See also* Ex. 2001 (The Authoritative Dictionary of IEEE Standard Terms, 7th Ed. © 2000) (listing “integrated circuit” as a synonym for “chip”). Chung does not meet either party’s

⁵ In the Petition, Petitioner curiously omits language from its proffered claim construction in the district court: “[, that chip includes].” *Compare* Petition at 13 with Ex. 1018 at 7.

⁶ Petitioner’s omitted language “[, that chip includes],” further demonstrates that that Petitioner contends that the claimed “microcontroller” requires everything to reside on a single chip.

proffered construction of “microcontroller.”⁷

In describing how this limitation is met, Petitioner deliberately cuts quotes from Chung’s disclosure short. Chung states that its “invention relates to controllers for microcomputers, and more particularly, to integrated circuit chip core logic system controllers for minimizing power consumption by a microprocessor *in a laptop computer*,” Ex. 1007 at 1:9-12, but Petitioner omits “in a laptop computer.” See Petition at 26. Chung also states that Figure 1 shows a schematic and block diagram of “an integrated circuit core logic chip system controller *in a laptop computer system and embodying the present invention*,” Ex. 1007 at 6:17-20, but again, Petitioner omits “in a laptop computer system and embodying the present invention. See Petition at 26.

Numerous disclosures throughout Chung confirm it does not teach a “microcontroller,” but rather a system controller for use in a computer. See Ex. 1007 at Title (“Integrated Circuit Chip Core Logic System Controller With Power Saving Features For A Microcomputer System.”); *id.* at Abstract (“A system controller manages communication of data between a microprocessor, a memory

⁷ Collabo submits that because the references do not teach the claimed “microcontroller” under either party’s construction, no construction is necessary for this term. *Wellman*, 642 F.3d at 1361.

and input/output controllers in a computer.”). Under Chung’s Summary of the Invention, the disclosure states on several occasions that its invention is directed at a computer system and not at a microcontroller. *See id.* at 3:52-53 (“an embodiment of the present invention is a system controller for use in a computer system.”); *id.* at 4:27-29 (“An embodiment of the invention is a system controller and a keyboard controller for use in a computer system.”); *id.* at 4:57-59 (“an embodiment of the present invention is for minimizing power consumption in laptop computer systems.”). Under Detailed Description, Chung explains that “FIG. 1 depicts a microprocessor system in a laptop or notebook-type computer incorporating power-saving and clock frequency and clock duty cycle optimizing features and embodying the present invention.” *Id.* at 7:7-10.

As was common at for all computer systems of the early 1990s, Chung teaches a multi-chip system. Chung explains that “[t]he principal management control functions for the system of FIG. 1 are performed by four integrated circuit chips. These integrated circuit chips are the system controller **10**, videographic adapter (VGA) controller **24**, a disk controller **26**, and a serial/parallel interface controller **28**. Each of these chips are implemented in well-known CMOS integrated circuitry for minimizing power consumption.” *Id.* at 7:44-51. Chung’s multi-chip system is not integrated on a single chip, and thus does not teach a “microcontroller” under either party’s construction.

Chung discloses controllers for a microcomputer, and the controller that Petitioner relies on is “system controller 10.” “The system controller **10** provides the main interface with the CPU, performing many of the management and input and output functions of the system traditionally handled by the CPU. The system controller **10** is preferably the system controller chip manufactured by Western Digital under Part No. WD76C10LP disclosed in the technical manual WD75C10, WD76C10, WD76C1OLP System Controller For 80386LX and 30286Desk Top and Portable Compatibles, published in 1991 by Western Digital Corporation, the disclosure of which is incorporated herein by reference.” *Id.* at 7:52-62.

Chung’s system controller 10 does not disclose a “microcontroller.” First, system controller 10 is not a “microcontroller” according to Petitioner’s proffered construction because it does not include all of Petitioner’s required elements: “a complete CPU, semiconductor memory sufficient for control applications, and input/output capability.” *See* Petition at 26. Chung’s CPU is distinct from system controller 10. Ex. 1007 at 7:16-18 (“The system, by way of example, includes a conventional 16-bit AT bus **100**,⁸ coupled to a CPU **12** and, if required, a math co-

⁸ At the time, “AT bus” was a well-known and widely-used board-level bus used within Personal Computers and other microcomputers for interconnecting many subsystems of the computer system, each comprising many integrated circuits. *See* Ex. 2003 (Microsoft Computer Dictionary, 4th Ed. ©1999) (**AT bus**: “The electric

processor **14.**”); *id.* at 7:52-55 (“The system controller **10** provides the main interface with the CPU, performing many of the management and input and output functions of the system traditionally handled by the CPU.”); *see also id.*, Figure 1 (showing system controller 10, CPU 12 and CPU 14). Chung further states that “[t]he *computer system* has input/output devices for communication of digital signals in the system.” Ex. 1007 at 3:53-55. As shown in detail below, Chung’s system controller 10 is also not the claimed “microcontroller” at least because it does not include the many components and interconnects recited in the elements of claims 1 and 17. *See infra*, IV.2-IV.16.

There is no disclosure within Chung that teaches a “microcontroller.” 37 C.F.R. § 42.104(b) requires a petitioner to “identify how each challenged claim is to be construed,” and “specify where each element of the claim is found” in the references. Petitioner has not shown how a “microcontroller,” either under its own construction or under Collabo’s, is taught in Chung.

pathway used by IBM AT and compatible computers to connect the motherboard and peripheral devices.”)

2. Limitation [1.F].

the power supply control unit outputs a shutdown request signal to the CPU in response to an occurrence of a power shutdown factor,

Claim 1 of the '575 patent (limitations [1.F] and [1.G], as well as claim 17 limitations [17.E] and [17.F]) requires a “shutdown request signal.” Ex. 1001 at 18:56-59, 20:59-62. Because Chung does not disclose that its system controller 10 (the alleged “power supply control unit”⁹) outputs a “shutdown request signal” to the CPU in response to an occurrence of a power shutdown factor, Petitioner argues that the combination of Chung and Crump “teaches or suggests” this

⁹ In the related district court proceeding, Petitioner argued the term “power supply control unit” was indefinite. Ex. 1018 at 12-13. However here, Petitioner adopts Collabo’s construction, Petition at 18, which Collabo argued was the plain and ordinary meaning and that no construction was required. Ex. 1018 at 12. Petitioner concludes, without citation, that it “understands” the plain and ordinary meaning to be “logic/circuitry for controlling the CPU and power supply unit.” Petition at 18. Petitioner’s construction (which was not Collabo’s), merely substitutes the words “logic/circuitry” into the language in which the term “power supply control unit” appears in claim 1. See Ex. 1001 at 18:50-51 (“a power supply control unit for controlling the CPU and power supply unit”).

limitation. See Petition at 36. Petitioner argues that “it would have been obvious to a POSITA that a signal, like Crump’s suspend request (i.e., a shutdown request signal), *could* have been sent from Chung’s system controller to its CPU in response to an occurrence of an activity suspend timer expiration (i.e., a power shutdown factor).” *Id.* (emphasis added). Petitioner’s unsupported hindsight conclusions that expressly use the ’575 patent as a roadmap do not demonstrate the requisite motivation to combine.

“[A] patent composed of several elements is not proved obvious merely by demonstrating that each of its elements was, independently, known in the prior art. *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 418 (2007). “A party that petitions the Board for a determination of obviousness must show that ‘a skilled artisan would have been motivated to combine the teachings of the prior art references to achieve the claimed invention, and that the skilled artisan would have had a reasonable expectation of success in doing so.’” *Apotex Inc. v. Wyeth LLC*, IPR2014-00115, Paper 94, slip op. at 11 (PTAB Apr. 20, 2015) (quoting *Procter & Gamble Co. v. Teva Pharms. USA, Inc.*, 566 F.3d 989, 994 (Fed. Cir. 2009)).

Petitioner baldly asserts that because “Chung provides only a few details about what happens between writing the power-down command into the controller and beginning the CPU’s register-saving program[,]” a “POSITA would have looked to the prior art for more details on signals sent from the controller to the

CPU.” Petition at 24 (citing Ex. 1003 (¶ 279)). “As such,” Petitioner argues, “a POSITA would have looked to Crump to merely fill in obvious details not disclosed in Chung.” *Id.* (citing Ex. 1003 (¶ 280)). The only evidence Petitioner cites for these assertions is the declaration from its expert, David Albonesi. But Dr. Albonesi’s declaration just repeats verbatim what is argued in the Petition and adds nothing to support the conclusion. *Compare* Ex. 1003 (¶¶ 279-280) *with* Petition at 24-25. Indeed, Dr. Albonesi’s declaration does not present any evidence for why there is a motivation to combine Chung and Crump in order to teach the ’575 patent’s “shutdown request signal,” but merely repeats the entire argument of the Petition. *Compare* Ex. 1003 (¶¶ 301-304) *with* Petition at 35-36. Petitioner has failed to meet its burden in showing a motivation to combine Chung and Crump for this limitation. *See InfoBionic, Inc. v. Braemer Manufacturing, LLC*, IPR2015-01704, Paper 11 slip op. at 14-15 (PTAB Feb. 16, 2016) (“Petitioner’s arguments and Dr. Stone’s testimony repeating the same (with the addition of the phrase ‘in my opinion’) are too conclusory to persuade us that Petitioner has met its burden at this stage of the case.”) (citing 37 C.F.R. § 42.65(a) (“Expert testimony that does not disclose the underlying facts or data on which the opinion is based is entitled to little or no weight.”))).

Petitioner offers no explanation for *why* a person of ordinary skill in the art looking to Chung would specifically be motivated to look “for additional details”

or to add any additional signals, let alone Crump's "suspend request" in order for Chung to execute its register-saving program. Stated differently, Chung does not describe any need for "additional details" in order to execute this function, so Petitioner has no reason to conclude that a person of ordinary skill in the art would have looked for "additional details," let alone specifically to Crump. Merely asserting that a signal "could" be sent from Chung's system controller 10 does not mean one of ordinary skill in the art would be motivated to use the specific "suspend request" from Crump, or that Chung needs any signal to be added to its system.

In fact, contrary to Petitioner's assertion, there are no missing details over how Chung's register-saving program is initiated. Chung states that the operating system running on the CPU decides when it will shut down, and when that happens, the CPU sends a signal to the system controller and then executes the register-saving program. *See* Ex. 1007 at 31:52-66 ("A monitor program (not shown) runs in the environment of the operating system to detect when an inactive condition exists in the CPU. ...[S]uch program would monitor activity indications from such operating systems as DOS and Windows, and after the CPU has been inactive for a predetermined length of time, would write a special power-down command into 1872 register **912** (FIG. **2K**) of system controller **10** so advising the system controller. The CPU then executes the register-saving program. . . ."); *see*

Petition at 35 (citing same).

Important here, Chung's CPU tells the system controller that it is going to shut down—the opposite of what is required by the '575 patent. *See* Ex. 1001 at 18:56-58 (“the *power supply control unit* outputs a shutdown request signal *to the CPU* in response to an occurrence of a power shutdown factor”) (emphasis added).

Further, there are no missing details over how Chung's register-saving program begins, and no reason to add anything to Chung's system. Simply said, Chung's system operates in a manner different than that of the microcontroller of the '575 patent, and there is no motivation to “add” any “missing details” to Chung's disclosure that would in effect reverse Chung's adequately disclosed method of operation.

Petitioner's argument “seems to say no more than that a skilled artisan, once presented with the two references, would have understood that they *could be* combined. And that is not enough: it does not imply a motivation to pick out those two references and combine them to arrive at the claimed invention.” *See PersonalWeb Techs., LLC v. Apple, Inc.*, 848 F.3d 987, 993-94 (Fed. Cir. 2017) (emphasis in original) (citing *Belden Inc.*, 805 F.3d at 1073 and *InTouch Techs., Inc. v. VGO Communications, Inc.*, 751 F.3d 1327, 1352 (Fed. Cir. 2014)). *See also ActiveVideo Networks, Inc. v. Verizon Communs., Inc.*, 694 F.3d 1312, 1327 (Fed. Cir. 2012) (“The expert failed to explain how specific references could be

combined, which combination(s) of elements in specific references would yield a predictable result, or how any specific combination would operate or read on the asserted claims. Rather, the expert's testimony on obviousness was essentially a conclusory statement that a person of ordinary skill in the art would have known, based on the 'modular' nature of the claimed components, how to combine any of a number of references to achieve the claimed inventions. This is not sufficient and is fraught with hindsight bias.") (citing *KSR*, 550 U.S. at 418).

Petitioner also offers no explanation of how a person of ordinary skill in the art would have a reasonable expectation of success in using Crump's "suspend request" as the claimed "shutdown request signal" within Chung's system, or what the result would even be. For example, Petitioner does not explain how Crump's "suspend request" would be "output" from Chung's system controller 10 to Chung's CPU in advance of the initiation of Chung's register-saving program, as required by claim 1 of the '575 patent. Moreover, Chung already discloses that its *CPU* tells the system controller when it will shut down—not the other way around. Because no attempt has been made by Petitioner to answer these essential questions, there is no evidence that the proposed combination would have or even could have been made by one of ordinary skill in the art.

"[A] conclusory assertion with no explanation is inadequate to support a finding that there would have been a motivation to combine because this type of

finding, without more, tracks the *ex post* reasoning” the Supreme Court has “warned of and fails to identify any actual *reason* why a skilled artisan would have combined the elements in the manner claimed.” *TQ Delta, LLC v. Cisco Sys.*, 942 F.3d 1352, 1359 (Fed. Cir. 2019) (citation omitted); *see id. at* 1361 (explaining that the Federal Circuit has “repeatedly expressed concerns that crediting such testimony risks allowing the challenger to use the challenged patent as a roadmap to reconstruct the claimed invention using disparate elements from the prior art—i.e., the impermissible *ex post* reasoning and hindsight bias that *KSR* warned against.”) (citing *InTouch Techs.*, 751 F.3d at 1351-54, *ActiveVideo Networks*, 694 F.3d at 1327-28, and *DSS Tech. Mgmt., Inc. v. Apple Inc.*, 885 F.3d 1367, 1374-77 (Fed. Cir. 2018)).

Petitioner is performing the impermissible exercise of picking and choosing elements from the alleged prior art without any evidence of a motivation to combine. Attempting to re-create the ’575 patent in this manner is classic hindsight and does not satisfy Petitioner’s burden.

3. Limitation [1.G].

the CPU, upon receiving the shutdown request signal, executes a power shutdown microprogram, evacuates the information necessary in proceeding with the program to the information holding unit, and outputs an evacuation completed signal to the power supply control unit after evacuation is completed,

As an initial matter, limitation [1.G] is not met because the proposed combination of Chung and Crump does not teach or suggest the claimed “shutdown request signal.” *See supra* section IV.2 (Limitation [1.F]).

Additionally, Petitioner has not explained how the claimed “power shutdown microprogram” of claim 1 (and claim 17) is rendered obvious over the asserted references. *See* Ex. 1001 at 18:59-60, 20:62-63. Petitioner relies solely on Chung’s “register-saving program” for this element. *See* Petition at 36 (“Chung’s CPU executes a register-saving program (i.e., a power shutdown microprogram) in response to a shutdown request signal”). Petitioner simply calls Chung’s “register-saving program” a “power shutdown microprogram” and cites a single sentence from Chung. *Id.* at 37 (citing Ex. 1007 at 31:63-66 [“CPU then executes the register-saving program where the content of all registers and other status indications are saved in a predetermined area of RAM **30** for subsequent retrieval during the resume operation.”])). Petitioner gives no explanation for how Chung’s

program teaches or suggests the claimed *microprogram*.

A microprogram is a special program that runs at the lowest level of the hardware. *See, e.g.*, Ex. 2002 (Modern Dictionary of Electronics, 7th Ed. © 1999) (**microprogram**: “1. A computer program written in the most basic instructions or subcommands that can be executed by the computer.”; **microprogramming**: “1. The setting up of basic suboperations for a computer to handle, after which the programmer combines them, and they are presented to the computer again in a higher-level program.”); *see also* Ex. 2001 (**microprogram**: “A sequence of instructions, called microinstructions, specifying the basic operation needed to carry out a machine language instruction.”). To clarify, a computer runs a program made up of instructions, also called macro-instructions. *See* Ex. 2003 (**program**: “A sequence of instructions that can be executed by a computer.... *Also called* software.”). These instructions are held in the main memory of the computer system until executed by the CPU. In many CPUs, these individual instructions are performed by executing a microprogram or microcode comprised of microinstructions. The microcode is held entirely within the CPU. The microcode directs and coordinates the lowest-level hardware resources within the CPU to effect the specific semantics of the macro-level instructions. *See* Exs. 2001-2003 (definitions of microprogram and program).

In Chung, the register-saving program is described as part of the “monitor program” that “runs in the environment of the operating system to detect when an inactive condition exists at the CPU.” Ex. 1007 at 31:52-54; *see id.* at 31:63-66 (“The CPU then executes the register-saving program where the content of all registers and other status indications are saved in a predetermined area of RAM **30** for subsequent retrieval during the resume operation.”). There is no indication in Chung that the register-saving program is a microprogram, and no argument is advanced by Petitioner arguing how Chung’s “register saving program” is a microprogram.

Chung also does not disclose the requisite “evacuation completed signal” output by the CPU to the power supply control unit. The signal Petitioner points to is a “halt instruction causing the CPU to go to a halt mode and set signals 1,0,1,1,0 on system controller inputs M/IO 943a [HALTDET 943a—indicating that the CPU has halted] D/C# 943b, W/R# 943c, BHE 943d, BLE# 943e and ADS# 943f.” Petition at 37 (citing Ex. 1007 at 31:67-32:6). What Petitioner omits, however, is that line HALTDET 943a, inside system controller 10 (the alleged “power supply control unit”), simply receives a “1” signal “indicating that a halt in the CPU has been detected.” Ex. 1007 at 32:52-55; *id.*, Figure 2L. Thus, the “1” signal to HALTDET 943a occurs when the system is shutting down, or pausing if not shutting it down. This happens irrespective of whether anything has been saved by

the register-saving program. Petitioner points to no disclosure that this halt instruction signal is *only* initiated when the registers have been saved by the register-saving program. Since Chung's halt instruction can be executed when shutting down or pausing the system, in which case HALTDET 943a becomes asserted and there has been no evacuation, neither the halt instruction nor the specific combination of signals at the system controller inputs noted previously can be the "evacuation completed signal" of the '575 patent that indicates the evacuation of the information necessary in proceeding with the program has been completed.

4. Limitation [1.H].

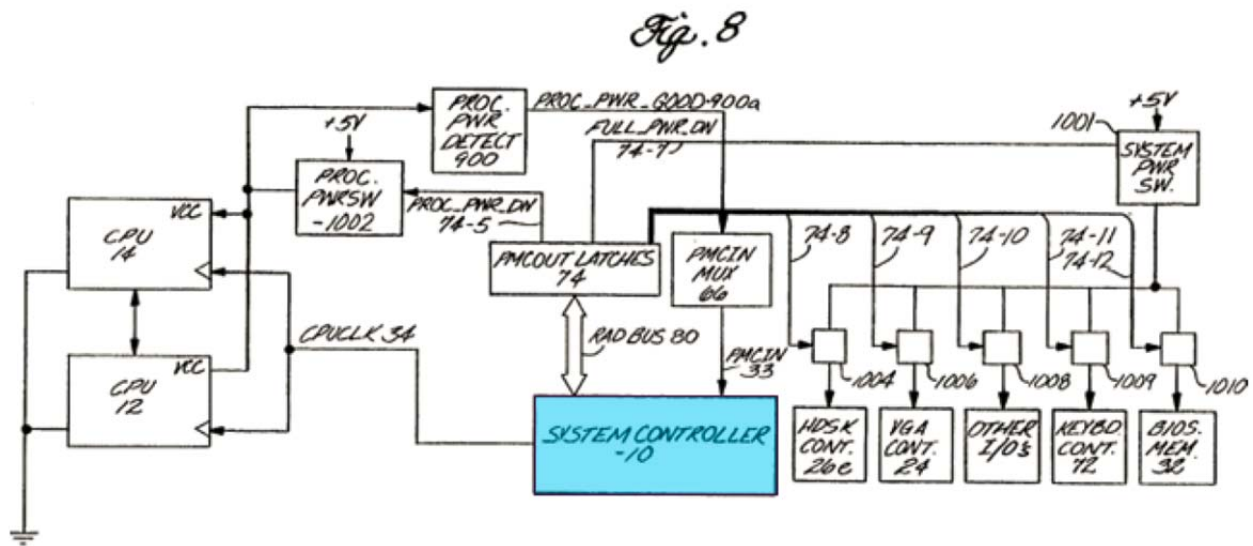
the power supply control unit, upon receiving the evacuation completed signal, outputs a power shutdown control signal to the power supply unit,

As an initial matter, limitation [1.H] is not met because Chung does not teach or suggest the claimed "evacuation completed signal." *See supra* section IV.3 (Limitation [1.G]).

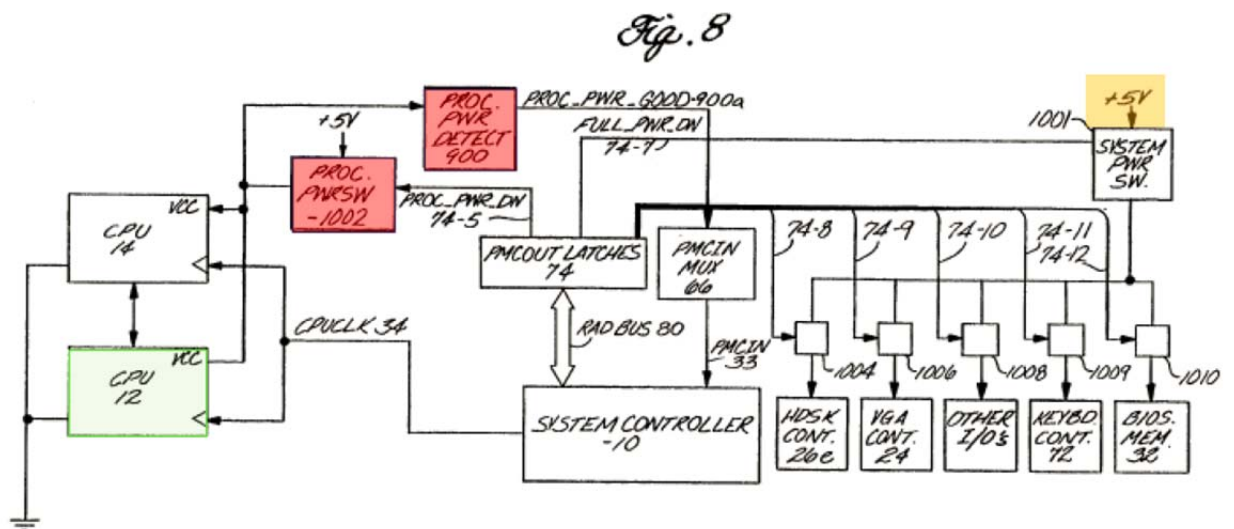
Claim 1 of the '575 patent (limitations [1.H] and [1.I]) also requires a "power shutdown control signal." Ex. 1001 at 18:65-19:3, 20:45-48. Petitioner has not shown how the claimed "power shutdown control signal" (output from the power supply control unit to the power supply unit) is rendered obvious over the references asserted.

Petitioner relies solely on Chung for this limitation. *See* Petition at 38-39. But Petitioner does not precisely identify what disclosure in Chung teaches the claimed “power shutdown control signal,” and the only identified items are not signals sent from Petitioner’s alleged “power supply control unit” (system controller 10) to its alleged “power supply unit” (processor power switch 1002 together with processor power detect 900).

First, Petitioner states that Chung “writes a value into PMCOOUT latches 74 (i.e., a power shutdown control signal) and thereby commands the CPU power supply to be disabled at power switch 1002.” Petition at 38 (citing Ex. 1007 at 32:14-19). Chung, however, confirms that the alleged “power shutdown control signal” only goes from system controller 10 to PMCOOUT latches 74. Ex. 1007 at 32:14-19 (“The system controller **10** then writes a value into the PMCOOUT latches **74** causing the processor power switch **1002** to be disabled, thus disabling power from the +5 V power supply to the CPUs while leaving the power switches **1001** through **1010** enabled and supplying power to the respective devices.”). Critically, Petitioner does not allege that PMCOOUT latches 74 is part of either the alleged “power supply control unit” (Chung’s system controller 10) or its alleged “power supply unit” (Chung’s processor power switch 1002 together with processor power detect 900). *See* Petition at 32 (shading in alleged “power supply control unit” in blue).



See also Petition at 29 (shading in alleged “power supply unit” in red).



Moreover, Petitioner does not explain, and there is no disclosure in Chung, of how processor power switch 1002 is instructed by PMCOUT latches 74 to either power up or power down the CPU. Additionally, Petitioner does not argue that PMCOUT latches 74 is a signal. Petitioner simply argues that PMCOUT latches 74 “commands the CPU power supply to be disabled at power switch 1002,” but the

disclosure cited for this conclusion (Ex. 1007 at 32:14-19) does not explain how PMCOOUT latches 74 “commands” the power switch 1002, or, for example, if that “command” is performed by a signal. *See* Petition at 38 (citing Ex. 1007 at 32:14-19). Therefore, Petitioner’s argument that Chung’s system controller 10 “writ[ing] a value into PMCOOUT latches 74” could teach or suggest the claimed “power shutdown control signal” is not persuasive.

Next, Petitioner argues that “Chung’s system controller 10 provides power management control signals (i.e. a shutdown request signal) to power switch 1002 through latches 74.” Petition at 38. Petitioner previously alleged that Chung’s “suspend request” taught the claimed “shutdown request signal,” so it is unclear why Petitioner now argues that Chung’s “power management control signals” are the “shutdown request signal.” *See* Petition at 36; *see supra*, section IV.2 (Limitation [1.F]). Although not stated, it is also unclear whether Petitioner is suggesting that Chung’s power management control signals teach the claimed “power shutdown control signal.” Petitioner adds that “[l]atches 74 receive control signals from the system controller 10, and in turn, outputs a signal PROC-PWR--DN 74-5 to enable and disable processor power switch 1002.” Petition at 38-39 (citing Ex. 1007 at 11:8-13, 31:13-22). Petitioner simply concludes: “Thus, Chung discloses this claim element.” Petition at 39 (citing to verbatim paragraphs in the declaration of Dr. Albonesi, ¶¶ 309-310). While Petitioner did not specify which

signal is the claimed “power shutdown control signal,” it cannot be Chung’s control signals or Chung’s PROC-PWR--DN 74-5 since neither is a signal sent from Chung’s system controller 10 (the alleged “power supply control unit” to processor power switch 1002 (part of the alleged “power supply unit”)—both reach only as far as the PMCOUT latches 74, which Petitioner does not argue is part of either the power supply control unit or the power supply unit.

5. Limitation [1.I].

the power supply unit shuts down power supply to the CPU upon receiving the power shutdown control signal from the power supply control unit,

Limitation [1.I] similarly requires the “power shutdown control signal” described in limitation [1.H], Ex. 1001 at 18:65-19:3; thus, Petitioner’s argument here also fails because Chung does not teach or suggest the claimed “power shutdown control signal” that is received by the “power supply unit.” *See supra*, IV.4 (Limitation [1.H]). Petitioner again cites the same disclosure from Chung, that “system controller 10 then writes a value into PMCOUT latches 74 causing the processor power switch 1002 to be disabled, thereby disabling power from the +5 V power supply to the CPUs...” Petition at 39. But because there is no “power shutdown control signal” sent from Chung’s system controller 10 (the alleged “power supply control unit”) to either of Chung’s processor power switch 1002 or processor power detect 900 (the alleged “power supply unit”), *see supra* IV.4,

Petitioner has not demonstrated how the “power supply unit shuts down power supply to the CPU *upon receiving the power shutdown control signal* from the power supply control unit.” Ex. 1001 at 19:1-3 (emphasis added).

6. Limitation [1.J].

the power supply control unit, upon receiving the evacuation completed signal, outputs a clock stop control signal to the clock generator,

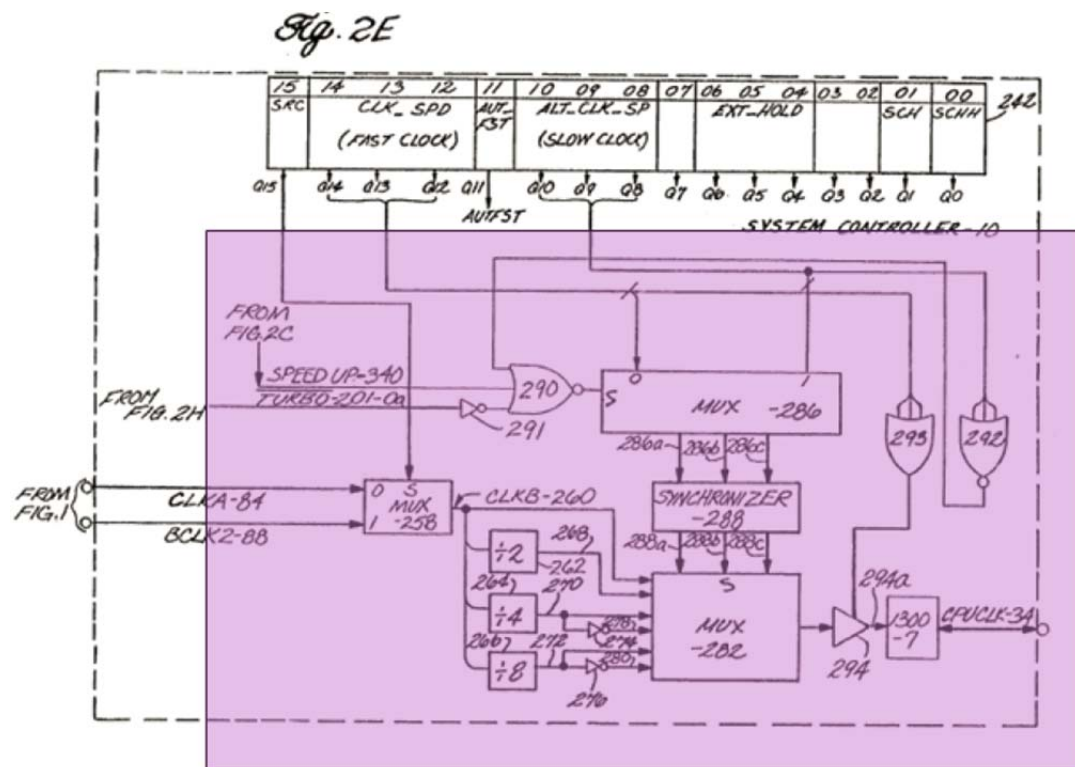
Claim 1 of the '575 patent also requires that a “clock stop control signal” be output from the “power supply control unit” to the “clock generator” upon receipt of the “evacuation completed signal.” Ex. 1001 at 19:4-6. As an initial matter, limitation [1.J] is not met because Chung does not teach or suggest the claimed “evacuation completed signal.” *See supra* section IV.3 (Limitation [1.G]).

Petitioner states that Chung’s system controller 10 (the alleged “power supply control unit”) “sends a signal to the circuits connected to the output of CPUCLK control register (i.e., the clock generator) to prevent clock pulses to the CPU (i.e., a clock stop control signal).” Petition at 39. Petitioner’s conclusion is not supported.

Petitioner alleged that the claimed “clock generator” is Chung’s “circuits connected to the output of CPUCLK control register 242,” which are contained within Chung’s system controller 10. Petition at 35; *see* Ex. 1007, Figure 2E. Petitioner’s only support in Chung for the claimed “clock stop control signal” is

that “the system controller . . . tristates the output driver for the clock at CPUCLK 34 preventing clock pulses to the CPUs.” *Id.* (citing Ex. 1007 at 32:7-13). There are, however, several inconsistencies in Chung that Petitioner does not account for or attempt to explain.

First, what Petitioner contends is Chung’s “clock generator” (what Petitioner shades in purple in its annotated Figure 2E below) is encompassed entirely in Chung’s system controller 10, the alleged “power supply control unit.”



Petition at 35. The alleged “clock generator” includes the tristating that occurs at driver 294 (depicted at the triangle in the lower right corner of Figure 2E). Since the alleged “clock generator” is internal to system controller 10, the alleged “power supply control unit,” the “power supply control unit” is not *outputting* a signal to

the “clock generator.” Additionally, the tristating signal of driver 294 is not a signal sent from system controller 10 to the alleged “clock generator” since it is completely within the alleged “clock generator”.

Chung also states that “output driver **1300-9** is connected to the **294a** output of tristate driver **294** as generally depicted in FIG. 2E.” Ex. 1007 at 36:50-55. As shown in Figure 2E, the tristating of the clock happens at “tristate driver 294” and *not* one gate later at CPUCLK 34. *Id.* at FIG. 2E. Thus, CPUCLK 34 according to Chung’s Figure 2E is never tristated. Petitioner does not account for this discrepancy in Chung, so Petitioner’s argument that the “clock stop control signal” occurs when the system controller “tristates the output driver for the clock at CPUCLK 34” is not possible. The verbatim paragraphs of Dr. Albonesi’s declaration that are cited as purported support similarly do not account for this problem with Chung’s disclosure. *Compare* Petition at 39-40 *with* Ex. 1003 at ¶¶ 313-315. Petitioner has not demonstrated that the claimed “clock stop control signal” is disclosed in Chung.

7. Limitation [1.K]

the power supply control unit outputs a power supply control signal to the power supply unit in response to an occurrence of a power supply restoration factor,

Claim 1 of the ’575 patent (limitations [1.K] and [1.L]) requires a “power

supply control signal.” Ex. 1001 at 19:7-11. As with limitation [1.H]’s “power shutdown control signal,” Petitioner blurs the details when it comes to limitation [1.K]’s “power supply control signal.” Asserting essentially the reverse of what it submitted with respect to limitation [1.H], Petitioner relies on Chung’s writing of a value to PMCOUT latches 74 to teach the claimed “power supply control signal.” Again, Petitioner does not precisely identify what disclosure in Chung teaches the claimed “power supply control signal,” and the only identified items are not signals sent from Petitioner’s alleged “power supply control unit” (system controller 10) to its alleged “power supply unit” (processor power switch 1002 together with processor power detect 900).

Petitioner states that Chung’s “system controller 10 writes out a value to the PMCOUT latches 74 causing the processor power switch 1002 to again start enabling power from the +5 V power supply to the CPU.” Petition at 40 (citing Ex. 1007 at 32:29-33). That disclosure in Chung, however, confirms that the alleged “power supply control signal” only goes from system controller 10 to PMCOUT latches 74. As explained above, *see supra* IV.4 (Limitation [1.H]), Petitioner does not allege that PMCOUT latches 74 is part of either the alleged “power supply control unit” (Chung’s system controller 10) or its alleged “power supply unit” (Chung’s processor power switch 1002 together with processor power detect 900). *See* Petition at 32, 29 (annotations to Chung’s Figure 8). Moreover, Petitioner does

not explain, and there is no disclosure in Chung, of how processor power switch 1002 is instructed by PMCOOUT latches 74 to either power up or power down the CPU. Petitioner also does not argue that PMCOOUT latches 74 is a signal.

This time, Petitioner simply argues that “[b]ecause the system controller must output signals to write a value to the PMCOOUT latches to enable power to flow to the CPU, a POSITA would have understood that Chung’s value-write signals teach or suggest the recited power supply control signal.” Petition at 40 (citing Ex. 1003 ¶ 318). Petitioner’s “evidence” in support of this statement is merely Dr. Albonesi parroting the petition’s words. No explanation is offered as to what are the so-called “signals” output from system controller 10 to write a value to PMCOOUT latches 74. Bare conclusions such as this cannot support an obviousness case. “[R]ejections on obviousness grounds cannot be sustained by mere conclusory statements; instead, there must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness.” *KSR*, 550 U.S. at 418 (quoting *In re Kahn*, 441 F.3d 977, 988 (Fed. Cir. 2006)); *TQ Delta*, 942 F.3d at 1359-63 (collecting cases); 37 C.F.R. § 42.65(a) (“Expert testimony that does not disclose the underlying facts or data on which the opinion is based is entitled to little or no weight.”); *InfoBionic*, IPR2015-01704, Paper 11 slip op. at 14-15 (expert testimony that merely repeats the petition too conclusory to meet petitioner’s burden). Petitioner has not demonstrated that Chung teaches or

suggests the claimed “power supply control signal.”

8. Limitation [1.L].

the power supply unit, upon receiving the power supply control signal, starts to supply power to the CPU,

Limitation [1.L] similarly requires the “power supply control signal” described in limitation [1.K], Ex. 1001 at 19:7-11; thus, Petitioner’s argument with respect to this limitation also fails because Chung does not teach or suggest the claimed “power supply control signal” that is received by the claimed “power supply unit.” *See supra*, IV.7 (Limitation [1.K]).

Petitioner cites the disclosure in Chung that “[d]uring the power resume operation, the system controller 10 writes out a value to the PMCOUT latches 74 causing the processor power switch 1002 to again start enabling power from the +5 V power supply to the CPU.” Ex. 1007 at 32:29-33; Petition at 41. But because there is no “power supply control signal” sent from Chung’s system controller 10 (the alleged “power supply control unit”) to either of Chung’s processor power switch 1002 or processor power detect 900 (the alleged “power supply unit”), *see supra* IV.7, Petitioner has not demonstrated how the “the power supply unit, *upon receiving the power supply control signal*, starts to supply power to the CPU[.]” Ex. 1001 at 19:10-11 (emphasis added).

9. Limitation [1.M].

the power supply control unit outputs a restoration request signal to the CPU and outputs a clock supply control signal to the clock generator when a supplied power supply voltage is stabilized,

The '575 patent requires that the “power supply control unit” output (1) a “restoration request signal” to the CPU and (2) a “clock supply control signal” to the “clock generator” when a supplied power supply voltage is stabilized. Ex. 1001 at 19:12-15. Claim 1 limitations [1.M] and [1.O] as well as claim 17 limitations [17.G] and [17.H] require the claimed “restoration request signal,” and claim 1 limitations [1.M] and [1.N] require the claimed “clock supply control signal.” See *id.* at 19:12-15, 19:18-24, 21:1-8. Petitioner makes no serious attempt to explain how this limitation is rendered obvious over the asserted references.

Petitioner asserts that Chung’s “CPU reset” teaches the claimed “restoration request signal.” See Petition at 41 (“Chung’s system controller asserts a CPU reset (i.e., a restoration request signal)”) (citing Ex. 1007 at 32:31-43 [*sic*]).¹⁰ As

¹⁰ “When the PROC__PWR__GOOD signal is true, the output signals from the system controller to the CPU are enabled. In particular, the CPU clock starts pulsing and the CPU reset is asserted. After a 1 micro second delay, the system controller inputs connected to the CPU are enabled. When a certain number of

purported support for this argument, as can best be discerned from the Petition, Petitioner argues that “Chung further describes the signals that cause the power-resume operations. *Id.*, 32:33-38 (describing that when “the PROC_PWR_GOOD signal is true, the output signals from the system controller to the CPU are enabled[,] the CPU clock starts pulsing and the *CPU reset* is asserted.”)[.]” Petition at 42 (emphasis added). Petitioner does not identify which of the signals cited is the claimed “restoration request signal.” See Petition at 42. Petitioner goes on to cite additional purported “signals” (ENCKOUT 926-4 and PROCOEN 926-7), but does not explain which signal it is relying on for the claimed “restoration request signal.” See *id.*

If Petitioner is relying on the cited “CPU reset” for the claimed “restoration request signal,” Petitioner has not explained how that is a “signal” output from the system controller (the alleged “power supply control unit”) to the CPU when a supplied power voltage is stabilized. Chung states that during its power up process, the “CPU reset” is *removed*. See Ex. 1007 at 32:38-40 (“When a certain number of clock pulses have been generated, the CPU reset is removed and the CPU will then resume normal operation.”); *id.* at 35:10-18 (“processor interface **218** (FIG. 2A)

clock pulses have been generated, the CPU reset is removed and the CPU will then resume normal operation.” Ex. 1007 at 32:33-41.

forms a 0 at CPURES 218a output to control bus 46 forcing the CPU to a reset mode”); *id.* at Figure 2N (showing the CPU reset being applied during power down and removed only as the last step of the power up process). Moreover, Petitioner has not accounted for the fact that Chung’s “CPU reset” need not cause a “restoration.” Since Chung’s “CPU reset” is initiated upon the powering on of the CPU, it cannot act as the “restoration request signal” because there may be no need to restore a previous state upon the initial powering-on of the CPU. *See id.* at 32:20-29. Further, Chung’s disclosure of the “CPU reset” is silent as to whether the CPU reset occurs only when a previous state is being restored. *See id.* Thus, removal of “CPU reset” does not unambiguously initiate state restoration.

For the claimed “clock supply control signal,” Petitioner argues, again without identifying a specific signal, that the signal is taught when Chung’s system controller “commands the CPU clock to start pulsing (i.e., a clock supply control signal).” *See id.* Petitioner lists a string of various “signals” without identifying which signal purportedly “commands” the CPU clock to start pulsing. *See id.* (citing Ex. 1007 at 32:33-38, 34:56-59, 34:59-64, 32:38-41). Petitioner gives no explanation for which signal is sent from the system controller (the alleged “power supply control unit”) to the “circuits connected to the output of CPUCLK control register 242” (the alleged “clock generator”) when a supplied power voltage is stabilized. *See* Petition at 34. Petitioner’s unexplained string cite, purportedly

describing “signals that cause the power-resume operations,” Petition at 42, is insufficient to meet Petitioner’s burden. Petitioner has not identified a signal that teaches the claimed “clock supply control signal.”

10. Limitation [1.N].

the clock generator, upon receiving the clock supply control signal, restarts to supply an operation clock, and

Limitation [1.N] similarly requires the “clock supply control signal” described in limitation [1.M], Ex. 1001 at 19:16-17; thus, Petitioner’s argument with respect to this limitation also fails because Petitioner has not shown how Chung teaches or suggests the claimed “clock supply control signal” that is output from the claimed “power supply control unit” to the claimed “clock generator.” See *supra*, IV.9 (Limitation [1.M]). Petitioner cites the same disclosure from Chung that when “PROC_PWR_GOOD signal is true, the output signals from the system controller to the CPU are enabled[,] the CPU clock starts pulsing and the CPU reset is asserted.” Petition at 42 (citing Ex. 1007 at 32:33-38). Petitioner also cites the same disclosure regarding ENCKOUT 926-4. *Id.* (citing Ex. 1007 at 34:56-59 [“ENCKOUT 926-4 enables the output driver [1300-7] to again apply the CPUCLK pulses on line CPUCLK 34 to the CPUs”]). But because Petitioner has not identified a signal that could be the claimed “clock supply control signal,” see *supra*, IV.9, Petitioner has not demonstrated how the “the clock generator, upon

receiving the clock supply control signal, restarts to supply an operation clock[.]”

Ex. 1001 at 19:16-17 (emphasis added).

11. Limitation [1.O].

the CPU, upon receiving the restoration request signal, executes a power supply restoration microprogram, restores the information necessary in proceeding with the program and evacuated in the information holding unit in time of power shutdown, and then branches a process to an address indicated by a program counter to continue program execution from a shutdown state.

Claim 1 requires that after the CPU receives the “restoration request signal,” the CPU (1) executes a “power supply restoration microprogram,” (2) “restores the information necessary in proceeding with the program and evacuated in the information holding unit in time of power shutdown,” and then (3) “branches a process to an address indicated by a program counter to continue program execution from a shutdown state.” Ex. 1001 at 19:18-24.

As an initial matter, this limitation [1.O] requires the “restoration request signal” described in limitation [1.M]. Ex. 1001 at 19:18. Petitioner has not shown how Chung teaches or suggests the claimed “restoration request signal” that is output from the claimed “power supply control unit” to the CPU. *See supra*, IV.9

(Limitation [1.M]). Petitioner has not demonstrated how the “the CPU, *upon receiving the restoration request signal*, executes a power supply restoration microprogram, restores the information necessary in proceeding with the program and evacuated in the information holding unit in time of power shutdown, and then branches a process to an address indicated by a program counter to continue program execution from a shutdown.” Ex. 1001 at 19:18-24 (emphasis added).

Petitioner does not explain how the remaining requisite elements of this limitation are rendered obvious over the asserted references. First, Petitioner does not explain how the claimed “power supply restoration *microprogram*” is taught. Petitioner simply states that “programs for storing the contents of the registers from the microprocessor to RAM and for restoring the content of the registers after power up are well known in the art[,]” and that “Chung also teaches or suggests a register saving program, where necessary information, including a program counter, is saved for subsequent retrieval, and a restoration request signal.” Petition at 43. Petitioner’s general conclusions about what was known in the art are not specific, and nothing Petitioner offers explains how the alleged “programs” teach the claimed “microprogram” of the ’575 patent. *See supra*, IV.3 (definitions of “microprogram” and “program”).

Petitioner argued that the phrase “restores the information necessary in proceeding with the program and evacuated in the information holding unit in time

of power shutdown” should be construed to mean “restores from the information holding unit the information necessary to proceed with the program, the information was stored in the information holding unit during power shut down.” Petition at 20. But Petitioner does not apply its proposed construction, nor does it apply Collabo’s construction which it knows from the district court proceedings, in arguing that the limitation is met. Petitioner points to a disclosure in Chung that “it can now continue operation from the condition at which it was originally stopped and powered down.” *Id.* at 43. But that does not explain how the “information necessary in proceeding with the program and evacuated in the information holding unit in time of power shutdown” is restored. Pointing to Chung’s end result is not sufficient to demonstrate how it got there, when how it got there is claimed in the ’575 patent.

Lastly, Petitioner concludes that “because Chung’s CPU is able to return to and continue operation from the condition at which it was originally stopped and powered down, it would have been obvious to branch a process to an address indicated by a program counter.” *Id.* at 44 (citing Ex. 1003 at ¶ 332). But as paragraph 332 of Dr. Albonesi’s declaration merely repeats the Petition it should be given little or no weight. Petitioner therefore has completely glossed over another requisite element of limitation [1.O] and has made no attempt to explain why it would have been obvious to one of ordinary skill in the art that Chung’s

CPU would “branch[] a process *to an address indicated by a program counter* to continue program execution from a shutdown state.” See Ex. 1001 at 19:22-24 (emphasis added); see also *TQ Delta*, 942 F.3d at 1359-63; 37 C.F.R. § 42.65(a); *InfoBionic*, IPR2015-01704, Paper 11 slip op. at 14-15. Petitioner’s obviousness argument does not meet the requisite standard. See *KSR*, 550 U.S. at 418 (quoting *In re Kahn*, 441 F.3d at 988) (“[R]ejections on obviousness grounds cannot be sustained by mere conclusory statements; instead, there must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness.”).

12. Limitations [17.Preamble], [17.E], And [17.F].

Because claim 17 limitations [17.Preamble]-[17.F] “are identical to limitations [1.Preamble]-[1.D],[1.F]-[1.G],” Petitioner presents no additional arguments for claim 17 limitations [17.P] through [17.F]. Petition at 53-54. As such, Petitioner’s invalidity challenge regarding independent claim 17 limitations [17.Preamble] through [17.F] suffers from the same problems described above with respect to claim 1 limitations [1. Preamble], [1.F], and [1.G]. See *supra*, IV.1-IV.3. Petitioner has not demonstrated how claim 17 limitations [17.Preamble] (“microcontroller”), [17.E] (“the power supply control unit outputs a shutdown request signal to the CPU in response to an occurrence of a power shutdown factor”), and [17.F] (“the CPU, upon receiving the shutdown request signal,

executes a power shutdown microprogram, evacuates the information necessary in proceeding with the program to the information holding unit, and outputs an evacuation completed signal to the power supply control unit after evacuation is completed”) are obvious over the combination of Chung and Crump. *See id.*

13. Limitation [17.G].

the power supply control unit, upon receiving an occurrence of a power supply restoration factor after receiving the evacuation completed signal, outputs a restoration request signal to the CPU,

Independent claim 17 of the '575 patent requires that “the power supply control unit, upon receiving an occurrence of a power supply restoration factor after receiving the evacuation completed signal, outputs a restoration request signal to the CPU[.]” Ex. 1001 at 21:1-4.

As an initial matter, this limitation [17.G] requires the receipt of the “evacuation completed signal” described in limitations [17.F]/[1.G]. *See supra*, IV.3 (Limitation [1.G]). Limitation [17.G] also requires that a “restoration request signal” be output from the “power supply control unit” to the CPU, as with the “restoration request signal” described in claim 1. *See supra*, IV.9 (Limitation [1.M]). Petitioner relies on the same arguments it presented with respect to limitations [1.G] and [1.M]. Petition at 54. Thus, Petitioner’s arguments with respect to this limitation also fail because Petitioner has not shown how Chung

teaches or suggests the claimed “evacuation completed signal” or the claimed “restoration request signal.” Petitioner has not demonstrated how the “*the power supply control unit*, upon receiving an occurrence of a power supply restoration factor *after receiving the evacuation completed signal*, outputs a restoration request signal to the CPU[.]” Ex. 1001 at 21:1-4 (emphasis added).

Next, Petitioner appears to be attempting to prove obviousness by inherency with respect to this limitation’s requirement that the “restoration request signal” be output from the “power supply control unit” after it receives “an occurrence of a power supply restoration factor after receiving the evacuation completed signal[.]” See Petition at 54 (citing Ex. 1003 at ¶ 359) (“It would have been obvious to a POSITA that Chung’s evacuation complete signal would have been received before receiving an occurrence of the power supply restoration factor because Chung’s evacuation complete signal . . . initiates Chung’s power-down sequence and a power supply factor would have no effect on a CPU that has not yet powered down.”). If that is the case, Petitioner has failed to meet the “high standard” of proving obviousness by inherency.

“[T]he use of inherency, a doctrine originally rooted in anticipation, must be carefully circumscribed in the context of obviousness.” *Par Pharm., Inc. v. TWi Pharm., Inc.*, 773 F.3d 1186, 1195 (Fed. Cir. 2014). “The mere fact that a certain thing *may* result from a given set of circumstances is not sufficient [to establish

inherency]. [M]ere recitation of a newly discovered function or property, inherently possessed by things in the prior art, does not distinguish a claim drawn to those things from the prior art.” *Id.* (internal citations and quotation marks omitted). “A party must, therefore, meet a high standard in order to rely on inherency to establish the existence of a claim limitation in the prior art in an obviousness analysis—the limitation at issue necessarily must be present, or the natural result of the combination of elements explicitly disclosed by the prior art. *Id.* at 1195-96.

The only evidence cited in support of Petitioner’s argument that “[i]t would have been obvious to a POSITA that Chung’s evacuation complete signal would have been received before receiving an occurrence of the power supply restoration factor...” is paragraph 359 of the declaration of its expert, Dr. Albonesi (Ex. 1003). However, paragraph 359 is merely a verbatim repetition of the petition. *Compare* Petition at 54 *with* Ex. 1003 at ¶ 359; 37 C.F.R. § 42.65(a); *InfoBionic*, IPR2015-01704, Paper 11 slip op. at 14-15. Neither Petitioner nor its expert Dr. Albonesi offers anything more. This is insufficient to prove obviousness by inherency.

14. Limitation [17.H].

the CPU, upon receiving the restoration request signal, executes a power supply restoration microprogram which does not restore the evacuated information, and continues program execution, and

Claim 17 of the '575 patent requires that after the CPU receives the “restoration request signal,” the CPU executes a “power supply restoration microprogram which does not restore the evacuated information, and continues program execution[.]” Ex. 1001 at 21: 5-8. Petitioner does not explain how all of the requisite elements of this limitation are rendered obvious over the asserted references.

First, this limitation [17.H] requires the “restoration request signal” that was output from the “power supply control unit” to the CPU that was described in limitation [17.G] (and also in claim 1 limitation [1.M]). As was the case with respect to those limitations, Petitioner did not show how Chung teaches or suggests the claimed “restoration request signal.” *See supra*, IV.9 (Limitation [1.M]), IV.13 (Limitation [17.G]). Petitioner’s bare conclusion that “Chung executes a power supply restoration microprogram upon receiving a restoration request signal and continues program execution” is not supported. *See* Petition at 55. Petitioner has not demonstrated how the “the CPU, *upon receiving the restoration request signal*,

executes a power supply restoration microprogram which does not restore the evacuated information, and continues program execution[.]” Ex. 1001 at 21:5-8 (emphasis added).

Second, Petitioner does not explain how the claimed “power supply restoration microprogram which does not restore the evacuated information” is taught. *See supra*, IV.3 (definitions of “microprogram” and “program”). Petitioner simply states that “it would have been obvious to a POSITA that if an interrupt occurred after Chung began its register-saving program—and before the control initiated the power-down sequence—there would be no need to perform a restoration, because the data would still reside at the CPU.” Petition at 55 (citing Ex. 1003 at ¶ 361). “Specifically, because nothing would have been powered down, the data would not yet be erased from the CPU and Chung’s CPU could resume without restoring the evacuated information.” *Id.* These conclusions are speculative, at best. Chung does not disclose a scenario wherein its system (which is a computer and not a microcontroller) is preparing to shut down power to its processor but stops that effort before power is shut down, such that restoring the state would be unnecessary at a later time. *See* Ex. 1001 at 20:59-21:8. Neither Petitioner, nor its expert repeating the words of the Petition, point to any evidence in Chung to support these conclusions. *KSR*, 550 U.S. at 418; *TQ Delta*, 942 F.3d at 1359-63; 37 C.F.R. § 42.65(a). Petitioner has not met its burden of

demonstrating that the claimed “power supply restoration microprogram” of claim limitation [17.H] is taught or suggested by Chung.

15. Limitation [17.I] / Dependent Claim 4.

the power shutdown microprogram evacuates the information necessary in proceeding with the program to a stack region in the information holding unit, and then evacuates to a specific place only a value of a stack pointer for pointing to an evacuation place.

Independent claim 17 of the '575 patent (as well as the substantially identical dependent claim 4 that depends on the microcontroller according to claim 1), requires that the “power shutdown microprogram” first described in limitation [17.F] (as well as in claim 1 limitation [1.G]) “evacuates the information necessary in proceeding with the program to a *stack region in the information holding unit*, and then evacuates to a *specific place only a value of a stack pointer for pointing to an evacuation place.*” Ex. 1001 at 21:9-13 (emphasis added). A “stack region” is “a hardware or software data structure in which items are stored in a last-in-first-out manner, similar to a cafeteria plate dispenser.” Ex. 2004 (Comprehensive Dictionary of Electronical Engineering, 2nd Ed. © 2005). *See also id.* (**stack pointer**: “a register in a processor that holds the address of the top of the stack memory location. The address varies as information is stored on or retrieved from

the stack; it always points to the top of the stack.”).

Petitioner asserts that “Chung teaches evacuating the information necessary in proceeding with the program to a dedicated cache memory and stores an address so the CPU can continue program execution from a shutdown state and continue operation from the condition at which it was originally stopped and powered down.” Petition at 44. Petitioner’s unexplained conclusion does not support a finding that Chung teaches or suggests a “power shutdown microprogram” wherein the information necessary in proceeding with the program is evacuated to a “stack region in the information holding unit” and then evacuates “to a specific place only a value of a stack pointer for pointing to an evacuation place.” *See supra*, IV.3 (definitions of “microprogram” and “program”).

Petitioner argues that to the extent Chung does not teach or suggest what is required of this limitation, “doing so was known in the art.” Petition at 44. As such, Petitioner proposes a combination of Chung and Crump to teach this limitation.

Petitioner concludes that “[i]t would have been obvious to a POSITA that Crump’s stack could have been implemented in Chung’s microcontroller to provide additional state saving/restoring functionality.” *Id.* (citing Ex. 1003 at ¶ 336). Petitioner has not demonstrated a motivation to combine. That something “could have been” implemented in Chung’s system does not mean one of ordinary skill in the art would be *motivated* to make that change. Petitioner has provided no

rationale as to *why* a person of ordinary skill in the art would combine Chung with Crump for the stated purpose, and has pointed to no teaching in Chung for any need of “additional” state saving or restoring functionality. Conclusory assertions are not sufficient in proving a motivation to combine. *See, e.g., PersonalWeb Techs.*, 848 F.3d at 993-94 (Petitioner’s argument “seems to say no more than that a skilled artisan, once presented with the two references, would have understood that they *could be* combined. And that is not enough: it does not imply a motivation to pick out those two references and combine them to arrive at the claimed invention.”). Additionally, since Petitioner argues that Chung purportedly already teaches this limitation, *see* Petition at 44, there is no motivation to combine where two references disclose common functionality that would be redundant if present in the combination. *See Stryker Corp. v. Karl Storz Endoscopy America, Inc.*, IPR2015-00764, Paper 13, slip op. at 13 (Sept. 2, 2015). The only cited evidence for petitioner’s motivation to combine is a single paragraph from the declaration of its expert which merely parrots the words of Petition. This is not evidence of a motivation to combine. *See* 37 C.F.R. § 42.65(a).

Even assuming a motivation, the Petition is bare as to how the proposed combination teaches or suggests the required elements of the limitation. Petitioner simply argues that “Crump teaches that microcode in the CPU 40, such as a ‘Save CPU State Routine,’ saves the state of the CPU 40, as is known to those skilled in

the art, a special CPU state save area in the segment E000H data structure, which comprises a stack.” Petition at 44-45 (citing Ex. 1008 at 37:11-33, 22:36-41, 37:47-48; Ex. 1003 at ¶ 335). None of the material in Petitioner’s string cite teaches the requirements of limitation [17.I] / dependent claim 4, and Petitioner does not attempt to explain the cited material in the Petition.

16. Dependent Claims 5, 7, 12, 15, 16, 20, 22, 27, 30, And 31.

Claims 5, 7, 12, 15, and 16 all depend from “the microcontroller according to claim 1[.]” See Ex. 1001 at 19:40-20:48. Claims 20, 22, 27, 30, and 31 all depend from “the microcontroller according to claim 17[.]” See *id.* at 21:23-22:47. Since Petitioner has not demonstrated that claim 1 or claim 17 are rendered obvious over the combination of Chung and Crump, *see supra* IV.1-IV.15, the Petition fails as to these claims that depend from claims 1 and 17.

V. THE BOARD LACKS AUTHORITY TO RULE ON THE PATENTABILITY OF THE CHALLENGED CLAIMS OF THE ’575 PATENT.

The Board should not institute trial because Administrative Patent Judges (APJs) are unconstitutionally appointed. See *Lucia v. SEC*, 138 S. Ct. 2044, 2049 (2018); *Masias v. Sec’y of HHS*, 634 F.3d 1283, 1294–95 (Fed. Cir. 2011); *Free Enter. Fund v. Pub. Co. Accounting Oversight Bd.*, 561 U.S. 477, 489, 496-498 (2010); *Edmond v. United States*, 520 U.S. 651, 662–65 (1997); *Freytag v. Commissioner*, 501 U.S. 868, 873 (1991); *see also Arthrex, Inc. v. Smith &*

Nephew, Inc., 941 F.3d 1320, 1325 (Fed. Cir. 2019).

APJs have the power to revoke patent rights, but there is no review of their decisions by constitutionally appointed principal officers. The Federal Circuit, in *Arthrex*, attempted to cure this constitutional defect by severing a provision of the Patent Act that applied Title 5's removal protections to APJs. *Arthrex*, 941 F.3d at 1325. Supreme Court and Federal Circuit precedent, however, demonstrates that the solution advanced in *Arthrex* is insufficient because it does not give a constitutionally appointed principal officer the power to review APJ decisions. *See, e.g., Lucia*, 138 S. Ct. at 2049; *Masias*, 634 F.3d at 1294–95; *Free Enter.*, 561 U.S. at 489, 496–498; *Edmond*, 520 U.S. at 662–65; *Freytag*, 501 U.S. at 873. Thus, APJs remain unconstitutionally appointed.

Congress has the power to remedy the constitutional defect, not the courts. Congress could give a constitutionally appointed principal officer the power to review APJ decisions or require that APJs be appointed by the President, with the advice and consent of the Senate. *See Arthrex*, 941 F.3d at 1327. Regardless of the path forward chosen by the legislative branch, *inter partes* review remains unconstitutional. The petition must be dismissed.

VI. CONCLUSION.

For the foregoing reasons, the Petition should be denied.

Date: January 3, 2020

/Jing H. Cherng/

Jing H. Cherng

Reg. No. 68,144

Counsel for Patent Owner

**CERTIFICATE OF COMPLIANCE WITH TYPE-VOLUME
LIMITATION, TYPEFACE REQUIREMENTS, AND
TYPE STYLE REQUIREMENTS**

I certify that the foregoing document complies with the type-volume limitation of 37 C.F.R. § 42.24(a) and contains 12,799 words based on the word count indicated by Microsoft Word, excluding those portions exempted by the rule, plus words in drawings created by the Patent Owner or as annotations added by the Patent Owner to images reproduced in this document.

Date: January 3, 2020

/Jing H. Cherng/

Jing H. Cherng

Reg. No. 68,144

Counsel for Patent Owner

CERTIFICATE OF SERVICE

It is certified that a copy of the foregoing has been served on Petitioner via electronic mail transmission addressed to the person(s) at the address below:

Michael B. Ray
mray-PTAB@sternekessler.com
Trent W. Merrell
tmerrell-PTAB@sternekessler.com
Michael D. Specht
mspecht-PTAB@sternekessler.com
Jonathan Tuminaro
jtuminar-PTAB@sternekessler.com
PTAB@sternekessler.com.

Date: January 3, 2020

/Jing H. Cherng/

Jing H. Cherng

Reg. No. 68,144

Counsel for Patent Owner