

A Low-power Design Method Using Multiple Supply Voltages

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Abstract

We present a low-power design method that utilizes the multiple supply voltages. The proposed method reduces the power consumption of random logic circuits by 47% on the average, with up to 15% area overhead, by the combination of "Clustered Voltage Scaling (CVS) scheme" and "Row by Row optimized Power Supply (RRPS) scheme". By the CVS scheme, the optimal netlist, that uses the minimized number of the level converters and the maximized number of the low Vdd gates under the timing constraints, is generated. To avoid the wiring resource consumption and the increase of the interconnect delay caused by the layout constraints of the multiple-supply-voltage design, a new power bus wiring scheme called "RRPS scheme" is proposed. The proposed method is applied to a media processor chip MpacTM and achieved the above mentioned results. In this paper, the emphasis is put on the interrelation between the generation of the two-supply-voltage netlist with the CVS scheme and the layout technology, such as the power supply scheme and the placement of the multiple-supply-voltage gates. The clocking scheme for the multiple supply voltages is also discussed.

1. Introduction

The power consumption of CMOS circuit consists of the following two factors. One is the dynamic power consumption by charging and discharging capacitive load [1]. The other is the static power consumption by leak current. In these two factors, the dynamic power consumption is dominant for the CMOS circuit and it is effective to scale down the supply voltage for reducing the power consumption. However, it is difficult to keep the circuit performance while reducing the supply voltage of the circuit.

To solve this problem, the Clustered Voltage Scaling (CVS)[2] [3] scheme has been proposed. The CVS

method reduces the power supply voltage of the non-timing critical parts of the circuit, while the power supply voltage of the timing critical parts of the circuit is kept. With the CVS method, the circuit performance on the critical path is expected not to be degraded, or we will not sacrifice the circuit performance to reduce the power dissipation.

By conventional layout method, the original circuit is partitioned into two sub-circuit groups or the layout blocks. One is supplied with the reduced supply voltage and the other is supplied with the original one. The problem with the conventional method is the difficulty in keeping up the performance of the original circuit. The interconnect delay caused by the long interconnections between the original supply voltage circuit block and the reduced one is unacceptable in the deep-sub micron design. A new layout method for the CVS structured circuits is required to reduce the interconnect delay, that can handle a mixture of the low voltage gates and the original voltage gates in a block. A new power bus scheme and placement method for the multiple-supply-voltage circuits should be established for minimizing the wiring resource consumption and assuring the performance.

In this paper, we propose a novel multiple power supply scheme, "Row by Row optimized Power Supply (RRPS) scheme", which provides different supply voltage to each cell row. With the RRPS scheme, we propose the placement method of the multiple-supply-voltage gates. Because of high percentage of the power consumption at the clock system in a LSI chip, we also propose the low-power clocking scheme that uses the multiple supply voltages. In this scheme, the low supply voltage is given to the clock buffer cells and all the flip-flops. Level converters are inserted at the interface with the circuit of the original voltage. We show the effectiveness of our approach by applying to the media processor chip MpacTM.

2. General Design Flow

The general design flow of the proposed low-power design method with the multiple supply voltages is shown in Fig.1.

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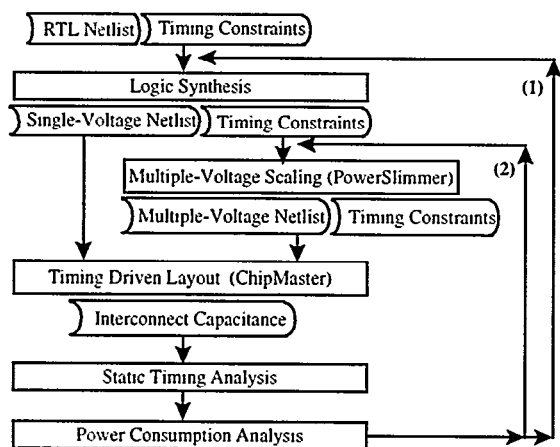


Fig.1 General design flow

There are two design loops. One is the ordinary timing driven design flow[4] between a logic synthesis and a layout which is labeled as (1) in Fig.1. The other is the proposed low-power design flow using the multiple supply voltages which is labeled (2). The input data of our low-power design is the gate-level netlist that satisfies the timing requirement of the circuit with the original supply voltage.

In Fig.1, the PowerSlimmer partitions the circuit into two sub-circuits operated at the original voltage and the low voltage under the timing constraints. The PowerSlimmer forwards the multiple-voltage netlist and the timing constraints to the ChipMaster, a in-house standard cell layout tool. The ChipMaster places the multiple-supply-voltage circuits, generates the RRPS scheme and creates the multiple-supply-voltage clock scheme.

The ChipMaster back annotates the estimated interconnect capacitance based on the placement result to the PowerSlimmer. Using the back annotated information, the PowerSlimmer re-optimize the multiple-supply-voltage netlist. The ChipMaster takes the re-optimized netlist and performs the layout again.

3. Structure Synthesis with Multiple Supply Voltages

The Extended architecture of the CVS which we call ECVS[5] is shown in Fig.2. The PowerSlimmer generates the ECVS structured circuit from a gate-level mapped netlist. Let the "LC" be a level converter, "CL" be a combination logic and "F/F" be a flip-flop in Fig.2. The level converters are inserted between the circuits operated at the low voltage level "VDDL" and the original voltage level "VDDH" to adjust the signal voltage level. The PowerSlimmer estimates the power reduction by replacing the VDDH cells with the VDDL

cells and the power increase by inserting the level converters. If there is some power decrease, the PowerSlimmer accepts the replacement of the supply voltage level of the circuit. Then the PowerSlimmer generates the optimum multiple-supply-voltage netlist with the minimum number of level converters.

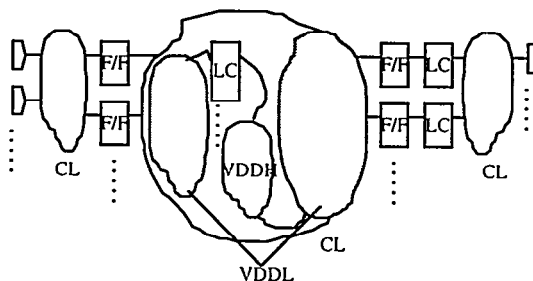


Fig.2 Extended-CVS(ECVS) method

4. Row by Row optimized Power Supply (RRPS) Scheme

We defined power supply busses using the RRPS scheme on the chip as shown in Fig.3. The two different supply voltages, VDDL and VDDH, are given to the internal logic through the power ring that runs inside of the I/O area. The internal logic contains several random logic modules and hard macros. The power supply busses that run between the modules and the macros are connected with the power ring. There are several additional power busses that cross the cell rows in the vertical direction in each module. These power busses are connected to the power busses that runs through the cell rows in horizontal direction. The RRPS scheme can vary the supply voltage level of each cell row. We prepared the VDDL cell library which has the same layout pattern as the one of the conventional VDDH cell with the same function.

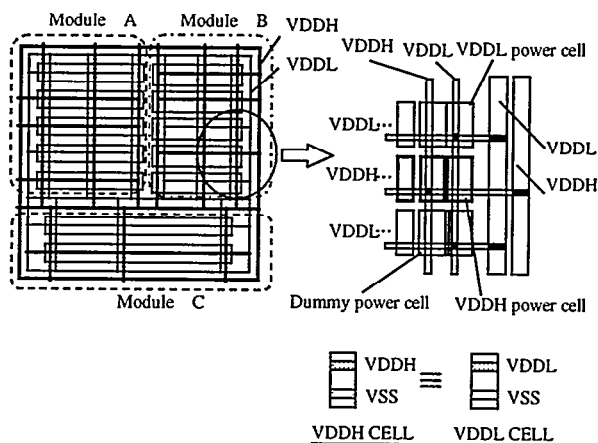


Fig.3 Row by Row optimized Power Supply (RRPS) Scheme

5. Physical Layout with Multiple Supply Voltages

The design flow of the physical layout for the proposed method is shown in Fig.4. The input data is the gate-level multiple-supply-voltage netlist generated by the PowerSlimmer and the timing constraints for each module.

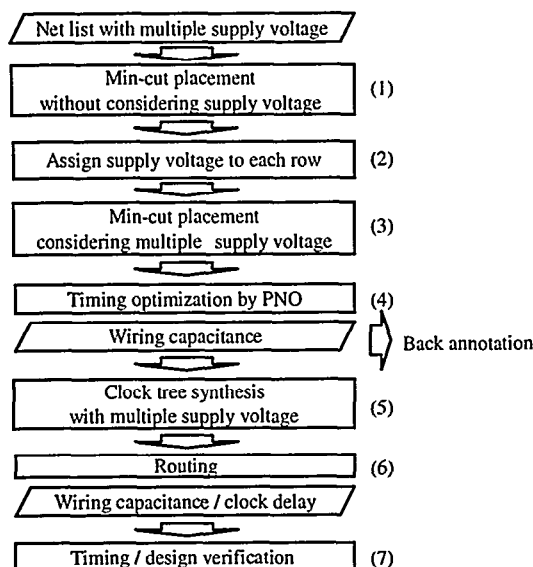


Fig.4 Physical design flow using multiple supply voltages

The ChipMaster places cells without considering voltages (see Fig.1(1)). This placement step is aimed to obtain the placement result of the minimum wire length with the netlist generated by the PowerSlimmer. Fig.5 shows the example of the min-cut placement process and its result.

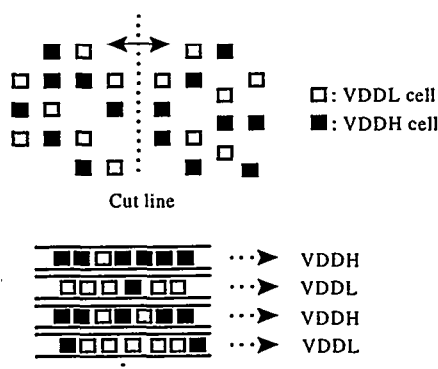


Fig.5 Generation of RRPS scheme

In the step (2) of Fig 4, the power supply to each row is determined by using the placement result

generated in the step (1). Basically, the cell row where the VDDH cells occupy the larger part of the cell area on the cell row is determined as the VDDH cell row (see Fig.5). In this way, the ChipMaster determines the supply voltage to all the cell rows in the region where a module is placed. This procedure is applied to other modules to generate the RRPS scheme on a chip. In this step, it is important to minimize the distance between a cell position of the step (1) and the closest cell row which has the same supply voltage with the cell, because the distance becomes the increase of the wiring length of the next step (3).

With the RRPS scheme, the ChipMaster places all the cells considering the supply voltage level to each cell (step (3)). The similar min-cut placement process to (1) is performed again. However, the assignment of a cell to a cell row is different from the process of (1).

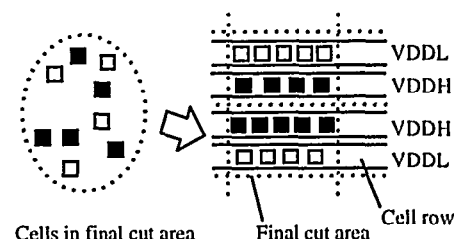


Fig. 6 Placement of multiple supply voltages

In the multiple-supply-voltage placement, the geometrical restrictions are applied to all the cells to place them on the valid voltage cell row. In the final cut area of the min-cut placement, the ChipMaster finds out the valid location for the cell corresponding with the supply voltage. Fig. 6 shows the example of the placement result of the multiple supply voltages.

Using the combination of the above steps, the ChipMaster places the VDDH cells and the VDDL cells on the critical path close together and controls the increase of the wire length between the VDDH cells and the VDDL cells. This is very important to controls the increase of the interconnect delay between the original supply voltage circuit and reduced one, and minimize the wiring resource consumption of the multiple-supply-voltage layout.

The timing violations remained after the placement are eliminated by the post-placement netlist optimizer (PNO[6]). The PNO performs the gate re-sizing or replaces cell model which has different gate width and has the same function to reduce critical path delay. If the critical path delay is reduced, the PNO accepts the replacement and the timing violation is removed. After

all the violations are removed, the ChipMaster back annotates the interconnect capacitance by using estimated wiring route[7] to the PowerSlimmer.

The routing process is the same as the ordinary design.

6. Clock Scheme with Multiple Supply Voltages

Fig.7 shows the clock scheme using multiple supply voltages. The proposed method creates the clock tree[8] on the RRPS scheme. We reduce the supply voltage level of all the flip-flops to the low voltage level. The proposed clocking scheme is created by using the buffer cell which operates at low voltage instead of the buffer cell which operates at the original voltage.

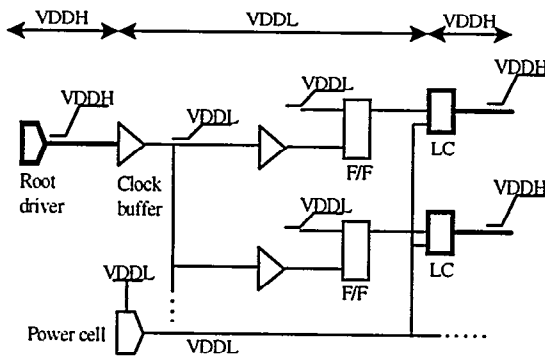


Fig. 7 Clock scheme with multiple supply voltages

The root driver operated at the VDDH generates the clock signal of the voltage swing of the VDDH level. This voltage swing is reduced to the VDDL level through the first clock buffer cell which operates at the VDDL. The low voltage swing of the clock signal propagates through the clock tree to the flip-flops that also operates at the VDDL.

The level converters are inserted where the flip-flops connect with the VDDH circuit as shown in Fig.7. A circuit example of the level converter is shown in Fig.8. The level converter needs both of the power supplies of the VDDH and the VDDL. We placed the level converter in the VDDH cell row to supply the VDDH. The VDDL is supplied only to the small inverter in the cell. We prepare the additional power pin in the level converter to supply the VDDL. The VDDL is provided via the power line that is connected with the power cell placed on the VDDL cell row. The VDDL power lines are routed by the wiring step of the common signal nets. However, we

restrict the number of the level converters that connect to a power cell to keep the performance of the level converters and to avoid the electromigration of the wire.

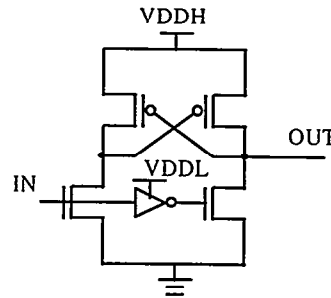


Fig.8 Example of level Converter

7. Experimental Results

7.1 Application Example

We applied the proposed method to the MpackTM media processor chip. The media processor provides MPEG2 decoding, real-time MPEG1 encoding, personal video conferencing, 28.8kbps fax / modem and audio / sound functions. The operating voltage is 3.3V and the main clock frequency is 75MHz. We applied the proposed method to the chip by using low level voltage 1.9V as the VDDL using an external voltage supply. In the layout, all the VDDL cell libraries are the same as the ones of the VDD cells except the level converter. The proposed method is applied to the combination logic circuits that contain 48K cells and 52Knets. The original chip size is 7.8X6.8mm².

7.2 Experimental Results

Fig.9 shows the effectiveness of the power reduction concerned with the random logic by the proposed method. The amount of the power consumption of the graph is the sum of the seven random logic modules. The left side bar corresponds to the power consumption of the original chip, while the right side bar corresponds to the power consumption of the proposed method. The total power reduction is about 123mW, i.e. 47% reduction from the original chip. We estimate the power consumption of the layout result by using the PowerMillTM simulation.

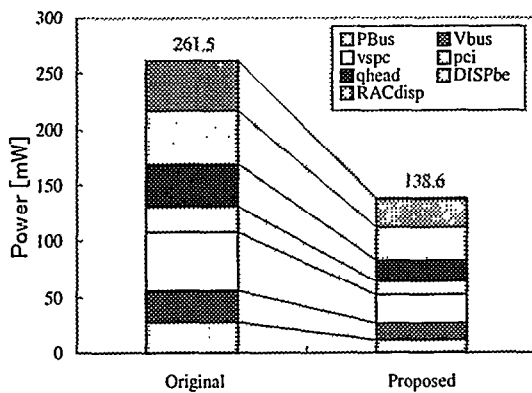


Fig.9 Effectiveness of total power reduction

Fig.10 shows the effectiveness of the power reduction of the clock system by using the proposed method. The left side bar is the original power consumption of the main clock system. This power consumption is the sum of the internal power consumption of the flip-flops, interconnects, buffer cells and the root driver.

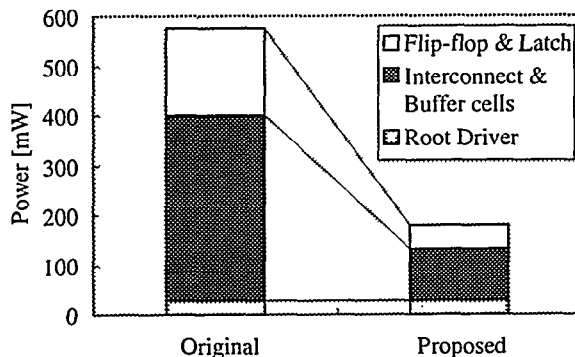


Fig. 10 Effect of power reduction of clock system

As shown in Fig.10, the power consumption of the flip-flops, interconnects and the buffer cells occupies a large part of the power consumption of the clock system. It is effective to reduce this portion of the power consumption. The proposed method aims to reduce this portion of the power consumption. The original power consumption of the main clock system was reduced by 68.9% by the proposed method. Although the clock delay was increased to 2.8nsec from 2.0nsec, the clock skew was almost the same as the original layout that is 430psec. Because the RRPS scheme has enough place area for the low-voltage buffer cells, it is easy to balance the clock

delay of each flip-flops by the clock tree synthesis. According to our static path analysis, the increase of the clock delay by the multiple-supply-voltage layout did not degrade the circuit performance.

The area overhead of the multiple supply voltages layout of this chip is 15% on the average of all the modules. The chip size increased by 7% and it becomes 7.8X7.3mm². There are three major factors that affect the chip area by using the proposed multiple-supply-voltage design. One is the constraint of the cell placement. We must place the VDDH cells and the VDDL cells on different cell rows. The second factor is the increase of the number of the cells, especially due to the inserted level converters. And the third is the wiring area of the VDDL power line.

The proposed method provides different voltage to each cell row to minimize the increase of wiring length between the VDDH circuit and the VDDL circuit. This allows us possible to keep the circuit performance the same as the original one with a small area overhead. We can make the further improvement about the increase of the wiring length by developing the layout model that allows to use different supply voltages in a cell row.

Fig. 11 shows the increase of the cell count in each random logic module. The left side bar is the number of cells in the original and the right side one is the number of cells that applied the proposed method. The increase is mainly caused by the insertion of the level converters. Particularly, the latches which have plural outputs and located on a critical path increase the number of the level converters.

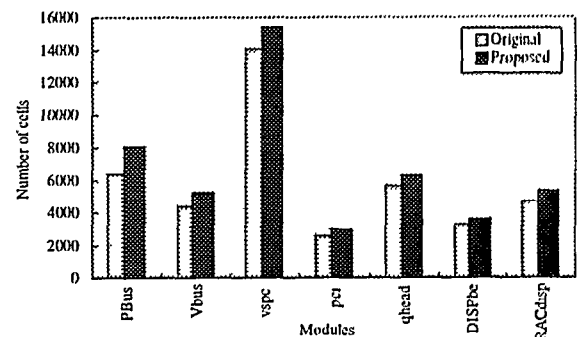


Fig. 11 Increase of cell count

This is the reason why the number of cells in the modules "PBus" and "VBus" have increased. This increase of cell area will be small by creating the combined cell of the latch and the level converter.

The area overhead by the increase of the power line is the minor factor, because our layout model does not need the extra power line in a cell. Each cell library has only

one power line of the VDDH or the VDDL.

The turn around time of each layout step such as the power routing, placement of the multiple-voltage-circuit and routing is almost the same to the ordinary layout. But the total TAT will increase because the proposed method has more layout steps than the ordinary layout. We can make the overhead of the TAT of the multiple-supply-voltage layout be small by the automation of the design flow.

Fig. 12 shows the final layout result of the entire chip. The proposed method has been applied to the highlighted seven modules.

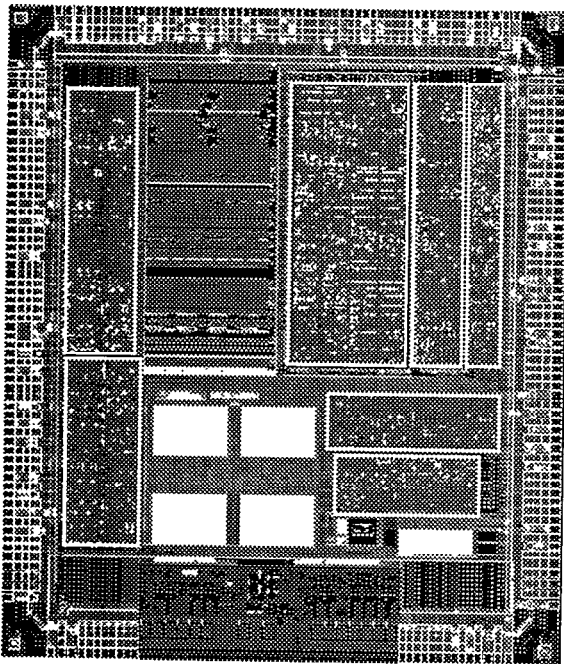


Fig. 12 Layout result

8. Conclusions

We have presented the low-power design method that utilizes the multiple supply voltages. The proposed method has reduced the power consumption by 47% on the average, with up to 15% area overhead. We have proposed a novel multiple power supply scheme, the RRPS scheme, which provides different supply voltage to each cell row. The proposed layout method controls the increase of the wire length between the original voltage circuit and the low voltage circuit of the CVS structured circuit. Our design strategy controls the increase of interconnect delay and does not degrade the original circuit performance. The proposed method also controls the increase of the wiring resource consumption of the

multiple-supply-voltage design. We applied the proposed method to the media processor MipactTM and achieved the above mentioned results. We have also shown that the power reduction of the clock system with the multiple supply voltages is very effective for low-power design. The RRPS scheme allows to place a low-voltage buffer cell at the balance point of the clock delay and it keeps the original minimum clock skew.

We have discussed that the additional cell library, *e.g.* the combined cell of a latch and a level converter is effective to reduce the area overhead of the proposed method. The TAT of each step of the design does not increase compared with the one of the ordinary design.

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