

Low Cost On-Die CMOS Distributed Voltage Regulation for Microcontrollers

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Abstract

A novel concept in on-die voltage regulation for power delivery is described. In contrast with traditional voltage regulation, a distributed architecture has been designed and implemented in a CMOS process. Distributed regulation employs multiple regulators distributed across the integrated circuit design placed according to the power consumption requirements of the power grid in the design. The core on-die de-coupling requirement is seen to reduce very significantly both due to the reduction in the operating voltage and correspondingly the operating currents as well as to the minimization of voltage differentials due to local regulation. The inherent regulating action of NFET-source follower regulating stages placed close to the load circuits allows for fast transient response. The design is scaleable and has low implementation cost primarily due to the reduction in de-coupling requirements.

1. Introduction

A transfer of a design from one process to another of finer geometry and lower voltage tolerance for a microcontroller brings about a smaller die, better performance and lower power consumption. The price in terms of design effort is that the shrunk part is expected to fit into the original system design and thus work with a higher voltage input than that which the new process tolerates. Hence the need for a voltage regulation system designed in the new process that can step down the input power supply voltage to the level that is acceptable for the new process. Prior efforts in this direction have resulted in on-package solutions that successfully addressed this requirement using discrete components for the processors. This paper presents a CMOS solution for on-die regulation as implemented on versions of the Intel 16-bit high performance, low cost microcontroller family.

Low cost was a primary concern for this design. A large single voltage regulator design would result in significant voltage differentials between different portions of the chip in addition to claiming large amounts of die area in the de-coupling requirement inherent in the structure. Transient VCC disturbances can be minimized in an on-package de-coupling solution that also has very minimal loop inductance, but that is not an option for very low cost microcontrollers. A distributed scheme blends in well with prior power distribution structures reducing the total area cost in the implementation of the regulator. Both linear and

switching regulators, were considered. Power consumption is reduced in both cases due to reduced total chip current that scales with the reduced operating VCC. Response to transients with the minimum de-coupling capacitance being an important factor, a linear regulator with better transient response was used as the basic regulator cell in the system.

Other considerations in the regulator design included the ability to power-down to a low (sub-10 microamperes) I_{pd} while maintaining internal VCC, transparency of the regulator to I_{DDQ} (static quiescent current) measurements and a BYPASS mode that would allow the chip to be used in a low-voltage system. A burn-in mode that would allow simultaneous burn-in of both the regulator and the load logic circuitry was also included in the system.

2. Distributed Regulation

Integrated circuits typically derive power from all sides of the chip package through multiple power pins. This minimizes the $L \cdot di/dt$ and the IR losses by distributing the chip current among the multiple impedance pathways. A distributed regulation system builds on the very same concept and consists of multiple "small" regulators feeding into the internal power bus structure and fits in very well with typical microcontroller power bus structures in low cost processes with lesser number of layers of metal.

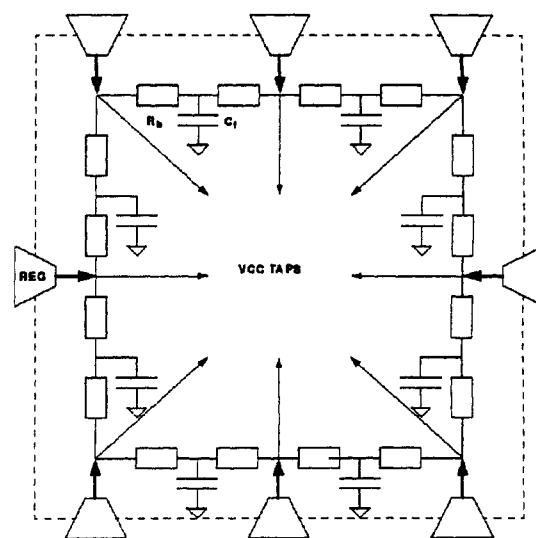


Figure 1: Distributed Regulation

Effective de-coupling of the input VCC is necessary, particularly since the regulation system isolates the input VCC from the internal on-die power distribution capacitance. This is an issue in such designs, since this de-coupling may not be feasible for reliability and cost reasons within the die. On-package de-coupling, such as that which is built onto an Organic Land Grid Array package mitigates this issue.

The distributed regulation scheme (figure (1)) consists of a number of small linear regulator placed at selected junctions on the core power (VCC) and the peripheral power (VCCP) rings. Each regulator is capable of an average current computed from the anticipated worst case total average current divided by the number of regulators and a peak transient current based on the maximum droop tolerated. With judicious placement, the regulators divide the total chip current approximately evenly, as shown by simulation results on a power structure model for the design. The regulators derive a reference from a single source and thus attempt to maintain the power bus at the same voltage.

The most significant advantage of the distributed regulation system is the minimization of the voltage differential between points on the power structure along with the minimization in the de-coupling requirement as compared with a single regulator design. Other advantages include good response to transients at all points on the power structure, distributed regulator power dissipation, ease of implementation and close similarity to the original power distribution scheme..

3. Linear Voltage Regulator

The basic linear regulator consists of a voltage reference, an error amplifier and a series pass element that connects in series with the input and the output and is controlled by the output of the error amplifier. The voltage reference output is compared with a feedback level derived from the output of the regulator by the error amplifier, which then develops the drive signal for the series pass element. The voltage regulator implementation in consideration utilizes a textbook band-gap CMOS reference design.

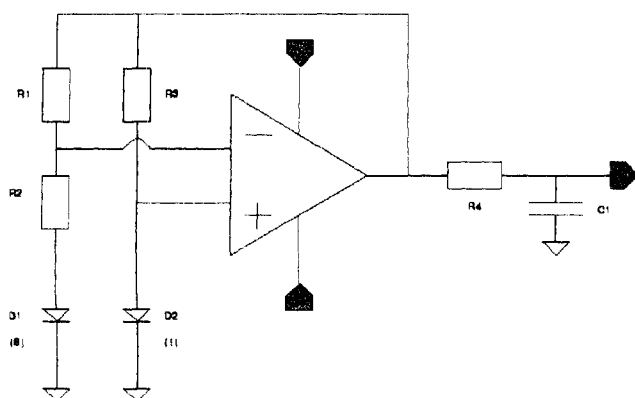


Figure 2: Band-gap Reference Generator

The operational amplifier used in the reference has additional circuitry to passively step the input VCC down to the core voltage requirement. The reference exhibits excellent PSRR and temperature independence with a 1% variation in output under all combinations of -15°C to 125°C and $\pm 10\%$ VCC input as indicated by circuit simulations. It also shows less than 2.6% variation in output over realistic process based variations under the above mentioned conditions. An RC filter at the output with a 40dB attenuation at 50 assists in improving the PSRR at high frequencies. The reference is scaled up to the desired VCC in a scaling amplifier cell that also has a facility for switching the scaled reference to a higher value when voltages near the burn-in level are sensed at the input. The scaling circuitry also includes an RC filter and displays a PSRR better than 50 dB for all worst-case noise voltage, and temperature conditions. A representative diagram is shown in figure (3). For the implemented design, under normal conditions, the input pins see voltages between 4.5 and 5.5 volts and the scale-up circuit develops 3.3 volts at it's output. When an input of approximately 6.0 volts is seen on the VCC pins, the additional resistance path for the gain computation switches on and raises the output reference level to the burn-in voltage requirement.

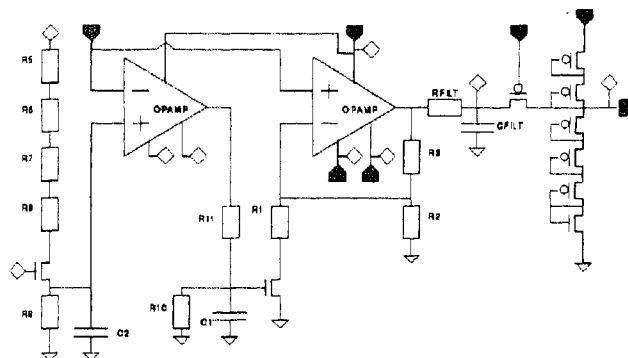


Figure 3: Gain Switched Scale-Up Circuitry

Each regulator cell (figure (4)) comprises of a differential error amplifier, pair of series pass transistors (NFET for normal regulation and a PFET for BYPASS) and a passive bias ladder that biases the NFET gate at a value proportional to the VCC. The error amplifier output overrides this bias in the regulating mode. The error amplifier is an NFET input differential amplifier with active PFET loads.

In the normal regulation mode, the error amplifier and the series pass N-device form a voltage source follower configuration that maintains the output of the regulator. The BYPASS mode is entered into in this implementation by grounding the analog power supply pin that powers all the regulator control circuitry. The power supply to the reference and control circuitry of the regulator system is derived from this pin, grounding it therefore disables normal regulation. The grounded pin is sensed through a line that feeds into the gates of the PFET devices and therefore allows the input voltage (in BYPASS) to pass through with minimal attenuation to the power structure.

The regulators are seen to display excellent transient response. The **response delay** of the basic regulator cell (an indication of the transient response capability) is measured as the time from the initiation of a step current load to the time the regulator supplies all of the load current required. Simulated with a 3.2Ω bus resistance and a 400pF power bus capacitance without loop inductance, it was found to be about 4.7nS in this particular implementation. The properties are summarized in the result section.

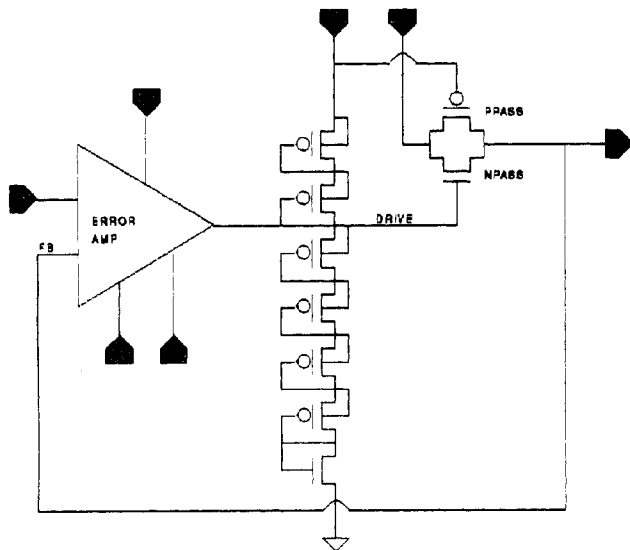


Figure 4: Basic Regulator

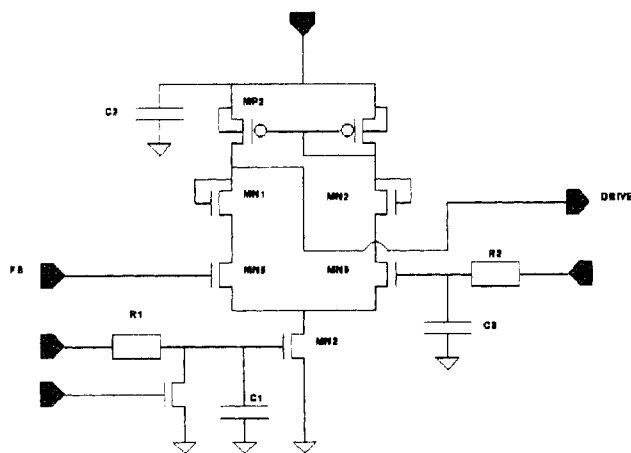


Figure 5: Regulator Error Amplifier

4. Power-down

A power-down signal is transmitted to all the analog circuitry of the regulation system to dislocate the active circuitry from both VCC and GND, and this facilitates the maintenance of the gates of the N-Pass devices at the bias value as determined by the low current bias ladders. In effect, the power-down functionality disables the active regulation circuitry and allows the distributed regulators to behave as passive pull-ups for the power structure. The passive regulation circuitry overlaps the active regulation.

The total power-down current expected in this implementation is about 25 microamperes more than the normal chip I_{pd} for the Regulation-ON mode, and is the same as the normal I_{pd} for the BYPASS mode.

5. Results

Simulations were carried out for each of the blocks designed for the regulation system independently to ascertain their stand-alone performance, and results were obtained for a representative power distribution model of the full-chip design with a fully integrated system including all components of the distributed regulator. The complete model included a core power bus (VCC), a peripheral power bus (VCCP), a core ground bus (VSS) and a peripheral ground bus (VSSP). These were modeled as rings of resistances and capacitance, inductance's for each power input pin, inductance's for each ground pin, and loads simulating worst-case loading conditions distributed along the power buses in congruence with their placement in the actual chip layout.

Line regulation was measured with the input voltage varying $\pm 10\%$ at operating frequencies ranging from 0 to 150 MHz. Load regulation tests were conducted on the basic regulator cell and the fully integrated model using only transient loads, both anticipated as well as simulated through clocks fed to buffers approximately as is expected on the chip. Tests on load regulation were carried out under recurrent maximum transient load scenarios that are rarely seen in practice for the design and exceed the anticipated loading by more than 100%.

Table 1: Test Load Scenario

Regulator	$I(av)$, ma	$I(pk)$, ma
1	41	92
2	27	55
3	41	84
4	30	70
5	27	50
6	46	104
7	44	78
Total I	256	N/A

Table 1 depicts the loading conditions for seven regulators under test in the integrated power structure model for the 8XC296SB measured at TYPICAL, 5.0V and 25°C. Table (2) displays the voltages measured on the junctions of the regulators and the power bus under the load shown above. The total loading of the regulators was significantly more than the anticipated loading on the chip. The loading circuits were concentrated at junctions on the power bus and distributed according to the side of the chip they were positioned in, and hence corresponded to an extremely severe load.

A 10% transient droop of VCC for a duration of less than 4 nS at each worst-case transient load time point was observed in simulation; the consequences on internal signal rise and fall times were evaluated and addressed. The trade-off is in the amount of on-die de-coupling versus the impact of power supply non-idealities on signal integrity for both intra-die and off-chip signals.

Table 2: Regulator-Power Bus Junction Voltages

Reg.	5V, 25°		4.5V, 125°	
	Ave., V	Dip	Ave., V	Dip
1	3.31	2.95	3.04	2.70
2	3.32	2.92	3.06	2.76
3	3.31	2.96	3.03	2.70
4	3.29	3.02	3.01	2.86
5	3.34	2.96	3.07	2.74
6	3.32	2.92	3.02	2.70
7	3.29	3.05	3.00	2.80

6. Silicon Results

Silicon results correlated well with the circuit modeling. The power supply voltage was observed to be within $\pm 2\%$ of the desired VCC, with noise contained within $\pm 10\%$ as required. Issues observed included voltage droop during recovery Idle, Stand-by and Power-Down modes indicating further improvements in this power delivery system design.

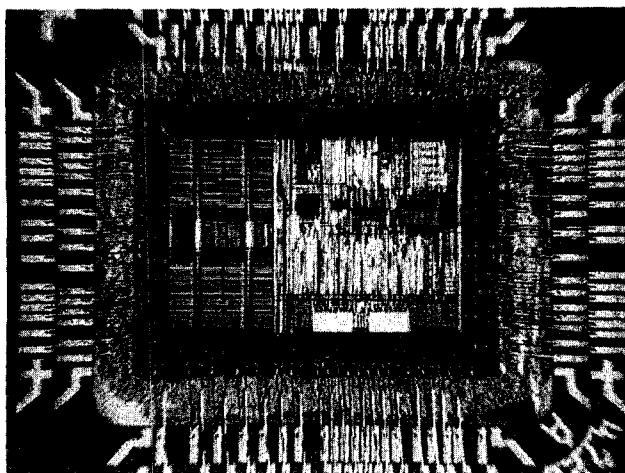


Figure 5: Die Photograph

7. Summary

The concept of On-Die Distributed Regulation employing Multi-Mode CMOS Regulators [1] is believed to be a unique implementation of a voltage regulator on silicon. Prior designs known to the authors have been either on-package or on-die BiCMOS, and the all-CMOS design allows for implementation on processes of much less cost.

Simulation results show good agreement with the expectations of uniform power structure voltage values and good transient response – as well as with measured results on silicon; voltage dips greater than 10% on the power structure are seen to occur only under unrealistic transient load scenarios coupled with severe operating conditions.

The system is scalable; it is believed that this design can be easily adapted to larger/lesser chip current requirements. It is also expected that the design can be ported to future finer dimension lower voltage processes with minor circuit modifications.

8. Acknowledgments

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9. References

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