

**IN THE UNITED STATES DISTRICT COURT
FOR THE WESTERN DISTRICT OF TEXAS
WACO DIVISION**

COLLABO INNOVATIONS, INC., a
Delaware Corporation

Plaintiff

v.

QUALCOMM INCORPORATED and
QUALCOMM TECHNOLOGIES, INC.,
both Delaware Corporations

Defendants

CIVIL ACTION NO. 6:24-cv-00472-ADA

**DEFENDANTS QUALCOMM INCORPORATED AND QUALCOMM
TECHNOLOGIES, INC.'S OPENING CLAIM CONSTRUCTION BRIEF**

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2	U.S. Patent No. 7,930,575
3	Transcript excerpts of <i>Markman</i> Hearing held August 23, 2019 in <i>Collabo Innovations, Inc. v. Advanced Micro Devices, Inc.</i> , No. 1:18-cv-00552 (W.D. Tex.), ECF 8
4	Transcript of supplemental <i>Markman</i> Hearing held June 30, 2023 in <i>Collabo Innovations, Inc. v. Advanced Micro Devices, Inc.</i> , No. 1:18-cv-00552 (W.D. Tex.), ECF 91
5	Claim Construction Order, <i>Collabo Innovations, Inc. v. Advanced Micro Devices, Inc.</i> , No. 1:18-cv-00552 (W.D. Tex.), ECF 93
6	Patent Owner's Preliminary Response (Paper 9) in <i>Advanced Micro Devices, Inc. v. Collabo Innovations Inc.</i> , IPR2019-01523 (P.T.A.B. Jan. 3, 2020).
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10	Excerpts from IEEE 100, The Authoritative Dictionary of IEEE Standard Terms (7th Ed. 2000)
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14	Revised Claim Construction Order and Memorandum in Support Thereof, <i>Sable Networks v. CloudFlare</i> , 6:21-cv-00261-ADA, Jan. 25, 2024

I. INTRODUCTION

This Court previously construed certain terms of U.S. Patent No. 7,930,575 (“the ’575 Patent”) in the *Collabo Innovations, Inc. v. Advanced Micro Devices, Inc.*, No. 1:18-cv-00552 (W.D. Tex. July 2, 2018) (“*Collabo v. AMD*”). While that litigation was ongoing, Advanced Micro Devices, Inc. (“AMD”) filed two *inter partes* review (IPR) petitions with the Patent Trial and Appeals Board (“PTAB”) challenging claims of the ’575 Patent that were asserted against AMD in that case, and are also asserted in this case. Collabo submitted detailed Patent Owner Preliminary Responses (“POPRs”) opposing both IPR petitions. In its POPRs, Collabo clarified the scope of its invention and advanced constructions for various claim terms. Because of the timing of the PTAB proceedings, Collabo’s statements to the PTAB were not part of claim construction briefing in *Collabo v. AMD*; however, they are part of the intrinsic record now.

Before the PTAB, Collabo argued that the claimed “microcontroller” was “a single integrated chip” and not “a set of multiple chips (a ‘chipset’).” In other words, Collabo narrowed the term to a single chip and excluded chipsets from its scope. Similarly, Collabo argued that the claimed “microprogram” was not a generic “program,” but a particular program that runs at the lowest level of hardware and is held entirely within the CPU. The PTAB declined to institute either of the IPR petitions based on the arguments advanced by Collabo regarding the scope of the “microcontroller” term. Qualcomm’s proposed constructions for these two terms seek to hold Collabo to its statements before the PTAB. Such statements are binding and limiting disclaimers of claim scope or, at a minimum, strong intrinsic evidence of the meaning of these claim terms.

Separately, Qualcomm respectfully submits that dependent claims 2 and 8 of the ’575 Patent, which were not at issue in *Collabo v. AMD*, are invalid as indefinite.

II. LEGAL STANDARD

Words of a claim are generally given their ordinary and customary meaning. *Phillips v.*

AWH Corp., 415 F.3d 1303, 1312 (Fed. Cir. 2005). When a patentee unequivocally and unambiguously disavows claim scope during prosecution to obtain or preserve a patent, this constitutes a disclaimer, which “narrows the meaning of the claim consistent with the scope of the claim surrendered.” *Biogen Idec, Inc. v. GlaxoSmithKline LLC*, 713 F.3d 1090, 1095 (Fed. Cir. 2013) (citation omitted). A patentee’s clear and unmistakable statements during an IPR, including those made in a POPR, can form the basis of a binding prosecution disclaimer. *Aylus Networks, Inc. v. Apple Inc.*, 856 F.3d 1353, 1361–62 (Fed. Cir. 2017). Furthermore, even when a patentee’s statement in a POPR does not give rise to a disclaimer, it is nonetheless part of the patent’s prosecution history, *see id.* at 1360–61, and so may be considered during claim construction as it “provides evidence of how the PTO and the inventor understood the patent.” *Phillips*, 415 F.3d at 1317. When a claim’s language “read in light of the specification delineating the patent, and the prosecution history, fail[s] to inform, with reasonable certainty, those skilled in the art about the scope of the invention,” that claim is invalid as indefinite. *Nautilus, Inc. v. Biosig Instruments, Inc.*, 572 U.S. 898, 901 (2014).

III. PROSECUTION AND LITIGATION HISTORY

Collabo filed a complaint in July 2018 alleging that AMD infringed certain claims of the ’575 Patent. The parties submitted Claim Construction briefs in May 2019, and a first *Markman* hearing was held in August 2019. Ex. 3 (*Markman* Tr., *Collabo v. AMD*, ECF 86 (Aug. 23, 2019)). While the IPRs were pending, the case was stayed. When the case resumed, the Court held a supplemental *Markman* hearing, Ex. 4 (Supp. *Markman* Tr., *Collabo v. AMD*, ECF 91 (June 30, 2023)). On July 5, 2023, the Court entered a claim construction order. Ex. 5 (Cl. Constr. Order, *Collabo v. AMD*, ECF 93 (July 5, 2023)). The case settled before trial.

After the first *Markman* hearing, AMD filed two IPR petitions challenging claims of the ’575 Patent. *See* IPR2019-01523 (“*AMD IPR I*”) and IPR2019-01524 (“*AMD IPR II*”). In *AMD*

IPR I, AMD relied on U.S. Patent Pub. No. 2007/0157036 (“Jahagirdar”) as the primary reference, whereas in *AMD IPR II*, AMD relied primarily on U.S. Patent No. 5,390,350 (“Chung”). Collabo filed POPRs opposing AMD’s petitions. In each, Collabo distinguished the asserted prior art—and clarified the scope of the claimed invention—by relying upon several technical dictionaries to define the terms “microcontroller” and “microprogram.” *See* Ex. 6 (POPR, *AMD IPR I*, Paper No. 9); Ex. 7 (POPR, *AMD IPR II*, Paper No. 9). Based on Collabo’s restrictive construction of “microcontroller,” the PTAB decided not to institute either of AMD’s IPR petitions. Ex. 8 (Institution Decision, *AMD IPR I*, Paper No. 18 (Mar. 27, 2020)) at 7, 11; Ex. 9 (Institution Decision, *AMD IPR II*, Paper No. 13 (Mar. 30, 2020)) at 7.

Collabo’s statements to the PTAB limiting the scope of “microcontroller” and “microprogram” were not discussed in the *Collabo v. AMD* supplemental *Markman* hearing on June 30, 2023, and do not appear to have been considered by the Court when issuing its July 5, 2023 order. *See* Ex. 4.

IV. THE ’575 PATENT

A. “microcontroller” (claim 1)

Collabo’s Construction	Qualcomm’s Construction
Plain and ordinary meaning	“a single integrated chip as opposed to a set of multiple chips (a “chipset”)”

Collabo concedes “microcontroller” requires a construction beyond its “plain and ordinary meaning.” In its prior litigation before this Court, Collabo proposed a construction of “an integrated circuit.” Then, before the PTAB, Collabo confirmed even if its construction of “an integrated circuit” were adopted, it would “require the microcontroller to be on a single integrated chip.” Ex. 6 at 18. Collabo further clarified to the PTAB that the claimed “microcontroller” is not a set of multiple chips, a multi-chip system, or a chipset. The PTAB relied on Collabo’s construction of “microcontroller” as a “single integrated chip” and not a chipset and decided not

to institute the IPR petitions on that basis. Collabo is bound by its representations to the PTAB under both the doctrines of prosecution disclaimer and judicial estoppel, and Collabo cannot now evade those representations by seeking a construction of “plain and ordinary meaning.” Qualcomm’s proposed construction reflects Collabo’s explicit, clear, unmistakable, and binding statements.¹

1. Collabo narrowed the scope to “a single integrated chip/not a chipset,” and expressly disclaimed chipsets

“*A single integrated chip/not a chipset*”: Qualcomm’s proposed construction incorporates Collabo’s clear and unmistakable representations to the PTAB that the claimed “microcontroller” is a “single integrated chip/not a chipset.” Ex. 1 at 18 (“Regardless of which construction [of ‘microcontroller’] is used in this proceeding, both constructions require the microcontroller to be on a *single integrated chip*.” (emphasis added)); Ex. 2 at 15 (same). Collabo clearly and unmistakably asserted that its construction of “microcontroller” was limited to a single chip. Ex. 6 at 27 (“Collabo’s construction also requires the ‘microcontroller’ to be a single chip.”).

Intrinsic evidence cited by Collabo in its POPRs describes a “chip” as “[a] small piece of silicon or other semiconductor material on which circuits can be placed,” or “[a] small unpackaged functional element made by subdividing a wafer of semiconductor material. Sometimes referred to as a die.” Ex. 10 (the Authoritative Dictionary of IEEE Standard Terms) at 166. Other technical dictionaries further confirm that a chip is a small piece of silicon, *a.k.a.*, a die. *See* Ex. 11

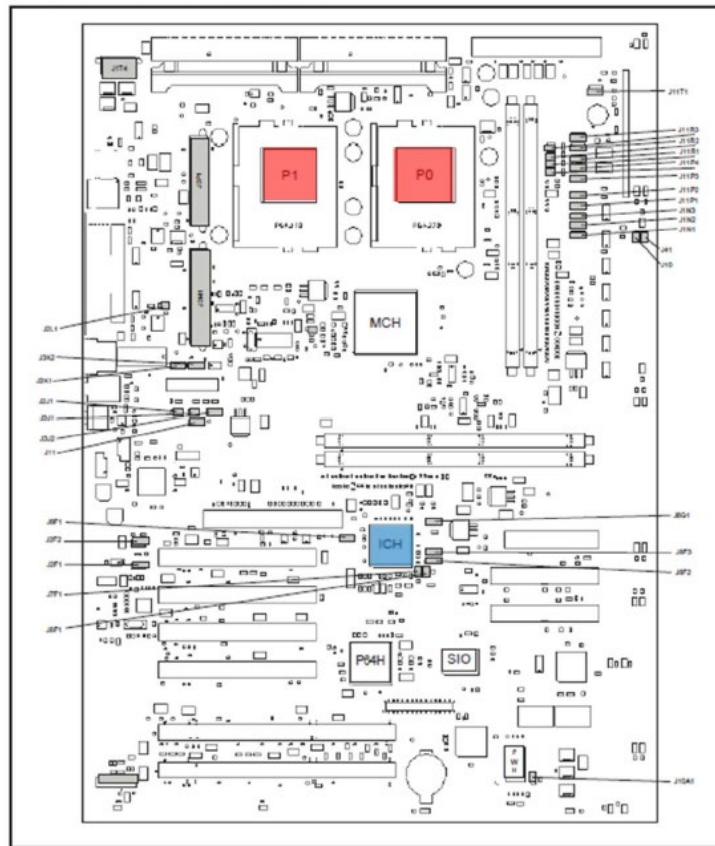
¹ The Court previously construed “microcontroller” as having its plain and ordinary meaning. Ex. 5 at 3. However, as noted, the Court did not have the benefit of Collabo’s statements to the PTAB in considering this construction. Further, Collabo’s proposed construction for “microcontroller” in the *Collabo v. AMD* case was “integrated circuit,” and it stated during the first *Markman* hearing that its own construction limited “microcontroller” to a single chip. Ex. 3 at 46:2–7 (“[T]he chip design you have — used to have the different chips and different circuits that were on a board that have been increasingly integrated *onto a chip*. And this is what we see here in this claim, *an integrated chip* comprising a CPU, a power supply unit, a power supply control unit, an information-holding unit, and a clock generator.”) (emphasis added).

(Comprehensive Dictionary of Electrical Engineering) at 110 (defining “chip” as “a small piece of semiconductor material upon which miniaturized electronic circuits can be built”); Ex. 12 (Modern Dictionary of Electronics) at 113 (“A single piece of semiconductor material (silicon, sapphire, germanium, etc.) containing one or more circuits, usually packaged as a unit.”). As Qualcomm’s expert Dr. Annavaram explains, a person of ordinary skill in the art would have recognized a “chip” to be a single piece of silicon or a die containing the associated circuitry. *See* Ex. 1 (Annavaram Decl.) ¶¶ 31-36.

Collabo then repeatedly argued its claims excluded the prior art multi-chip systems or “chipsets.” Ex. 6 at 23–24 (“As shown above, the ‘board’ *is not* a single ‘chip,’ but rather is a *set of multiple chips (a ‘chipset’)* Because Jahagirdar’s *multi-chip system* is not integrated on a single chip, it does not teach a ‘microcontroller’ under either party’s construction.” (emphases added)); Ex. 7 at 17 (“Chung’s *multi-chip system* is not integrated on a single chip, and thus does not teach a ‘microcontroller’ under either party’s construction.” (emphasis added)).

Collabo’s own annotations to the cited prior art confirm its disavowed claim scope. In opposing AMD’s first IPR petition, Collabo explained that the Jahagirdar reference disclosed a chipset. Ex. 6 at 21. Collabo argued that the evaluation board of Jahagirdar contains multiple chips, *i.e.*, two Pentium III processors and an Intel 840 chipset. *Id.* Collabo pointed out that the Intel 840 chipset itself includes multiple chips, such as, the MCH (Memory Controller Hub), the ICH (I/O Controller Hub), the P64H (PCI 64 Hub), and the FWH (Firmware Hub). *Id.* To make its point unmistakably clear for the PTAB, Collabo annotated the schematic of the evaluation board with two processors shaded red, and the I/O Controller Hub (ICH) of the Intel 840 chipset shaded blue:

Figure 2-1. Evaluation Board Jumpers



Ex. 6 at 23. Collabo argued “the ‘board’ is not a single ‘chip,’ but rather is a *set of multiple chips* (*a ‘chipset’*), with the ICH, MCH, P64H, and FWH as separate chips residing on the board.” *Id.* at 23 (emphasis added). Collabo further stated that “[b]ecause Jahagirdar’s multi-chip system is not integrated on a single chip, it does not teach a ‘microcontroller’ under either party’s construction.” *Id.* at 24; *see also id.* at 16 (“Petitioner’s main problem is that Jahagirdar does not teach that its system resides on a single chip. Thus, it does not teach a ‘microcontroller.’”).

In response to AMD’s second IPR petition, Collabo made similar arguments about Chung. Ex. 7 at 17 (“[Prior art] Chung’s multi-chip system is not integrated on a single chip, and thus does not teach a ‘microcontroller’ under either party’s construction.”). In doing so, Collabo expressly disclaimed a construction of “microcontroller” that includes chipsets or multi-chip systems. *See Spectrum Int’l, Inc. v. Sterile Corp.*, 164 F.3d 1372, 1378–79 (Fed. Cir. 1998)

(“explicit statements made by a patent applicant during prosecution to distinguish a claimed invention over prior art may serve to narrow the scope of a claim” because “[b]y distinguishing the claimed invention over the prior art, an applicant is indicating what the claims do not cover”) (quotation omitted).

2. Because the PTAB relied on Collabo’s narrowing disclaimer in denying institution of AMD’s IPR petitions, Collabo is estopped from arguing otherwise

Collabo ultimately prevailed in convincing the PTAB to adopt its “single integrated chip/not a chipset” construction of “microcontroller,” and the PTAB declined to institute the IPR based on that construction. Ex. 8 at 7 (“We agree with Patent Owner that, as both parties’ constructions reflect, a microcontroller must be a *single, integrated chip*.” (emphasis added)); Ex. 9 at 7 (same); *see also* Ex. 8 at 11 (“We agree with Patent Owner that Petitioner has not shown sufficiently that Jahagirdar’s system resides on *a single chip*, as Petitioner’s claim construction requires. . . . Specifically, as Patent Owner explains, Jahagirdar’s ‘system 200’ is not a *single-chip microcontroller*, but rather a ‘system’ with multiple separate components.”) (emphasis added).²

Collabo’s clear and unmistakable disclaimer of multi-chip systems and limiting “microcontroller” to a “single, integrated chip/not a chipset” is binding on Collabo in this action as a prosecution disclaimer. *See Biogen*, 713 F.3d at 1095.

Collabo’s disclaimer is also binding under the doctrine of judicial estoppel. Each of the elements of judicial estoppel is satisfied here: first, Collabo previously argued that a microcontroller was a “single integrated chip,” a position inconsistent with its opposition to

² Despite its insistence to the PTAB that a microcontroller must be a “single, integrated chip” and cannot be a “chipset,” Collabo argued in response to Qualcomm’s Motion to Dismiss that a “microcontroller” is instead a “single, packaged semiconductor device.” ECF 26 at 5. However, a single packaged device can include several dies (i.e., several chips), and therefore is not necessarily a “microcontroller,” as Collabo defined that term in its POPRs. *See* Ex. 1 (Annavaram Decl.) ¶ 37. Collabo now abandons that construction in favor of a *fourth* proposed construction of the term: “plain and ordinary meaning.”

Qualcomm’s proposed construction; second, the PTAB accepted that position; and, third, there is no reason to believe Collabo’s change of position is inadvertent. *See In re Flugence*, 738 F.3d 126, 129 (5th Cir. 2013) (identifying elements of judicial estoppel); *see also Trs. of Columbia Univ. v. NortonLifeLock, Inc.*, No. 3:13-cv-808, 2019 WL 7040931, at *4–5 (E.D. Va. Dec. 20, 2019) (applying judicial estoppel based on IPR arguments).

Contrary to Qualcomm’s proposal, Collabo’s proposal ignores its statements to the PTAB and will encompass multi-chip systems that Collabo clearly disclaimed.

B. “microprogram” (claim 1)

Collabo’s Construction	Qualcomm’s Construction
Plain and ordinary meaning	“a control program (or a microcode) that runs at the lowest level of the hardware to control internal source of the CPU to execute command, interrupt processing, and the like, and is held entirely within the CPU as opposed to a program that is held in main memory until executed”

Qualcomm’s proposed construction of “microprogram” stems from the clear teachings of the ’575 Patent and Collabo’s own clarifying statements made before the PTAB regarding this term when opposing AMD’s IPR petitions.

Although the specification provides a description of the term, Collabo further delineated the metes and bounds of the claimed “microprogram” to the PTAB when opposing IPR petitions filed by AMD. *See* Ex. 6 (POPR, *AMD IPR I*, Paper No. 9) at 54–55; Ex. 7 (POPR, *AMD IPR II*, Paper No. 9) at 27–29. In distinguishing the claimed “microprogram” from a “program” disclosed in a prior art reference cited by AMD, Collabo identified three distinguishing characteristics of a “microprogram” that differentiate the term from a “program.” Specifically, Collabo explained that a “microprogram” is a particular type of program that (i) runs at the lowest level of hardware, (ii) is housed entirely within the CPU, and (iii) unlike a general “program,” is not held in the main memory of the computer system until execution by the CPU. *Id.* Collabo then represented to the

PTAB that the “program” disclosed in the prior art was not a “microprogram” because it lacked the characteristics enumerated above. *Id.*

Explicit statements by Collabo distinguishing the claimed “microprogram” over prior art are a clear disclaimer that bind Collabo to those statements and define the scope of the term. *See N. Am. Container, Inc. v. Plastipak Packaging, Inc.*, 415 F.3d 1335, 1345 (Fed. Cir. 2005) (“The inescapable consequence” of narrowly interpreting a claim to overcome the prior art during prosecution is “that the scope of applicant’s claims cannot cover [the disclaimed claim scope].”). Collabo’s argument that the term should be ascribed a “plain and ordinary meaning” is a blatant attempt to impermissibly broaden the scope of “microprogram,” and should be rejected.

As described below, Qualcomm’s proposed construction starts with the disclosures in the specification of the ’575 Patent and then incorporates Collabo’s distinguishing characteristics of the claimed “microprogram” that Collabo provided in its POPRs. Thus, the construction reflects how a person of ordinary skill would understand the meaning of the term “microprogram” in light of Collabo’s characterization to the PTAB. *See* Ex. 1 (Annavaram Decl.) ¶¶ 38–68.

1. The specification defines the claimed “microprogram”

The specification of the ’575 Patent describes the claimed “microprogram” as follows:

The microprogram herein refers to the control program for controlling internal sources of the CPU 1 in order to execute command, interrupt processing, and the like.

Ex. 2 (’575 Patent) at 9:46–49. As the patent explains, a “microprogram” is a specific type of program that controls or directs the resources of the CPU in order to execute a desired command, or instruction. This excerpt from the specification comports with the general understanding of “microprogram” that a person of ordinary skill in the art reading the specification would have

had at the time of the purported invention.³ Ex. 1 (Annaram Decl.) ¶ 55. As Qualcomm’s expert Dr. Annaram explains, a “microprogram” refers to a particular type of program that is used to control a CPU’s hardware resources and implement higher-level instructions. Ex. 1 (Annaram Decl.) ¶¶ 40–53. Qualcomm’s proposed construction simply adopts this teaching from the specification as understood by a person of ordinary skill in the art.

2. Collabo defined further characteristics of the claimed “microprogram” at the PTAB

In its opposition to AMD’s IPR petitions, Collabo further refined the meaning of “microprogram” as used in the ’575 Patent. Not content with the disclosure in the specification, Collabo carefully distinguished the claimed “microprogram” from a general “program” as disclosed in Chung, prior art cited in AMD’s petition. Collabo offered three distinguishing characteristics that are consistent with the definition in the specification but clearly and unmistakably narrow the scope. Collabo argued the claimed “microprogram,” or microcode, must (1) “run[] at the lowest level of the hardware” and (2) be “held entirely within the CPU,” as opposed to (3) being a program “held in the main memory of the computer system until executed by the CPU.” *See* Ex. 6 at 54–55; Ex. 7 at 28. Based on this explication, Collabo argued that the Chung reference’s disclosure of a “register-saving program” did not disclose the required “microprogram.” *Id.* at 27–29.

a) “Microprogram” runs at the lowest level of hardware

Relying on dictionaries contemporaneous to the time of the purported invention, Collabo explained to the PTAB that a “microprogram is a special program that runs at the lowest level of

³ The lack of extensive description of a “microprogram” is of no particular surprise, given that the concept of microprogramming itself has been around since at least the 1950s and the use of microprograms is not described as a novel concept in and of itself in the ’575 Patent. *See* Ex. 1 (Annaram Decl.) ¶ 52. As discussed further, Collabo identified additional commonly known characteristics of a “microprogram” in its POPRs.

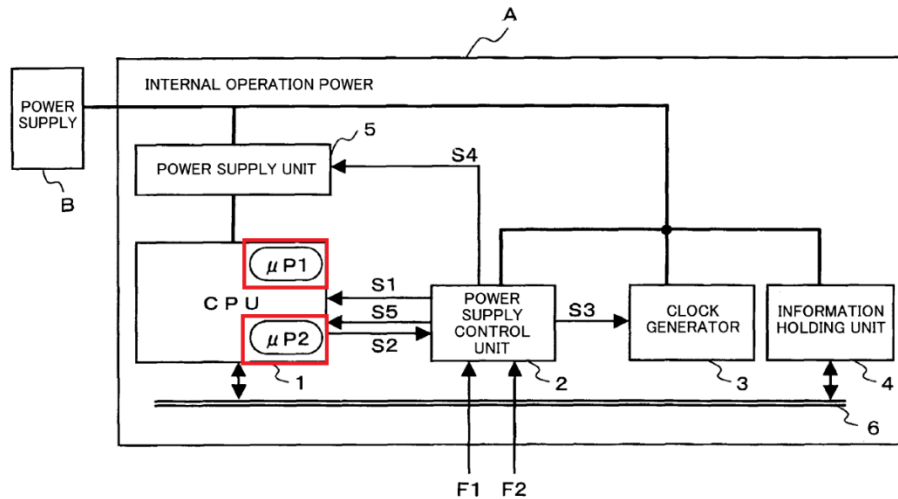
the hardware.” Ex. 6 at 54; Ex. 7 at 28; *see also* Ex. 12 at 472 (microprogram: “1. A computer program written in the most basic instructions or subcommands that can be executed by the computer.”); Ex. 10 at 693 (Microprogram: “A sequence of instructions, called microinstructions, specifying the basic operation needed to carry out a machine language instruction.”).

A person of ordinary skill in the art would have also understood, as suggested by Collabo, that a “microprogram” operates at the lowest level of hardware. As Qualcomm’s expert Dr. Annavaram explains, a POSA would have understood that a “microprogram” is a particular type of program that serves to facilitate the operation of a system’s hardware at the lowest level of operation. Ex. 1 (Annavaram Decl.) ¶¶ 40–53, 63.

b) “Microprogram” is held entirely within the CPU, not in the main memory of the computer system

In its POPR, Collabo further distinguished the term from a mere “program” by explaining that the claimed “microprogram,” or microcode, “is held entirely within the CPU.” Ex. 6 at 55; Ex. 7 at 28. This is consistent with how the term would be understood by a person of ordinary skill in the art. As Dr. Annavaram explains, a “microprogram” is a means through which some CPUs may implement the macro-instructions of a higher-level program and is contained entirely within the CPU. Ex. 1 (Annavaram Decl.) ¶¶ 40–53, 63. A CPU responding to macroinstructions using microprograms sidesteps the need to fetch additional code from outside the CPU. *Id.*

Further, figures from the ’575 Patent illustrate microprograms held entirely within the CPU. For example, Figure 1 depicts “a microcontroller according to a first embodiment of the present invention” with both a first and second microprogram (denoted as $\mu P1$ and $\mu P2$) contained within the CPU 1:



c) **“Microprogram” is not “held in the main memory of the computer system” like a mere “program”**

* * *

microprogram.” Ex. 7 at 29. In other words, Collabo contended that the disclosure of a *program* in Chung did not amount to a disclosure of a *microprogram*—the “microprogram” requires a specific kind of program that comports with the characteristics identified by Collabo in its POPRs.

Collabo’s statements opposing AMD’s IPR petitions provide a clear disclaimer of any understanding of the term “microprogram” that does not incorporate these three characteristics. “Claims may not be construed one way in order to obtain their allowance and in a different way against accused infringers.” *Southwall Techs., Inc. v. Cardinal IG Co.*, 54 F.3d 1570, 1576 (Fed. Cir. 1995). “Because an IPR proceeding involves reexamination of an earlier administrative grant of a patent, it follows that statements made by a patent owner during an IPR proceeding can be considered during claim construction and relied upon to support a finding of prosecution disclaimer.” *Aylus Networks*, 856 F.3d at 1360. Following these same principles, other courts in this district have similarly held that statements like Collabo’s made to the PTAB arguing against institution of an IPR warrant disclaimer. *See* Ex. 14 (*Sable Networks, Inc. v. Cloudflare, Inc.*, No. 6:21-CV-00261-ADA (W.D. Tex. Jan. 25, 2024) (Albright, J.)) at 16–18 (finding patentee in opposing institution of IPR had disclaimed claim scope even though PTAB did not rely on patentee’s arguments).

“[B]y distinguishing [the claims] over the prior art, [Collabo] . . . indicat[ed] what the claims do not cover.” *Spectrum*, 164 F.3d at 1378–79. Qualcomm’s proposal adopts this clear disclaimer by incorporating these three characteristics with the disclosures of the specification. Each of these three distinctions between a “microprogram” and a mere “program” made by Collabo serves to limit the appropriate construction of “microprogram” in the ’575 Patent. After justifying the validity of the claims on the basis that the prior art did not disclose these features of a “microprogram,” Collabo “cannot now escape [Defendants’] reliance upon this unambiguous

surrender of subject matter.” *Southwall*, 54 F.3d at 1581.⁴

3. Collabo’s attempt to enlarge the scope of “microprogram” under the guise of plain and ordinary meaning should be rejected

Despite the teachings of the specification and the further characteristics identified for the PTAB, Collabo now contends the term needs no construction and should be construed according to its “plain and ordinary meaning.” Though Collabo has not yet identified which of its prior statements to the PTAB are inaccurate, or why a departure from them is appropriate, it should nevertheless be “bound by its arguments made to convince [the PTAB] that [the claims] are patentable.” *Kaken Pharm. Co. v. Iancu*, 952 F.3d 1346, 1354 (Fed. Cir. 2020). Moreover, the term “microprogram” on its face is a distinctly technical term that requires the Court’s construction to ultimately “instruct the jury on the meanings to be attributed to all disputed terms used in the claims in suit so that the jury will be able to ‘intelligently determine the questions presented.’” *Sulzer Textil A.G. v. Picanol N.V.*, 358 F.3d 1356, 1366 (Fed. Cir. 2004) (citation omitted).

To the extent Collabo now argues that “microprogram” should be ascribed a plain and ordinary meaning, its clear statements to the PTAB should foreclose such a theory.

C. “power shutdown microprogram” (claim 1)

Collabo’s Construction	Qualcomm’s Construction
Plain and ordinary meaning	“a microprogram that evacuates the information necessary in proceeding with the program to the information holding unit, and then outputs the evacuation completed signal to the power supply control unit”

Claim 1 requires the execution of two microprograms, both of which have meanings

⁴ Though Collabo’s statements during the AMD IPRs do constitute disclaimer, if the Court disagrees, it should still find that Qualcomm’s proposed construction is appropriate. Even where “prosecution history statements do not rise to the level of unmistakable disavowal, they do inform the claim construction,” and here too should still provide persuasive evidence of how a POSA would understand the “microprogram” term. *Shire Dev., LLC v. Watson Pharms., Inc.*, 787 F.3d 1359, 1366 (Fed. Cir. 2015)

defined in the '575 Patent. The first is “power shutdown microprogram.” Qualcomm’s proposed construction identifies the “power shutdown microprogram” as a “microprogram” (pursuant to Qualcomm’s construction above) that “evacuates the information necessary in proceeding with the program to the information holding unit, and then outputs the evacuation completed signal to the power supply control unit.” These functions are more than a simple “power shutdown.”

The language of claim 1 confirms Qualcomm’s proposed construction. Claim 1 requires that “the CPU, upon receiving the shutdown request signal, executes a power shutdown microprogram, evacuates the information necessary in proceeding with the program to the information holding unit, and outputs an evacuation completed signal to the power supply control unit after evacuation is completed.” Ex. 2 ('575 Patent), Claim 1 at 18:59–64. In other words, execution of the “power shutdown microprogram” causes the CPU to “evacuate[] the information necessary in proceeding with the program to the information holding unit” and “output[] an evacuation completed signal to the power supply control unit after evacuation is completed.” *See* Ex. 1 (Annavaram Decl.) ¶ 70.

The specification further confirms this understanding:

The power shutdown microprogram evacuates the information necessary in proceeding with the program to the information holding unit, and then outputs the evacuation completed signal to the power supply control unit.

Ex. 2 ('575 Patent) at 2:62–65. Importantly, this statement appears within a passage that describes “the features of ‘the present invention’ as a whole,” further confirming that a skilled person would have understood the “power shutdown microprogram” to conform to this disclosed meaning. *Verizon Servs. Corp. v. Vonage Holdings Corp.*, 503 F.3d 1295, 1308 (Fed. Cir. 2007).

Embodiment 1 also confirms the construction offered by Qualcomm. Figure 1 shows that the CPU 1 includes a microprogram μ P1, which is the “power shutdown microprogram.” *See* Ex. 2 ('575 Patent) at Figure 1, 9:50 (identifying μ P1 as “power shutdown microprogram”). Referring

to Figure 1, the specification explains, “[t]he power shutdown microprogram $\mu P1$ evacuates the information (PC, PSW, SP, etc.) necessary in proceeding with the program to the information holding unit 4 or the register via the internal bus 6 in step n3, and lastly outputs the evacuation completed signal S2 to the power supply control unit 2.” *Id.* at 9:50–54.

Qualcomm’s proposed construction correctly defines the specific “power shutdown microprogram” of the claimed invention: a microprogram that “evacuates the information necessary in proceeding with the program to the information holding unit, and then outputs the evacuation completed signal to the power supply control unit.”

D. “power supply restoration microprogram” (claim 1)

Collabo’s Construction	Qualcomm’s Construction
Plain and ordinary meaning	“a microprogram that restores the information necessary in proceeding with the program and evacuated in the information holding unit to the CPU, and then branches the processes to the addresses indicated by the program counter to continue the program execution from the shutdown state”

The second microprogram is the “power supply restoration microprogram.” Qualcomm’s proposed construction identifies that the “power supply restoration microprogram” as a “microprogram” (pursuant to Qualcomm’s construction discussed above) that “restores the information necessary in proceeding with the program and evacuated in the information holding unit to the CPU, and then branches the processes to the addresses indicated by the program counter to continue the program execution from the shutdown state.” As with “power shutdown microprogram,” these functions are more than a simple “power supply restoration,” as explained by the claims and the specification.

The text of claim 1 confirms Qualcomm’s proposed construction. Claim 1 requires that:

the CPU, upon receiving the restoration request signal, executes a power supply restoration microprogram, restores the information necessary in proceeding with the program and evacuated in the information holding unit in time of power

shutdown, and then branches a process to an address indicated by a program counter to continue program execution from a shutdown state.

Ex. 2 ('575 Patent), Claim 1 at 19:18–24. In other words, execution of the “power supply restoration microprogram” causes the CPU to “restore[] the information necessary in proceeding with the program and evacuated in the information holding unit in time of power shutdown” and then “branch[] a process to an address indicated by a program counter to continue program execution from a shutdown state.” *See* Ex. 1 (Annavaram Decl.) ¶ 74.

The specification further confirms this understanding:

The power supply restoration microprogram restores the information necessary in proceeding with the program and evacuated in the information holding unit to the CPU, and then branches the processes to the addresses indicated by the program counter to continue the program execution from the shutdown state.

Ex. 2 ('575 Patent), 4:1–6. Importantly, this statement also appears within a passage that describes “the features of ‘the present invention’ as a whole,” further confirming that a person of skill in the art would have understood the “power supply restoration microprogram” to conform to this disclosed meaning. *Verizon Servs. Corp.*, 503 F.3d at 1308.

As with the “power shutdown microprogram,” exemplary embodiment 1 confirms Qualcomm’s construction for “power supply restoration microprogram.” *See* Ex. 2 ('575 Patent), 10:18–27 (describing “restor[ing]” and “branch[ing]” steps performed by “power supply restoration microprogram”).

Qualcomm’s proposed construction correctly defines the specific “power supply restoration microprogram” of the claimed invention: a microprogram that “restores the information necessary in proceeding with the program and evacuated in the information holding unit to the CPU, and then branches the processes to the addresses indicated by the program counter to continue the program execution from the shutdown state.”

E. Claim 2

Collabo's Construction	Qualcomm's Construction
Plain and ordinary meaning	Indefinite

Claim 2 is indefinite because a person of ordinary skill would be unable to understand what it requires, even after consulting the specification for guidance. *See Nautilus*, 572 U.S. at 901.

The grammatical structure of the claim is difficult to parse. The claim appears to describe that the clock generator selects from among two options upon receiving the clock stop control signal from the power supply control unit: [i] “operation performed after stopping supply of an operation clock,” (“*first option*”) or [ii] “operation stop performed without stopping the supply of the operation clock” (“*second option*”). However, a person of ordinary skill would find both options insolubly ambiguous.

The *first option* is unclear as to what “operation” is “performed” after stopping supply of the clock. Obviously, the “operation” is not the stopping of supply of the clock. It is some undefined “operation” that is performed “after” stopping the supply. The specification does not provide any guidance as to what “operation” is implied in this context.

The *second option* is also insolubly ambiguous. It requires an “operation stop” **without** stopping supply to the operation clock. It is not clear at all what “operation stop” means in this context when the claim requires simultaneously to perform “operation stop” while **not stopping** the supply of the clock. The specification does not elaborate on how to perform the two contradictory steps at the same time. Indeed, the patent does not mention an “operation stop.”

The specification discusses aspects of the two options set forth in Claim 2. Ex. 2 (’575 Patent) at 11:3–9; *see also id.* at 4:49–55 (parroting language of Claim 2). However, the specification fails to resolve the ambiguities of the claim mentioned above.

The Court should find Claim 2 invalid for indefiniteness.

F. Claim 8

Collabo's Construction	Qualcomm's Construction
Plain and ordinary meaning	Indefinite

Claim 8 is indefinite. A POSA would be unable to understand how the two microprograms recited in the claim are to be “selectively executed in an alternative way” based on two power shutdown factors, even after consulting the specification. *See Nautilus*, 572 U.S. at 901.

The phrase “selectively executed in an alternative way” seems to imply selection of one of two microprograms based on “the generated **power shutdown factor** or a type of **power shutdown factor**.” The specification implies that the power shutdown factor F1 results in the activation of the power shutdown microprogram $\mu P1$ and the power supply restoration factor results in the activation of the power supply restoration program ($\mu P2$ or $\mu P2'$). *See* Ex. 2 ('575 Patent) at 8:55–9:28, 10:48–53. The specification does not describe how the power **shutdown** factor results in the selective execution of the power supply **restoration** microprogram in an alternate way. The specification fails to provide any guidance; instead, it largely parrots the claim but in the context of the second embodiment, *id.* at 12:32–36, and mentions only **selectively activated**.

The terms “the generated power shutdown factor” and “the selected power shutdown factor” compound the ambiguity because both lack an antecedent basis. Neither Claim 8 nor Claim 1 refer to a “generated” or a “selected” power shutdown factor.” Claim 1 describes a power supply control unit that outputs a shutdown response signal in response to a “an occurrence of a power shutdown factor,” but that factor is not described as either “generated” or “selected.” And even if it were one or the other, the power shutdown factor in Claim 1 could not simultaneously be **both** the “generated” and “selected” power shutdown factors referenced in Claim 8.

Finally, Claim 8 presents two intractable alternatives. Claim 8 could require “selectively executing” one of the two recited microprograms. If that is correct, then the patent does not explain

how the selected microprogram is to be executed in an “alternative way.” But, “alternative way” could imply alternating execution between the two microprograms. If that is correct, then the patent does not clarify what “selectively executing” requires. While the specification mentions that the two microprograms can be “selected in an alternative way,” the specification is silent on the “selectively executed” aspect. *See* Ex. 2 (’575 Patent) at 5:39–44. Thus, POSA would not know how to “selectively execute” microprograms and also in an “alternate way.”

The specification does not resolve any of these intractable ambiguities; indeed, it largely parrots Claim 8 while providing no additional insight. Ex. 2 (’575 Patent) at 5:39–44. The Court should find Claim 8 invalid for indefiniteness.

G. “power supply unit” (claim 1)

Collabo’s Construction	Qualcomm’s Construction
Plain and ordinary meaning (neither requiring nor excluding the power switch)	Plain and ordinary meaning

There is no discussion in the specification that the claimed “power supply unit” requires a power switch. Indeed, the specification makes no mention of the term “power switch,” and Qualcomm is uncertain of what structure Collabo is seeking to capture by its construction. Instead, Figure 9 differentiates the “power supply unit” from the depicted switching circuits 9 and 10. Ex. 2 (’575 Patent) at 12:43–59, Fig. 9. Collabo’s construction seeks to inject additional meaning into the claim limitation to include a “power switch” without intrinsic support. Regardless, Collabo’s construction could only serve to confuse a jury by introducing a new structure that is not described in the specification, only to note that an unspecified structure is neither required nor excluded. The term should be given its plain and ordinary meaning without reference to a “power switch.”

V. CONCLUSION

Qualcomm respectfully requests that the Court adopts its proposed constructions for the disputed terms and find claims 2 and 8 invalid for indefiniteness.

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Respectfully submitted,

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CERTIFICATE OF SERVICE

I hereby certify that on 21st day of March, 2025, a true and correct copy of the foregoing document was served electronically, via ECF, on all counsel of record who are deemed to have consented to such service under the Court's local rules.

/s/ Anupam Sharma
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