IN THE UNITED STATES DISTRICT COURT
FOR THE WESTERN DISTRICT OF TEXAS
WACO DIVISION

COLLABO INNOVATIONS, INC., a Delaware Corporation, Plaintiff v. QUALCOMM INCORPORATED and QUALCOMM TECHNOLOGIES, INC., both Delaware Corporations, Defendants	CIVIL ACTION NO. 6:24-cv-00472-ADA **JURY TRIAL DEMANDED**

PLAINTIFF COLLABO INNOVATIONS, INC.'S
RESPONSIVE CLAIM CONSTRUCTION BRIEF

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I. INTRODUCTION

Plaintiff Collabo Innovations, Inc. ("Collabo") respectfully requests that the Court reject Qualcomm's[1] proposed claim constructions and adopt Collabo's positions. Qualcomm seeks to inject unwarranted limitations into readily understood terms and asserts indefiniteness where one of ordinary skill would readily understand the scope and meaning of the claims. Collabo also seeks to clarify the plain and ordinary meaning of one previously construed term. For the reasons set forth below, the Court should adopt Collabo's positions on claim construction.

II. LEGAL STANDARDS FOR CLAIM CONSTRUCTION

The general standards applicable to claim construction are well-summarized in this Court's opinions such as, for example, *Jawbone Innovs. LLC v. Meta Platforms, Inc.*, No. 6:23-cv-00158-ADA, ECF 104 at 2-5 (W.D. Tex. Nov. 24, 2024), and *Intellectual Ventures I LLC v. TCL Elecs. Holdings Ltd.*, No. 6:23-cv-00309-ADA, ECF 44 at 3-5 (W.D. Tex. Sept. 10, 2024).

III. RELEVANT BACKGROUND

Collabo accuses Qualcomm of infringing claims 1-3, 5, 8, 11, 12, 15, and 16 of U.S. Patent No. 7,930,575 ("the '575 patent"[2]) in this case. Collabo previously asserted the '575 patent in this Court in *Collabo Innovs., Inc. v. Advanced Micro Devices, Inc.*, No. 1:18-cv-00552 (W.D. Tex.) ("AMD case"). AMD filed two *inter partes* review ("IPR") petitions during the pendency of the AMD case, IPR2019-01523 and IPR2019-01524, both of which were denied institution. *See* ECF 32, Exs. 8 and 9. The Court conducted two claim construction hearings in

[1] "Qualcomm" refers to Defendants Qualcomm Incorporated and Qualcomm Technologies, Inc., collectively.
[2] A copy of the '575 patent is attached to ECF 32 as Ex. 2.

the AMD case, the first before Judge Yeakel (ECF 32, Ex. 3) prior to a stay pending IPR and a second supplemental hearing before the present judge (ECF 32, Ex. 4) after the case resumed.

In this case, the parties identify seven terms/phrases for construction from claims 1, 2, and 8. *See* ECF 32 at 3-20. The Court previously construed two of these terms. *See* ECF 32, Ex. 5 at 4 ("microcontroller"); 5 ("power supply unit"). In the AMD case Claim Construction Order, the Court stated that these were the "Court's final claim construction rulings" though "a more-detailed Order explaining [the Court's] analysis" would be forthcoming. *Id*. at 1. Thereafter, the parties settled and dismissed the case prior to any further orders on claim construction. *See* AMD case, ECF 133.

IV. DISPUTED CLAIM TERMS OF THE '575 PATENT

A. "microcontroller" (claim 1)

Collabo's Construction:	Qualcomm Construction:
Plain and ordinary meaning	"a single integrated chip as opposed to a set of multiple chips (a "chipset")"

Collabo agrees that the term "microcontroller" in the preamble is limiting and that it requires an integrated circuit including all the limitations of claim 1. Indeed, Collabo asserted precisely this position in the AMD case, and the Court decided (with good reason as explained below) to construe the term "microcontroller" as limiting and subject to its "[p]lain and ordinary meaning." ECF 32, Ex. 4 at 3-4. This construction was consistent with the findings of the Board in denying AMD's IPR petitions. To be clear, Collabo's construction maintains the same claim scope that the Board relied on in the IPR petitions. Conversely, Qualcomm's proposed construction improperly imports language and imputes unwarranted meaning from the IPR decisions that should not be part of the construction of the term "microcontroller." Further, Qualcomm's use of "as opposed to" in its construction is akin to an example and improper. *Plant*

Equip., Inc. v. Intrado, Inc., No. 2:09-CV-395-JRG, 2012 U.S. Dist. LEXIS 59495, at *32 (E.D. Tex. Apr. 27, 2012) (finding that "the suggested inclusion of an example in a construction — 'such as TCP/IP' — is improper."); *Layne Christensen Co. v. Bro-Tech Corp.*, No. 09-2381-JWL, 2011 U.S. Dist. LEXIS 80319, at *13 (D. Kan. July 22, 2011) (observing that "it is inappropriate to include such examples in the definition of the term.").

1) Collabo's Arguments and the Board's Decisions in AMD IPR I

In AMD IPR I (IPR2019-01523), Collabo distinguished the primary reference, Jahagirdar, on the basis that it did not teach "a microcontroller" because it did not teach a "system [that] resides on a single chip" and was instead a "multi-chip PC (personal computer system)." ECF 32, Ex. 6 at 16. Collabo noted that both parties agreed the term "microcontroller" in the preamble was limiting and that both parties' "constructions require the microcontroller to be on a single integrated chip." *Id*. at 18. Collabo then explained at length the difference between a single chip and the various chips dispersed across an entire PC board in Jahagirdar. *Id*. at 19-24.

Notably, Collabo did *not* assert that integrating multiple chips into a larger integrated chip would cause that single chip to not be "a microcontroller." Despite this, Qualcomm's construction seeks to introduce a negative limitation that "a single integrated chip *as opposed to a set of multiple chips (a "chipset")*." ECF 32 at 3 (emphasis added). Collabo's arguments in AMD IPR I do not support such a limitation. Rather in AMD IPR I, AMD identified a series of disparate components as satisfying the individual limitations of claim 1. Ex. 1 at 27-28. Recognizing that these disparate components were not part of a single microcontroller, AMD argued that "Jahagirdar's components *can* be located on the same chip." *Id*. at 28 (emphasis added). AMD based this argument on the statement in Jahagirdar that "[i]t will be appreciated that . . . various embodiments may be applied to different types of power management

configurations and/or for different types of integrated circuits." *Id.* Collabo responded by pointing out the leap in AMD's logic. Simply because Jahagirdar acknowledges different types of integrated circuits it does not mean that Jahagirdar discloses a single integrated circuit or chip that disclosed all of the components needed to satisfy claim 1. ECF 32, Ex. 6 at 24-25.

In view of these arguments, the Board agreed with Collabo "that, as both parties' constructions reflect, a microcontroller must be a single, integrated chip." ECF 32, Ex. 8 at 7. The Board noted that this was "consistent with the term's ordinary meaning" and declined any further construction. *Id*. at 8. The Board then concluded that AMD had "not shown sufficiently that Jahagirdar's system resides on a single chip" and that "the record evidence does not show sufficiently that Jahagirdar teaches its components 'can be located on the same chip.'" *Id*. at 11. The Board denied institution on that basis. *Id*. at 12.

2) Collabo's Arguments and the Board's Decisions in AMD IPR II

In AMD IPR II (IPR2019-01524), Collabo similarly distinguished the primary reference, Chung, on the basis that it did not teach "a microcontroller" because the cited components were a "multi-chip system" dispersed throughout a laptop computer and "not integrated on a single chip." ECF 32, Ex. 7 at 16-17. The Board again agreed that AMD had "not shown sufficiently that Chung's system resides on a single chip" and noted that AMD failed to assert that what it identified as the claimed "microcontroller" included all the requisite elements. ECF 32, Ex. 9 at 11. Once again, though the Board recognized that ordinary meaning of "microcontroller" is a single, integrated chip (*id*. at 7), that definition is not "opposed to a set of multiple chips" if they were alleged to be included in one microcontroller.

3) This Court's Prior Construction of "Plain and ordinary meaning"

In the AMD case, both before and after the stay for the IPRs, Collabo agreed that the preamble "a microcontroller" is limiting and should be construed as "an integrated circuit." *See,*

e.g., ECF 32, Ex. 5 at 3-4. The oral argument before Judge Yeakel, however, quickly revealed the pitfalls in simply replacing one word for another:

> THE COURT: What do you contend is included -- how --stated another way, how would one of skill in the art understand an integrated circuit? . . . Or what do you contend is included in an integrated -- the term "an integrated circuit" from the perspective of one of skill in the art?
>
> MR. CHERNG [Collabo counsel]: Yes, Your Honor. And this is something that we touched a bit on yesterday. Our proposal was "an integrated circuit," and it was criticized for -- I believe misunderstood a bit and criticized. AMD argued that, well, *it's not necessarily only one circuit* integrated onto the same chip. *And that's not what we are arguing either*.
>
> THE COURT: So tell me what it would mean to one of skill in art if I were to accept your proposed construction and say that a microcontroller means an integrated circuit.
>
> MR. CHERNG [Collabo counsel]: Right. And, Your Honor, a person of skill in the art would read the claim and look at the – find the CPU, the power supply unit, the power play control unit, information holding unit, and clock generator and know that those would be structures integrated onto that chip.

ECF 32, Ex. 3 (48:9-49:5) (emphasis added). This exchange reveals the futility in replacing the word "microcontroller" with "integrated circuit" (or chip or any other word) when Collabo has already agreed (repeatedly) that the preamble is limiting. The preamble of claim 1 recites "[a] microcontroller comprising" several elements, including (1) a CPU, (2) a power supply unit . . .; (3) a power supply control unit . . ., (4) an information holding unit . . ., and (5) a clock generator. *See*'575 patent, Cl.1. By agreeing that this preamble is limiting, Collabo has already affirmed that each of the claimed limitations must be found on "a microcontroller." And though the AMD case settled before the Court could "issue a more-detailed Order explaining its analysis," it was entirely appropriate to rule that the preamble "microcontroller" is (a) limiting

and (b) subject to its "[p]lain and ordinary meaning." ECF 32, Ex. 5 at 2-4; *see also* Dorney Decl.[3] ¶¶35-41.

* * *

Qualcomm's attempts to rewrite the term "microcontroller" to use different words and import improper negative limitations introduce ambiguity and invite further dispute. As explained above with respect to the arguments made in IPR, Collabo has never asserted, and the Board never found, that a "microcontroller" excludes "a set of multiple chips" or "(a chipset)." *See supra* Section.A.1)-2. Rather, what is clear from the arguments and decisions in the IPRs is that when multiple chips or chipsets are not included in a single "microcontroller," this limiting requirement of the preamble is not satisfied.

And as the Court's prior order in the AMD case correctly concluded, replacing the word "microcontroller" with "integrated circuit" or "chip" provides no further clarity or change in claim scope. Qualcomm's expert declaration further reinforces this point. Qualcomm's expert quotes what he contends are "pertinent definitions" that define a "chip" as both:

> A small *unpackaged functional element* made by subdividing a wafer of semiconductor material. Sometimes referred to as a die. (ECF 32, Ex. 1 ¶34) (emphasis added).
>
> A single piece of semiconductor material (silicon, sapphire, germanium, etc.) containing *one or more circuits*, *usually packaged* as a unit. (*Id*. ¶35) (emphasis added).

According to these definitions, a "chip" may be packaged or unpackaged, a functional element or "one or more circuits." Qualcomm's expert nevertheless opines that a semiconductor may be implemented on a "die" that contains "one microcontroller" and acknowledges that each package

[3] "Dorney Decl." refers to the Declaration of Timothy D. Dorney, Ph.D. Regarding Claim Construction attached hereto.

"usually contains one die" but "[a] package may contain two or more dies depending on the functional circuits." *Id*. ¶¶36-37. None of these observations are at odds with the positions Collabo has taken before this Court or in the IPRs—i.e., that "a microcontroller" of claim 1 must contain all of the claimed elements which Qualcomm's expert acknowledges could be on one or more dies that are packaged (or unpackaged) as a unit. Thus, adding Qualcomm's proposed additional terms to the plain and ordinary meaning of "microcontroller" add nothing to clarify the scope, and perhaps more notably have no justification from the specification.

For at least these reasons, the Court should reject Qualcomm's proposed construction of "microcontroller" and give the term its "plain and ordinary meaning," acknowledging the parties' agreement that this preamble is limiting.

B. "microprogram" (claim 1)

Collabo's Construction:	Qualcomm Construction:
Plain and ordinary meaning	"a control program (or a microcode) that runs at the lowest level of the hardware to control internal source of the CPU to execute command, interrupt processing, and the like, and is held entirely within the CPU as opposed to a program that is held in main memory until executed"

The chief purpose of claim construction is to elaborate terse claim language to help the jury understand. *See, e.g.*, *Terlep v. Brinkmann Corp.*, 418 F.3d 1379, 1382 (Fed. Cir. 2005) ("The construction of claims is simply a way of elaborating the normally terse claim language in order to understand and explain, but not to change, the scope of the claims."). Qualcomm's proposed construction does the opposite—replacing a straightforward term with a convoluted and unwarranted 50-word muddle. Claim 1 of the '575 patent uses the term "microprogram" twice, in both cases describing a "microprogram" executed by the CPU when it saves or restores the information used to run a program in order to enter or exit a standby or shutdown state. '575

patent, Cl.1; *see also infra* Section.C (regarding the specific microprograms). Specifically, claim 1 requires:

> . . . an information holding unit for holding information evacuated from the CPU, the information being necessary in proceeding with *a program*; . . .
>
> the CPU, upon receiving the shutdown request signal, executes a power shutdown *microprogram*, evacuates the information necessary in proceeding with *the program* to the information holding unit, . . .
>
> the CPU, upon receiving the restoration request signal, executes a power supply restoration *microprogram*, restores the information necessary in proceeding with *the program* and evacuated in the information holding unit in time of power shutdown, and then branches a process to an address indicated by a program counter to continue *program* execution from a shutdown state.

Id. (emphasis added). Claim 1 indicates at least that the CPU executes a "microprogram" to perform functions in the CPU (related to power shutdown and restoration) as distinct from a more general "program" run by the CPU for which the claimed invention seeks to preserve the information "necessary in proceeding with the program." *Id*.

The specification similarly distinguishes between the CPU executing power shutdown and restoration "microprograms" when it preserves information to execute a "program" after restoration from a standby, shutdown or low power state. *See, e.g.*, '575 patent, 8:59-63; 9:50-52; 10:58-65; 11:23-27; 11:63-66; 12:32-39; 15:50-55; 16:37-41; 17:15-23. The specification explains in Embodiment 1 that:

> The microprogram herein refers to the control program for controlling internal sources of the CPU 1 in order to execute command, interrupt processing, and the like.

Id. at 9:46-49. That is, a microprogram relates to control functions of the CPU as distinct from more general programs run by the CPU. The description in this embodiment is explicitly explanatory of the plain and ordinary meaning of microprogram (referring to programs that "execute command, interrupt processing, *and the like*") and does not define the term. For

example, the second embodiment describes different types of "power supply restoration microprogram[s]" including "(a) microprogram for restoring the evacuated information necessary in proceeding with the program, and proceeding with the program, (b) microprogram for jumping to a specific address and running a dedicated initialization and a restoration application program to restore the set value without using the evacuated information, and (c) microprogram for resetting, may be prepared to be selected by the register, signal, terminal, or the like." '575 patent, 12:21-31. That is, even these open-ended examples of types of microprograms may include the instructions for performing the stated functions or direct the CPU to an address for another program. *See* Dorney Decl. ¶44. Nevertheless, one of ordinary skill would understand the plain and ordinary meaning of a "microprogram." Dorney Decl. ¶¶42-49.

Despite this, Qualcomm's proposed construction seeks to insert several limitations that find no support in the claims or specification based on the citation of third-party dictionaries during the two AMD IPRs discussed previously. Specifically, Qualcomm seeks to add to the construction of "microprogram" (a) all description from Embodiment 1; (b) the term "microcode"; (c) require that it "runs at the lowest level of the hardware"; and (d) that it "is held entirely within the CPU as opposed to a program that is held in main memory until executed." Except for (a) the description from the specification, these additional limitations derive from third-party dictionaries cited as examples of what a microprogram is as distinct from what the petitioner had identified in the IPRs. *See* ECF 32, Ex. 6 at 54-55 and Ex. 7 at 28 (citing IPR Exs. 2001-03 *corresponding to* ECF 32, Exs. 10, 12-13).

Qualcomm asserts the citation and discussion of these dictionaries constitute a disclaimer requiring the inclusion of elements of these definitions in the construction of "microprogram."

Qualcomm Ex. 1049 - 12/22

ECF 32 at 13. It is true "[t]hat explicit *arguments* made during prosecution to overcome prior art can lead to narrow claim interpretations." *See Spectrum Int'l, Inc. v. Sterilite Corp.*, 164 F.3d 1372, 1378 (Fed. Cir. 1998) (emphasis added). But Federal Circuit "precedent requires that, in order for prosecution disclaimer to attach, the disavowal must be both clear and unmistakable." *3M Innovative Props. Co. v. Tredegar Corp.*, 725 F.3d 1315, 1325-26 (Fed. Cir. 2013) (citations omitted). Federal Circuit "cases also warn that, because the prosecution history represents an ongoing negotiation between the PTO and the inventor,[4] 'it often lacks the clarity of the specification and thus is less useful for claim construction purposes.'" *Id*. (quoting *Lazare Kaplan Int'l, Inc. v. Photoscribe Techs., Inc.*, 628 F.3d 1359, 1370 (Fed. Cir. 2010)). Thus, the Court must "analyze whether statements [] made during the prosecution of the asserted patents amount to a clear and unmistakable disclaimer limiting the meaning of the claim terms." *Mass. Inst. of Tech. v. Shire Pharms., Inc.*, 839 F.3d 1111, 1119 (Fed. Cir. 2016).

Collabo contends that the citation of these third-party dictionaries during the AMD IPRs do not constitute such "a clear and unmistakable disclaimer" at least because (1) the elements Qualcomm seeks to add were not the basis of the arguments over the art in the IPRs; and (2) they contradict the specification.

To the first point, none of the arguments Collabo made in the IPRs were premised on a microprogram being "a microcode", "run at the lowest level of the hardware"; or "held entirely within the CPU." In AMD IPR I, Collabo asserted that the "Petitioner does not argue that a 'microprogram' for restoring power supply is taught in the asserted references" at all. ECF 32,

[4] Although the statements at issue here occurred during a Preliminary Response in IPR, Collabo submits that the same logic would apply particularly whereas here, the Board did not address or base its decision regarding patentability on any of these statements and trial was not instituted to enable any further clarification.

Ex. 6 at 54. Collabo then listed off the various third-party dictionary definitions articulating a distinction between "microprogram" and "program," but the argument was that the Petition had failed to argue that the reference taught a "microprogram" not that Petitioner had pointed to something lacking one or more of these limitations. *Id*. As noted above, the Board denied institution for other reasons and did not address the argument regarding "microprogram." ECF 32, Ex. 8 at 12. In AMD IPR II, Collabo argued that the identified "register-saving program" was part of the "monitor program" that "*runs in the environment of the operating system* to detect when an inactive condition exists at the CPU." ECF 32, Ex. 7 at 29 (emphasis added). Collabo distinguished the asserted "register-saving program" from a microprogram because it ran in the environment of the operating system and not because it did not run "at the lowest level of hardware" or was not held "entirely within the CPU as opposed to . . . main memory." This distinction is consistent with the distinction from the specification between a program and a microprogram for controlling internal sources of the CPU. *See also* Dorney Decl. ¶43. In AMD IPR II, the Board likewise denied institution for other reasons and did not address the argument regarding "microprogram." ECF 32, Ex. 9 at 12.

Second, Qualcomm's proposed construction is directly at odds with the specification insofar as it purports to construe a "microprogram" as a program "that runs at the lowest level of the hardware." Dorney Decl. ¶¶44**.** The specification specifically refers to using the "microprogram for jumping to a specific address and running a dedicated initialization and a restoration application program . . . ." '575 patent, 12:26-29. The described functionality of "jumping to a specific address" is typically part of the assembly language of a microcontroller and is necessarily not the "lowest level." Dorney Decl. ¶¶44-47**.**

The third-party dictionary definitions that Qualcomm seeks to incorporate into the construction of "microprogram" are also inconsistent with the specification and even with Qualcomm's proposed construction. For example, the IEEE dictionary provides that a "microprogram" is:

> A sequence of instructions, called microinstructions, specifying the basic operations needed to carry out a machine language instruction. *See also:* control store; microcode.

ECF 32, Ex. 10 at 693. This definition would imply that the "microprogram" is at a lower level than machine language instructions, but as noted in the previous paragraph the specification describes a microprogram that could be implemented at the level of assembly language. *See* Dorney Decl. ¶¶44-47**.** Furthermore, the Modern Electronics dictionary provides eight definitions of "microprogram." *See* ECF 32, Ex. 12 at 472. The first definition cited in Qualcomm's brief provides that a "microprogram" is "[a] computer program written in the most basic instructions or subcommands that can be executed by the computer." *Id*.; *see* ECF 32 at 11. But that definition also provides that "*Frequently*, it is stored in read-only memory" which at least undermines Qualcomm's proposal that such a microprogram must *always* be "held entirely within the CPU." *Id*. (emphasis added). The Modern Electronics dictionary provides many other definitions of varying scope including "5. A type of program that directly controls the operation of each function element in a microprocessor" which is much closer to the explanation in the '575 patent's specification of its use of the term "microprogram." *Id*. No one element of these third-party definitions should be incorporated into the readily understood meaning of "microprogram" within the context of the '575 patent. More importantly, Qualcomm cannot pick and choose which random elements to include. The argument made in the IPRs was simply that the petitioner had failed to adequately identify a microprogram.

For at least these reasons, the Court should reject Qualcomm's proposed construction of "microprogram" and give the term its "plain and ordinary meaning."

C. "power shutdown microprogram" (claim 1)[5]

Collabo's Construction:	Qualcomm Construction:
Plain and ordinary meaning	"a microprogram that evacuates the information necessary in proceeding with the program to the information holding unit, and then outputs the evacuation completed signal to the power supply control unit"

"power supply restoration microprogram" (claim 1)

Collabo's Construction:	Qualcomm Construction:
Plain and ordinary meaning	"a microprogram that restores the information necessary in proceeding with the program and evacuated in the information holding unit to the CPU, and then branches the processes to the addresses indicated by the program counter to continue the program execution from the shutdown state"

Qualcomm's proposed constructions for these two microprograms seeks to rewrite claim 1 by inserting other limitations of the claim into readily-understood terms and improperly importing aspects of a preferred embodiment. Claim 1 requires that:

> *the CPU*, upon receiving the shutdown request signal, *executes a power shutdown microprogram*, evacuates the information necessary in proceeding with the program to the information holding unit, and outputs an evacuation completed signal to the power supply control unit after evacuation is completed,. . .
>
> *the CPU*, upon receiving the restoration request signal, *executes a power supply restoration microprogram*, restores the information necessary in proceeding with the program and evacuated in the information holding unit in time of power

[5] Collabo presents these two terms together because Qualcomm's arguments raise the same issues for both "power shutdown microprogram" and "power supply restoration microprogram." Though Qualcomm presented its arguments in consecutive Sections.IV.C and D in its brief (ECF 32 at 14 and 16), Collabo submits that the presentation here nevertheless complies with the Court's OGP Briefing Procedure (Section IX) by maintaining the same order.

> shutdown, and then branches a process to an address indicated by a program counter to continue program execution from a shutdown state.

Id. (emphasis added). The claim as drafted requires that the CPU executes a microprogram (either related to power shutdown or restoration as appropriate), and then *the CPU* performs the functions of evacuating or restoring information and subsequent actions. Qualcomm's request to insert additional limitations into the construction of the respective microprograms is improper.

Qualcomm's attempt to attribute the claimed actions of the CPU to the microprograms is both technically imprecise and improperly seeks to import aspects of an exemplary embodiment. As initial matter, even if Qualcomm were correct to assert that the claim requires that the claimed microprograms "cause[]" the CPU to perform the claimed functions (*see* ECF 32 at 15 and 17), it is still the CPU that executes the instructions of the microprogram as claimed. *See* Dorney Decl. ¶¶52, 56. This is how one of ordinary skill would understand the statements Qualcomm relies on such as "[t]he power shutdown microprogram μP1 evacuates the information . . ." or "power supply restoration microprogram μP2 restores the information . . . ." *See* ECF 32 at 15 (quoting '575 patent at 9:50-54); *id*. at 17 (quoting '575 patent at 10:18-27). Dorney Decl. ¶¶52-53, 56-57.

Moreover, these statements regarding what these two microprograms do are part of exemplary Embodiment 1. Limitations from exemplary embodiments should not ordinarily be read into claims. *See, e.g.*, *Comark Communs., Inc. v. Harris Corp.*, 156 F.3d 1182, 1187 (Fed. Cir. 1998). As noted above, the second embodiment describes different types of "power supply restoration microprogram[s]" including "(a) microprogram for restoring the evacuated information necessary in proceeding with the program, and proceeding with the program, (b) microprogram for jumping to a specific address and running a dedicated initialization and a restoration application program to restore the set value without using the evacuated information,

and (c) microprogram for resetting, may be prepared to be selected by the register, signal, terminal, or the like." '575 patent, 12:21-31. Thus, the specification provides that the microprograms perform functions in the CPU, related either to power shutdown or restoration as named, but they may comprise the instructions for performing the stated function, "jump" the CPU to an address to run a dedicated application to carry out the function "or the like." The specification, like the claims, do not require that the microprogram necessarily include the instructions to carry out each of the claimed functions. And more importantly, the claim plainly requires that it is the CPU that carries out the claimed functions whether as a direct function of executing the instructions of the microprogram or in conjunction with executing such microprogram.

For at least these reasons, the Court should reject Qualcomm's proposed construction of "power shutdown microprogram" and "power supply restoration microprogram," and give these terms their "plain and ordinary meaning."

D. "The microcontroller according to claim 1, wherein the clock generator selects one of operation performed after stopping supply of an operation clock and operation stop performed without stopping the supply of the operation clock as operation to be performed upon receiving the clock stop control signal from the power supply control unit." (claim 2)

Collabo's Construction:	Qualcomm Construction:
Plain and ordinary meaning	Indefinite

The language of claim 2 is not indefinite and would be readily understood by one of ordinary skill in the art in light of the specification. *See* Dorney Decl. ¶¶58-63. As Qualcomm acknowledges, the language describes a capability of the claimed clock generator to select between two options upon receipt of the clock stop control signal: (1) operation performed after stopping supply of an operation clock and (2) operation stop performed without stopping the supply of the operation clock. '575 patent, Cl.2. The clock generator is one of the structures

claimed as part of the microcontroller of claim 1 and it receives "a clock stop control signal" from the power supply control unit. '575 patent, Cl.1. The language of claim 2 describes one of the "[v]ariants" of Embodiment 1 in the specification where the clock generator is configured to select between either stopping the clock or not. '575 patent, 11:3-9. This feature provides the capability to determine whether to stop the clock or not as part of the claimed functions in claim 1 that "shuts down power supply to the CPU." *See* '575 patent, 11:9-14. Thus, the invention of claim 2 allows the shutdown of the CPU as required by claim 1 with the capability of choosing whether or not to also shut down the clock. There is nothing ambiguous about the claim language and one of ordinary skill would understand its scope with more than reasonable certainty. *See* Dorney Decl. at ¶¶58-63. For at least this reason, the Court should not find this claim indefinite and it should be given its plain and ordinary meaning.

E. "The microcontroller according to claim 1, wherein one of the power shutdown microprogram and the power supply restoration microprogram is selectively executed in an alternative way, according to the generated power shutdown factor or a type of the selected power shutdown factor." (claim 8)

Collabo's Construction:	Qualcomm Construction:
Plain and ordinary meaning	Plain and ordinary meaning

The language of claim 8 is not indefinite and would be readily understood by one of ordinary skill in the art in light of the specification. *See* Dorney Decl. ¶¶64-70. Claim 8 requires that either the power shutdown microprogram or the power supply restoration microprogram is selectively executed in an alternative way according to the power shutdown factor. '575 patent, Cl.8. The specification explains that this feature "enables the number of information necessary in proceeding with the program to be changed" such that "an efficient application system can be built by executing the microprogram respectively corresponding to the number of information necessary in proceeding with the program." '575 patent, Col. 5:39-50; *see also* 12:32-39. Claim 1 requires "a power shutdown factor" the occurrence of which prompts the power supply

control unit to output a shutdown request signal and in turn leads to the execution of the power shutdown microprogram and power supply restoration microprogram in accordance with the other limitations of the claim. *See* '575 patent, Cl.1. Claim 8 captures this embodiment in the specification where the claimed "power shutdown factor" provides more nuanced indication (i.e. "according to the generated power shutdown factor or a type of the selected power shutdown factor") such that one or both of the microprograms is "selectively executed in an alternative way" to permit changes in the information necessary to be evacuated or restored as required by claim 1. The claim language is not ambiguous and one of ordinary skill would understand its scope with more than reasonable certainty. *See* Dorney Decl. ¶¶64-70. For at least this reason, the Court should not find this claim indefinite and it should be given its plain and ordinary meaning.

F. "power supply unit" (claim 1)

Collabo's Construction:	Qualcomm Construction:
Plain and ordinary meaning (neither requiring nor excluding the power switch)	Plain and ordinary meaning

Collabo and Qualcomm agree that the term "power supply unit" should be subject to its plain and ordinary meaning. Collabo has raised this issue and its proposed negative parenthetical only to address an aspect of the Court's prior construction in the AMD case. In the AMD case, the Court construed "power supply unit" as "Not subject to 35 U.S.C. § 112, para. 6; plain and ordinary meaning, *wherein the power switch is not a part of the power supply unit*." ECF 32, Ex. 5 at 5 (emphasis added). As noted above, the Court's Claim Construction Order provided that these constructions were the "Court's final claim construction rulings" though "a more-detailed Order explaining [the Court's] analysis" would be forthcoming, but the case settled before any further discussion or objections could be raised. *Id*. at 1. As is apparent from the prior construction, the arguments between Collabo and AMD centered around the application of

Section 112¶6. *See also* ECF 32, Ex. 4 at 3:2-9:17 (suppl. *Markman* hr. tr.). Collabo contends that "power supply unit" should again be given its plain and ordinary meaning, which neither necessarily includes nor excludes a "power switch." *See also* Dorney Decl. ¶¶71-74. As Qualcomm notes, "[t]here is no discussion in the specification that the claimed 'power supply unit' requires a power switch." ECF 32 at 20. Likewise, there is nothing in the specification or the plain and ordinary meaning of the term "power supply unit" that the presence of a switch renders something not "a power supply unit." Thus, so long as Qualcomm agrees that the claimed "power supply unit" should be subject to its plain and ordinary meaning and cannot seek to leverage the AMD case order to make arguments regarding a "power supply unit" including or not including a switch, then this term should be agreed as subject to its plain and ordinary meaning.

V. CONCLUSION

For at least the foregoing reasons, Collabo respectfully requests that the Court adopt its positions on claim construction and reject those put forward by Qualcomm.

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Respectfully submitted,

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CERTIFICATE OF SERVICE

I hereby certify that all counsel of record who have consented to electronic service are being served with a copy of this document via the Court's CM/ECF system on April 11, 2025.

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