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32/64-BIT 80x86 ASSEMBLY LANGUAGE ARC

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The increasing complexity of programming environments provides a number of opportunities for assembly language programmers. *32/64-Bit 80x86 Assembly Language Architecture* attempts to break through that complexity by providing a step-by-step understanding of programming Intel and AMD 80x86 processors in assembly language. This book explains 32-bit and 64-bit 80x86 assembly language programming inclusive of the SIMD (single instruction multiple data) instruction supersets that bring the 80x86 processor into the realm of the supercomputer, gives insight into the FPU (floating-point unit) chip in every Pentium processor, and offers strategies for optimizing code.

Learn about:

- 3DNow! MMX, SSE, SSE-2, SSE-3, AMD64, and EM64T instruction sets
- The similarities of and differences between various 80x86 processors
- Boolean bit manipulation
- Data swizzling, shuffling, and splatting
- Integer and floating-point math operations
- Branching and branchless coding methods
- Coding standards
- Debugging functions

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James Leiterman is a senior computer engineer who has been developing hardware and software professionally since 1978 and programming video/computer games for 20 years. He has worked for multiple game companies including Midway, LucasArts, Atari, Wild Goose Games, a casino gaming company, and two Internet online game companies and has shipped nine games. He is also the author of *Vector Game Math Processors* and *Learn Vertex and Pixel Shader Programming with DirectX 9*. He lives in Thousand Oaks, prospecting for California gold.

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JAMES C. LEITERMAN

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	Intel
P	Pentium
PII	Pentium II (MMX)
SSE	SSE (Katmai NI)
SSE2	SSE2
SSE3	SSE3 (Prescott NI)
E64T	64-bit Memory

	AMD
K6	K6
3D!	3DNow!
3Mx+	3DNow! and MMX Ext.
A64	AMD64

Mnemonic	P	PII	K6	3D!	3Mx+	SSE	SSE2	A64	SSE3	E64T
INC	✓	✓	✓	✓	✓	✓	✓	32	✓	32
SYSRET			✓	✓	✓			✓		64

✓	Mnemonic supported
32	32-bit support only
64	64-bit support only

Each mnemonic will also have a table showing its organization as well as type of data, bit size of data, and operand method for each processor supported.

	Op *rmDst, rSrc(8/16/32/64)*	Signed	
	Op *rDst, rmSrc(8/16/32/64)*		
MMX	Op *mmxDst, mmxSrc/m64*	Signed	64
3DNow!	Op *mmxDst, mmxSrc/m64*	Signed	64
SSE	Op *xmmDst, xmmSrc/m128*	Single-precision	128
SSE2	Op *xmmDst, xmmSrc/m128*	Single-precision	128

rDst	General-purpose register — {8-, 16-, 32-, 64-bit}
rSrc{8/16/32/64}	
m32, m64, m128	32-, 64-, 128-bit memory access
rmDst	General-purpose register and/or memory
mmxDst, mmxSrc	MMX registers
xmmDst, xmmSrc	XMM registers

Note: When general-purpose registers specify 64 bit, such as rDst, rmSrc{8/16/32/64}, then that is *only* available when running in 64-bit mode. Contrarily, 64-bit data is available for MMX and SSE instruction sets.

Some operators take zero, one, two, or three arguments. Unlike some non-80x86 processors, *sourceB* is the same as the *destination*. The 80x86 uses a D += A methodology. When the SIMD operator is being explained, both arguments will be used, such as "The Op instruction

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80x86 Registers

The Intel 80x86 processor family has internal storage that is referred to as registers. These have been organized into seven groups: general-purpose data registers, segment registers, status registers, control registers, FPU registers used by the FPU (floating-point unit), MMX registers, and XMM registers. Please note that the FPU and MMX registers share storage area and thus are mutually exclusive (only one of them can be used at a time). Each has its own set of functionality.

The following registers and their ranges are for dealing with the SIMD instruction sets directly. They do not include system registers.

Table 3-2: SIMD instruction with register names and bit widths

SIMD Instruction Set	Regs	IA-32	EM64T	Bits
MMX	mm#	(0...7)	(0...7)	64
3DNow!	mm#	(0...7)	(0...7)	64
3DNow! Extensions (3DNow!+)	mm#	(0...7)	(0...7)	64
3DNow! MMX Extensions (MMX+)	mm#	(0...7)	(0...7)	64
SSE	xmm#	(0...7)	(8...15)	128
SSE2	xmm#	(0...7)	(8...15)	128
SSE3	xmm#	(0...7)	(8...15)	128

General-Purpose Registers

The general-purpose registers are organized into two groups of eight registers: The RAX, RBX, RCX, and RDX general registers each have an 8-, 16-, 32-, and 64-bit form, as well as the index registers RSI and RDI, and the stack pointers RBP and RSP. The second set of eight are new registers R8...R15. The instruction pointer RIP has a 16-, 32-, and 64-bit form depending on which mode the processor is running in.

No 64-bit: There is a special case where the AH, BH, CH, and DH are not accessible when the REX prefix is used. REX is used for all extended 64-bit registers as well as SIL, DIL, BPL, and SPL register access.

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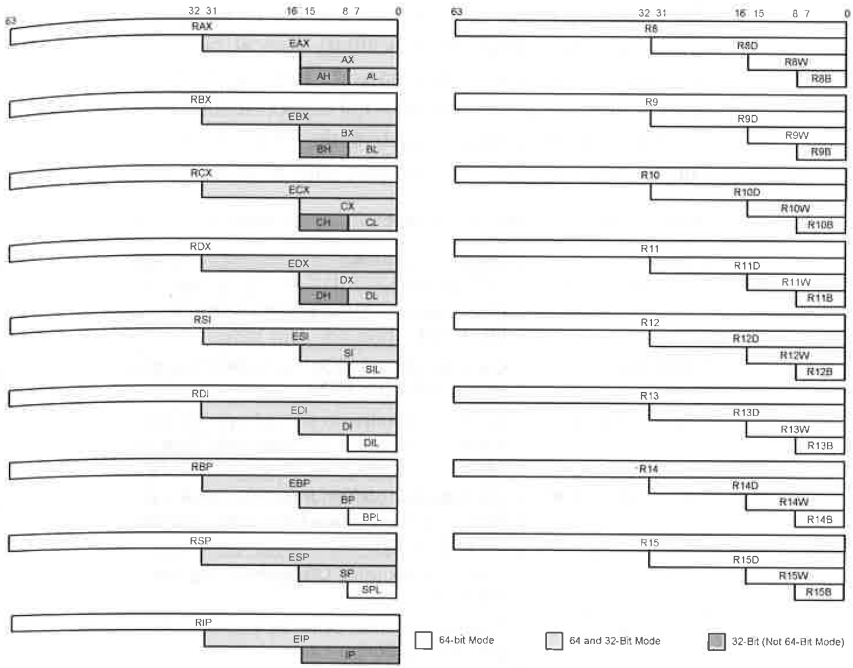

Figure 3-2: 64/32/16-bit general-purpose 80x86 registers

Table 3-3: 64-bit mode registers

64	RAX	RBX	RCX	RDX	RSI	RDI	RBP	RSP	RIP
32	EAX	EBX	ECX	EDX	ESI	EDI	EBP	ESP	
16	AX	BX	CX	DX	SI	DI	BP	SP	
8	AL	BL	CL	DL	SIL	DIL	BPL	SPL	

64	R8	R9	R10	R11	R12	R13	R14	R15
32	R8D	R9D	R10D	R11D	R12D	R13D	R14D	R15D
16	R8W	R9W	R10W	R11W	R12W	R13W	R14W	R15W
8	R8B	R9B	R10B	R11B	R12B	R13B	R14B	R15B

Table 3-4: 32-bit (Protected/Real Mode) registers

32	EAX	EBX	ECX	EDX	ESI	EDI	EBP	ESP	EIP
16	AX	BX	CX	DX	SI	DI	BP	SP	IP
8	AL AH	BL BH	CL CH	DL DH					

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The general-purpose registers are used as memory pointers, address calculations (displacement w/scaling), logical bit, and mathematical operations. There is an exception as the RSP register is the stack pointer and has limitations such as it does not support scaling and displacement. In relation to the segment registers, the 64-bit stack pointer is used in conjunction with the stack segment-selector (SS) register as a default.

Table 3-5: 64-, 32-, and 16-bit general-purpose registers

Register	Extra Functionality
RAX, EAX, AX	The accumulator. If used as a pointer in Protected Mode uses the DS segment register as a default. DS:[EAX]
RBX, EBX, BX	Used as a data pointer using the DS segment register as a default. DS:[EBX]
RCX, ECX, CX	Used as a counter in string (rep) and loop operations. If used as a pointer in Protected Mode uses the DS segment register as a default. DS:[ECX]
RDX, EDX, DX	Input/output port address. If used as a pointer in Protected Mode uses the DS segment register as a default. DS:[EDX]
RSI, ESI, SI	Source index using DS segment register as a default. DS:[ESI]
RDI, EDI, DI	Destination index using ES segment register as a default. ES:[EDI]
RBP, EBP, BP	Pointer to data on the stack (very similar to ESP); uses the SS segment register as a default. SS:[EBP]
RSP, ESP, SP	Stack pointer used the SS segment register as a default. SS:[ESP]
RIP, EIP, IP	Instruction pointer. CS:[EIP]

Note: The "R" prefix of these registers only became available with the 64-bit versions of the processor. The "E" prefix of these registers became available with the introduction of the 32-bit 386 processor. Prior to that, only 16-bit registers were supported.

Regardless of which mode you were in, you could access either 32-bit or 16-bit registers. But this was with the introduction of a pre-op code. If in 32 bit, you accessed 32-bit registers. In 16 bit, you accessed 16-bit registers. But if you needed to access the alternate type, then a hidden leading prefix was embedded in the binary output:

(**66h**) operand-size prefix
(**67h**) address-size prefix

So from 32-bit code…

```
    mov eax,3
66h mov ax,3
```

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Logical Packed XOR D=(A⊕B)

Listing 4-8: ...\chap04\pbool\PBool.cpp

```
void vmp_pxor(void *pvD, void *pvA, void *pvB)
{
  uint32 *pD, *pA, *pB;

  pD=(uint32*) pvD;
  pA=(uint32*) pvA;
  pB=(uint32*) pvB;
  *(pD+0) = *(pA+0) ^ *(pB+0);   // {31...0}
  *(pD+1) = *(pA+1) ^ *(pB+1);   // {63...32}
  *(pD+2) = *(pA+2) ^ *(pB+2);   // {95...64}
  *(pD+3) = *(pA+3) ^ *(pB+3);   // {127...96}
}
```

See the code snippets from the previously discussed instruction AND, then substitute the instruction {^, *xor*, *pxor*} for the {&, *and*, *pand*} accordingly.

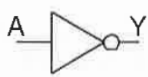
Another use for this operation is as a Boolean NOT (one's complement) operator. By using an input *A* and setting *B* permanently to a logical one, an inverse bit is achieved. Note the following table where zero becomes one and one becomes zero.

A ⊕ B	Y
0 1	1
1 1	0

Figure 4-1: Example of using a logical XOR with a logical true bit to achieve the equivalent of a logical NOT condition.

As can be seen, input A and output Y are the exact opposite. Keep in mind that Boolean logic is bit based and bit isolated so that adjacent bits do not affect each other.

NOT — One's Complement Negation



A	Y
0	1
1	0

Mnemonic	P	PII	K6	3D!	3Mx+	SSE	SSE2	A64	SSE3	E64T
NOT	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓

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not *rmDst(8/16/32/64)* [Un]signed

This instruction logically inverts the bits of the destination. All ones become zeros, and all zeros become ones.

Flags	O.flow	Sign	Zero	Aux	Parity	Carry
	-	-	-	-	-	-

Flags: None are affected by this opcode.

```
        mov     eax,00000a5a5h
        not     eax
; NOT 00000000000000001010010110100101b   00000a5a5h
;    11111111111111101011010010110101b   0ffff5a5ah
```

And guess what you get when you flip it again?

```
; NOT 11111111111111101011010010110101b   0ffff5a5ah
;    00000000000000001010010110100101b   00000a5a5h
```

The original value! Flip-flop.

NEG — Two's Complement Negation

Mnemonic	P	PII	K6	3D!	3Mx+	SSE	SSE2	A64	SSE3	E64T
NEG	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓

neg *rmDst(8/16/32/64)* [Un]signed

This instruction logically inverts the sign of the number.

Flags	O.flow	Sign	Zero	Aux	Parity	Carry
	X	X	X	X	X	X

Flags: Carry is cleared if the destination is 0; else it is set. The other bits are set accordingly from its results.

```
        mov     eax,00000a5a5h
        neg     eax
;   00000000000000001010010110100101b   00000a5a5h (42405)
;   11111111111111101011010010110101b   0ffff5a5bh (-42405)
```

Hint: For a NEG (two's complement negation), use an XOR followed by an increment.

```
    00000000000000001010010110100101b   00000a5a5h (42405)
NOT 11111111111111101011010010110101b   0ffff5a5ah (-42406)
INC 11111111111111101011010010110110b   0ffff5a5bh (-42405)
```

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