

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

QUALCOMM INCORPORATED,
Petitioner,

v.

COLLABO INNOVATIONS, INC.,
Patent Owner.

Case No. IPR2025-01015
U.S. Patent No. 7,930,575

**PETITION FOR *INTER PARTES* REVIEW OF U.S. PATENT NO. 7,930,575
UNDER 35 U.S.C. §§ 311-319 AND 37 C.F.R. § 42.100 *et seq.***

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List of Exhibits

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1001	U.S. Patent No. 7,930,575 (the “’575 Patent”)
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1003	Declaration of Murali Annavaram, Ph.D.
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1007	U.S. Patent No. 7,219,248 (“Shikata”)
1008	U.S. Patent No. 5,530,879 (“Crump”)
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1013	Petition for <i>Inter Partes</i> Review, <i>Advanced Micro Devices, Inc. v. Collabo Innovations Inc.</i> , IPR2019-01523, Paper 2 (P.T.A.B. Sep. 16, 2019) (“Jahagirdar IPR Petition”)
1014	Patent Owner’s Preliminary Response, <i>Advanced Micro Devices, Inc. v. Collabo Innovations Inc.</i> , IPR2019-01523, Paper 9 (P.T.A.B. Jan. 3, 2020) (“Jahagirdar POPR”)
1015	Decision Denying Institution of <i>Inter Partes</i> Review, <i>Advanced Micro Devices, Inc. v. Collabo Innovations Inc.</i> , IPR2019-01523, Paper 18 (P.T.A.B. Mar. 27, 2020) (“Jahagirdar Institution Decision”)
1016	Petition for <i>Inter Partes</i> Review, <i>Advanced Micro Devices, Inc. v. Collabo Innovations Inc.</i> , IPR2019-0152, Paper 2 (P.T.A.B. Sept. 16, 2019) (“Chung IPR Petition”)
1017	Patent Owner’s Preliminary Response, <i>Advanced Micro Devices, Inc. v. Collabo Innovations Inc.</i> , IPR2019-01524, Paper 9 (P.T.A.B. Jan. 3, 2020) (“Chung POPR”)
1018	Decision Denying Institution of <i>Inter Partes</i> Review, <i>Advanced Micro Devices, Inc. v. Collabo Innovations Inc.</i> , IPR2019-01524, Paper 13 (P.T.A.B. Mar. 30, 2020) (“Chung Institution Decision”)
1019	Complaint, <i>Collabo Innovations, Inc. v. Advanced Micro Devices, Inc.</i> , No. 1:18-cv-552, ECF 1 (W.D. Tex. July 2, 2018) (“AMD Complaint”)

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1020	Claim Construction Order, <i>Collabo Innovations, Inc.</i> , No. 1:18-cv-552, ECF 93 (W.D. Tex. July 5, 2023) (“AMD Claim Construction”)
1021	Michael J. Flynn, <i>Computer Architecture: Pipelined and Parallel Processor Design</i> (1995) (“Flynn Textbook”)
1022	Excerpts from <i>The Modern Dictionary of Electronics</i> (7th Ed. 1999)
1023	M.V. Wilkes, <i>Microprogramming</i> , AIEE-ACM-IRE: Papers and Discussions Presented at the Dec. 3-5, 1958 Easter Joint Computer Conference (1958) (“Wilkes Paper”)
1024	M.V. Wilkes, <i>The Growth of Interest in Microprogramming: A Literature Survey</i> , 1 Computing Surveys 139 (1969) (“Wilkes Survey”)
1025	David A. Patterson, <i>Microprogramming</i> , 248 Sci. Am. 50 (1983)
1026	Mutunori Igarashi et al., <i>A Low-power Design Method Using Multiple Supply Voltages</i> , in <i>Proceedings of 1997 International Symposium on Low Power Electronics and Design</i> , Monterey, CA 36 (1997) (“Igarashi”)
1027	Jui-Ming Chang & Massoud Pedram, <i>Energy Minimization Using Multiple Supply Voltages</i> , 5 IEEE Transactions on Very Large Scale Integration (VLSI) Systems 436 (1997) (“Chang”)
1028	U.S. Patent No. 7,174,472 (“Hill”)
1029	Zhigang Hu et al., <i>Microarchitectural Techniques for Power Gating of Execution Units</i> , in <i>Proceedings of 2004 International Symposium on Low Power Electronics and Design</i> 32 (2004) (“Hu”)
1030	Shekhar Borkar, <i>Design Challenges of Technology Scaling</i> , 19 IEEE Micro 23 (July-Aug. 1999) (“Borkar”)
1031	Lawrence T. Clark et al., <i>Standby Power Management for a 0.18μm Microprocessor</i> , in <i>Proceedings of 2002 International Symposium on Low Power Electronics and Design</i> 7 (2002) (“Clark”)
1032	Luca Benini et al., <i>A Survey of Design Technologies for System-Level Dynamic Power Management</i> , 8 IEEE Transactions on Very Large Scale Integration (VLSI) Systems 299 (2000) (“Benini”)

Exhibit	Description
1033	Resve Saleh et al., <i>System-on-Chip: Reuse and Integration</i> , 94 Proceedings of the IEEE 1050 (2006) (“Saleh”)
1034	Raj Nair & Bao Tang, <i>Low Cost On-Die CMOS Distributed Voltage Regulation for Microcontrollers</i> , in <i>Proceedings of the 24th European Solid-State Circuits Conference</i> 188 (1998) (“Nair”)
1035	L. Richard Carley & Akshay Aggarwal, <i>A Completely On-Chip Voltage Regulation Technique for Low Power Digital Circuits</i> , in <i>Proceedings of 1999 International Symposium on Low Power Electronics and Design</i> 109 (1999) (“Carley”)
1036	Sape J. Mullender, <i>Interprocess Communication: Computer Networks</i> , Ch. 1, 47 (1992) (“Mullender”)
1037	Howard Lee Morgan, <i>An Interrupt Based Organization for Management Information Systems</i> , 13 Communications of the ACM 734 (1970) (“Morgan”)
1038	A.C. Fischer-Cripps, <i>Newnes Interfacing Companion</i> (2002) (“Fischer-Cripps”)
1039	B Holdsworth & R.C. Woods, <i>Digital Logic Design</i> (2003) (“Holdsworth”)
1040	Jurij Silc et al., <i>Processor Architecture: From Dataflow to Superscalar and Beyond</i> (Springer 1999) (“Processor Architecture”)
1041	Preliminary Infringement Contentions, <i>Collabo Innovations, Inc. v. Qualcomm Inc.</i> , No. 6:24-cv-00472 (W.D. Tex. Dec. 6, 2024) (“Collabo’s Preliminary Infringement Contentions”)
1042	U.S. Patent No. 6,141,762 to Nicol et al. (“Nicol”)
1043	U.S. Patent No. 5,784,628 to Reneris (“Reneris”)
1044	U.S. Patent No. 6,804,632 B2 to Orenstien et al. (“Orenstien”)
1045	Excerpts from <i>The Authoritative Dictionary of IEEE Standard Terms</i> (7th Ed. 2000)
1046	Excerpts from <i>Microsoft Computer Dictionary</i> (4th Ed. 1999)
1047	Joint Claim Construction Statement, <i>Collabo Innovations, Inc. v. Qualcomm Inc.</i> , No. 6:24-cv-00472-ADA (W.D. Tex.)
1048	Opening Claim Construction Brief, <i>Collabo Innovations, Inc. v. Qualcomm Inc.</i> , No. 6:24-cv-00472-ADA, Dkt. 32 (W.D. Tex.)
1049	Responsive Claim Construction Brief, <i>Collabo Innovations, Inc. v. Qualcomm Inc.</i> , No. 6:24-cv-00472-ADA, Dkt. 33 (W.D. Tex.)

Exhibit	Description
1050	James Leiterman, <i>32/63-BIT 80x86 Assembly Language Architecture</i> , 2005 (“Leiterman”)
1051	U.S. Patent Application Publication No. 2004/0257898 (“Ozawa”)
1052	U.S. Patent No. 6,715,090 (“Totsuka”)

I. INTRODUCTION

Qualcomm Incorporated (“Qualcomm” or “Petitioner”) petitions for *inter partes* review seeking cancellation of claims 1-3, 5, 8, 11, 12, 15, and 16 (the “Challenged Claims”) of U.S. Patent No. 7,930,575 (“the ’575 Patent”), assigned to Collabo Innovations, Inc. (“Collabo” or “Patent Owner”). The ’575 Patent is directed to a microcontroller that reduces power consumption by disconnecting power to the CPU during standby mode. The patent notes that cutting off power may destroy the CPU’s internal state, resulting in longer restoration times upon wake-up. To address this issue, the ’575 Patent proposes saving the CPU’s internal state (i.e., the working context) before power is cut off and restoring it when exiting standby, thus enabling the CPU to resume operations quickly. The patent claims priority to an application filed in September 2006.

Before the priority date of the ’575 Patent, several companies had developed power-saving techniques similar to those described and claimed in the ’575 Patent. For example, U.S. Patent No. 7,293,183 (*Lee*) discloses a system-on-chip (SOC) that conserves power by placing its CPU into a power-off standby mode when the CPU is not in use for an extended period. Lee further discloses the process of saving the CPU’s working context before entering this mode and restoring that context upon exiting standby mode, enabling the CPU to resume its previous state. Assigned to Samsung, Lee claims priority from an application filed in Korea in August 2002,

four years before the priority date of the '575 Patent. Similarly, U.S. Patent No. 7,219,248 (*Shikata*) discloses a processor that reduces power consumption by putting its CPU into standby mode. Shikata discloses the process of saving the CPU's working context upon entering standby and restoring it upon exiting, allowing the CPU to resume operations. Assigned to Fujitsu, Shikata claims priority from an application filed in Japan in June 2004, two years before the priority date of the '575 Patent.

The '575 Patent discloses using a microprogram to facilitate saving and restoring the CPU's working context. While both *Lee* and *Shikata* explicitly address saving and restoring context, they assume that a skilled artisan would be knowledgeable of routine implementation details. In fact, U.S. Patent No. 7,664,970 (*Jahagirdar*), assigned to Intel, and U.S. Patent No. 5,530,879 (*Crump*), assigned to IBM, specifically utilize microprograms for saving and restoring the CPU's working context during entry and exit from standby modes. Petitioner's expert, Dr. Murali Annavaram, explains that microprograms have been prevalent in the computer industry since the 1960s, and that a skilled artisan would have been motivated to implement the save and restore functionality in Lee and in Shikata using microprograms instead of alternative methods. Therefore, the combinations of *Lee with Jahagirdar* and *Shikata with Crump* render most of the Challenged Claims

obvious, and render the remaining claims obvious in view of further references, as discussed in Section IX below.

II. MANDATORY NOTICES AND FEE AUTHORIZATION

A. Real Parties-in-Interest

The real parties-in-interest are Qualcomm Incorporated and Qualcomm Technologies, Inc.

B. Related Matters

Petitioner identifies the following related matter, *Collabo Innovations, Inc. v. Qualcomm Inc.*, 6:24-cv-00472 (W.D. Tex.) (“Qualcomm Texas Case”).

C. Lead and Back-Up Counsel

Petitioner designates the following counsel.

Lead Counsel	Back-Up Counsel
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Pursuant to 37 C.F.R. § 42.10 (b), Petitioner has filed a power of attorney with the above designation of counsel.

D. Service Information

Please address correspondence to counsel at the address above. Petitioner consents to electronic service to: Qualcomm-Collabo-IPR@cov.com and the email addresses listed above. Service information is provided in the designation of counsel above.

E. Fee Authorization

This Petition is accompanied by the fees set forth in 37 C.F.R. § 42.15(a). Please charge or credit Deposit Account No. 60-3160 with any shortage or overpayment of fees associated with this Petition and any other fees incurred by Petitioner.

III. GROUNDS FOR STANDING

Pursuant to 37 C.F.R. § 42.104(a), Petitioner certifies that the '575 Patent is available for *inter partes* review, and that Petitioner is not barred or estopped from requesting *inter partes* review based on the grounds identified in this petition.

IV. STATEMENT OF PRECISE RELIEF REQUESTED FOR EACH CLAIM CHALLENGED

A. Claims for Which Review Is Requested (37 C.F.R. §42.104(b)(1))

Petitioner requests cancellation of Claims 1-3, 5, 8, 11, 12, 15, and 16.

B. Statutory Grounds of Challenge (§42.104(b)(2))

Ground I: Claims 1, 3, 5, 8, 11, 12, 15, and 16 are unpatentable under §103 over US 7,293,183 (Ex-1005) (“Lee”) in view of US 7,664,970 (Ex-1006) (“Jahagirdar”).

Ground II: Claim 2 is unpatentable under §103 over Lee and Jahagirdar, further in view of US 5,502,689 (Ex-1010) (“Peterson”).

Ground III: Claim 3 is unpatentable under §103 over Lee and Jahagirdar, further in view of US 7,369,815 (Ex-1011) (“Kang”).

Ground IV: Claim 11 is unpatentable under §103 over Lee and Jahagirdar, further in view of US 7,167,991 (Ex-1009) (“Higashida”).

Ground V: Claims 1, 5, 11, 12, and 15 are unpatentable under §103 over US 7,219,248 (Ex-1007) (“Shikata”) in view of US 5,530,879 (Ex-1008) (“Crump”).

Ground VI: Claim 2 is unpatentable under §103 over Shikata and Crump, further in view of Peterson.

Ground VII: Claim 3 is unpatentable under §103 over Shikata and Crump, further in view of Kang.

Ground VIII: Claim 16 is unpatentable under §103 over Shikata and Crump, further in view of US 5,390,350 (Ex-1012) (“Chung”).

V. LEVEL OF ORDINARY SKILL IN THE ART

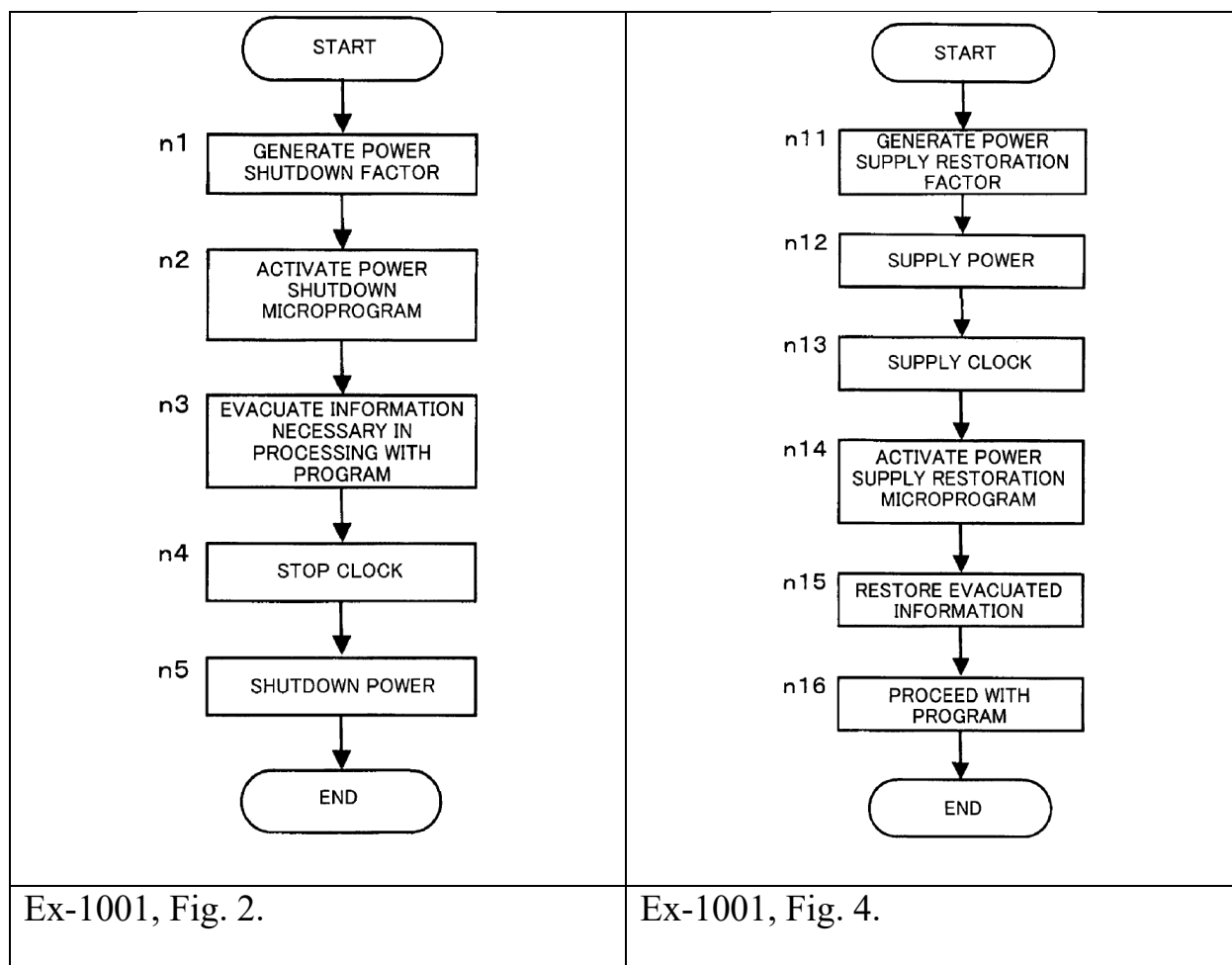
A person of ordinary skill in the art (“POSITA”) would have a B.S. degree in Computer Engineering, Electrical Engineering or an equivalent field along with 3 to 5 years of academic or industry experience in microprocessor architecture, design of computer systems, designs of computer chips, or comparable industry experience. A person with less education but greater pertinent and relevant industry experience would also meet the standard. Ex-1003 ¶45.

VI. THE ’575 PATENT

A. Overview

The ’575 Patent is titled “Microcontroller for Controlling Power Shutdown Process.” According to the “Summary of the Invention” section of the ’575 Patent, “it is a main object of the present invention to provide a microcontroller capable of easily and rapidly evacuating and restoring information necessary in proceeding with a program when realizing a standby state in which internal operation voltage supply is shutdown.” Ex-1001, 2:26-31.

Figure 2 is a flowchart showing the operation in a power shutdown process, and Figure 4 is a flowchart showing the operation of a power supply restoration process, Ex-1001, 7:22-24, 7:31-33; Ex-1003 ¶¶77-79.



B. Prosecution History

During prosecution, the Examiner rejected the pending claims as anticipated by U.S. Patent No. 7,167,991 (“Higashida”). Ex-1002, 246-51. In response to the rejection, the applicant amended independent claim 1, and argued that three features were not disclosed by Higashida. Ex-1002, 313-14, 323-25. First, the applicant argued that Higashida’s switch 16 was not the claimed power supply unit because it “does not *shut down power supply to the CPU upon receiving the power shutdown control signal from the power supply control unit.*” Ex-1002, 324. Second, the

applicant argued that Higashida’s SRAM was not the claimed information holding unit because it fails to disclose that information was stored *upon receiving the shutdown request signal*. Ex-1002, 324. Third, the applicant argued that Higashida did not disclose that the CPU branches to an address indicated by the program counter. Ex-1002, 324-25. Subsequently, the Examiner allowed the amended claims. Ex-1002, 337.

C. Litigation History

Patent Owner asserted the ’575 Patent against Advanced Micro Devices, Inc. (“AMD”) in a complaint that was filed on July 2, 2018. Ex. 1019. The Court issued a claim construction order on July 5, 2023. Ex. 1020. It appears that the parties subsequently reached a settlement in the case.

D. AMD IPRs

On September 16, 2019, AMD filed two IPR petition, one **IPR2019-01523 (Jahagirdar IPR)** relying upon Jahagirdar as the primary reference, Ex-1013, and other **IPR2019-01524 (Chung IPR)** relying up Chung as the primary reference. Ex-1016. On January 3, 2020, Patent Owner filed its preliminary responses (POPRs), arguing, among other things, that the claimed “microcontroller” was a single integrated chip, whereas the systems disclosed in Jahagirdar and Chung were a set of multiple chips. Ex-1014, 16-24; Ex-1017, 15-19. On March 7, 2020, the PTAB issued its decisions declining to institute the petitions, Ex-1015 and Ex-1018, noting

that the constructions proposed by both parties required the microcontroller to be a single integrated chip whereas prior art disclosed multi-chip systems. Ex-1015, 7; *see also* Ex-1015, 11; Ex-1018, 10.

VII. CLAIM CONSTRUCTION

In the related Qualcomm Texas Case, the parties agreed to the following construction. Ex-1047, 2.

Term	Agreed Construction
Whether the preamble of claim 1 (“a microcontroller”) is limiting. (claim 1)	The preamble of claim 1 is limiting.
“power supply device” (claim 1)	“power supply”
“restores the information necessary in proceeding with the program and evacuated in the information holding unit in time of power shutdown” (claim 1)	“Restores the information necessary to proceed with the program, the information was evacuated from the CPU in the information holding unit in the power shut down process”
“a power shutdown range” (claims 11 and 12)	“circuit for which power supply will be shutdown”

In the Qualcomm Texas Case, the parties dispute the construction of four terms discussed below.¹

A. microcontroller (claims 1-3, 5, 8, 11, 12, 15, and 16)

Petitioner’s Construction	Patent Owner’s Construction
“a single integrated chip as opposed to a set of multiple chips (a ‘chipset’)”	Plain and ordinary meaning

¹ Petitioner also argues that claims 2 and 8 are indefinite in the Qualcomm Texas Case, but assumes for the purpose of this petition that those claims are not indefinite.

Petitioner has proposed a construction for “microcontroller” based on Patent Owner’s clear and unmistakable disclaimers in its responses in IPR2019-01523 & IPR2019-01524 (collectively, “AMD IPRs”). As described in Section VI.D above, Patent Owner argued to the Board that a “microcontroller” must be a “single integrated chip.” Ex-1014, 18 (“Regardless of which construction [of microcontroller] is used in this proceeding, both constructions require the microcontroller to be on a single integrated chip.”); Ex-1017, 15 (same). Patent Owner then expressly distinguished the asserted prior art references on the basis that they disclosed multi-chip systems or chipsets, not single integrated chips. Ex-1014, 23-24 (“As shown above, the ‘board’ is not a single ‘chip,’ but rather is a set of multiple chips (a ‘chipset’) Because Jahagirdar’s multi-chip system is not integrated on a single chip, it does not teach a ‘microcontroller’ under either party’s construction.”); Ex-1017, 17 (“Chung’s multi-chip system is not integrated on a single chip, and thus does not teach a ‘microcontroller’ under either party’s construction.”).

The Board expressly relied on Patent Owner’s statements in deciding not to institute the IPRs. Ex-1015, 7 (“We agree with Patent Owner that, as both parties’ constructions reflect, a microcontroller must be a single, integrated chip.”); Ex-1018, 7 (same); *see also* Ex-1015, 11. This gives rise to a binding disclaimer which narrows claim scope, under the doctrines of both prosecution disclaimer and judicial

estoppel. *Aylus Networks, Inc. v. Apple Inc.*, 856 F.3d 1353, 1361-62 (Fed. Cir. 2017) (statements in a POPR may give rise to prosecution disclaimer); *Trs. of Columbia Univ. v. NortonLifeLock, Inc.*, No. 3:13cv808, 2019 WL 7040931, at *4-5 (E.D. Va. Dec. 20, 2019) (applying judicial estoppel based on IPR arguments).

B. microprogram (claims 1 and 8)

Petitioner's Construction	Patent Owner's Construction
“a control program (or a microcode) that runs at the lowest level of the hardware to control internal source of the CPU to execute command, interrupt processing, and the like, and is held entirely within the CPU as opposed to a program that is held in main memory until executed”	Plain and ordinary meaning

Likewise, Petitioner proposes a construction of “microprogram” which directly reflects statements Patent Owner made in the AMD IPRs.

“Microprogram” is described in the ’575 Patent specification as “the control program for controlling internal sources of the CPU 1 in order to execute command, interrupt processing, and the like.” Ex-1001, 9:46-49. However, in the AMD IPRs, Patent Owner distinguished “microprograms” from “programs,” further clarifying the meaning of “microprogram” as used in the ’575 Patent. In particular, Patent Owner argued the claimed “microprogram,” or microcode, must (1) “run[] at the lowest level of the hardware” and (2) be “held entirely within the CPU,” as opposed to (3) being a program “held in the main memory of the computer system until

executed by the CPU.” Ex-1014, 54-55; Ex-1017, 28. The distinction between a “microprogram” and a “program” was significant: Patent Owner argued that Chung’s disclosure of a “register-saving program” was insufficient disclosure of the “microprogram” limitation of the ’575 Patent because there was no evidence that “Chung’s ‘register saving program’ is a microprogram.” Ex-1017, 29.

As with “microcontroller,” Patent Owner’s clear statements about the meaning of “microcontroller” to this Board are a narrowing disclaimer. *Aylus*, 856 F.3d at 1360. Petitioner’s proposed construction accurately reflects this disclaimer.

C. power shutdown microprogram (claims 1 and 8)

Petitioner’s Construction	Patent Owner’s Construction
“a microprogram that evacuates the information necessary in proceeding with the program to the information holding unit, and then outputs the evacuation completed signal to the power supply control unit”	Plain and ordinary meaning

Petitioner’s construction of “power shutdown microprogram” reflects the structure of claim 1 and the disclosures of the ’575 Patent’s specification. The structure of the claim implies that the execution of the “power shutdown microprogram” performs the evacuation function and then outputs the evacuation completed signal. Ex-1001, 18:59-64.

That implication is confirmed by the description of “power shutdown microprogram” appearing in a passage from the specification purporting to describe

“the features of ‘the present invention’ as a whole” in the Summary of the Invention section of the ’575 Patent. *Cf. Verizon Servs. Corp. v. Vonage Holdings Corp.*, 503 F.3d 1295, 1308 (Fed. Cir. 2007) (citation omitted) (noting that statements describing invention as a whole carry increased weight). The specification confirms that it is the power shutdown program itself which performs the evacuation and signaling functions. Ex-1001, 2:62-65.

Embodiment 1 lends further support to this conclusion, explaining that, in Figure 1 of the ’575 Patent, “[t]he power shutdown microprogram μ P1 evacuates the information (PC, PSW, SP, etc.) necessary in proceeding with the program to the information holding unit 4 or the register via the internal bus 6 in step n3, and lastly outputs the evacuation completed signal S2 to the power supply control unit 2.” Ex-1001, 9:50–54.

Petitioner’s construction confirms that it is a “microprogram” that saves and restores context within the scope of the ’575 Patent. Patent Owner disavowed the use of a “program” for saving and restoring information when it argued in the AMD IPRs that “register-saving *program*” employed by Chung was not the claimed microprogram. Ex-1017, 29 (“There is no indication in Chung that the register-saving program is a microprogram.”). Patent Owner cannot now expand the scope of the claims by arguing that the CPU can evacuate and restore information using a “program.”

D. power supply restoration microprogram (claims 1 and 8)

Petitioner's Construction	Patent Owner's Construction
"a microprogram that restores the information necessary in proceeding with the program and evacuated in the information holding unit to the CPU, and then branches the processes to the addresses indicated by the program counter to continue the program execution from the shutdown state"	Plain and ordinary meaning

Similarly, claim 1 implies that execution of a "power supply restoration microprogram" performs the evacuation and branching functions. Ex-1001, 19:18-24. This is confirmed by the specification's description of the "invention as a whole." Ex-1001, 4:1-6. Embodiment 1 likewise supports this understanding. Ex-1001, 10:18-27.

VIII. OVERVIEW OF PRIOR ART

A. U.S. 7,293,183 (Lee)

Lee, filed on August 26, 2003, predates the foreign application priority date of the '575 Patent, which is September 12, 2006. Lee is prior art under pre-AIA 35 U.S.C. § 102(e).

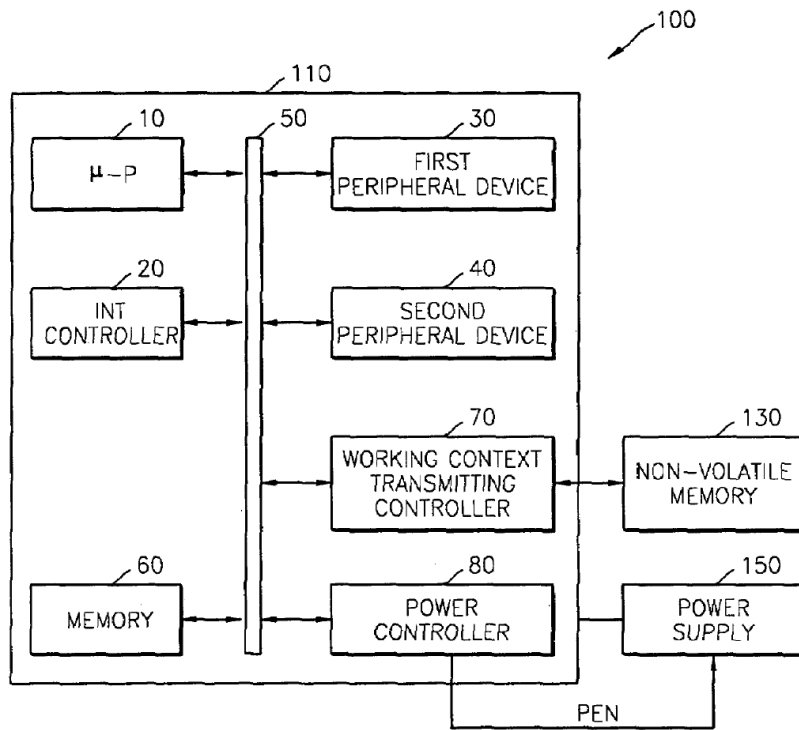
In the "Background of the Invention" section, Lee discusses that portable devices, such as mobile phones utilizing a system-on-a chip (SOC) design, employ a standby mode to minimize power consumption. Ex-1005, 1:24-25. According to Lee, "[t]he most common method of reducing power consumption in a standby mode

is to cut off a clock signal supplied to all or several circuits of a SOC and reduce the amount of dynamic current consumed by all or several circuits of the SOC.” Ex-1005, 1:30-34. To conserve power even further, Lee notes that “some SOC’s use a power-off standby mode, during which power supplied to all or several circuits of the SOC’s ... is cut off to remove static leakage current generated in the SOC’s.” Ex-1005, 1:43-47.

Lee identifies a challenge associated with such SOC designs: “when the power supplied to the SOC’s is cut off, the working context of all or several circuits of the SOC’s is lost,” necessitating a lengthy boot-up process once power is restored. Ex-1005, 1:48-55. To address this, Lee discloses a method for preserving the working context prior to cutting off the power supply, allowing the SOC to quickly return to its previous state upon power restoration. Ex-1005, 1:63-67.

Figure 1 of Lee depicts an example system 100 including an SOC 110. Ex-1005, 5:35-40; Ex-1003 ¶¶96-97.

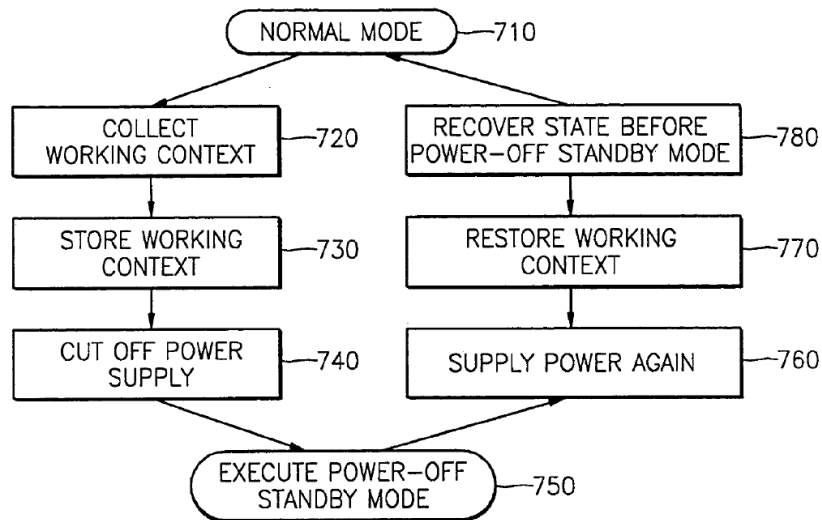
FIG. 1



Ex-1005, Fig. 1.

Figure 7 depicts the steps to store and recover working context. Ex-1005, 10:4-6; Ex-1003 ¶¶98-111.

FIG. 7



Ex-1005, Fig. 7. Note that the arrows from 760 to 770 and from 770 to 780 should point upwards.

B. U.S. 7,219,248 (Shikata)

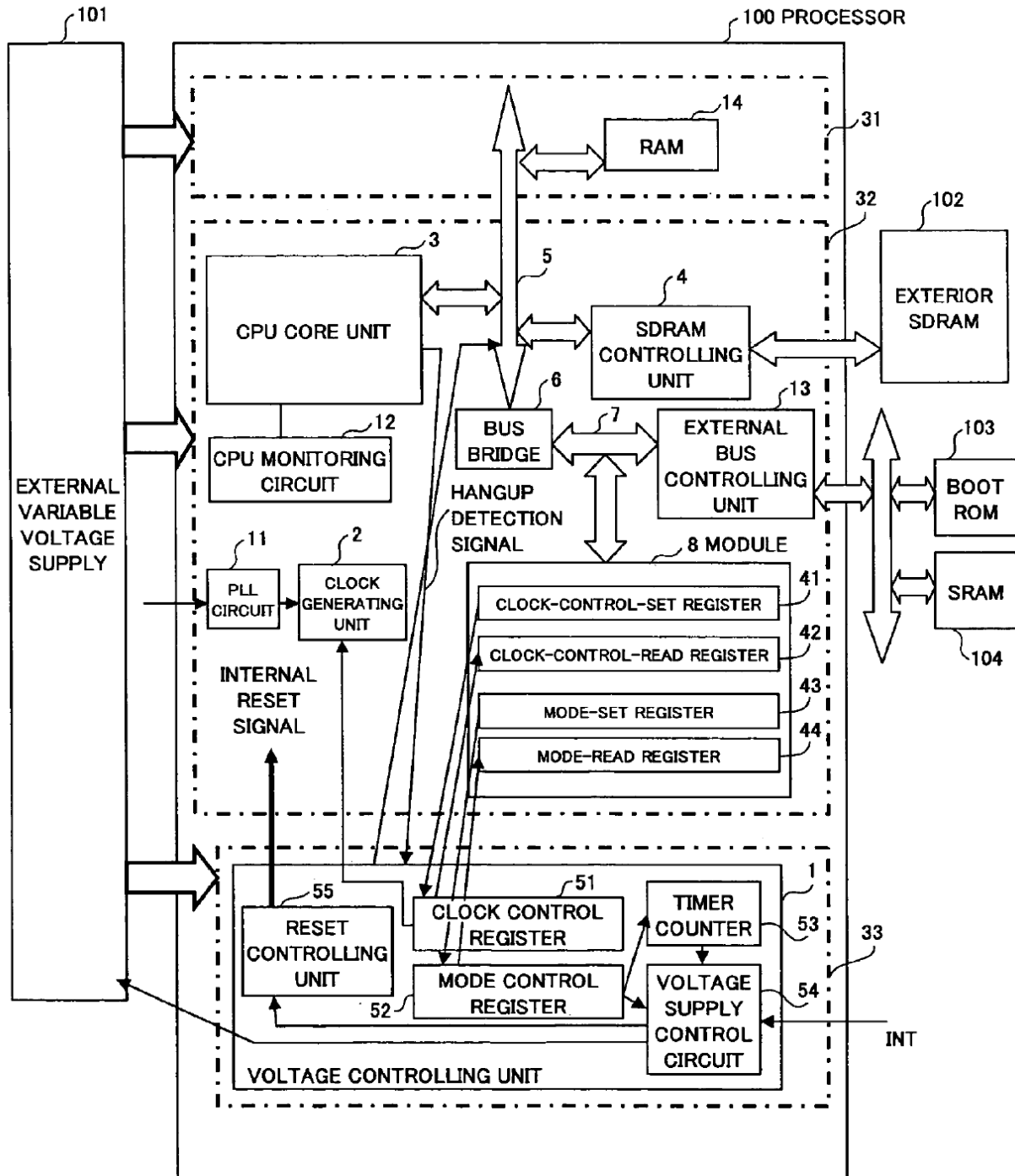
Shikata, filed on October 20, 2004, predates the foreign application priority date of the '575 Patent, which is September 12, 2006. As such, Shikata is prior art under pre-AIA 35 U.S.C. § 102(e).

Shikata relates to “a semiconductor integrated circuit which controls a power supply voltage for the purpose of reducing power consumption.” Ex-1007, 1:17-20. Specifically, Shikata discloses a system that enters a standby state by saving register values, suspending the clock signal, and halting power supply. Ex-1007, 8:21-42. Subsequently on wake-up, the system exits the standby state by resuming the power

supply, restarting the clock signal, and restoring register values, thereby continuing the execution of the application program. Ex-1007, 8:46-65.

Figure 5 depicts an example system. Ex-1007, 7:4-7; Ex-1003 ¶¶114-17.

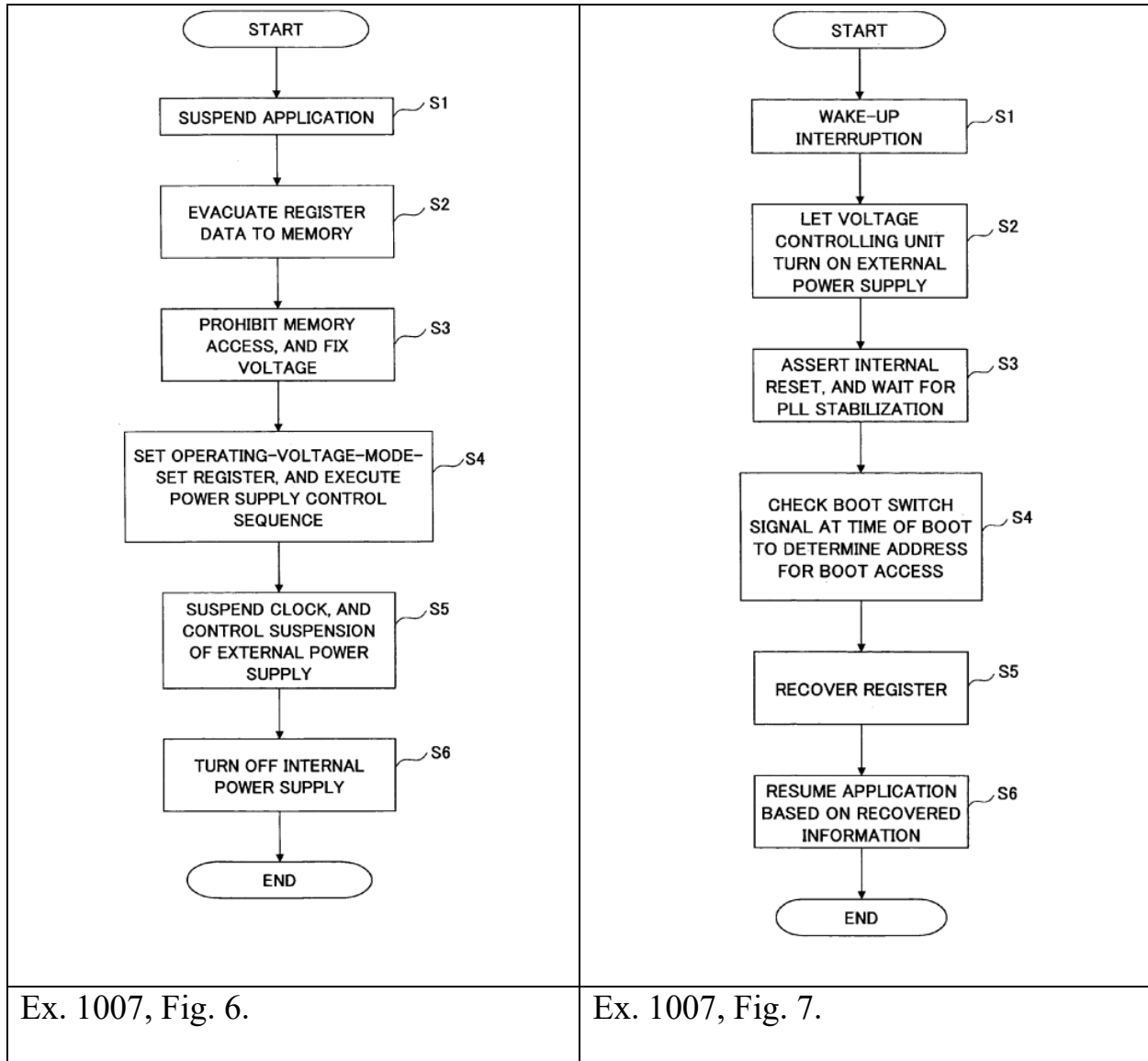
FIG.5



Ex-1007, Fig. 5.

Figures 6 and 7 depict the steps to transition to, and out of, a standby state.

Ex-1007, 8:18-20, 8:43-45; Ex-1003 ¶¶118-26.



C. U.S. 7,664,970 (Jahagirdar)

Jahagirdar, filed on December 30, 2005, predates the foreign application priority date of the '575 Patent, which is September 12, 2006. As such, Jahagirdar is prior art under pre-AIA 35 U.S.C. § 102(e).

Jahagirdar “relates to a method and apparatus for a zero voltage processor sleep state.” Ex-1006, Abstract. It describes a processor designed to save its critical state before the power is turned off to reduce power consumption. Ex-1006, 3:4-23. Upon a request to restore power, the processor reinstates the critical state. Ex-1006, 3:24-28. Jahagirdar explains employing microcode for the save and restore functions. Ex-1006, 8:45-52.

Besides controlling power states, Jahagirdar also addresses the management of clock signals, including turning them on or off. Ex-1006, 5:27-42, 10:46-54, 11:41-48.

D. U.S. 5,530,879 (Crump)

Crump, issued on June 25, 1996, predates the filing date of the '575 Patent, which is September 10, 2007, by over eleven years. As such, Crump is prior art under pre-AIA 35 U.S.C. § 102(b).

Crump discloses a system designed to transition into to a suspend state to conserve power and to resume normal operation upon wake-up. Ex-1008, 14:50-57, 14:63-66. Specifically, Crump discloses the use of a microcontroller that sends an

interrupt signal to the CPU, prompting it to save its state prior to the discontinuation of the power supply. Ex-1008, 21:53-22:3. The saving of the CPU state is accomplished through the use of microcode. Ex-1008, 22:4-6, 37:1-13, Fig. 10A.

E. U.S. 5,502,689 (Peterson)

Peterson, issued on March 26, 1996, predates the filing date of the '575 Patent, which is September 10, 2007, by over eleven years. As such, Peterson is prior art under pre-AIA 35 U.S.C. § 102(b).

Peterson discloses a clock generator that reduces power consumption by disabling the output clock signal upon receiving a shutdown entry request signal, provided that the signal meets a predetermined protocol requirement. Ex-1010, 1:59-62, 3:40-60; *see also id.*, 7:59-8:16.

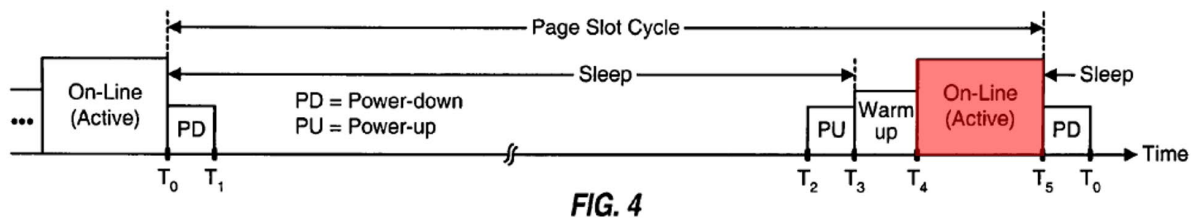
F. U.S. 7,369,815 (Kang)

Kang, with a filing date of February 24, 2004, and a provisional application date of September 19, 2003, predates the foreign application priority date of the '575 Patent, which is September 12, 2006. As such, Kang is prior art under pre-AIA 35 U.S.C. § 102(e).

Kang is directed to “conserving power for a wireless terminal.” Ex-1011, 1:12-14. Kang teaches that “[a] wireless terminal (e.g., a cellular phone) in a cellular communication system is only sporadically active and remains in an ‘idle’ mode for significant periods of time when no call is in progress.” Ex-1011, 1:16-19. “To

ensure that the terminal can still receive messages sent to it by the system, the terminal periodically monitors a paging channel.” Ex-1011, 1:19-21.

Kang explains that the system assigns each terminal a specific “slot” for the paging channel. Ex-1011, 1:19-21. “[T]he terminal enters an ‘active’ state prior to its assigned slot, monitors the paging channel for messages, and transitions to an ‘inactive’ state if additional communication is not required.” Ex-1011, 1:31-34. In the inactive state, the terminal “deactivates as much circuitry as possible to conserve power.” Ex-1011, 1:35-37. Such a “[p]ower collapse is typically performed in conjunction with a sleep timeline that indicates when the wireless terminal can go to sleep.” Ex-1011, 2:12-14. Figure 4 of Kang depicts an example annotated timeline. Ex-1011, 2:52-53.



Ex-1011, Fig. 4 (annotated).

During the assigned slot (T_4 to T_5) (red) for the paging channel, the terminal must be active to process the paging channel, after which it returns to sleep mode. Ex-1011, 8:31-35.

G. U.S. 7,167,991 (Higashida)

Higashida, filed on July 10, 2001, predates the foreign application priority date of the '575 Patent, which is September 12, 2006. As such, Higashida is prior art under pre-AIA 35 U.S.C. § 102(e).

Higashida discloses a system with two power supply regions. Ex-1009, 5:28-30, Fig. 1. In a standby state, the voltage of a backup power supply region is set low, just enough to hold the content of an SRAM in the backup power supply region. Ex-1009, 12:62-65, 13:8-13; *see also id.*, 13:30-45.

H. U.S. 5,390,350 (Chung)

Chung, issued on February 14, 1995, predates the filing date of the '575 Patent, which is September 10, 2007, by over 12 years. As such, Chung is prior art under pre-AIA 35 U.S.C. § 102(b).

Chung is directed to “integrated circuit chip core logic system controllers for minimizing power consumption by a microprocessor.” Ex-1012, 1:9-12. Specifically, Chung discloses powering down CPUs on sleep and resuming operation on wake-up. Ex-1012, 31:4-6. If a CPU has been inactive for a predetermined length of time, it “executes the register-saving program where the content of all registers and other status indications are saved in a predetermined area of RAM 30 for subsequent retrieval during the resume operation.” Ex-1012, 31:52-66. In addition, the system controller “tristates the output driver for the clock at CPUCLK 34 preventing clock

pulses to the CPUs.” Ex-1012, 32:12-13. The system controller then disables power to the CPUs, but does not disable power to other system components. Ex-1012, 32:14-19. Then, during the power resume operation, the system controller resumes power supply to the CPUs, and starts providing clocks pulses. Ex-1012, 32:29-40, 34:56-59. After the power resume operation, the CPU “can now continue operation from the condition at which it was originally stopped and powered down.” Ex-1012, 35:10-19.

IX. REASONS FOR RELIEF REQUESTED (§§42.22(a)(2), 42.104(b)(4))

A. Ground I: Lee and Jahagirdar Render Obvious Claims 1, 3, 5, 8, 11, 12, 15, and 16

1. The Combination of Lee and Jahagirdar

Lee discloses the essence of the alleged invention claimed in the ’575 Patent, which involves saving the context upon entering standby mode and restoring it upon exiting. Lee also discloses an SOC that contains all the key components arranged as claimed by the ’575 Patent. In describing its SOC, Lee assumes that a POSITA would be aware of routine implementation details that are well-known and well-understood in the art.

First, Lee assumes that a POSITA would understand the necessity of a clock in an SOC and know how to integrate it within the SOC. Lee acknowledges that the clock plays an essential yet routine role, as identified in the “Background of the Invention” section, where Lee states that SOC typically include clock systems and

that disabling clock signals is “[t]he most common method” for reducing power consumption. Ex-1005, 1:30-36. Jahagirdar discloses a system that has the same purpose as Lee’s and offers details about a clock generator that provides and suspends clock signals to various circuits as required. Ex-1006, 5:27-42, 10:46-54, 11:41-48. Dr. Annavaram explains that a POSITA would have recognized the necessity of a clock in digital design. Ex-1003 §§VII.B.2, XII.A.1.

Second, while Lee discusses the save and restore functionality of saving the CPU’s working context, sending a completion signal upon saving the context, and restoring the context, Lee assumes that POSITA would know how to efficiently implement this functionality. Ex-1005, 1:63-67, 6:46-49. Jahagirdar discloses the use of microprograms (or microcode) for saving and restoring the working context when entering and exiting standby modes. Ex-1006, 8:45-52. Dr. Annavaram explains that a POSITA would have appreciated that utilizing microcode for implementing the save and restore functionality provides a more effective method compared to other available options. Ex-1003 §§VII.B.4, XII.A.1.

In implementing Lee’s systems, a POSITA would likely have consulted analogous art, such as Jahagirdar. Both Lee and Jahagirdar pertain to digital systems designed to reduce power consumption by cutting off power. Ex-1005, 6:49-54; Ex-1006, 5:27-42, 10:46-54. Both disclose techniques for saving working contexts before power off, Ex-1005, 6:21-41; Ex-1006, 10:32-45, and restoring them upon

power-on to enable quick resumption of normal operations, Ex-1005, 9:59-10:3; Ex-1006, 11:41-48.

Integrating Jahagirdar's clock generator and microcode into Lee's systems would have been a combination of prior art elements according to known methods to yield predictable results. Ex-1003 §§XII.A.1-2. Dr. Annavaram explains that clock generators were both fundamental and pervasive components of circuit design, and the benefits of using microcode were widely recognized. Ex-1003 §§XII.A.2 & 4. Thus, a POSITA would have seen it as obvious to apply Jahagirdar's clock generator and microcode to Lee's systems, yielding predictable results. Ex-1003 ¶173. Specifically, a POSITA would recognize that clocks are essential in digital designs and that microcode provides a superior solution in terms of flexibility and low latency compared to hardware-based or program-based alternatives. Ex-1003 ¶173. A POSITA would have assessed the pros and cons of each approach and recognized the obvious choice of microcode for its balanced attributes of flexibility and low latency over the hardware-based or program-based solutions. Ex-1003 ¶173.

A POSITA would have had a reasonable expectation of success in using Jahagirdar's clock generator and microcode in Lee's systems. Ex-1003 ¶173. In digital systems like Lee's, the inclusion of a clock generator is critical yet routine for proper operation. Ex-1003 ¶173. Furthermore, employing microcode is a standard procedure for implementing saving and restoring functions. Ex-1003 ¶173.

The decision to use microcode, hardware, or program hinges on the requirement for flexibility and latency. Ex-1003 §§XII.A.4. A POSITA would have been well-acquainted with the efficiency and adaptability offered by using microcode. *Id.*

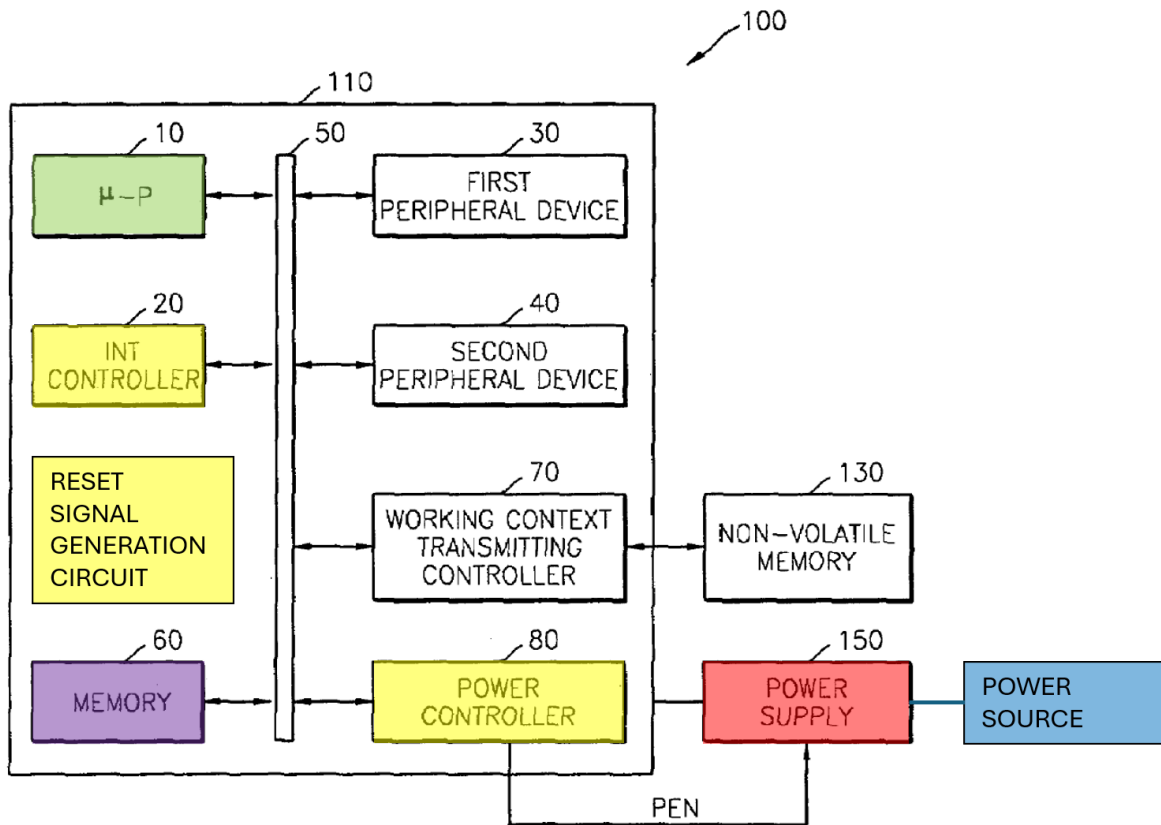
2. Claim 1

Lee in view of Jahagirdar renders claim 1 obvious.

[1pre]

Lee discloses an “apparatus and method that can minimize power consumption” within a system-on-a chip (SOC) design. Ex-1005, 1:59-62; *see also id.*, 5:37-38. Annotated Figure 1 depicts a system 100 including an SOC 110. Ex-1005, 5:35-40.

FIG. 1



Ex-1005, Fig. 1 (annotated with highlights and additional blocks of power source and reset signal generation circuit, as further discussed below).

Lee explains that “SOC means that a plurality of systems having independent functions are mounted on one semiconductor chip.” Ex-1005, 1:27-29. Therefore, Lee’s SOC is “a single integrated chip as opposed to a set of multiple chips (a ‘chipset’)” required by Petitioner’s proposed construction of *microcontroller*.

a) [1a]

Lee discloses that its SOC includes a microprocessor 10 (green). Ex-1005, 5:52-60; *see also id.* 5:35-41, Fig. 1. A POSITA would recognize that the microprocessor is the claimed *CPU* (Central Processing Unit). Ex-1003 ¶177.

b) [1b]

Lee discloses a power supply 150 (i.e., the claimed *power supply unit*) (red), which “supplies a predetermined operating power to the SOC 110.” Ex-1005, 5:48-49. The power supply 150 “may be implemented as an *on-chip regulator* inside the SOC.” Ex-1005, 5:49-51 (emphasis added). A POSITA would understand that the power supply 150 (red) is connected to the microprocessor 10 (green) within the SOC 110 because power is necessary for its operation. Ex-1003 ¶178.

Moreover, a POSITA would understand that the power supply 150 is connected to a power source (blue) providing AC or DC power, given that an on-chip regulator within an SOC requires a power source in order to deliver power to the microprocessor. Ex-1003 ¶178. Such a power source corresponds to the claimed *power supply device*, which the parties agree means “power supply.” Ex-1003 ¶178. Thus, a POSITA would understand that the power supply 150 (i.e., the claimed *power supply unit*) is *arranged between CPU and a power supply device for supplying power to the CPU*. Ex-1003 ¶178.

c) [1c]

Lee discloses an (1) interrupt controller 20, (2) a reset signal generation circuit, and (3) a power controller 80, which jointly constitute the claimed *power supply control unit for controlling the CPU and the power supply unit* (yellow). Ex-1005, 6:14-25, 9:44-64, 6:46-54. The interrupt controller 20 *controls* the microprocessor (i.e., the claimed *CPU*) by sending interrupt signals that prompt the microprocessor to transmit working contexts to memory. Ex-1005, 6:14-25. Additionally, the reset signal generation circuit also *controls the CPU* by dispatching a reset release signal to the microprocessor, enabling the restoration of the working contexts. Ex-1005, 9:44-64. Furthermore, the power controller 80 *controls* the power supply 150 (i.e., the claimed *power supply unit*) by issuing a power control signal (PEN) to the power supply to turn power on or off. Ex-1005, 6:46-54, 9:25-32.

d) [1d]

Upon receiving an interrupt signal from the interrupt controller, the microprocessor (green) “transmits all working contexts stored in all registers of the first peripheral device 30, the second peripheral device 40, and the microprocessor 10 to the memory 60 [purple].” Ex-1005, 6:21-25. Therefore, the memory 60 is the

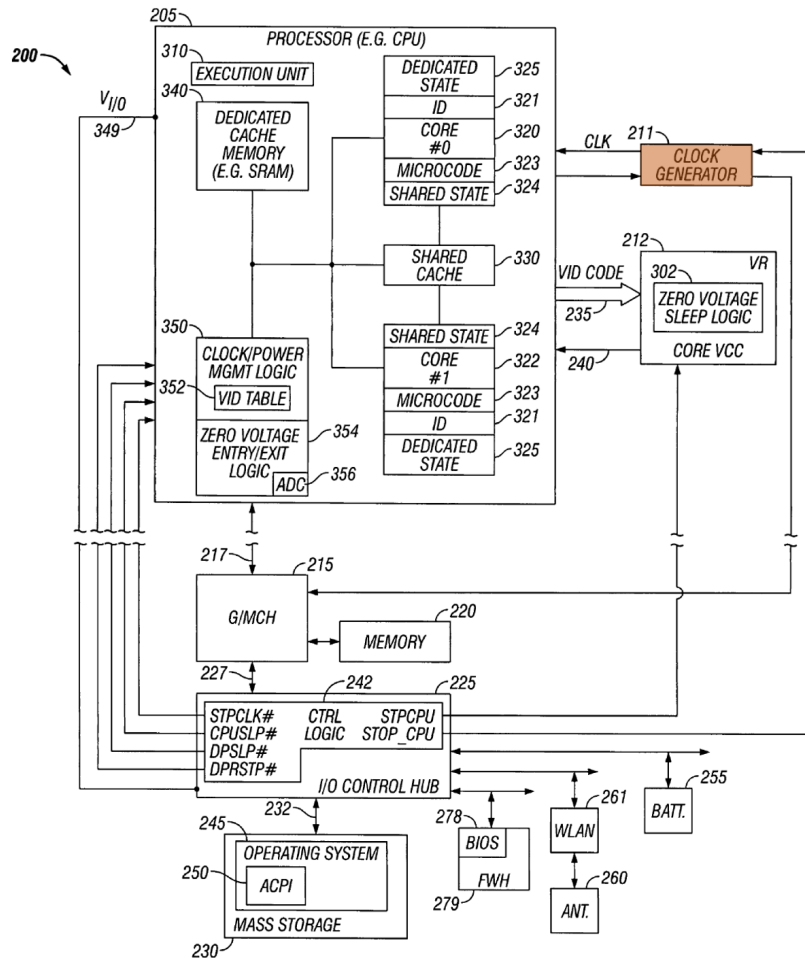
claimed *information holding unit for holding information evacuated from the CPU*.²

Additionally, a POSITA would understand that “all working contexts stored in all registers” of the microprocessor (i.e., the claimed *information evacuated from the CPU*) includes information *necessary in proceeding with a program* that was active when the microprocessor received the interrupt signal. Ex-1003 ¶180.

e) [1e]

Jahagirdar discloses a clock generator (brown). Ex-1006, 3:58-59; *see also id.*, 7:18-22, Fig. 1.

² The content of the memory 60 is also subsequently stored in a non-volatile memory 130, Ex-1005, 6:26-36, but the memory 60 on its own meets the claimed limitation.



Ex. 1006 (Jahagirdar), Figs. 2A-B (annotated).

As discussed in Section IX.A.1 above, incorporating a clock control mechanism into Lee's systems, based on Jahagirdar's teachings, would have been obvious. Ex-1003 §§XII.A.1-2. In implementing Lee's systems, it would have been obvious for a POSITA to incorporate the clock generator within the SOC because a POSITA would have appreciated the benefits of higher integration, such as an increase in performance, lower power consumption, and lower production costs. Ex-1003 ¶181 (citing Ex-1051 & Ex-1052). As Dr. Annavaram explains, integrating a

greater number of circuit blocks on a single semiconductor die enhances performance. Ex-1003 §VII.B.5. Furthermore, this higher level of integration leads to reduced power consumption. Ex-1003 ¶¶67-68. Additionally, it contributes to lower production costs. Ex-1003 ¶69. There would have been a reasonable expectation of success in implementing this change, as integrating a clock generator within a single-die system had been implemented routinely and successfully. Ex-1003 ¶181.

f) [1f]

Lee discloses that the interrupt controller (i.e., a component of the claimed *power supply control unit*) sends an interrupt signal to the microprocessor (i.e., *outputs a shutdown request signal to the CPU*) when “a predetermined time set by a user has passed or a user selects a power-off standby mode” (i.e., *in response to an occurrence of a power shutdown factor*). Ex-1005, 6:10-20. A POSITA would understand that the interrupt signal from the interrupt controller to the microprocessor corresponds to the claimed *shutdown request signal to the CPU* because it is initiated when a user selects a “power-off standby mode,” prompting the microprocessor to transmit working contexts to the memory in anticipation of entering the power-off standby mode. Ex-1005, 6:21-25, 6:46-54.

g) [1g]

As discussed in Section IX.A.2.f above, the microprocessor (i.e., the claimed *CPU*), in response to the interrupt signal (i.e., *upon receiving the shutdown request signal*), transmits working contexts to the memory, i.e., *evacuates the information necessary in proceeding with the program to the information holding unit*. Ex-1005, 6:21-25. After the working contexts have been saved, the microprocessor (i.e., the claimed *CPU*) outputs a predetermined command signal (i.e., the claimed *evacuation completed signal*) to the power controller (i.e., the claimed *power supply control unit*). Ex-1005, 6:46-49.

Jahagirdar teaches using microcode to save (i.e., *evacuate*) the CPU state. Ex-1006, 8:45-52; *see also id.*, 9:40-48, 10:18-38. A POSITA would understand that “microcode” and “microprogram” are synonymous, recognizing Jahagirdar’s microcode as the claimed *microprogram* under Petitioner’s proposed construction. Ex-1003 ¶¶183-87. Patent Owner admitted that microcode and microprogram are synonymous. Ex-1017, 28 (“In many CPUs, these individual instructions are performed by executing a microprogram or microcode comprised of microinstructions.”).

Additionally, Lee in view of Jahagirdar suggests the claimed *power shutdown microprogram*, which is “a microprogram that evacuates the information necessary in proceeding with the program to the information holding unit, and then outputs the

evacuation completed signal to the power supply control unit” under Petitioner’s proposed construction. As discussed above, Lee discloses *evacuating the information necessary in proceeding with the program to the information holding unit, and outputting an evacuation completed signal to the power supply control unit after evacuation is completed*. Implementing Lee’s evacuation function, including sending the above mentioned predetermined command signal, by adopting Jahagirdar’s approach of using microcode would have been obvious, as discussed in Section IX.A.1 above. Ex-1003 §§XII.A.1-2, ¶¶188-89.

h) [1h]

Lee discloses that “[t]he power controller 80 [i.e., a component of the claimed *power supply control unit*] responds to the predetermined command signal [i.e., the claimed *evacuation completed signal*] output from ... the microprocessor 10 to output a power control signal PEN to the power supply 150 [i.e., the claimed *power supply unit*].” Ex-1005, 6:46-49. The power control signal PEN corresponds to the claimed *power shutdown control signal*, as in response to PEN, the power supply 150 discontinues the supply of power. Ex-1005, 6:49-54.

i) [1i]

As discussed in Section IX.A.2.h above, the power supply 150 (i.e., the claimed *power supply unit*) discontinues power delivery to the microprocessor (i.e., *shuts down power supply to the CPU*) in response to the power control signal PEN

from the power controller (i.e., *upon receiving the power shutdown control signal from the power supply control unit*). Ex-1005, 6:49-54.

j) [1j]

As discussed in Section IX.A.2.h above, Lee discloses that “[t]he power controller 80 [i.e., a component of the claimed *power supply control unit*] responds to the predetermined command signal [i.e., the claimed *evacuation completed signal*] ... to output a power control signal PEN.” Ex-1005, 6:46-50.

Jahagirdar discloses an input/output controller that manages clock signals in addition to power. Ex-1006, 5:27-42. Jahagirdar discloses that the input/output controller sends a STOP_CPU signal (i.e., the claimed *clock stop control signal*) to “the clock generator 211 to cause the clock generator to halt the clock signal CLK to the CPU 205.” Ex-1006, 7:19-22; *see also id.*, 7:12-18.

As discussed in Section IX.A.1 above, utilizing Jahagirdar’s teachings to implement a clock control mechanism in Lee’s systems would have been obvious. Ex-1003 §§XII.A.1-2. Specifically, Lee’s power controller would send a clock stop control signal to the clock generator, as well as sending the power control signal PEN to the power supply 150. Ex-1003 ¶¶193-96.

k) [1k]

Lee discloses that the power controller (i.e., a component of the claimed *power supply control unit*) sends “a power control signal PEN” (i.e., the claimed

power supply control signal to the power supply 150 (i.e., the claimed *power supply unit*) “when a user releases a power-off standby mode ... or when a predetermined standby time set by the user has passed,” i.e., *in response to an occurrence of a power supply restoration factor*. Ex-1005, 9:25-32.

l) [1l]

Lee discloses that when the power supply 150 (i.e., the claimed *power supply unit*) receives the power control signal PEN (i.e., the claimed *power supply control signal*), it resumes delivering power to the microprocessor (i.e., the claimed *CPU*). Ex-1005, 9:25-32.

m) [1m]

Lee discloses a reset signal generation circuit (i.e., a component of the claimed *power supply control unit*) that outputs a reset release signal to the microprocessor (i.e., the claimed *CPU*). Ex-1005, 9:44-50. The reset release signal is the claimed *restoration request signal* because in response to the signal the microprocessor restores the system to “a state immediately before the power-off standby mode was executed.” Ex-1005, 9:51-10:3.

As discussed in Section IX.A.2.j above, Jahagirdar discloses an input/output controller that manages both clock signals and power. Ex-1006, 5:27-42. Specifically, Jahagirdar discloses that, “[a]t a predetermined time ... a signal to

assert the clocks back on [i.e., the claimed *clock supply control signal*] is asserted.”

Ex-1006, 11:41-45.

As discussed in Section IX.A.1 above, adopting Jahagirdar’s teachings to integrate a clock control mechanism into Lee’s systems would have been obvious. Ex-1003 §§XII.A.1-2 & 3.m. Specifically, Lee’s reset signal generation circuit would send a signal to assert the clocks back on, as well as sending the reset release signal. Ex-1003 ¶204. A POSITA would understand that the reset signal generation circuit would output the signals when the supplied power supply voltage is stabilized because circuits can operate reliably only after a certain delay that permits the voltage level to rise and settle down. Ex-1003 ¶204.

n) [1n]

Jahagirdar discloses that the assertion of a clock supply control signal restarts the supply of clock signals. Ex-1006, 11:41-48.

As discussed in Section IX.A.1 above, it would have been obvious to implement the clock control in Lee’s systems according to Jahagirdar’s teaching. Ex-1003 §§XII.A.1-2 & 3.n.

o) [1o]

Lee discloses that the microprocessor (i.e., the claimed *CPU*), in response to the reset release signal (i.e., *upon receiving the restoration request signal*), recovers its working context (i.e., the claimed *information necessary in proceeding with the*

program and evacuated in the information holding unit in time of power shutdown) from the memory 60 (i.e., the claimed *information holding unit*). Ex-1005, 9:60-64, 9:51-55, 9:56-58. Accordingly, Lee discloses *restoring the information necessary in proceeding with the program and evacuated in the information holding unit in time of power shutdown* under the parties' agreed construction.

Consequently, "the microprocessor 10 and the hardware modules 30 and 40 are recovered to a state immediately before the power-off standby mode was executed." Ex-1005, 9:65-67. This enables the SOC to "operate in the state immediately before the power-off standby mode was executed," i.e., *branch a process to an address indicated by a program counter to continue program execution from a shutdown state*. Ex-1005, 9:67-10-3. Ex-1003 ¶210. A POSITA would understand that a program counter (PC) is a register within the microprocessor that determines which program instruction should be executed next. Ex-1003 ¶210. Lee discloses the saving of all microprocessor registers pre-power-off-standby mode and their restoration post-mode. Ex-1005, 6:21-26, 9:60-64.

Additionally, Jahagirdar teaches using microcode to execute a restore function. Ex-1006, 8:45-52; *see also id.*, 9:40-48, 10:18-38. Lee in view of Jahagirdar suggests the claimed *power supply restoration microprogram* under Petitioner's proposed construction. As discussed above, Lee discloses *restoring the information necessary in proceeding with the program and evacuated in the information holding unit in*

time of power shutdown, and then branching a process to an address indicated by a program counter to continue program execution from a shutdown state. Implementing Lee's restore function by adopting Jahagirdar's approach of using microcode would have been obvious, as discussed in Section IX.A.1 above. Ex-1003 §§XII.A.1-2, 3.o.

3. Claim 3

Lee in view of Jahagirdar renders claim 3 obvious. Ex-1003 §XII.A.4.

Jahagirdar discloses that its CPU cannot be shut down until both cores 320 and 322 are prepared for shutdown. Ex-1006, 9:56-61. This disclosure teaches the concept of *limiting a period in which shutdown is possible*. Ex-1003 ¶215.

As discussed in Section IX.A.1 above, it would have been obvious to combine Lee and Jahagirdar. Lee discloses the process of turning off power to the microprocessor along with at least two peripheral modules 30 and 40. Ex-1005, 5:52-60, 6:49-54, Fig. 1. A POSITA would recognize that the power supplied to the microprocessor should remain on if a peripheral module is actively engaged and requires input from the microprocessor. Ex-1003 ¶216. To prevent system malfunctions, a POSITA would utilize Lee's power controller (i.e., a component of the claimed *power supply control unit*) to regulate the timing of power shutdown to the microprocessor. Ex-1003 ¶216.

This implementation would reasonably be expected to succeed, as it was a routine process to design a component like Lee's power controller to discontinue power without precipitating system malfunctions. Ex-1003 ¶217.

4. Claim 5

Lee in view of Jahagirdar renders claim 5 obvious. Ex-1003 §XII.A.5.

As discussed in Section IX.A.2.k above, one of the *power supply restoration factors* is “when a user releases a power-off standby mode.” Ex-1005, 9:25-32. Lee discloses that when this happens, “*an interrupt signal* is generated from the outside,” i.e., *the power supply restoration factor uses an interrupt system of the microcontroller*. Ex-1005, 9:25-32 (emphasis added); *see also id.*, 6:14-20 (discussing an interrupt controller of the microcontroller).

5. Claim 8

Assuming claim 8 is not indefinite, Lee in view of Jahagirdar renders it obvious. Ex-1003 §XII.A.6.

In the Qualcomm Texas Case, Petitioner argued that claim 8 is indefinite. Ex-1048, 19. In response, Patent Owner asserted that claim 8 is not indefinite and that it requires that the microprogram is “‘selectively executed in an alternative way’ to permit changes in the information necessary to be evacuated or restored as required by claim 1.” Ex-1049, 16-17 (citing ’575 Patent, 5:39-50, 12:32-39). Under this

interpretation, Lee in view of Jahagirdar renders claim 8 obvious for two reasons, one based on Lee's disclosures and another based on Jahagirdar's disclosures.

First, Lee discloses that its SOC includes the microprocessor, the first peripheral module 30, and the second peripheral module 40, each maintaining its own working context. Ex-1005, Fig. 1, 5:61-67. In entering the power-off standby mode, Lee discloses turning off the power supply to all or only some of these modules. Ex-1005, 6:1-4, 10:20-25. When the power supply to only some of these modules is turned off, such as the microprocessor, a POSITA would implement microprograms to save and restore working contexts solely for the modules that are powered down, i.e., they would be *selectively executed in an alternative way*. Ex-1003 ¶¶224-27.

A POSITA would have recognized the benefits of disabling different modules *according to the generated power shutdown factor or a type of the selected power shutdown factor*. As discussed in Section IX.A.2.f above, Lee discloses two example power shutdown factors: "a predetermined time set by a user has passed or a user selects a power-off standby mode." Ex-1005, 6:10-20. For example, when a display timer expires, a POSITA would discern the advantage of shutting down the display driver while keeping the microprocessor operational to allow rapid restoration. Ex-1003 ¶226. Conversely, when a user opts for a system-wide power-off standby mode, a POSITA would understand the advantage of shutting down all modules. *Id.* There

would have been a reasonable expectation of success in implementing a selective execution of micrograms because such a process had been implemented routinely and successfully. *Id.*

Second, Jahagirdar discloses saving the “critical state” of the processor when transitioning into the zero voltage power management state. Ex-1006, 3:13-15. “The critical state of the processor includes state variables associated with the architectural, micro-architectural, debug state, *and/or* similar state variables associated with that processor.” Ex-1006, 3:14-17 (emphasis added). A POSITA would implement microprograms to save and restore all or only some of these state variables depending on the shutdown factor, i.e., they would be *selectively executed in an alternative way, according to the generated power shutdown factor or a type of the selected power shutdown factor*. Ex-1003 ¶¶228-30.

As discussed in Section IX.A.1 above, it would have been obvious to combine Lee and Jahagirdar. Based on Jahagirdar’s teaching, a POSITA would have incorporated a selective execution of microprograms in Lee’s systems. Dr. Annavaram explains that saving all states results in longer transitions into and out of the zero voltage state. Ex-1003 ¶229. In contrast, saving only select states expedites the transitions, which is advantageous for certain system requirements. *Id.* There would have been a reasonable expectation of success in implementing a selective

execution of micrograms because such a process had been implemented routinely and successfully. Ex-1003 ¶230.

6. Claim 11

Lee in view of Jahagirdar renders claim 11 obvious. Ex-1003 §XII.A.7.

Jahagirdar discloses that “voltage from the I/O control hub 225 ($V_{I/O}$ 349) may be provided to the processor 205 in order to provide **sufficient power** to the dedicated cache memory 340 such that it can store the critical state variables associated with the processor 205 while the rest of the processor 205 is powered down by the reduction of the operating voltage 240 down to a zero state.” Ex-1006, 5:43-49 (emphasis added). A POSITA would understand the application of “sufficient power” to cache memory 340 implies that a lower voltage is applied to the cache memory when the processor 205 is powered down, i.e., *lowering a voltage to be supplied to a circuit portion outside a power shutdown range to a lower limit voltage for information holding when the power shutdown factor occurs*. Ex-1006, 5:43-49; see also *id.*, 1:58-60 (discussing “a Deeper Sleep state in which all processor clocks are stopped and the processor voltage is reduced to a **lower data retention point**”) (emphasis added). Ex-1003 ¶233. Because the cache memory is not powered down, it is outside the *power shutdown range*, which the parties agree means “circuit for which power supply will be shutdown.”

As discussed in Section IX.A.1 above, it would have been obvious to combine Lee and Jahagirdar. Based on Jahagirdar's teaching, a POSITA would have incorporated a second power supply unit in Lee to deliver a lower limit voltage to the memory during the power-off standby mode. Ex-1003 ¶235. This approach negates the need to transfer working contexts to off-chip non-volatile memory, facilitating a faster transition to and recovery from the power-off standby state. Ex-1003 ¶234. In this adapted Lee system, the claimed *power shutdown range* includes the microprocessor and the peripheral circuits 30 and 40 because they are "circuit[s] for which power supply will be shutdown," as required by the parties' agreed construction in the Qualcomm Texas Case. Conversely, the memory 60 remains outside this *power shutdown range*.

There would have been a reasonable expectation of success because reducing voltage in power-saving modes had been performed routinely and successfully. Ex-1003 ¶235. Implementing these measures aligns with Lee's objective of minimizing power consumption while ensuring the rapid saving and restoring of working contexts. *Id.*

7. Claim 12

Lee in view of Jahagirdar renders claim 12 obvious. Ex-1003 §XII.A.8.

As discussed in Section IX.A.2.a above, Lee discloses a microprocessor 10. Ex-1005, 5:52-60; *see also id.* 5:35-41, Fig. 1. As Dr. Annavaram explains, a

POSITA would understand that the microprocessor would have circuits to implement a NOT operation and save the result in a register (i.e., *a circuit for loading an inverted value to a register*). Ex-1003 ¶¶238-41. Moreover, as discussed in Section IX.A.6 above, the claimed *power shutdown range* includes the microprocessor.

8. Claim 15

Lee in view of Jahagirdar renders claim 15 obvious. Ex-1003 §XII.A.9.

Lee discloses that “[t]he power supply 150 supplies a predetermined operating power to the SOC 110” and that the power supply 150 “may be implemented as an *on-chip regulator inside the SOC 110*.” Ex-1005, 5:48-51 (emphasis added). A POSITA would understand that “on-chip regulator,” which serves as the power supply 150 (i.e., the claimed *power supply unit*), corresponds to the claimed *voltage regulator*. Ex-1003 ¶243.

9. Claim 16

Lee in view of Jahagirdar renders claim 16 obvious. Ex-1003 §XII.A.10.

Jahagirdar discloses that its input/output controller sends a STOP_CPU signal to the clock generator to cause the clock generator to “halt the clock signal CLK to the CPU 205.” Ex-1006, 7:19-22; *see also id.*, 7:12-18. A POSITA would understand that the clock generator halts the clock signal by employing gating techniques, indicating that the clock generator remains powered. Ex-1003 ¶246.

As discussed in Section IX.A.1 above, utilizing Jahagirdar's teachings to implement a clock control mechanism in Lee's systems would have been obvious. Ex-1003 §§XII.A.1-2. Specifically, Lee's power controller would send a clock stop control signal to the clock generator, causing it to halt the clock signal without interrupting the power supply to the clock generator. Ex-1003 ¶247. Dr. Annavaram explains that gating the clock signal while maintaining power to the clock generator reduces the time required to resume from the standby state because the system does not need to wait for the clock generator to power on to produce a valid clock signal. *Id.*

There would have been a reasonable expectation of success because gating the clock signal while maintaining power to the clock generator had been implemented routinely and successfully. Ex-1003 ¶247.

B. Ground II: Lee, Jahagirdar, and Peterson Render Obvious Claim 2

Assuming claim 2 is not indefinite, Lee in view of Jahagirdar and Peterson renders it obvious. Ex-1003 §XII.B.

In the Qualcomm Texas Case, Petitioner argued that claim 2 is indefinite. Ex-1048, 18. In response, Patent Owner asserted that claim 2 is not indefinite and that "the invention of claim 2 allows the shutdown of the CPU as required by claim 1 with the capability of choosing whether or not to also shut down the clock." Ex-1049, 16. Under this interpretation, *upon receiving the clock stop control signal from the*

power supply control unit, the clock generator decides whether to cease the clock signal.

As discussed in Section VIII.E above, when Peterson's clock generator receives a shut-down entry request signal (i.e., the claimed *clock stop control signal*), it determines whether to stop the clock signal based on confirmation that a predetermined protocol requirement has been satisfied. Ex-1010, 3:40-60; *see also id.*, 7:59-8:16.

When implementing Lee's system in view of Jahagirdar, it would have been obvious to incorporate Peterson's teaching of halting the clock signal only after validating that the clock stop control signal adheres to a predetermined protocol requirement. Ex-1003 ¶253. Peterson teaches that "[t]his access protection scheme avoids the inadvertent placement of the clock generator into shut-down mode, and thus reduces the risk of accidental clock stoppage." Ex-1010, 8:13-16.

Lee, Jahagirdar, and Peterson are analogous art, all focusing on digital systems aimed at reducing power consumption. Ex-1005, 6:49-54; Ex-1006, 5:27-42, 10:46-54; Ex-1010, 1:60-63. They each disclose controlling clock generator to achieve this objective. Ex-1005, 1:30-34; Ex-1006, 7:19-22; Ex-1010, 3:11-15.

Integrating Peterson's teachings into the combined Lee and Jahagirdar system would have been a combination of prior art elements according to known methods to yield predictable results. Ex-1003 ¶255. Peterson's approach to disabling the

clock signal following protocol verification was a known and understood technique, one that a POSITA would have found obvious to apply to Lee's systems implemented in view of Jahagirdar. *Id.* A POSITA would have particularly recognized the advantage of minimizing accidental clock stoppage risk. Ex-1003 ¶254.

A POSITA would have had a reasonable expectation of success in incorporating Peterson's teaching. Ex-1003 ¶255. The method of disabling the clock signal subsequent to verifying the clock stop control signal was a well-established means to circumvent unintended clock stoppage that had been implemented successfully. *Id.*

C. Ground III: Lee, Jahagirdar, and Kang Render Obvious Claim 3

Lee in view of Jahagirdar and Kang renders claim 3 obvious. Ex-1003 §XII.C.

As discussed in Section VIII.F above, Kang teaches that wireless terminals, such as cellphones, must remain active during specific time slots to ensure message reception, i.e., *the power supply control unit limits a period in which shutdown is possible.*

When implementing Lee's system in view of Jahagirdar for a cellphone, it would have been obvious to incorporate Kang's teaching that the system should not be shut down during certain time slots, thereby preventing the cellphone from missing incoming messages. Ex-1011, 1:19-22; Ex-1003 ¶262.

Lee, Jahagirdar, and Kang are analogous art, each pertaining to digital systems that reduce power consumption by shutting off power. Ex-1005, 6:49-54; Ex-1006, 5:27-42, 10:46-54; Ex-1011, 1:12-14. Specifically, they all contemplate reducing power consumption within cellphones. Ex-1005, 6:16-20; Ex-1006, 3:51-56; Ex-1011, 1:16-19. Moreover, they detail saving working contexts before power shutdown, Ex-1005, 6:21-41; Ex-1006, 10:32-45; Ex-1011, 2:21-28, and restoring these contexts after power is resumed, so systems can quickly return to normal operation. Ex-1005, 9:61-10:3; Ex-1006, 11:41-48; Ex-1011, 2:28-34.

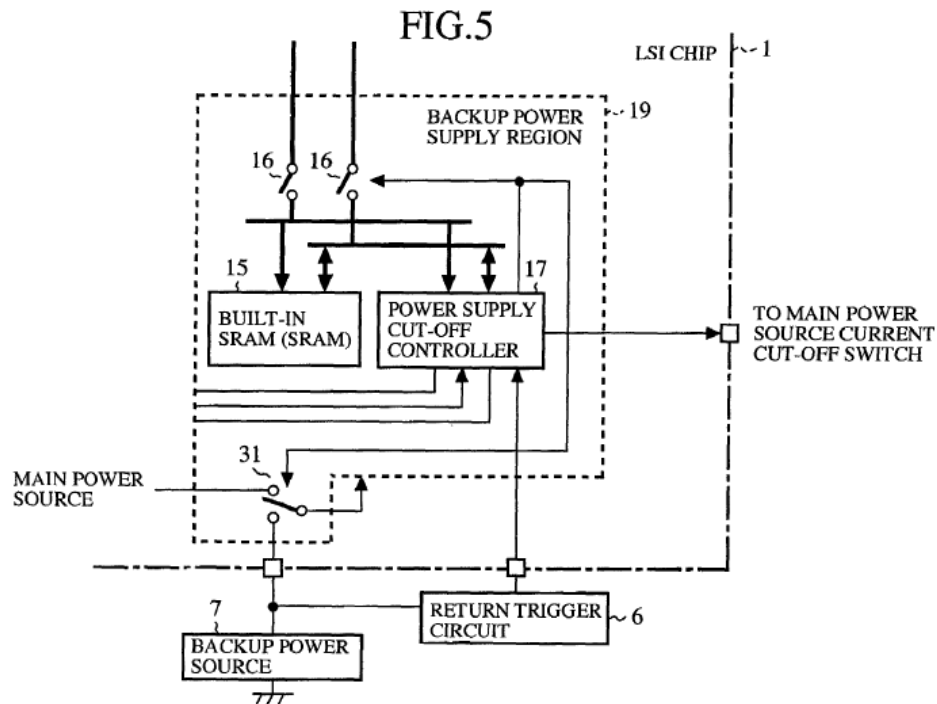
Incorporating Kang's teaching in the combined Lee and Jahagirdar system would have been a combination of prior art elements according to known methods to yield predictable results. Ex-1003 ¶263. Kang's strategy of ensuring a cellphone remains active during specific time slots was a known method that a POSITA would have found obvious to apply within Lee's systems implemented in view of Jahagirdar. *Id.* Specifically, a POSITA would understand that periodic monitoring of the paging channel is crucial for ensuring a cellphone receives incoming messages. *Id.*

A POSITA would have had a reasonable expectation of success in incorporating Kang's teaching. Ex-1003 ¶263. Periodic monitoring of the paging channel was widely acknowledged as an effective method for securing message reception on a cellphone. *Id.*

D. Ground IV: Lee, Jahagirdar, and Higashida Render Obvious Claim 11

Lee in view of Jahagirdar and Higashida renders claim 11 obvious. Ex-1003 §XII.D.

As discussed in Section VIII.G above, in the fifth embodiment, Higashida discloses the use of a backup power source that provides a voltage lower than that of the main power source to the backup power supply region containing an SRAM (i.e., the claimed *second power supply unit for lowering a voltage to be supplied to a circuit portion outside a power shutdown range*). Ex-1009, 12:61-65, 13:8-13. Figure 5 depicts a portion of the LSI chip 1 that highlights the key aspects of the fifth embodiment:



Ex-1009, Fig. 5. In Figure 5, the backup power source 7 supplies power to the

backup power supply region 19 when the LSI chip 1 is in the operation standby state.

Higashida discloses that the voltage of the backup power source 7 is “set lower than that of the main power source 3, enough for holding the content of the built-in SRAM provided in the backup power supply region 19” (i.e., the claimed *lower limit voltage for information holding*). Ex-1009, 13:8-13; *see also id.*, 13:30-45. The backup power source delivers this lower voltage during the “operation standby state” (i.e., *when the power shutdown factor occurs*). Ex-1009, 12:61-65.

When implementing Lee’s system in view of Jahagirdar, it would have been obvious to incorporate Higashida’s approach of supplying a lower voltage sufficient for retaining memory content during a standby state. Ex-1003 ¶267. As discussed in Section IX.A.6 above, a key advantage of this scheme is that it would obviate the need to transfer working context to off-chip non-volatile memory 130 in Lee, hence expediting the transition to the power-off standby state and facilitating faster recovery from that state. *Id.* Because the memory is not powered down in this adapted Lee system, it is outside the claimed *power shutdown range*, which the parties agree means “circuit for which power supply will be shutdown.”

Lee, Jahagirdar, and Higashida are analogous art, each addressing digital systems aimed at power consumption reduction through power shutdown. Ex-1005, 6:49-54; Ex-1006, 5:27-42, 10:46-54; Ex-1009, 6:7-11. They disclose methods to

save working contexts prior to power shutdown, Ex-1005, 6:21-41; Ex-1006, 10:32-45; Ex-1009, 7:30-36, and to restore these contexts post-power recovery, enabling swift resumption of normal system operations, Ex-1005, 9:61-10:3; Ex-1006, 11:41-48; Ex-1009, 7:65-8:6.

Incorporating Higashida's teaching in Lee's systems implemented in view of Jahagirdar would have been a combination of prior art elements according to known methods to yield predictable results. Ex-1003 ¶268. Higashida's teaching of a second power supply unit providing a lower voltage that is enough for holding the content of a memory during a standby state was a known technique that a POSITA would have found obvious to apply to Lee's systems implemented in view of Jahagirdar. *Id.* A POSITA would specifically appreciate the advantages of preserving information within memory while enhancing power efficiency. *Id.*

A POSITA would have had a reasonable expectation of success in incorporating Higashida's teaching, considering that it mirrored routine procedures for voltage reduction within power-saving modes had been implemented successfully. Ex-1003 ¶268.

E. Ground V: Shikata and Crump Render Obvious Claims 1, 5, 11, 12, and 15

1. The Combination of Shikata and Crump

Shikata also discloses the purportedly inventive features of the '575 Patent. Shikata discloses a processor that saves the CPU's working context when entering

standby mode and restoring it upon exiting that mode. The processor in Shikata also contains all the key components arranged as claimed by the '575 Patent. While describing its systems, Shikata omits implementation specifics that were routine at the time of the '575 Patent's alleged invention and, consequently, within the knowledge of a POSITA.

First, Shikata discloses that an application will be suspended, Ex-1007, Fig. 6, and the CPU will enter standby mode. *Id.*, 8:18-42. Shikata assumes that a POSITA would be familiar with mechanisms to notify the processor to undertake the steps to enter the standby state, such as saving register data. Crump addresses the saving and restoring of context upon entering a standby state, revealing that its microcontroller triggers a system management interrupt (SMI) signal to alert the CPU to save the CPU state when transitioning to the standby state. Ex-1008, 20:31-33, 21:53-22:6.

Second, Shikata describes the save and restore functionality of saving the working context to internal RAM upon entering standby mode, sending a completion signal upon saving the context, and restoring it when exiting standby mode. Ex-1007, 4:46-53, 5:4-11, 8:52-63. Moreover, Shikata teaches that boot instructions should be stored in internal RAM during standby entry to enable quick and efficient evacuation and recovery, yet again omitting the specifics of this functionality's implementation. Ex-1007, 5:50-57, 8:56-63. As Dr. Annavaram explains, a POSITA at the time of

the alleged invention of the '575 Patent would have understood that utilizing a microprogram rather than boot instructions for the save and restore functionality would further Shikata's objectives with minimal system modification. For example, Crump teaches the use of microcode for saving and restoring the CPU state to memory during standby mode. Ex-1008, 22:4-6; *see also id.*, Fig. 10A, 37:1-13. Dr. Annavaram also elaborates that a POSITA would recognize microcode as offering a superior solution, combining flexibility with low latency, compared to other hardware-based or program-based alternatives available at the time. Ex-1003 §VII.B.4.

In implementing Shikata's systems, a POSITA would likely have consulted analogous art, such as Crump. Both Shikata and Crump relate to digital systems designed to reduce power consumption by disabling power. Ex-1007, 1:17-20; Ex-1008, 2:9-13. Both disclose techniques for saving the CPU state before power shutdown, Ex-1007, 8:22-24; Ex-1008, 22:4-6, and restoring it upon power-up, thereby enabling a rapid resumption of operations, Ex-1007, 8:60-65; Ex-1008, 14:63-15:12.

Integrating Crump's SMI signal and microcode into Shikata's systems would have been a combination of prior art elements according to known methods to yield predictable results. Ex-1003 §§XII.E.1-2. As Dr. Annavaram explains, interrupt signals were fundamental components of digital systems, and the advantages of

microcode were well-recognized. Ex-1003 §§VII.B.4 & 8, ¶274. Consequently, applying Crump's SMI signal and microcode to Shikata's systems would have been an obvious step for a POSITA, yielding predictable results. Ex-1003 ¶274. Specifically, a POSITA would readily understand the significance of the SMI signal in instructing the CPU core unit to save register data. *Id.* Moreover, microcode provides a superior balance of flexibility and low latency compared to other methods available to a POSITA at the time of the alleged invention of the '575 Patent. *Id.* The flexibility offered by a microprogram is particularly advantageous giving Shikata's emphasis on minimizing hardware alterations while efficiently saving and restoring register values. Ex-1007, 2:40-45, 3:25-30; Ex-1003 ¶274.

Furthermore, it would also have been obvious to try microcode, as it was one of three approaches to saving and restoring context, alongside hardware-based or program-based solutions. Ex-1003 ¶274. A POSITA would have evaluated the advantages and disadvantages of each approach and recognized microcode as the clear choice for its optimal balance of flexibility and low latency. *Id.*

A POSITA would have had a reasonable expectation of success in integrating Crump's SMI signal and microcode in Shikata's systems. Ex-1003 ¶274. Interrupt signals were a well-established communication method successfully performed within digital systems like those described by Shikata. *Id.* Additionally, employing microcode was a conventional technique for implementing save-and-restore

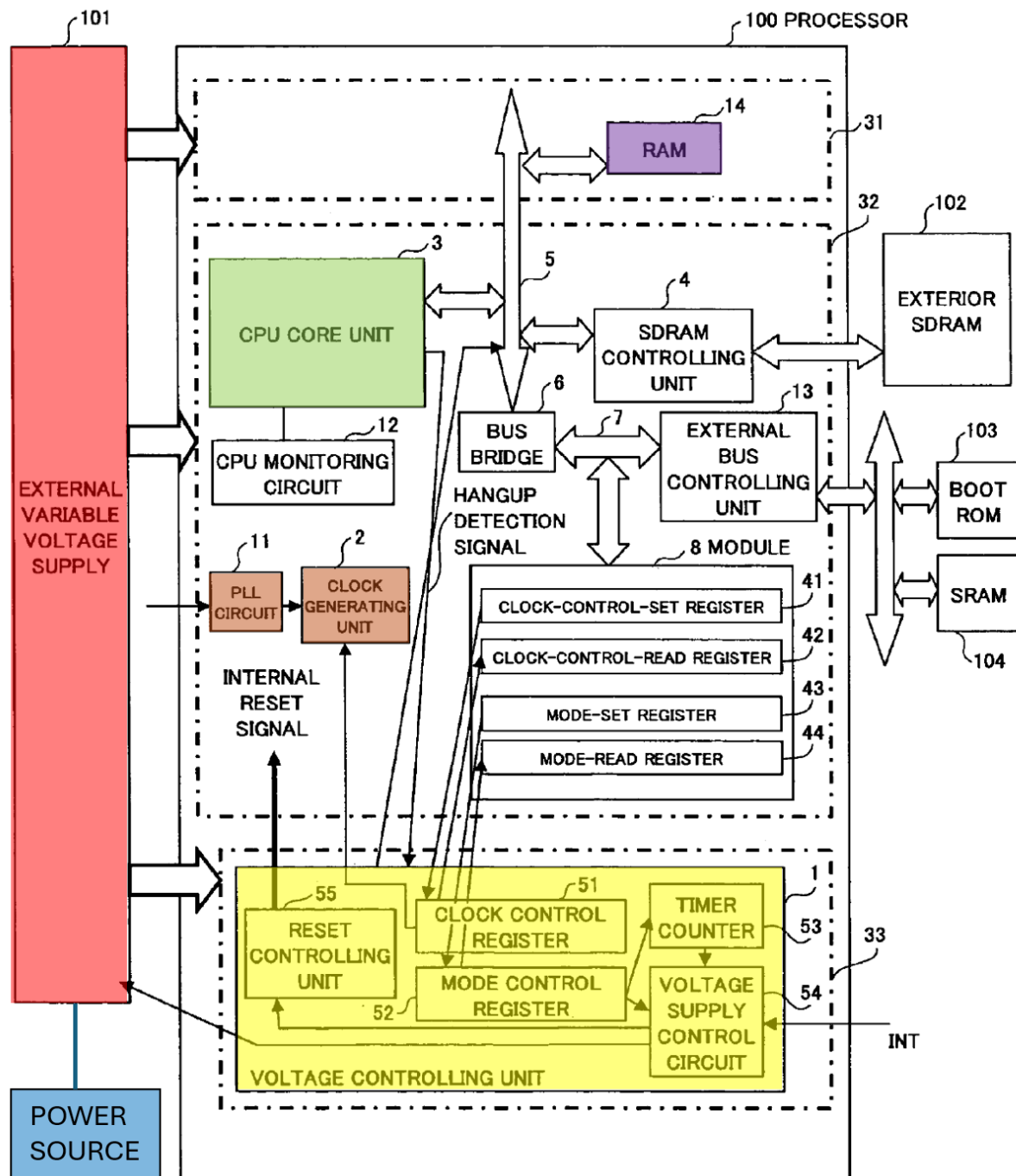
functions. *Id.* The choice between microcode, hardware, or program solutions depends on the requirements for flexibility and latency, and a POSITA would be familiar with the efficiency and adaptability afforded by microcode. *Id.*

2. Claim 1

Shikata in view of Crump renders claim 1 obvious.

[1pre]

Shikata discloses a semiconductor integrated circuit, specifically a processor. Ex-1007, 3:66-4:12, Figs. 1, 4, 5. Figure 5 depicts a processor 100. Ex-1007, 7:4-7.



Ex-1007, Fig. 5 (annotated with highlights and an additional block of power source, as further discussed below).

A POSITA would have known that the processor is implemented on a single chip. Ex-1003 ¶276. Consequently, Shikata’s processor is “a single integrated chip as opposed to a set of multiple chips (a ‘chipset’)” required by Petitioner’s proposed construction of *microcontroller*.

a) [1a]

Shikata discloses that its processor includes a CPU core unit (i.e., the claimed *CPU*) (green). Ex-1007, 3:66-4:12, Figs. 1, 4, 5.

b) [1b]

Shikata discloses an external variable voltage supply 101 (i.e., the claimed *power supply unit*) (red) that provides power to the processor. Ex-1007, 4:7-8, 4:29-30, Figs. 1, 4, 5; Ex-1003 §XII.E.3.b. This external variable voltage supply is connected to the CPU core unit within the processor. Ex-1007, 8:51-52. A POSITA would understand that the external variable voltage supply is also connected to a power source (blue) that delivers either AC or DC power, as a variable voltage supply needs such a source to power the processor. Ex-1003 ¶279. This power source corresponds to the claimed *power supply device*, which the parties agree means “power supply.” *Id.* Thus, a POSITA would understand that the external variable voltage supply is *arranged between CPU and a power supply device for supplying power to the CPU. Id.*

In implementing Shikata's systems, it would have been obvious for a POSITA to incorporate the external variable voltage supply within the processor because a POSITA would have appreciated the benefits of higher integration, such as an increase in performance, lower power consumption, and lower production costs. Ex-1003 ¶280. As Dr. Annavaram explains, integrating a greater number of circuit blocks on a single semiconductor die enhances performance. *Id.* Furthermore, this higher level of integration leads to reduced power consumption. *Id.* Additionally, it contributes to lower production costs. *Id.* There would have been a reasonable expectation of success in implementing this change, as integrating power supply circuitry within a single-die system had been implemented routinely and successfully. *Id.*

c) [1c]

Shikata discloses a voltage controlling unit 1 (i.e., the claimed *power supply control unit*) (yellow) that *controls* the external variable voltage supply (i.e., the claimed *power supply unit*) via a control signal. Ex-1007, 4:31-35, 8:34-42, 8:46-52. A POSITA would understand that the voltage controlling unit also *controls* the CPU core. For example, the voltage controlling unit contains a reset controlling unit for "initializing the individual modules of the CPU core unit 3." Ex-1007, 8:2-5, Fig. 5.

d) [1d]

Shikata discloses an internal RAM (i.e., the claimed *information holding unit*) (purple). Ex-1007, 3:66-4:12, Figs. 1, 4, 5. This internal RAM is for holding “register values necessary for the resumption of an operation” (i.e., *for holding information evacuated from the CPU, the information being necessary in proceeding with a program*). Ex-1007, 4:46-53; *see also id.*, 3:9-10 (“the CPU core unit includes an internal register”).

e) [1e]

Shikata discloses a PLL circuit and a clock generating unit working in tandem (brown) to generate clock signals. Ex-1007, 3:66-4:12, Figs. 1, 4, 5. Shikata explains that “[t]he PLL circuit 11 generates a frequency-multiplied clock signal ... and supplies the generated clock signal to the clock generating unit 2.” Ex-1007, 4:25-28. The clock generating unit then “generates operating clock signals for provision to individual modules including the CPU core unit 3 based on the frequency-multiplied clock signal supplied from the PLL circuit 11.” Ex-1007, 4:35-39. Thus, together, the PLL circuit and the clock generating unit form the claimed *clock generator*.

f) [1f]

Shikata discloses a procedure for transitioning to a standby state. Ex-1007, 8:18-42; Ex-1003 §XII.E.3.f. A POSITA would understand that the voltage controlling unit (i.e., the claimed *power supply control unit*) issues a signal (i.e., the

claimed *shutdown request signal*) to the CPU core unit to initiate its shutdown. Ex-1003 ¶285. Because the voltage controlling unit includes the reset controlling unit, which sends a signal to power on the CPU core unit when returning from standby, Ex-1007, 8:2-5, Fig. 5, a POSITA would understand that the voltage controlling unit would initiate the CPU core unit's shutdown as well. Ex-1003 ¶285.

It would also have been obvious for the voltage controlling unit to issue a signal to the CPU core unit to power it down in response to a power shutdown request (i.e., *in response to an occurrence of a power shutdown factor*). Ex-1003 ¶¶286-87. In fact, Crump discloses a microcontroller (i.e., the claimed *power supply control unit*) that sends a system management interrupt (SMI) signal (i.e., the claimed *shutdown request signal*) to a CPU upon the activation of a power switch (i.e., *in response to an occurrence of a power shutdown factor*). Ex-1008, 20:31-33, 21:53-22:3. Specifically, Crump discloses that its microcontroller asserts the SMI signal, interrupting the CPU prior to causing the power supply to cease delivering regulated power to the system. Ex-1008, 21:63-22:1.

As discussed in Section IX.E.1 above, it would have been obvious to implement Shikata's voltage controlling unit to output the SMI signal to the CPU core unit in response to a power shutdown request. Ex-1003 §§XII.E.1-2.

g) [1g]

Shikata discloses that “register values necessary for the resumption of an operation [i.e., the claimed *information necessary in proceeding with the program*] are saved to the internal RAM 14 [i.e., *evacuated to the information holding unit*] when a transition is to be made to shift into a standby state.” Ex-1007, 4:46-53; *see also id.*, 9:3-5; Ex-1003 §XII.E.3.g. Additionally, Shikata discloses that the CPU core sets a value in a control register of the voltage controlling unit to indicate that the “saved register data are stored in the internal RAM,” i.e., *the CPU outputs an evacuation completed signal to the power supply control unit after evacuation is completed.* Ex-1007, 5:4-11.

Crump discloses that its CPU, upon receiving the SMI signal (i.e., *upon receiving the shutdown request signal*), executes microcode to save the CPU state to memory (i.e., *evacuates the information necessary in proceeding with the program to the information holding unit*). Ex-1008, 22:4-6; *see also id.*, Fig. 10A, 37:1-13. A POSITA would understand that “microcode” and “microprogram” are synonymous, recognizing Crump’s microcode as the claimed *microprogram* under Petitioner’s proposed construction. Ex-1003 ¶292. Patent Owner admitted that microcode and microprogram are synonymous. Ex-1017, 28.

Additionally, Shikata in view of Crump suggests the claimed *power shutdown microprogram*, which is “a microprogram that evacuates the information necessary

in proceeding with the program to the information holding unit, and then outputs the evacuation completed signal to the power supply control unit” under Petitioner’s proposed construction. As discussed above, Shikata discloses *evacuating the information necessary in proceeding with the program to the information holding unit, and outputting an evacuation completed signal to the power supply control unit after evacuation is completed*. Implementing Shikata’s evacuation function, including notifying the voltage controlling unit 1 that the evacuation is complete, by adopting Crump’s approach of using microcode would have been obvious, as discussed in Section IX.E.1 above. Ex-1003 §§XII.E.1-2.

h) [1h]

Shikata discloses that the voltage controlling unit (i.e., the claimed *power supply control unit*) outputs a control signal (i.e., the claimed *power shutdown control signal*) to the external variable voltage supply (i.e., the claimed *power supply unit*) to suspend the operating voltage supply. Ex-1007, 4:29-35, 8:34-42. Shikata discloses that the voltage controlling unit outputs the control signal or instruction to the external variable voltage supply after the register data are saved. Ex-1007, 8:21-42. Consequently, a POSITA would understand that the voltage controlling unit issues the control signal after the CPU core sets a value in the voltage controlling unit’s control register, indicating that the “saved register data are stored in the

internal RAM,” i.e., *upon receiving the evacuation completed signal*. Ex-1007, 5:4-11; Ex-1003 ¶294.

i) [1i]

Shikata discloses that the external variable voltage supply (i.e., the claimed *power supply unit*) suspends the provision of operating voltage to the CPU core unit (i.e., *shuts down power supply to the CPU*) upon receipt of the control signal from the voltage controlling unit (i.e., *upon receiving the power shutdown control signal from the power supply control unit*). Ex-1007, 4:29-35, 8:34-42; *see also id.*, 6:51-54.

j) [1j]

Shikata discloses that the voltage controlling unit (i.e., the claimed *power supply control unit*) issues an instruction to the clock generating unit to suspend the clock signal (i.e., *outputs a clock stop control signal to the clock generator*). Ex-1007, 8:34-36. This instruction is transmitted after the register data are saved. Ex-1007, 8:21-36. Accordingly, a POSITA would understand that the voltage controlling unit sends this instruction once the CPU core sets a value in the voltage controlling unit’s control register, indicating that the “saved register data are stored in the internal RAM,” i.e., *upon receiving the evacuation completed signal*. Ex-1007, 5:4-11; Ex-1003 ¶297.

k) [1k]

Shikata discloses that the voltage controlling unit (i.e., the claimed *power supply control unit*) issues a control command (i.e., *outputs a power supply control signal*) to the external variable voltage supply (i.e., the claimed *power supply unit*) when “an external interruption or a Wake-up interruption such as a timer interruptions or the like has occurred” (i.e., *in response to an occurrence of a power supply restoration factor*). Ex-1007, 8:46-52; *see also id.*, 7:63-8:5.

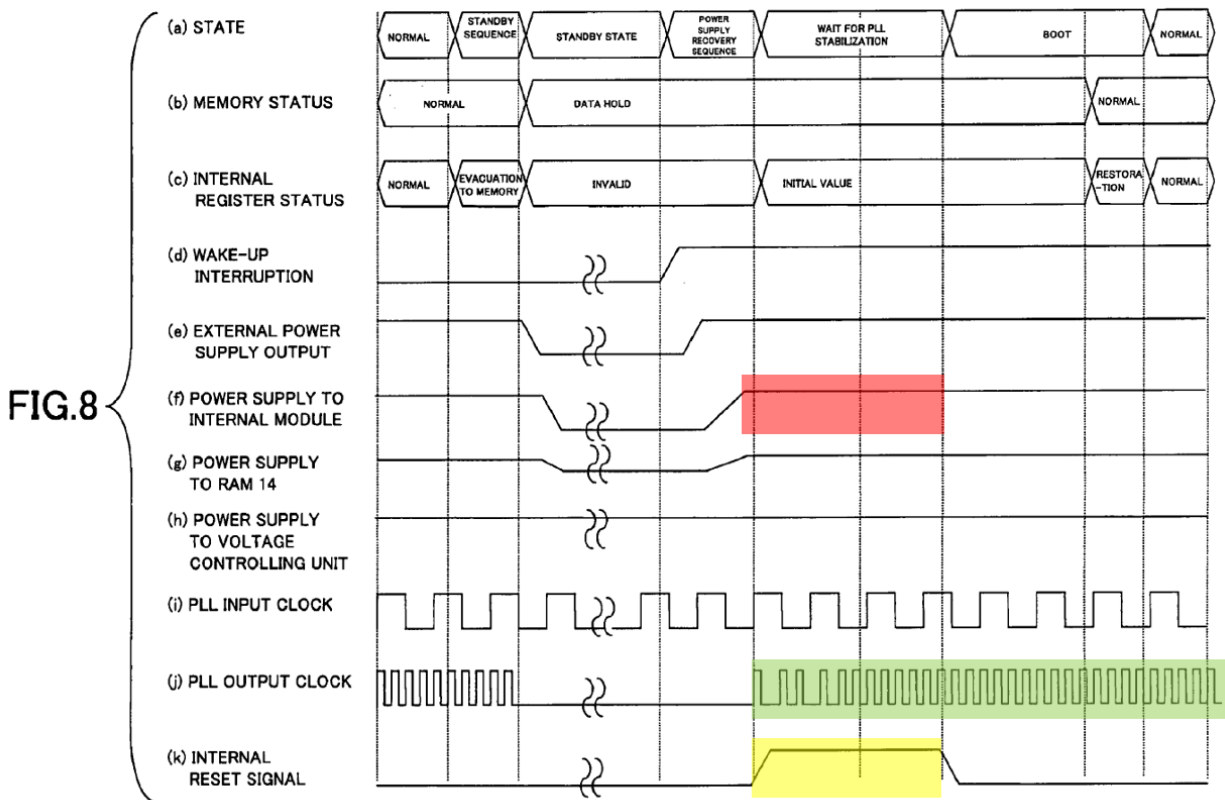
l) [1l]

Shikata discloses that the external variable voltage supply (i.e., the claimed *power supply unit*), in response to the control command (i.e., *upon receiving the power supply control signal*), resumes voltage supply to the CPU core unit (i.e., *starts to supply power to the CPU*). Ex-1007, 8:48-52.

m) [1m]

Shikata discloses that the voltage controlling unit (i.e., the claimed *power supply control unit*) includes a reset controlling unit responsible for initializing the individual modules of the CPU core unit by asserting an internal reset signal. Ex-1007, 7:65-8:5, 8:52-56, Fig. 5; Ex-1003 §XII.E.3.m. The segment of the internal reset signal that reaches the CPU core unit is the claimed *restoration request signal* because it prompts the CPU core unit to conduct a boot operation and recover register values before resuming application program execution. Ex-1007, 8:56-65.

Moreover, the segment of the internal reset signal directed towards the PLL circuit corresponds to the claimed *a clock supply control signal to the clock generator* because it prompts the PLL circuit (i.e., a component of the claimed *clock generator*) to restart the clock signal. Ex-1007, 8:52-56, Fig. 5. Figure 8 is an annotated timing diagram that demonstrates how the assertion of the internal reset signal (k—yellow) causes restarting of the clock signal by the PLL circuit (j—green). Ex-1007, 9:17-19.



Ex-1007, Fig. 8 (annotated).

Additionally, Shikata's annotated timing diagram illustrates that the internal reset signal is initiated (k—yellow) after the power supply is restored to internal

modules such as the CPU core unit (i.e., *when a supplied power supply voltage is stabilized*) (f—red). Ex-1007, 9:15-19; *see also id.*, 5:39-40 (describing CPU core unit as an internal module).

n) [1n]

As discussed above in Section IX.E.2.m, the PLL circuit (i.e., a component of the claimed *clock generator*), in response to the internal reset signal (i.e., *upon receiving the clock supply control signal*), restarts the clock signal (i.e., *restarts to supply an operation clock*). Ex-1007, 8:52-56, 9:17-19, Figs. 5, 8; Ex-1003 ¶305.

o) [1o]

Shikata discloses that the CPU core unit, upon receiving the segment of the internal reset signal directed towards it (i.e., *upon receiving the restoration request signal*), recovers the register values previously saved in the internal RAM. Ex-1007, 8:52-63; *see also id.*, 4:66-5:3; Ex-1003 §XII.E.3.o. Accordingly, Shikata discloses *restoring the information necessary in proceeding with the program and evacuated in the information holding unit in time of power shutdown* under the parties' agreed construction.

Subsequently, the CPU core unit resumes the application program “in a continuing fashion based on the recovered register data” (i.e., *branches a process to an address indicated by a program counter to continue program execution from a shutdown state*). Ex-1007, 8:63-65; Ex-1003 ¶308.

As discussed in Section IX.E.1 above, Crump discloses that its CPU executes microcode to save its state to memory. Ex-1008, 22:4-6; *see also id.*, Fig. 10A, 37:1-13. A POSITA would understand that Crump employs a similar microcode mechanism to restore the CPU's state from memory. Ex-1003 ¶309.

Moreover, Shikata in view of Crump suggests the claimed *power supply restoration microprogram* under Petitioner's proposed construction. As discussed above, Shikata discloses *restoring the information necessary in proceeding with the program and evacuated in the information holding unit in time of power shutdown, and then branching a process to an address indicated by a program counter to continue program execution from a shutdown state*. Implementing Shikata's restore function by adopting Crump's approach of using microcode would have been obvious, as discussed in Section IX.E.1 above. Ex-1003 §§XII.E.1-2.

3. Claim 5

Shikata in view of Crump renders claim 5 obvious.

As discussed in Section IX.E.2.k above, Shikata discloses that the restoration of power supply is triggered by “an interruption signal INT from an exterior” or “a periodic interruption signal supplied from the timer counter” (i.e., *the power supply restoration factor uses an interrupt system of the microcontroller*). Ex-1007, 7:63-8:2.

4. Claim 11

Shikata in view of Crump renders claim 11 obvious. Ex-1003 §XII.E.5.

Shikata discloses the division of its processor into distinct power supply blocks labeled 31, 32, and 33. Ex-1007, 7:4-10, Fig. 5; *see also id.*, 6:42-44, Fig. 4. Specifically, the internal RAM is positioned within the power supply block 31; the voltage controlling unit is positioned within the power supply block 33; and the remaining components of the processor, including the CPU core unit, are positioned within the power supply block 32. Ex-1007, 6:44-48.

In a standby state, power supply is suspended for the power supply block 32 (i.e., the claimed *power shutdown range*, which the parties agree means “circuit for which power supply will be shutdown”). Ex-1007, 7:10-12. However, power supply is maintained for the remaining two power supply blocks, including the power supply block 31. Ex-1007, 7:12-17; *see also id.*, 6:51-56. Instead of suspension, Shikata discloses that the voltage for the power supply block 31—which houses the internal RAM with saved register values—undergoes reduction in a standby state (i.e., *lowering a voltage to be supplied to a circuit portion outside a power shutdown range to a lower limit voltage for information holding when the power shutdown factor occurs*). Ex-1007, 7:12-17, 7:47-49.

Furthermore, Shikata discloses that “[t]he power supply blocks 31 through 33 receive respective, separate power supplies from the external variable voltage

supply.” Ex-1007, 6:48-51. Therefore, a POSITA would understand that the external variable voltage supply consists of three distinct units, each delivering a separate power supply to its corresponding power supply block. Ex-1003 ¶¶314-15. The unit supplying power to the power supply block 31 corresponds to the claimed *second power supply unit*.

5. Claim 12

Shikata in view of Crump renders claim 12 obvious.

As discussed in Section IX.E.2.a above, Shikata discloses a CPU core unit (i.e., the claimed *CPU*). Ex-1007, 3:66-4:12, Figs. 1, 4, 5. As Dr. Annavaram explains, a POSITA would understand that the CPU core unit would have circuits to implement a NOT operation and save the result in a register (i.e., *a circuit for loading an inverted value to a register*). Ex-1003 ¶318. Furthermore, the CPU core unit is located within the power supply block 32, which as discussed in Section IX.E.4 above, is the claimed *power shutdown range*.

6. Claim 15

Shikata in view of Crump renders claim 15 obvious. Ex-1003 §XII.E.7.

Shikata discloses that its external variable voltage supply 101 (i.e., the claimed *power supply unit*) regulates voltage supply (i.e., *includes a voltage regulator*). Ex-1003 ¶321. Specifically, Shikata discloses that this external variable voltage supply delivers an operating voltage to the processor. Ex-1007, 4:29-30. The

external variable voltage supply can “suspend the supply of the operating voltage or lower the operating voltage.” Ex-1007, 4:30-35; *see also id.*, 8:34-42, 9:4-6, Fig. 8. Additionally, it can raise the operating voltage. Ex-1007, 8:11-15; *see also id.*, 8:48-52, 9:15-17, Fig. 8.

To the extent Shikata does not disclose that its external variable voltage supply does not include a voltage regulator (it does), it would have been obvious in view of Crump. Crump discloses a power supply unit that includes a primary/regulation unit (i.e., the claimed *voltage regulator*). Ex-1008, 15:43-45, 15:53-61. Figure 5 of Crump “is a block diagram showing the relevant portions of the power supply.” Ex.-1008, 5:46-47.

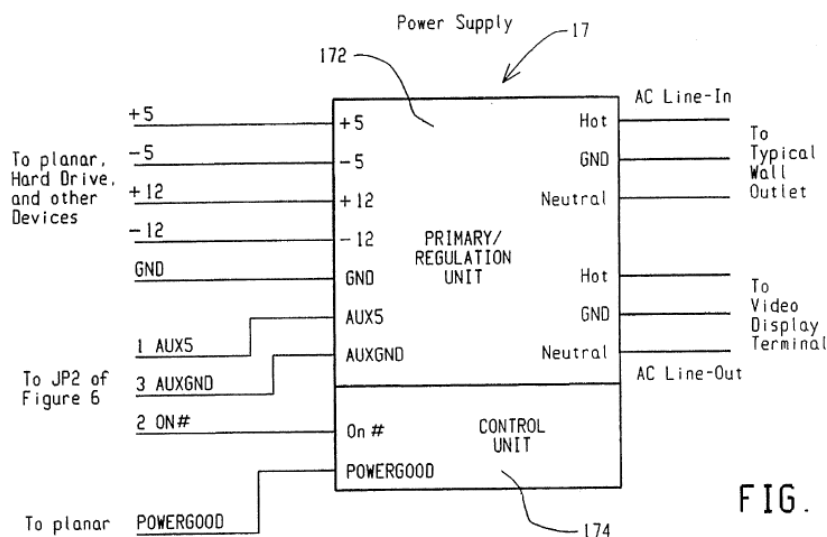


FIG. 5

Ex-1008, Fig. 5. As depicted in Figure. 5, “[t]he power supply 17 has two units: a control unit 174 and a primary/regulation unit 172.” Ex-1008, 15:43-45, 15:53-61.

A POSITA would have known that a voltage regulator is necessary for Shikata's external variable voltage supply to control the supply of the operating voltage as discussed above. Ex-1003 ¶323. There would have been a reasonable expectation of success because implementing a voltage regulator was a routine process that had been performed successfully. *Id.*

F. Ground VI: Shikata, Crump, and Peterson Render Obvious Claim 2

Assuming claim 2 is not indefinite, Shikata in view of Crump and Peterson renders it obvious. Ex-1003 §XII.F.

As discussed in Section VIII.E above, when Peterson's clock generator receives a shut-down entry request signal (i.e., the claimed *clock stop control signal*), it determines whether to stop the clock signal based on confirmation that a predetermined protocol requirement has been satisfied. Ex-1010, 3:40-60; *see also id.*, 7:59-8:16.

When implementing Shikata's system in view of Crump, it would have been obvious to incorporate Peterson's teaching of halting the clock signal only after validating that the clock stop control signal adheres to a predetermined protocol requirement. Ex-1003 ¶327. Peterson teaches that "[t]his access protection scheme avoids the inadvertent placement of the clock generator into shut-down mode, and thus reduces the risk of accidental clock stoppage." Ex-1010, 8:13-16.

Shikata, Crump, and Peterson are analogous art, all focusing on digital systems aimed at reducing power consumption. Ex-1007, 1:17-20; Ex-1008, 2:9-13; Ex-1010, 1:60-63. They each disclose controlling clock generator to achieve this objective. Ex-1007, 8:34-40; Ex-1008, 10:31-33, 26:22-23, 58:10, 58:35-39; Ex-1010, 3:11-15.

Integrating Peterson's teachings into Shikata's systems implemented in view of Crump would have been a combination of prior art elements according to known methods to yield predictable results. Ex-1003 ¶328. Peterson's approach to disabling the clock signal following protocol verification was an understood technique, one that a POSITA would have found obvious to apply to Shikata's systems implemented in view of Crump. *Id.* A POSITA would have particularly recognized the advantage of minimizing accidental clock stoppage risk. *Id.*

A POSITA would have had a reasonable expectation of success in incorporating Peterson's teaching. Ex-1003 ¶329. The method of disabling the clock signal subsequent to verifying the clock stop control signal was a well-established means to circumvent unintended stopping of clocks that had been performed successfully. *Id.*

G. Ground VII: Shikata, Crump, and Kang Render Obvious Claim 3

Shikata in view of Crump and Kang renders claim 3 obvious. Ex-1003 §XII.G.

As discussed in Section VIII.F above, Kang teaches that wireless terminals, such as cellphones, must remain active during specific time slots to ensure message reception, i.e., *the power supply control unit limits a period in which shutdown is possible.*

When implementing Shikata's system in view of Crump for a cellphone, it would have been obvious to incorporate Kang's teaching that the system should not be shut down during certain time slots, thereby preventing the cellphone from missing incoming messages. Ex-1011, 1:19-22. Ex-1003 ¶333.

Shikata, Crump, and Kang are analogous art, each pertaining to digital systems that reduce power consumption by shutting off power. Ex-1007, 1:17-20; Ex-1008, 2:9-13; Ex-1011, 1:12-14. Moreover, they describe saving CPU states before power shutdown, Ex-1007, 8:22-24; Ex-1008, 22:4-6; Ex-1011, 2:21-28, and restoring these states after power is resumed, so systems can quickly return to normal operation. Ex-1007, 8:60-63; Ex-1008, 22:7-10; Ex-1011, 2:28-34.

Incorporating Kang's teaching in Shikata's systems implemented in view of Crump would have been a combination of prior art elements according to known methods to yield predictable results. Ex-1003 ¶333. Kang's strategy of ensuring a cellphone remains active during specific time slots was a known method that a POSITA would have found obvious to apply within Shikata's systems implemented in view of Crump. *Id.* Specifically, a POSITA would understand that periodic

monitoring of the paging channel is crucial for ensuring a cellphone receives incoming messages. *Id.*

A POSITA would have had a reasonable expectation of success in incorporating Kang’s teaching. Ex-1003 ¶334. Periodic monitoring of the paging channel was widely acknowledged as an effective method for securing message reception on a cellphone. *Id.*

H. Ground VIII: Shikata, Crump, and Chung Render Obvious Claim 16

Shikata in view of Crump and Chung renders claim 16 obvious. Ex-1003 §XII.H.

As discussed in Section VIII.H above, Chung teaches a power-down sequence, where the power supplies to the CPUs are disabled, while maintaining the power supply to the clock generator. Instead of cutting off power to the clock generator, Chung discloses “tristat[ing]” clock signals to the CPU—essentially blocking clock signals from reaching the CPUs. Ex-1003 ¶338.

In implementing Shikata’s system in view of Crump, it would have been obvious to integrate Chung’s teachings by configuring the external variable voltage supply (i.e., the claimed *power supply unit*) to sustain power to the clock generator even when receiving control signals from the voltage controlling unit (i.e., *the power supply unit does not shut down the power supply at least to the clock generator upon receiving the power shutdown control signal from the power supply control unit*).

Ex-1003 ¶¶337-41. Dr. Annavaram explains that a POSITA would understand that using a tristate gate to inhibit the supply of clock signals to the CPU, instead of disabling the power supply to the clock generator, is more advantageous for circuits frequently transitioning in and out of standby mode because clock signals can resume swiftly. Ex-1003 ¶340. Conversely, disabling and then restoring power to a clock generator takes considerable time for it to produce stable clock signals again. Ex-1007, 9:15-18, Fig. 8; Ex-1003 ¶340.

Shikata, Crump, and Chung are analogous art, each concerned with digital systems that aim to reduce power consumption by shutting off power. Ex-1007, 1:17-20; Ex-1008, 2:9-13; Ex-1012, 32:14-19. Additionally, they describe saving CPU states prior to power shutdown. Ex-1007, 8:22-24; Ex-1008, 22:4-6; Ex-1012, 31:63-66. These states are subsequently restored after power is resumed, allowing systems to swiftly return to normal operation. Ex-1007, 8:60-63; Ex-1008, 22:7-10; Ex-1012, 35:10-18.

Integrating Chung's teaching into Shikata's systems implemented in view of Crump would have been a combination of prior art elements according to known methods to yield predictable results. Ex-1003 ¶341. Chung's teaching of tristating clock signals, as opposed to disabling power to the clock generator, was a known method that a POSITA would have found obvious to apply within Shikata's systems implemented in view of Crump. *Id.*

A POSITA would have had a reasonable expectation of success in implementing Chung's teaching, as tristating clock signals was recognized as a routine and standard procedure that had been implemented successfully. Ex-1003 ¶341.

X. Conclusion

Petitioner respectfully requests institution of *inter partes* review and cancellation of the Challenged Claims of the '575 Patent.

Date: May 20, 2025

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APPENDIX A: THE CHALLENGED CLAIMS OF THE '575 PATENT

Claim	Limitation #	Limitation
1	[1pre]	A microcontroller comprising:
	[1a]	a CPU;
	[1b]	a power supply unit arranged between the CPU and a power supply device for supplying power to the CPU;
	[1c]	a power supply control unit for controlling the CPU and the power supply unit;
	[1d]	an information holding unit for holding information evacuated from the CPU, the information being necessary in proceeding with a program; and
	[1e]	a clock generator; wherein:
	[1f]	the power supply control unit outputs a shutdown request signal to the CPU in response to an occurrence of a power shutdown factor,
	[1g]	the CPU, upon receiving the shutdown request signal, executes a power shutdown microprogram, evacuates the information necessary in proceeding with the program to the information holding unit, and outputs an evacuation completed signal to the power supply control unit after evacuation is completed,
	[1h]	the power supply control unit, upon receiving the evacuation completed signal, outputs a power shutdown control signal to the power supply unit,
	[1i]	the power supply unit shuts down power supply to the CPU upon receiving the power shutdown control signal from the power supply control unit,
	[1j]	the power supply control unit, upon receiving the evacuation completed signal, outputs a clock stop control signal to the clock generator,
	[1k]	the power supply control unit outputs a power supply control signal to the power supply unit in response to an occurrence of a power supply restoration factor,
	[1l]	the power supply unit, upon receiving the power supply control signal, starts to supply power to the CPU,

	[1m]	the power supply control unit outputs a restoration request signal to the CPU and outputs a clock supply control signal to the clock generator when a supplied power supply voltage is stabilized,
	[1n]	the clock generator, upon receiving the clock supply control signal, restarts to supply an operation clock, and
	[1o]	the CPU, upon receiving the restoration request signal, executes a power supply restoration microprogram, restores the information necessary in proceeding with the program and evacuated in the information holding unit in time of power shutdown, and then branches a process to an address indicated by a program counter to continue program execution from a shutdown state.
2	[2]	The microcontroller according to claim 1, wherein the clock generator selects one of operation performed after stopping supply of an operation clock and operation stop performed without stopping the supply of the operation clock as operation to be performed upon receiving the clock stop control signal from the power supply control unit.
3	[3]	The microcontroller according to claim 1, wherein the power supply control unit limits a period in which shutdown is possible.
5	[5]	The microcontroller according to claim 1, wherein the power supply restoration factor uses an interrupt system of the microcontroller.
8	[8]	The microcontroller according to claim 1, wherein one of the power shutdown microprogram and the power supply restoration microprogram is selectively executed in an alternative way, according to the generated power shutdown factor or a type of the selected power shutdown factor.
11	[11]	The microcontroller according to claim 1, further comprising a second power supply unit for lowering a voltage to be supplied to a circuit portion outside a power shutdown range to a lower limit voltage for information holding when the power shutdown factor occurs.
12	[12]	The microcontroller according to claim 1, further comprising a circuit for loading an inverted value to a register in a circuit portion in a power shutdown range.

15	[15]	The microcontroller of claim 1, wherein the power supply unit includes a voltage regulator.
16	[16]	The microcontroller of claim 1, wherein the power supply unit does not shut down the power supply at least to the clock generator upon receiving the power shutdown control signal from the power supply control unit.

CERTIFICATION OF WORD COUNT

Pursuant to 37 C.F.R. § 42.24(d), I certify that the foregoing complies with the type-volume limitation of 37 C.F.R. § 42.24 and contains 13,950 words based on the word count indicated by the word-processing system used to prepare the paper, and excluding those portions exempted by § 42.24(a).

Date: May 20, 2025

/Scott C. Weidenfeller/
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Registration No. 54,531

CERTIFICATE OF SERVICE

Pursuant to 37 C.F.R. § 42.105, I hereby certify that on May 20, 2025, I caused a true and correct copy of the foregoing Petition for *Inter Partes* Review of 7,930,757, supporting exhibits, and Power of Attorney to be served via Priority Mail Express on the Patent Owner at the following correspondence address of record as listed on the USPTO Patent Center:

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