

**IN THE UNITED STATES DISTRICT COURT
FOR THE WESTERN DISTRICT OF TEXAS
WACO DIVISION**

COLLABO INNOVATIONS, INC., a
Delaware Corporation

Plaintiff

v.

QUALCOMM INCORPORATED and
QUALCOMM TECHNOLOGIES, INC.,
both Delaware Corporations

Defendants

CIVIL ACTION NO. 6:24-cv-00472-ADA

PRELIMINARY INVALIDITY CONTENTIONS

Pursuant to the Court’s Standard Order Governing Proceedings 4.1—Patent Cases (“OGP”) and the Court’s scheduling order (D.I. 29), Defendants Qualcomm Incorporated and Qualcomm Technologies, Inc. (“Defendants” or “Qualcomm”) provide their Preliminary Invalidity Contentions concerning U.S. Patent No. 7,930,575 (“the ’575 patent”). These contentions set forth Defendants’ Preliminary Invalidity Contentions with respect to the claims that were identified by Plaintiff Collabo Innovations, Inc. (“Plaintiff” or “Collabo”) in its Preliminary Infringement Contentions (“PICs”), dated December 6, 2024.

Defendants also serve herewith the document production accompanying these disclosures pursuant to the OGP and the Court’s scheduling order (D.I. 29).

I. INTRODUCTORY STATEMENT

The claims asserted by Plaintiff against Defendants in this case are claims 1-3, 5, 8, 11, 12, 15, and 16 of the ’575 Patent. *See* PICs at 2. These claims are collectively referred to as “the Asserted Claims” of the ’575 Patent. The Asserted Claims of the ’575 Patent, however, are either not novel, or obvious, in view of the state of the prior art and the understanding of a person of

2. Anticipation

Qualcomm identifies the following prior art now known to it to anticipate at least one of the Asserted Claims of the '575 patent, either expressly or inherently as understood by a person having ordinary skill in the art. Each of these prior art patents, publications, systems, and services anticipates the Asserted Claims. In some instances, Qualcomm treated certain prior art as anticipatory where certain elements are inherently present based on Collabo's apparent claim construction in Collabo's infringement contentions. By disclosing a patent or patent application as prior art, Qualcomm incorporates by reference each and every related patent and patent application.

The following patents and publications are prior art under at least 35 U.S.C. §§ 102(a), (b), (e), and/or (g):

1. Qualcomm MSM7500
2. Jahagirdar
3. Chung
4. Crump
5. Shikata
6. Kang
7. Intel XScale PXA250 and XScale PXA210
8. Intel StrongARM SA-1110

(collectively, Anticipatory References)

Claim charts containing examples of where elements of the Asserted Claims of the '575 patent are found in the foregoing prior art patents, patent applications, and prior art systems are provided in the attached charts.

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Each exemplary printed publication describing or relating to a prior art system should be understood to discuss the system’s capabilities generally and also to discuss specific implementation examples of specific installations of the particular system. For example, the PXA250 Developer’s Manual discloses the structure, function, and operation of the Intel XScale PXA250 product which, upon information and belief, was on sale and in public use prior to the filing of the patent; thus, the sale, offer for sale, and use of the Intel XScale PXA250 product is itself invalidating prior art. On information and belief, and as evidenced by the corroborating references, at least the Intel StrongARM SA-1110 and Intel XScale PXA250 devices and systems were in use or on sale before the earliest possible priority date of the ’575 patent, and operate in a manner that practices the Asserted Claims. On information and belief, and as evidenced by the corroborating references, at least the Qualcomm MSM7500 devices and systems were made, offered for sale, or on sale before the earliest possible priority date of the ’575 patent, and operates in a manner that practices the Asserted Claims. To the extent the exemplary references describe various implementations of the same underlying system, that underlying system is a single reference under 35 U.S.C. §§ 102(a), 102(b), and/or 102(g). The exemplary references are evidence of the capabilities of the prior art system, and each chart provided for a prior art system should be understood to incorporate by reference all printed publications describing or relating to that prior art system and all charts provided for those printed publications. In addition, each of the references itself also qualifies as prior art on separate grounds as a publication under sections 102(a) and/or 102(b). On information and belief, the capabilities of the prior art systems are not limited to the evidence provided in the exemplary references. Even if the exemplary references are not treated as a single prior art

reference, at the very least it would have been obvious to combine the features described in those references inasmuch as the individual references discuss the same system.

The cited portions of prior art references are exemplary and representative of the content of the prior art references, and should be understood in the context of the reference as a whole, as understood by one of ordinary skill in the art. The patents and patent publications listed above are representative and incorporate each and every related patent application, patent publication, and issued patent. To the extent any cited prior art reference is deemed not to anticipate a claim as noted in the attached charts for failing to teach or suggest one or more limitations of that claim, the claim would nonetheless have been inherent and/or obvious to one of ordinary skill in the art at the time of the alleged invention(s), either alone or by the combination of the cited prior art references with any of the other listed references. Charts listing examples of certain combinations, with examples of specific citations to portions of the references are attached hereto.

3. Obviousness and Motivations to Combine

As shown in the prior art matrix above, each cited prior art reference may be combined with one or more other prior art references to render obvious the Asserted Claims in combination, as explained in more detail below. The disclosures of these references may also be combined with information known to persons skilled in the art at the time of the alleged inventions, and understood and supplemented in view of the common sense and knowledge of persons skilled in the art at the time of the alleged inventions, including any statements in the intrinsic records of the '575 Patent and related applications.

A person of ordinary skill would have been motivated to combine the prior art cited in the Exhibits based on the nature of the problem to be solved, the teachings of the prior art, and the knowledge of persons of ordinary skill in the art. The identified prior art references, including

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portions cited in attached Exhibits 1 through 23, address the same or similar technical issues and suggest the same or similar solutions to those issues as the Asserted Claims. On such bases, on a limitation-by-limitation basis, Defendants expressly intend to combine one or more prior art items identified in the Exhibits with each other to address any further contention from Plaintiff that a particular prior art item supposedly lacks one or more limitations of an Asserted Claim. In other words, Defendants contend that each charted prior art item can be combined with other charted prior art items when a particular prior art item lacks or does not explicitly disclose a limitation or feature of an Asserted Claim. The suggested obviousness combinations described below are not to be construed to suggest that any reference included in the combinations is not anticipatory. Further, if Plaintiff contends that any of the anticipatory prior art fails to disclose one or more limitations of the Asserted Claims, Defendants reserve the right to identify other prior art references that, when combined with the anticipatory prior art, would render the claims obvious despite an allegedly missing limitation. Defendants will further specify the motivations to combine the prior art, including through reliance on expert testimony, at the appropriate later stage of this lawsuit.

A person of skill in the art would have been motivated to combine the identified prior art items. As the United States Supreme Court held in *KSR Int’l Co. v. Teleflex, Inc.*, 550 U.S. 398, 416 (2007): “The combination of familiar elements according to known methods is likely to be obvious when it does no more than yield predictable results.” The Supreme Court further held that, “[w]hen a work is available in one field of endeavor, design incentives and other market forces can prompt variations of it, either in the same field or a different one. If a person of ordinary skill can implement a predictable variation, § 103 likely bars its patentability. For the same reason, if a technique has been used to improve one device, and a person of ordinary skill in the art would

proceeding with a program was well-known. For example, Crump discloses that a “Resume Routine restores the state of the computer system 10 back to its configuration before the system 10 was suspended.” 33:7-12. As another example, Chung discloses that programs “for restoring the content of the registers after power up are well known in the art,” and that when “activity indications are detected, the system controller initiates a power resume operation.” Chung, 3:37-47, 32:20-26. *See also, e.g.*, Jahagirdar at [0053]-[0056]; Arai, 1:10-28; 3:1-5; Higashida, 8:16-36; Fleischmann, 2:29-3:2; Shikata, 4:54-61; Lee, 9:44-10:3, 10:28-57, Fig. 7, Hill, Abstract, 6:48-56, Fig. 5; Kang, Abstract, 7:29-45, 8:64-9:15, Table I, Fig. 5B.

Qualcomm identifies the following additional prior art references that provide context and background for the concepts and alleged benefits in addition to any prior art disclosed in Sections V.A and V.B below.

b) Specific Motivation to Combine: Claim 1

In addition to the Anticipatory References listed above (i.e., Jahagirdar, Chung, Crump, Kang, Intel XScale PXA250, Intel StrongARM SA-1110, Qualcomm MSM 7500), a person of ordinary skill in the art would have been motivated to make the following combinations of prior art:

1. Lee combined with one of Chung, Jahagirdar or Shikata
2. Hill combined with one of Chung, Jahagirdar or Shikata
3. Shikata with one of Lee, Hill, Chung, Jahagirdar, or Crump
4. Crump with one of Chung, Jahagirdar, or Kang
5. Kang with one of Lee, Hill, Shikata, Jahagirdar, Chung or Crump
6. Intel XScale PXA250 and XScale PXA210 with one of Lee, Hill, Chung, Jahagirdar, or Crump
7. Intel StrongARM SA-1110 with one of Lee, Hill, Chung, Jahagirdar, or Crump
8. Qualcomm MSM7500 with one of Lee, Hill, Chung, Jahagirdar, or Crump

placing the output in tristate) to reduce power consumption and to avoid the latching problem as disclosed by Chung or by Baum. *See* Chung, 8:4-9, Baum, 9:43-45, Fig. 6. **Higashida** states that its “invention relates to a method for reducing leakage current of an LSI, which is designed to suppress an increase in power consumption caused by leakage current in an operation standby stage.” Higashida, 1:10-13. Higashida discloses that when the CPU is placed in a shutdown state, the clock stopping circuit is instructed to stop the clock supply. Higashida, 6:65-67 (“the power supply cut-off controller 17 instructs the clock stopping circuit 24 to stop clock supply, and the scanning control circuit 23 to start a scanning operation.”). *See also* Higashida, 8:7-11. Power management circuits disclosed in Combinations for Claim 1 would operate with a programmable clock generation register, similar to the one disclosed by Chung or by Baum. *See, e.g.*, Chung, Fig. 2E, Baum, Fig. 6, Higashida, Fig. 1 and Fig. 2. Thus, the modified clock generator would receive a clock stop control signal from the power management circuit to stop generation of the clock before power to the CPU is shutdown. Doing so would disable the generation of the CPU clock “so as to prevent unnecessary power from being drawn . . . and to prevent latching of the CPU circuits which would prevent the processor from quickly resuming operation” as taught by Chung. *See* Chung, 8:4-9. Such an implementation would be within the skill of a person of ordinary skill and the person will have a reasonable expectation of success because the modification would be a predictable result by combining known elements in a known manner.

C. Claim Charts

Subject to Defendants’ reservation of rights, claim charts providing a limitation-by-limitation analysis of where specifically, in each prior art item, each limitation of the Asserted Claims of the ’575 Patent, including for each limitation that Defendants contend is governed by 35 U.S.C. § 112 ¶ 6, the identity of the structure(s), act(s), or material(s) in each item of prior art that performs the claimed function, are attached in Exhibits 1 through 23.

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Exhibit	Prior Art Reference
Exhibit 1	Lee (U.S. Patent No. 7,293,183)
Exhibit 2	Hill (U.S. Patent No. 7,174,472)
Exhibit 3	Shikata (U.S. Patent No. 7,218,248)
Exhibit 4	Kang (U.S. Patent No. 7,369,815)
Exhibit 5	Jahagirdar (U.S. Patent Appl. No. 2007/0157036)
Exhibit 6	Chung (U.S. Patent No. 5,390,350)
Exhibit 7	Crump (U.S. Patent No. 5,530,879)
Exhibit 8	Ozawa (U.S. Patent Appl. No. 2004/0257898; U.S. Patent No. 7,380,149)
Exhibit 9	Wisor (U.S. Patent No. 5,504,910)
Exhibit 10	Higashida (U.S. Patent No. 7,167,991)
Exhibit 11	Ooishi (U.S. Patent No. 6,999,342)
Exhibit 12	Product: Qualcomm MSM7500
Exhibit 13	Product: Transmeta Crusoe
Exhibit 14	Product: Intel XScale PXA250 and XScale PXA210
Exhibit 15	Product: Intel StrongARM SA-1110
Exhibit 16	Arai (U.S. Patent No. 5,978,922)
Exhibit 17	Fleischmann (U.S. Patent No. 6,968,469)
Exhibit 18	Negi (JP S61-1821123)
Exhibit 19	Ikeda (JP H06-123150)
Exhibit 20	Sano (JP H02-178818)
Exhibit 21	Iwata (U.S. Patent No. 5,872,903)
Exhibit 22	Baum (WO 2001/035200)
Exhibit 23	ACPI, (“Advanced Configuration and Power Interface Specification,”

	Revision 2.0, Compaq Computer Corporation et al. and Revision 3.0a, Hewlett-Packard Corporation et al)
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D. Invalidity Under 35 U.S.C. §§ 102(a), 102(b), 102(g)

Subject to Defendants’ reservation of rights, Defendants identify the following products and systems that, on information and belief, are prior art to the Asserted Patent under 35 U.S.C. §§ 102(a), 102(b) and/or § 102(g). The “Product” column identifies the products/systems. The “Company/Individual” identifies the entity that (a) sold the product/system, (b) offered the product/system for sale, (c) publicly used the product/system, (d) was involved in manufacturing the product/system, or (e) has information regarding the product/system’s development or manufacturing before the priority date of the corresponding Asserted Patent. The “Date of first sale/offer for sale/public use/made” identifies the date when the product/system was first: known or used by others (102(a)); sold, offered for sale, or in public use (102(b)); or made (102(g)) in the United States to the best of Defendants’ current knowledge.

At least as early as October 2000, Transmeta Corporation sold or offered for sale its Crusoe series of microprocessors. *See* QCOLLABO_0004540-QCOLLABO_0004542. The Crusoe series of processors supported five power states: Normal, Auto Halt, Quick Start, Deep Sleep, and Off. During Auto Halt, Quick Start, and Deep Sleep modes, power to the microprocessor core is halted, while context is preserved. *See* QCOLLABO_0004447-QCOLLABO_0004532 at QCOLLABO_0004467; QCOLLABO_0004533-QCOLLABO_0004539 at QCOLLABO_0004538-39.

At least as early as December 2005, Actel Corporation sold or offered for sale its Fusion family of mixed-signal flash FPGA PSCs with Optional Soft ARM Support (“Fusion”). *See* QCOLLABO_0006319-QCOLLABO_0006322. Fusion is a single chip containing power

Exhibit 12
Claims 1, 2, 3, 5, 8, 11, 12, 15, and 16 U.S. Patent No. 7,930,575
Are Anticipated and/or Rendered Obvious by
Qualcomm MSM7500 (“MSM7500”)

At the present time, subject to its express reservation of rights of supplement or amend these contentions as may be appropriate in view of further discovery, further investigation, and/or the Court’s claim construction ruling, Qualcomm identifies below specifically where each element of the asserted claim is disclosed or taught by the prior art. The contentions provided in this chart represent at least one way in which the prior art anticipates and/or renders obvious the asserted claims of the ’575 patent. Nothing in these contentions should be interpreted as a concession regarding the breadth of the asserted claims.

Claim 1	Exemplary Disclosures
[1pre] A microcontroller comprising:	MSM7500 discloses and/or renders obvious this limitation. MSM7500, Fig. 5-1:  MSM7500, Fig. 5-2:

Exhibit 13
Claims 1, 2, 3, 5, 8, 11, 12, 15, and 16 U.S. Patent No. 7,930,575
Are Anticipated and/or Rendered Obvious by
Transmeta Crusoe Processor Model TM5400/TM5600 (“Transmeta”)

At the present time, subject to its express reservation of rights of supplement or amend these contentions as may be appropriate in view of further discovery, further investigation, and/or the Court’s claim construction ruling, Qualcomm identifies below specifically where each element of the asserted claim is disclosed or taught by the prior art. The contentions provided in this chart represent at least one way in which the prior art anticipates and/or renders obvious the asserted claims of the ’575 patent. Nothing in these contentions should be interpreted as a concession regarding the breadth of the asserted claims.

Transmeta Crusoe Processor Model TM5400/TM5600. The Transmeta Crusoe TM5400/TM5600 Data Book, Transmeta Crusoe Processor Model TM5400 Product Brief and/or Transmeta Crusoe Processor Model TM5400/TM5600 system is prior art under at least 35 U.S.C. §§ 102(a) and 102(b):

- https://web.archive.org/web/20000818000541/http://www.transmeta.com/crusoe/download/pdf/TM5400_ProductBrief_5-23-00.pdf (“Transmeta Product Brief”)
- https://web.archive.org/web/20031214014530/http://transmeta.com/crusoe_docs/tm5400n5600_databook_001101.pdf (“Transmeta Data Book”)
- <https://abcnews.go.com/Technology/CuttingEdge/story?id=119347&page=1>
- U.S. Patent No. 6,968,469

Claim 1	Exemplary Disclosures
[1pre] A microcontroller comprising:	Transmeta discloses and/or renders obvious this limitation. Transmeta Product Brief, 1: “The Transmeta Crusoe Processor is an ultra-low power, high-speed microprocessor based on an advanced VLIW core architecture.” Transmeta Product Brief, 2: “The Crusoe Processor incorporates integer and floating point execution units, separate instruction and data caches, a level-2 write-back cache, memory management unit, and multimedia instructions. In addition to these traditional processor features, the device integrates a DDR SDRAM memory controller, SDR SDRAM memory controller, PCI bus controller and serial ROM interface controller.”

Exhibit 14
Claims 1, 2, 3, 5, 8, 11, 12, 15, and 16 U.S. Patent No. 7,930,575
Are Anticipated and/or Rendered Obvious by
Intel XScale PXA250 and PXA210 Processors and/or Publications (listed below) describing the Processors (“PXA250”)

At the present time, subject to its express reservation of rights of supplement or amend these contentions as may be appropriate in view of further discovery, further investigation, and/or the Court’s claim construction ruling, Qualcomm identifies below specifically where each element of the asserted claim is disclosed or taught by the prior art. The contentions provided in this chart represent at least one way in which the prior art anticipates and/or renders obvious the asserted claims of the ’575 patent. Nothing in these contentions should be interpreted as a concession regarding the breadth of the asserted claims.

Intel PXA250 Processor (“PXA250”). The Intel PXA250 and PXA210 Application Processors Developer’s Manual and/or Intel PXA250 system is prior art under at least 35 U.S.C. §§ 102(a) and 102(b):

- <https://web.archive.org/web/20020214182843/http://developer.intel.com/design/pca/applicationsprocessors/index.htm>
- <https://web.archive.org/web/20020215223335/http://developer.intel.com/design/pca/applicationsprocessors/manuals/index.htm>
- <https://web.archive.org/web/20020214181907/http://developer.intel.com:80/pressroom/archive/releases/20020212net.htm>
- https://www.eetimes.com/document.asp?doc_id=1200054
- <https://www.intel.cn/content/dam/doc/report/history-2002-annual-report.pdf>
- <https://web.archive.org/web/20020314041910/http://lwn.net/2002/0228/a/mv-pxa250.php3>
- <https://web.archive.org/web/20020222235105/http://developer.intel.com/design/pca/applicationsprocessors/manuals/278525-001.htm>
- <https://web.archive.org/web/20030612021658/http://developer.intel.com/design/pca/applicationsprocessors/manuals/278522-001.pdf>

Claim 1	Exemplary Disclosures
[1pre] A microcontroller comprising:	PXA250 discloses and/or renders obvious this limitation. PXA250, 1-1: “This document applies to both the Intel® PXA250 and the PXA210 application processors. They are Application Specific Standard Products (ASSP) that provide industry-leading MIPS/mW performance for Handheld Computing Applications. Each application processor is a highly integrated system on a chip and includes a high-performance low-power Intel® XScale™ Core with a variety of different system peripherals.”

Exhibit 15
Claims 1, 2, 3, 5, 8, 11, 12, 15, and 16 U.S. Patent No. 7,930,575
Are Anticipated and/or Rendered Obvious by
Intel StrongArm SA-1110 Microprocessor Developer's Manual and/or Intel StrongARM SA-1110 ("SA-1110")

At the present time, subject to its express reservation of rights of supplement or amend these contentions as may be appropriate in view of further discovery, further investigation, and/or the Court's claim construction ruling, Qualcomm identifies below specifically where each element of the asserted claim is disclosed or taught by the prior art. The contentions provided in this chart represent at least one way in which the prior art anticipates and/or renders obvious the asserted claims of the '575 patent. Nothing in these contentions should be interpreted as a concession regarding the breadth of the asserted claims.

Intel StrongArm SA-1110 Microprocessor ("SA-1110"). The Intel StrongArm SA-1110 Microprocessor Developer's Manual and/or Intel StrongArm SA-1110 system is prior art under at least 35 U.S.C. §§ 102(a) and 102(b):

- <https://web.archive.org/web/20020204060141/http://www.intel.com:80/design/strong/manuals/278240.htm>;
- https://web.archive.org/web/20010204001900/http://www.intel.com:80/design/strong/1110_brf.htm;
- "Energy Efficient Operating Systems and Software," Sinha, Massachusetts Institute of Technology, August 2001;
- Intel StrongArm SA-1110 Microprocessor, Specification Update, Intel Corp., Jan. 2000.

Claim 1	Exemplary Disclosures
[1pre] A microcontroller comprising:	SA-1110 discloses and/or renders obvious this limitation. SA-1110, 21: "The Intel® StrongARM* SA-1110 Microprocessor (SA-1110) is a highly integrated communications microcontroller that incorporates a 32-bit StrongARM RISC processor core, system support logic, multiple communication channels, an LCD controller, a memory and PCMCIA controller, and general-purpose I/O ports. As do the Intel StrongARM SA-110 Microprocessor (SA-110) and Intel StrongARM SA-1100 Microprocessor (SA-1100), earlier members of the StrongARM family, the SA-1110 provides power efficiency, low cost, and high performance. Figure 1-1 shows the features of the SA-1110. The shaded boxes are features that have carried over with few or no changes from the SA-110. The nonshaded boxes are new or updated features for the SA-1110; most of the features are equivalent to that of the SA-1100. The SA-1110 differs from the SA-1100 only in the features of its memory and PCMCIA controller."