

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

QUALCOMM INCORPORATED,

Petitioner,

v.

COLLABO INNOVATIONS, INC.,

Patent Owner.

Case IPR2025-01015

U.S. Patent 7,930,575

PATENT OWNER'S PRELIMINARY RESPONSE

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Rules

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I. INTRODUCTION

Pursuant to 35 U.S.C. § 313 and 37 C.F.R. § 42.107, Patent Owner Collabo Innovations, Inc. (“Patent Owner”) submits this Preliminary Response to the Petition for *Inter Partes* Review (“Petition,” Paper 1) filed by Qualcomm Incorporated (“Petitioner”) challenging claims 1-3, 5, 8, 11, 12, 15, and 16 of U.S. Patent No. 7,930,575 (the “’575 patent”) (Ex. 1001). The Board should not institute *inter partes* review because Petitioner has not met its burden of showing a reasonable likelihood of prevailing on any of its proposed grounds of unpatentability, each based on obviousness under 35 U.S.C. § 103(a) (pre-AIA).

The Petition suffers from many fundamental flaws, each of which warrants denial of institution. For example, to prevail under Grounds I-IV, Petitioner must show that U.S. Patent No. 7,293,183 (“Lee”) in combination with U.S. Patent No. 7,664,970 (“Jahagirdar”) discloses or suggests each element of independent claim 1. But as explained in detail below, Lee in combination with Jahagirdar fails to disclose or suggest multiple elements of the claim. Similarly, under Grounds V-VIII, Petitioner must show that U.S. Patent No. 7,219,248 (“Shikata”) in combination with U.S. Patent No. 5,530,879 (“Crump”) discloses or suggests each element of independent claim 1, which Petitioner also fails to do.

To justify the institution of an *inter partes* review, a petitioner must establish that there is a “reasonable likelihood that the petitioner would prevail with respect

to at least 1 of the claims challenged in the petition.” 35 U.S.C. § 314(a). For at least the reasons discussed in this preliminary response, Petitioner has not shown a reasonable likelihood of prevailing on any of the challenged claims.

II. THE ’575 PATENT AND THE CHALLENGED CLAIMS

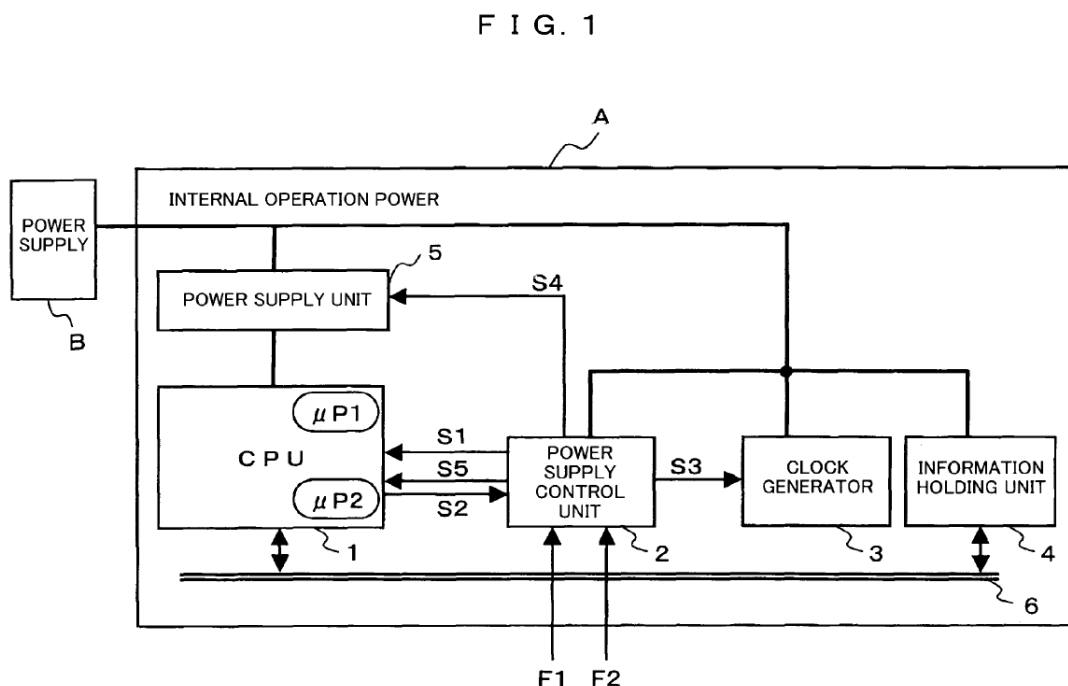
The inventions disclosed and claimed in the ’575 patent relate generally “to microcontrollers, and in particular, to a technique of suppressing current consumption in time of stand-by in a power shutdown mode in which a program can proceed.” Ex. 1001 at 1:13-16. In conventional microcontrollers that have a “stop mode,” high speed restoration is possible but tends to have large current consumption caused by leakage current. *Id.* at 1:19-29. Another prior approach—shutting down power supplied to the microcontroller—enabled substantially zero current consumption caused by leakage current, but “the time required for restoration becomes longer.” *Id.* at 1:30-39. A known “standby control circuit” workaround, although achieving power reduction and high-speed restoration, had other drawbacks such as timing hazards and extra hardware requirements, i.e., increased circuit scale. *Id.* at 1:40-2:22.

An improved microcontroller design that efficiently balanced power saving and system responsiveness was needed. To address such problems, the ’575 patent provides “a microcontroller capable of easily and rapidly evacuating and restoring information necessary in proceeding with a program when realizing a standby state

in which internal operation voltage supply is shutdown, a state in which an internal operation voltage is lowered, or the like.” *Id.* at 2:26-2:31.

The invention of the '575 patent achieves low standby current while preserving program state by cutting power to the CPU yet keeping an information-holding unit awake. *See id.* at 2:58-3:6. It makes the transition fast and reliable by executing a dedicated microprogram that evacuates and restores just the necessary state, avoiding interrupt races without having to prohibit interrupts and reusing existing on-chip wiring. *See id.* at 3:7-23, 6:57-7:3. The net result is a compact, hardware-light microcontroller that delivers materially lower standby power with quick resume.

Figure 1 of the '575 patent is a block diagram of one embodiment of the microcontroller architecture that enables the controlled power shutdown process:



Id. at 7:22-24, FIG. 1. Figure 2 is the flowchart for the power shutdown process, and Figure. 4 is the flowchart for the power supply restoration process for that embodiment:

FIG. 2

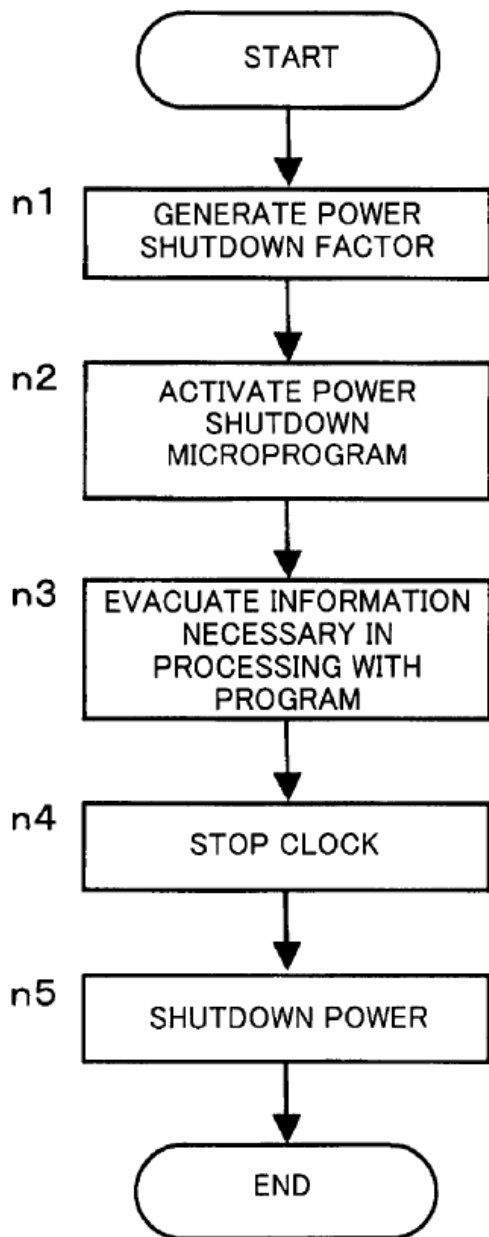
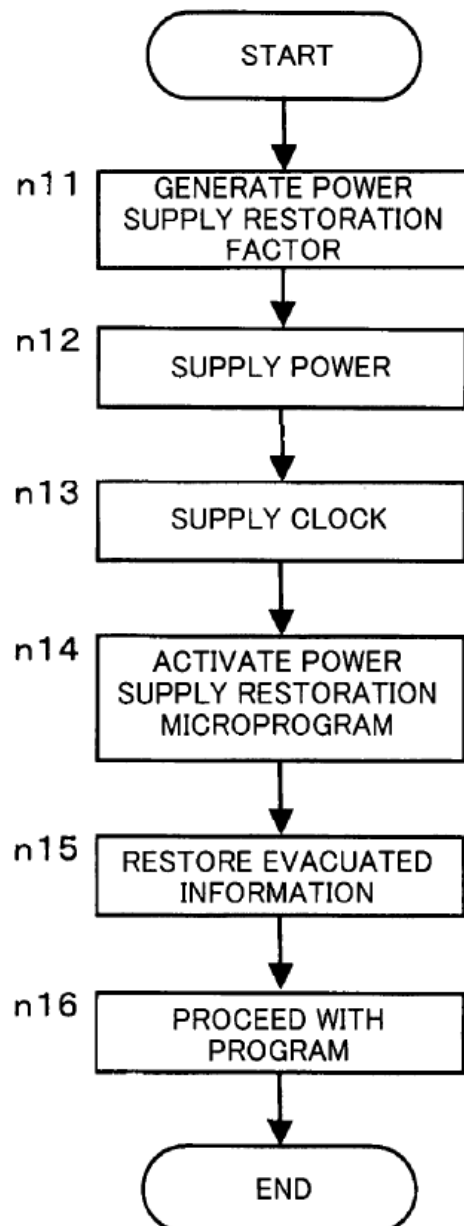


FIG. 4



Id. at 7:25-27, 7:31-33, FIG. 2, FIG. 4.

Consistent with the foregoing, the '575 patent contains independent claim 1 as follows:

Claim 1	Limitations
1[pre]	A microcontroller comprising:
1[a]	a CPU;
1[b]	a power supply unit arranged between the CPU and a power supply device for supplying power to the CPU;
1[c]	a power supply control unit for controlling the CPU and the power supply unit;
1[d]	an information holding unit for holding information evacuated from the CPU, the information being necessary in proceeding with a program; and
1[e]	a clock generator; wherein:
1[f]	the power supply control unit outputs a shutdown request signal to the CPU in response to an occurrence of a power shutdown factor,
1[g]	the CPU, upon receiving the shutdown request signal, executes a power shutdown microprogram, evacuates the information necessary in proceeding with the program to the information holding unit, and outputs an evacuation completed signal to the power supply control unit after evacuation is completed,
1[h]	the power supply control unit, upon receiving the evacuation completed signal, outputs a power shutdown control signal to the power supply unit,
1[i]	the power supply unit shuts down power supply to the CPU upon receiving the power shutdown control signal from the power supply control unit,

1[j]	the power supply control unit, upon receiving the evacuation completed signal, outputs a clock stop control signal to the clock generator,
1[k]	the power supply control unit outputs a power supply control signal to the power supply unit in response to an occurrence of a power supply restoration factor,
1[l]	the power supply unit, upon receiving the power supply control signal, starts to supply power to the CPU,
1[m]	the power supply control unit outputs a restoration request signal to the CPU and outputs a clock supply control signal to the clock generator when a supplied power supply voltage is stabilized,
1[n]	the clock generator, upon receiving the clock supply control signal, restarts to supply an operation clock, and
1[o]	the CPU, upon receiving the restoration request signal, executes a power supply restoration microprogram, restores the information necessary in proceeding with the program and evacuated in the information holding unit in time of power shutdown, and then branches a process to an address indicated by a program counter to continue program execution from a shutdown state.

Id. at 18:46-19:24.

III. LEVEL OF ORDINARY SKILL

For the limited purpose of this Preliminary Response, Patent Owner does not contest Petitioner's definition of a person of ordinary skill in the art, but it reserves the right to do so if trial is instituted.

IV. CLAIM CONSTRUCTION

Similarly, for the limited purpose of this Preliminary Response, Patent Owner does not contend that any claim terms need construction, and can be given their plain

and ordinary meaning, but it reserves the right to do so if trial is instituted. *See Real Time Data, LLC v. Iancu*, 912 F.3d 1368, 1375 (Fed. Cir. 2019) (“The Board is required to construe ‘only those terms . . . that are in controversy, and only to the extent necessary to resolve the controversy.’” (quoting *Vivid Techs., Inc. v. Am. Sci. & Eng’g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999))).

V. APPLICABLE LEGAL STANDARDS

The Board may only grant a petition for *inter partes* review where “the information presented in the petition ... shows that there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition.” 35 U.S.C. § 314(a); 37 C.F.R. § 42.108(c). Petitioner bears the burden of showing that this statutory threshold has been met. *See* Office Patent Trial Practice Guide, 77 Fed. Reg. 48,756 (Aug. 14, 2012) (“The Board ... may institute a trial where the petitioner establishes that the standards for instituting the requested trial are met”).

At a minimum, the reasonable-likelihood-of-prevailing standard “effectively requires the petitioner to present a *prima facie* case justifying a rejection of the claims in a patent.” 112 Cong. Rec. S1375 (daily ed. Mar. 8, 2011) (quoting Sen. Kyl). As explained by the Federal Circuit, “the expedited nature of IPRs bring[s] with it an obligation for petitioners to make their case in their petition to institute.” *Intelligent Bio-Sys., Inc. v. Illumina Cambridge Ltd.*, 821 F.3d 1359, 1369 (Fed. Cir.

2016). Moreover, the Board may not overlook flaws in the petition or reformulate its challenges to enhance their suitability. *See SAS Inst. Inc. v. Iancu*, 138 S. Ct. 1348, 1355 (2018) (“[I]t’s the petitioner, not the Director, who gets to define the contours of the proceeding.”); *see also id.* (“[T]he petitioner is master of its complaint . . .”); *see also id.* at 1353 (forbidding the Board from “curat[ing]” the petition).

A. Obviousness

Section 103 of the Patent Act provides that “[a] patent may not be obtained . . . if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.” 35 U.S.C. § 103(a). The obviousness analysis requires several threshold inquiries: the level of ordinary skill in the art must be established; the scope and content of the prior art must be determined; and any differences between the prior art and the claims at issue must be ascertained. *Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966).

1. Claims cannot be found obvious if an element is absent.

If a single element of the claim is absent from the prior art, the claim cannot be considered obvious. *See CFMT, Inc. v. YieldUp Int’l Corp.*, 349 F.3d 1333, 1342 (Fed. Cir. 2003) (“Obviousness requires a suggestion of all limitations in a claim.”)

(citing *In re Royka*, 490 F.2d 981, 985 (C.C.P.A. 1974)); *In re Rijckaert*, 9 F.3d 1531, 1534 (Fed. Cir. 1993) (reversing obviousness rejection where prior art did not teach or suggest all claim limitations); *Garmin Int’l, Inc. v. Patent of Cuozzo Speed Techs. LLC*, IPR2012-00001, Paper 15 at 15 (PTAB Jan. 9, 2013) (refusing to institute an *inter partes* review under 35 U.S.C. § 103 where prior art did not disclose all claim limitations).

2. A petition must address the Graham factors.

Obviousness is resolved on several factual determinations “including (1) the scope and content of the prior art, (2) any differences between the claimed subject matter and the prior art, and (3) the level of ordinary skill in the art.” *See Graham*, 383 U.S. at 17-18. Petitions for *inter partes* reviews “must address the Graham factors.” *Eizo Corp. v. Barco N.V.*, IPR2014-00358, Paper 11 at 29-30 (PTAB July 23, 2014).

3. A petition must provide articulated reasoning with rational underpinning to combine references.

The conclusion of obviousness based on a combination of references must also be supported with explicit analysis of a reason to combine those references. *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 418 (2007). The Federal Circuit has stated that such reasons must be more than “mere conclusory statements; instead, there must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness.” *In re Kahn*, 441 F.3d 977, 988 (Fed. Cir. 2006);

accord Innogenetics, N.V. v. Abbott Labs., 512 F.3d 1363, 1374 (Fed. Cir. 2008) (agreeing with the district court’s reasoning that “some kind of motivation must be shown from some source, so that the jury can understand why a person of ordinary skill would have thought of either combining two or more references or modifying one to achieve the patented method”); *see also LG Elecs., Inc. v. Cellular Commc’ns Equip. LLC*, IPR2016-00197, Paper 7 at 7-11 (PTAB April 29, 2016) (faulting a petition’s obviousness analysis for lack of sufficient articulated reasons with rational underpinnings for modifying references to achieve particular elements required in the claims).

VI. THE PETITION DOES NOT ESTABLISH A REASONABLE LIKELIHOOD OF SUCCESS

Petitioner has not met its burden of establishing a reasonable likelihood of success at least because the Petition fails to show that any of its obviousness combinations disclose each and every limitation of a challenged claim and that one of ordinary skill would have chosen to combine the cited elements to achieve the claimed inventions of the ’575 Patent. Consequently, the Board should deny the Petition and decline to institute the *inter partes* review.

Petitioner has failed to demonstrate that independent claim 1 is rendered obvious over the cited references in grounds I-VIII. Because the remaining challenged claims (claims 2, 3, 5, 8, 11, 12, 15, and 16) all depend from independent claim 1, should the Board agree that trial should not be instituted on independent

claim 1, it necessarily follows that trial should not be instituted on the dependent claims. Accordingly, Patent Owner focuses on addressing independent claim 1.

A. Grounds I-IV: Lee in View of Jahagirdar Fails to Render Obvious Independent Claim 1

Ground I relies on Lee (Ex. 1005) and Jahagirdar (Ex. 1006) to challenge independent claim 1 and claims depending therefrom. Ground II combines Peterson (Ex. 1010) with the Lee-Jahagirdar combination to challenge dependent claim 2, ground III combines Kang (Ex. 1011) with the Lee-Jahagirdar combination to challenge dependent claim 3, and ground IV combines Higashida (Ex. 1009) with the Lee-Jahagirdar combination to challenge dependent claim 11. As detailed below, Petitioner is unlikely to prevail on grounds I-IV.

1. Ground I Fails (Claims 1, 3, 5, 8, 11, 12, 15, and 16)

Lee in view of Jahagirdar fails to disclose each and every limitation of claim 1 and there is no motivation to combine Jahagirdar with Lee. Thus, Petitioner is unlikely to prevail on ground I. Because Lee in combination with Jahagirdar fails to disclose every limitation of claim 1, the challenges to the dependent claims likewise fail.

In sum, the Lee-Jahagirdar combination fails to disclose the internal “information holding unit” driven by a “microprogram” handshake with a single “power supply control unit” that sends the “shutdown request signal” to the CPU and, in response to a CPU “evacuation completed signal,” sends commands to both

the “clock generator” and the “power supply unit,” then later restores power, restarts the clock, requests CPU restoration, and branches to the saved program counter as required by claim 1 of the ’575 patent.

i. Failure to Disclose an Information Holding Unit (1[d])

Claim 1 recites “an information holding unit *for holding* information evacuated from the CPU, the information being necessary in proceeding with a program.” Petitioner points to “memory 60” of Lee as disclosing this limitation (Petition at 31-32), but memory 60 of Lee does not *hold* the information as required by the claim. In fact, Lee temporarily stores working context in memory 60, moves the information off chip to non-volatile memory 130, then shuts power down to SOC 110 (including memory 60) in which memory 60 loses the information (i.e., is volatile memory). *See* Ex. 1005 at 1:48-55, 6:66-7:7, Fig. 1. Because memory 60 loses the information, it cannot be said to be “holding information evacuated from the CPU, the information being necessary in proceeding with a program.” Indeed, Lee reiterates throughout (in its title, background, summary, and detailed description) that non-volatile memory 130 “placed outside the SOC,” not memory 60, holds the context information evacuated from the CPU. *Id.* at 1:1-6, 1:18-22, 1:63-67, 6:37-41.

- ii. Failure to Disclose Power Supply Control Unit Signaling (1[f], 1[g], [1h], [1j], [1m])

Claim 1 requires the same power supply control unit to (a) output a shutdown/restoration request signal to the CPU, (b) receive an evacuation complete signal from the CPU, (c) output a power shutdown control signal to the power supply unit, and (d) output a clock stop/supply control signal to the clock generator.

The Lee-Jahagirdar combination splits these roles into four different units (Lee's interrupt controller 20, Lee's power controller 80, Lee's reset signal generation circuit, and Jahagirdar's input/output controller 225). *See* Ex. 1005 at Fig 1; *see also* Ex. 1006 at Fig. 2B; *see also* Petition at 29, 31, 37-39. As to (a) outlined above, Petitioner contends that Lee's interrupt controller 20 outputs a shutdown request signal to the CPU and Lee's reset signal generation circuit outputs a restoration request signal to the CPU. Petition at 34, 38; *see also* Ex. 1005 at 6:10-20, 9:44-50. As to (b) and (c) outlined above, Petitioner contends Lee's power controller 80 receives the evacuation complete signal from the CPU and outputs a power shutdown control signal to the power supply unit. *See* Petition at 35-36; *see also* Ex. 1005 at 6:46-49. As to (d) outlined above, Petitioner contends that Jahagirdar's input/output controller 225 outputs clock stop/supply control signals to the clock generator. Petition at 37-39; *see also* Ex. 1006 7:12-22. Lee in combination with Jahagirdar never teaches the claimed power supply control unit that handles the above identified signaling. It cannot be said that four disparate units across two

different references teaches the claimed power supply control unit that controls power and further controls and signals to the clock generator to stop/start. *See, e.g.*, Ex. 1005 at 10:4-57, Fig. 1, Fig. 7. What is more, Jahagirdar's clock-stop is asserted by chipset signals (e.g., STPCLK#) and/or platform logic, not a single microcontroller control unit governing both clock and power as required by claim 1. *See, e.g.*, Ex. 1006 at 5:27-42.

iii. Failure to Disclose the Restore Sequence ([1o])

Claim 1 further requires that, upon a restoration factor, the power supply control unit restores power, waits for stability, then outputs both a clock supply control signal to the clock generator and a restoration request signal to the CPU; in response, the CPU executes a power supply restoration microprogram, restores the evacuated information from the information holding unit, and branches a process to the saved program counter. The Lee-Jahagirdar fails to teach "the CPU ... branch[ing] a process to an address indicated by a program counter." *See, e.g.*, Ex. 1005 at 10:34-57. The Petition instead relies on a POSITA's understanding to meet this limitation. Petition at 40 ("A POSITA would understand that a program counter (PC) is a register within the microprocessor that determines which program instruction should be executed next. Ex-1003 ¶210.").

Petitioner's reliance on expert testimony to fill gaps in the references is improper. In her July 31, 2025, Memorandum ("July 31 Memorandum"), Director

Stewart recognized the problem with using expert testimony and general declarations about what a person of ordinary skill purportedly would know. Specifically, doing such violates 37 C.F.R. § 42.104(b)(4), which requires that “[t]he petition must specify where each element of the claim is found in the prior art patents or printed publications relied upon.”¹ Director Stewart explained that “enforcement of Rule 104(b)(4) means that applicant admitted prior art (AAPA), expert testimony, common sense, and other evidence that is not ‘prior art consisting of patents or printed publications’ (collectively, ‘general knowledge’) may not be used to supply a missing claim limitation.” July 31 Memorandum at 1 (emphasis added).

Thus, ground V, based on Lee and Jahagirdar (and nothing more) fails for this reason alone.

iv. No Motivation to Combine Lee with Jahagirdar

The Petition glosses over technical incompatibilities and conflicting design objectives of these references to piece prior art together without a clear, articulated rationale explaining why a POSITA would have been motivated to combine them. In fact, a POSITA would not have been inclined to combine Lee with Jahagirdar

¹ It also violates 35 U.S.C. § 311(b) (“[a] petitioner in an inter partes review may request to cancel as unpatentable 1 or more claims of a patent only on a ground that could be raised under section 102 or 103 and only on the basis of prior art consisting of patents or printed publications.”) (emphasis added).

given the distinct objectives, technical differences, and lack of motivation in the prior art. Such a hindsight-driven combination would undermine the specific objectives and technical advantages of the microcontrollers of Lee and Jahagirdar.

Petitioner's rationale reduces to a conclusory assertion that a POSITA would "implement the save and restore functionality in Lee ... using microprograms" and "integrat[e] Jahagirdar's clock generator and microcode into Lee's systems." Petition at 2, 27. But the Petition cites no teaching in either reference that suggests swapping Lee's architecture for Jahagirdar's, relying instead on "routine" know-how of clocking and microcode as a glue. *Id.* at 25-28. Lee solves a different problem with a different structure: it evacuates the working context off chip to external non-volatile memory via a dedicated working context transmitting controller and later restores from that external memory to resume exactly at the pre-shutdown state. *See* Ex. 1005 at 1:59-3:3. Jahagirdar, by contrast, teaches microcode-directed entry to a zero-voltage state, coordinated with platform logic, where microcode saves critical CPU state in on-chip volatile memory. *See* Ex. 1006 at 8:45-54, 9:40-48, 10:18-45. These approaches are substitutes, not complements: adopting Jahagirdar's microcode sequence would displace Lee's off-chip evacuation mechanism—the very heart of Lee—rather than predictably fill in a missing detail. The Petition's attempt to bridge this gap by saying both references save and restore working context (Petition at 26-27) merely states a result and ignores the incompatible levels of

implementation (SoC controller to external non-volatile memory in Lee vs. CPU-core microcode and platform power states in Jahagirdar), offering no teaching that they should be merged or that such a merger would preserve the principles of operation of either system.

For at least the foregoing reasons, a person of ordinary skill in the art would not have been motivated to combine Lee with Jahagirdar. The asserted combination represents a hindsight-driven modification that lacks any support in the references themselves and would frustrate the design objectives of Lee. Accordingly, Petitioner's challenge based on this combination should be rejected.

2. Grounds II-IV Fail (Claims 2, 3, and 11)

Petitioner does not rely on Peterson, Kang, or Higashida to disclose any limitations of independent claim 1 from which claims 2, 3 and 11 depend. The added references (Peterson, Kang, and Higashida) are cited for different dependent claim limitations and do not cure the fundamental gaps identified above. Consequently, grounds II-IV suffer at least the same shortcomings as ground I. Thus, Petitioner is unlikely to prevail on grounds II-IV.

i. No Motivation to Combine

The tertiary references (Peterson, Kang, and Higashida) are invoked only to supply ancillary features of dependent claims. The Petition does not—and cannot—explain why a POSITA would mix the disparate clock shutdown safety protocol

teachings of Peterson, wireless terminal power collapse, always-on domain architecture of Kang, or on-chip state backup scheme of Higashida with the already-strained Lee-Jahagirdar combination. *See* § VI.A.1.iv above.

Petitioner’s add-ons do not fit the Lee–Jahagirdar architecture or problem statement, so a POSITA would lack a reason to graft them on. Peterson is a clock generator safety scheme that verifies a shutdown request against a predetermined protocol and inserts entry/exit delays to avoid accidental or unstable clock stoppage—not a context save and restore technique—and it solves a different problem than Lee’s off-chip working-context evacuation (*see* Ex. 1005 at 1:48-2:10) and Jahagirdar’s microcode-driven zero-voltage transitions (*see* Ex. 1006 at Abstract, 8:45-52). *See* Ex. 1010 at 3:10-60, 8:13-16. Indeed, Petitioner’s own rationale is limited to “minimizing accidental clock stoppage risk.” Petition at 50. Kang, by contrast, is a wireless-terminal “power collapse” design that depends on an always-on domain, sleep/paging timelines, freezing/clamping I/O, and oscillator power cycling—an architectural regime that replaces, rather than complements, Lee’s evacuation to external non-volatile memory and Jahagirdar’s microcode sequencing. *See* Ex. 1011 at Abstract, 1:65-2:36, 7:7-27. Importing Kang would force an always-on controller and domain interfaces that change the principle of operation rather than predictably fill any gap in Lee–Jahagirdar. And Higashida teaches a different solution entirely—retaining state in an on-chip backup region

powered by a lower-voltage backup supply—so adopting it would supplant Lee’s core innovation of evacuating context to off-chip memory. *See* Ex. 1009 at 2:64-4:14. Indeed, Petitioner admits Higashida would “obviate the need to transfer working context to off-chip” in Lee, confirming it’s an alternative design path, not a complementary module a POSITA would be motivated to incorporate into the Lee–Jahagirdar combination. Petition at 53.

For at least the foregoing reasons, a person of ordinary skill in the art would not have been motivated to combine Peterson, Kang, or Higashida with the Lee–Jahagirdar combination. The asserted combinations represent a hindsight-driven modification that lacks any support in the references themselves. Accordingly, Petitioner’s challenge based on these combinations should be rejected.

B. Grounds V-VIII: Shikata in View of Crump Fails to Render Obvious Independent Claim 1

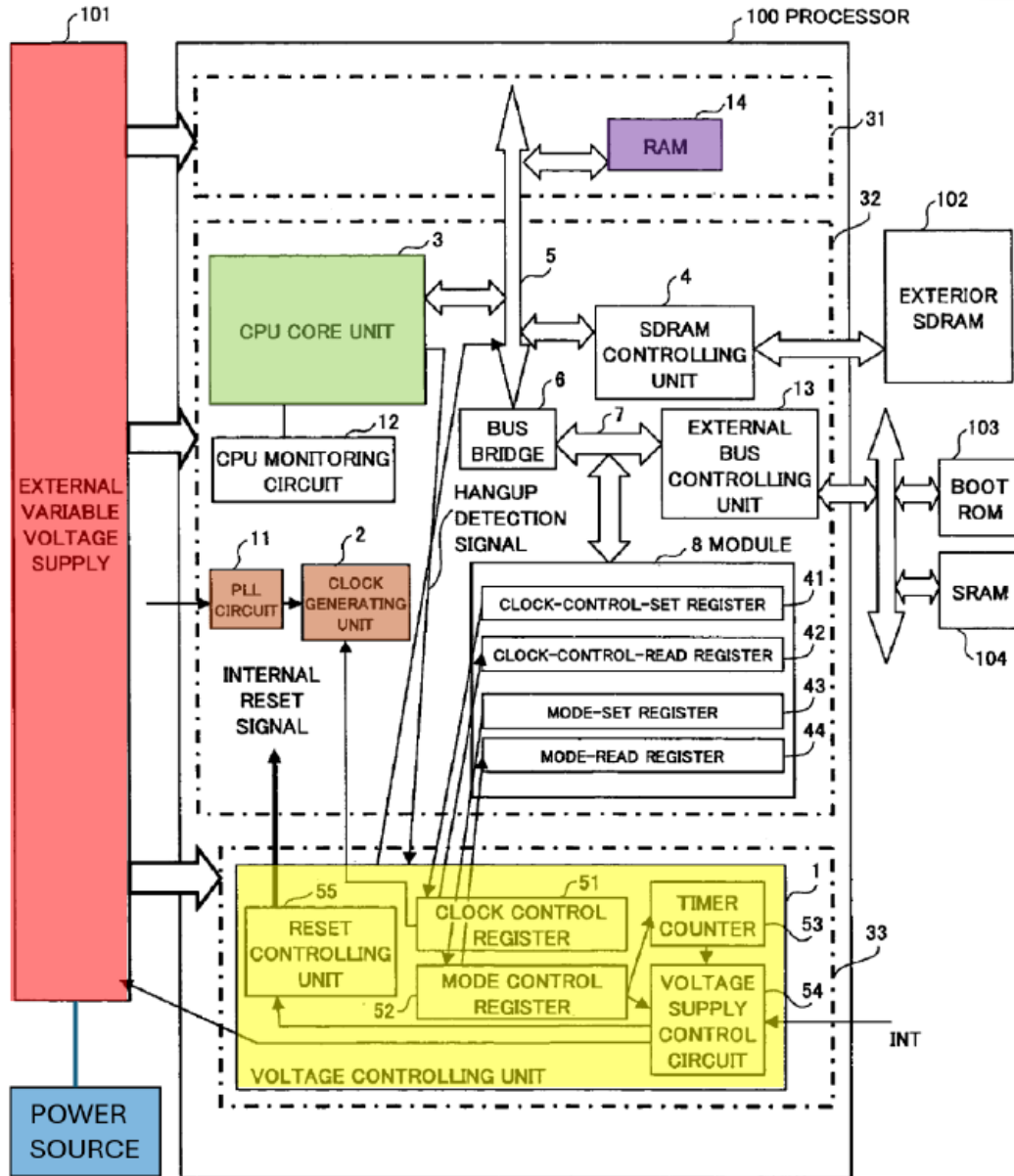
Ground V relies on Shikata (Ex. 1007) and Crump (Ex. 1008) to challenge independent claim 1 and claims depending therefrom. Ground VI combines Peterson (Ex. 1010) with the Shikata-Crump combination to challenge dependent claim 2, ground VII combines Kang (Ex. 1011) with the Shikata-Crump combination to challenge dependent claim 3, and ground VIII combines Chung (Ex. 1012) with the Shikata-Crump combination to challenge dependent claim 16. As detailed below, Petitioner is unlikely to prevail on grounds V-VIII.

1. Ground V Fails (Claims 1, 5, 11, 12, and 15)

Shikata in view of Crump fails to disclose each and every limitation of claim 1 and there is no motivation to combine Shikata and Crump. Thus, Petitioner is unlikely to prevail on ground V. Because Shikata in combination with Crump fails to disclose every limitation of claim 1, the challenges to the dependent claims likewise fail.

i. Failure to Disclose the Claimed Power Supply Unit (1[b])

Claim 1 requires a “microcontroller comprising ... a power supply unit arranged between the CPU and a power supply device.” Petitioner, relying on Shikata, contends processor 100 is the microcontroller and external variable voltage supply 101 is the power supply unit. Petition at 60. However, a cursory review of Shikata shows that processor 100 does not comprise *external* variable voltage supply 101:



Petition at 59 (citing Ex. 1007, Fig. 5). The Petition instead relies on hindsight stating that “it would have been obvious for a POSITA to incorporate the external variable voltage supply within the processor.” Petition at 61. Neither Shikata nor Crump explicitly disclose this limitation. Thus, Petitioner has not met its burden to show the Shikata-Crump combination of ground V is likely to prevail.

ii. Failure to Disclose a Shutdown Request / Evacuation Completed Signaling ([1f]-[1j])

Claim 1 requires “the power supply control unit outputs a shutdown request signal to the CPU” and “the CPU ... outputs an evacuation completed signal to the power supply control unit.” Shikata’s voltage controlling unit drops power without ever consulting the CPU core unit; there is no signal sent from the “power supply control unit” to the “CPU” requesting shutdown, nor any signal returned indicating evacuation completion as required by claim 1. *See, e.g.*, Ex. 1007, 4:43-5:20, 8:18-42. Without more, Petitioner resorts to claiming that “it would also have been obvious.” Petition at 63. And Crump likewise lacks this bidirectional exchange.

iii. No Motivation to Combine Shikata with Crump.

Petitioner’s attempt to combine Shikata with Crump is fundamentally flawed. Petitioner’s theory asks a POSITA to splice the personal computer suspend-to-disk snapshot of Crump into Shikata’s embedded, on-chip retention/fast-resume design, but the two solve different problems with incompatible architectures.

Shikata achieves a fast, low-leakage standby by saving register values and a recovery boot program into on-chip internal RAM and then booting from the internal RAM to restore the saved registers on wake—explicitly to enable high-speed recovery. *See* Ex. 1007 at 2:64-3:30, 4:42-5:25. By contrast, Crump is a personal computer suspend-to-disk regime coordinated by microcode: it saves CPU and other system device states to a “Suspend File” on an external hard drive. *See* Ex. 2008 at

11:15-32, 38:59-67, 39:26-36, 46:64-67, Fig. 10A. Grafting Crump's disk-image, storage and operating system dependent machinery onto Shikata would supplant Shikata's integrated, on-chip retention path and undermine its core goal of high-speed resume, while adding platform components (e.g., an external hard drive) that Shikata's partitioned power-down expressly avoids. *See, e.g.*, Ex. 1007 at 3:17-24 (Shikata "eliminates a need to access the boot ROM that is extremely slow, and significantly reduces the number of processing steps, thereby achieving high-speed register evacuation and recovery in a simple and efficient manner."). A POSITA would see these as non-complementary, competing regimes. Petitioner's own rationale is reduced to the generic observation that both save/restore states to reduce power (Petition at 56), which is classic hindsight that ignores Shikata's express aim to avoid slow external memory paths. Petitioner does not identify any teaching that these distinct mechanisms should be merged to yield a predictable, benefit-preserving improvement.

For at least the foregoing reasons, a person of ordinary skill in the art would not have been motivated to combine Shikata with Crump. The asserted combination represents a hindsight-driven modification that lacks any support in the references themselves and would frustrate the design objectives of Shikata. Accordingly, Petitioner's challenge based on this combination should be rejected.

2. Grounds VI-VIII Fail (Claims 2, 3, and 16)

Petitioner does not rely on Peterson, Kang, or Chung to disclose independent claim 1 from which claims 2, 3 and 16 depend from. The auxiliary references (Peterson, Kang, and Chung) do not fill the missing microprogram and handshake features of claim 1 identified above. Consequently, grounds VI-VIII suffer at least the same shortcomings as ground V, thus, Petitioner is unlikely to prevail on grounds VI-VIII.

i. No Motivation to Combine

Peterson, Kang, and Chung are only relied on to disclose ancillary features of dependent claims. The Petition does not—and cannot—explain why a POSITA would mix the disparate clock shutdown safety protocol teachings of Peterson, wireless terminal power collapse, always-on domain architecture of Kang, and system controller power/clock management scheme of Chang with the already-strained Shikata-Crump combination. *See* § VI.B.1.iii above.

A POSITA would have had no reason to graft Peterson, Kang, or Chung onto the Shikata–Crump scheme because each tertiary reference solves a different problem within a different power-management regime, and adopting any of them would require redesigns that change Shikata–Crump’s principle of operation. In contrast to Shikata and Crump, Peterson is a clock generator shut-down safety scheme that refuses to stop the clock unless a predetermined access protocol is

satisfied and that inserts entry/exit delays to avoid inadvertent or unstable stoppage—nothing about saving or restoring processor context. Ex. 1010 at 3:10-60, 8:13-16. Importing Peterson would not advance Shikata–Crump’s context-evacuation/resume mechanisms. Kang teaches a wireless-terminal “power collapse” architecture with an always-on domain, scheduled no-shutdown paging slots, I/O freeze/isolation, and oscillator power cycling to keep radios reachable. Ex. 1011 at Abstract, 1:65-2:36, 7:7-27. Adopting Kang would replace, not complement, Shikata–Crump’s standby/restore model and would add radio-centric constraints and isolation hardware that Shikata–Crump does not contemplate. And Chung tackles a different problem—preventing power feedback and latch-up when the CPU is powered down while the system (including the clocking infrastructure) remains powered—by tristating system controller outputs to the CPU. Ex. 1012 at 3:9-30, 3:52-5:20, 8:4-9. Chung’s approach is fundamentally inconsistent with Shikata’s explicit suspension of the clock during standby and its partitioned power-down of most blocks. Petitioner’s own theory treats these tertiary teachings as generic additions to Shikata–Crump, yet these references conflate distinct problem statements and operating contexts. Thus, Petitioner relies on hindsight rather than a coherent, contemporaneous rationale to combine.

For at least the foregoing reasons, a person of ordinary skill in the art would not have been motivated to combine Peterson, Kang, or Chung with the Shikata-

Crump combination. The asserted combinations represent a hindsight-driven modification that lacks any support in the references themselves. Accordingly, Petitioner's challenge based on these combinations should be rejected.

VII. PATENT OWNER'S FINAL COMMENTS

Patent Owner does not concede the legitimacy of any arguments in the Petition that are not specifically addressed herein and expressly reserves the right to rebut any such arguments in its Patent Owner Response if *inter partes* review is instituted. Similarly, Patent Owner also does not concede any underlying contentions in the Petition and reserves the right to rebut them later. Additionally, Patent Owner is not limited to the arguments presented here in this Preliminary Response, but expressly reserves the right to raise further arguments, including claim construction arguments, not presented in this Preliminary Response. Patent Owner also incorporates and makes reference to the arguments presented in Patent Owner's Request for Discretionary Denial of Institution (Paper 6).

VIII. CONCLUSION

Petitioner has not met their burden of showing that any combination of references relied upon in the Petition disclose or suggest multiple elements of the independent claims. Consequently, Petitioner has not met their burden of showing a reasonable likelihood of prevailing. Patent Owner respectfully submits that the Board should deny institution.

Dated: September 22, 2025

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CERTIFICATE OF COMPLIANCE WITH WORD COUNT

Pursuant to 37 C.F.R. § 42.24(d), I certify that this Response complies with the type-volume limits of 37 C.F.R. § 42.24(b)(1) because it contains 5,384 words, excluding the parts of this Patent Owner's Preliminary Response that are exempted by 37 C.F.R. § 42.24(a), according to the word processing system used to prepare this Patent Owner's Preliminary Response.

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CERTIFICATE OF SERVICE

The undersigned certifies that the foregoing Patent Owner's Preliminary Response was served on September 22, 2025 to Lead and Back-up Counsel for Petitioner at the service address provided in Petitioner's Mandatory Notices:

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