IN THE UNITED STATES DISTRICT COURT
FOR THE WESTERN DISTRICT OF TEXAS
WACO DIVISION

COLLABO INNOVATIONS, INC., a Delaware Corporation, Plaintiff v. QUALCOMM INCORPORATED and QUALCOMM TECHNOLOGIES, INC., both Delaware Corporations, Defendants	CIVIL ACTION NO. 6:24-cv-00472 **JURY TRIAL DEMANDED**

PLAINTIFF'S COMPLAINT FOR PATENT INFRINGEMENT

Collabo Innovations, Inc. ("Collabo") files this Complaint against Qualcomm Incorporated and Qualcomm Technologies, Inc. (together, "Qualcomm" or "Defendants"), for their infringements of U.S. Patent No. 7,930,575.

THE PARTIES

1. Collabo Innovations, Inc. ("Collabo") is a Delaware corporation with a principal place of business in Plano, TX, 75024.

2. Defendant Qualcomm Incorporated ("QCI") is a corporation organized and existing under the laws of Delaware and maintains established places of business at 9600 N. Mopac, Suite 900, Stonebridge Plaza II, Austin, Texas 78759 and 13929 Center Lake Drive, Parmer Building 1 Austin, Texas 78753. QCI may be served in Texas via its registered agent Prentice Hall Corp. System, 211 E. 7th Street, Suite 620, Austin, TX 78701-3218.

3. Defendant Qualcomm Technologies, Inc. ("QTI") is a corporation organized and existing under the laws of Delaware and maintains established places of business at 9600 N. Mopac, Suite 900, Stonebridge Plaza II, Austin, Texas 78759 and 13929 Center Lake Drive,

Parmer Building 1, Austin, Texas 78753. QTI may be served in Texas via its registered agent Corporation Service Company d/b/a CSC-Lawyers Incorporating Service Company, 211 E. 7th Street, Suite 620, Austin, TX 78701.

4. QTI is a wholly-owned subsidiary of QCI and, together with its affiliated subsidiaries, serves and performs substantially all of Qualcomm's research and development efforts, its engineering operations, and its products and services businesses. *See* https://www.qualcomm.com/company. Such relevant QTI-affiliated subsidiaries include, at least, Qualcomm CDMA Technologies and Qualcomm CDMA Technologies Asia Pacific Pte. Ltd.

5. Qualcomm is one of the world's premier manufacturers of integrated circuits for the wireless device industry. Its website states that "[r]eferences to 'Qualcomm' may mean Qualcomm Incorporated, or subsidiaries or business units within the Qualcomm corporate structure, as applicable." *Id*. Qualcomm's website further states that "Qualcomm Technologies, Inc., a subsidiary of Qualcomm Incorporated, operates, along with its subsidiaries, substantially all of our engineering, research and development functions, and substantially all of our products and services businesses, including our QCT semiconductor business." *Id*.

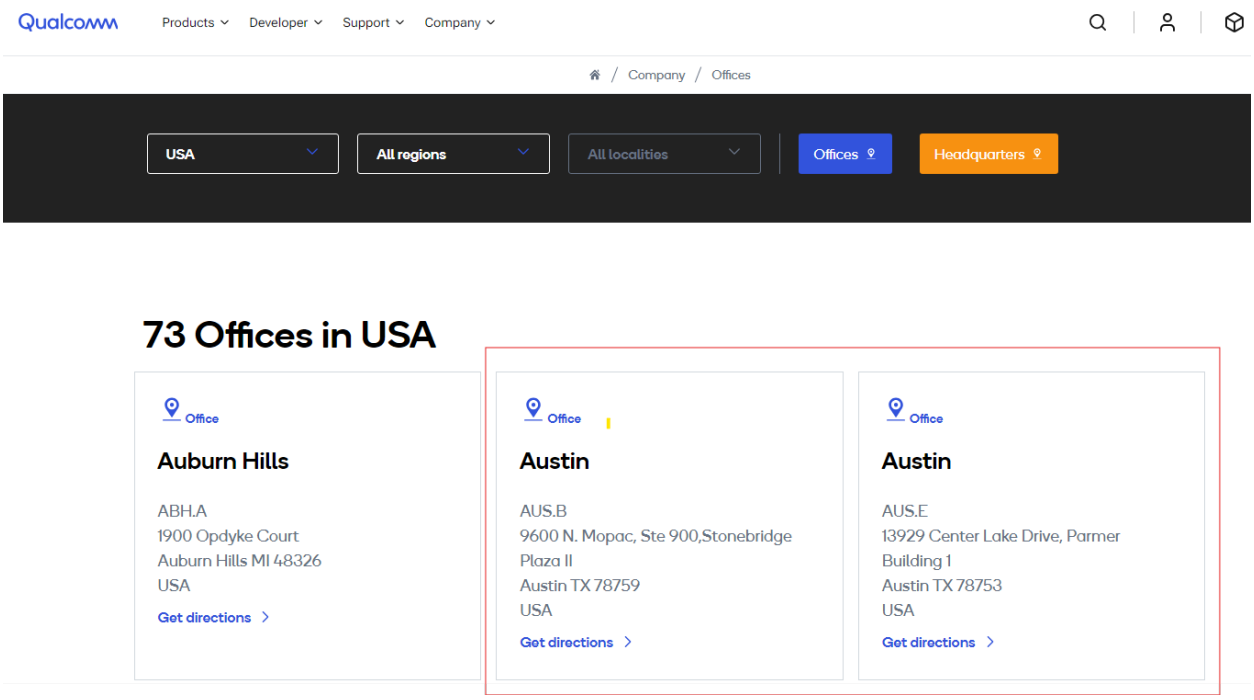
6. QCI, QTI, and their subsidiaries and related companies share the same management, common ownership, advertising platforms, facilities, distribution and sales channels, and accused products and product lines. In this way, QCI, QTI, and their subsidiaries and related companies operate as a singular, unitary business enterprise and are, thus, jointly, severally and communally liable for the acts of patent infringement detailed below.

7. QCI, QTI, and their subsidiaries and related companies are doing business collectively, directly and through agents, on a persistent and ongoing basis in this District and elsewhere in the United States, and they each have regular and established places of business here.

JURISDICTION AND VENUE

8. This is an action for patent infringement arising under the patent laws of the United States, 35 U.S.C. §§ 1, *et seq*. This Court has jurisdiction over this action pursuant to 28 U.S.C. §§ 1331 and 1338(a).

9. This Court has personal jurisdiction over Qualcomm because it has engaged, and continues to engage, in continuous, systematic, and substantial activities within this State, including the substantial marketing and sale of products and services within this State and this District. Indeed, this Court has personal jurisdiction over Qualcomm because it has committed acts giving rise to Collabo's claims for patent infringement within and directed to this District, has derived substantial revenue from its goods and services provided to individuals and entities in this State and this District, and maintains regular and established places of business in this District, including at least its two brick-and-mortar locations in Austin, Texas:[1]



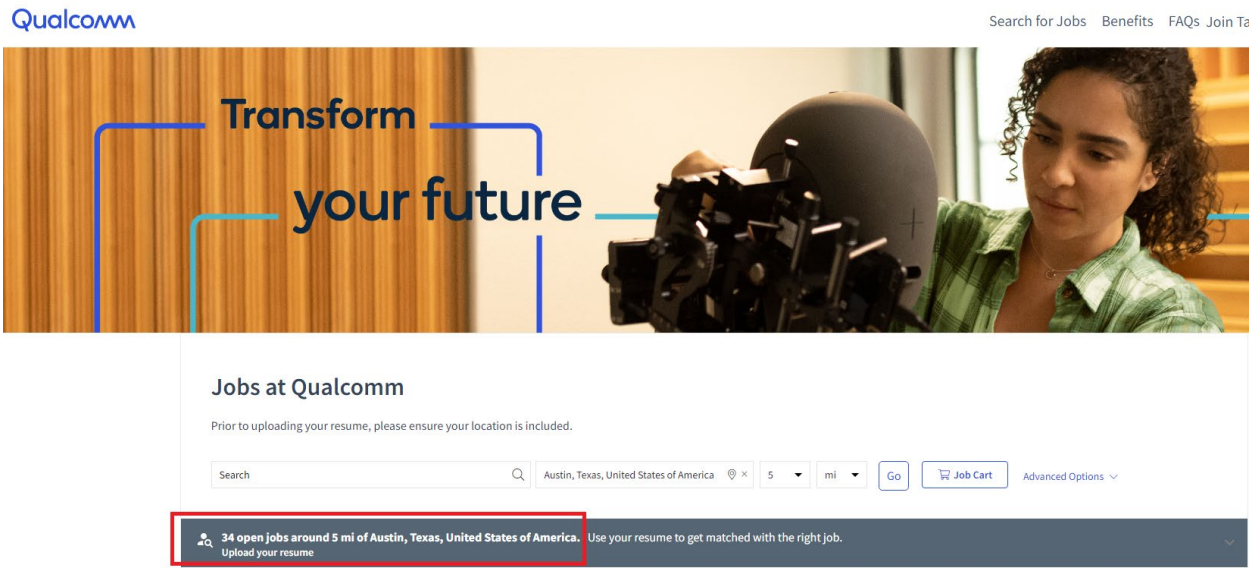
[1] *See* https://www.qualcomm.com/company/facilities/offices?country=USA&page=2

10. Relative to patent infringement, Qualcomm has committed and continues to commit acts in violation of 35 U.S.C. § 271, and has made, used, offered for sale, sold, and imported infringing products, systems, and services in this State, including this District, and has otherwise engaged in infringing conduct within and directed at, or from, this District. Such infringing products, systems, and services (collectively, the "Accused Instrumentalities") include Qualcomm processors such as the Qualcomm Snapdragon 600 Processor APQ8064 and other processors and platforms offered and sold by Qualcomm that support low power state with power collapse (and similar functionality).

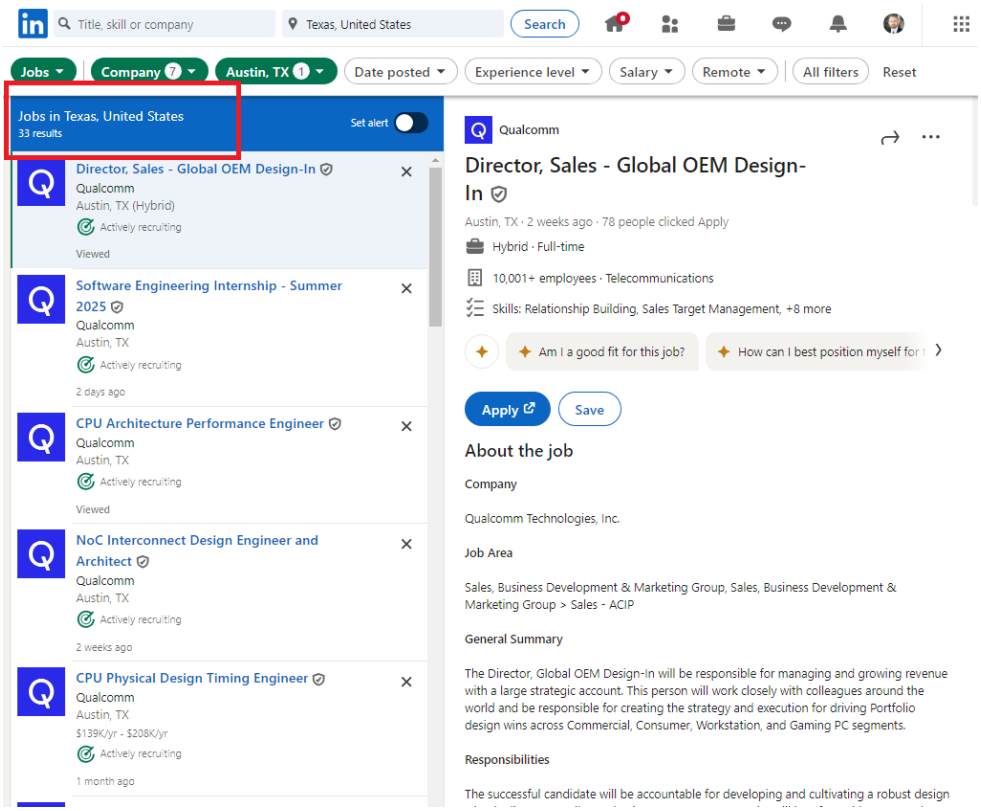
11. Qualcomm's infringing activities have caused harm to Collabo in this District. Qualcomm and/or its partners and agents offer to sell and sell the Accused Instrumentalities within this District, and on information and belief, Qualcomm, its partners and agents, and/or their customers use the Accused Instrumentalities in this District in infringing ways. These are purposeful acts and transactions in this State and this District such that Qualcomm reasonably should know and expect that it can be haled into this Court to answer for its actions.

12. Moreover, this Court maintains personal jurisdiction over Qualcomm because Qualcomm conducts business in this State by, among other things, "recruit[ing] Texas residents, directly or through an intermediary located in this State, for employment inside or outside this State." Tex. Civ. Prac. & Rem. Code § 17.042(3). For instance, Qualcomm lists numerous job openings in Texas (as of Aug. 22, 2024):[2]

[2] https://careers.qualcomm.com/careers?location=Austin%2C%20Texas%2C%20United%20States%20of%20America&pid=446697682796&domain=qualcomm.com&sort_by=relevance&location_distance_km=8&triggerGoButton=true

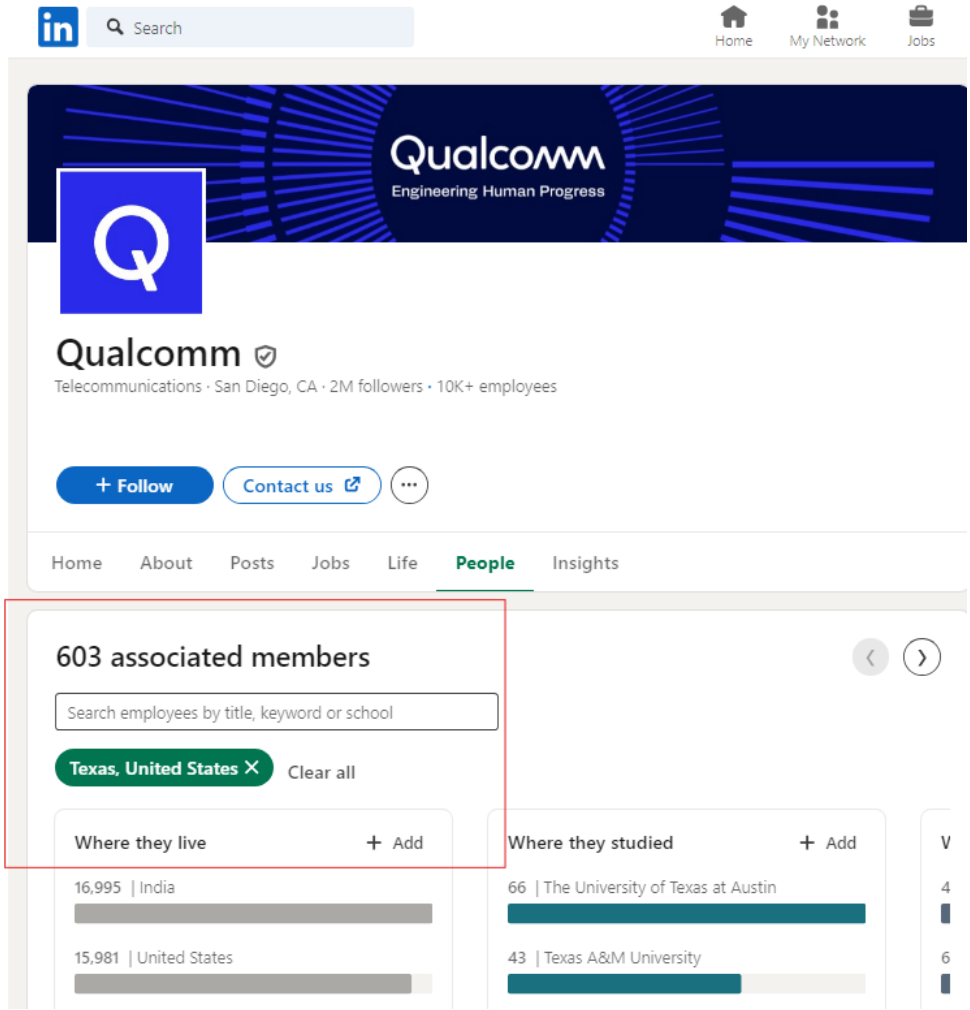


13. Qualcomm also lists its job openings in Texas on LinkedIn (as of Aug. 22, 2024):[3]



[3] https://www.linkedin.com/jobs/search/?currentJobId=3981845068&f_C=2017%2C154985%2C162572%2C2923434%2C38387%2C595224%2C75115234&f_CR=103644278&geoId=102748797&origin=JOB_SEARCH_PAGE_LOCATION_AUTOCOMPLETE&refresh=true&sortBy=R

14. Further, on Qualcomm's LinkedIn page, it boasts 603 "associated members" in its Texas offices (as of Aug. 1, 2024):[4]



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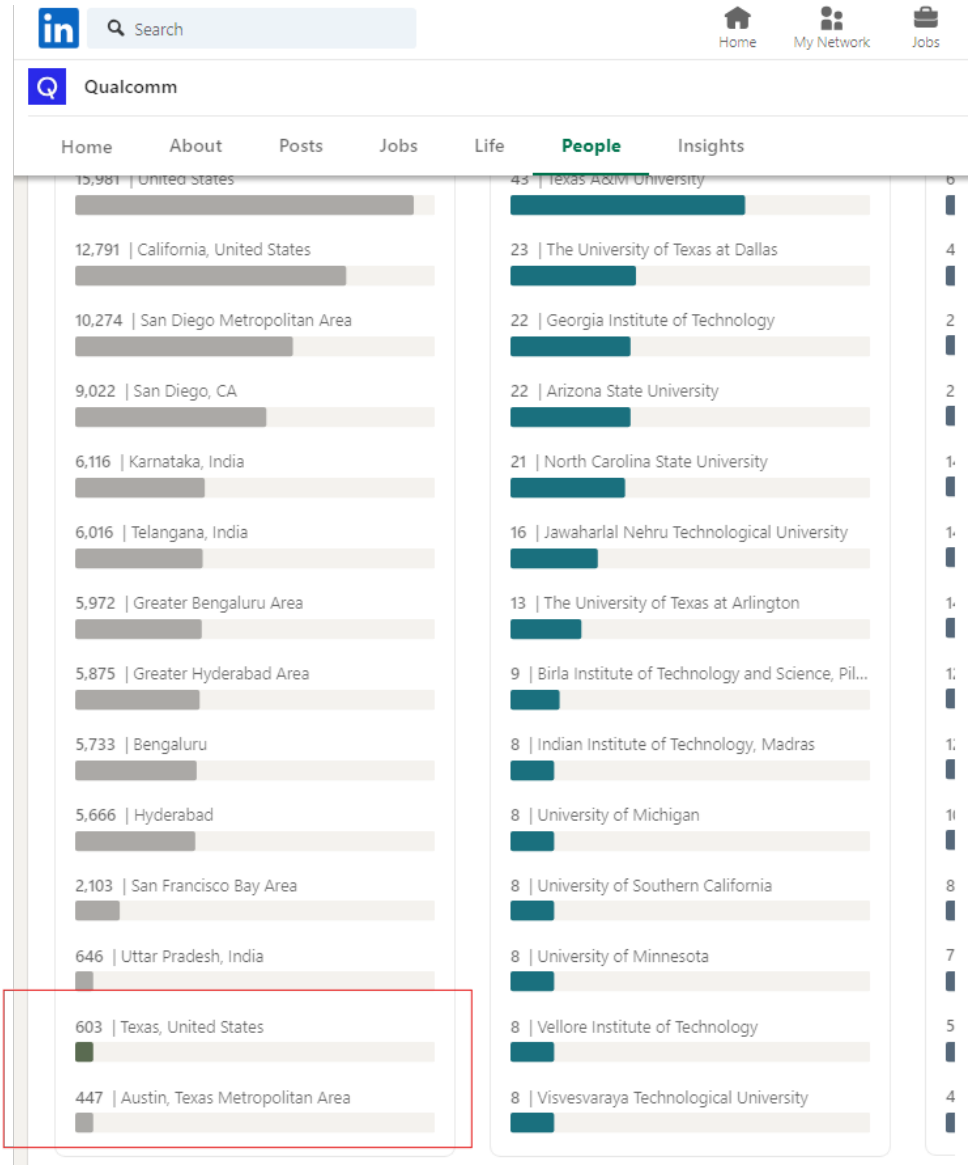
[4] https://www.linkedin.com/company/qualcomm/people/?facetGeoRegion=102748797



15. Venue is proper in this District under 28 U.S.C. §§ 1391 and 1400(b) because Qualcomm has two regular and established places of business in Austin, which is in this District. Venue is further proper in this District because Qualcomm has directly infringed and/or induced the infringements of others, including its customers, in this District by offering for sale and selling Accused Instrumentalities in this District, using Accused Instrumentalities in infringing ways in this District, and inducing infringing customer use of Accused Instrumentalities in this District.

THE ASSERTED PATENT

16. On April 19, 2011 the United States Patent and Trademark Office duly and legally issued United States Patent No. 7,930,575 B2 ("the '575 patent" or "the Asserted Patent"), which is titled "Microcontroller for Controlling Power Shutdown Process." The '575 patent identifies Yukari Suginaka, Toshifumi Hamaguchi, Yoshitaka Kitao, and Shinya Muramatsu as inventors. The'575 patent has been assigned to Plaintiff Collabo, which holds all right, title, and interest in the '575 patent, including the right to sue for, and recover, damages for past, present and future infringements.

17. To the extent necessary, Collabo has complied with the requirements of 35 U.S.C. § 287, such that Collabo may recover pre-suit damages.

DEFENDANT'S PRE-SUIT KNOWLEDGE OF ITS INFRINGEMENT

18. Prior to the filing of this Complaint, Collabo sent a letter to Qualcomm notifying Qualcomm that its processors infringe the '575 patent and that it needs to take a license. Qualcomm has not agreed to license the Asserted Patent, and Collabo brought this action to protect its rights.

COUNT I

(INFRINGEMENT OF U.S. PATENT NO. 7,930,575)

19. Plaintiff incorporates the preceding paragraphs herein by reference.

20. This cause of action arises under the patent laws of the United States, and, in particular, 35 U.S.C. §§ 271, *et seq*.

21. Collabo is the owner of all substantial rights, title, and interest in and to the '575 patent, including the right to exclude others and to enforce, sue, and recover damages for past, current and future infringements.

22. The '575 patent is valid, enforceable, and was duly and legally issued by the United States Patent and Trademark Office on April 19, 2011, after a full and fair examination.

23. Qualcomm has directly and/or indirectly infringed, and continues to directly and/or indirectly infringe, one or more claims of the ’575 patent in this District, and elsewhere in Texas and the United States, by making, using, offering to sell, selling, and/or importing Accused Instrumentalities, and by actively inducing others to make, use, offer to sell, sell, and/or import, Accused Instrumentalities, and their components and processes, that incorporate the fundamental technologies covered by the ’575 patent. As noted previously, this includes, but is not limited to, Qualcomm processors supporting low power state with power collapse and similar functionality, such as the Qualcomm Snapdragon 600 Processor APQ8064.

Direct Infringement (35 U.S.C. § 271(a))

24. Qualcomm has directly infringed and continues to directly infringe one or more claims of the ’575 patent in this District and elsewhere in Texas and the United States.

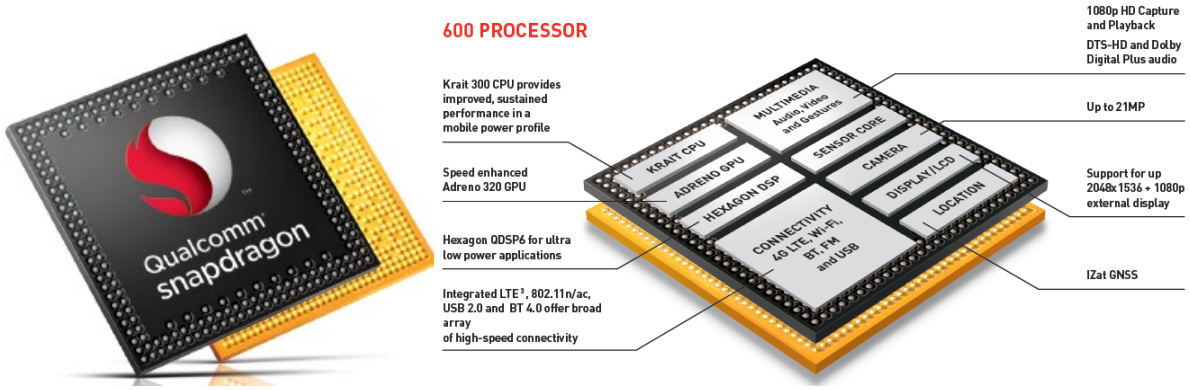
25. Qualcomm has directly infringed and continues to directly infringe, either by itself or via agents, at least claim 1 of the ’575 patent,[5] as set forth under 35 U.S.C. § 271(a), by making, using, offering for sale, selling, and/or importing Accused Instrumentalities. Moreover, Qualcomm makes, offers to sell, and sells Accused Instrumentalities outside of the United States and then imports and delivers those Accused Instrumentalities to its customers, distributors, agents and/or subsidiaries in the United States. In the case that Qualcomm delivers Accused Instrumentalities outside of the United States, it does so knowing and intending that those Accused Instrumentalities are destined for the United States, and/or that they are designed and designated for sale in the

[5] Wherever Collabo identifies specific claims of the Asserted Patent infringed by Qualcomm, Collabo expressly reserves the right to identify additional claims (and, for that matter, products) in its infringement contentions in accordance with applicable local patent rules and the Court’s case management order. Claims explicitly identified in this Complaint are provided for notice pleading only.

United States, thereby directly infringing the ’575 patent. *See, e.g., Lake Cherokee Hard Drive Techs., L.L.C. v. Marvell Semiconductor, Inc.*, 964 F. Supp. 2d 653, 658 (E.D. Tex. 2013).

26. Furthermore, Qualcomm directly infringes the ’575 patent through its direct involvements in, and control of, the activities of subsidiaries and agents. Subject to Qualcomm’s direction and control, the subsidiaries and agents conduct activities that constitute direct infringement of the ’575 patent under 35 U.S.C. § 271(a) by making, using, offering for sale, selling, and/or importing Accused Instrumentalities. Qualcomm receives direct financial benefit from such infringements of its U.S.-based sales subsidiaries and agents.

27. By way of illustration only, the Accused Instrumentalities include each and every element of claim 1 of the ’575 patent. The Accused Instrumentalities are “microcontrollers” that comprise the limitations of claim 1. For example, the Qualcomm Snapdragon 600 Processor APQ8064, is a microcontroller:



Qualcomm Snapdragon 600 Processors, Product Brief (available at https://www.qualcomm.com /content/dam/qcomm-martech/dm-assets/documents/snapdragon-600-processor-product-brief.pdf).

28. The Accused Instrumentalities comprise “a CPU.” For example, the Qualcomm Snapdragon 600 Processor APQ8064 comprises a CPU, including four Krait mP cores and one QDSP6 core, which is the low power audio subsystem (LPASS) core:

1.3.2 Summary of key APQ8064E features

Table 1-4 lists all the key features of APQ8064E.

Table 1-4 Key APQ8064E features

Feature	APQ8064E capability
Processors	
Processors	
Applications subsystem	Four Krait mP cores (to 1.5 GHz) plus one QDSP6 core (to 500 MHz)
RPM system	ARM7
Smart peripheral subsystem	ARM7
BT/FM	ARM9
GPS subsystem	Cortex A5
Cache	2 MB L2 cache (combined)
Coprocessor	VeNum 128-bit SIMD multimedia (Single Instruction Multiple Data)

Qualcomm Snapdragon 600E Processor APQ8064E Device Specification, p.16 (available at https://developer.qualcomm.com/download/sd600/snapdragon-600-device-spec.pdf).

Low-power audio subsystem (LPASS)	
Power efficient audio processing	New QDSP6v4 core New SLIMbus interfaces ■ Approximately 24 Mbps of uncompressed audio data bandwidth ■ SLIMbus includes customized slew-rate limited IOs Support for up to 6 digital microphones
Low-power features	Power gating within LPASS core QDSP6 supports L2 cache data retention during power collapse Supported modes: ACTIVE / IDLE / DORMANT / OFF
Clock control	Local clock control with dedicated PLL
Low-power memory	Dedicated SRAM Bitstream buffer, PCM buffers, DSP OS
Musical Instrument Digital Interface (MIDI)	Acceleration HW 128-poly MIDI processing
Audio DSP	Near-zero cache miss-rates during steady-state low-power audio playback Separate voltage domain is scaled with performance requirements
Audio interfaces	PCM, DMIC, MI^{2}S/I^{2}S legacy low-power audio interfaces

Qualcomm Snapdragon 600E Processor APQ8064E Device Specification, p.22 (available at https://developer.qualcomm.com/download/sd600/snapdragon-600-device-spec.pdf).

29. The Accused Instrumentalities comprise "a power supply unit arranged between the CPU and a power supply device for supplying power to the CPU." For example, the Qualcomm Snapdragon 600 Processor APQ8064 includes power and sleep control features demonstrating that there exists at least one power supply unit that receives power from an external power device and supplies power to the cores (e.g., the four Krait mP cores and LPASS core):

1.6.3 Power and sleep control

Four types of sleep modes reduce APQ leakage current:

1. Clock off
   - Clock sources (CXO and PXO) are turned off, but the core and memory power-supply voltages operate normally.
   - Upon wakeup, one of the interrupt sources is triggered, and then forwards the interrupt to other parts of the RPM system.
2. Core and memory supply voltages minimized
   - Up to four preprogrammed SSBI commands are sent to the PMIC to initiate the shutdown or wakeup process.
   - Core supply voltage is reduced first, and then the memory supply voltage.
   - Memory states and logic states are preserved.
   - Clocks are also turned off.
3. Core power-supply voltage collapsed and memory supply voltage minimized (but still on)
   - Pertinent comments from #2 apply, except the following:
     - Core voltage is collapsed, not just minimized.
     - Memory contents are retained, but logic states are lost.
4. Full IC power collapse (core and memory supply voltages collapsed)
   - Pertinent comments from #2 apply, except the following:
     - Both voltages are collapsed, not just minimized.
   - Lowest leakage current, but requires saving and restoring necessary states.
   - Software overhead and complexity are significant.

Qualcomm Snapdragon 600E Processor APQ8064E Device Specification, p.28 (available at https://developer.qualcomm.com/download/sd600/snapdragon-600-device-spec.pdf).

Low-power audio subsystem (LPASS)	
Power efficient audio processing	New QDSP6v4 core New SLIMbus interfaces ■ Approximately 24 Mbps of uncompressed audio data bandwidth ■ SLIMbus includes customized slew-rate limited IOs Support for up to 6 digital microphones
Low-power features	Power gating within LPASS core QDSP6 supports L2 cache data retention during power collapse Supported modes: ACTIVE / IDLE / DORMANT / OFF
Clock control	Local clock control with dedicated PLL

Qualcomm Snapdragon 600E Processor APQ8064E Device Specification, p.21 (available at https://developer.qualcomm.com/download/sd600/snapdragon-600-device-spec.pdf).

30. The Accused Instrumentalities comprise "a power supply control unit for controlling the CPU and the power supply unit." For example, the power and sleep controls for the Qualcomm Snapdragon 600 Processor APQ8064 demonstrate that there is a control unit, such as the RPM (resource and power manager) and the SPM (subsystem power manager), that controls the power delivery to components including the cores, memory, and clock:

3.6 Resource and power manager (RPM)

Main RPM objective: lower the IC's average power consumption – static (1) and dynamic (2)

1. Static power management (primarily to limit leakage current)
   - Avoids using the high-powered processor
   - Executes code exclusively from internal RAM
   - Enables reduced logic supply of 0.5 V
2. Dynamic power management
   - Rapidly configures shared system resources and power-level configurations without impacting active processes and workloads.
   - Achieves optimal clock rate and supply voltage settings according to workload.
   - Improves overall system power efficiency while maintaining quality-of-service.
   - Minimizes overhead and latency needed to make voltage and clock change decisions.

3.6.1 Key RPM features

- Fast response times, low latency – less than 1 ms for clock frequency requests, 10 ms for supply voltage requests
- Autonomous and coordinated controls
  - Adjusts frequency, voltage, and resource usage without impacting other subsystems
  - Controls shared resources without other subsystems being active
  - Supports voting mechanisms for resource management
- Security – RPM is trusted at all times
  - Authenticates and validates trust level of subsystems calling RPM
  - Employs QFPROM
  - The Krait applications processor is assumed to be the secure root-of-trust (SROT) after initial boot
- Performs initial boot, coordinates other subsystems' boot-ups
- Resources controlled include: power management; clock sources and routing (CXO, PXO, sleep); supply voltages; clock frequencies; temperature compensation; and elements of the other APQ subsystems

Resource and power manager (RPM)	Improved efficiency through clock control, split-rail power collapse and voltage scaling, supports several low-power sleep modes Enables new boot sequences compared to previous APQs

Qualcomm Snapdragon 600E Processor APQ8064E Device Specification, p.79 (available at https://developer.qualcomm.com/download/sd600/snapdragon-600-device-spec.pdf); *see also id.* at 18 (defining RPM).

31. The Accused Instrumentalities comprise "an information holding unit for holding information evacuated from the CPU, the information being necessary in proceeding with a program." For example, in the Qualcomm Snapdragon 600 Processor APQ8064 "full IC power collapse" mode, the memory states and logic are preserved, which is achieved through an information holding unit, such as, for example, the L1/L2 cache in the LPASS and Krait cores:

1.6.3 Power and sleep control

Four types of sleep modes reduce APQ leakage current:

1. Clock off
   - Clock sources (CXO and PXO) are turned off, but the core and memory power-supply voltages operate normally.
   - Upon wakeup, one of the interrupt sources is triggered, and then forwards the interrupt to other parts of the RPM system.
2. Core and memory supply voltages minimized
   - Up to four preprogrammed SSBI commands are sent to the PMIC to initiate the shutdown or wakeup process.
   - Core supply voltage is reduced first, and then the memory supply voltage.
   - Memory states and logic states are preserved.
   - Clocks are also turned off.
3. Core power-supply voltage collapsed and memory supply voltage minimized (but still on)
   - Pertinent comments from #2 apply, except the following:
     - Core voltage is collapsed, not just minimized.
     - Memory contents are retained, but logic states are lost.
4. Full IC power collapse (core and memory supply voltages collapsed)
   - Pertinent comments from #2 apply, except the following:
     - Both voltages are collapsed, not just minimized.
   - Lowest leakage current, but requires saving and restoring necessary states.
   - Software overhead and complexity are significant.

Qualcomm Snapdragon 600E Processor APQ8064E Device Specification, p.28 (available at https://developer.qualcomm.com/download/sd600/snapdragon-600-device-spec.pdf).

Table 1-5 APQ8064E chip subsystems

Feature	APQ8064E capability
Krait microprocessor subsystem	
Fast and power-efficient Krait cores	
ARM7 architecture extensions	Virtualization & 36-bit physical addressing
	QGIC2 interrupt controller includes virtualization extension ARM generic timer (QTIMER) 2nd-generation SAW (SAW2) Dynamic power management using SAW2 New address map to support security requirements
Quad Krait mP CPUs, each with:	Operating frequency up to 1.5 GHz 2 MB L2 cache 32 kB L1 instruction and data caches ARM v7 compliant TrustZone support VeNum 128-bit SIMD MM coprocessor
Shared L2 cache	2 MB, 8-way set associative with ECC Hardware-enforced coherency, including slave port Dual-interleaved AXI master ports increase memory BW L2 lines individually lockable to create virtual TCM
KMSS AHB	32-bit at 66 MHz Local connection from CPUs to memory High-BW multimedia traffic mostly localized to separate multimedia FABRIC Tiered arbitration to enable efficient bus/memory sharing with priority for CPUs
SDRAM memory	See Section 1.5 Memory Map
Multiple power and clock domains	Independent domains for μP1, μP2, μP3, μP4, and memories L2 data retention enables CPU power-collapse Independently-scalable clocks for each core and L2

Qualcomm Snapdragon 600E Processor APQ8064E Device Specification, p.20 (available at https://developer.qualcomm.com/download/sd600/snapdragon-600-device-spec.pdf).

Low-power audio subsystem (LPASS)	
Power efficient audio processing	New QDSP6v4 core New SLIMbus interfaces ■ Approximately 24 Mbps of uncompressed audio data bandwidth ■ SLIMbus includes customized slew-rate limited IOs Support for up to 6 digital microphones
Low-power features	Power gating within LPASS core QDSP6 supports L2 cache data retention during power collapse Supported modes: ACTIVE / IDLE / DORMANT / OFF
Clock control	Local clock control with dedicated PLL
Low-power memory	Dedicated SRAM Bitstream buffer, PCM buffers, DSP OS
Musical Instrument Digital Interface (MIDI)	Acceleration HW 128-poly MIDI processing
Audio DSP	Near-zero cache miss-rates during steady-state low-power audio playback Separate voltage domain is scaled with performance requirements
Audio interfaces	PCM, DMIC, MI^{2}S/I^{2}S legacy low-power audio interfaces

Qualcomm Snapdragon 600E Processor APQ8064E Device Specification, p.21 (available at https://developer.qualcomm.com/download/sd600/snapdragon-600-device-spec.pdf).

32. The Accused Instrumentalities comprise "a clock generator." For example, the Qualcomm Snapdragon 600 Processor APQ8064 includes a clock generator as shown by the clock architecture diagram below, including the Krait mP Clock Block for the Krait cores and the Audio Clock Block for the LPASS core:

1.6.2.1 Clock architecture

Figure 1-3 illustrates the APQ8064E clock architecture. For details, see the *Qualcomm Snapdragon 600E (APQ8064E) Clock Plan*, LM80-P0598-15.

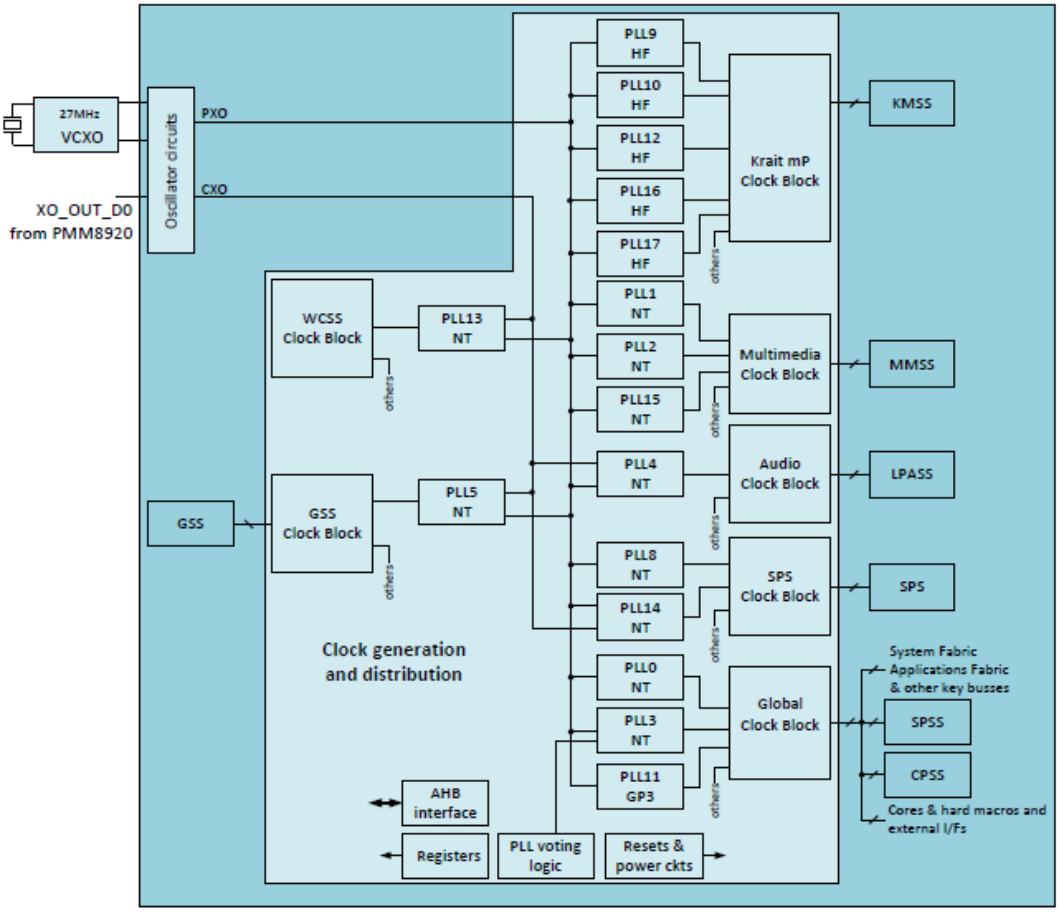


Figure 1-3 Clock architecture

Qualcomm Snapdragon 600E Processor APQ8064E Device Specification, p.26 (available at https://developer.qualcomm.com/download/sd600/snapdragon-600-device-spec.pdf).

3.12.1.1 LPASS clocks

- The LPASS PLL circuit is within the APQ's clock generation and distribution block.
- The LPASS clock controller (LCC) generates all the clocks needed for APQ audio functions, including the new SLIMbus and digital microphone interfaces.

3.12.1.1.1 Primary clock configuration

- The platform crystal oscillator (PXO, 27 MHz) is the reference source.
- The LPASS PLL output is routed to the LPASS, and selected as the LCC input signal.
- The LCC generates all audio clocks.
- Individual audio interfaces route the clocks to their functional blocks.
- Each interface allows an external clock source to be used and allows the generated clock to be routed externally.

Qualcomm Snapdragon 600E Processor APQ8064E Device Specification, p.113 (available at https://developer.qualcomm.com/download/sd600/snapdragon-600-device-spec.pdf).

33. In the Accused Instrumentalities, "the power supply control unit outputs a shutdown request signal to the CPU in response to an occurrence of a power shutdown factor." For example, in the Qualcomm Snapdragon 600 Processor APQ8064, the RPM initiates the entry into the low power mode including power collapse:

1.6.3 Power and sleep control

Four types of sleep modes reduce APQ leakage current:

1. Clock off
   - Clock sources (CXO and PXO) are turned off, but the core and memory power-supply voltages operate normally.
   - Upon wakeup, one of the interrupt sources is triggered, and then forwards the interrupt to other parts of the RPM system.
2. Core and memory supply voltages minimized
   - Up to four preprogrammed SSBI commands are sent to the PMIC to initiate the shutdown or wakeup process.
   - Core supply voltage is reduced first, and then the memory supply voltage.
   - Memory states and logic states are preserved.
   - Clocks are also turned off.
3. Core power-supply voltage collapsed and memory supply voltage minimized (but still on)
   - Pertinent comments from #2 apply, except the following:
     - Core voltage is collapsed, not just minimized.
     - Memory contents are retained, but logic states are lost.
4. Full IC power collapse (core and memory supply voltages collapsed)
   - Pertinent comments from #2 apply, except the following:
     - Both voltages are collapsed, not just minimized.
   - Lowest leakage current, but requires saving and restoring necessary states.
   - Software overhead and complexity are significant.

Qualcomm Snapdragon 600E Processor APQ8064E Device Specification, p.28 (available at https://developer.qualcomm.com/download/sd600/snapdragon-600-device-spec.pdf).

34. In the Accused Instrumentalities, "the CPU, upon receiving the shutdown request signal, executes a power shutdown microprogram, evacuates the information necessary in proceeding with the program to the information holding unit, and outputs an evacuation completed signal to the power supply control unit after evacuation is completed." For example, in the Qualcomm Snapdragon 600 Processor APQ8064, when the RPM outputs a shutdown request to initiate the shutdown process, the CPU (e.g., any of the four Krait cores and LPASS core) executes

a power shutdown microprogram and evacuates the information necessary in proceeding with the program to the information holding unit, including for sleep modes 3 and 4:

1.6.3 Power and sleep control

Four types of sleep modes reduce APQ leakage current:

1. Clock off
   - Clock sources (CXO and PXO) are turned off, but the core and memory power-supply voltages operate normally.
   - Upon wakeup, one of the interrupt sources is triggered, and then forwards the interrupt to other parts of the RPM system.
2. Core and memory supply voltages minimized
   - Up to four preprogrammed SSBI commands are sent to the PMIC to initiate the shutdown or wakeup process.
   - Core supply voltage is reduced first, and then the memory supply voltage.
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   - Pertinent comments from #2 apply, except the following:
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   - Lowest leakage current, but requires saving and restoring necessary states.
   - Software overhead and complexity are significant.

Qualcomm Snapdragon 600E Processor APQ8064E Device Specification, p.28 (available at https://developer.qualcomm.com/download/sd600/snapdragon-600-device-spec.pdf).

35. In the Accused Instrumentalities, "the power supply control unit, upon receiving the evacuation completed signal, outputs a power shutdown control signal to the power supply unit" and "the power supply unit shuts down power supply to the CPU upon receiving the power shutdown control signal from the power supply control unit." For example, in the Qualcomm Snapdragon 600 Processor APQ8064, on information and belief, the RPM/SPM confirms that the

memory states and logic have been preserved before instructing the power supply unit to enter a full IC power collapse:

1.6.3 Power and sleep control

Four types of sleep modes reduce APQ leakage current:

1. Clock off
   - Clock sources (CXO and PXO) are turned off, but the core and memory power-supply voltages operate normally.
   - Upon wakeup, one of the interrupt sources is triggered, and then forwards the interrupt to other parts of the RPM system.
2. Core and memory supply voltages minimized
   - Up to four preprogrammed SSBI commands are sent to the PMIC to initiate the shutdown or wakeup process.
   - Core supply voltage is reduced first, and then the memory supply voltage.
   - Memory states and logic states are preserved.
   - Clocks are also turned off.
3. Core power-supply voltage collapsed and memory supply voltage minimized (but still on)
   - Pertinent comments from #2 apply, except the following:
     - Core voltage is collapsed, not just minimized.
     - Memory contents are retained, but logic states are lost.
4. Full IC power collapse (core and memory supply voltages collapsed)
   - Pertinent comments from #2 apply, except the following:
     - Both voltages are collapsed, not just minimized.
   - Lowest leakage current, but requires saving and restoring necessary states.
   - Software overhead and complexity are significant.

Qualcomm Snapdragon 600E Processor APQ8064E Device Specification, p.28 (available at https://developer.qualcomm.com/download/sd600/snapdragon-600-device-spec.pdf).

36. In the Accused Instrumentalities, "the power supply control unit, upon receiving the evacuation completed signal, outputs a clock stop control signal to the clock generator." For example, in the Qualcomm Snapdragon 600 Processor APQ8064, at least in sleep modes 3 and 4, the RPM/SPM signals the clock to stop after completing evacuation:

1.6.3 Power and sleep control

Four types of sleep modes reduce APQ leakage current:

1. Clock off
   - Clock sources (CXO and PXO) are turned off, but the core and memory power-supply voltages operate normally.
   - Upon wakeup, one of the interrupt sources is triggered, and then forwards the interrupt to other parts of the RPM system.
2. Core and memory supply voltages minimized
   - Up to four preprogrammed SSBI commands are sent to the PMIC to initiate the shutdown or wakeup process.
   - Core supply voltage is reduced first, and then the memory supply voltage.
   - Memory states and logic states are preserved.
   - Clocks are also turned off.
3. Core power-supply voltage collapsed and memory supply voltage minimized (but still on)
   - Pertinent comments from #2 apply, except the following:
     - Core voltage is collapsed, not just minimized.
     - Memory contents are retained, but logic states are lost.
4. Full IC power collapse (core and memory supply voltages collapsed)
   - Pertinent comments from #2 apply, except the following:
     - Both voltages are collapsed, not just minimized.
   - Lowest leakage current, but requires saving and restoring necessary states.
   - Software overhead and complexity are significant.

Qualcomm Snapdragon 600E Processor APQ8064E Device Specification, p.28 (available at https://developer.qualcomm.com/download/sd600/snapdragon-600-device-spec.pdf).

37. In the Accused Instrumentalities, "the power supply control unit outputs a power supply control signal to the power supply unit in response to an occurrence of a power supply restoration factor." For example, in the Qualcomm Snapdragon 600 Processor APQ8064, the RPM outputs a wakeup request to initiate the wakeup process, it communicates with the PMIC and internal power switches via the SPM, including for sleep modes 3 and 4:

1.6.3 Power and sleep control

Four types of sleep modes reduce APQ leakage current:

1. Clock off
   - Clock sources (CXO and PXO) are turned off, but the core and memory power-supply voltages operate normally.
   - Upon wakeup, one of the interrupt sources is triggered, and then forwards the interrupt to other parts of the RPM system.
2. Core and memory supply voltages minimized
   - Up to four preprogrammed SSBI commands are sent to the PMIC to initiate the shutdown or wakeup process.
   - Core supply voltage is reduced first, and then the memory supply voltage.
   - Memory states and logic states are preserved.
   - Clocks are also turned off.
3. Core power-supply voltage collapsed and memory supply voltage minimized (but still on)
   - Pertinent comments from #2 apply, except the following:
     - Core voltage is collapsed, not just minimized.
     - Memory contents are retained, but logic states are lost.
4. Full IC power collapse (core and memory supply voltages collapsed)
   - Pertinent comments from #2 apply, except the following:
     - Both voltages are collapsed, not just minimized.
   - Lowest leakage current, but requires saving and restoring necessary states.
   - Software overhead and complexity are significant.

Qualcomm Snapdragon 600E Processor APQ8064E Device Specification, p.28 (available at https://developer.qualcomm.com/download/sd600/snapdragon-600-device-spec.pdf).

38. In the Accused Instrumentalities, "the power supply unit, upon receiving the power supply control signal, starts to supply power to the CPU." For example, in the Qualcomm Snapdragon 600 Processor APQ8064, on information and belief, the power supply unit starts to supply power to the CPU at the start of the wakeup process.

39. The Accused Instrumentalities comprise a clock generator wherein "the power supply unit, upon receiving the power supply control signal, starts to supply power to the CPU," "the power supply control unit outputs a restoration request signal to the CPU and outputs a clock

supply control signal to the clock generator when a supplied power supply voltage is stabilized," and "the clock generator, upon receiving the clock supply control signal, restarts to supply an operation clock." For example, in the Qualcomm Snapdragon 600 Processor APQ8064, on information and belief, the power supply unit starts to supply power to the CPU at the start of the wakeup process, the RPM/SPM signals the clock to turn on when the voltage is stabilized, and the clock generator, upon receiving the clock supply control signal, restarts to supply an operation clock:

1.6.3 Power and sleep control

Four types of sleep modes reduce APQ leakage current:

1. Clock off
   - Clock sources (CXO and PXO) are turned off, but the core and memory power-supply voltages operate normally.
   - Upon wakeup, one of the interrupt sources is triggered, and then forwards the interrupt to other parts of the RPM system.
2. Core and memory supply voltages minimized
   - Up to four preprogrammed SSBI commands are sent to the PMIC to initiate the shutdown or wakeup process.
   - Core supply voltage is reduced first, and then the memory supply voltage.
   - Memory states and logic states are preserved.
   - Clocks are also turned off.
3. Core power-supply voltage collapsed and memory supply voltage minimized (but still on)
   - Pertinent comments from #2 apply, except the following:
     - Core voltage is collapsed, not just minimized.
     - Memory contents are retained, but logic states are lost.
4. Full IC power collapse (core and memory supply voltages collapsed)
   - Pertinent comments from #2 apply, except the following:
     - Both voltages are collapsed, not just minimized.
   - Lowest leakage current, but requires saving and restoring necessary states.
   - Software overhead and complexity are significant.

Qualcomm Snapdragon 600E Processor APQ8064E Device Specification, p.28 (available at https://developer.qualcomm.com/download/sd600/snapdragon-600-device-spec.pdf).

40. In the Accused Instrumentalities, "the CPU, upon receiving the restoration request signal, executes a power supply restoration microprogram, restores the information necessary in proceeding with the program and evacuated in the information holding unit in time of power shutdown, and then branches a process to an address indicated by a program counter to continue program execution from a shutdown state." For example, in the Qualcomm Snapdragon 600 Processor APQ8064, the preservation of memory and logic states during shutdown demonstrates the presence of a restoration microprogram.

Indirect Infringement (Inducement – 35 U.S.C. § 271(b))

41. In addition and/or in the alternative to its direct infringements, Qualcomm has indirectly infringed, and continues to indirectly infringe, one or more claims of the '575 patent by knowingly and intentionally inducing others, including its subsidiaries, affiliates, distributors, agents, partners, retailers, suppliers, integrators, importers, customers, and/or consumers, to directly infringe by making, using, offering to sell, selling and/or importing into the United States the Accused Instrumentalities.

42. At a minimum, Qualcomm has knowledge of the '575 patent since being served with this Complaint. Qualcomm also has knowledge of the '575 patent since receiving Collabo's letter providing details of Qualcomm's infringements prior to the filing of this Complaint. Since receiving notice of its infringements, Qualcomm has actively induced the direct infringements of its subsidiaries, affiliates, distributors, agents, partners, retailers, suppliers, integrators, importers, customers, and/or consumers as set forth under U.S.C. § 271(b). Such inducements have been committed with the knowledge, or with willful blindness to the fact, that the acts induced constitute infringement of the '575 patent. Indeed, Qualcomm has intended to cause, continues to intend to cause, and has taken, and continues to take, affirmative steps to induce infringement by, among other things, creating and disseminating advertisements and instructive materials that promote the

infringing use of the Accused Instrumentalities;[6] creating and/or maintaining established distribution channels for the Accused Instrumentalities into and within the United States; manufacturing the Accused Instrumentalities in conformity with U.S. laws and regulations; distributing or making available product briefs and device specifications supporting use of the Accused Instrumentalities that promote their features, specifications, and applications;[7] promoting the incorporation of the Accused Instrumentalities into end-user products,[8] and providing technical support and/or related services for these products to purchasers in the United States.

Damages

43. Collabo has been damaged as a result of Qualcomm's infringing conduct described in this Count. Qualcomm is, thus, liable to Collabo in an amount that adequately compensates Collabo for Qualcomm's infringements, which, by law, cannot be less than a reasonable royalty, together with interest and costs as fixed by this Court under 35 U.S.C. § 284.

44. On information and belief, despite having knowledge of the '575 patent and knowledge that it is directly and/or indirectly infringing one or more claims of the '575 patent, Qualcomm has nevertheless continued its infringing conduct and disregarded an objectively high likelihood of infringement. Qualcomm's infringing activities relative to the '575 patent have been, and continue to be, willful, wanton, malicious, in bad-faith, deliberate, and consciously wrongful, thus comprising an egregious case of misconduct beyond typical infringement, such that Collabo is entitled to enhanced damages under 35 U.S.C. § 284 up to three times the amount found or assessed.

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[6] *See, e.g.*, https://www.qualcomm.com/news/releases/2011/11/qualcomm-unveils-new-snapdragon-mobile-processors-across-all-tiers; https://www.qualcomm.com/news/releases/2011./02/qualcomm-announces-next-generation-snapdragon-mobile-chipset-family

[7] *See, e.g.*, https://www.qualcomm.com/products/technology/processors/s4-s1; https://developer.qualcomm.com/download/sd600/snapdragon-600-device-spec.pdf

[8] *See* https://www.qualcomm.com/snapdragon/overview

CONCLUSION

45. Collabo is entitled to recover from Qualcomm the damages it has sustained as a consequence of Qualcomm's wrongful acts and willful infringements, in an amount subject to proof at trial, which, by law, cannot be less than a reasonable royalty, together with interest and costs as fixed by this Court.

46. Collabo has incurred, and will incur, attorneys' fees, costs, and expenses in the prosecution of this action. The circumstances of this dispute may give rise to an exceptional case within the meaning of 35 U.S.C. § 285, and Collabo is entitled to recover its reasonable and necessary attorneys' fees, costs, and expenses.

JURY DEMAND

47. Collabo hereby requests a trial by jury pursuant to Rule 38 of the Federal Rules of Civil Procedure.

PRAYER FOR RELIEF

Collabo respectfully requests that the Court find in its favor and against Qualcomm, and that the Court grant Collabo the following relief:

(i) A judgment that one or more claims of the Asserted Patent have been infringed, directly and/or indirectly, either literally and/or under the doctrine of equivalents, by Qualcomm;

(ii) A judgment that one or more claims of the Asserted Patents have been willfully infringed, either literally and/or under the doctrine of equivalents, by Qualcomm;

(iii) A judgment that Qualcomm account for and pay to Collabo all damages and costs incurred by Collabo because of Qualcomm's infringing activities and other conduct

complained of herein, including an accounting for any sales or damages not presented at trial;

(iv) A judgment that Qualcomm account for and pay to Collabo a reasonable, ongoing, post-judgment royalty because of Qualcomm's infringing activities, including continuing infringing activities, and other conduct complained of herein;

(v) A judgment that Collabo be granted pre-judgment and post-judgment interest on the damages caused by Qualcomm's infringing activities and other conduct complained of herein;

(vi) A judgment that this case is exceptional under the provisions of 35 U.S.C. § 285 and award enhanced damages; and

(vii) Such other and further relief as the Court deems just and equitable.

Dated: September 13, 2024

Respectfully submitted,

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