

A 200-mW, 3.3-V, CMOS Color Camera IC Producing 352×288 24-b Video at 30 Frames/s

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Abstract—A digital color camera has been monolithically realized in a standard 0.8- μm CMOS technology. The chip integrates a 354×292 photogate sensor array with a unity-gain column circuit, a hierarchical column multiplexer, a switched-capacitor programmable-gain amplifier, and an 8-b flash analog/digital converter together with digital circuits performing color interpolation, color correction, computation of image statistics, and control functions. The 105-mm² chip produces 24-b RGB video at 30 frames/s. The sensor array achieves a conversion gain of 40 $\mu\text{V}/\text{electron}$ and a monochrome sensitivity of 7 V/lux-s. For a 33-ms exposure time, the camera chip achieves a dynamic range of 65 dB and peak-to-peak fixed pattern noise that is 0.3% of saturation. Digital switching noise coupling into the analog circuits is shown to be data independent and therefore has no effect on image quality. Total power dissipation is less than 200 mW from a 3.3-V supply.

Index Terms—Active pixel sensors, cameras, CMOS image sensors, image sensors, mixed analog-digital integrated circuits, video cameras.

I. INTRODUCTION

DURING this decade, advances in CMOS imaging technology [1]–[4] have enabled the creation of single-chip digital cameras [5], [6]. Such devices offer camera system designers the benefits of reduced part counts, fully digital I/O interfaces, and low power dissipation. The ability to build an imager with customized on-chip signal-processing and control functions is another important advantage of this technology. These benefits, if fully realized, will lower digital-camera manufacturing costs, shorten product development cycles, and lead to ubiquitous, compact, mobile cameras for real-time communication, scientific, industrial, and security applications.

Fig. 1 shows a block diagram for a PC-based digital-camera system utilizing a single-chip camera. The chip produces digital video data that are delivered to the host over a digital interface. On the camera chip is an imager that feeds into a programmable-gain amplifier (PGA) that is used for gain control and white balancing. The PGA drives an analog/digital (A/D) converter that allows all subsequent color processing to be performed digitally. Digital processing consists of color interpolation, color correction, and image statistics computation for the measurement of exposure level and white balance.

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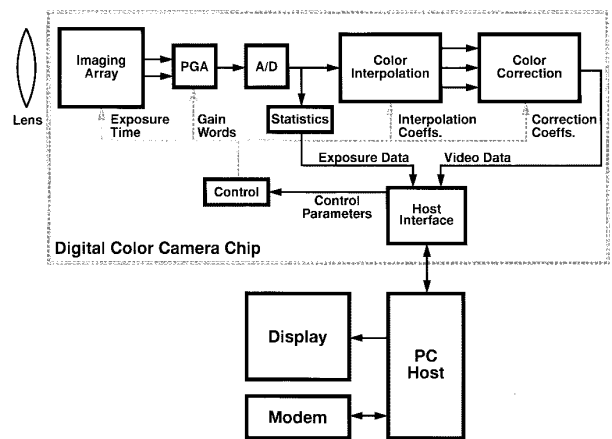


Fig. 1. Multimedia camera system block diagram.

The host has the ability to adjust the operation of the camera by setting its frame rate, exposure time, analog gains, and color-processing coefficients. The system is partitioned so that frame-rate processing, such as automatic exposure control and white balance algorithms, are implemented in software running on the host. On the other hand, pixel-rate tasks requiring intensive computation, i.e., color interpolation and color correction, are performed in hardware on the camera chip.

Over the last several years, researchers have demonstrated CMOS imaging arrays [7]–[9] with performance approaching that of charge-coupled-device (CCD)-based imagers for desktop and multimedia applications [11], [12]. A quantitative study of CMOS photogate sensors [10] shows that these devices can perform as well as CCD imagers in terms of sensitivity if quantum efficiency can be increased and dark current reduced. Techniques for doing this with only minor modifications to a standard CMOS process have been reported [13]. It is these authors' opinion that improvements in CMOS image sensor technology via incremental process modifications and innovative circuit techniques will enable CMOS imagers to steadily close the performance gap with CCD-based sensors over the next several years.

One goal of this paper is to demonstrate the feasibility of integrating a single-chip camera with the architecture shown in Fig. 1. Specifically, the effects of switching noise coupling from the digital signal-processing circuits into the analog signal chain must be shown to be manageable. While CCD

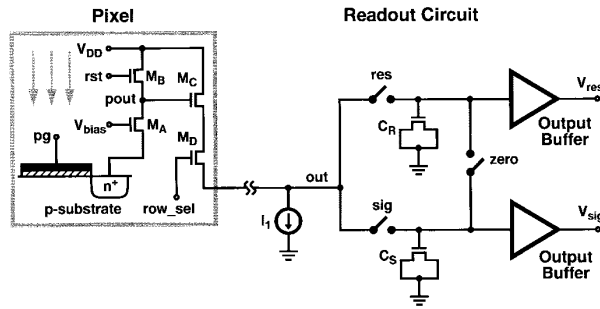


Fig. 2. CMOS photogate sensor and basic readout circuit.

technology has traditionally been the province of the device designer and process-integration engineer, CMOS imaging technology has placed imager design also within the domain of the integrated-circuit (IC) designer. Another goal of this paper is to bring the wealth of analog and digital IC design techniques to bear on the optimization of CMOS imagers for low read noise, low fixed-pattern noise (FPN), and low power dissipation.

This paper describes the design and testing of a single-chip digital color camera. In Section II, the operation and performance of the photogate image sensor used in the prototype are presented, and the circuits used to read out the sensor array are described. Additionally, the design of the programmable-gain amplifier and A/D converter are outlined. In Section III, the digital color-processing blocks are described. Experimental results for the prototype chip are presented in Section IV, along with a discussion of the effects of switching noise coupled from the digital blocks into the analog signal chain.

II. ANALOG SIGNAL CHAIN

A. Sensor and Column Circuit

Fig. 2 shows the schematic of a photogate pixel circuit and a basic readout circuit [7], [8]. During photocurrent integration, the *pg* terminal is held high and generated electrons are stored in the potential well underneath the photogate. When a pixel row is selected for readout (*row_sel* high), the *rst* line for that row is pulsed high to reset the voltage at node *pout*. The *res* line is then pulsed, and the reset *out* voltage is stored on capacitor C_R . The *pg* signal is then pulsed low, transferring the photogenerated charge onto the parasitic capacitance at node *pout*. The *sig* line is then pulsed, and the integrated signal value is stored on C_S . The difference between V_{res} and V_{sig} represents the pixel output corrected for reset noise produced by M_B and FPN due to static pixel-to-pixel variations in M_B , M_C , and M_D . When the *zero* signal goes high, the inputs of the two output buffers are connected so that the difference between the random offset voltages of the two buffers can be measured and subsequently subtracted from $V_{res} - V_{sig}$ so as to eliminate column FPN [7].

The pixel circuit as implemented on the prototype chip has a cell area of $18 \times 18 \mu\text{m}$. A pixel circuit fabricated in the same technology but with an optically reduced area of $16 \times 16 \mu\text{m}$ was characterized and the results presented in [10].

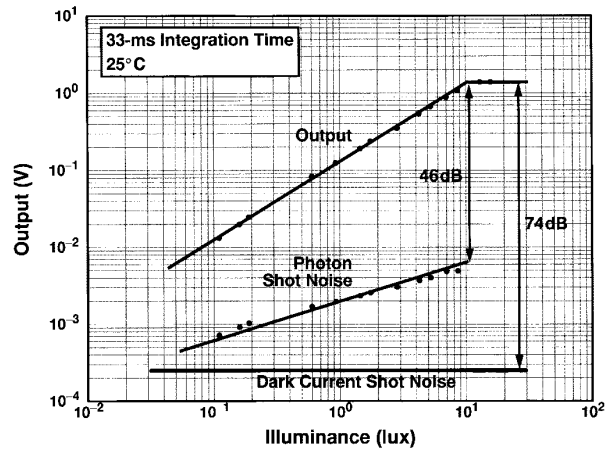


Fig. 3. CMOS photogate sensor sensitivity.

Sensitivity and quantum-efficiency measurements illustrate the performance limitations of this photogate pixel and drive the performance requirements for the analog signal chain. The sensitivity of the $16 \times 16 \mu\text{m}$ pixel circuit is plotted in Fig. 3. Maximum signal-to-noise ratio is limited to 46 dB by photon shot noise, and the sensor dynamic range is limited to 74 dB by dark current shot noise and not by read noise.

The read noise stored on C_R and C_S in Fig. 2 is primarily due to thermal noise in device M_C and is approximated by

$$\sigma_{V_R-V_S} \approx \sqrt{\frac{4}{3} kT \left(\frac{g_{mC}}{g_{mbC} + g_{mC} \cdot (1-k)} \cdot \frac{1}{C_R} \right)} \quad (1)$$

where g_{mC} is the transconductance of M_C and g_{mbC} is its body effect transconductance. The parameter k is given by

$$k = \frac{C_{gsC}}{C_{gsC} + C_{gdC} + C_{fd}} \quad (2)$$

where C_{gsC} and C_{gdC} are the gate-to-source and gate-to-drain capacitances of M_C , respectively, and C_{fd} is the parasitic capacitance to ac ground at node *pout* in Fig. 2. In deriving (1), it has been assumed that $C_R = C_S$ and that the “on” resistance of M_D is negligible. The thermal noise produced by the output buffers in Fig. 2 will be much lower than that produced by M_C because the capacitive loads driven by these circuits are typically much larger than C_R and C_S . It is important to note that the readout circuit shown in Fig. 2 can be designed so that read noise is lower than dark current shot noise by setting large enough values for capacitors C_R and C_S . For the experimental results presented in [10], the use of $C_R = C_S = 1 \text{ pF}$ results in read noise that is 4 dB lower than dark current shot noise.

Sensor quantum efficiency is plotted as a function of light wavelength in Fig. 4 [10]. For short wavelengths, the monochrome quantum efficiency is low, substantially lower than that of a frame-transfer CCD [14], because of absorption in the relatively thick polysilicon layer that forms the photogate. At long wavelengths, quantum efficiency drops off because

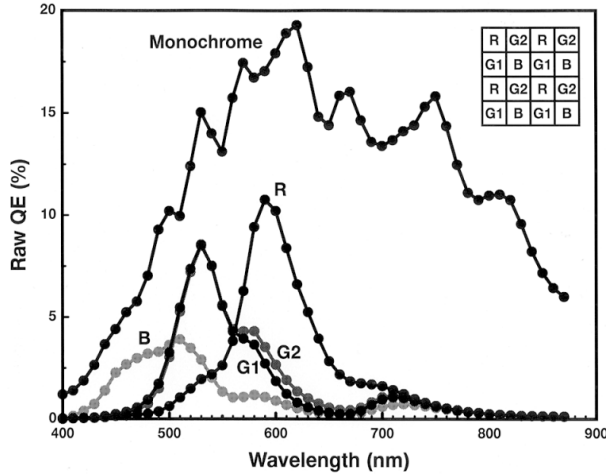


Fig. 4. CMOS photogate sensor quantum efficiency.

incoming photons are not energetic enough to create electron-hole pairs. Also shown in Fig. 4 are the quantum efficiencies of pixels covered by red, green, and blue (RGB) color filters. These measurements were taken with the use of a color-compensating filter that attenuates the near infrared response of the sensor. To achieve white balance, it is evident from Fig. 4 that the outputs of the blue and green pixels must be amplified with respect to the outputs of the red pixels.

The use of a source follower made up of M_C , M_D , and I_1 in Fig. 2 results in a gain from the *pout* node to the *out* node given by (neglecting the “on” resistance of triode device M_D)

$$A_{pout-out} = \frac{g_{mC}}{g_{mC} + g_{mbC} + g_{oC}} \quad (3)$$

where g_{oC} is the output conductance of device M_C . Circuit simulations show that source-follower gain is nominally 0.8. If source followers are also used for the output buffers in Fig. 2, the resulting gain from the *pout* node to the V_{res} and V_{sig} terminals may be as low as 0.64. Source follower attenuation therefore reduces the effective conversion gain of the sensor array.

Rather than using source-follower-based readout circuits, the prototype chip employs a unity-gain amplifier for pixel readout, as shown in Fig. 5. The 354 column circuits are positioned at the bottom of the sensor array with one column circuit for each 292-pixel column. The voltage at *pout* is read out by the distributed amplifier made up of devices M_C , M_D , M_1 , and M_2 along with current sources I_1 and I_2 . M_C and M_1 form a differential pair with triode devices M_D and M_2 acting as degeneration resistors. These four transistors and the two current sources comprise an operational transconductance amplifier (OTA) that is connected in unity-gain feedback so that the *col_out* signal is a buffered version of *pout*. The gain from the *pout* node to the *col_out* node is given by

$$\begin{aligned} A_{pout-col_out} &= \frac{g_{mC}}{g_{mC} + g_{mbC} + g_{oC}} \cdot \frac{g_{m1} + g_{mb1} + g_{o1}}{g_{m1} + g_{o1}} \\ &\approx \frac{g_{mC}}{g_{mC} + g_{oC}} \end{aligned} \quad (4)$$

again neglecting the “on” resistance of triode devices M_D and M_2 and assuming that devices M_C and M_1 are identical. This gain has a nominal simulated value of 0.96. In Fig. 5, the output buffers used to drive V_{res} and V_{sig} are also implemented using single-stage OTA’s in unity-gain feedback, as shown in Fig. 6. The column output buffers are powered up only when the column-select signal *col_sel* is high. It should be noted that because g_m is typically much greater than g_o , (4) indicates that excellent gain uniformity will be achieved even as g_m , g_o , and g_{mb} values vary from pixel to pixel and from column to column.

The use of feedback OTA’s in the pixel and column readout results in a 40–50% gain improvement relative to previously proposed source-follower-based circuits [7], [8] while achieving good gain uniformity and linearity. This results in higher imager conversion gain. However, the improvement in conversion gain comes at the price of increased read noise because there are more transistors in the signal path. Simulations show a 1–2-dB increase in read noise with the use of the circuit in Fig. 5 and $C_R = C_S = 1$ pF. The simulated value for imager read noise is 130 mV rms, 78 dB below the output buffer saturation level of 1 V. This value is still lower than the dark current shot noise shown in Fig. 3.

In Fig. 5, $I_2 = 15$ μ A, and the power dissipation associated with 354 such circuits operating in parallel is 18 mW. The dc current flowing in each of the output buffer OTA’s is 300 μ A. Because only two column output buffers are active at any given time, power dissipation in the column output buffers is only 2 mW. The total power dissipation in the imager is therefore 20 mW at a pixel readout rate of 3 MHz, corresponding to 30 frames/s.

B. Column Multiplexer

Previous imager designs (e.g., [8]) have employed decoder-based column multiplexers, as shown in Fig. 7(a). All corresponding column buffer outputs are connected together with buses running the entire length of the array so that a uniform load capacitance is seen by each output buffer, resulting in low column FPN. The result is that each column circuit has to drive the output capacitance associated with 353 other column circuits. This translates to an effective load capacitance of tens of picofarads as seen by each column buffer. It is possible to reduce this effective load capacitance by employing hierarchical multiplexing techniques, as are used in column tree decoders for random-access memories [15].

In this work, a hierarchical multiplexer, shown in Fig. 7(b), is used to reduce the capacitive load seen by each column output buffer. Each output buffer has to drive only the output capacitance of seven other output buffers within its block of eight plus the parasitics associated with two “on” switches and 12 “off” switches along with associated interconnect capacitance. While the multiplexing circuit shown in Fig. 7(b) may result in capacitive load variations for different columns because each block of eight columns has a different physical output path, the column buffers are designed for 0.1% setting. As a result, the use of hierarchical readout results in no detectable degradation in column FPN (even at the transition

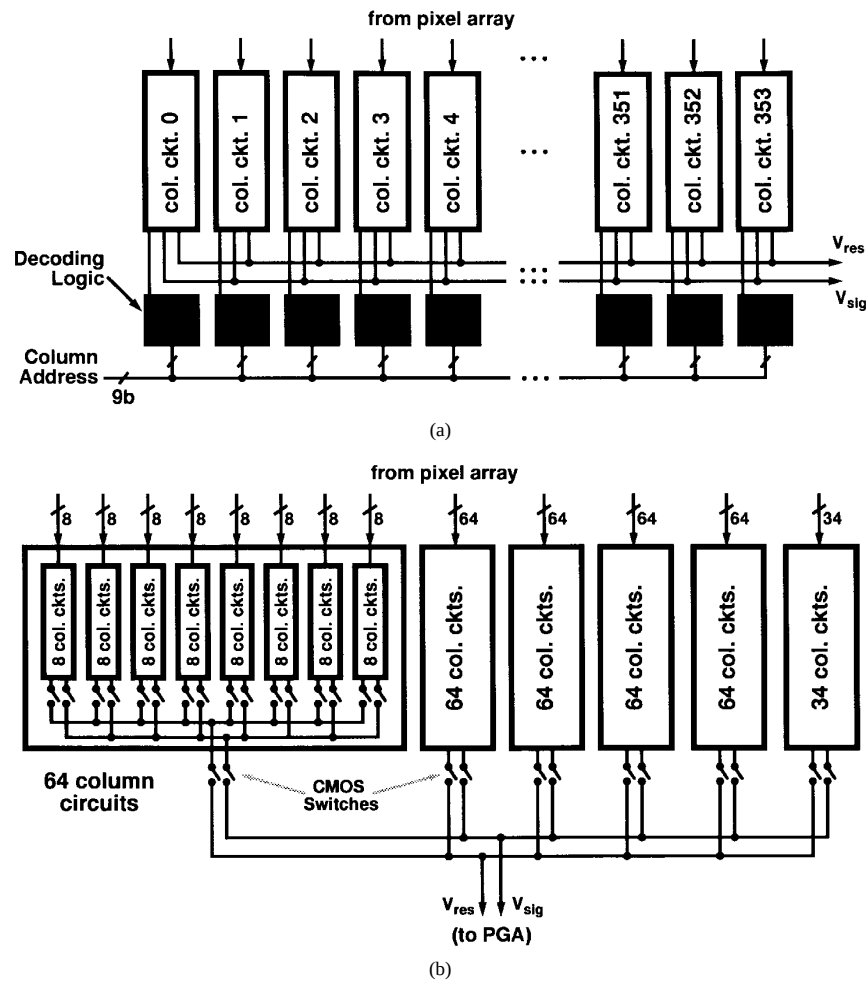


Fig. 7. (a) Conventional column multiplexer and (b) hierarchical column multiplexer used in prototype.

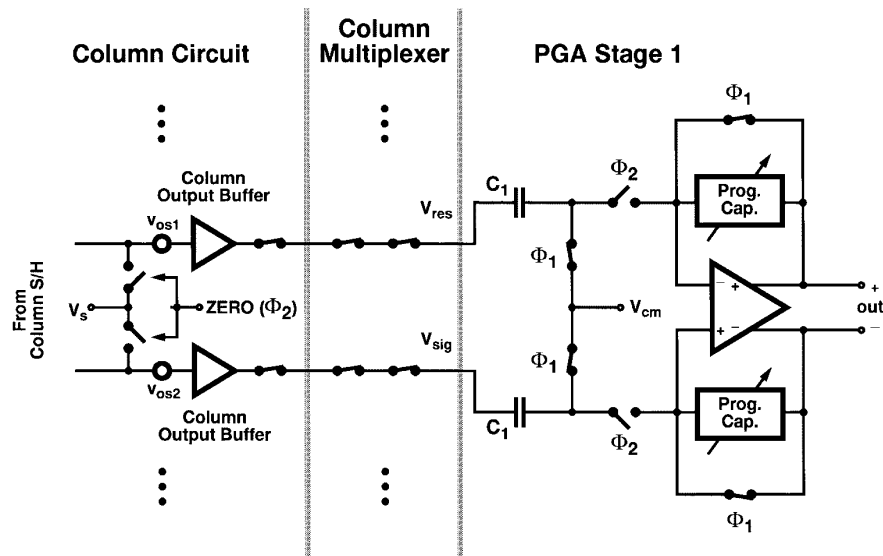


Fig. 8. Interface among column circuits, multiplexer, and PGA.

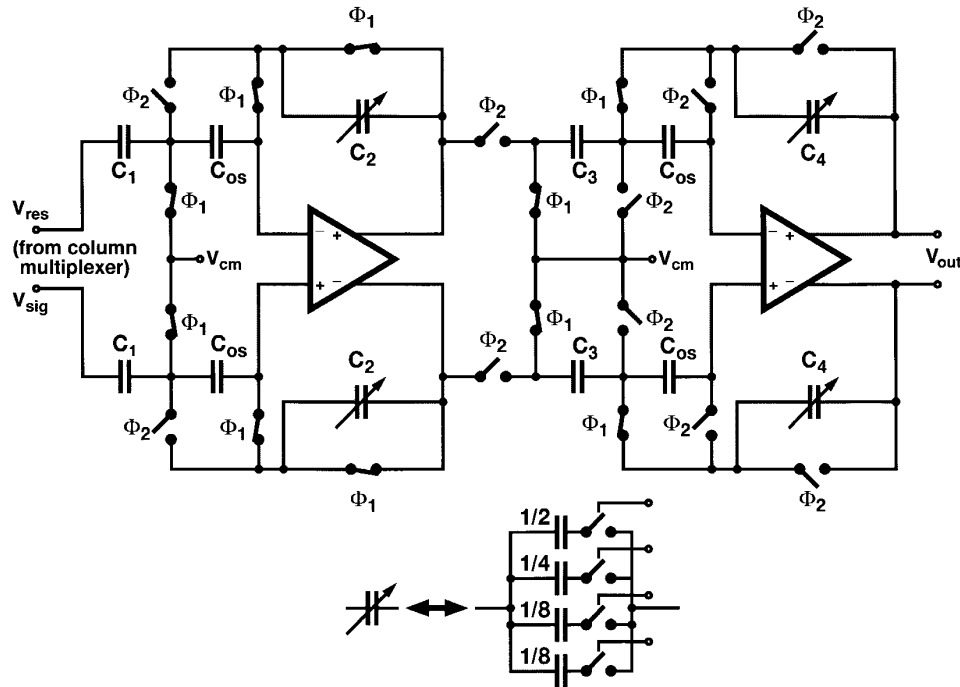


Fig. 9. PGA implementation.

D. A/D Converter

The 8-b full-flash A/D employs 256 single-ended comparators with a total input capacitance of 13 pF. As is typical in video applications, blanking or synchronization intervals are inserted between successive lines and frames during readout. Self-calibration can therefore be performed by the A/D during these “dead” times. Each comparator in the converter is offset-calibrated over ten pixel clock periods during the horizontal blanking interval between lines. Calibration voltages are stored within each comparator block on large-valued MOS capacitors so that diode leakage and photocurrents do not compromise A/D performance. While it is likely that a pipeline A/D, rather than a flash architecture, would result in the lowest possible converter power dissipation in this application, the aforementioned blanking period calibration has allowed the flash converter to be optimized so that power dissipation is under 40 mW at 3 MSamples/s.

E. Color Filter Array (CFA)

The primary Bayer checkerboard CFA pattern [17] shown below was selected for the prototype

$$\begin{array}{ccccccc} R & G & R & G & \dots \\ G & B & G & B & \dots \\ R & G & R & G & \dots \\ G & B & G & B & \dots \\ \dots & & & & \end{array}$$

The checkerboard pattern provides superior horizontal resolution compared to stripe CFA patterns at the expense of diagonal resolution where the acuity of the eye is poor [18]. A CFA

based on primary colors was used rather than one based on complementary colors so as to simplify the subsequent stages of digital color processing.

III. DIGITAL PROCESSING

A. Color Interpolation

The use of a CFA necessitates the use of spatial interpolation to construct three color components (R_{int} , G_{int} , and B_{int}) for each pixel, since each pixel is covered by only one type of filter. For ease of implementation, an elementary linear interpolation over a 3×3 pixel neighborhood is used. To support common intermediate form (CIF) resolution of 352×288 pixels, the imaging array includes two extra rows and two extra columns to simplify interpolation at the image boundaries. A further two rows serve as dark level references. A block diagram of the interpolation subsystem is shown in Fig. 10. The pixels in the current interpolation neighborhood are held in a 3×3 register file, and a pair of first-in, first-out buffers (FIFO's) is used to store the previous two lines. The FIFO's are implemented using a 352×2 byte SRAM and an address generator. Three multiply-and-accumulate (MAC) units running in parallel perform the convolution of the pixel data in the 3×3 register file with the coefficients of the interpolation filters. Each MAC unit comprises a multiplier, an accumulator, a normalization stage, and a coefficient store. The nine interpolation coefficients for each color are programmable and represented using a 6-b signed fractional mantissa and a 4-b exponent. To simplify the MAC implementation, one exponent is common for all nine coefficients for each color.

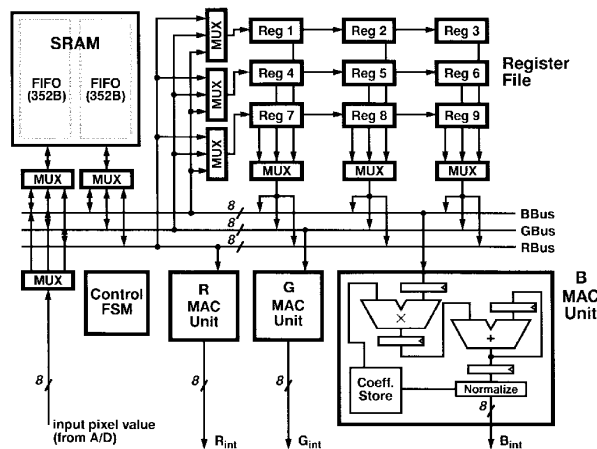


Fig. 10. Color interpolation unit.

The control finite-state machine is responsible for directing all the pixels of a given color from the register file into the corresponding MAC unit. As each pixel value is loaded into a MAC, the appropriate coefficient is fetched from the store according to to which register the pixel value corresponds. After multiplication, the product is accumulated by the adder. The result is then normalized by a shift to the right determined by the exponent magnitude. The final output from the MAC unit is truncated to 8 b. In total, the interpolation subsystem performs nine multiplies and at most six accumulations per pixel clock cycle.

The digital color-processing circuits are controlled by a 27-MHz master clock that is taken from off-chip. From this master clock, the 3-MHz pixel clock is derived. While nine clock cycles are available for digital processing within each pixel cycle, only six are used due to the switching noise management strategy, as will be discussed in Section III-E. The operation of the interpolation subsystem in Fig. 10 can be illustrated using as an example an input pixel value from the A/D corresponding to a red pixel. During the first digital clock cycle, the contents of the 3×3 register file are shifted to the right by one register, i.e., register 1 $\rightarrow$ register 2, register 2 $\rightarrow$ register 3, register 4 $\rightarrow$ register 5, register 5 $\rightarrow$ register 6, register 7 $\rightarrow$ register 8, and register 8 $\rightarrow$ register 9. The previous contents of registers 3, 6, and 9 are discarded. The current pixel value from the A/D (a red pixel in this example) is loaded into register 1 and into the R MAC via the RBus. During the second and third digital clock cycles, the pixel values from the previous two rows are removed from FIFO 1 and FIFO 2 and loaded into registers 4 and 7 and into the G and R MAC units via the GBus and RBus. Two clock cycles are needed to extract data from the FIFO's because the SRAM read is pipelined. During the fourth digital clock cycle, the pixel values in registers 3 and 6 are inserted into FIFO 1 and FIFO 2, respectively, and the R and G MAC units. During the fifth digital clock cycle, the pixel values in Registers 5, 8, and 9 are loaded into the B, G, and R MAC units, respectively. In the sixth digital clock cycle, the contents of Register 2 are loaded into the G MAC unit. Data flow is analogous for green and blue pixels.

B. Color Correction

To improve the color rendition of solid-state imagers, it is necessary to apply a 3×3 matrix transformation to the interpolated color component values for each pixel [19]. The color-correction subsystem takes the interpolated colors for each pixel (R_{int} , G_{int} , B_{int}) and converts them into the output (R_0 , G_0 , B_0) using

$$\begin{bmatrix} R_0 \\ G_0 \\ B_0 \end{bmatrix} = \begin{bmatrix} c_{11} & c_{12} & c_{13} \\ c_{21} & c_{22} & c_{23} \\ c_{31} & c_{32} & c_{33} \end{bmatrix} \times \begin{bmatrix} R_{int} \\ G_{int} \\ B_{int} \end{bmatrix} + \begin{bmatrix} r_{offset} \\ g_{offset} \\ b_{offset} \end{bmatrix}. \quad (5)$$

The values of the coefficients and offsets are chosen to minimize the mean colorimetric error for a test set of color samples and to transform to the color space of the display primaries (e.g., NTSC). Colorimetric simulations were used to determine the precision with which the matrix coefficients and offsets were represented. The matrix coefficients are programmable and have a 6-b signed fractional mantissa and an individual 2-b exponent. The offsets are each signed 8-b quantities.

A block diagram of the color-correction subsystem is shown in Fig. 11. It includes a coefficient store and three MAC units running in parallel. Inside each MAC unit, pixel components are multiplied in turn by the mantissa of the three matrix coefficients of the appropriate row of the matrix, with each result being normalized by the exponent of the coefficient. These products are accumulated with the corresponding offset, and the final result is truncated to 8 b. The color-correction subsystem performs nine multiplications and 12 accumulations for each pixel.

C. Computation of Image Statistics

To facilitate automatic exposure control and white balance via host software, the camera IC computes image statistics in the form of histograms for the red, green, and blue pixels in each frame. The histograms each have four bins defined by five programmable thresholds. Each bin is implemented using a counter. At the start of each frame, the histogram bins are cleared. During sensor readout, each pixel value from the A/D is compared with the five thresholds, and the corresponding histogram bin is incremented. At the end of each frame, the host is able to read the histogram counters.

D. Host Interface

The host interface consists of a set of 80 read-write registers on the camera chip that are accessed using a low-speed transceiver board on a PC. All on-chip parameters are double buffered to eliminate glitches. The 24-bit video data are acquired by the PC with a digital frame grabber that allows the image data to be displayed at 30 frames/s. Gamma correction is performed in an 8-bit hardware lookup table on the frame grabber.

E. Switching Noise Management

In mixed-signal IC's, it has been shown that switching transients produced by the digital logic can couple into sensi-

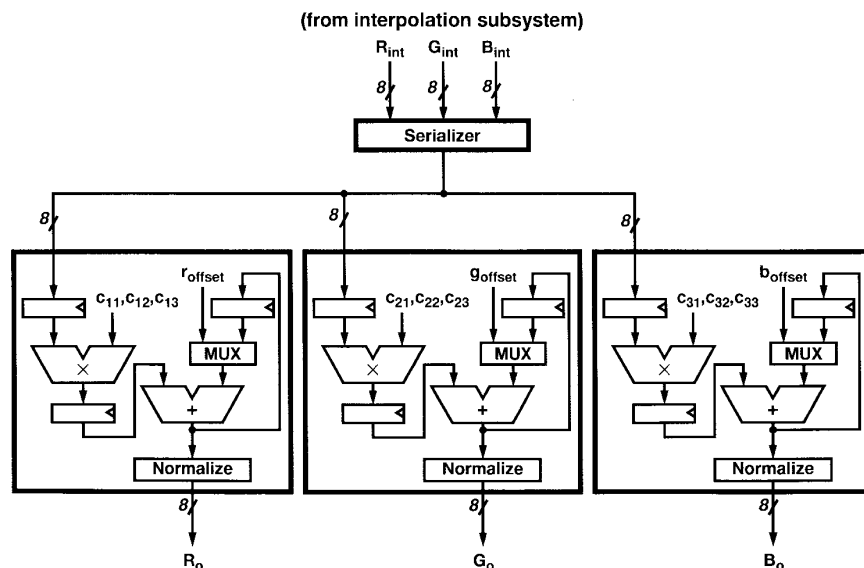


Fig. 11. Color-correction unit.

tive analog components via the die substrate and IC package [20]. This coupling may limit the analog precision that can be achieved. However, the impact of switching noise can be reduced by ensuring that digital switching does not coincide with sensitive analog operations [21]. The switching-noise management strategy employed in the prototype was to freeze the operation of the digital circuits when single-ended analog operations are being performed. As previously described, the camera IC takes a 27-MHz master clock, from which the 3-MHz pixel clock and digital circuit clock are derived. The digital clock is suppressed entirely during the horizontal blanking intervals when the pixels in a selected row are read by the column circuits and the A/D is calibrated. Furthermore, the digital clock is gated such that only six of the nine possible cycles per pixel clock are presented to the digital subsystems. One of the three remaining external clock cycles is used to clock the A/D while no digital computation is being performed. To assess the effectiveness of the switching-noise management strategy, it is possible to program the chip to run in a “noisy” mode in which the digital processing circuits are operating while the single-ended comparators in the A/D are being latched.

IV. EXPERIMENTAL RESULTS

A. Circuit Performance

The prototype chip incorporates all the elements of the digital color camera block diagram shown in Fig. 1. The chip has 740 000 transistors and was fabricated in a 0.8- μm single-poly, double-metal CMOS process. Deposition of a polyimide CFA was performed after standard CMOS processing. A die micrograph taken before CFA processing is shown in Fig. 12. The chip takes a 27-MHz clock and produces 352×288 24-b RGB data that is driven off-chip at the pixel clock rate of 3 MHz, which corresponds to 30 frames/s. As an additional

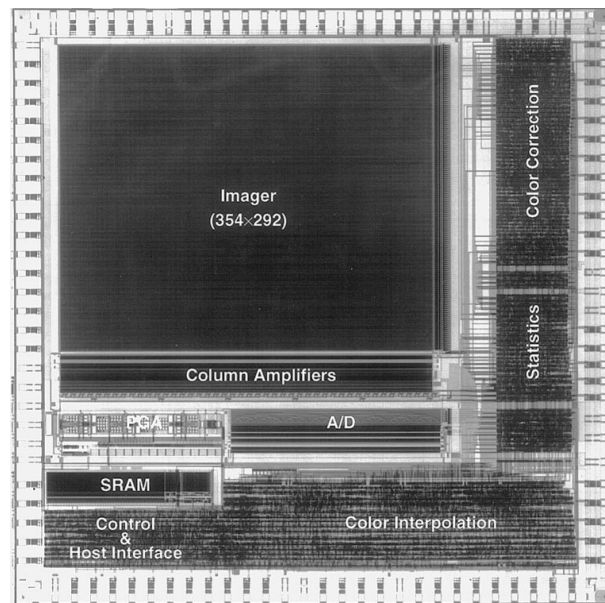


Fig. 12. Die micrograph.

feature, electronic shuttering is used to produce exposure times from 110 μs to 33 ms. The imager, PGA, A/D, bias circuits, and SRAM block were custom designed. The color-processing, chip-control, and host-interface blocks consist of more than 40 000 gates and were synthesized from a hardware description language with the use of a standard-cell library. Layout of the digital circuits was performed with the use of an automatic place-and-route tool.

The chip is fully functional, and a clean color video image is produced at 30 frames/s. Fig. 13 shows a sample monochrome image taken from the chip. A summary of chip characteristics



Fig. 13. Sample monochrome image.

TABLE I
SUMMARY OF CHIP CHARACTERISTICS

Array Size	354×292
Output Format	24-b RGB, 352×288 (CIF)
Input Clock Frequency	27MHz
Pixel Rate	3MHz
Frame Rate	30Hz
Number of Transistors	740,000
Total Power Dissipation	182mW (@3.3V)
Imager	20mW (11%)
PGA	10mW (5%)
A/D	40mW (22%)
Digital Core	92mW (51%)
Pad Frame	20mW (11%)
Die Size	10.2mm × 10.3mm
Imager	45mm ² (43%)
PGA	1.8mm ² (1.7%)
A/D	3.6mm ² (3.4%)
Digital Core	37mm ² (35%)
Technology	0.8-μm CMOS 1-P 2-M

is given in Table I. Over half the total power dissipation of 182 mW is dissipated in the digital processing block and the pad frame. It should be emphasized that power minimization was *not* an explicit goal in the design of the color-processing circuits. The color-processing circuits were designed to be highly programmable with experimental goals in mind. Furthermore, the chip has 15 extra digital output signals, switching at either the pixel clock rate or the digital clock rate, that are intended for testing and debugging purposes only. Based on these considerations and the use of full-custom design techniques, the digital color-processing circuit area and power dissipation can be significantly reduced.

The imaging performance of the prototype is summarized in Table II. The measured conversion gain of 40 $\mu\text{V}/\text{electron}$ is 43% higher than the result presented in [10] due to the use of unity-gain OTA's in the pixel readout path, as discussed in Section II-A. Although the photogate sensor is capable of

TABLE II
SUMMARY OF IMAGING PERFORMANCE

Pixel Size	18 μm × 18 μm
Drawn Active Area Fill Factor	35%
Saturated Signal	40k electrons (1 V)
Conversion Gain	40 $\mu\text{V}/\text{electron}$
Sensitivity (monochrome)	7V/lux-s
Sensitivity (red)	1.3 V/lux-s
Sensitivity (green)	1.5 V/lux-s
Sensitivity (blue)	0.91 V/lux-s
Imager + PGA Dynamic Range	65dB
Dark Signal (norm. to pixel area)	0.1 nA/cm ²
Pixel-Pixel FPN	0.3% p-p of sat.
Column-Column FPN	0.3% p-p of sat.

(All data at 33-ms integration time and 25°C)

a dynamic range well over 70 dB, as shown in Fig. 2, the dynamic range of the imager-PGA combination is limited to 65 dB by thermal noise in the PGA.

For the purposes of this work, FPN was evaluated using a dark image created by averaging 100 frames. The peak-to-peak pixel FPN is defined as six times the square root of the average of the variances of each column. Peak-to-peak column FPN is defined as six times the square root of the average of the variances of each row. By this definition, column FPN includes the effects of both pixel-to-pixel and column-to-column mismatches that are not eliminated by the operation of the column readout circuits and the PGA as described in Section II. A typical value for pixel FPN is 0.25% peak-to-peak relative to the 1-V full-scale output of the imager. As in [10], pixel FPN is limited by dark current nonuniformity in the sensor array. A typical value for column FPN is 0.29% peak to peak. Column FPN is slightly higher than pixel FPN because of gain variations in the column output buffers. While column FPN is not visible under normal room lighting conditions, it becomes noticeable at light levels of 1–5 lux, when the maximum PGA gain of 64 is used.

B. Digital Switching Noise

To study the effects of switching noise produced by the digital circuits on the analog signal chain, supply bounce sensor transistors were integrated on the chip. As shown in Fig. 14, separate positive supplies are used for the analog signal chain and for the digital color-processing circuits. The negative digital and analog supplies were shorted together through the substrate. The negative supplies could not be separated because the standard cells used in the digital section incorporated substrate contacts tied to the negative supply. The supply bounce sensors are PMOS devices (M_1 and M_2 in Fig. 14) with their gates connected to the local negative power supply and their sources connected to the local positive power supply. The current flowing in each of the bounce sensors is therefore a direct measure of the voltage difference between the local positive and negative supplies. This current is measured by connecting the drain of the bounce sensor

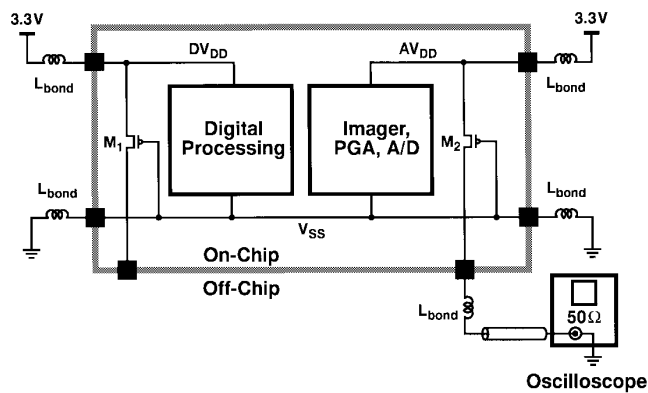


Fig. 14. Supply bounce measurement setup.

device, through a pad, to the 50- Ω terminated input of an oscilloscope.

The video image produced by the chip was subjectively very clean. No artifacts in the image have been attributed to switching noise coupling from the digital circuits into the analog circuits. Some insight as to why this is can be gained from studying the supply bounce waveforms. Fig. 15(a) shows the master-clock, pixel-clock, and digital-clock waveforms. As described in Section III, the strobing of the A/D comparators occurs during the quiet period in the digital clock. Fig. 15(b) shows the outputs of the PGA and the digital and analog supply bounce sensors. The output of the PGA (loaded by a 10-pF oscilloscope probe) shows a transition in the image from a bright to a dark section. It is important to note that the bounce waveforms are essentially periodic with the pixel clock, even as the input data are changing. Furthermore, the noise occurring outside the quiet period is highly correlated with the digital clock edges. This implies that the switching noise produced by the digital circuits in the analog blocks is dominated by the switching of the clock tree and is therefore largely data independent.

Because the supply bounce is essentially data independent, it tends to produce the same disturbance on every pixel in the output frame. This uniformity of disturbance and the supply rejection in the circuits making up the column output buffers and PGA circuits results in a video image with no visible artifacts attributable to switching noise. To test this hypothesis, the chip was configured so that the quiet period in the digital clock was eliminated and the color-processing circuits were active during the A/D comparator strobe. Note that, as mentioned in Section III, the A/D input is single ended. Again, no visible effect was observed in the video image except for a slightly perceptible dc shift.

V. CONCLUSION

A single-chip digital color camera has been described. The chip produces 24-b CIF video at 30 frames/s while dissipating 200 mW from a 3.3-V supply. An imager, PGA, and A/D converter are integrated along with digital color-processing cir-

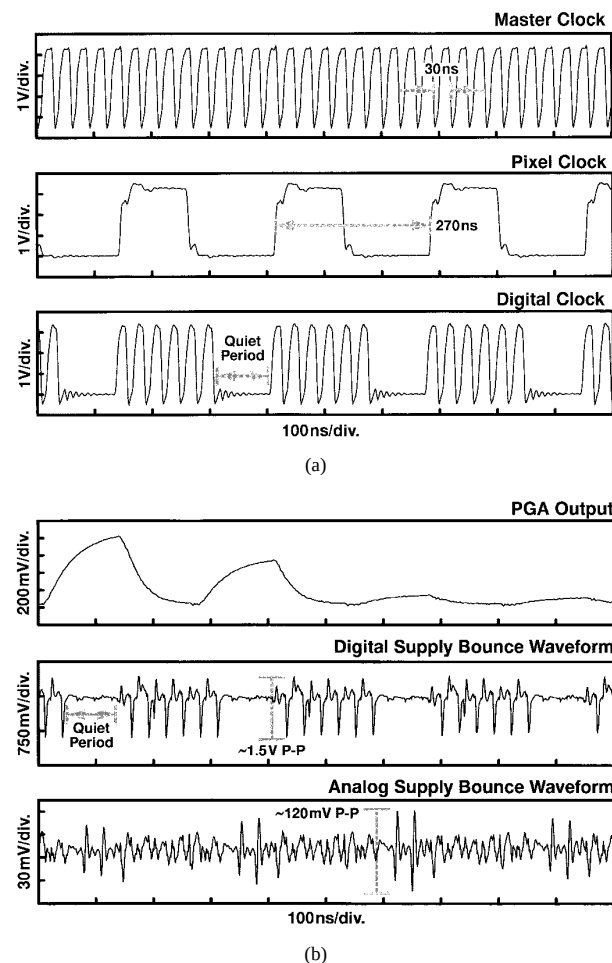


Fig. 15. (a) Clock waveforms and (b) PGA and supply bounce waveforms.

cuits that deliver over 120-M arithmetic operations per second. The digital circuits perform color interpolation, color correction, and computation of image statistics. Column circuits based on OTA's configured in unity-gain feedback have been used to increase the effective conversion gain of the imager. A hierarchical multiplexer was used for column readout, greatly reducing the capacitive load driven by column output buffers. A switched-capacitor PGA was used to cancel column FPN and to provide gain control in the analog signal chain. The PGA has a gain that is dynamically variable from pixel to pixel and allows white balancing to be performed in the analog domain by a single pipelined amplifier. The A/D converter was designed to take advantage of video blanking intervals to perform self-calibration. Experimental results show that the switching noise generated by the digital processing circuits is largely data independent and has no visible effect on image quality.

In implementing a single-chip digital color camera, circuit-design techniques have been taken from the areas of CMOS sensor design, memory decoder design, switched-capacitor circuits, and A/D conversion to optimize the analog signal chain for low power, low read noise, and low fixed-

pattern noise. This full-custom design methodology was seamlessly combined with a digital design flow based upon high-level specification and logic synthesis with standard cells. The performance of the prototype single-chip camera proves that it is feasible for a CMOS sensor array in a mixed-signal system-on-a-chip to achieve image quality comparable to that of CCD-based desktop multimedia camera systems.

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REFERENCES

- [1] D. Renshaw, P. Denyer, G. Wang, and M. Lu, "ASIC vision," in *Proc. CICC*, June 1990, pp. 7.3.1–7.3.4.
- [2] O. Yadid-Pecht, R. Ginosar, and Y. Diamand, "A random access photodiode array for intelligent image capture," *IEEE Trans. Electron Devices*, vol. 38, pp. 1772–1780, Aug. 1991.
- [3] E. Fossum, "Active pixel image sensors—Are CCD's dinosaurs?" in *Proc. SPIE*, vol. 1900, Feb. 1993, pp. 2–14.
- [4] B. Ackland and A. Dickinson, "Camera on a chip," in *ISSCC Dig.*, Feb. 1996, pp. 22–25.
- [5] M. Loinaz, K. Singh, A. Blanksby, D. Inglis, K. Azadet, and B. Ackland, "A 200-mW 3.3V CMOS color camera IC producing 352×288 24b video at 30 frames/s," in *ISSCC Dig.*, Feb. 1998, pp. 168–169.
- [6] S. Smith, J. Hurwitz, M. Torrie, D. Baxter, A. Holmes, M. Panaghiston, R. Henderson, A. Murray, S. Anderson, and P. Denyer, "A single-chip 306×244 -pixel CMOS NTSC video camera," in *ISSCC Dig.*, Feb. 1998, pp. 170–171.
- [7] S. Mendis, S. Kemeny, and E. Fossum, "CMOS active pixel image sensor," *IEEE Trans. Electron Devices*, vol. 41, pp. 452–453, Mar. 1994.
- [8] A. Dickinson, B. Ackland, E. Eid, D. Inglis, and E. Fossum, "A 256×256 CMOS active pixel image sensor with motion detection," in *ISSCC Dig.*, Feb. 1995, pp. 226–227.
- [9] J. Hurwitz, P. Denyer, D. Baxter, and G. Townsend, "An 800K-pixel color CMOS sensor for consumer still cameras," in *Proc. SPIE*, vol. 3019, pp. 115–124, Feb. 1997.
- [10] A. Blanksby, M. Loinaz, D. Inglis, and B. Ackland, "Noise performance of a color CMOS photogate image sensor," in *IEDM Dig.*, Dec. 1997, pp. 8.6.1–8.6.4.
- [11] K. Itakura, T. Nobusada, Y. Toyoda, Y. Saitoh, N. Kokusanya, R. Nagayoshi, H. Tanaka, and M. Ozaki, "An aspect ratio switchable 2/3-inch 800k-pixel CCD image sensor," in *ISSCC Dig.*, Feb. 1995, pp. 220–221.
- [12] J. Bosiers, Y. Boersma, A. Kleimann, D. Verbugt, H. Peek, and A. van der Sijde, "A 1/3 progressive scan $1280(H) \times 960(V)$ FT-CCD for digital still camera applications," in *IEDM Dig.*, Dec. 1997, pp. 8.1.1–8.1.4.
- [13] R. Guidash, T. Lee, P. Lee, D. Sackett, C. Drowley, M. Swenson, L. Arbaugh, R. Hollstein, F. Shapiro, and S. Domer, "A 0.6-mm CMOS pinned photodiode color imager technology," in *IEDM Dig.*, Dec. 1997, pp. 8.8.1–8.8.3.
- [14] J. Bosiers, E. Roks, H. Peek, A. Kleinmann, and A. Van der Sijde, "An S-VHS compatible 1/3" color FT-CCD imager with low DAR current by surface pinning," *IEEE Trans. Electron Devices*, vol. 42, pp. 1449–1460, Aug. 1995.
- [15] N. Weste and K. Eshraghian, *Principles of CMOS VLSI Design*. Reading, MA: Addison-Wesley, 1985.
- [16] K. Nagaraj, J. Vlach, T. Viswanathan, and K. Singhal, "Switched-capacitor integrator with reduced sensitivity to amplifier gain," *Electron. Lett.*, vol. 22, pp. 1103–1105, Oct. 1986.
- [17] B. E. Bayer, "Color imaging array," U.S. Patent 3971065, July 1976.
- [18] K. A. Parulski, "Color filters and processing alternatives for one-chip cameras," *IEEE Trans. Electron Devices*, vol. ED-32, no. 8, pp. 1381–1389, Aug. 1985.
- [19] W. N. Sproson, *Color Science in Television and Display Systems*. Bristol, U.K.: Adam Hilger, 1983.
- [20] D. K. Su, M. J. Loinaz, S. Masui, and B. A. Wooley, "Experimental results and modeling techniques for substrate noise in mixed-signal integrated circuits," *IEEE J. Solid-State Circuits*, vol. 28, pp. 420–430, Apr. 1993.
- [21] T. Blalack and B. A. Wooley, "The effects of switching noise on an oversampling A/D converter," in *ISSCC Dig.*, Feb. 1995, pp. 200–201.



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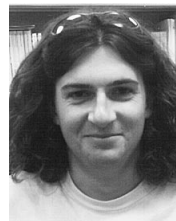
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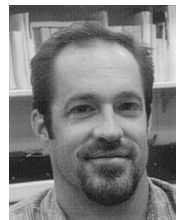
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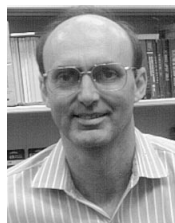


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