

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD.
Petitioner

v.

PICTOS TECHNOLOGIES, INC.
Patent Owner

Patent No. 6,838,651

**DECLARATION OF R. JACOB BAKER, PH.D., P.E.
IN SUPPORT OF PETITION FOR *INTER PARTES* REVIEW
OF U.S. PATENT NO. 6,638,651**

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I, R. Jacob Baker, Ph.D., P.E., declare as follows:

I. INTRODUCTION

1. I have been retained by Samsung Electronics Co., Ltd. (“Petitioner”) as an independent expert consultant in this proceeding before the United States Patent and Trademark Office (“PTO”) regarding U.S. Patent No. 6,838,651 (“the ’651 patent”) (Ex. 1001).¹

2. I am being compensated at a rate of \$615/hour for my work in this proceeding.

3. My compensation is in no way contingent on the nature of my findings, the presentation of my findings in testimony, or the outcome of this or any other proceeding. I have no other interest in this proceeding.

4. I have been asked to consider whether certain references disclose or suggest the features recited in claims 1-5 and 18-22 of the ’651 patent. My opinions are set forth below.

¹ Where appropriate, I refer to exhibits that I understand are to be attached to the petition for *Inter Partes* Review of the ’651 patent.

II. BACKGROUND AND QUALIFICATIONS

5. I presently serve as a Professor of Electrical and Computer Engineering at the University of Nevada, Las Vegas (UNLV). All of my opinions stated in this declaration are based on my own personal knowledge and professional judgment. In forming my opinions, I have relied on my knowledge and experience in designing, developing, researching, and teaching regarding integrated circuit design, including the design and fabrication of image processing circuits.

6. I am over 18 years of age and, if I am called upon to do so, I would be competent to testify as to the matters set forth herein. I understand that a copy of my current curriculum vitae, which details my education and professional and academic experience, is being submitted by Petitioner as Exhibit 1003. The following provides an overview of some of my experience that is relevant to the matters set forth in this declaration.

7. I have been teaching electrical engineering at UNLV since 2012. Prior to this position, I was a Professor of Electrical and Computer Engineering at Boise State University from 2000. Prior to my position at Boise State University, I was an Associate Professor of Electrical Engineering between 1998 and 2000 and Assistant Professor of Electrical Engineering between 1993 and 1998 at the University of Idaho. I have been teaching electrical engineering since 1991.

8. I received my Ph.D. in Electrical Engineering from the University of Nevada, Reno in 1993. I also received a MS and BS in Electrical Engineering from UNLV in 1988 and 1986, respectively.

9. As described in my CV, I am a licensed Professional Engineer and have more than 30 years of industry and academic experience, including extensive experience in the design of imaging pixels. Three of my PhD students have focused their dissertations on the design of pixels for various uses including increasing the dynamic range of a CMOS imager, radiation hardness, and very high-speed frame-rates. Further, I have worked on the design of commercial imagers, including the pixel design, when I worked for Micron imaging and OmniVision.

10. I have taught courses in integrated circuit design (analog, digital, mixed-signal, memory circuit design, etc.), linear circuits, microelectronics, communication systems, power electronics, and fiber optics. As a professor, I have been the main advisor to over 90 Master's and Doctoral students.

11. I am the author of several books covering the area of integrated circuit design including: DRAM Circuit Design: Fundamental and High-Speed Topics (two editions), CMOS Circuit Design, Layout, and Simulation (four editions), and CMOS Mixed-Signal Circuit Design (two editions). I have authored, and coauthored, more

than 100 papers and presentations in the areas of solid-state circuit design, and I am the named inventor on 152 granted U.S. patents.

12. I have received numerous awards for my work, including the Frederick Emmons Terman (the “Father of Silicon Valley”) Award. The Terman Award is bestowed annually upon an outstanding young electrical/computer engineering educator in recognition of the educator’s contributions to the profession.

13. I am a Fellow of the IEEE for contributions to memory circuit design. I have also received the IEEE Circuits and Systems Education Award (2011).

14. I have received the President’s Research and Scholarship Award (2005), Honored Faculty Member recognition (2003), and Outstanding Department of Electrical Engineering Faculty recognition (2001), all from Boise State University. I have also received the Tau Beta Pi Outstanding Electrical and Computer Engineering Professor award four of the years I have been at UNLV.

15. I am not an attorney and offer no legal opinions, but in the course of my work, I have had experience studying and analyzing patents and patent claims from the perspective of a person skilled in the art.

III. MATERIALS REVIEWED

16. The opinions contained in this Declaration are based on the documents I reviewed, my professional judgment, as well as my education, experience, and knowledge regarding circuits, including fuse-based circuits used in memory devices.

17. In forming my opinions expressed in this Declaration, I reviewed the '651 patent (Ex. 1001); the prosecution file history for the '651 patent (Ex. 1004); Japanese Patent Publication 2000-12819 ("*Isogai*") (Ex. 1005); U.S. Patent No. 5,982,984 to Inuiya et al. ("*Inuiya*") (Ex. 1006); U.S. Patent No. 7,133,073 to *Neter* ("*Neter*") (Ex. 1007); U.S. Patent No. 6,704,049 to Fossum ("*Fossum*") (Ex. 1008); Loinaz et al., "A 200-mW, 3.3-V, CMOS Color Camera IC Producing 352 x 288 24-b Video at 30 Frames/s," *IEEE Journal of Solid-State Circuits*, Vol. 33, No. 12, December 1998 ("*Loinaz*") (Ex. 1010); U.S. Patent No. 6,115,065 to Yadid-Pecht et al. ("*Yadid-Pecht*") (Ex. 1011); U.S. Patent No. 6,882,364 to Inuiya et al. ("*Inuiya-364*") (Ex. 1012); U.S. Patent No. 5,982,318 to Yiannoulous ("*Yiannoulous*") (Ex. 1013); and any other materials I refer to in this Declaration in support of my opinions.

18. All of the opinions contained in this declaration are based on the documents I reviewed and my knowledge and professional judgment. My opinions have also been guided by my appreciation of how a person of ordinary skill in the

art would have understood the claims and the specification of the '651 patent at the time of the alleged invention, which I have been asked to consider was the early 2000's (including May 4, 2000, the date an Innovation Disclosure from the listed inventor Richard Mann was mailed to patent counsel (Ex. 1004, 38-39) and March 28, 2002, the filing date of U.S. Application No. 10/113,545 ("the '545 application") which led to the '651 patent). My opinions reflect how one of ordinary skill in the art would have understood the '651 patent, the prior art to the '651 patent, and the state of the art at the time of the alleged invention.

19. Based on my experience and expertise, it is my opinion that certain references disclose or suggest all the features recited in claims 1-5 and 18-22 ("challenged claims") of the '651 patent, as I discuss in detail below.

IV. PERSON OF ORDINARY SKILL IN THE ART

20. Based on my knowledge and experience, I understand what a person of ordinary skill in the art would have known at the time of the alleged invention. My opinions herein are, where appropriate, based on my understandings as to a person of ordinary skill in the art at that time. In my opinion, based on the materials and information I have reviewed, and based on my experience in the technical areas relevant to the '651 patent, a person of ordinary skill in the art at the time of the alleged invention of the '651 patent would have had at least a bachelor's degree in

electrical engineering, computer science, or the equivalent, and two or more years of experience with image processing. More education can supplement practical experience and *vice versa*. I apply this understanding in my analysis herein.

21. My analysis of the '651 patent and my opinions in this declaration are from the perspective of one of ordinary skill in the art, as I have defined it above, during the relevant time frame, which I have been asked to assume is the early 2000s timeframe (including the May 4, 2000 Innovation Disclosure date as well as the March 28, 2002 the filing date of the '545 application"). During this time frame, I possessed at least the qualifications of a person of ordinary skill in the art, as defined above.

V. TECHNICAL BACKGROUND

22. In this section, I discuss the state of the art with respect to certain technologies relevant to the subject matter of the '651 patent.

A. Solid-State Imaging Devices

23. At the time of the invention, solid-state imaging devices typically included an array of pixels, where, for example, different pixels are sensitive to different colors in the light spectrum. For example, the figures below show red, green, and blue pixels arranged in the checkered "Bayer" pattern where two green pixels are included for each red and blue pixel. (Ex. 1005, ¶[0009], "In the

arrangement shown in FIG. 28, the green (G) color filters are arranged in a checkered pattern, and the red (R) and blue (B) color filters are line-sequentially arranged corresponding to the remaining pixels (generally called a Bayer array).”)

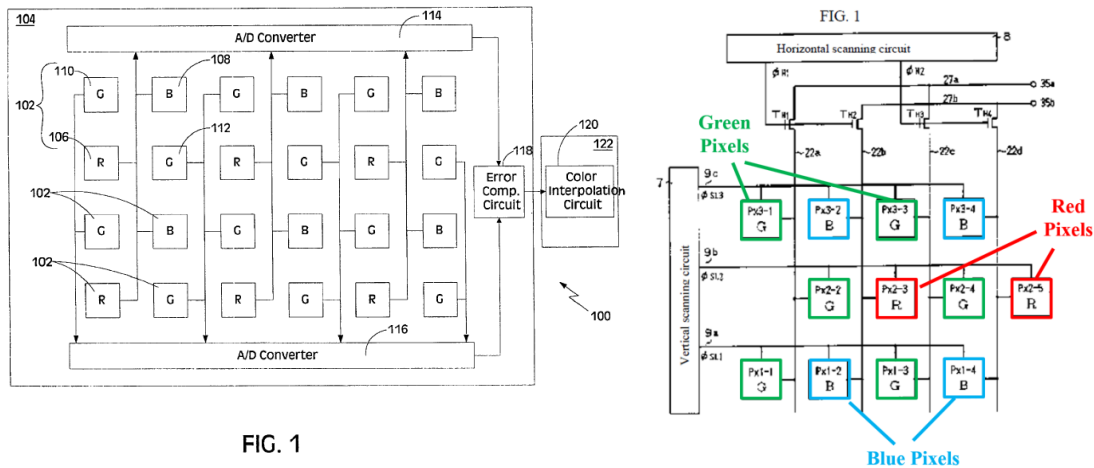
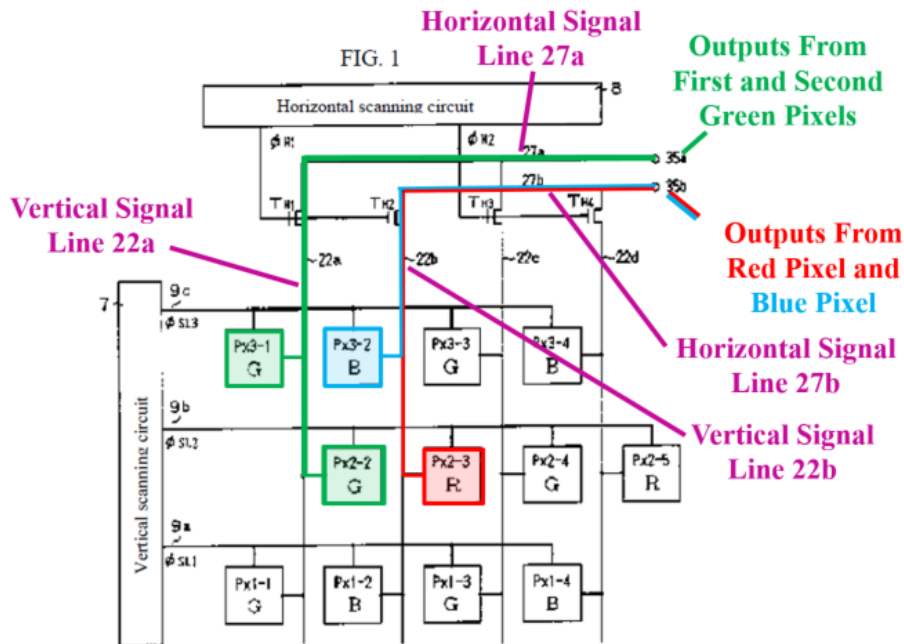


FIG. 1

(Ex. 1001, FIG. 1; Ex. 1005, FIG. 1 (annotated).)

24. Light incident on the pixels, which typically include photosensors such as photodiodes, results in a signal charge being generated in the pixel, where the accumulated charge is output by the pixel when the particular pixel is accessed by the row/column circuitry used to select pixels in the array (e.g. horizontal and vertical scanning circuits shown in figure 1 of *Isogai* below).

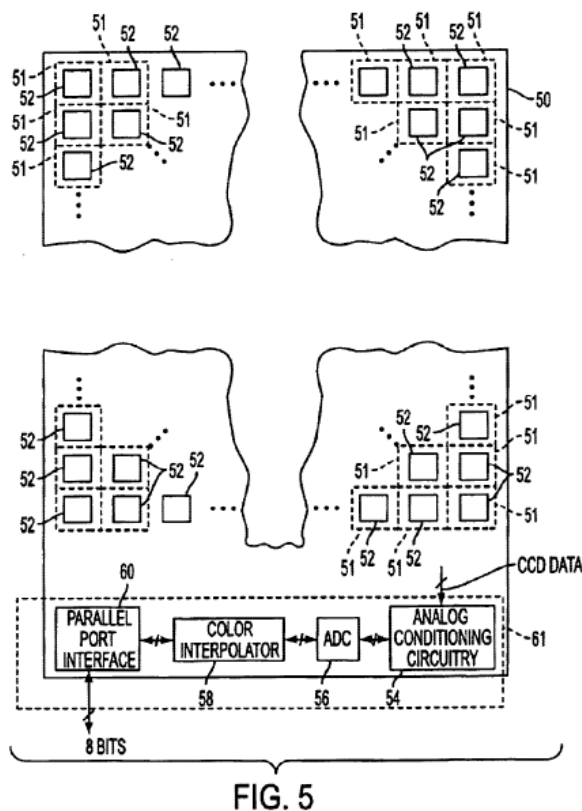


(Ex. 1005, FIG. 1 (annotated).)

25. As shown in figure 1 of *Isogai* above, the horizontal and vertical signal lines route the output signals from the pixels to subsequent processing circuitry. (Ex. 1005, FIG. 1.) The horizontal and vertical scanning circuits step through the pixel array, causing the outputs of the pixels in each row and column to be sequentially output on the horizontal signal lines 27a and 27b shown above.

26. The analog signals produced by the pixels are typically digitized in order to allow subsequent processing of the digital signals. As such, imaging systems include analog-to-digital converters that convert the analog pixel outputs to digital signals that can be combined with digital processing circuitry, such a digital

signal processor (DSP). For example, *Fossum* shows a pixel array included on a chip with analog-to-digital conversion circuitry (ADC 56) as well as a color interpolator that processes the resulting digital signals



(Ex. 1008, FIG. 5.)

VI. OVERVIEW OF THE '651 PATENT

A. The '651 Patent

27. The '651 patent is entitled "High Sensitivity Snap Shot CMOS Image Sensor." The '651 patent "relates generally to solid-state imaging devices" "implementing multiple analog-to-digital ('A/D') converters to obtain high frame

rates.” (Ex. 1001, 1:6-11.) The ’651 patent states that the imaging device has “four color channels (one red, one blue and two greens) used to define a color image based upon the Bayer Pattern of color filters.” (Ex. 1001, 3:1-4.) While “it is natural to use a separate A/D converter for each of the color channels,” the ’651 patent discloses that “two A/D converters may be employed, where one A/D converter is used for the red and blue channels and the second A/D converter is used for the green channels.” (*Id.*, 3:8-10.)

28. Figure 1 of the ’651 patent “illustrates a block diagram of a solid state imaging device having two analog-to-digital converters” (Ex. 1001, 4:16-17, FIG. 1) that includes a two-dimensional array of image pixels 102 (*id.*, 4:30-31). “Each pixel 102 is either a red pixel 106 having a red photodiode, a blue pixel 108 having a blue photodiode or a green pixel 110, 112 having a green photodiode.” (*Id.*, 4:33-36.) “The output of each pixel 102 is proportional to the amount of light incident on the pixel 102.” (*Id.*, 4:43-44.)

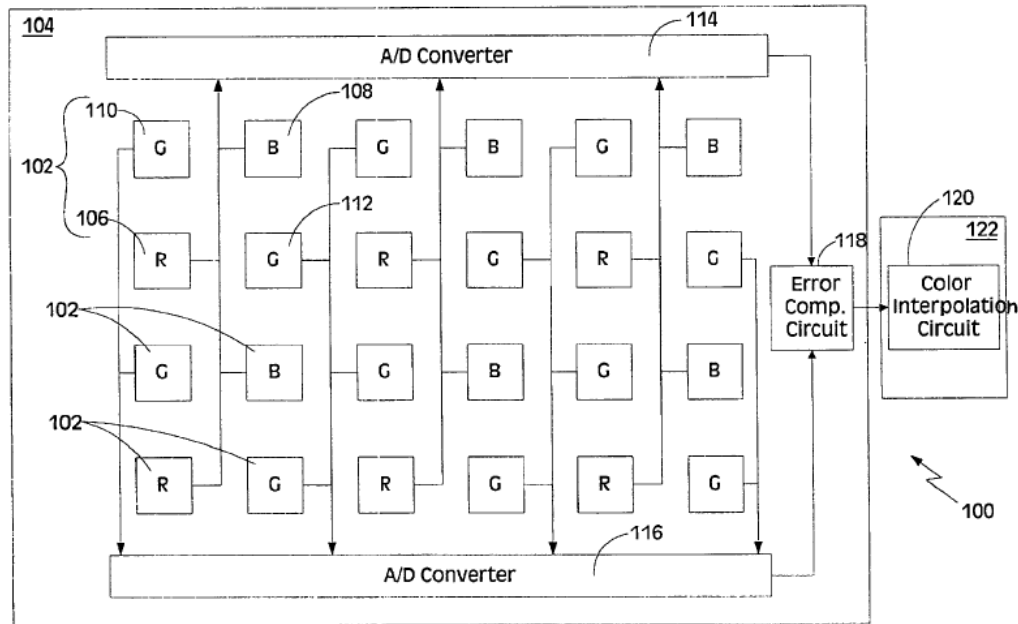


FIG. 1

(Ex. 1001, FIG. 1.)

29. The imaging device includes a first analog-to-digital converter 114 and a second analog to digital converter 116. (*Id.*, 4:62-64.) An error compensation circuit 118 “provides an independent gain to correct the gain for each color channel” and “provides an independent offset to correct the fixed pattern noise offset for each color channel.” (*Id.*, 5:3-7.) “The color interpolation circuit 120 performs the interpolation for each pixel 102 to determine the color of the pixel,” where “[t]he color interpolation circuit 120 may be located on a second chip 122, as shown in FIG 1” or “may be located on chip 104.” (*Id.*, 5: 23-27.)

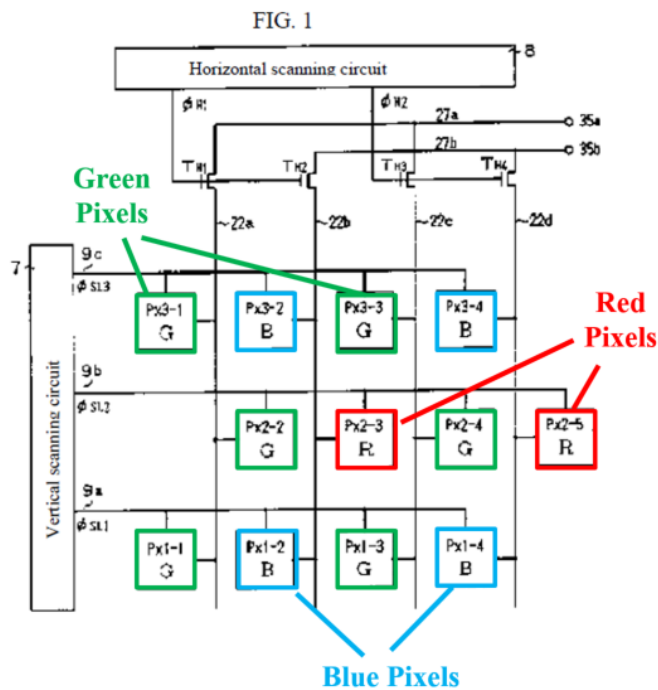
VII. CLAIM CONSTRUCTION

30. I understand that claim terms are typically given their ordinary and customary meaning, as would have been understood by a person of ordinary skill in the art, at the time of the alleged invention, which I understand is the early 2000s (including the time preceding the May 4, 2000 Innovation Disclosure date as well as the March 28, 2002 the filing date of the '545 application). In considering the meaning of the claims, however, I understand that one must consider the language of the claims, the specification, and the prosecution history of record.

VIII. OVERVIEW OF THE PRIOR ART

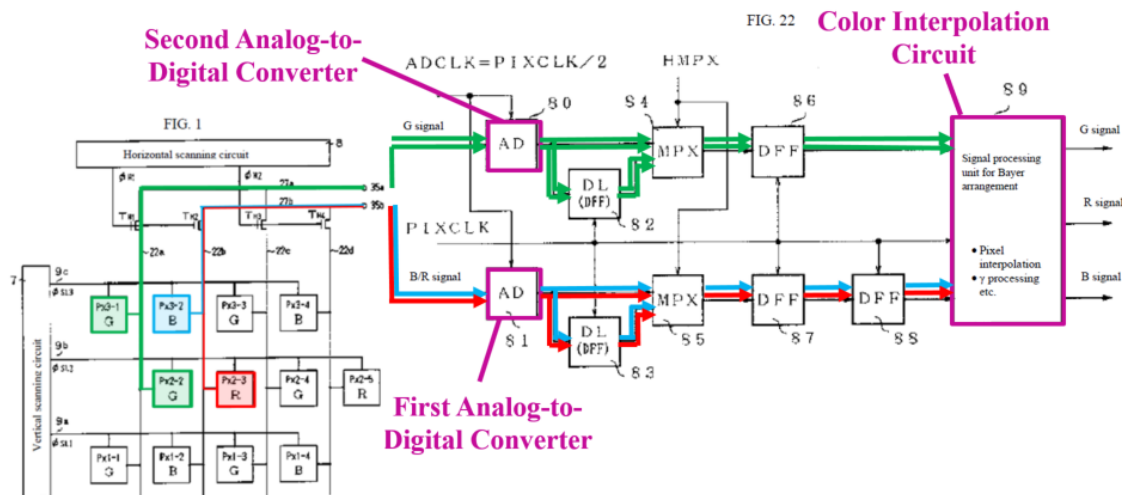
A. *Isogai*

31. *Isogai* discloses a “solid-state image sensing element having a parallel output configuration” where “a signal of a specified pixel arranged in a checkered pattern is output to one of two horizontal signal lines . . .” (Ex. 1005, Abstract; *see also id.*, ¶[0001]). As shown in annotated figure 1 below, the “solid state image sensing element” includes red, blue, and green pixels arranged in a checkered pattern that is consistent with the Bayer arrangement. (*Id.*, ¶¶[0026], [0028], FIG. 1.)



(*Id.*, FIG. 1 (annotated).)

32. *Isogai* also discloses a system for processing the signal outputs from the solid-state imaging sensing elements. (*Id.*, ¶¶[0077]-[0078], FIG. 22.) The processing system, which is shown in a demonstrative that combines figures 1 and 22 below, receives inputs from *Isogai*'s solid-state image sensing element shown in figure 1 and “performs color imaging using the solid-state image sensing element of the present invention in which a color filter is arranged in each pixel as described above” (*Id.*, ¶[0078], FIG. 22.)



(*Id.*, FIGs. 1, 22 (annotated).)

33. As shown in the demonstrative above, the outputs of the red and blue pixels are provided as the “B/R signal” to the analog-to-digital converter (AD) 81, whereas the outputs of the green pixels are provided as the “G signal” to the analog-to-digital converter (AD) 80. (*Id.*, ¶[0079] (“The G signal has the same frequency

as the signal output frequency of the solid-state image sensing element, and is **AD-converted** into the output signal in accordance with the timing.”) (emphasis added), ¶[0080] (“The second channel, in which the **B signal and the R signal** are output line-sequentially, is signal **processed in the same manner** as the first channel (G signal)”) (emphasis added).)

34. *Isogai* also includes a signal processing unit 89 that combines the first, second, third, and fourth digital signals (Ex. 1005, ¶¶[0077]-[0080], FIG. 22.) For example, *Isogai* discloses that:

The **signal processing unit 89** is a signal processing unit for Bayer arrangement, and **performs signal processing such as R / B color separation, pixel interpolation of empty grid points of each RGB color and λ processing to output RGB color signals with all pixels having RGB color signal.**

(*Id.*, ¶[0080], emphasis added.)

B. *Inuiya*

35. *Inuiya* discloses a “a solid-state electronic image sensing device and a method of reading a signal change out of the solid-state electronic image sensing device.” (Ex. 1006, 1:15-18; *see also id.*, 2:20-23.) *Inuiya* discloses:

A solid-state electronic image sensing device according to the present invention comprises photoelectric

transducers arrayed in a plurality of columns in the horizontal direction and a plurality of rows in the vertical direction, vertical transfer lines extending in the vertical direction adjacent the columns of photoelectric transducers for transfer, in the vertical direction, signal charge that has accumulated in the photoelectric transducers, a horizontal transfer line for transferring, in the horizontal direction, signal charge that has been transferred by the vertical transfer lines

(Ex. 1006, 4:56-67.)

36. Figure 18 of *Inuiya* is a block diagram of a digital video tape recorder that includes an image sensing section that includes a charge-coupled device (CCD) 100 that includes a large number of pixels. (*Id.*, 20:12-20.)

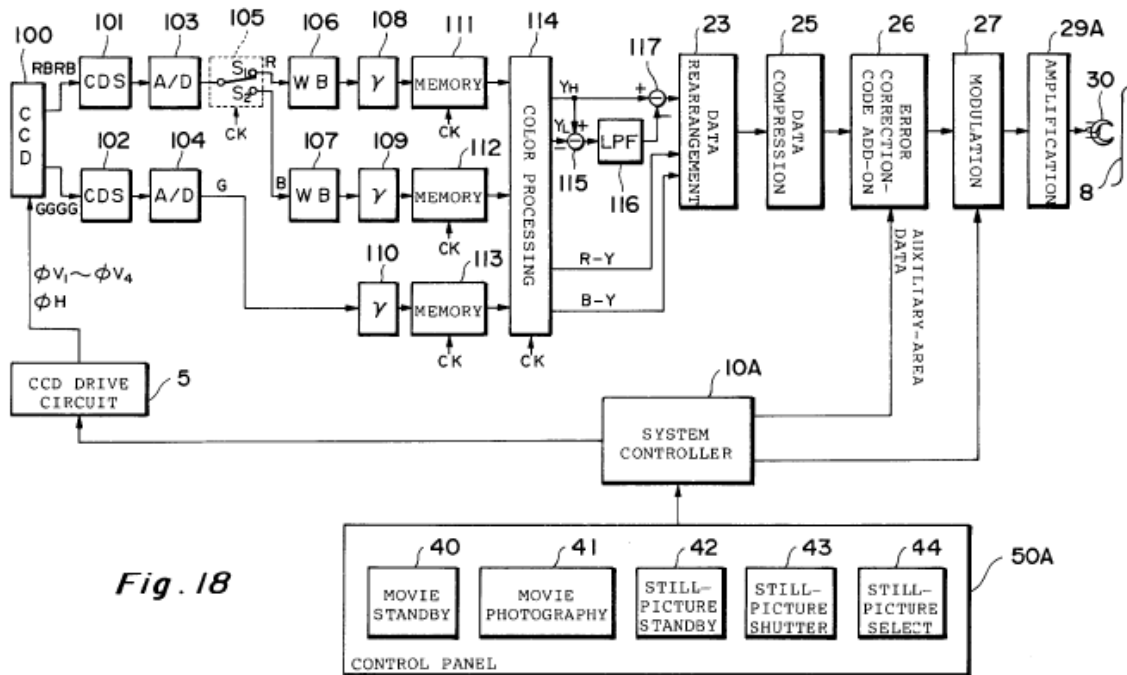
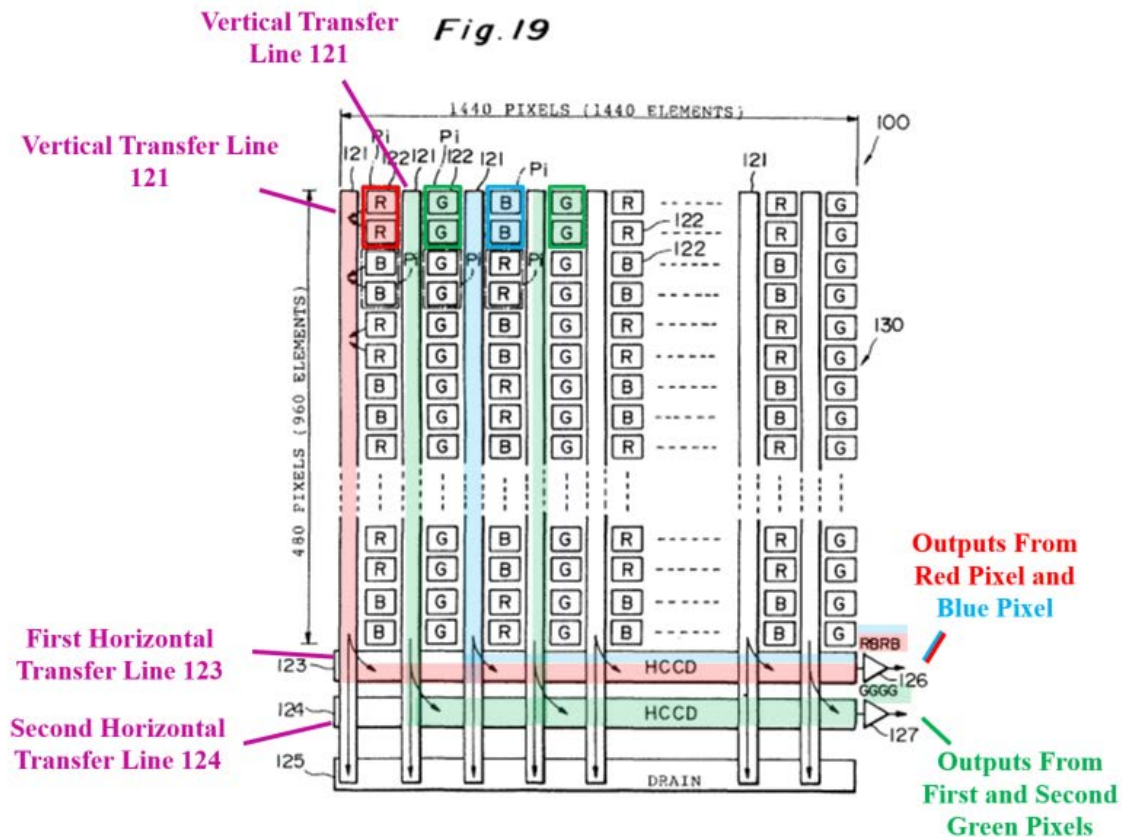


Fig. 18

(Id., FIG. 18.)

37. Figure 19 of *Inuiya* is a schematic view of the CCD 100 included in the solid-state image processing device shown in figure 18. (*Id.*, 20:23.) The CCD 100 includes a plurality of red, blue, and green pixels. *Inuiya* discloses that the signal charges that have accumulated in two photodiodes are mixed in the vertical transfer lines 121 of the CCD 100 such that the pixels, which are labeled “Pi” in figure 19, are each composed of two photodiodes 122. (*Id.*, 20:47-62.)

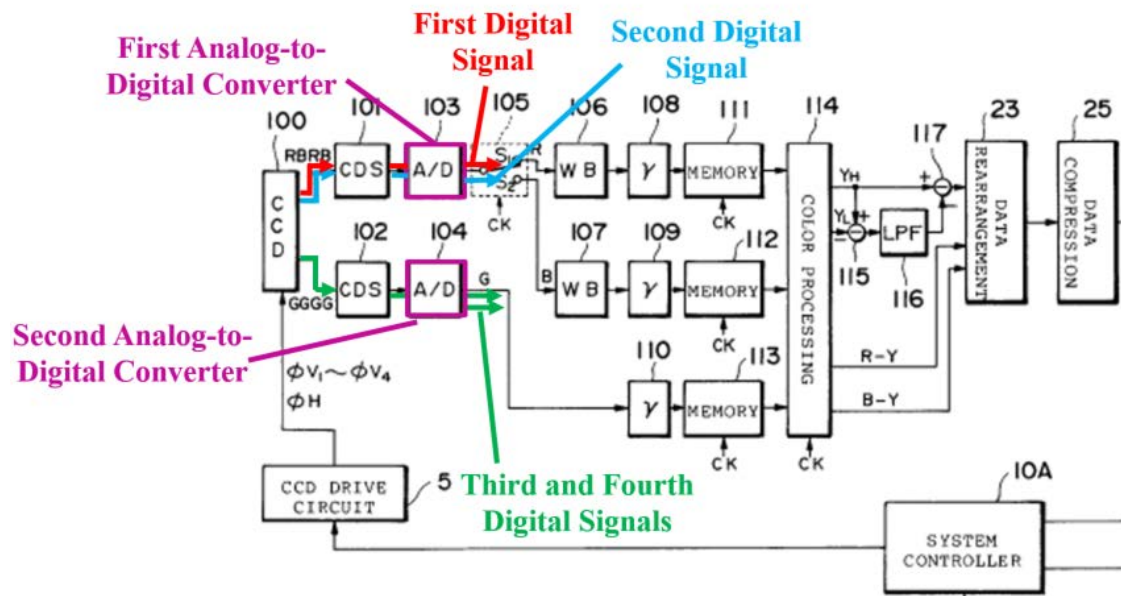


(*Id.*, FIG. 19 (annotated).)

38. As shown in figure 19 above, the red pixel output is connected to the first vertical transfer line 121, and the blue pixel output is connected to the third vertical transfer line 121. Similarly, the first green pixel output is connected to the second vertical transfer line 121, and the second green pixel output is connected to the fourth vertical transfer line 121. (Ex. 1006, 20:44-53, 21:7-12, FIG. 19.) The first and third vertical transfer lines 121 are connected to the horizontal transfer line 123, whereas the second and fourth vertical transfer lines are connected to the

horizontal transfer line 124. (Ex. 1006, 21:36-49.) Therefore, outputs of the red and blue pixels are output by amplifier 126 and the first/second green pixel outputs are output by amplifier 127. (*Id.*, 21:36-62, FIG. 19; *see also id.*, 23:10-14.)

39. As shown in the annotated excerpt of figure 18 below, *Inuiya* discloses that the output signals from the CCD 100 are provided through correlated data sampling circuits 101, 102 to analog-to-digital converters 103, 104. (*Id.*, 25:36-43.)



(*Id.*, FIG. 18 (excerpt, annotated).)

40. As shown in the annotated excerpt of figure 18 above, the outputs of the red and blue pixels are provided to the analog-to-digital converter (A/D) 103, and the outputs of the first and second green pixels (GGGG) are provided to the analog-to-digital converter (A/D) 104. (*Id.*, 25:36-43 .) After conversion to digital

signals, the output data from the pixels is provided to color processing circuit 114, which combines the pixel data to generate luminance and color difference data. (*Id.*, 26:5-19.)

IX. THE PRIOR ART DISCLOSES OR SUGGESTS ALL OF THE FEATURES OF CLAIMS 1-5 AND 18-22

A. *Isogai* Discloses or Suggests the Features of Claims 1 and 18

41. In my opinion, *Isogai* discloses or suggests all of the features of claims 1 and 18 of the '651 patent.

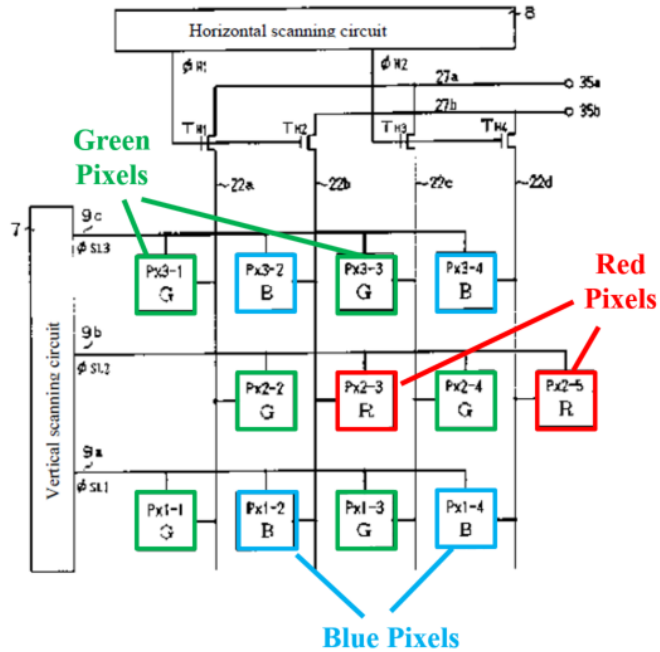
1. Claim 1

a) “A solid state imaging device, comprising:”

42. I understand that “[a] solid state imaging device, comprising” is the preamble of claim 1. I have been asked to assume that the preamble is limiting. In my opinion, *Isogai* discloses this feature. *Isogai* discloses a “solid-state image sensing element having a parallel output configuration” where “a signal of a specified pixel arranged in a checkered pattern is output to one of two horizontal signal lines” (Ex. 1005, Abstract; *see also id.*, ¶[0001].)

43. Annotated figure 1 of *Isogai* below, shows a solid state image sensing element according to a first embodiment disclosed in *Isogai*. (*Id.*, ¶[0026], FIG. 1.)

FIG. 1



(*Id.*, FIG. 1 (annotated).)

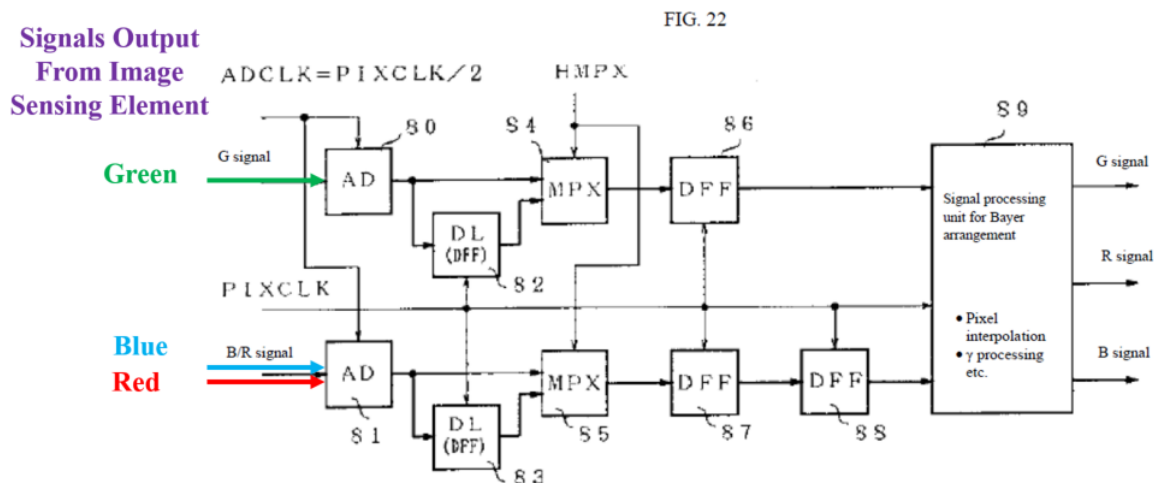
44. As shown in annotated figure 1 above, the “solid state image sensing element” includes red, blue, and green pixels arranged in a checkered pattern that is consistent with the Bayer arrangement that I discussed above in Section V.A. (*Id.*, ¶¶[0026], [0028], FIG. 1.; *see* my discussion above in Section V.A.) *Isogai* further discloses:

According to the solid-state image sensing element of the actual embodiment, one hundred or more pixels are arranged in both the row direction and the column direction. FIG. 1 (and each circuit diagram showing another embodiment) shows a part thereof for

convenience. Here, the number of pixels is set as described above, but the present invention is not limited to this. For example, 1000 or more pixels may be arranged in both the row direction and the column direction depending on the application.

(Ex. 1005, ¶[0026].)

45. In addition to disclosing various embodiments of solid-stage image sensing elements, including that shown in figure 1, *Isogai* also discloses a system for processing the signal outputs from the solid-state imaging sensing elements. (*Id.*, ¶[0077]-[0078], FIG. 22.) The processing system, which is shown in annotated figure 22 below, receives inputs from any one of *Isogai*'s disclosed solid-state image sensing elements (e.g. like that shown in figure 1) and “performs color imaging using the solid-state image sensing element of the present invention in which a color filter is arranged in each pixel as described above” (*Id.*, ¶[0078], FIG. 22.)

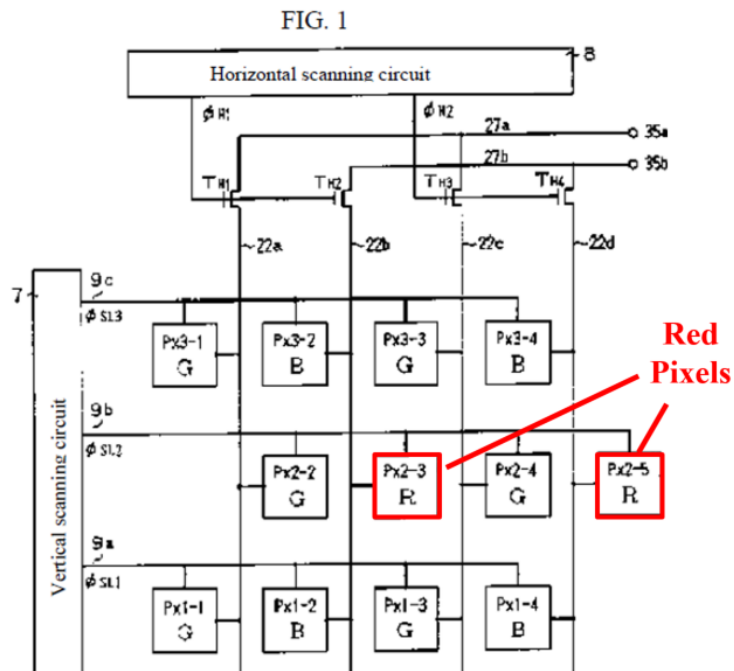


(*Id.*, FIG. 22 (annotated).)

46. The combination of the solid-stage image sensing element shown in figure 1 of *Isogai* with the processing system shown in figure 22 constitutes a “solid state imaging device” as recited in claim 1.

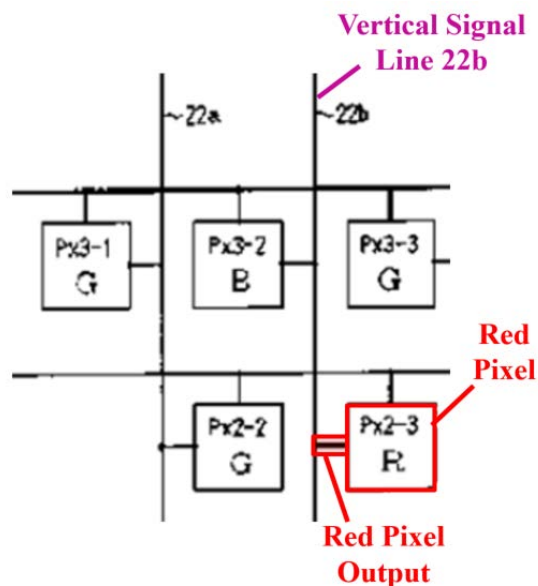
b) “a red pixel having an output;”

47. In my opinion, *Isogai* discloses this feature. As discussed above in section IX.A.1(a), each of the solid-stage image sensing elements that is included in a “solid state imaging device” disclosed in *Isogai* includes a plurality of red pixels. (See my discussion above in section IX.A.1(a).) For example, two such red pixels are shown in annotated figure 1 below. (Ex. 1005, ¶[0028] (“Further, green (G) color filters are provided in a checkered pattern and arranged on the corresponding pixels (Px1-1, Px1-3, Px2-2, Px2-4, Px3-1, Px3-3). **Red (R) and Blue (B) color filters are arranged** line-sequentially (Bayer arrangement) **on the remaining pixels.**”) (emphasis added), ¶¶[0024], [0035]-[0036], FIGs. 1, 3.) Specifically, as shown below, pixels Px2-3 and Px2-5 are red (R) pixels. (*Id.*)



(*Id.*, FIG. 1 (annotated).)

48. Each of the red pixels highlighted above has an output. With respect to the first embodiment in figure 1, *Isogai* discloses that vertical signal lines 22a-22b are used to connect alternating columns of pixels to either the first horizontal signal line 27a or the second horizontal signal line 27b. (*Id.*, ¶¶[0025], [0027], FIG. 1.) The signals (“outputs”) from the pixels are routed from the vertical signal lines to the horizontal signal lines and then output by the output terminals 35a and 35b. (*Id.*, ¶¶[0025], [0027]-[0029], FIG. 1.) As shown in the annotated and enlarged excerpt of figure 1 below, the red pixel Px2-3 has an output (“a red pixel having an output”) that connects to the vertical signal line 22b. (*Id.*, ¶¶[0025], [0027]-[0029], FIG. 1.)

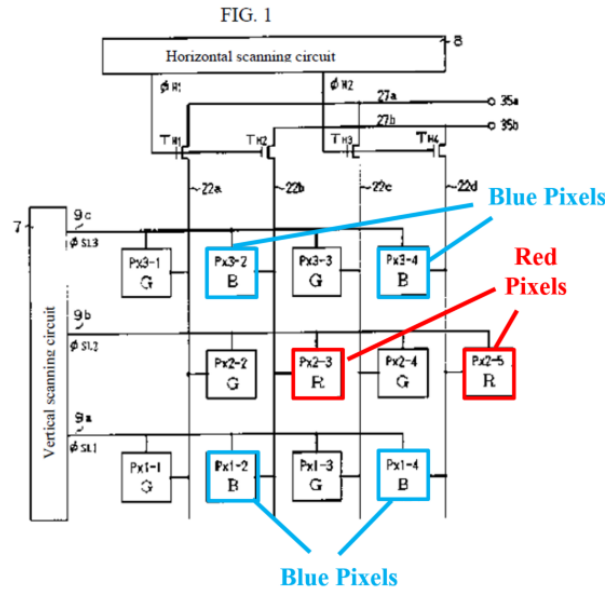


(*Id.*, FIG. 1 (excerpt, annotated).)

c) “a blue pixel having an output;”

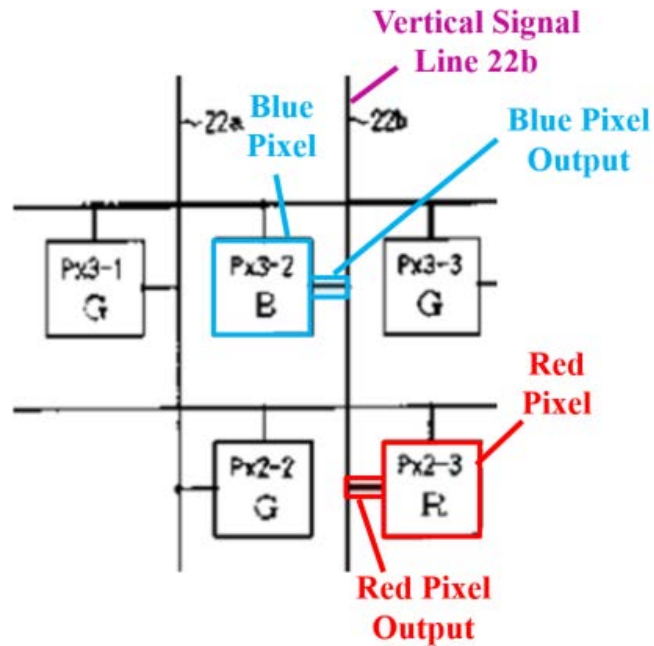
49. In my opinion, *Isogai* discloses this feature. As discussed above, each of the solid-state image sensing elements that is included in a “solid state imaging device” disclosed in *Isogai* includes a plurality of blue pixels. For example, four such blue pixels are shown in annotated figure 1 below. (Ex. 1005, ¶[0028] (“Further, green (G) color filters are provided in a checkered pattern and arranged on the corresponding pixels (Px1-1, Px1-3, Px2-2, Px2-4, Px3-1, Px3-3). Red (R) and **Blue (B) color filters are arranged line-sequentially (Bayer arrangement) on the remaining pixels.**”) (emphasis added), ¶¶[0025], [0027]-[0029], FIG. 1.)

Specifically, as shown below, pixels Px1-2, Px1-4, Px3-2, and Px3-4 are blue (B) pixels. (*Id.*, FIG. 1.)



(*Id.*, FIGs. 1, 3 (annotated).)

50. Like the red pixels I discussed above in Section IX.A.1(b), each of the blue pixels highlighted above has an output. (*Id.*, ¶¶[0025], [0027]-[0029], FIG. 1; *see* my analysis above in Section IX.A.1(b).) For example, as shown in the annotated and enlarged excerpt of figure 1 below, the blue pixel Px3-2, like the red pixel Px-2-3, has an output (“a blue pixel having an output”) that connects to the vertical signal line 22b. (*Id.*, ¶¶[0025], [0027]-[0029], FIG. 1.)

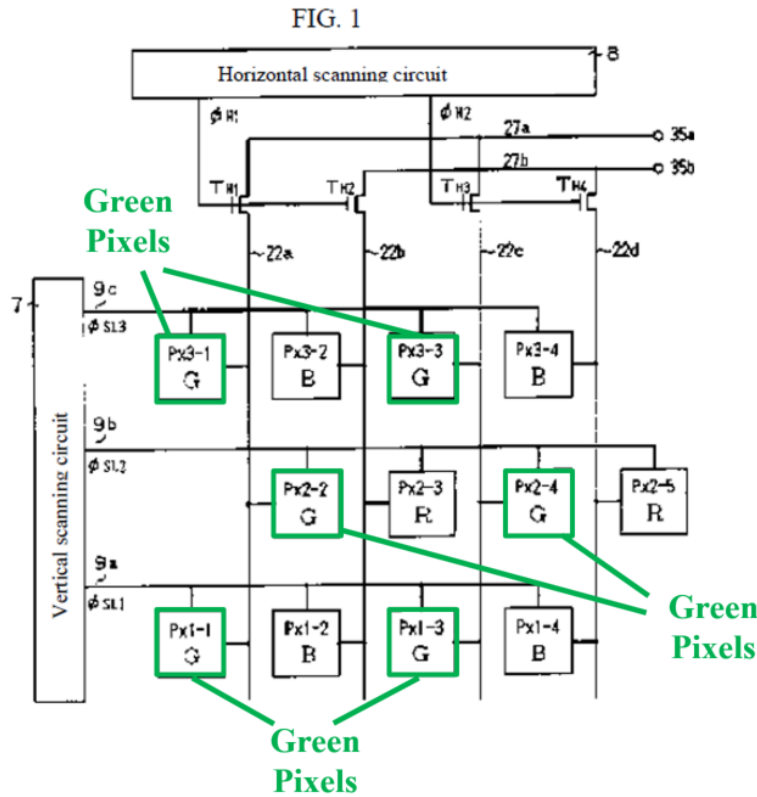


(*Id.*, FIG. 1 (excerpt, annotated).)

d) “a first green pixel having an output;”

51. In my opinion, *Isogai* discloses this feature. As discussed above, each of the solid-state image sensing elements that is included in a “solid state imaging device” disclosed in *Isogai* includes a plurality of green pixels. For example, six such green pixels are shown in annotated figure 1 below. (Ex. 1005, ¶[0028] (“Further, **green (G) color filters are provided in a checkered pattern and arranged on the corresponding pixels (Px1-1, Px1-3, Px2-2, Px2-4, Px3-1, Px3-3).** Red (R) and Blue (B) color filters are arranged line-sequentially (Bayer arrangement) on the remaining pixels.”) (emphasis added), ¶¶[0024], [0027]-[0029],

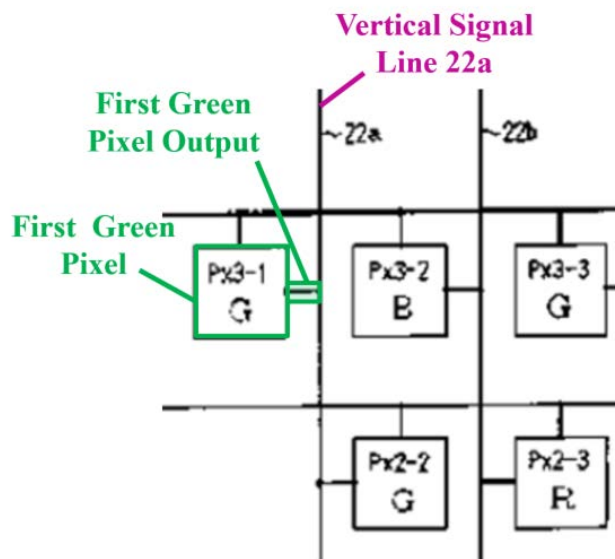
FIG. 1.) Specifically, as shown below, pixels Px1-1, Px1-3, Px2-2, Px2-4, Px3-1, and Px3-3 are green (G) pixels. (*Id.*, FIG. 1.)



(*Id.*, FIG. 1 (annotated).)

52. Like the red and blue pixels I discussed above in Sections IX.A.1(a)-(b), each of the green pixels highlighted above has an output. (*Id.*, ¶¶[0025], [0027]-[0029], FIGs. 1; see my analysis above in Sections IX.A.1(a)-(b).) For example, as shown in the annotated and enlarged excerpt of figure 1 below, the green pixel Px3-

1 has an output (“a first green pixel having an output”) that connects to the vertical signal line 22a. (*Id.*, ¶¶[0025], [0027]-[0029], FIG. 1.)



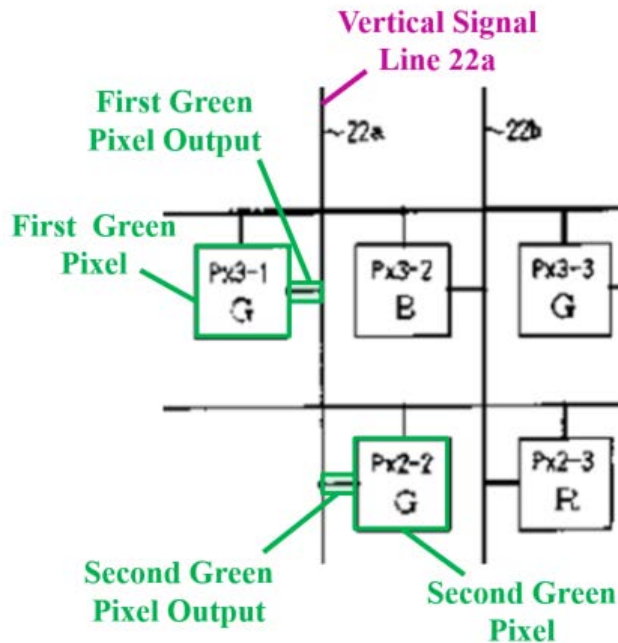
(*Id.*, FIG. 1 (excerpt, annotated).)

e) “a second green pixel having an output;”

53. As discussed above in Section IX.A.1(d), each of the solid-stage image sensing elements that is included in a “solid state imaging device” disclosed in *Isogai* includes a plurality of green pixels, where each of the green pixels has an output. (*See* my discussion above in Section IX.A.1(d).)

54. For example, as shown in the annotated and enlarged excerpt of figure 1 of *Isogai* below, the green pixel Px2-2 has an output (“a second green pixel having

an output”) that, like the first green pixel Px3-1, connects to the vertical signal line 22a. (*Id.*, ¶¶[0025], [0027]-[0029], FIG. 1.)

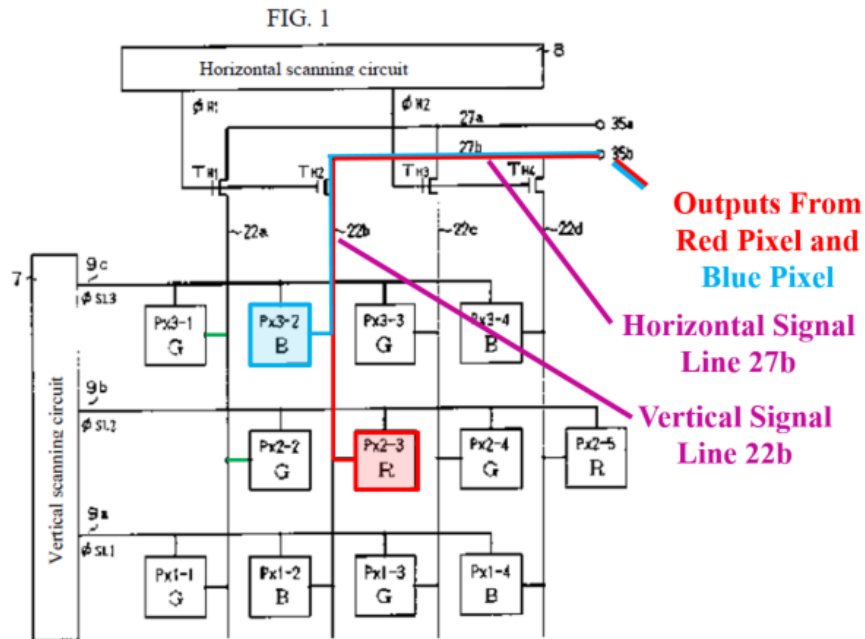


(*Id.*, FIG. 3 (excerpt, annotated).)

- f) “a first analog-to-digital converter connected to the output of the red pixel for converting the output of the red pixel into a first digital signal and connected to the output of the blue pixel for converting the output of the blue pixel into a second digital signal;”

55. In my opinion, Isogai discloses this feature. As discussed above in Section IX.A.1(s), the combination of the solid-stage image sensing element shown in figure 1 of *Isogai* with the processing system shown in figure 22 constitutes a “solid state imaging device” as recited in claim 1. (*See* my discussion above in

Section IX.A.1(a).) As also discussed above in Sections IX.A.1(b)-(e), each of the outputs of the red pixel Px2-3 (“red pixel”) and of the blue pixel Px3-2 (“blue pixel”) are connected to the vertical signal line 22b, whereas each of the outputs of the green pixel Px3-1 (“first green pixel”) and the green pixel Px2-2 (“second green pixel”) are connected to the vertical signal line 22a. (Ex. 1005, ¶¶[0027], FIG. 1; *see* my discussion above in sections IX.A.1(b)-(e).) As shown in annotated figure 1 below, the vertical signal lines 22a and 22b are connected to horizontal signal lines 27a and 27b, respectively. (*Id.*, ¶¶[0027] (“Further, the vertical signal lines 22a and 22c are connected to one of the horizontal signal lines 27a via the column selection transistors TH1 and TH3. The vertical signal lines 22b and 22d are connected to the other horizontal signal line 27b via the column selection transistors TH2 and TH4.”), FIG. 1.)



(*Id.*, FIG. 1 (annotated).)

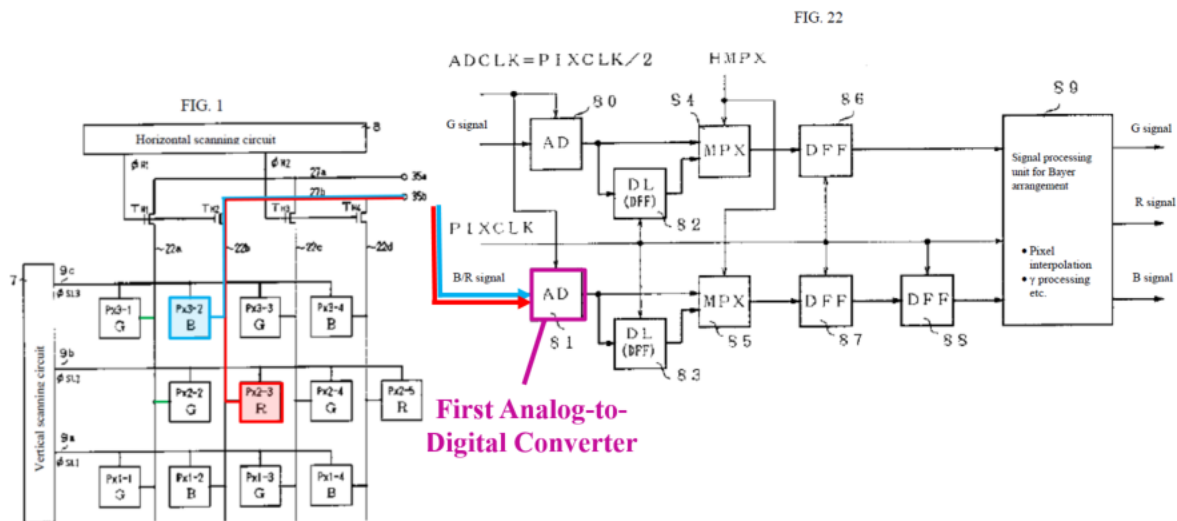
56. As disclosed by *Isogai*:

When the color filters are arranged in this way, the green (G) signal is output from the output terminal 35a via the same horizontal signal line 27a. Further the red (R) and blue (B) signals are output from the output terminal 35b via the other horizontal signal line 27b.

(*Id.*, ¶[0029].)

57. Thus, the outputs of the first and second green pixels are provided from the vertical signal line 22a to the vertical signal line 27a, whereas the outputs of the red and blue pixels are provided from the vertical signal line 22b to the horizontal signal line 27b.

58. *Isogai* discloses that the output signals from the solid-state image sensing element are processed using the processing system shown in figure 22. (*Id.*, ¶¶[0077]-[0078].) I have created the demonstrative below based on this disclosure of *Isogai*, where the demonstrative combines figures 1 and 22 of *Isogai*. As the demonstrative shows, the output signal corresponding to the horizontal signal line 27a, which includes the output of the first green pixel Px3-1 and the output of the second green pixel Px2-2, is provided as a first input to the processing system shown in figure 22. Similarly, the output signal corresponding to the horizontal signal line 27b, which includes the output of the red pixel Px2-3 and the output of the blue pixel Px3-2, is provided as a second input to the processing system shown in figure 22.



(*Id.*, FIGs. 1, 22 (annotated).)

59. As shown in the demonstrative above, the outputs of the red and blue pixels on the horizontal signal line 27b are provided as the “B/R signal” to the analog-to-digital converter (AD) 81. (*Id.*, ¶[0079] (“The G signal has the same frequency as the signal output frequency of the solid-state image sensing element, and is **AD-converted** into the output signal in accordance with the timing.”) (emphasis added), ¶[0080] (“The second channel, in which the **B signal and the R signal** are output line-sequentially, is signal **processed in the same manner** as the first channel (G signal)”) (emphasis added).)

60. A person of ordinary skill in the art would have understood that AD blocks 80 and 81, which are further identified in the “Explanation of Reference Numerals” of *Isogai* as “80, 81 AD converter,” are analog-to-digital (A/D) converters that convert the outputs of the pixels into digital signals. Such an understanding is supported by the fact that the signals entering AD blocks 80, 81 are analog, whereas the outputs of the AD blocks 80, 81 are provided to, for example, delay elements (D flip-flops) 82, 83 and multiplexers 84, 85, which are digital circuit elements.

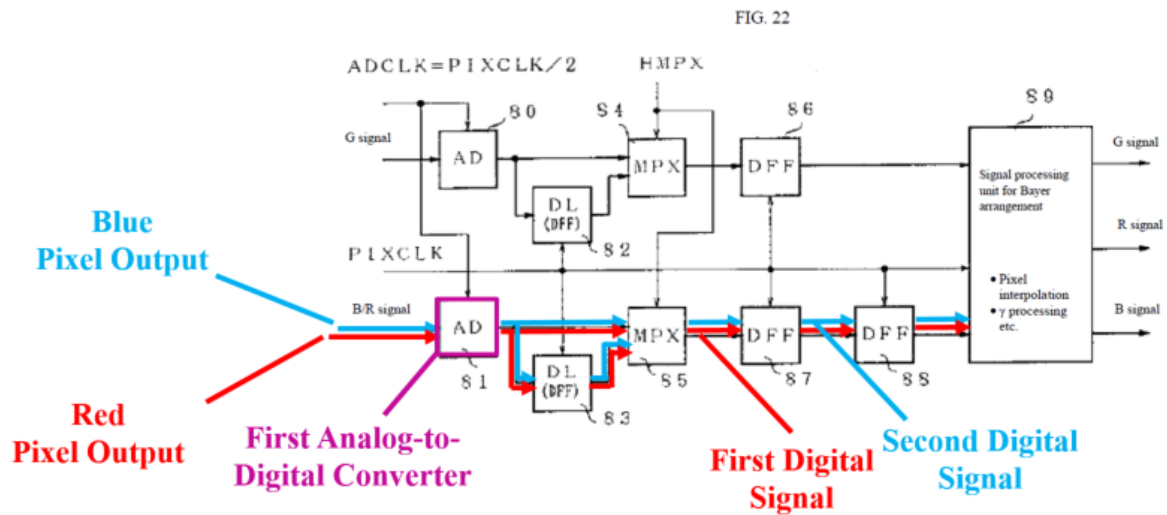
61. A person of ordinary skill in the art would also have understood that AD block 81 is “connected to the output of the red pixel” and “connected to the output of the blue pixel.” Figure 1 only includes column selection transistors TH1-

TH4 between the pixels and the analog to digital converters 80, 81. While such intervening column selection transistors are not shown in the '651 patent, some selection circuitry is necessarily positioned between the pixel outputs and A/D converters.

62. *Isogai* further discloses that the digital signals generated by the analog-to-digital converter 81 include a red digital signal (R signal) (“first digital signal”) and a blue digital signal (B signal) (“second digital signal”) that are “sequentially output” by the analog-to-digital converter 81. (*Id.*, ¶[0079] (“This apparatus output the G signal as the first channel, and **output the line sequential signals of R and B as the second channel.**”) (emphasis added), ¶[0080] (“The second channel, in which **the B signal and the R signal are output line-sequentially,** is signal-processed in the same manner as the first channel (G signal), and then delayed by another pixel by the DFF, and is sent to the signal processing unit 89.”) (emphasis added).) A person of ordinary skill in the art would have understood that when the row select signal 55c corresponding to the top row of pixels is asserted, the blue pixel output is provided to the vertical signal line 22b and horizontal signal line 27b and converted to the first digital signal by AD 81. (*Id.*) Similarly, when the row select signal 55b corresponding to the second row of pixels is asserted, the red pixel output is provided to the vertical signal line 22b and horizontal signal line 27b and converted to the

second digital signal by AD 81. (*Id.*) Thus, AD 81 will sequentially convert different red and blue pixel outputs into digital signals that are “sequentially output.” (*Id.*)

63. I have created the demonstrative below to show the general flow of the pixel outputs through the processing system of figure 22. The signal path for the first (red) and second (blue) digital signals includes D-flip flops 83, 87, and 88, and multiplexer 85, where such elements control the timing of the presentation of the first and second digital signals to the signal processing unit 89. (Ex. 1005, ¶¶[0079], [0080], FIG. 22.) The PIXCLK scanning clock controls the presentation of the red/blue digital pixel information to the processing block 89 by the D-flip flop (DFF) 88, whereas the HMPX signal selects which of the red/blue pixel digital signals that are sequentially output by AD 81 is forwarded to the DFF 87 using the multiplexer (MPX) 85.



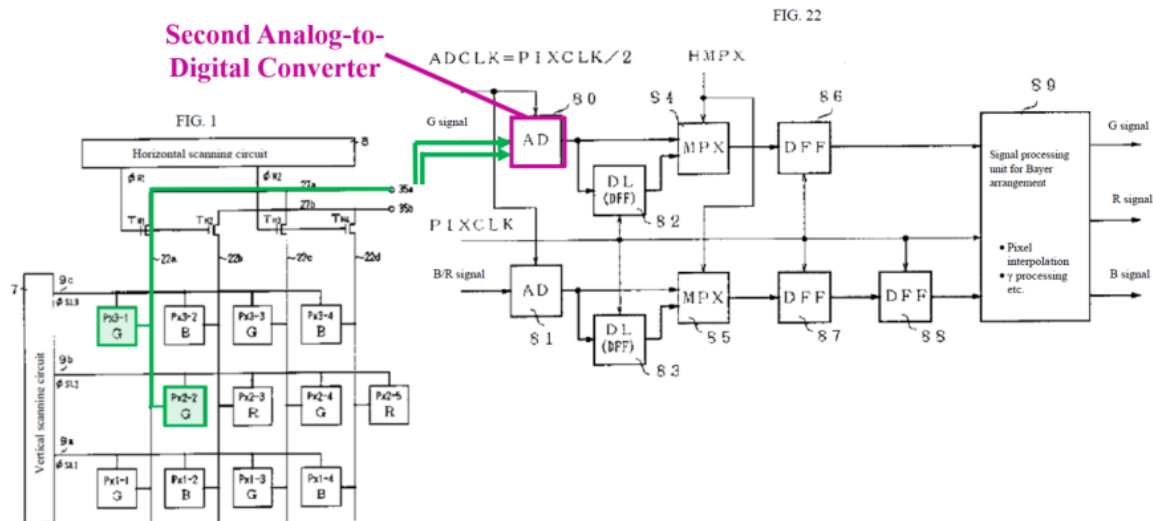
(Id., FIG. 22 (annotated).)

64. Therefore, in my opinion, the analog-to-digital converter 81 constitutes “a first analog-to-digital converter connected to the output of the red pixel for converting the output of the red pixel into a first digital signal and connected to the output of the blue pixel for converting the output of the blue pixel into a second digital signal” as recited in claim 1.

- g) **“a second analog-to-digital converter connected to the output of the first green pixel for converting the output of the first green pixel into a third digital signal and connected to the output of the second green pixel for converting the output of the second green pixel into a fourth digital signal; and”**

65. In my opinion, *Isogai* discloses this feature. As discussed above in Section IX.A.1(a), the combinations of the solid-stage image sensing element shown in figure 1 of *Isogai* with the processing system shown in figure 22 includes analog-

to-digital converters 80, 81 that convert the analog outputs of the pixels into digital signals. (See my discussion above in Section IX.A.1(a).) Moreover, as also discussed above in Section IX.A.1(f) and shown in figure 22, the outputs of the green pixels are provide to the analog-to-digital converter (AD) 80. (*Id.*; Ex. 1005, FIG. 22.) Just as the analog-to-digital converter 81 converts the red and blue pixel outputs from analog signals to digital signals, the analog-to-digital converter 80 converts the analog outputs of the first and second green pixels to digital signals. (See my discussion above in Section IX.A.1(f); *see also* Ex. 1005, ¶[0079] (“The G signal has the same frequency as the signal output frequency of the solid-state image sensing element, and is **AD-converted** into the output signal in accordance with the timing.”) (emphasis added), FIGs. 1, 3, 22.)

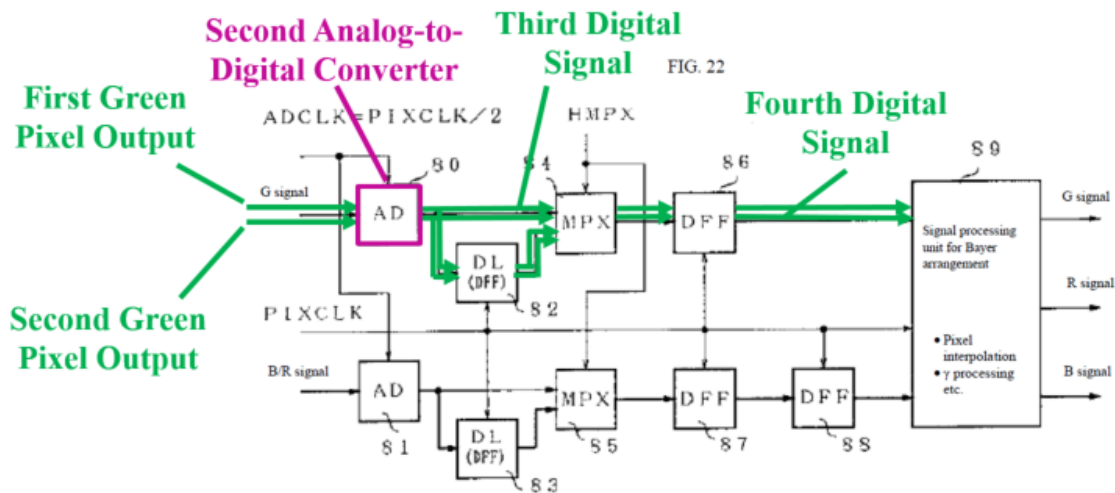


(*Id.*, FIGs. 1, 22 (annotated).)

66. A person of ordinary skill in the art would also have understood that AD block 80 is “connected to the output of the first green pixel” and “connected to the output of the second green pixel”. (*See* my discussion above in Section IX.A.1(f).)

67. *Isogai* further discloses that the digital signals generated by the analog-to-digital converter 80 include first and second green digital signals (G signal) (“third digital signal” and “fourth digital signal”). (*Id.*, ¶[0079] (“This apparatus output **the G signal as the first channel**, and output the line sequential signals of R and B as the second channel. The G signal . . . is AD-converted into the output signal” where the “A/D conversion frequency is 1/2 of PIXCLK.”) (emphasis added).) A person of ordinary skill in the art would have understood that when the row select signal 55c corresponding to the top row of pixels is asserted, the first green pixel output is provided to the vertical signal line 22a and horizontal signal line 27a and converted to the third digital signal by AD 80. Similarly, when the row select signal 55b corresponding to the second row of pixels is asserted, the second green pixel output is provided to the vertical signal line 22a and horizontal signal line 27a and converted to the fourth digital signal by AD 80. Thus, AD 80 will sequentially convert different green pixel outputs into two digital signals. (*Id.*, ¶[0079], FIG. 22.)

68. I have annotated figure 22 below to show the general flow of the pixel outputs through the processing system. Note that the signal path for the third (first green) and fourth (second green) digital signals after analog-to-digital conversion includes D-flip flops 82 and 86 as well as multiplexer 84, where such elements control the timing of the presentation of the third and fourth digital signals to the signal processing unit 89. (*Id.*) The PIXCLK scanning clock controls the presentation of the green digital pixel information to the processing block 89 by the D-flip flop (DFF) 86, whereas the HMPX signal selects which of the first/second green pixel digital signals that are sequentially output by AD 81 is forwarded to the DFF 86 using the multiplexer (MPX) 84.



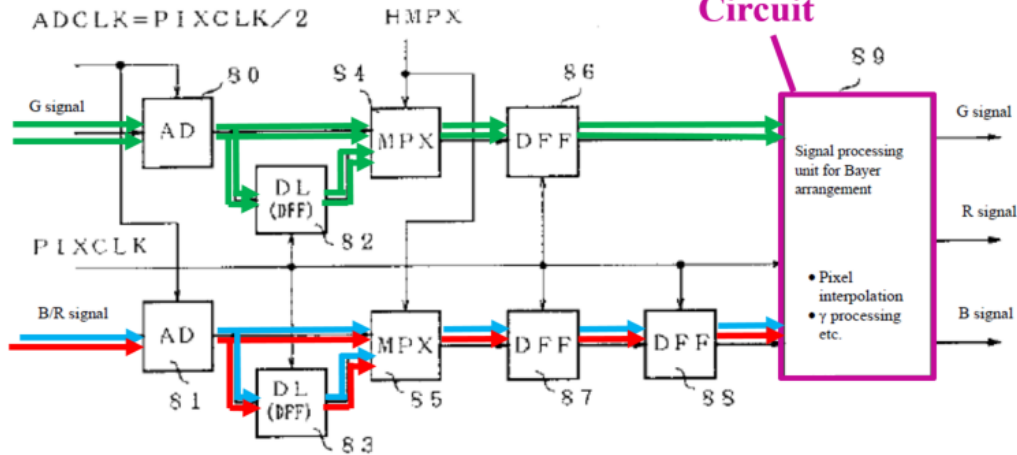
(*Id.*, FIG. 22 (annotated).)

69. Therefore, in my opinion, the analog-to-digital converter 80 shown in the annotated demonstrative above constitutes “a second analog-to-digital converter connected to the output of the first green pixel for converting the output of the first green pixel into a third digital signal and connected to the output of the second green pixel for converting the output of the second green pixel into a fourth digital signal” as recited in claim 1.

h) **“a color interpolation circuit for combining the first, second, third and fourth digital signals.”**

70. In my opinion, *Isogai* discloses this feature. For example, *Isogai* discloses a signal processing unit 89 that combines the first, second, third, and fourth digital signals (“a color interpolation circuit for combining the first, second, third and fourth digital signals”). As discussed above in Sections IX.A.1(f)-(g), the analog-to-digital converters 80, 81 convert the outputs of red, blue, first green, and second green pixels into the first, second, third, and fourth digital signals, respectively. (See my discussion above in Sections IX.A.1(f)-(g).) *Isogai* further discloses that the first, second, third, and fourth digital signals are provided to the signal processing unit 89 (“color interpolation circuit”). (Ex. 1005, ¶¶[0077]-[0080], FIG. 22.)

FIG. 22 **Color Interpolation Circuit**



(*Id.*, FIG. 22 (annotated).)

71. *Isogai* discloses that:

The second channel, in which the B signal and the R signal are output line-sequentially, is signal-processed in the same manner as the first channel (G signal), and then delayed by another pixel by the DFF 88, and is sent to the signal processing unit 89. The **signal processing unit 89** is a signal processing unit for Bayer arrangement, and **performs signal processing such as R / B color separation, pixel interpolation of empty grid points of each RGB color and λ processing to output RGB color signals with all pixels having RGB color signal.**

(*Id.*, ¶[0080] (emphasis added).)

72. A person of ordinary skill in the art would have understood that the “pixel interpolation of empty grid points each RGB color” performed by the signal processing unit includes processing that combines the digital signals corresponding to the outputs of the pixels in a manner consistent with the disclosure of the ’651 patent. (*Id.*, ¶[0078] (“The signal processing apparatus performs color imaging using the solid-state image sensing element of the present invention in which a color filter is arranged in each pixel as described above, and a signal output and distributed into two terminals and converted to the time-series signal corresponding to pixel position.”); Ex. 1001, 5:13-25.) For example, a person of ordinary skill in the art would have understood that *Isogai*’s disclosure of “pixel interpolation of empty grid points of each RGB color . . . to output RGB color signals with all pixels having RGB color signal” would include combining color data corresponding to neighboring pixels in order to determine the pixel color data for each pixel in the array. (Ex. 1005, ¶[0080]; Ex. 1001, 5:13-25.)

73. A person of ordinary skill in the art would have understood that *Isogai*’s disclosure of “pixel interpolation” would include combining color data corresponding to neighboring pixels in order to determine the pixel color data for the empty grid points as described by the ’651 patent:

Color interpolation is used to determine the amount of red, green and blue light incident on each pixel. This process averages the color outputs of appropriate neighboring pixels to approximate each pixel's unknown color data. For example, for any given blue pixel 108, the process of color interpolation determines the green content of the pixel 108 by averaging the outputs of the green pixels 110, 112 above, below, to the left and to the right of the pixel 108. Similarly, the red content of the pixel 108 is determined by averaging the outputs of the red pixels 106 diagonally adjacent to the pixel 108. The color interpolation circuit 120 performs the interpolation for each pixel 102 to determine the color of the pixel 102.

(Ex. 1001, 5:13-25.)

74. Therefore, in my opinion, *Isogai*'s signal processing unit 89 constitutes "a color interpolation circuit for combining the first, second, third and fourth digital signal" as recited in claim 1.

2. Claim 18

a) "An imaging method comprising:"

75. I understand that "[an] imaging method, comprising" is the preamble of claim 18. I have been asked to assume that the preamble is limiting. In my opinion, *Isogai* discloses this feature. As discussed above in Section IX.A.1(a), *Isogai* discloses a solid-state image sensing element and a system for processing the

signal outputs from the solid-state imaging sensing element that together form an imaging device, where the operation of such an imaging device, which includes the capture and processing of pixel data, constitutes an “imaging method.” (See my analysis above in Section IX.A.1(a).)

- b) **“converting an output of a red pixel into a first digital signal using a first analog-to-digital converter;”**
- c) **“converting an output of a blue pixel into a second digital signal using the first analog-to-digital converter;”**

76. In my opinion, *Isogai* discloses these limitations. As I discussed above in Sections IX.A.1(b)-(c), *Isogai* discloses a red pixel and a blue pixel, each of which has a corresponding “output.” (See my analysis above in Sections IX.A.1(b)-(c).) As I also discussed above in Section IX.A.1(f), the outputs of the red and blue pixels are converted to first and second digital signals, respectively, by a first analog-to-digital converter. (See my analysis above in Section IX.A.1(f).)

- d) **converting an output of a first green pixel into a third digital signal using a second analog-to-digital converter;”**
- e) **“converting an output of a second green pixel into a fourth digital signal using the second analog-to-digital converter; and;”**

77. In my opinion, *Isogai* discloses these limitations. As I discussed above in Sections IX.A.1(d)-(e), *Isogai* discloses a first and second green pixel, each of

which has a corresponding “output.” (See my analysis above in Sections IX.A.1(d)-(e).) As I also discussed above in Section IX.A.1(g), the outputs of the first and second green pixels are converted to third and fourth digital signals, respectively, by a second analog-to-digital converter. (See my analysis above in Section IX.A.1(g).)

f) combining the first, second, third and fourth digital signals using a color interpolation circuit.”

78. In my opinion, *Isogai* discloses this limitation. As I discussed above in Section IX.A.1(h), *Isogai* discloses “combining the first, second, third and fourth digital signals using a color interpolation circuit.” (See my analysis above in Section IX.A.1(h).)

B. *Isogai* in Combination with *Neter* Discloses or Suggests the Features of Claims 2-5 and 19-22

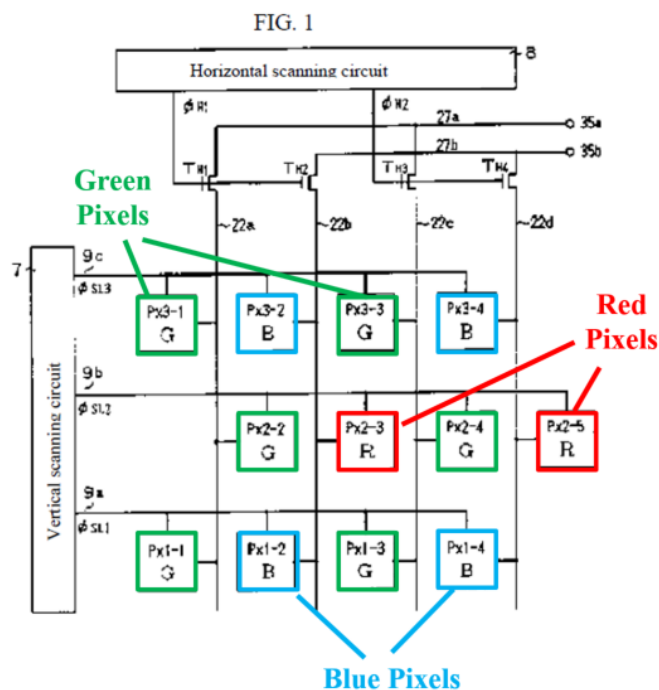
1. Claim 2

a) “The solid stage imaging device of claim 1, further comprising an error compensation circuit for correcting a gain of one of the output of the red pixel, the output of the blue pixel, the output of the first green pixel and the output of the second green pixel.”

79. In my opinion, *Isogai* in combination with *Neter* discloses or suggests this feature. While the '651 patent shows the error compensation circuit operating on digital signals output from the A/D converters (Ex. 1001, FIGs. 1-3), claim 2 indicates that the error compensation circuit corrects a gain of one of the outputs of the red, blue, and first and second green pixels, where those outputs are the analog

signals that have not yet been converted to digital signals by the A/D converters. I have been asked to assume that, for purposes of the present analysis, the scope of claim 2 includes correcting a gain of one of the analog outputs of the red, blue, first green, and second green pixels, which is consistent with the language of claim 2. With such an assumption in mind, *Isogai* in combination with *Neter* discloses or suggests this feature.

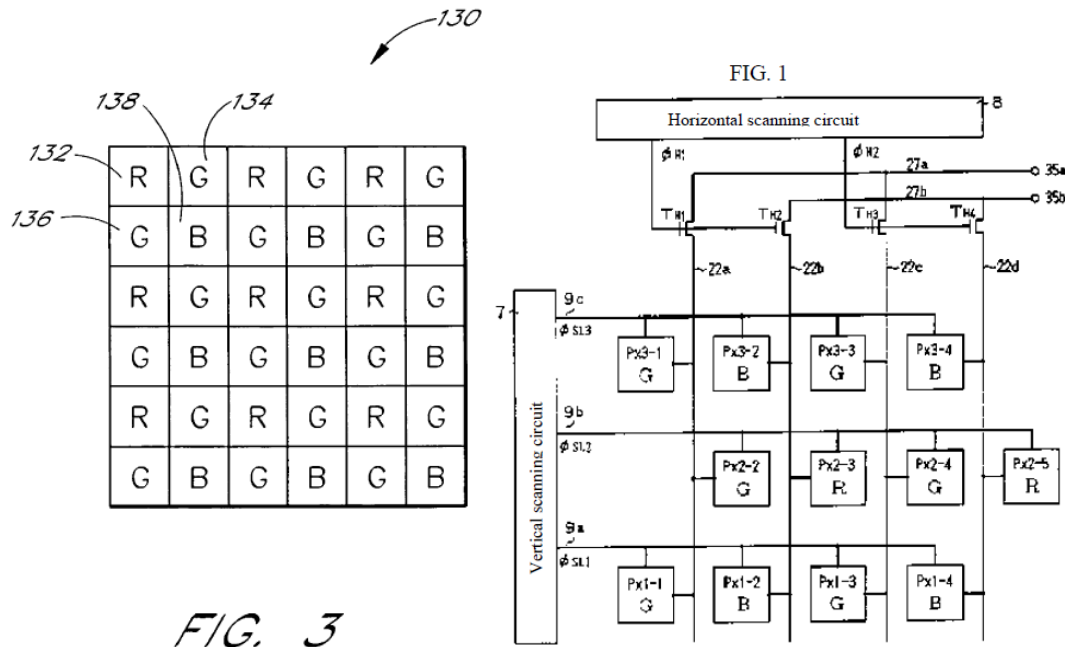
80. As I discussed above, *Isogai* discloses a solid state imaging device that includes a solid state image sensing element according to a first embodiment disclosed in *Isogai*. (See my discussion above in section IX.A.1(a).)



(Ex. 1005, FIG. 1 (annotated).)

81. The embodiment of figure 1 of *Isogai* does not explicitly disclose an error compensation circuit for correcting a gain of the analog signals output by the red, blue, and green pixels. However, as I discuss below, *Neter* discloses gain correction of the analog signal outputs from the pixels, and a person of ordinary skill in the art would have been motivated in view of *Neter* to utilize such gain correction in the solid state imaging device that includes the solid state image sensing element corresponding to the first embodiment of *Isogai*.

82. *Neter*, like *Isogai*, describes circuits for processing imaging pixel sensor elements. (Ex. 1007, 2:60-62 (“The present invention is directed to imaging methods and systems for flexibly addressing and processing imaging pixel sensor elements.”); 3:4-16.) Both *Neter* and *Isogai* describe image sensing devices that include red, blue, and green pixels. (*Id.*, 3:12-14, FIG. 3.) Indeed, also like *Isogai*, *Neter* discloses pixel elements arranged in the Bayer pattern scheme. (*Id.*, 3:12-14, FIG. 3; Ex. 1004, ¶[0028], FIG. 1.) Therefore, a person of ordinary skill in the art implementing the image sensing device of *Isogai* would have had reason to look to *Neter*.



(Ex. 1007, FIG. 3 (left); Ex. 1005, FIG. 1 (right).)

83. *Neter* discloses that conventional imaging devices include a process for reconstructing the color components of the image that includes color interpolation, which is typically done after analog-to-digital conversion, which is consistent with the disclosure of *Isogai*. (Ex. 1007, 1:12-49; see my discussion above in Section IX.A.1(h).)

84. *Neter* also discloses that in addition to such color interpolation, imaging devices also perform color compensation, which involves adjusting the signals for different colored pixels as the pixel elements may be more responsive to one color of light in comparison to another color of light:

Conventional imaging devices also require color compensation for difference in the response of the various color filters and for variations within the integrated circuit sensor array, such as process, materials, temperature or manufacturing. For example, when the primary color scheme is used, **the response of an element that absorbs red light may be different than an element that absorbs blue light even when illuminated by light of equal red and blue luminosity levels.** When exposed to a flat light image having equal intensity and chromaticity levels through, **typical CMOS or CCD arrays may generate analog signals having significant magnitude variations for the different color components.** According, if the analog signals are used to reproduce the original image, the reproduced image colors will not match the original colors.

(Ex. 1007, 1:50-64 (emphasis added).)

85. *Neter* further discloses performing such color compensation with separate amplification of different colored pixel outputs using programmable gain amplifiers:

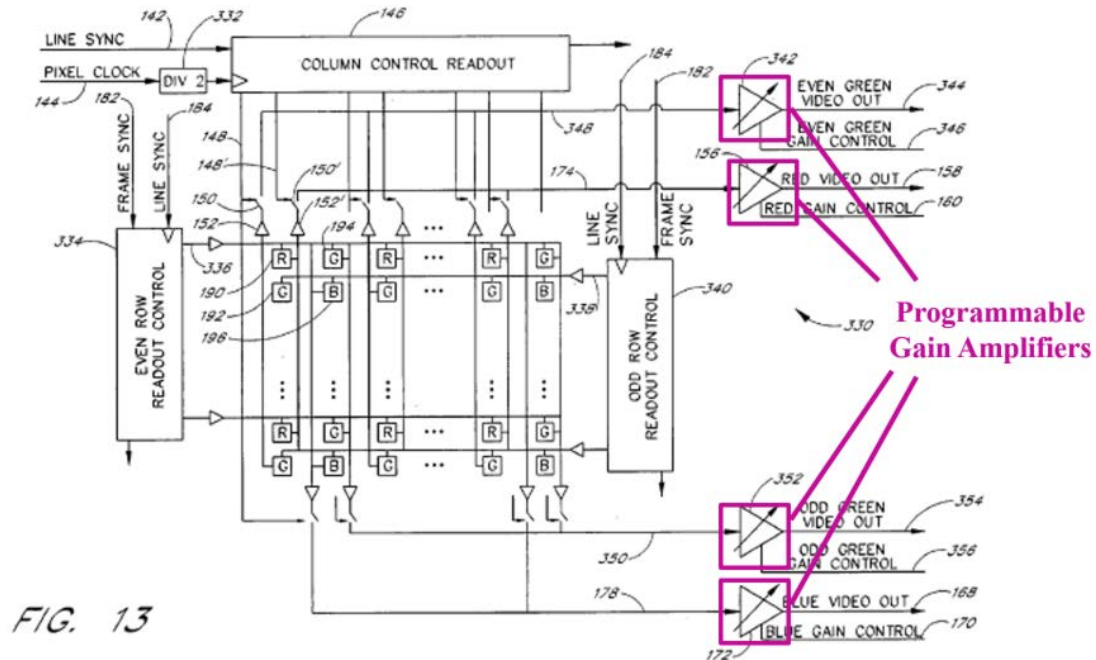
In one embodiment, the imaging system with **color compensation** includes a control circuit that provides **four output paths that can be amplified separately via one or more stages of programmable gain amplifiers** and/or

summing amplifiers. The control circuit allows four independent readouts for even rows, odd rows, even columns and odd columns, thus providing separate and/or simultaneous output paths for Red, Green and Blue pixels.

For example, one embodiment of the imaging system employs a readout control that provides outputs for the Red pixel, the Blue pixel, and the two Green pixels. Thus the imaging system allows further gain compensation for a Green pixel that resides in an even column compared to a Green pixel that resides in an odd column. The four signals are then amplified via four corresponding programmable gain amplifiers. The readout control logic ensures that the row and column switches are closed in the appropriate sequence.

(Ex. 1007, 4:19-36 (emphasis added).)

86. For example, figure 13 of *Neter*, which I have annotated below, discloses a color imaging system 330 that includes color compensation using such programmable gain amplifiers. (*Id.*, 13:39-41, FIG. 13.)



(*Id.*, FIG. 13 (annotated).)

87. Figure 14 of *Neter* shows one embodiment for analog color correction process performed by the system shown in figure 13, where the different amplifiers are used to amplify the signals corresponding to the red, green, and blue pixels. (*Id.*, 14:5-22, FIG. 14.) *Neter* further discloses that different transfer functions can be implemented by the programmable gain amplifiers such that “each color can be optimized independently for maximum dynamic range.” (*Id.*, 4:51-55; *see also id.*, 13:55-14:4.)

88. *Neter* further discloses that the disclosed imaging systems provide flexible processing where “the imaging system may provide on-the-fly color

interpolation, color compensation (also called color correction, color maximization or white balance) **and/or** fixed pattern noise reduction.” (*Id.*, 7:24-32, emphasis added.) Therefore, a person of ordinary skill in the art would have understood that while *Neter* discloses circuits and methods for on-the-fly color interpolation, color compensation, and fixed pattern noise reduction, it also discloses that all three need not be employed together. Such a person of ordinary skill in the art would have understood, for example, that on-the-fly color compensation could be applied to the analog outputs of the pixels while still performing color interpolation after digital-to-analog conversion of the pixel outputs to form digital signals.

89. Given the disclosure of a color compensation in *Neter*, a person of ordinary skill in the art would have been motivated to combine the teachings of *Isogai* and *Neter* such that at least one of the output signals for the red, blue, first green, and second green pixels identified above with respect to claim 1 are amplified by a programmable gain amplifier in order to provide color compensation for the image sensing device. A person of ordinary skill in the art would have been motivated to do so because, as disclosed by *Neter*, such color-specific amplification compensates for differences in the response of various color filters and variations in the sensor array resulting from variations in process, materials, temperature, and manufacturing:

The color compensation process compensates for differences in the response of various color filters and variations within the integrated circuit sensor array, such as process, materials, temperature or manufacturing. The color compensation process of the present invention improves color dynamic range, decreases computations and hardware and improves speed of operation. The color compensation process of the present invention is advantageously performed in the analog domain before analog-to-digital conversion.

(Ex. 1007, 13:30-39.)

90. Moreover, a person of ordinary skill in the art would have understood that performing such color compensation – in either the analog or the digital domain - was commonplace in image processors at the time of the alleged invention. Such an understanding is supported by *Loinaz*², which discloses such color compensation (“white balancing”) in order to align the output levels of the different colored pixels. (Ex. 1010, 2094 (“To achieve white balance, it is evident from Fig. 4 that the outputs of the blue and green pixels must be amplified with respect to the outputs of the red pixels.”), 2095 (“[T]hree separate and independent gains are used for pixels covered

² I refer to *Loinaz* to demonstrate the knowledge of a person of ordinary skill in the art at the relevant time.

by red, green, and blue filters, respectively. White balancing can therefore be performed in the analog domain.”).)

91. Accordingly, such a person of ordinary skill in the art would have combined the teachings of *Isogai* and *Neter* such that the output of at least one of the red, blue, first green, and second green pixels in *Isogai* is amplified to provide color compensation in order to, for example, improve color dynamic range and white balancing. In such an *Isogai-Neter* combination, a person of ordinary skill in the art would have understood that such color compensation corresponds to “correcting a gain of one of the output of the red pixel, the output of the blue pixel, the output of the first green pixel and the output of the second green pixel” as recited in claim 2 of the ’651 patent. Moreover, such a person of ordinary skill in the art would have understood that the programmable gain amplifiers and related circuitry to support such color compensation, which *Neter* also refers to as “color correction,” would constitute an “error correction circuit” that, as recited in claim 2, performs such gain correction.

92. Including color compensation circuitry like that disclosed in *Neter* in the imaging device of *Isogai* would have involved nothing more than the combination of known prior art elements (the image array with pixel outputs of *Isogai* with the amplifiers of *Neter* to compensate for gain differentials between different colored

pixels) using known circuit design methods, where each element performs the same function described in *Neter* and *Isogai*, to achieve the predictable result of an imaging device that is improved to provide color compensation. Both *Isogai* and *Neter* describe circuits for processing imaging pixel sensor elements, but a person of ordinary skill in the art would have appreciated that *Neter* describes additional circuitry not found in *Isogai* for color compensation. Therefore, such a skilled person would have recognized that *Neter*'s teachings relating to color compensation could be applied to *Isogai*'s system in a similar way. As also discussed above, such a skilled person would have been encouraged to implement such color compensation in *Isogai*'s system to provide similar color correction capabilities to improve overall system performance, including improved image quality and white balancing.

93. Including such color compensation circuitry in *Isogai*'s imaging device would have been straightforward for a skilled person to implement given such a person's knowledge and the disclosure in *Neter*. For example, the combination would have required nothing more than adding well-known and widely available amplifiers for color compensation to *Isogai*'s system, which, as evidenced by *Neter* and *Loinaz*, were commonly used for color correction at the time. Moreover, *Isogai*'s system would have continued to operate as described in *Isogai* with the added circuitry to correct gain differentials for the different colors as necessary.

94. Furthermore, a person of ordinary skill in the art would have understood how to make any needed modifications in order to ensure that the programmable gain amplifiers would operate correctly in the imaging device of *Isogai*. For example, if needed, providing selection circuitry to route the red, blue, first green, and second green pixels to the color compensation circuitry, as well as circuitry for recombining the outputs of that circuitry to provide the proper sequence of signals to the analog-to-digital converters as disclosed in *Isogai*, would have been routine for such a person of ordinary skill in the art. Similarly, if additional control circuitry is required to provide the control information to the programmable gain amplifiers, such circuitry would also have been within the capability of a person of ordinary skill in the art. It is my opinion that any modifications necessary to ensure that the color compensation circuitry would work in the *Isogai* imaging device would have been apparent to, and within the capabilities of, a person of ordinary skill in the art.

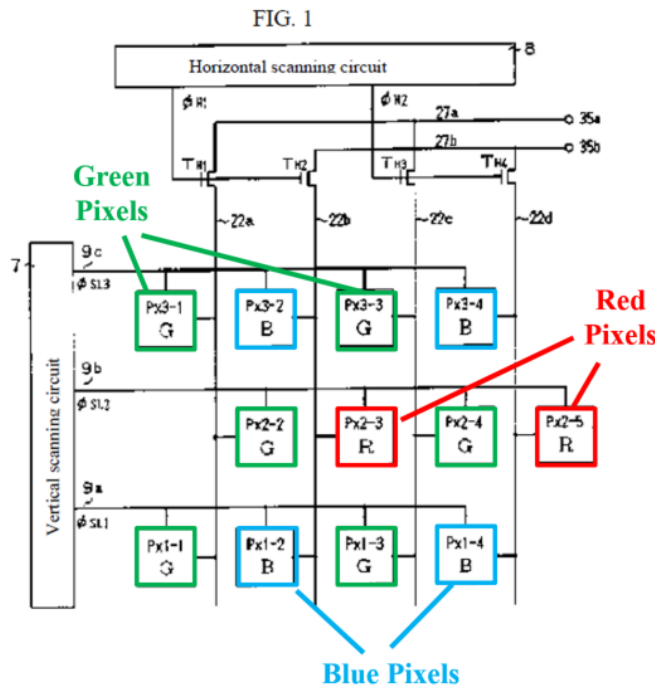
2. Claim 3

- a) **“The solid stage imaging device of claim 1, further comprising an error compensation circuit for correcting a fixed pattern noise offset from one of the output of the red pixel, the output of the blue pixel, the output of the first green pixel and the output of the second green pixel.”**

95. In my opinion, *Isogai* in combination with *Neter* discloses or suggests this feature. As I discussed above in Section IX.B.1, while the '651 patent shows

the error compensation circuit operating on digital signal outputs from the A/D converters (Ex. 1001, FIGs. 1-3), claim 3 indicates that the error compensation circuit corrects a fixed pattern noise offset from one of the outputs of the red, blue, and first and second green pixels, where those outputs are the analog signals that have not yet been converted to digital signals by the A/D converters. I have been asked to assume that, for purposes of the present analysis, the scope of claim 3 includes correcting a fixed pattern noise offset from one of the analog outputs of the red, blue, first green, and second green pixels. With such an assumption in mind, *Isogai* in combination with *Neter* discloses this feature.

96. As I discussed above, *Isogai* discloses a solid state imaging device that includes a solid state image sensing element according to a first embodiment corresponding to figure 1. (See my discussion above in Section IX.A.1(a).)



(Ex. 1005, FIG. 1 (annotated).)

97. The embodiment of figure 1 of *Isogai* does not explicitly disclose an error compensation circuit for correcting a fixed pattern noise offset from one of the analog signals output by the red, blue, and green pixels. However, as I discuss below, *Neter* discloses correcting a fixed pattern noise offset in the analog signal outputs from red, blue, and green pixels, and a person of ordinary skill in the art would have been motivated in view of *Neter* to utilize such fixed pattern noise offset correction in the solid state imaging device of *Isogai* that includes the solid state image sensing element corresponding to the first embodiment.

98. As I discussed above in section IX.B.1, *Neter*, like *Isogai*, describes circuits for processing imaging pixel sensor elements, and a person of ordinary skill in the art implementing an image sensing device as disclosed in *Isogai* would have had reason to look to *Neter*. (See my discussion above in Section IX.B.1.) *Neter* discloses circuitry and methods for addressing fixed pattern noise corresponding to pixel outputs in an array of colored pixels like that of *Isogai* (e.g. a Bayer pattern):

Another aspect of the invention relates to a fixed pattern noise reduction apparatus and process. The fixed pattern noise reduction process reduces noise related to pixel-to-pixel variation. This variation is primarily due to dark current leakage, which may be integrated together with the signal and hence contaminate the signal. The dark current leakage may be due to thermal generation in the neutral bulk material, in the depletion region and due to surface states. The dark current level may vary between pixels and may be particularly noticeable between columns due to column buffers.

The fixed pattern noise reduction process of the present invention allows increased dynamic range (high image quality), high speed of operation and reduced computational complexity. The fixed pattern noise reduction of the present invention is advantageously

performed in the analog domain before an analog-to-digital conversion.

(Ex. 1007, 5:1-17, 15:53-16:2.)

99. Therefore, *Neter* discloses that fixed pattern noise reduction is used in imaging systems in order to address noise related to pixel-to-pixel variation, which can be caused by, for example, dark current in the imaging array. (*Id.*) Figure 20 of *Neter* discloses a color imaging system that supports fixed pattern noise reduction. (*Id.*, 16:3-16, FIG. 20.)

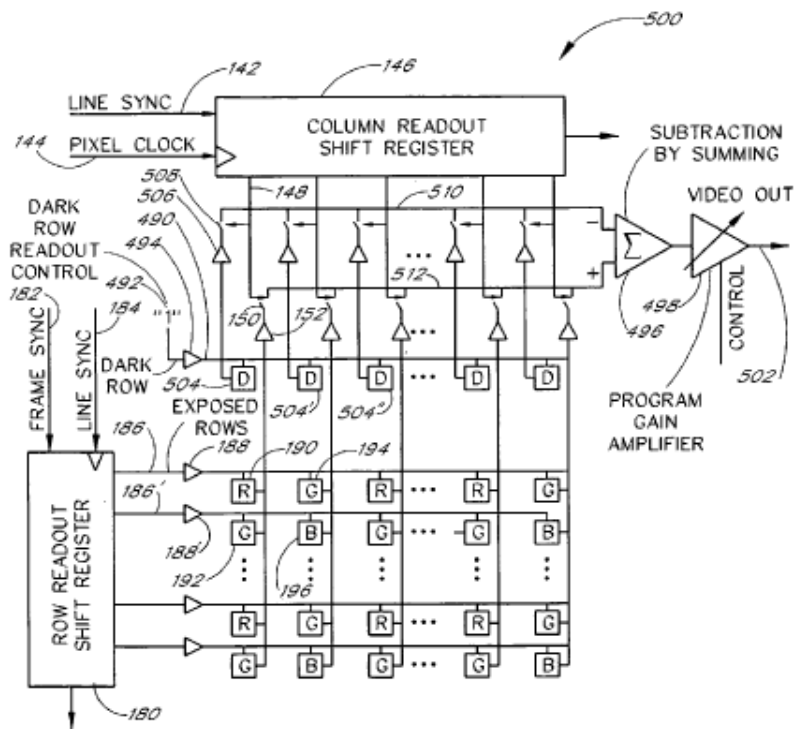


FIG. 20

(*Id.*, FIG. 20.)

100. As shown in figure 20, a dark row of pixels is added with an opaque mask layer such that they are not exposed to light. (*Id.*, 16:17-19.) In order to subtract out the dark current, two pixels are read out from the same column, where one pixel is from the dark row and the other is from one of the exposed rows. (*Id.*, 16:30-34.) “The dark pixel value is then subtracted from the exposed pixel value by the summing amplifier 496, thereby providing fixed pattern noise reduction.” (*Id.*, 16:34-37.)

101. As discussed above with respect to claim 2, *Neter* further discloses that the imaging system provides flexible processing where “the imaging system may provide on-the-fly color interpolation, color compensation (also called color correction, color maximization or white balance) **and/or** fixed pattern noise reduction.” (*Id.*, 7:24-32, emphasis added.) Therefore, a person of ordinary skill in the art would have understood that while *Neter* discloses circuits and methods for on-the-fly color interpolation, color compensation, and fixed pattern noise reduction, it further discloses that all three need not be employed together and one or more can be used in a particular embodiment. Such a person of ordinary skill in the art would have understood, for example, that on-the-fly fixed pattern noise reduction could be applied to the analog outputs of the pixels while still performing color compensation

and/or color interpolation after digital-to-analog conversion of the pixel outputs to form digital signals.

102. Given the disclosure of a fixed pattern noise reduction in *Neter*, a person of ordinary skill in the art would have been motivated to combine the teachings of *Isogai* and *Neter* such that at least one of the output signals for the red, blue, first green, and second green pixels in *Isogai* has an offset corresponding to fixed pattern noise corrected. A person of ordinary skill in the art would have been motivated to do so because, as disclosed by *Neter*, fixed pattern noise reduction provides advantages, including less contamination of the image signal, thereby providing increased dynamic range and higher image quality. (*Id.*, 15:55-57, 15:64-67.)

103. Moreover, a person of ordinary skill in the art would have understood, as evidenced by *Neter*, that performing such fixed pattern noise reduction – in either the analog or the digital domain - was commonplace in image processors at the time of the alleged invention.

104. Including fixed pattern noise reduction circuitry like that disclosed in *Neter* in the imaging device of *Isogai* would have involved nothing more than the combination of known prior art elements (the image array with pixel outputs of *Isogai* with the dark current removal circuitry of *Neter* to compensate for fixed

pattern noise) using known circuit design methods, where each element performs the same function described in *Neter* and *Isogai*, to achieve the predictable result of an imaging device that is improved have higher image quality because of reduced noise. As I discussed above, both *Isogai* and *Neter* describe circuits for processing imaging pixel sensor elements, but *Neter* describes additional circuitry not found in *Isogai* for dark current removal. Therefore, a skilled person would have recognized that *Neter*'s teachings relating to noise reduction could be applied to *Isogai*'s system in a similar way. As I also discussed above, such a skilled person would have been encouraged to implement such dark current removal in *Isogai*'s system to provide similar noise reduction capabilities to improve overall system performance, including providing higher image quality.

105. Including such fixed pattern noise reduction circuitry in *Isogai*'s imaging device would have been straightforward for a skilled person to implement given such a person's knowledge and the disclosure of *Neter*. For example, the combination would have required nothing more than adding well-known, straightforward circuitry to subtract dark current to *Isogai*'s system, where such dark current removal circuitry, as evidenced by *Neter*, was commonly used for fixed pattern noise reduction at the time. Such a combination would not have detracted

from the overall functionality of *Isogai*'s system, which would have continued to operate as described in *Isogai* with the added circuitry to reduce fixed pattern noise.

106. A person of ordinary skill in the art would have understood such color compensation circuitry to constitute an “an error compensation circuit for correcting a fixed pattern noise offset from one of the output of the red pixel, the output of the blue pixel, the output of the first green pixel and the output of the second green pixel” as recited in claim 3 of the '651 patent.

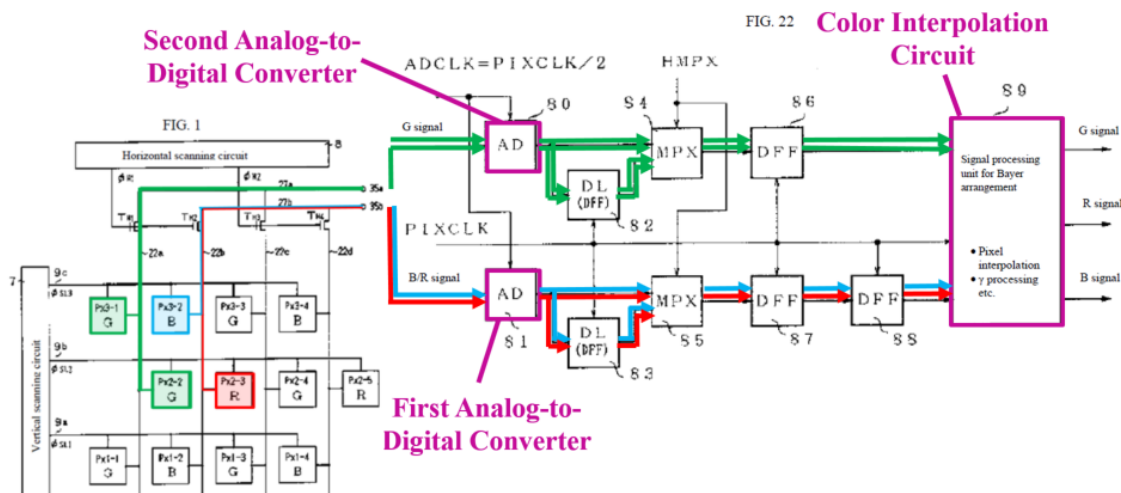
107. Moreover, a person of ordinary skill in the art would have understood how to make any needed modifications in order to ensure that the fixed pattern noise reduction circuitry would operate correctly within the imaging device of *Isogai*. For example, if needed, including multiple subtraction circuits and providing selection circuitry to route the red, blue, first green, and second green pixels to the appropriate subtraction circuit in order to maintain the desired presentation of the outputs of the red and blue pixels to a first A/D converter and the outputs of the first and second green pixels to a second A/D converter would have been routine for such a person of ordinary skill in the art. Moreover, if additional control circuitry is required to provide the control information to the fixed pattern noise reduction circuitry, that would also have been within the capability of a person of ordinary skill in the art. It is my opinion that any modifications necessary to ensure that the fixed pattern noise

reduction circuitry would work in Isogai's imaging device would have been apparent to, and within the capabilities of, a person of ordinary skill in the art.

3. Claim 4

- a) “The solid stage imaging device of claim 1 further comprising a first chip and a second chip, wherein the red pixel, the blue pixel, the first green pixel, the second green pixel, the first analog-to-digital converter and the second analog-to-digital converter are disposed on the first chip and the color interpolation circuit is disposed on the second chip.”

108. In my opinion, *Isogai* in combination with *Neter* discloses or suggests these features. As I discussed above in Section IX.A.1(a), *Isogai* discloses a solid state imaging device that includes a solid state image sensing element according to the first embodiment in combination with the processing system shown in figure 22. (See my discussion above in section IX.A.1(a).)



(*Id.*, FIGs. 1, 22 (annotated).)

109. *Isogai* does not explicitly disclose that that the red pixel, the blue pixel, the first green pixel, the second green pixel, the first analog-to-digital converter, and the second analog-to-digital converter are disposed on a first chip and the color interpolation circuit is disposed on a second chip as recited in claim 4. However, including the pixels and analog-to-digital converters on a first chip and associated color interpolation circuitry on a second chip is disclosed by *Neter*, and a person of ordinary skill in the art would have been motivated in view of *Neter* to implement the recited components in *Isogai* on two separate chips as recited in claim 4.

110. As I discussed above in section IX.B.1, *Neter*, like *Isogai*, describes circuits for processing imagining pixel sensor elements and a person of ordinary skill in the art implementing the image sensing device of *Isogai* would have had reason to look to *Neter*. (See my discussion above in Section IX.B.1.)

111. *Neter* discloses that the disclosed imaging system, which includes red, blue, and green pixels, analog-to-digital converters, and additional processing circuitry like a color interpolation circuit can be implemented on one or more chips. For example, *Neter* discloses that “[t]he exemplified imaging systems described below with reference to FIGs. 1-23 use a CMOS integrated circuit, an array of pixels organized in a rectangle matrix, and a color filter with a primary color system (RGB)

in Bayer color pattern.” (Ex. 1007, 7:33-37.) *Neter* further discloses that different additional components, including analog-to-digital converters and color interpolation circuitry, may be included on the same integrated circuit as the array of pixels. (*Id.*, 5:47-52 (“The imaging system in accordance with the present invention may also include additional **on-chip or off chip** amplification stages, **analog-to-digital conversion units**, memory units and various other **signal processing blocks.**”) (emphasis added), 7:48-53 (“The imaging system may also include **either on-chip**, as is possible with CMOS integrated circuit imaging devices, **or off-chip**, as is the case with CCD integrated circuit imaging devices, amplification stages, **analog to digital conversion units**, memory units and various other signal processing blocks.”), 7:55-63 (“In one embodiment, the color interpolation system, the color compensation system and/or the fixed pattern noise reduction system reside together with the sensor array in the same chip, such as in a CMOS integrated circuit color imaging device. In another embodiment, the color interpolation system, the color compensation system **and/or** the fixed pattern noise reduction system reside in a separate companion chip, such as in a CCD integrated circuit imaging device.”) (emphasis added), 3:1-3.)

112. Given *Neter’s* disclosure of various image processing system components being included either on the same chip as the pixel array or on another

chip separate from the pixel array, a person of ordinary skill in the art would have been motivated to combine the teachings of *Neter* and *Isogai* such that, for some embodiments, *Isogai's* imaging device would include the analog-to-digital converters on the same chip as the red, blue, and green pixels, whereas the color interpolation circuitry is on a separate chip. A person of ordinary skill in the art would have been motivated to do so because, while integration may be desirable, in some embodiments, the complexity of the color interpolation circuitry may require significant hardware and software that would be better implemented on a separate chip. For example, *Neter* discloses:

Because each pixel is only capable of detecting a single color, conventional imaging devices require a process by which all of the color components are reconstructed for each pixel in order to maintain the original unfiltered array resolution. To reconstruct the color components, convention imaging devices use a process of color interpolation that is performed after an analog signal associated with each pixel has been digitized. The conventional process of color interpolation performed after an analog signal associated with each pixel has been digitized requires conversion from analog to digital (A/D) and **may require extensive computations** in order to achieve a high quality color presentation of the

image. The A/D conversion and extensive computations **may require hardware, such as** analog-to-digital (A/D) converters, memory, **processors, and software.** The hardware and software **may add to the complexity, size and expense of the imaging device** and reduce the speed of the imaging process.

(Ex. 1007, 1:32-49 (emphasis added).)

113. Indeed, *Isogai* recognizes that implementing components of its imaging device on the same or different chips is a design choice. (Ex. 1005, ¶[0065] (disclosing, with respect to the embodiment shown in FIG. 17, that the output buffer amplifiers 28a-28d can be provided “inside the solid-state image sensing element in order to avoid the influence of external noise” whereas differential amplifiers 34a-b are provided “outside the solid-state image sensing element.”, FIG. 17.)

114. Therefore, *Neter* discloses that in conventional image processing systems (like that disclosed by *Isogai*) the image processing **may require** significant resources that could increase the complexity, size and expense of the imaging device. A person of ordinary skill in the art reading *Neter* would have understood that *Neter* discloses that the color interpolation circuitry, as well as the analog-to-digital conversion circuitry, can either be placed on the same chip as the pixel array or not, where the decision as to whether to use one chip or two is a design choice that will be influenced by many factors. A person of ordinary skill in the art would have

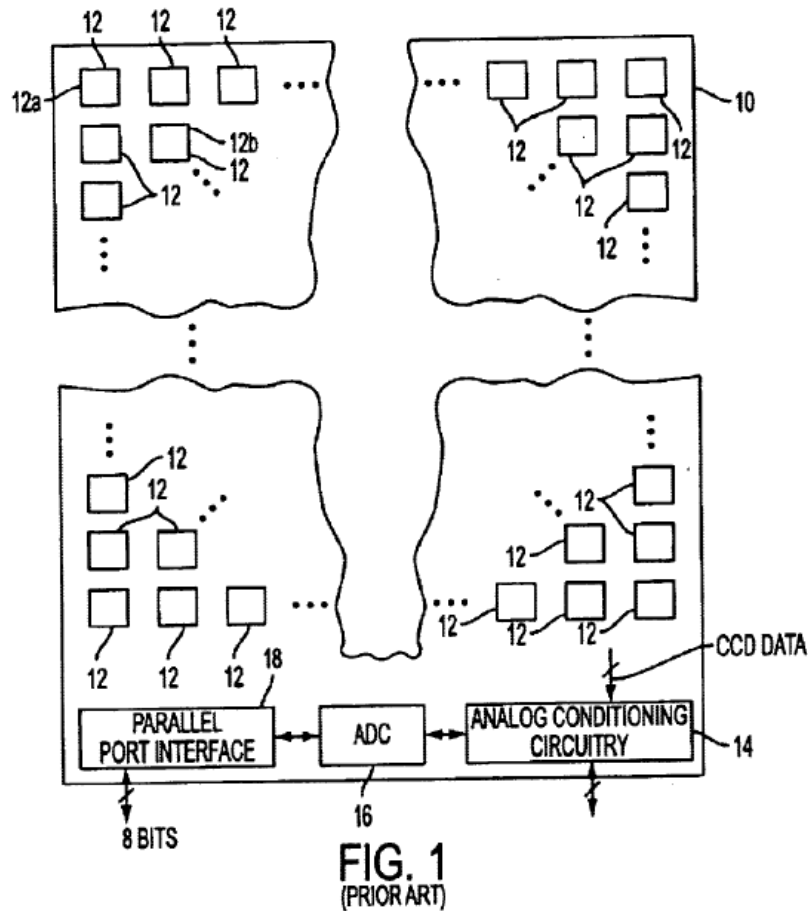
understood that such factors would include the complexity of pixel interpolation and other processing, the size of the pixel array, the complexity of the analog-to-digital converters, as well as the presence or absence of additional intervening circuitry between the pixel array and the color interpolation circuitry.

115. Indeed, a person of ordinary skill in the art would have understood that while integration of circuitry onto a single chip can provide a number of advantages, including increased performance, reduced manufacturing costs, fewer chips required, and the like, in some instances it is preferable to maintain the color interpolation circuitry on a separate chip while integrating the analog-to-digital converters onto the same chip as the pixel array. For example, including the analog-to-digital conversion on the same chip as the pixel array while keeping the color interpolation circuitry on a separate chip provides flexibility to support different systems/applications with different levels of color processing. In such a scenario, a single pixel array chip that includes analog-to-digital converters would provide digital outputs that can be provided as the inputs to different color interpolation/processing chips with different processing capabilities in order to satisfy the needs of different applications.

116. Indeed, such an understanding is supported by contemporaneous references that disclose analog-to-digital converters being included with the pixel

array on the same chip while the color interpolation circuitry resides on a separate chip. For example, *Fossum*³ discloses CMOS imagers with analog-to-digital conversion on the same chip as the pixel array “to provide a digital representation of the image which can be retrieved from the imager 10 through a parallel port interface.” (Ex. 1008, 1:7-26, FIG. 1 (showing analog to digital converter (ADC) 16 on the same chip as pixel cells 12).)

³ I refer to *Fossum* to demonstrate the knowledge of a person of ordinary skill in the art at the relevant time.



(Ex. 1008, FIG. 1.) *Fossum* further discloses that a separate DSP chip 30 can be used with the imaging chip 10 above, where the DSP chip 30 performs color interpolation. (*Id.*, 2:5-7 (“Referring to FIG. 4, a third solution might be to use an off chip discrete-time signal processing (DSP) engine 30 to interpolate the two missing colors for each pixel cell.”).)

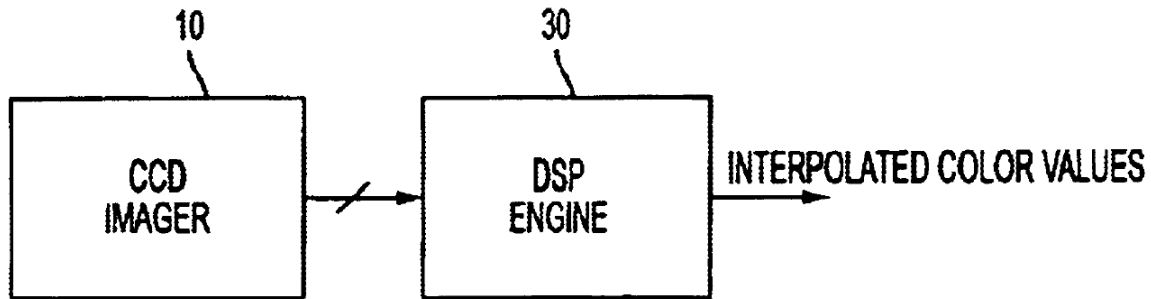


FIG. 4
(PRIOR ART)

(*Id.*, FIG. 4.)

117. Therefore, a person of ordinary skill in the art would have understood that choosing whether to put the analog-to-digital converters and/or color interpolation circuitry for an image processing system on the same chip with the pixel array is a design choice. Moreover, such a person of ordinary skill in the art would have understood that for some applications the analog-to-digital converters are on the same chip as the pixel array, whereas the color interpolation circuitry is on a second chip. Therefore, in view of *Neter* and having knowledge of the state of the art at the relevant time, a person of ordinary skill in the art looking to implement a solid state imaging device as disclosed in *Isogai* would have been motivated to include the analog-to-digital converters for the outputs of the pixels on the same chip as the pixel array, while providing a second chip that includes the color processing circuitry.

118. Including the analog-to-digital converters on the same chip as the pixel array in the imaging device of *Isogai* and a second chip that includes the color processing circuitry would have merely involved the use of a known technique (performing analog-to-digital conversion of the pixel outputs on the same chip as the red, blue, and green pixels and color processing on a separate chip) to improve a similar device (the device described in *Isogai*) to achieve the expected and desired result of increased integration while maintaining flexibility to support different systems/applications with different levels of pixel interpolation. Additionally, as discussed above, it was known and predictable that imaging circuitry like that described in *Isogai* could have been implemented on either one chip or more than one chip, depending on the needs of the system. Thus, a skilled would have had reason to try implementing the circuitry in *Isogai* on either one chip or more than one chip with a reasonable expectation that one would be successful.

119. Therefore, the *Isogai-Neter* combination discloses or suggests “a first chip and a second chip, wherein the red pixel, the blue pixel, the first green pixel, the second green pixel, the first analog-to-digital converter and the second analog-to-digital converter are disposed on the first chip and the color interpolation circuit is disposed on the second chip” as recited in claim 4 of the ’651 patent.

120. Including the analog-to-digital converters 80, 81 in *Isogai's* imaging device as shown in figure 1 would have been straightforward for a skilled person to implement given such a person's knowledge of the state of the art and the disclosure in *Neter*. Moreover, a person of ordinary skill in the art would have understood how to make any needed modifications in order to ensure that such integration was successful. For example, as demonstrated by *Neter*, *Fossum*, and *Loinaz*⁴, a person of ordinary skill in the art at the relevant time had the capability to include both the analog-to-digital conversion circuitry and the color processing (color interpolation) circuitry on the same chip as the pixel array. (Ex. 1007, 5:47-52; Ex. 1008, FIGs. 1, 5; Ex. 1010, FIG. 1; *see* my analysis below with respect to claim 5 in section IX.B.4.) Therefore, such a person of ordinary skill in the art would also have been able to include a subset of those components on the same chip while keeping the color processing circuitry on a second chip. It is my opinion that any modifications necessary to ensure that the functionality *Isogai's* imaging device with the components partitioned between two chips as described above would have been apparent to, and within the capabilities of, a person of ordinary skill in the art.

⁴ I refer to *Fossum* to demonstrate the knowledge of a person of ordinary skill in the art at the relevant time.

4. Claim 5

- a) **“The solid stage imaging device of claim 1 further comprising a chip, wherein the red pixel, the blue pixel, the first green pixel, the second green pixel, the first analog-to-digital converter, the second analog-to-digital converter and the color interpolation circuit are disposed on the chip.”**

121. In my opinion, *Isogai* in combination with *Neter* discloses or suggests this feature. As I discussed above in Section IX.B.3, a person of ordinary skill in the art would have understood, based on the disclosure of *Neter* and their understanding of the state of the art, that implementing the analog-to-digital converters and color processing circuitry on the same chip as the pixel array in an image processing device is a design choice. (See my analysis above in Section IX.B.3.) Moreover, as I also discussed above in Section IX.B.3, a person of ordinary skill in the art would have been motivated to include all of these components of an imaging device, like that disclosed by *Isogai*, on the same chip in order to realize a number of advantages, including increased performance, reduced manufacturing costs, fewer chips required, and the like.

122. As discussed above, *Neter* discloses “[t]he exemplified imaging systems described below with reference to FIGs. 1-23 use a CMOS integrated circuit, an array of pixels organized in a rectangle matrix, and a color filter with a primary color system (RGB) in Bayer color pattern.” (Ex. 1007, 7:33-37.) *Neter*

further discloses an embodiment where the analog-to-digital converters and color interpolation circuitry for the imaging device are included on the same integrated circuit as the array of pixels. (*Id.*, 7:55-59 (“In one embodiment, the color interpolation system, the color compensation system and/or the fixed pattern noise reduction system reside together with the sensor array in the same chip, such as in a CMOS integrated circuit color imaging device.”), 5:47-52 (“The imaging system in accordance with the present invention may also include additional **on-chip** or off chip amplification stages, **analog-to-digital conversion units**, memory units and various other **signal processing blocks**.”) (emphasis added), 7:48-53 (“The imaging system may also include either **on-chip**, as is possible with CMOS integrated circuit imaging devices, or off-chip, as is the case with CCD integrated circuit imaging devices, amplification stages, **analog to digital conversion units**, memory units and various other signal processing blocks.”) (emphasis added), 3:1-3.) Therefore, in my opinion, such a person of ordinary skill in the art would have been motivated to combine all of these components on the same chip in order to realize the benefits of integration.

123. Including the analog-to-digital converters and color processing circuitry on the same chip as the pixel array in the imaging device of *Isogai* would have merely involved the use of a known technique (performing analog-to-digital

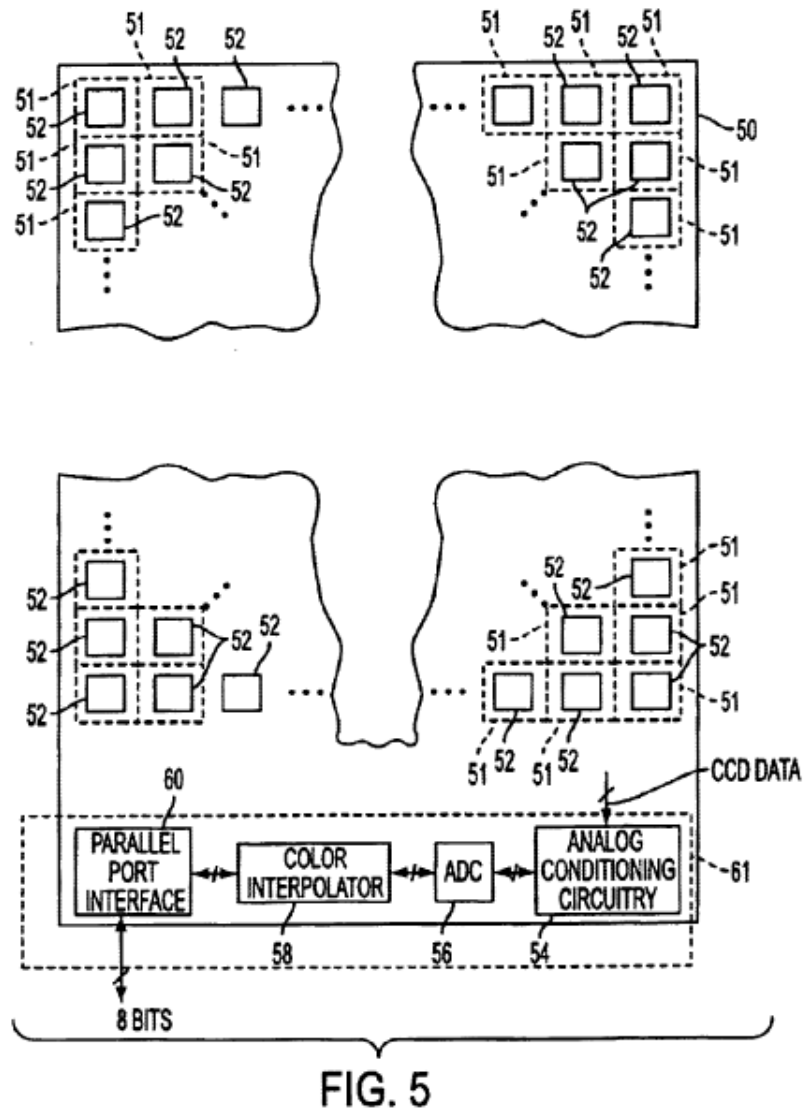
conversion and color processing on the same chip as the red, blue, and green pixels as disclosed in *Neter*) to improve a similar device (the imaging device of *Isogai*) to achieve the expected and desired result of increased integration that can provide increased speed, reduced costs, and support for smaller devices. Additionally, as I discussed above, it was known and predictable that imaging circuitry like that described in *Isogai* could be implemented on either one chip or more than one chip, depending on the needs of the system. Thus, a person of ordinary skill in the art would have had reason to try implementing the circuitry in *Isogai* on either one chip or more than one chip with a reasonable expectation that one would be successful.

124. Therefore, in my opinion, the *Isogai-Neter* combination discloses or suggests “a chip, wherein the red pixel, the blue pixel, the first green pixel, the second green pixel, the first analog-to-digital converter, the second analog-to-digital converter and the color interpolation circuit are disposed on the chip” as recited in claim 5 of the '651 patent. Including the analog-to-digital converters 80, 81 and color processing circuitry in *Isogai*'s solid-state image sensing element as shown in figure 1 would have been straightforward for a skilled person to implement given such a person's knowledge of the state of the art and the disclosure in *Neter*.

125. Indeed, the motivation and ability for a person of ordinary skill in the art to perform such integration is supported by contemporaneous references that

disclose analog-to-digital converters and color processing circuitry being included with the pixel array on the same chip. For example, *Fossum*⁵ discloses CMOS imagers with analog-to-digital conversion and color interpolation circuitry on the same chip as the pixel array. (Ex. 1008, 4:4-6, 4:33-44, FIG. 5.)

⁵ I refer to *Fossum* to demonstrate the knowledge of a person of ordinary skill in the art at the relevant time.



(Ex. 1008, FIG. 5.)

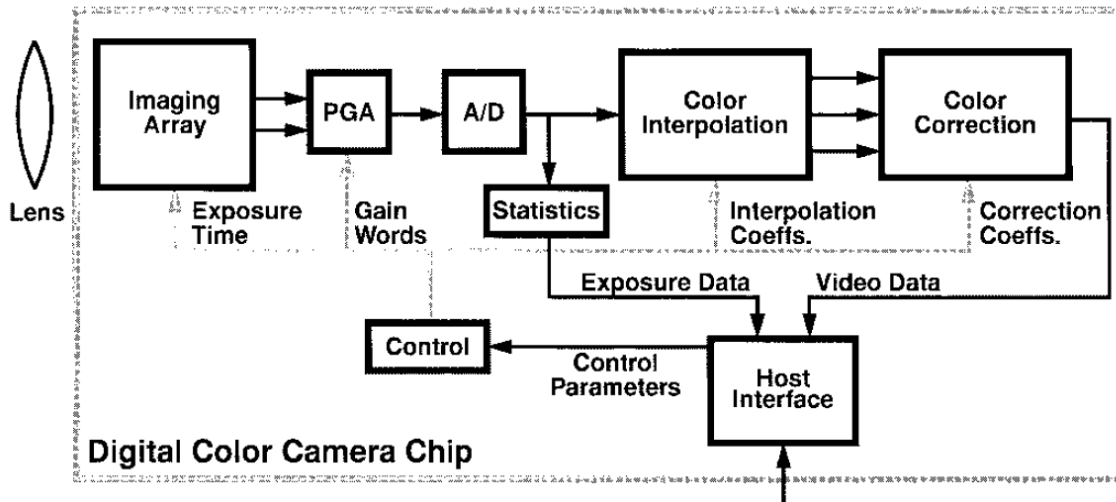
126. As *Fossum* discloses, “FIG. 5 shows a CMOS imager 50 located on a monolithic semiconductor substrate, or chip” (*id.*, 4:33-34), without “requiring . . . off chip-color interpolation” (*id.*, 4:40-44). *Fossum* further discloses that “[a]mong

the advantages of the invention” is that [t]rue color imaging occurs on a single semiconductor chip.” (*Id.*, 4:4-6.) Indeed, the color interpolation performed on-chip in *Fossum* is the same interpolation disclosed by *Isogai* and the ’651 patent:

The imager 50 has an on chip color interpolator 58 which for each photosensitive site 51 estimates the level of the primary colors that are not sensed by the pixel cell 52 at the photosensitive site 51. The color sensed by the pixel cell 52 is determined by a primary color filter of the site 51 that covers the pixel cell 52. In this manner, the primary color filter (which is a red, green, or blue filter) covers the cell 52. Each cell 52 senses the level of light by measuring the intensity of the light in one of the primary color bands (e.g., red, green or blue) but does not sense the level of light in the other two primary color bands. The interpolator 58 estimates the missing color levels for the site 51 by using the outputs of pixel cells 52 in adjacent photo sensitive sites 51 that are sensing these color levels.

(*Id.*, 4:45-58.)

127. Similarly, as shown in figure 1 below, *Loinaz*⁶ discloses a digital color camera chip that includes the imaging array, analog-to-digital conversion circuitry, and color interpolation circuitry on the same chip. (Ex. 1010, Abstract, FIG. 1.)



(*Id.*, FIG. 1 (excerpt).)

128. Loinaz discloses:

A digital color camera has been **monolithically realized** in a standard 0.8- μ m CMOS technology. **The chip integrates** a 354 x 292 photogate **sensor array** with unity-gain column circuit, a hierarchical column multiplexer, a switched-capacitor programmable-gain amplifier, and a **8-b flash analog/digital converter**

⁶ I refer to *Loinaz* to demonstrate the knowledge of a person of ordinary skill in the art at the relevant time.

together with digital circuits performing color interpolation, color correction, computation of image statistics, and control functions.

(*Id.*, Abstract (emphasis added).)

5. Claim 19

- a) **“The imaging method of claim 18 further comprising: correcting a gain of one of the output of the red pixel, the output of the blue pixel, the output of the first green pixel and the output of the second green pixel.”**

129. In my opinion, *Isogai* in combination with *Neter* discloses or suggests this feature for the reasons I discuss above with respect to claim 2. (*See* my analysis above in Section IX.B.1.)

6. Claim 20

- a) **“The imaging method of claim 18 further comprising: correcting a fixed pattern noise offset from one of the output of the red pixel, the output of the blue pixel, the output of the first green pixel and the output of the second green pixel.”**

130. In my opinion, *Isogai* in combination with *Neter* discloses or suggests this feature for the reasons I discuss above with respect to claim 3. (*See* my analysis above in Section IX.B.2.)

7. Claim 21

- a) **“The imaging method of claim 18, wherein the red pixel, the blue pixel, the first green pixel, the second green pixel, the first analog-to-digital converter, and the second analog-to-digital converter are disposed on**

a first chip and the color interpolation circuit is disposed on a second chip.”

131. In my opinion, *Isogai* in combination with *Neter* discloses or suggests this feature for the reasons I discuss above with respect to claim 4. (See my analysis above in Section IX.B.3.)

8. Claim 22

- a) **“The imaging method of claim 18, wherein the red pixel, the blue pixel, the first green pixel, the second green pixel, the first analog-to-digital converter, the second analog-to-digital converter and the color interpolation circuit is disposed on a chip.”**

132. In my opinion, *Isogai* in combination with *Neter* discloses or suggests this feature for the reasons I discuss above with respect to claim 5. (See my analysis above in Section IX.B.4.)

C. *Isogai* in Combination with *Fossum* Discloses or Suggests the Features of Claims 2-5 and 19-22

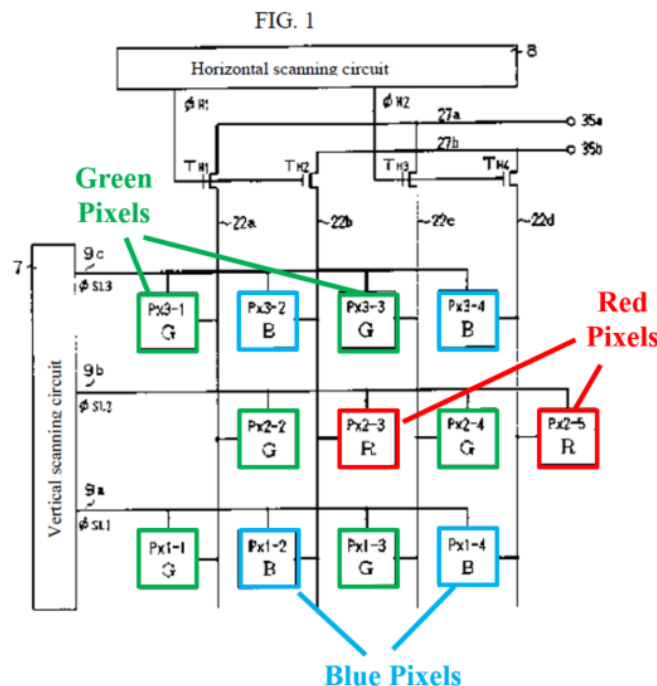
1. Claim 2

- a) **“The solid stage imaging device of claim 1, further comprising an error compensation circuit for correcting a gain of one of the output of the red pixel, the output of the blue pixel, the output of the first green pixel and the output of the second green pixel.”**

133. In my opinion, *Isogai* in combination with *Fossum* discloses or suggests this feature. While the '651 patent shows the error compensation circuit operating on digital signals output from the A/D converters (Ex. 1001, FIGs. 1-3),

claim 2 indicates that the error compensation circuit corrects a gain of one of the outputs of the red, blue, and first and second green pixels, where those outputs are the analog signals that have not yet been converted to digital signals by the A/D converters. I have been asked to assume that, for purposes of the present analysis, the scope of claim 2 includes correcting a gain of one of the analog outputs of the red, blue, first green, and second green pixels. With such an assumption in mind, *Isogai* in combination with *Fossum* discloses or suggests this feature.

134. As I discussed above, *Isogai* discloses a solid state imaging device that includes a solid state image sensing element according to a first embodiment disclosed in *Isogai*. (See my discussion above in Section IX.A.1(a).)



(Ex. 1005, FIG. 1 (annotated).)

135. The embodiment of figure 1 of *Isogai* does not explicitly disclose an error compensation circuit for correcting a gain outputs of the red, blue, and green pixels. However, as I discuss below, *Fossum* discloses correcting a gain in the form of gain control of outputs from the pixels, and a person of ordinary skill in the art would have been motivated in view of *Fossum* to utilize such gain correction in the solid state imaging device that includes the solid state image sensing element corresponding to the first embodiment of *Isogai*.

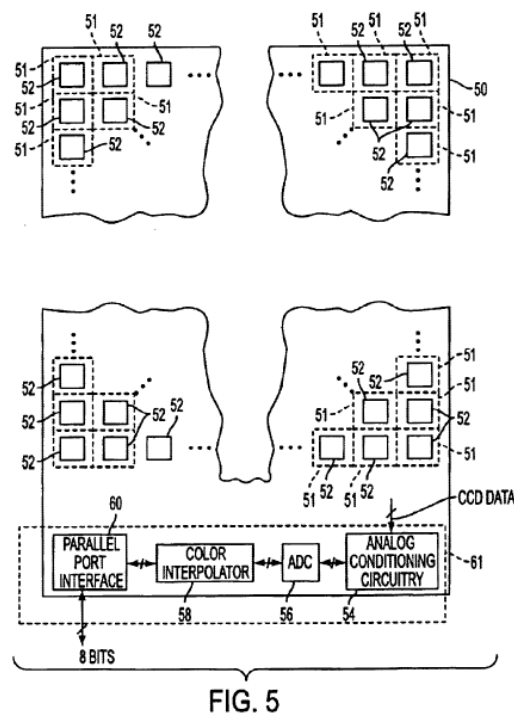
136. *Fossum*, like *Isogai*, describes circuits for processing red, blue, and green imaging pixel sensor elements that includes color interpolation:

The imager 50 has an on chip color interpolator 58 which for each photosensitive site 51 estimates the level of the primary colors that are not sensed by the pixel cell 52 at the photosensitive site 51. The color sensed by the pixel cell 52 is determined by a primary color filter of the site 51 that covers the pixel cell 52. In this manner, the primary color filter (which is a red, green, or blue filter) covers the cell 52. Each cell 52 senses the level of light by measuring the intensity of the light in one of the primary color bands (e.g., red, green or blue) but does not sense the level of light in the other two primary color bands. The interpolator 58 estimates the missing color

levels for the site 51 by using the outputs of pixel cells 52 in adjacent photo sensitive sites 51 that are sensing these color levels.

(Ex. 1008, 4:45-59.)

137. Therefore, a person of ordinary skill in the art implementing the image sensing device of *Isogai* would have had reason to look to *Fossum*.



(Ex. 1008, FIG. 5.)

138. As shown in figure 5 above, *Fossum* further discloses that color interpolation done after analog-to-digital conversion, which is consistent with the disclosure of *Isogai*. (Ex. 1008, FIG. 5; *see also id.*, 5:7-11 (“The circuitry 54 furnishes its output to an analog-to-digital converter 56 which converts the analog

outputs of the pixel cells 52 into digital data and supplies the digital data to the interpolator 58.”.) *Fossum* also discloses imaging devices that also adjust the gain of the analog outputs from the pixels. For example, as shown in figure 5 above, *Fossum* discloses analog conditioning circuitry 54 that performs “correlated double sampling of the analog outputs of the pixel cells 52 and **provide[s] gain control.**” (*Id.*, 5:4-6, (emphasis added); *see also id.*, FIG. 5.)

139. A person of ordinary skill in the art would have understood that *Fossum*’s disclosure of gain control with respect to the analog outputs of the pixels constitutes “correcting a gain” of one of the pixel outputs as is recited in claim 2. Such an understanding is supported by *Neter*,⁷ which discloses that in addition to color interpolation, imaging devices also perform color compensation, which involves adjusting the signals for different colored pixels as the pixel elements may be more responsive to one color of light in comparison to another color of light:

Conventional imaging devices also require color compensation for difference in the response of the various color filters and for variations within the integrated circuit sensor array, such as process, materials, temperature or

⁷ I refer to *Neter* to demonstrate the knowledge of a person of ordinary skill in the art at the relevant time.

manufacturing. For example, when the primary color scheme is used, **the response of an element that absorbs red light may be different than an element that absorbs blue light even when illuminated by light of equal red and blue luminosity levels.** When exposed to a flat light image having equal intensity and chromaticity levels through, **typical CMOS or CCD arrays may generate analog signals having significant magnitude variations for the different color components.** According, if the analog signals are used to reproduce the original image, the reproduced image colors will not match the original colors.

To overcome this problem, conventional imaging devices employ a process of color correction that is performed after the analog signals for each pixel have been digitized. One drawback of the conventional color correction process is a loss in color dynamic range that results from under-utilization of the A/D converter for some of the color components. Another drawback is increased computations that translates into additional hardware, size expense and/or reduced speed.

(Ex. 1007, 1:50-2:6 (emphasis added).)

140. *Neter* also discloses that the described color compensation, like the gain control described by *Fossum*, is done to the analog outputs of the pixels:

In one embodiment, the imaging system with **color compensation** includes a control circuit that provides **four output paths that can be amplified separately via one or more stages of programmable gain amplifiers** and/or summing amplifiers. The control circuit allows four independent readouts for even rows, odd rows, even columns and odd columns, thus providing separate and/or simultaneous output paths for Red, Green and Blue pixels.

For example, one embodiment of the imaging system employs a readout control that provides outputs for the Red pixel, the Blue pixel, and the two Green pixels. Thus the imaging system allows further gain compensation for a Green pixel that resides in an even column compared to a Green pixel that resides in an odd column. The four signals are then amplified via four corresponding programmable gain amplifiers. The readout control logic ensures that the row and column switches are closed in the appropriate sequence.

(Ex. 1007, 4:19-36 (emphasis added).)

141. Therefore, a person of ordinary skill in the art would have understood that the gain control disclosed by *Fossum* constitutes “correcting a gain” as recited in claim 2 of the ’651 patent. Moreover, such a person of ordinary skill in the art would also have understood *Fossum*’s “analog conditioning circuitry” to correspond to an “error compensation circuit” as recited in claim 2 as it performs the gain

correction ascribed to the claimed error compensation circuit in that the gain control is able to compensate for magnitude variations for the different color components.

142. Given the disclosure of a gain control for color compensation in *Fossum*, a person of ordinary skill in the art would have been motivated to combine the teachings of *Isogai* and *Fossum* such that at least one of the output signals for the red, blue, first green, and second green pixels identified above with respect to claim 1 is conditioned in a manner that includes gain control in order to provide color compensation in *Isogai*'s image sensing device. A person of ordinary skill in the art would have been motivated to do so because such color compensation is able to compensate for "differences in the response of various color filters and variations within the integrated circuit sensor array, such as process, materials, temperature or manufacturing." (Ex. 1007, 13:30-34.) As a person of ordinary skill in the art would have understood, as evidenced by *Neter*, performing such color compensation on the analog outputs improves color dynamic range and image quality. (*Id.*, 13:34-39.)

143. Including analog-conditioning circuitry for gain control ("error compensation circuit for correcting a gain of one of the output of the red pixel, the output of the blue pixel, the output of the first green pixel and the output of the second green pixel") like that disclosed in *Fossum* in the imaging device of *Isogai* would have involved nothing more than the combination of known prior art elements

(the imaging array with pixel outputs of *Isogai* with the gain control as disclosed in *Fossum* to compensate for needed gain differentials between different colored pixels) using known circuit design methods, where each element performs the same function described in *Isogai* and *Fossum*, to achieve the predictable result of an imaging device that is improved to provide color compensation. As discussed above, both *Isogai* and *Fossum* describe circuits for processing imaging pixel sensor elements, but *Fossum* describes conditioning circuitry not found in *Isogai* for providing gain control. Therefore, a person of ordinary skill in the art would have recognized that *Fossum*'s teachings relating to gain control could be applied to *Isogai*'s system in a similar way. As also discussed above, such a skilled person would have been encouraged to implement such gain control in *Isogai*'s system to provide similar gain control capabilities to improve overall system performance.

144. Including such analog conditioning circuitry for gain control in *Isogai*'s imaging device would have been straightforward for a skilled person to implement given such a person's knowledge and the disclosure in *Fossum*. For example, the combination would have required nothing more than adding well-known and widely available conditioning circuitry for gain control to *Isogai*'s system, where such conditioning circuitry was commonly used for color correction at the time. Such a combination would not have detracted from the overall functionality of *Isogai*'s

system, which would have continued to operate as described in *Isogai* with the added circuitry to improve color output.

145. Furthermore, a person of ordinary skill in the art would have understood how to make any needed modifications in order to ensure that the analog conditioning circuitry for gain control would operate correctly in the imaging device of *Isogai*. For example, if needed, providing selection circuitry to route the red, blue, first green, and second green pixels to the analog conditioning circuitry, as well as circuitry for recombining the outputs of that circuitry to provide the proper sequence of signals to the analog-to-digital converters as disclosed in *Isogai*, would have been routine for such a person of ordinary skill in the art. Similarly, if additional control circuitry is required to provide the control information to the analog conditioning circuitry, that would also have been within the capability of a person of ordinary skill in the art. It is my opinion that any modifications necessary to ensure that the analog conditioning circuitry for gain control would work in the *Isogai* imaging device would have been apparent to, and within the capabilities of, a person of ordinary skill in the art.

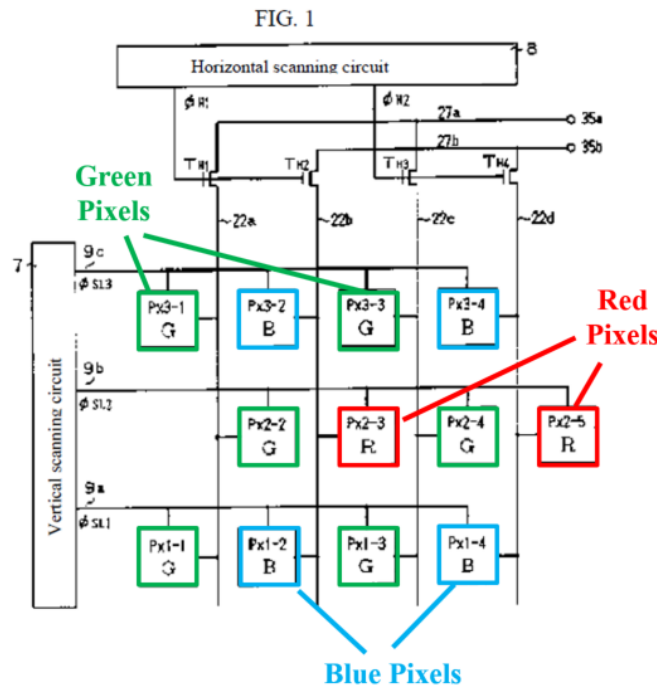
2. Claim 3

- a) **“The solid stage imaging device of claim 1, further comprising an error compensation circuit for correcting a fixed pattern noise offset from one of the output of the red pixel, the output of the blue pixel, the**

output of the first green pixel and the output of the second green pixel.”

146. As I also discussed above in Section IX.B.2, while the '651 patent shows the error compensation circuit operating on digital signal outputs from the A/D converters (Ex. 1001, FIGs. 1-3), claim 3 indicates that the error compensation circuit corrects a fixed pattern noise offset from one of the outputs of the red, blue, and first and second green pixels, where those outputs are the analog signals that have not yet been converted to digital signals by the A/D converters. I have been asked to assume that, for purposes of the present analysis, the scope of claim 3 includes correcting a fixed pattern noise offset from one of the analog outputs of the red, blue, first green, and second green pixels. With such an assumption in mind, *Isogai* in combination with *Fossum* discloses or suggests this feature.

147. As I discussed above, *Isogai* discloses a solid state imaging device that includes a solid state image sensing element according to a first embodiment corresponding to figure 1. (See my discussion above in section IX.A.1(a).)



(Ex. 1005, FIG. 1 (annotated).)

148. The embodiment of figure 1 of *Isogai* does not explicitly disclose an error compensation circuit for correcting a fixed pattern noise offset from one of the analog signals output by the red, blue, and green pixels. However, as I discuss below, *Fossum* discloses correcting a fixed pattern noise offset in the analog signal outputs from red, blue, and green pixels, and a person of ordinary skill in the art would have been motivated in view of *Fossum* to utilize such fixed pattern noise offset correction in the solid state imaging device of *Isogai* that includes the solid state image sensing element corresponding to the first embodiment.

149. As I discussed above in section IX.C.1, *Fossum*, like *Isogai*, describes circuits for processing imaging pixel sensor elements, and a person of ordinary skill in the art implementing an image sensing device as disclosed in *Isogai* would have had reason to look to *Fossum*. (See my discussion above in Section IX.C.1.) As I also discussed above in section IX.C.1, *Fossum* discloses analog conditioning circuitry that performs correlated double sampling and gain control with respect to the analog outputs of the pixels. (See my discussion above in section IX.C.1; Ex. 1007, 1:20-22, 5:4-6.)

150. A person of ordinary skill in the art would have understood that the correlated double sampling of the analog outputs of the pixels by *Fossum*'s analog conditioning circuitry reduces fixed pattern noise. (Ex. 1011, 7:35-38 ("on-chip correlated doubling sampling can be implemented in many active pixel sensors to suppress noise such as the fixed pattern noise and the kTC noise."); Ex. 1012, 40:17-23 ("signal conversion" includes "a CDS (Correlated Double Sampling) 110d" "[t]CDS 110d samples and holds the output of the image pick-up 51d two times and performs subtraction with the resulting two signal levels in order to reduce noise.")⁸

⁸ I refer to *Yadid-Pecht* and *Imuyia-364* to demonstrate the knowledge of a person of ordinary skill in the art at the relevant time.

151. Therefore, in my opinion, *Fossum* discloses an “error compensation circuit for correcting a fixed pattern noise offset from one of the output of the red pixel, the output of the blue pixel, the output of the first green pixel and the output of the second green pixel” as recited in claim 3. Moreover, a person of ordinary skill in the art would also have understood *Fossum*’s “analog conditioning circuitry” to correspond to an “error compensation circuit” as recited in claim 3 as, like the recited error compensation circuit, it corrects a fixed pattern noise offset.

152. Given the disclosure of a fixed pattern noise offset reduction by correlated double sampling in *Fossum*, a person of ordinary skill in the art would have been motivated to combine the teachings of *Isogai* and *Fossum* such that at least one of the output signals for the red, blue, first green, and second green pixels identified above with respect to claim 1 is conditioned in a manner that includes correlated double sampling in order to reduce fixed pattern noise in *Isogai*’s image sensing device. A person of ordinary skill in the art would have been motivated to do so because, as such a skilled person would have known, fixed pattern noise

reduction allows for increased dynamic range and higher image quality. (Ex. 1007, 5:12-14, 15:64-66.)⁹

153. Accordingly, such a person of ordinary skill in the art would have combined the teachings of *Isogai* and *Fossum* such that the output of at least one of the red, blue, first green, and second green pixels in *Isogai* has fixed pattern noise reduced in order to, for example, improve dynamic range of the output for the pixel. A person of ordinary skill in the art would have understood that fixed pattern noise reduction circuitry, like analog conditioning circuitry disclosed in *Fossum*, constitutes an “error correction circuit” that, as recited in claim 3, corrects a fixed pattern noise offset for at least one of the red, blue, and first and second green pixels.

154. Including fixed pattern noise reduction circuitry like that disclosed in *Fossum* in the imaging device of *Isogai* would have involved nothing more than the combination of known prior art elements (the image array with pixel outputs of *Isogai* with the correlated double sampling circuitry of *Fossum* to compensate for fixed pattern noise) using known circuit design methods, where each element performs the same function described in *Fossum* and *Isogai*, to achieve the

⁹ I refer to *Neter* to demonstrate the knowledge of a person of ordinary skill in the art at the relevant time.

predictable result of an imaging device that is improved have higher image quality because of reduced noise. As discussed above, both *Isogai* and *Fossum* describe circuits for processing imaging pixel sensor elements, but *Fossum* describes additional circuitry not found in *Isogai* for correlated double sampling. Therefore, a person of ordinary skill in the art would have recognized that *Fossum*'s teachings relating to noise reduction could be applied to *Isogai*'s system in a similar way. As also discussed above, such a skilled person would have been encouraged to implement such correlated double sampling in *Isogai*'s system to provide similar noise reduction capabilities to improve overall system performance, including improved image quality.

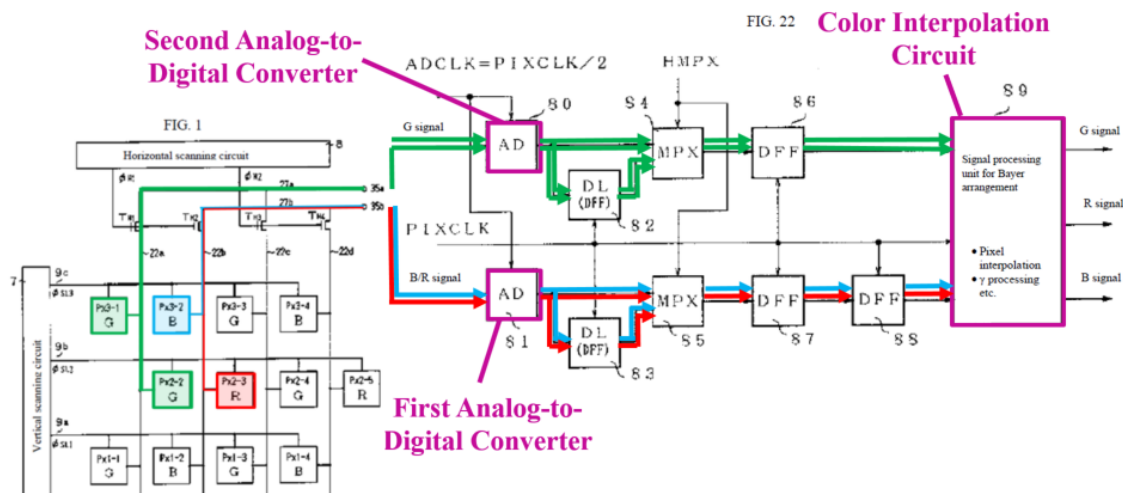
155. Including correlated double sampling in *Isogai*'s imaging device would have been straightforward for a skilled person to implement given such a person's knowledge and the disclosure of *Fossum*. Moreover, a person of ordinary skill in the art would have understood how to make any needed modifications in order to ensure that the analog conditioning circuitry would operate correctly within the imaging device of *Isogai*. If additional control circuitry is required to provide the control information to the analog conditioning circuitry, that would also have been within the capability of a person of ordinary skill in the art. It is my opinion that any modifications necessary to ensure that the analog conditioning circuitry would work

in *Isogai's* imaging device would have been apparent to, and within the capabilities of, a person of ordinary skill in the art.

3. Claim 4

- a) “The solid stage imaging device of claim 1 further comprising a first chip and a second chip, wherein the red pixel, the blue pixel, the first green pixel, the second green pixel, the first analog-to-digital converter and the second analog-to-digital converter are disposed on the first chip and the color interpolation circuit is disposed on the second chip.”

156. In my opinion, *Isogai* in combination with *Fossum* discloses or suggests these features. As I discussed above in Section IX.A.1(a), *Isogai* discloses a solid state imaging device that includes a solid state image sensing element according to the first embodiment in combination with the processing system shown in figure 22. (See my discussion above in section IX.A.1(a).)

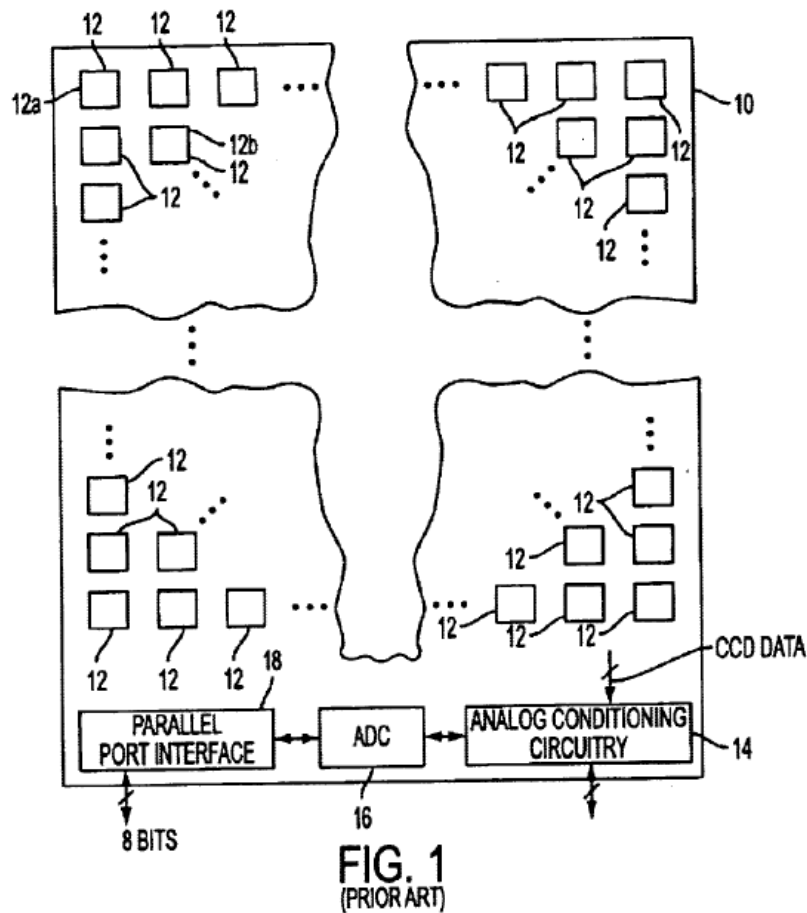


(*Id.*, FIGs. 1, 22 (annotated).)

157. *Isogai* does not explicitly disclose that, for this solid state imaging device, that the red pixel, the blue pixel, the first green pixel, the second green pixel, the first analog-to-digital converter, and the second analog-to-digital converter are disposed on a first chip and the color interpolation circuit is disposed on a second chip as recited in claim 4. However, *Fossum* discloses such a feature and, in my opinion, a person of ordinary skill in the art would have been motivated to combine the teachings of *Fossum* with those of *Isogai* to implement the recited components in *Isogai* on two separate chips as recited in claim 4.

158. As I discussed above in section IX.C.1, *Fossum*, like *Isogai*, describes circuits for processing imaging pixel sensor elements and a person of ordinary skill in the art implementing the image sensing device of *Isogai* would have had reason to look to *Fossum*. (See my discussion above in Section IX.C.1.)

159. *Fossum* discloses CMOS imagers with analog-to-digital conversion on the same chip as a red, blue, and green pixel array “to provide a digital representation of the image which can be retrieved from the imager 10 through a parallel port interface.” (Ex. 1008, 1:7-26, FIG. 1 (showing analog to digital converter (ADC) 16 on the same chip as pixel cells 12).)



(Ex. 1008, FIG. 1.) *Fossum* further discloses that a separate DSP chip 30 is used with the imaging chip 10 above, where the DSP chip 30 performs color interpolation. (*Id.*, 2:5-7 (“Referring to FIG. 4, a third solution might be to use an off chip discrete-time signal processing (DSP) engine 30 to interpolate the two missing colors for each pixel cell.”).)

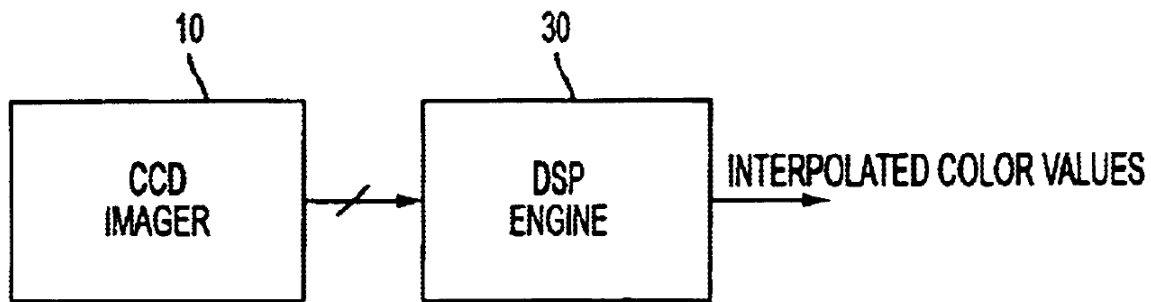


FIG. 4
(PRIOR ART)

(*Id.*, FIG. 4.)

160. Therefore, *Fossum* discloses “a first chip and a second chip, wherein the red pixel, the blue pixel, the first green pixel, the second green pixel, the first analog-to-digital converter and the second analog-to-digital converter are disposed on the first chip and the color interpolation circuit is disposed on the second chip” as recited in claim 4. In my opinion, a person of ordinary skill in the art implementing the imaging device of *Isogai* would have been motivated, in view of *Fossum*, to include *Isogai*’s analog-to-digital converters 80, 81 on the same chip with the red, blue, first green and second green pixels while maintaining the color processing circuitry on a separate chip.

161. A person of ordinary skill in the art would have understood that while integration of circuitry onto a single chip can provide a number of advantages, including increased performance, reduced manufacturing costs, fewer chips required

for smaller applications, and the like, in some instances it may be preferable to maintain the color interpolation circuitry on a separate chip while integrating the analog-to-digital converters onto the same chip as the pixel array. For example, including the analog-to-digital conversion on the same chip as the pixel array while keeping the color interpolation circuitry on a separate chip would provide flexibility to support different systems/applications with different levels of color processing. For example, a pixel array chip that includes analog-to-digital converters would provide digital outputs that can be provided as the inputs to different color interpolation/processing chips with different processing capabilities in order to satisfy the needs of different applications. Such an understanding is supported by *Fossum*, which discloses that the semiconductor imager in figure 1, which includes the pixels as well as the analog-to-digital conversion circuitry “provide[s] a digital representation of the image which can be retrieved from the imager 10 through a parallel port interface.” (Ex. 1008, 1:24-26.)

162. Moreover, a person of ordinary skill in the art would have understood that determining whether to put the analog-to-digital converters and/or color interpolation circuitry for an image processing system on the same chip with the pixel array is a design choice. Indeed, *Isogai* recognizes that implementing components of its imaging device on the same or different chips is a design choice.

(Ex. 1007, ¶[0065] (disclosing, with respect to the embodiment shown in FIG. 17, that the output buffer amplifiers 28a-28d can be provided “inside the solid-state image sensing element in order to avoid the influence of external noise” whereas differential amplifiers 34a-b are provided “outside the solid-state image sensing element.”, FIG. 17.)

163. A person of ordinary skill in the art would have understood that for some applications (e.g. figure 1 of *Fossum*) the analog-to-digital converters are on the same chip as the pixel array, whereas the color interpolation circuitry is on a second chip. In other applications, the analog-to-digital converters, the color interpolation circuitry, and the pixel array are all on the same chip (e.g. figure 5 of *Fossum*). Such a person of ordinary skill in the art would have understood that the design choice as to whether to use one chip or two can be influenced by many factors. A person of ordinary skill in the art would have understood that such factors include the complexity of pixel interpolation and other processing, the size of the pixel array, the complexity of the analog-to-digital converters, as well as the presence or absence of additional intervening circuitry between the pixel array and the color interpolation circuitry.

164. Therefore, in view of *Fossum* and having knowledge of the state of the art at the relevant time, a person of ordinary skill in the art looking to implement a

solid state imaging device as disclosed in *Isogai* would have been motivated to include the analog-to-digital converters for the outputs of the pixels on the same chip as the pixel array, while providing a second chip that includes the color processing circuitry.

165. Including the analog-to-digital converters on the same chip as the pixel array in the imaging device of *Isogai* would have merely involved the use of a known technique (performing analog-to-digital conversion on the same chip as the pixels as disclosed in *Fossum* and color processing on a separate chip) to improve a similar device (the device of *Isogai*) achieve the expected and desired result of increased integration while maintaining flexibility to support different systems/applications with different levels of color processing. Additionally, as I discussed above, it was known and predictable that imaging circuitry like that described in *Isogai* could have been implemented on either one chip or more than one chip, depending on the needs of the system. Thus, a person of ordinary skill in the art would have had reason to try implementing the circuitry in *Isogai* on either one chip or more than one chip with a reasonable expectation that one would be successful.

166. Therefore, a person of ordinary skill in the art would have been motivated to include *Isogai's* analog-to-digital converters 80, 81 on the same chip as the pixel array as shown in figure 1 of *Isogai*, while maintaining the color

processing circuitry 89 on a second chip such that the *Isogai-Fossum* combination discloses “a first chip and a second chip, wherein the red pixel, the blue pixel, the first green pixel, the second green pixel, the first analog-to-digital converter and the second analog-to-digital converter are disposed on the first chip and the color interpolation circuit is disposed on the second chip” as recited in claim 4 of the ’651 patent. Including the analog-to-digital converters 80, 81 in Isogai’s imaging device as shown in figure 1 would have been straightforward for a skilled person to implement given such a person’s knowledge of the state of the art and the disclosure in *Fossum*.

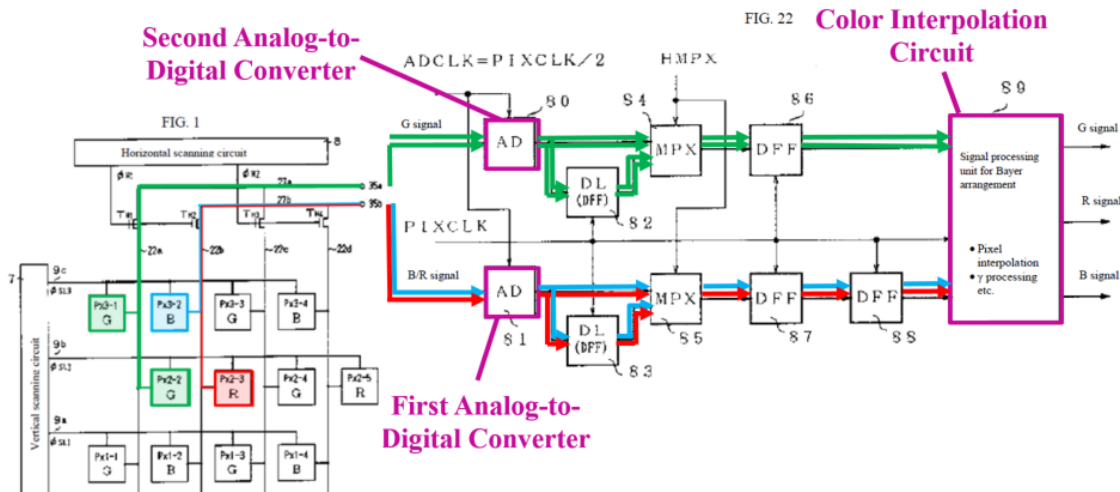
167. Moreover, a person of ordinary skill in the art would have understood how to make any needed modifications in order to ensure that such integration was possible. For example, as demonstrated by *Fossum*, *Neter*, and *Loinaz*, a person of ordinary skill in the art at the relevant time had the capability to include both the analog-to-digital conversion circuitry and the color processing (color interpolation) circuitry on the same chip as the pixel array. (Ex. 1007, 5:47-52; Ex. 1008, FIGs. 1, 5; Ex. 1010, FIG. 1; *see* my discussion above in Section IX.B.4.) Therefore, such a person of ordinary skill in the art would also have been able to include a subset of those components on the same chip while keeping the color processing circuitry on a second chip. It is my opinion that any modifications necessary to ensure that the

functionality *Isogai's* imaging device with the components partitioned between two chips as described above would have been apparent to, and within the capabilities of, a person of ordinary skill in the art.

4. Claim 5

- a) “The solid stage imaging device of claim 1 further comprising a chip, wherein the red pixel, the blue pixel, the first green pixel, the second green pixel, the first analog-to-digital converter, the second analog-to-digital converter and the color interpolation circuit are disposed on the chip.”

168. In my opinion, *Isogai* in combination with *Fossum* discloses or suggests this feature. As I discussed above in Section IX.A.1(a), *Isogai* discloses a solid state imaging device that includes a solid state image sensing element according to the first embodiment in combination with the processing system shown in figure 22. (See my discussion above in section IX.A.1(a).)



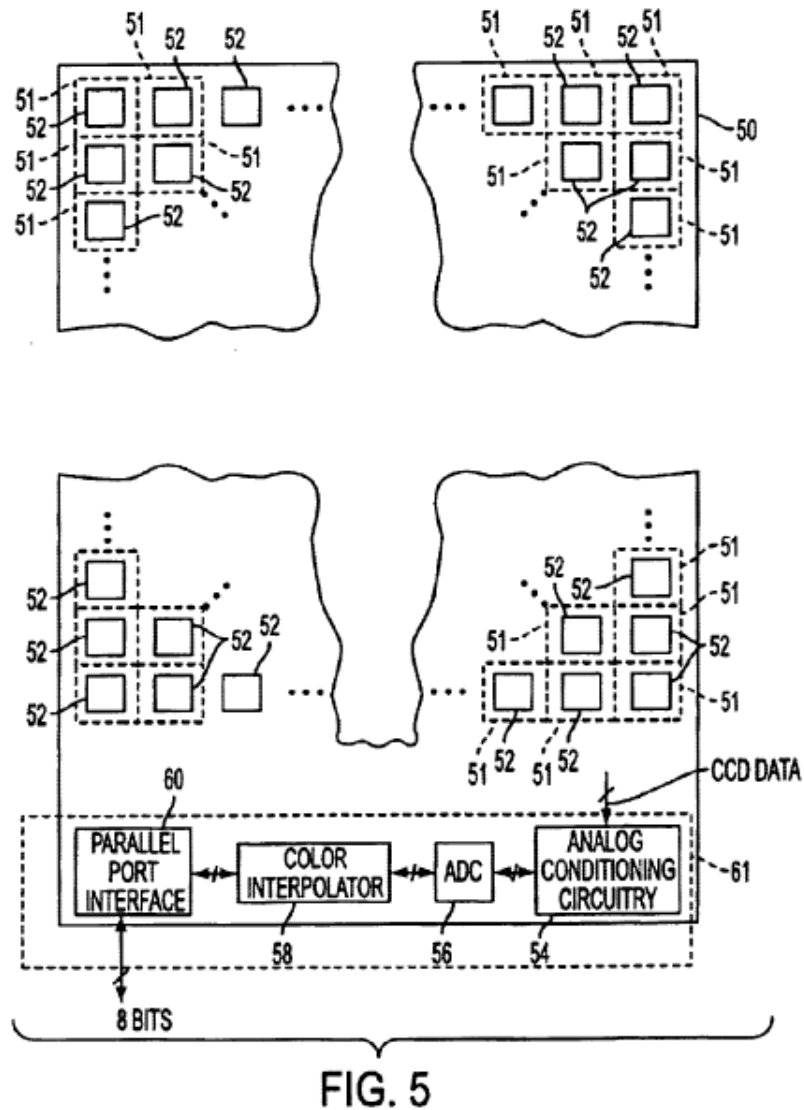
(*Id.*, FIGs. 1, 22 (annotated).)

169. *Isogai* does not explicitly disclose, for this solid state imaging devices that the red pixel, the blue pixel, the first green pixel, the second green pixel, the first analog-to-digital converter, and the second analog-to-digital and the color interpolation circuit are all disposed on a chip as recited in claim 5. However, *Fossum* discloses such a feature and, in my opinion, a person of ordinary skill in the art would have been motivated to combine the teachings of *Fossum* with those of *Isogai* to include all these components in *Isogai* on a single chip as recited in claim 5.

170. As I discussed above in Section IX.C.3, a person of ordinary skill in the art would have understood, based on the disclosure of *Fossum* and their understanding of the state of the art, that implementing the analog-to-digital converters and color processing circuitry on the same chip as the pixel array in an image processing device is a design choice. (See my analysis above in section IX.C.3.) Moreover, as I also discussed above in Section IX.C.3, a person of ordinary skill in the art would have been motivated to include all of these components of an imaging device like that disclosed by *Isogai* on the same chip in order to realize a number of advantages, including increased performance, reduced manufacturing

costs, fewer chips required for smaller applications, and the like. (*See* my analysis above in Section IX.C.3.)

171. Figure 5 of *Fossum* discloses a CMOS imager with analog-to-digital conversion and color interpolation circuitry on the same chip as the pixel array. (Ex. 1008, 4:33-44, FIG. 5.)



(Ex. 1008, FIG. 5.)

172. As *Fossum* discloses, “FIG. 5 shows a CMOS imager 50 located on a monolithic semiconductor substrate, or chip” (*id.*, 4:33-34), without “requiring . . . off chip-color interpolation” (*id.*, 4:40-44). *Fossum* further discloses that “[a]mong

the advantages of the invention” is that [t]rue color imaging occurs on a single semiconductor chip.” (*Id.*, 4:4-6.) Indeed the color interpolation performed on-chip in *Fossum* is the same interpolation disclosed by *Isogai* and the ’651 patent:

The imager 50 has an on chip color interpolator 58 which for each photosensitive site 51 estimates the level of the primary colors that are not sensed by the pixel cell 52 at the photosensitive site 51. The color sensed by the pixel cell 52 is determined by a primary color filter of the site 51 that covers the pixel cell 52. In this manner, the primary color filter (which is a red, green, or blue filter) covers the cell 52. Each cell 52 senses the level of light by measuring the intensity of the light in one of the primary color bands (e.g., red, green or blue) but does not sense the level of light in the other two primary color bands. The interpolator 58 estimates the missing color levels for the site 51 by using the outputs of pixel cells 52 in adjacent photo sensitive sites 51 that are sensing these color levels.

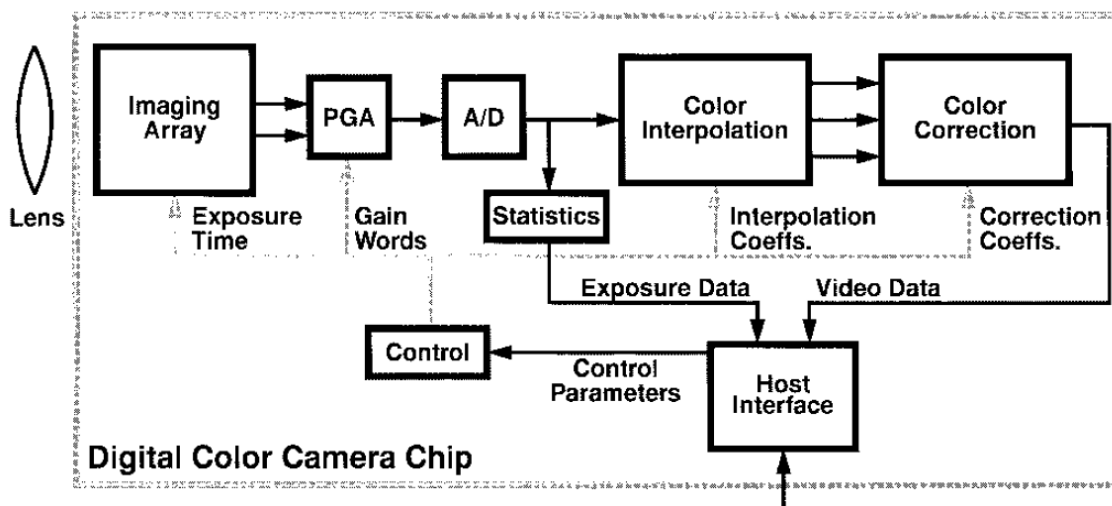
(*Id.*, 4:45-58.)

173. Including the analog-to-digital converters and color processing circuitry on the same chip as the pixel array in the imaging device of *Isogai* would have merely been the use of a known technique (performing analog-to-digital conversion and color processing on the same chip as the pixels as disclosed in

Fossum) for a similar device (the imaging device of *Isogai*) to achieve the expected and desired result of increased integration that can provide increased speed, reduced costs, and support for smaller devices. Additionally, as discussed above, it was known and predictable that imaging circuitry like that described in *Isogai* could have been implemented on either one chip or more than one chip, depending on the needs of the system. Thus, a person of ordinary skill in the art would have had reason to try implementing the circuitry in *Isogai* on either one chip or more than one chip with a reasonable expectation that one would be successful.

174. Therefore, a person of ordinary skill in the art would have been motivated to include *Isogai*'s analog-to-digital converters 80, 81 and color processing circuitry 89 on the same chip as the pixels array as shown in figure 1 of *Isogai* such that the *Isogai-Fossum* combination discloses or suggests "a chip, wherein the red pixel, the blue pixel, the first green pixel, the second green pixel, the first analog-to-digital converter, the second analog-to-digital converter and the color interpolation circuit are disposed on the chip" as recited in claim 5 of the '651 patent. Including the analog-to-digital converters 80, 81 and color processing circuitry in *Isogai*'s solid-state image sensing element as shown in figure 1 would have been straightforward for a skilled person to implement given such a person's knowledge of the state of the art and the disclosure in *Fossum*.

175. Such an understanding is further supported by *Loinaz*. (Ex. 1010.)¹⁰ As shown in figure 1 below, *Loinaz* discloses a digital color camera chip that includes the imaging array, analog-to-digital conversion circuitry, and color interpolation circuitry on the same chip. (Ex. 1010, Abstract, FIG. 1.)



(*Id.*, FIG. 1 (excerpt).)

176. *Loinaz* discloses:

A digital color camera has been monolithically realized in a standard 0.8- μ m CMOS technology. The chip integrates a 354 x 292 photogate sensor array with unity-gain column circuit, a hierarchical column

¹⁰ I refer to *Loinaz* to demonstrate the knowledge of a person of ordinary skill in the art at the relevant time.

multiplexer, a switched-capacitor programmable-gain amplifier, and a 8-b flash analog/digital converter together with digital circuits performing color interpolation, color correction, computation of image statistics, and control functions.

(*Id.*, Abstract (emphasis added).)

177. Therefore, in my opinion, a person of ordinary skill in the art would have been motivated to, and had the capability to, include *Isogai*'s red pixel, blue pixel, first green pixel, second green pixel, first and second analog-to-digital converters, and color processing circuitry on a single chip. As demonstrated by *Fossum*, *Neter*, and *Loinaz*, a person of ordinary skill in the art at the relevant time had the capability to include both the analog-to-digital conversion circuitry and the color processing (color interpolation) circuitry on the same chip. (Ex. 1007, 5:47-52; Ex. 1008, FIGs. 1, 5; Ex. 1010, FIG. 1; *see* my discussion above in Section IX.B.4.) Moreover, in my opinion, a person of ordinary skill in the art would have understood how to make any needed modifications in order to ensure that such integration was possible.

5. Claims 19-22

178. *Isogai* in combination with *Fossum* discloses or suggests the features of claims 19-22 for the same reasons that I discuss above for each of claims 2-5, respectively. (*See* my analysis above in Sections IX.C.2-4.)

D. Inuiya Discloses the Features of Claims 1-3 and 18-20

179. In my opinion, *Inuiya* discloses all of the features of claims 1-3 and 18-20 of the '651 patent.

1. Claim 1

a) **“A solid state imaging device, comprising:”**

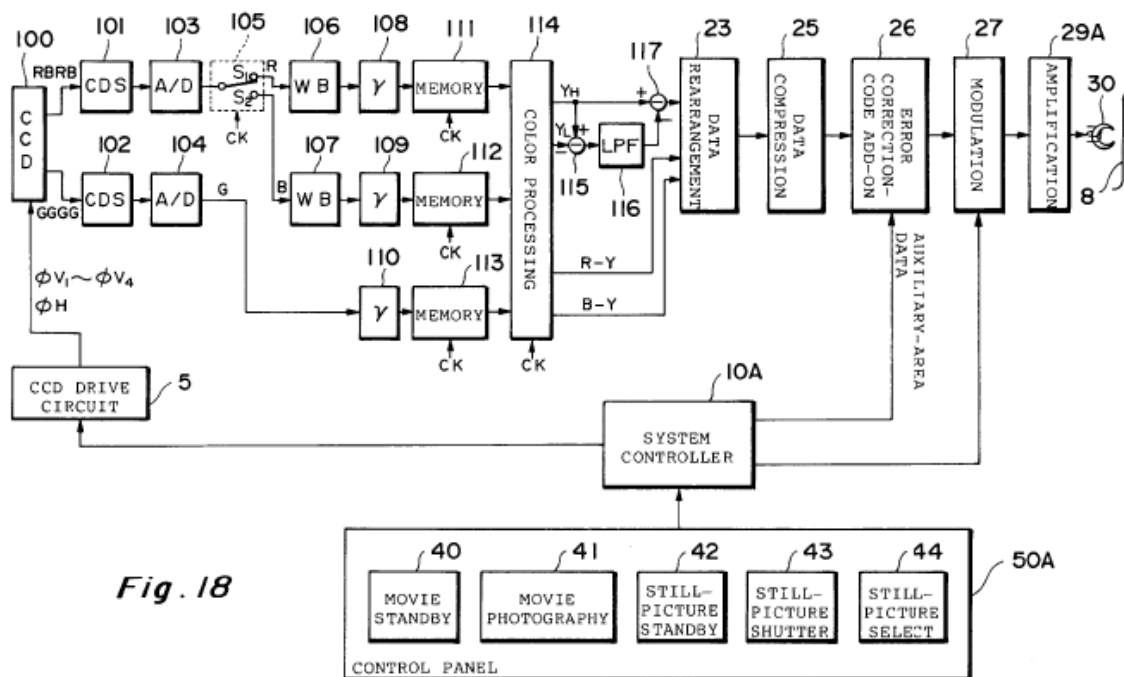
180. I understand that “[a] solid state imaging device, comprising” is the preamble of claim 1. I have been asked to assume that the preamble is limiting. In my opinion, *Inuiya* discloses this feature. For example, *Inuiya* discloses a “a solid-state electronic image sensing device and a method of reading a signal change out of the solid-state electronic image sensing device.” (Ex. 1006, 1:15-18; *see also id.*, 2:20-23 (“Further, an object of the present invention is to realize readout of signal charger, and recording and reproducing of a signal suitably in accordance with number of pixels of a solid state electronic image sensing device.”).) *Inuiya* further discloses:

A solid-state electronic image sensing device according to the present invention comprises photoelectric transducers arrayed in a plurality of columns in the horizontal direction and a plurality of rows in the vertical direction, vertical transfer lines extending in the vertical direction adjacent the columns of photoelectric transducers for transfer, in the vertical direction, signal

charge that has accumulated in the photoelectric transducers, a horizontal transfer line for transferring, in the horizontal direction, signal charge that has been transferred by the vertical transfer lines

(*Id.*, 4:56-67 (emphasis added).)

181. Figure 18 of *Inuiya* is a block diagram of a digital video tape recorder that includes an image sensing section that includes a charge-coupled device (CCD) 100 that includes a large number of pixels. (*Id.*, 20:12-22.)

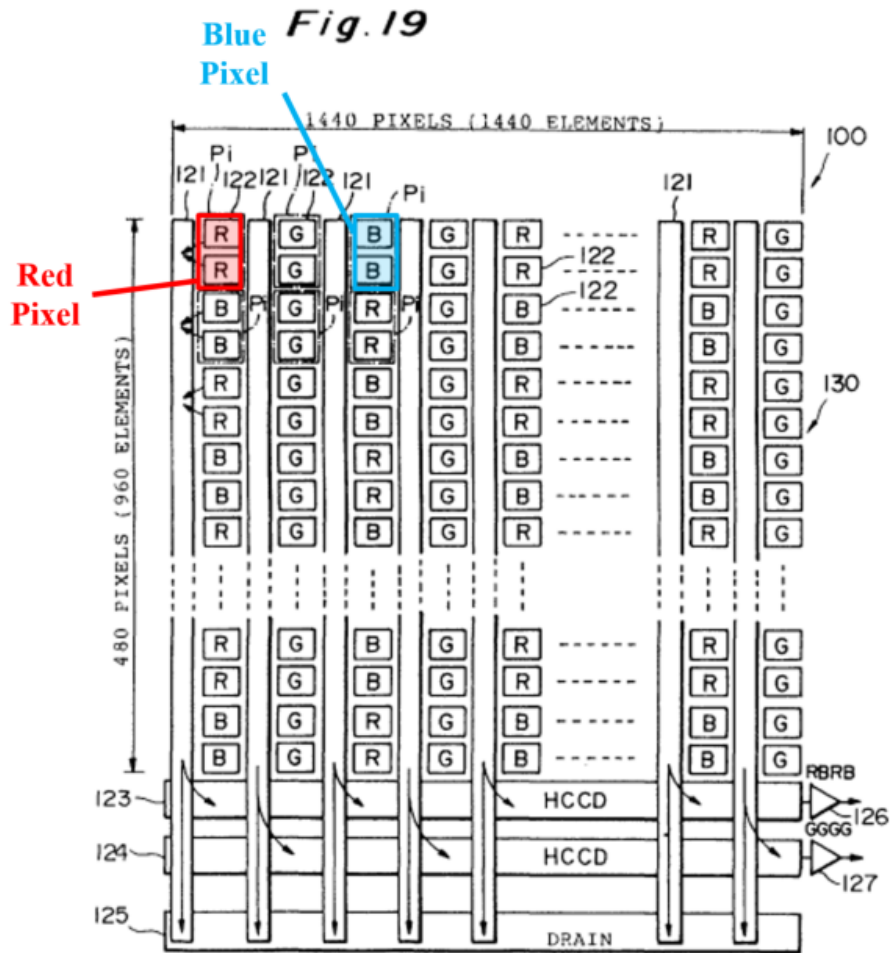


(*Id.*, FIG. 18.) Image data from the CCD 100 is provided to color processing circuit 114, which combines the pixel data to generate luminance and color difference data.

(See my discussion below in Section IX.D.1(h).) *Inuiya*'s digital tape recorder constitutes a solid-state imaging device as recited in claim 1.

- b) **“a red pixel having an output;”**
- c) **“a blue pixel having an output;”**

182. In my opinion, *Inuiya* discloses these features. Figure 19 of *Inuiya* is a schematic view of the CCD 100 included in the solid-state image processing device shown in figure 18. (*Id.*, 20:23.) The CCD 100 includes a plurality of red and blue pixels, including the red pixel made up of the top two photodiodes 122 in the first column and the blue pixel that is made up of the top two photodiodes 122 in the third column highlighted in annotated figure 19 below. *Inuiya* discloses that the signal charges that have accumulated in two photodiodes are mixed in the vertical transfer lines 121 of the CCD 100 such that the pixels, which are labeled “Pi” in figure 19, are each composed of two photodiodes 122. (*Id.*, 20:47-62.)



(*Id.*, FIG. 19 (annotated).)

183. As disclosed by *Inuiya*:

The light-receiving area 130 includes a number of photodiodes 122 arrayed in the horizontal and vertical directions, and vertical transfer lines 121 provided alongside the photodiodes 122 in the vertical direction. Here 1440 photodiodes 122 are provided in the horizontal direction and 960 in the vertical direction. The

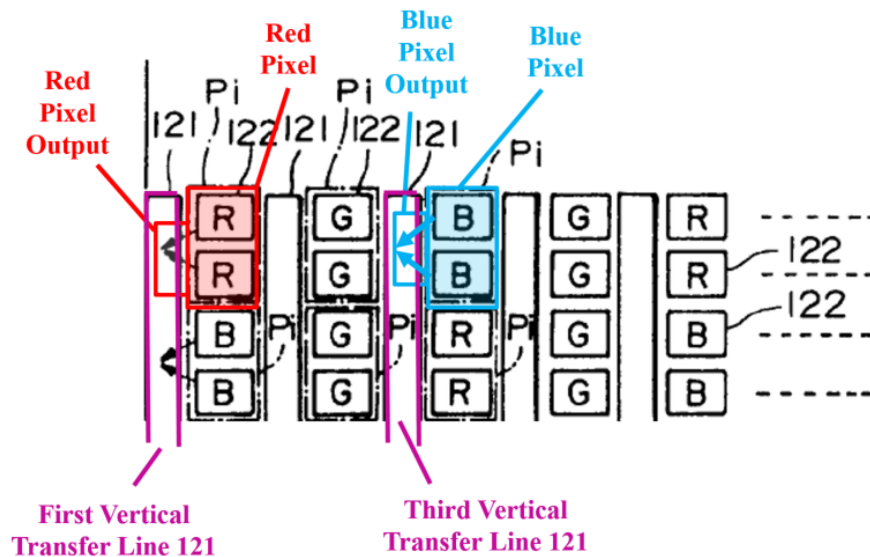
photodiodes 122 in the odd columns each have a red (R) or a blue (B) color filter provide on the light-receiving surface thereof, with the red and blue color filters alternating every two photodiodes 122. The photodiodes 122 in the even columns each have a green (G) color filter provided on the light-receiving surface thereof.

(*Id.*, 20:33-44.)

184. Each of the red and blue pixels in the CCD 100 has an output. As noted above, *Inuiya* discloses that the signal charges that have accumulated in two photodiodes are mixed in the vertical transfer lines 121, and therefore the combination of the outputs from the two photodiodes 122 that make up the pixel correspond to the output of the pixel itself. (*Id.*, 20:47-62, FIG. 19.) A transfer gate is used to control when the charge for each pixel is applied to the vertical transfer line. (*Id.*, 21:7-12 (“Provided between each photodiode 122 and adjacent vertical transfer line 121 is a transfer gate TG, which is for shifting the signal charge that has accumulated in the photodiode 122 to the vertical transfer line 121”) As shown in the enlarged and annotated excerpt of figure 19 below, *Inuiya* includes arrows showing the output of the highlighted red pixel connected to the first vertical transfer line and similar arrows are added in the annotation to show the output of the blue pixel connected to the third vertical transfer line. (*Id.*) Therefore, *Inuiya* discloses

“a red pixel having an output” and “a blue pixel having an output” as recited in claim

1.

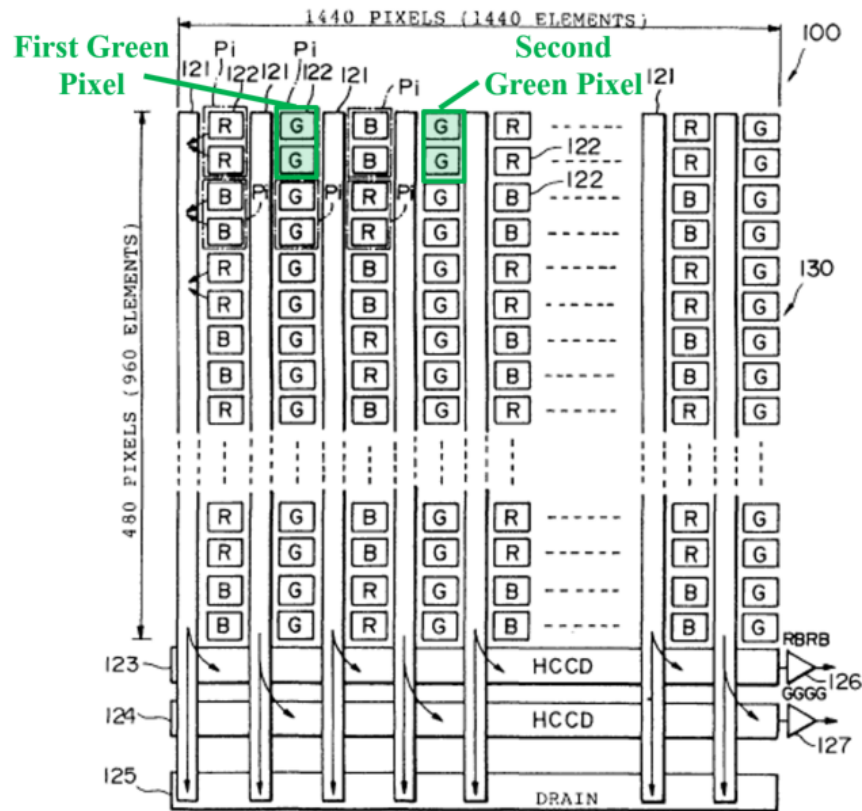


(*Id.*, FIG. 19 (excerpt, annotated).)

- d) **“a first green pixel having an output;”**
- e) **“a second green pixel having an output;”**

185. In my opinion, *Inuiya* discloses these features. The CCD 100 includes a plurality of green pixels, each of which, like the red and blue pixels discussed above in Sections IX.D.1(b)-(c), is made up of two photodiodes. (See my discussion above in Sections IX.D.1(b)-(c); Ex. 1006, 20:33-62.) For example, in the top row of the array, *Inuiya* discloses “a first green pixel” (second column) and a “second green pixel” (fourth column), which are highlighted in annotated figure 19 below.

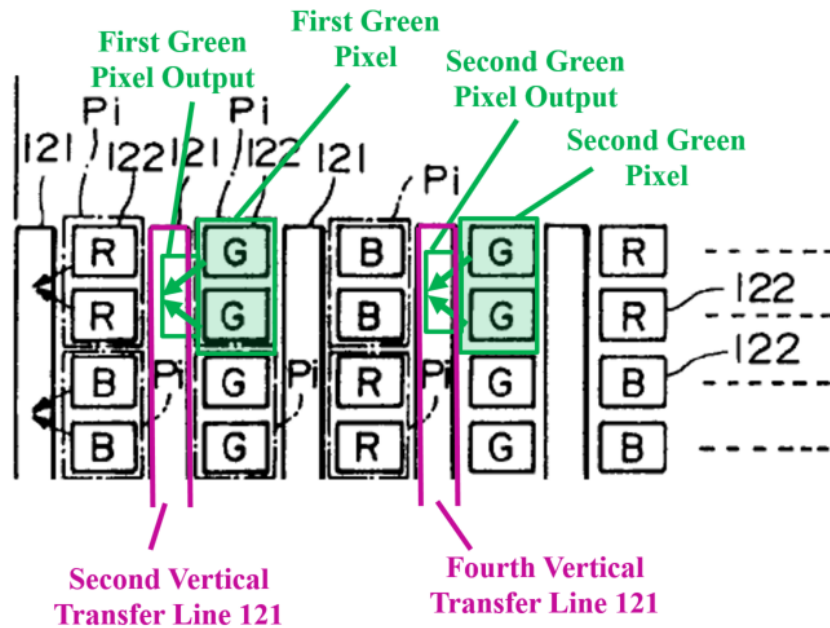
Fig. 19



(Ex. 1006, FIG. 19 (annotated).)

186. As also discussed above with respect to the red and blue pixels in Sections IX.D.1(b)-(c), *Inuiya* discloses that the outputs of the first green pixel and second green pixel highlighted above are connected to vertical transfer lines 121 just to the left of each of the green pixels. (See my discussion above in Sections IX.D.1(b)-(c); Ex. 1006, 20:47-62, 21:7-12, FIG. 19.) As shown in the enlarged and annotated excerpt of figure 19 below, I have included arrows showing the output of

the highlighted first green pixel connected to the second vertical transfer line and the output of the second green pixel connected to the fourth vertical transfer line. (Ex. 1006, 20:47-62, 21:7-12, FIG. 19.) Therefore, *Inuiya* discloses “a first green pixel having an output” and “a second green pixel having an output” as recited in claim 1.



(*Id.*, FIG. 19 (excerpt, annotated).)

- f) “a first analog-to-digital converter connected to the output of the red pixel for converting the output of the red pixel into a first digital signal and connected to the output of the blue pixel for converting the output of the blue pixel into a second digital signal;”
- g) “a second analog-to-digital converter connected to the output of the first green pixel for converting the output of the first green pixel into a third digital signal and connected to the output of the second green pixel for

converting the output of the second green pixel into a fourth digital signal; and”

187. In my opinion, *Inuiya* discloses these features. As discussed above in Sections IX.D.1(b)-(c), the red pixel output is connected to the first vertical transfer line 121, and the blue pixel output is connected to the third vertical transfer line 121. (Ex. 1006, 20:44-53, 21:7-12, FIG. 19; *see* my discussion above in Sections IX.D.1(b)-(c).) Similarly, the first green pixel output is connected to the second vertical transfer line 121, and the second green pixel output is connected to the fourth vertical transfer line 121. (Ex. 1006, 20:44-53, 21:7-12, FIG. 19; *see* my discussion above in Sections IX.D.1(d)-(e).) As shown in annotated figure 19 below, the first and third vertical transfer lines 121 are connected to the horizontal transfer line 123, whereas the second and fourth vertical transfer lines are connected to the horizontal transfer line 124. As disclosed by *Inuiya*:

In the CCD 100 illustrated in FIG. 19 and in FIGS. 20a, b and c, the CCD includes the first horizontal transfer line 123 and the second horizontal transfer line 124. The first horizontal transfer line 123 transfers the signal charge that has accumulated in the photodiodes 122 of odd columns, namely the R (red) data and the B (blue) data, in the horizontal direction, and the second horizontal transfer line 124 transfers the signal charge that has accumulated in the photodiodes 122 of even columns, namely the G

(green) data, in the horizontal direction. The signal charges outputted by first horizontal transfer line 123 and second horizontal transfer line 124 are converted to voltage signals in the floating diffusion amplifiers 126 and 127 and these signals become the outputs of the CCD 100.

(Ex. 1006, 21:36-49.)

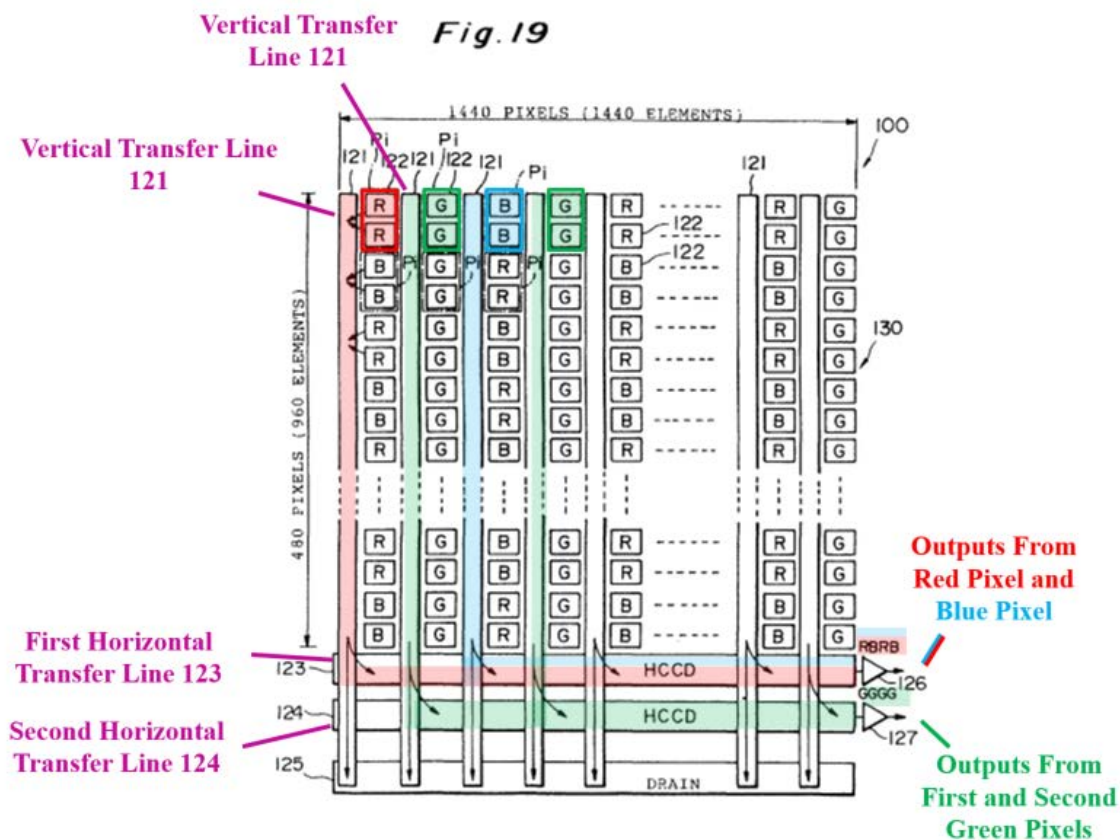
188. *Inuiya* discloses that pulses are applied to control the mixing of the charge corresponding to photodiodes included in a pixel in the vertical transfer lines, where the charge for the pixels is shifted from the vertical transfer lines to the horizontal transfer lines on a pixel-by-pixel basis so that the charge for one pixel is presented in a sequential manner on each of the horizontal transfer lines. (*Id.*, 22:1-23:25.) For example, *Inuiya* discloses:

The vertical transfer lines 121 are connected to the horizontal transfer lines 122 and 123 in such a manner that the signal charge that has accumulated in the photodiodes 122 of the odd rows is applied to the first horizontal transfer line 123 and signal charge that has accumulated in the photodiodes 122 of the even rows is applied to the second horizontal transfer line 123. As a result, the signal charge representing the R data and B data is transferred through the first horizontal transfer line and the signal charge representing the G data is transferred through the second horizontal transfer line 124. Transfer of the signal

charge in the first horizontal transfer line 123 and second horizontal transfer line 124 ends before the next set of transfer pulses $\phi V_1 \sim \phi V_4$ is applied to the transfer electrodes $\phi V_1 \sim \phi V_4$. In the CCD 100 of the present embodiment, the first horizontal transfer line 123 is used for transfer with regard to the R and B data in the data of all pixels, and the second horizontal transfer line 1234 is used for transfer with regard to the G data. This means that the amount of data transferred in one horizontal transfer line becomes half the amount of data of all pixels. Accordingly, even though the CCD 100 is one having a large number of pixels, transfer of signal charge is possible using comparatively slow horizontal transfer pulses. Application of the vertical transfer pulses $\phi V_1 \sim \phi V_4$ to the vertical transfer electrodes $\phi V_1 \sim \phi V_4$ is repeated in alternation with application of the horizontal transfer pulses to the horizontal transfer lines so that the signal charge of all of the approximately 700,000 pixels is outputted from the CCD 100 upon being divided into the R data and the B and G data.

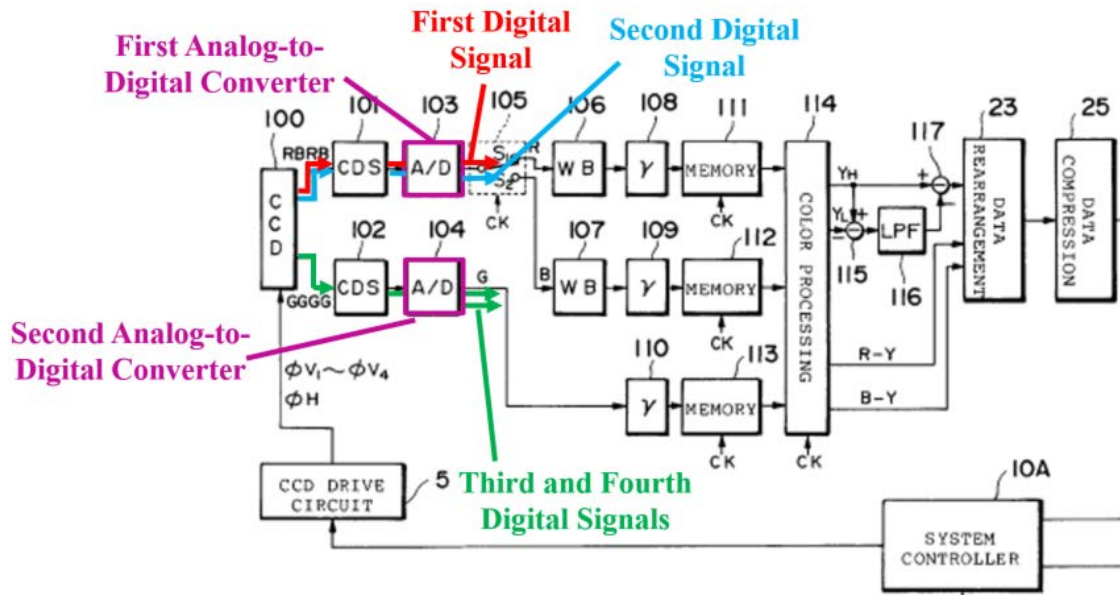
(*Id.*, 22:63-23:25.)

189. Therefore, outputs of the red and blue pixels are output by amplifier 126 and the first/second green pixel outputs are output by amplifier 127. (*Id.*, 21:36-62, FIG. 19; *see also id.*, 23:10-14.)



(*Id.*, FIG. 19 (annotated).)

190. As shown in the annotated excerpt of figure 18 below, *Inuiya* discloses that the output signals from the CCD 100 are provided through correlated data sampling circuits 101, 102 to analog-to-digital converters 103, 104. (*Id.*, 25:36-43.)



(*Id.*, FIG. 18 (excerpt, annotated).)

191. As shown in the annotated excerpt of figure 18 above, the outputs of the red and blue pixels (“RBRB”) are “outputted alternately by the first horizontal transfer line 123” and provided to the CDS circuit 101 and then to the analog-to-digital converter (A/D) 103, and the outputs of the first and second green pixels (GGGG) are sequentially provided to the analog-to-digital converter (A/D) 104. (*Id.*, 25:36-43 (“The **R signal and B signal** contained in the video signal from the CCD 100 and outputted alternately by the horizontal transfer line 123 are applied to CDS (correlated double sampling) circuit 101, and the G signal contained in the video signal is applied to a CDS circuit 102. The CDS circuit 101 removes kTC noise from **the R and B signals, which are then converted to digital image data in an**

analog/digital converter circuit 103.”) (emphasis added).) A person of ordinary skill in the art would have understood that the analog-to-digital converter 103 is “connected to” the outputs of the red and blue pixels and the analog-to-digital converter 104 is “connected to” the outputs of the first and second green pixels as those analog-to-digital converters receive and convert the analog signals from those outputs into digital image data.

192. Moreover, the digital image data generated by the analog-to-digital converter 103 includes a “first digital signal” corresponding to the red pixel output and a “second digital signal” corresponding to the blue pixel output. The red and blue pixel outputs are sequentially provided from the CCD 100 to the CDS block 101 and A/D 103. The digital image data generated by the analog-to-digital converter 103 includes a “first digital signal” that is output when the red pixel is provided to A/D 103 and a “second digital signal” that is output when the blue pixel output is provided to the A/D 103. *Inuiya* discloses that a switch 105 is used to direct the digital red pixel data, including the “first digital signal” for the “red pixel” as well as other digital signals corresponding to other red pixels to the S1 side of the switch and white-balance circuit 106, whereas the switch 105 directs the digital blue pixel data, including the “second digital signal” for the “blue pixel” as well as other

digital signals corresponding to other blue pixels to the S2 side of the switch and white-balance circuit 107. (*Id.*, 25:43-55.)

193. Similarly, the first and second green pixel outputs are sequentially provided from the CCD 100 to the CDS block 101 and A/D 103. *Inuiya* discloses the G signals are converted into a digital G data, including the “third digital signal” for the “first green pixel,” the “fourth digital signal” for the “second green pixel,” and other digital signals corresponding to other green pixels. (*Id.*, 25:55-59.) All of the digital green pixel data is output as a sequential stream of digital data from the A/D 104 to the gamma correction block 110. (*Id.*, *see id.*, FIG. 18.) *Inuiya* discloses that there is twice as much green digital data as red or blue digital data because there are two green pixels for every red and blue pixel. (*Id.*, 25:60-26:12.)

194. The analog-to-digital converter 103 constitutes “a first analog-to-digital converter connected to the output of the red pixel for converting the output of the red pixel into a first digital signal and connected to the output of the blue pixel for converting the output of the blue pixel into a second digital signal” as recited in claim 1. Similarly, the analog-to-digital converter 104 shown in the annotated demonstrative above constitutes “a second analog-to-digital converter connected to the output of the first green pixel for converting the output of the first green pixel into a third digital signal and connected to the output of the second green pixel for

converting the output of the second green pixel into a fourth digital signal” as recited in claim 1.

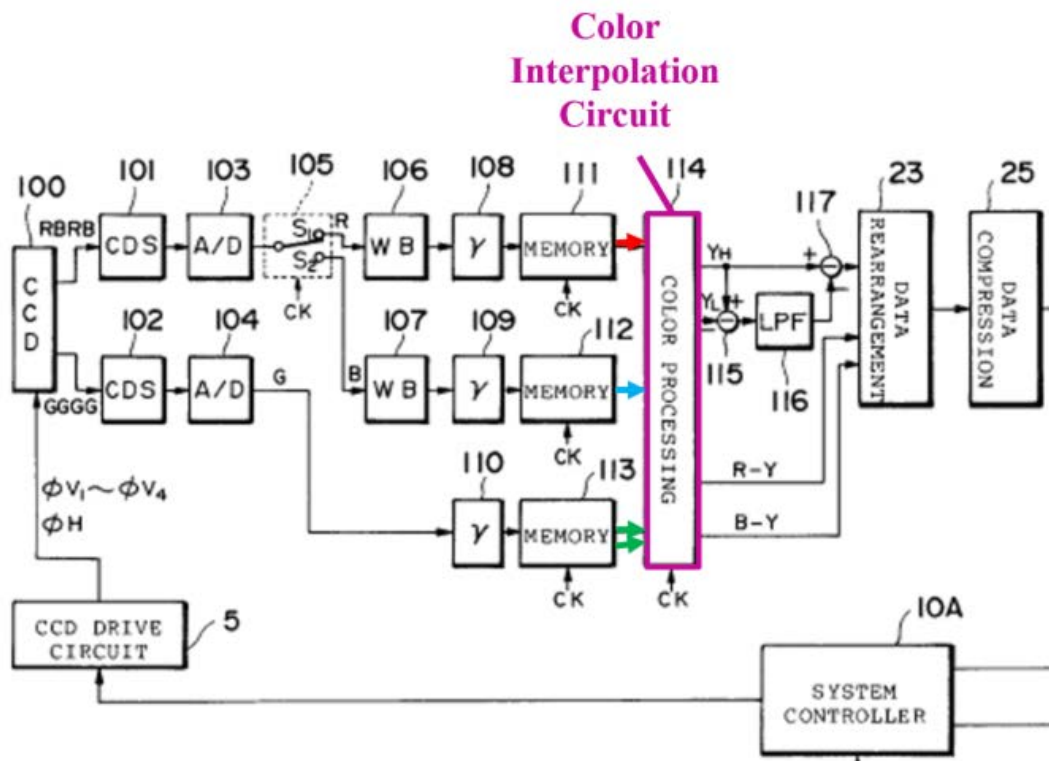
h) **“a color interpolation circuit for combining the first, second, third and fourth digital signals.”**

195. In my opinion, *Inuiya* discloses this feature. As discussed above in Sections IX.D.1(f)-(g), the analog-to-digital converters 103 and 104 convert the outputs of red, blue, first green, and second green pixels into the first, second, third, and fourth digital signals, respectively. (*See* my discussion above in Sections IX.D.1(f)-(g).) *Inuiya* further discloses that the first and second digital signals corresponding to the red and blue pixels are applied to white-balance adjustment circuits 106 and 107 and then are gamma corrected by gamma-correction circuits 108 and 109 before being stored in memories 111 and 112. (Ex. 1006, 25:49-63, FIG. 18.) The third and fourth digital signals corresponding to the first green pixel and the second green pixel are gamma-corrected by gamma-correction circuit 110 and then stored in memory 113. (*Id.*, 25:58-63 (“A gamma correction is applied to the R data, B data and G data in the gamma-correction circuits 108, 109 and 110, respectively after which the corrected data is applied to memories 111, 112 and 113.”), FIG. 18.)

196. The digital pixel data stored in the memories 111-113 is then processed by the color processing block, which combines the first, second, third and fourth digital signals. *Inuiya* discloses that:

The R, B and G image data represented in conformity with the delta array of the CCD 100 as shown in FIG. 27 is divided solely into items of R, B and G data, as illustrated in FIGS. 28a, b and c, and the image data is stored in the memories 111, 112 and 113 in such a manner that the data of the pixels in identical rows of the CCD becomes the data of identical rows in the memories 111, 112 and 113. The R, G and B image data that has been stored in the memories 111, 112 and 113 is read out of the respective memories 111, 112 and 113 and applied to a color processing circuit 114. The latter generates and outputs luminance data Y_H of high-frequency components, luminance data Y_L of low-frequency components as well as R-Y and B-Y color difference data from the input R, B and G data.

(*Id.*, 26:5-19.)



(*Id.*, FIG. 18 (excerpt, annotated).)

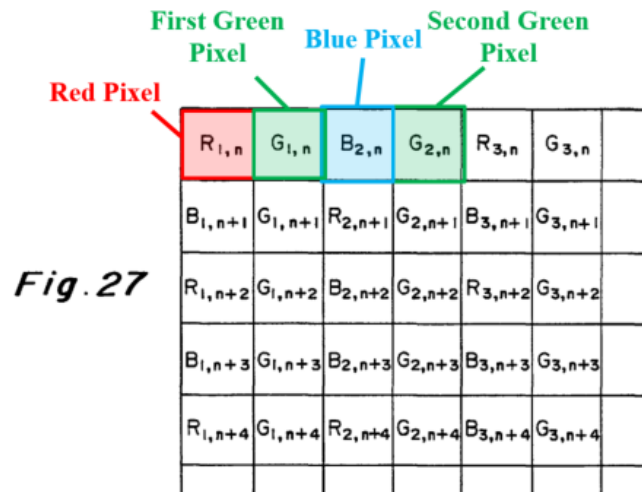
197. *Inuiya* further discloses that the generation of the luminance and R-Y and B-Y color-difference data includes combining the digital signals corresponding to the red, blue, first green, and second green pixels:

Described next will be the processing executed by the color processing circuit 114 to generate the luminance data Y_H containing the high-frequency components, the luminance data Y_L containing the low-frequency components, as well as the R-Y and B-Y color-difference data.

FIG. 29 illustrates a procedure through which the wideband luminance data Y_H containing the high-frequency components is generated from the R, B and G data provided by the memories 111, 112 and 113, respectively.

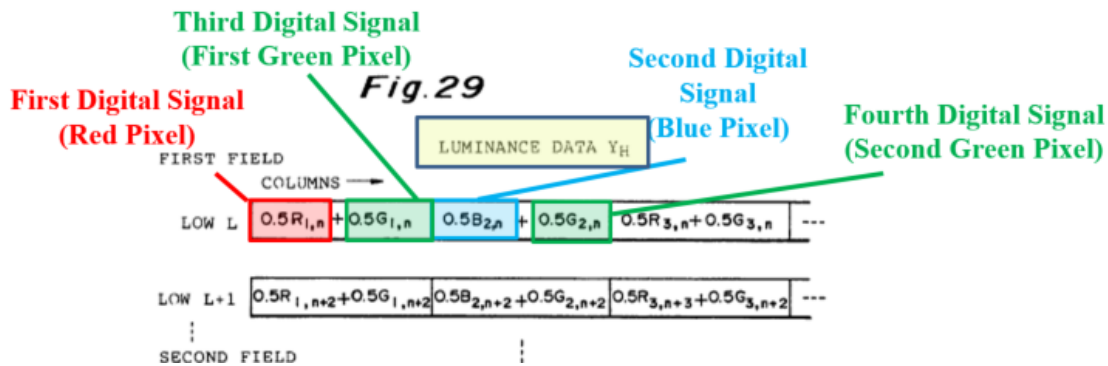
(*Id.*, 27:10-18.)

198. As shown in figure 29, generation of the luminance data includes combining the digital signals corresponding to the red pixel, the blue pixel, the first green pixel, and the second green pixel. (*Id.*, FIGs. 27, 29.) For example, the red pixel, the blue pixel, the first green pixel, and the second green pixel are highlighted in annotated figure 27 below.



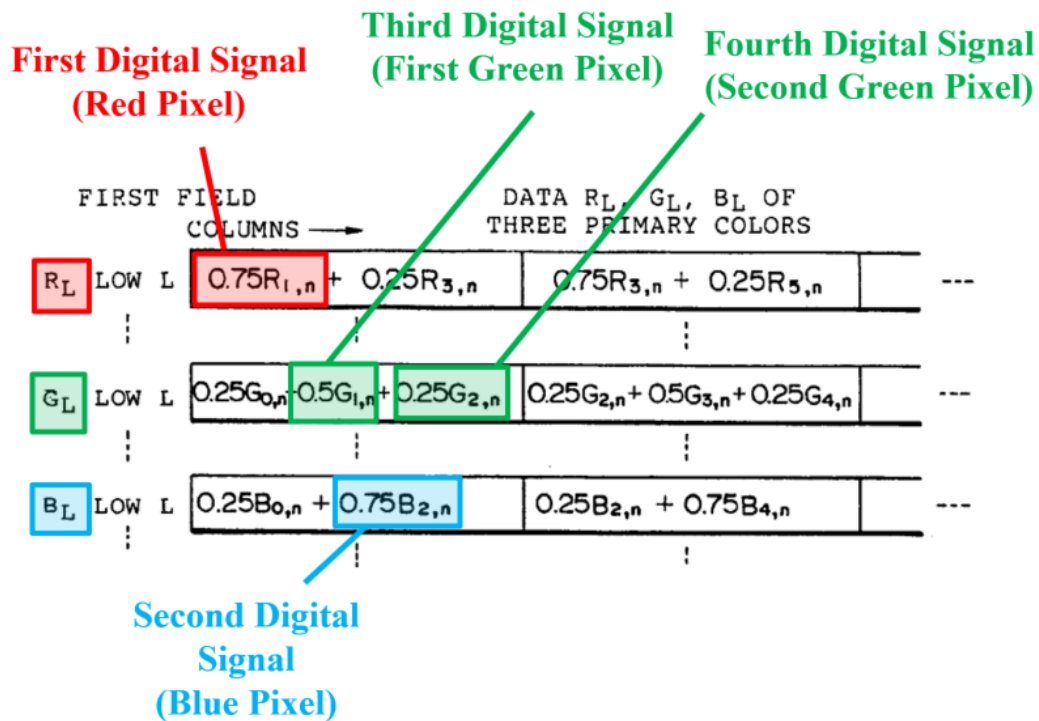
(*Id.*, FIG. 27 (annotated).)

199. As shown in the annotated excerpt of figure 29 below, the first, second, third, and fourth digital signals are combined by the color processing circuit 114 to generate the luminance data Y_H .



(*Id.*, FIG. 29 (excerpt, annotated).)

200. *Inuiya* further discloses that the pixel outputs for the red, blue, first green, and second green pixels are combined in calculating the luminance data Y_L of the low-frequency components. Specifically, figure 30 of *Inuiya* shows that the outputs for the red, blue, first green, and second green pixels are included in calculating R_L , G_L , and B_L :



(*Id.*, FIG. 30 (excerpt, annotated).)

201. *Inuiya* further discloses that the luminance data Y_L of the low-frequency components is calculated using the R_L , G_L , and B_L values calculated according to figure 30:

When the R_L data, G_L data and B_L data is generated for each of the first, second, third and fourth fields, the luminance data Y_L of the low-frequency components is generated, for each of the first, second, third and fourth fields, from the R_L data, G_L data and B_L data in accordance with the following equation:

$$Y_L = 0.3\textcolor{red}{R}_L + 0.59\textcolor{green}{G}_L + .11\textcolor{blue}{B}_L \quad (\text{Eq. (1)})$$

(*Id.*, 28:49-57 (equation annotated).)

202. As demonstrated above, the digital signals corresponding to the red, blue, first green, and second green pixels are combined by the color processing block 114. (*Id.*, FIGs. 27, 29.) Therefore, the color processing block 114 constitutes a “color interpolation circuit for combining the first, second, third and fourth digital signal.”

2. Claim 2

- a) **“The solid stage imaging device of claim 1, further comprising an error compensation circuit for correcting a gain of one of the output of the red pixel, the output of the blue pixel, the output of the first green pixel and the output of the second green pixel.”**

203. In my opinion, *Inuiya* discloses this feature in a manner consistent with that of the '651 patent. Specifically, the '651 patent shows the error compensation circuit operating on digital signals output from the A/D converters. (Ex. 1001, FIGs. 1-3.)

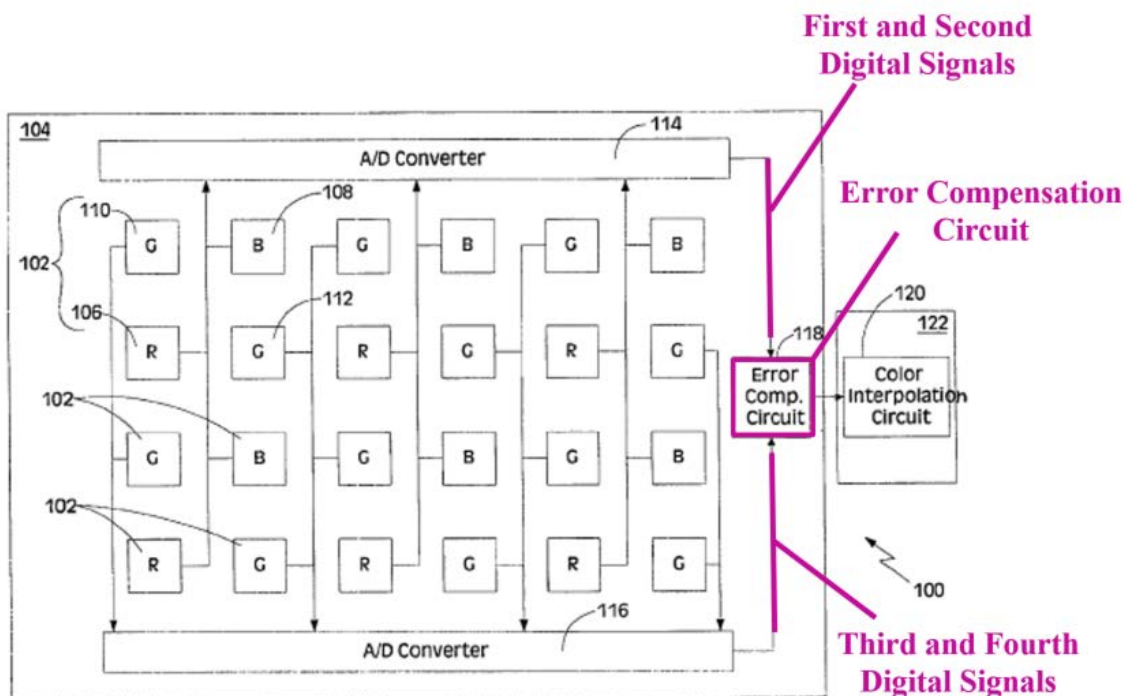


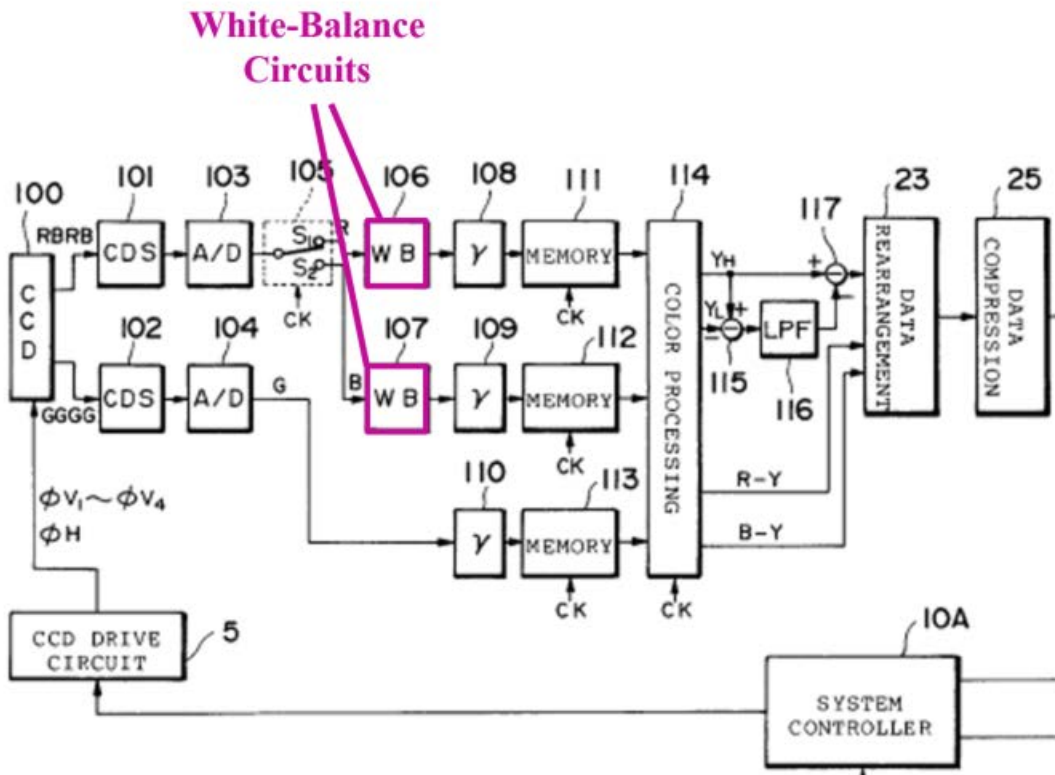
FIG. 1

(*Id.*, FIG. 1.)

204. Therefore, while claim 2 indicates that the error compensation circuit corrects gain of one of the outputs of the red, blue, and first and second green pixels, those outputs, which are initially analog signals, are converted to digital signals by the A/D converters prior to being provided to the error compensation circuit. (*Id.*, FIGs. 1-3.) Therefore, while the scope of claim 2 is not clear, I have been asked to assume that the scope of claim 2 includes correcting gain of one of the outputs of the

red, blue, first green, or second green pixels after the digital-to-analog conversion has been completed. With such an assumption in mind, *Inuiya* discloses this feature.

205. As shown in the annotated excerpt of figure 18 below, *Inuiya* discloses that, the outputs of the red and blue pixels are provided from the CCD 100 (“RBRB”) to the analog-to-digital converter (A/D) 103. (*Id.*, 25:36-43 (“The R signal and B signal contained in the video signal from the CCD 100 and outputted alternately by the horizontal transfer line 123 are applied to CDS (correlated double sampling) circuit 101, and the G signal contained in the video signal is applied to a CDS circuit 102. The CDS circuit 101 removes kTC noise from the R and B signals, which are then converted to digital image data in an analog/digital converter circuit 103.”).) The output of the analog-to-digital converter 103 is then provided to white balance adjustment circuits 106 and 107 that apply white-balance adjustment to the red and blue pixel data. (Ex. 1006, 25:49-55 (“The serial R data and B data is converted to parallel R data and B data by the changeover switch 105, and the parallel R and B data is applied to white-balance adjustment circuits 106 and 107, respectively. The **white-balance circuits 106 and 107 apply a white-balance adjustment** and apply the adjusted R and B data to gamma-correction circuits 108 and 109 respectively.”) (emphasis added).)



(*Id.*, FIG. 18 (excerpt, annotated).)

206. A person of ordinary skill in the art would have understood that white-balance adjustment involves inserting equalizing gain for one or more of the color components to correct for sensor sensitivity variation across the radiation spectrum.

Yiannoulous confirms this understanding of a person of ordinary skill in the art:

White balancing:

In another embodiment of the present invention the proportionality constant (T/I_r) of Eq. 1, is used as a parameter to advantageously implement the white

balancing function required in color imaging applications.

White balancing corrects for sensor sensitivity variations across the radiation spectrum. A silicon based photo-sensor for example, is most sensitive near the green part, and least sensitive in the blue part of the visible spectrum. A color camera **compensates for these differences by inserting equalizing gain in the separate color components of its signal path.**

(Ex. 1013, 9:60-10:3 (emphasis added).)¹¹

207. Similarly, as evidenced by *Loinaz*, a person of ordinary skill in the art would have understood that white balancing requires amplification of the output signals corresponding to pixels of certain colors. (Ex. 1010, 2094 (“To achieve white balance, it is evident from Fig. 4 that the outputs of the blue and green pixels must be amplified with respect to the outputs of the red pixels.”).)¹² Therefore, a person of ordinary skill in the art would have understood that the white-balance circuits in *Inuiya* correct the gain for the blue and red pixels. Notably, the ’651

¹¹ I refer to *Yiannoulos* to demonstrate the knowledge of a person of ordinary skill in the art at the relevant time.

¹² I refer to *Loinaz* to demonstrate the knowledge of a person of ordinary skill in the art at the relevant time.

patent simply states that the error compensation circuit “provides an independent gain to correct the gain for each color channel” (Ex. 1001, 5:3-5), “corrects the gain and the fixed pattern noise offset for each color channel” (*id.*, 5:41-43), and “is used to correct the gain and the fixed pattern noise offset for each pixel” (*id.*, 5:35:66-6:10.) While the ’651 patent indicates that “[s]mall adjustments to the gain and offset can be self-calibrated by the imager 100 by the self-testing of black and white reference rows each time the imager 100 is powered” and that “[t]he correction coefficients for the pair of green A/D converters 116 can then be automatically derived and stored on chip static RAM,” the ’651 patent does not further specify or explain what “corrects the gain” entails. (*Id.*, 5:7-12.)

208. Therefore, in my opinion, because *Inuiya* discloses white balancing circuits that perform gain control on the red and blue pixels, *Inuiya* discloses “an error compensation circuit for correcting a gain of one of the output of the red pixel, the output of the blue pixel, the output of the first green pixel and the output of the second green pixel” as recited in claim 2 in a manner consistent with the disclosure of the ’651 patent.

3. Claim 3

- a) **“The solid stage imaging device of claim 1, further comprising an error compensation circuit for correcting a fixed pattern noise offset from one of the output of the red pixel, the output of the blue pixel, the**

output of the first green pixel and the output of the second green pixel.”

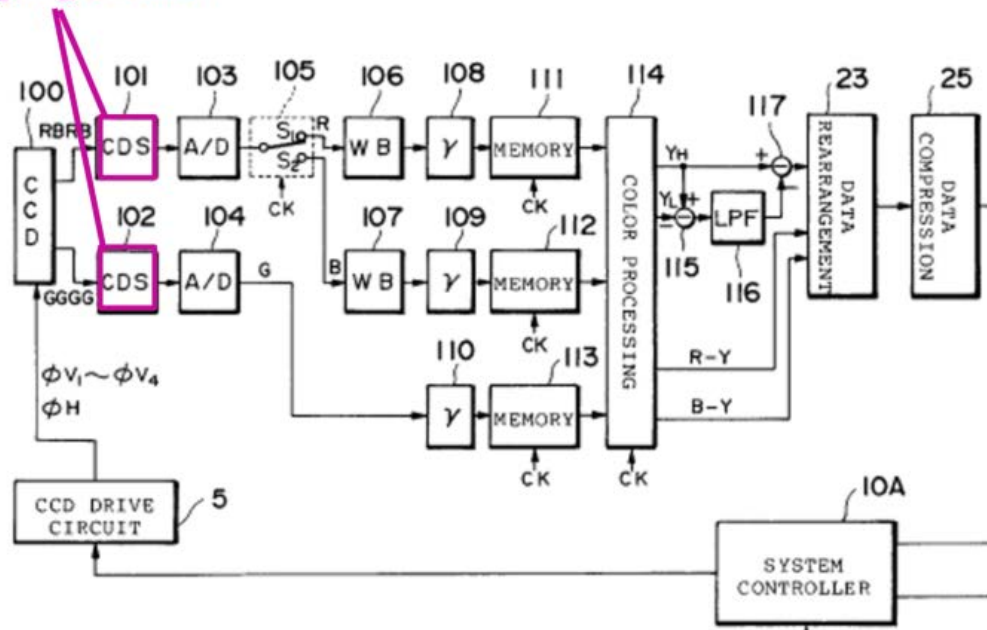
209. In my opinion, *Inuiya* discloses this feature. While the '651 patent shows the error compensation circuit operating on digital signal output from the A/D converters (Ex. 1001, FIGs. 1-3), claim 3 indicates that the error compensation circuit corrects a fixed pattern noise offset from one of the outputs of the red, blue, and first and second green pixels, where those outputs are the analog signals that have not yet been converted to digital signals by the A/D converters. I have been asked to assume that, for purposes of the present analysis, the scope of claim 3 includes correcting a fixed pattern noise offset from one of the analog outputs of the red, blue, first green, and second green pixels. With such an assumption in mind, *Inuiya* discloses this feature.

210. As shown in the annotated excerpt of figure 18 below, *Inuiya* discloses that, the outputs of the red and blue pixels are provided from the CCD 100 (“RBRB”) to the analog-to-digital converter (A/D) 103. (Ex. 1006, 25:36-43 (“The R signal and B signal contained in the video signal from the CCD 100 and outputted alternately by the horizontal transfer line 123 are applied to CDS (correlated double sampling) circuit 101, and the G signal contained in the video signal is applied to a CDS circuit 102. The CDS circuit 101 removes kTC noise from the R and B signals, which are then converted to digital image data in an analog/digital converter circuit

103.”.) A person of ordinary skill in the art would have understood that the double sampling performed by the correlated double sampling (CDS) circuits 101 and 102 reduces fixed pattern noise (“error compensation circuit for correcting a fixed pattern noise offset”) in the pixel outputs. (Ex. 1011, 7:34-38 (“on-chip correlated doubling sampling can be implemented in many active pixel sensors to **suppress noise such as the fixed pattern noise** and the kTC noise.”) (emphasis added); Ex. 1012, 40:17-23 (“signal conversion 51b includes a CDS (Correlated Double Sampling) 110d” “[t]he CDS 110d samples and holds the output of the image pick-up 51d two times and performs subtraction with the resulting two signal levels in order to reduce noise.”).)¹³

¹³ I refer to *Yadid-Pecht* and *Inuiya-364* to demonstrate the knowledge of a person of ordinary skill in the art at the relevant time.

**Correlated Double
Sampling Circuits**



(*Id.*, FIG. 18 (excerpt, annotated).)

211. A person of ordinary skill in the art would have understood that the correlated double sampling circuits 101, 102 reduce fixed pattern noise for the red, blue, and green pixels. Therefore, in my opinion, *Inuiya* discloses an “error compensation circuit for correcting a fixed pattern noise offset from one of the output of the red pixel, the output of the blue pixel, the output of the first green pixel and the output of the second green pixel” as recited in claim 3.

4. Claim 18

a) “An imaging method comprising:”

212. I understand that “[a]n imaging method, comprising” is the preamble of claim 18. I have been asked to assume that the preamble is limiting. In my opinion, *Inuiya* discloses this feature. As discussed above in Section IX.D.1(a), *Inuiya* discloses a digital tape recorder that constitutes a solid-state imaging device, where the operation of such an imaging device, which includes the capture and processing of pixel data, constitutes an “imaging method.” (See my analysis above in Section IX.D.1(a).)

b) “converting an output of a red pixel into a first digital signal using a first analog-to-digital converter;”

c) “converting an output of a blue pixel into a second digital signal using the first analog-to-digital converter;”

213. In my opinion, *Inuiya* discloses these limitations. As I discussed above in Sections IX.D.1(b)-(c), *Inuiya* discloses a red pixel and a blue pixel, each of which has a corresponding “output.” (See my analysis above in Sections IX.D.1(b)-(c).) As I also discussed above in Section IX.D.1(f), the outputs of the red and blue pixels are converted to first and second digital signals, respectively, by a first analog-to-digital converter. (See my analysis above in Section IX.D.1(f).)

d) converting an output of a first green pixel into a third digital signal using a second analog-to-digital converter;”

e) “converting an output of a second green pixel into a fourth digital signal using the second analog-to-digital converter; and;”

214. In my opinion, *Inuiya* discloses these limitations. As I discussed above in Sections IX.D.1(d)-(e), *Inuiya* discloses a first and second green pixel, each of which has a corresponding “output.” (See my analysis above in Sections IX.D.1(d)-(e).) As I also discussed above in Section IX.D.1(g), the outputs of the first and second green pixels are converted to third and fourth digital signals, respectively, by a second analog-to-digital converter. (See my analysis above in Section IX.D.1(g).)

f) combining the first, second, third and fourth digital signals using a color interpolation circuit.”

215. In my opinion, *Inuiya* discloses these limitations. As I discussed above in Section IX.D.1(h), *Inuiya* discloses “combining the first, second, third and fourth digital signals using a color interpolation circuit.” (See my analysis above in Section IX.D.1(h).)

5. Claim 19

a) “The imaging method of claim 18 further comprising: correcting a gain of one of the output of the red pixel, the output of the blue pixel, the output of the first green pixel and the output of the second green pixel.”

216. In my opinion, *Inuiya* discloses this feature for the reasons I discuss above with respect to claim 2. (See my analysis above in Section IX.D.2.)

6. Claim 20

- a) **“The imaging method of claim 18 further comprising: correcting a fixed pattern noise offset from one of the output of the red pixel, the output of the blue pixel, the output of the first green pixel and the output of the second green pixel.”**

217. In my opinion, *Inuiya* discloses this feature for the reasons I discuss above with respect to claim 3. (See my analysis above in Section IX.D.3.)

E. *Inuiya* in Combination with *Neter* Discloses or Suggests the Features of Claims 4-5 and 21-22

1. Claim 4

- a) **“The solid stage imaging device of claim 1 further comprising a first chip and a second chip, wherein the red pixel, the blue pixel, the first green pixel, the second green pixel, the first analog-to-digital converter and the second analog-to-digital converter are disposed on the first chip and the color interpolation circuit is disposed on the second chip.”**

218. In my opinion, *Inuiya* in combination with *Neter* discloses or suggests these features. As I discussed above in Section IX.B.3, a person of ordinary skill in the art would have understood that implementing the components of an imaging device on two chips would have been an apparent combination and/or design choice. (See my discussion above in Section IX.B.3.) *Inuiya*, like *Isogai* and *Neter*, discloses an imaging device with a pixel array, analog-to-digital converters, and color processing circuitry. Therefore, for the same reasons discussed above with respect

to *Isogai* in combination with *Neter* in Section IX.B.3, a person of ordinary skill in the art would have been motivated to combine the teachings of *Inuiya* and *Neter* with a reasonable expectation of success such that *Inuiya*'s analog-to-digital converters are on the same chip as the pixel array, while maintaining the color processing circuitry on a second chip.

2. Claim 5

- a) **“The solid stage imaging device of claim 1 further comprising a chip, wherein the red pixel, the blue pixel, the first green pixel, the second green pixel, the first analog-to-digital converter, the second analog-to-digital converter and the color interpolation circuit are disposed on the chip.”**

219. In my opinion, *Inuiya* in combination with *Neter* discloses or suggests this feature. As discussed above in Section IX.B.4, a person of ordinary skill in the art would have understood that implementing the components of an imaging device on one chip would have been an apparent combination and/or design choice. (See my discussion above in section IX.B.4.) *Inuiya*, like *Isogai* and *Neter*, discloses an imaging device with a pixel array, analog-to-digital converters, and color processing circuitry. Therefore, for the same reasons discussed above with respect to *Isogai* in combination with *Neter* in Section IX.B.4, a person of ordinary skill in the art would have been motivated to combine the teachings of *Inuiya* and *Neter* with a reasonable

expectation of success such that *Inuiya*'s analog-to-digital converters and color processing circuitry are on the same chip as the pixel array.

3. Claims 21-22

220. In my opinion, *Inuiya* in combination with *Neter* discloses or suggests the features of claims 21-22 for the same reasons that I discuss above for each of claims 4-5, respectively. (See my analysis above in Sections IX.E.1-2.)

F. *Inuiya* in Combination with *Fossum* Discloses or Suggests the Features of Claims 4-5 and 21-22

1. Claim 4

- a) **“The solid stage imaging device of claim 1 further comprising a first chip and a second chip, wherein the red pixel, the blue pixel, the first green pixel, the second green pixel, the first analog-to-digital converter and the second analog-to-digital converter are disposed on the first chip and the color interpolation circuit is disposed on the second chip.”**

221. In my opinion, *Inuiya* in combination with *Fossum* discloses or suggests these features. As I discussed above in Section IX.C.3, a person of ordinary skill in the art would have understood that implementing the components of an imaging device on two chips would have been an apparent combination and/or design choice. (See my discussion above in Section IX.C.3.) *Inuiya*, like *Isogai* and *Fossum*, discloses an imaging device with a pixel array, analog-to-digital converters, and color processing circuitry. Therefore, for the same reasons discussed above with

respect to *Isogai* in combination with *Fossum* in Section IX.C.3, a person of ordinary skill in the art would have been motivated to combine the teachings of *Inuiya* and *Fossum* with a reasonable expectation of success such that *Inuiya*'s analog-to-digital converters are on the same chip as the pixel array, while maintaining the color processing circuitry on a second chip.

2. Claim 5

- a) **“The solid stage imaging device of claim 1 further comprising a chip, wherein the red pixel, the blue pixel, the first green pixel, the second green pixel, the first analog-to-digital converter, the second analog-to-digital converter and the color interpolation circuit are disposed on the chip.”**

222. In my opinion, *Inuiya* in combination with *Fossum* discloses or suggests this feature. As discussed above in Section IX.C.4, a person of ordinary skill in the art would have understood that implementing the components of an imaging device on one chip would have been an apparent combination and/or design choice. (See my discussion above in Section IX.C.4.) *Inuiya*, like *Isogai* and *Fossum*, discloses an imaging device with a pixel array, analog-to-digital converters, and color processing circuitry. Therefore, for the same reasons discussed above with respect to *Isogai* in combination with *Fossum* in Section IX.C.4, a person of ordinary skill in the art would have been motivated to combine the teachings of *Inuiya* and

Fossum with a reasonable expectation of success such that *Inuiya*'s analog-to-digital converters and color processing circuitry are on the same chip as the pixel array.

3. Claims 21-22

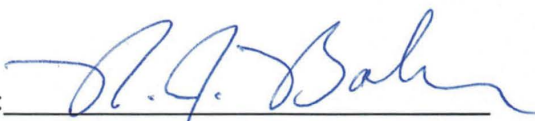
223. *Inuiya* in combination with *Fossum* discloses or suggests the features of claims 21-22 for the same reasons that I discuss above for each of claims 4-5, respectively. (See my analysis above in Sections IX.F.1-2.)

X. CONCLUSION

224. In summary, it is my opinion that all of the features recited in claims 1-5 and 18-22 of the '651 patent are disclosed or suggested by the prior art.

225. I declare that all statements made herein of my knowledge are true, and that all statements made on information and belief are believed to be true, and that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

Dated: January 15, 2021

By: 
R. Jacob Baker, Ph.D., P.E.