

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

OMNIVISION TECHNOLOGIES, INC.,
Petitioner

v.

RE SECURED NETWORKS, LLC
Patent Owner

U.S. Patent No. 6,838,651

Inter Partes Review Case No. IPR2025-01019

PATENT OWNER PRELIMINARY RESPONSE

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37 CFR § 42.104 6

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I. INTRODUCTION

Petitioner OmniVision Technologies, Inc. (“Petitioner”) has challenged the validity of U.S. Patent No. 6,838,651 (the “’651 patent”) (EX1001). Patent Owner RE Secured Networks, LLC (“Patent Owner”) opposes institution. The arguments in this Preliminary Response are merits arguments that are separate and in addition to the arguments presented in Patent Owner’s previously filed request for discretionary denial of institution. Paper 9.

As outlined in Patent Owner’s discretionary denial brief, this is a clear case in which the Director should discretionarily deny institution of review. There are strong settled expectations in a patent that issued over 20 years ago, which has been asserted in multiple proceedings in the relevant market, including against companies incorporating Petitioner’s sensors into their own products, and Petitioner became aware of the ’651 patent years ago in connection with one of those proceedings. Petitioner also waited until the very last possible day to file the instant Petition—over a year after Petitioner filed the declaratory judgment action that initiated the parallel litigation. Further, all of the *Fintiv* factors favor discretionary denial as there is complete overlap of the parties and issues, no stay or likelihood of a stay, and the jury trial date in the parallel litigation is almost two months before a Final Written Decision would issue in this matter. Petitioner also filed and extensively relied on a declaration from another party’s expert, from a

previously filed IPR, which Petitioner's expert herein improperly adopted in whole, meaning that Patent Owner would need to depose one expert on another expert's work if review is instituted. All of these discretionary arguments are in addition to the merits arguments presented herein which, on their own, warrant denial of institution.

Independent claims 1 and 18 of the '651 patent, the sole independent claims challenged herein, are directed to an imaging device, and related imaging method, that employs one red, one blue, and two green pixels. Analog signals from the red and blue pixels are converted by a first analog-to-digital ("A/D") converter, while analog signals from the two green pixels are converted by a second A/D device. The four resultant digital signals are then combined using a color interpolation circuit.

Independent claims 1 and 18 are challenged in Ground 1 as being anticipated by Japanese Patent Application Pub. No. 2000-12819 ("Isogai") (EX1005), and in Ground 4 as being anticipated by U.S. Patent No. 5,982,984 ("Inuiya") (EX1006). As such, each of these allegedly anticipatory references must disclose, explicitly or inherently, every feature of claims 1 and 18, and the allegations of anticipation must be made, in the first instance, in the Petition. If the Petition does not show a reasonable likelihood that the Petitioner would prevail as to at least one of the claims challenged, institution should be denied.

In relying on Isogai in Ground 1, however, the Petition fails to show a reasonable likelihood of success on the merits. For the purposes of the Petition, Petitioner proposed and adopted a set of claim constructions requiring that the “color interpolation circuit” is hardware, and that “combining the first, second, third, and fourth digital signals” requires combining all four signals. However, when applying Petitioner’s self-adopted claim constructions, the Petition fails to show for claims 1 and 18 that Isogai explicitly or inherently discloses a hardware “color interpolation circuit.” Nor does the Petition explain how the alleged “color interpolation circuit” of Isogai necessarily “combin[es] [all of] the first, second, third and fourth digital signals,” as construed by Petitioner for claims 1 and 18. Ground 1 must therefore fall, and with it Grounds 2 and 3, which merely expand upon Ground 1 without remedying these fundamental issues with Ground 1.

Similarly, the Petition’s reliance on Inuiya in Ground 4 is misplaced. Beyond improperly relying upon two, distinct embodiments in Inuiya to support its allegations of anticipation, the Petition fails to explain how Inuiya discloses a hardware “color interpolation circuit,” under Petitioner’s proposed claim construction. Ground 4 as presented by Petitioner therefore also cannot provide a reasonable likelihood of success on the merits, and Grounds 5 and 6, which simply expand upon Ground 4 without remedying these fundamental issues with Ground 4, similarly fail.

For these and the other reasons set forth herein, Patent Owner respectfully submits that the Petition is inadequate to warrant institution of review.

II. TIMELINESS

Patent Owner notes that Petitioner's brief in opposition to discretionary denial (Paper 10), incorrectly argues that the notice of filing date accorded to the Petition in this matter was dated June 18, 2025, citing Paper 3. Paper 10 at 1. Patent Owner notes that Paper 3 was expunged, and, in any event, P-TACTS further shows that Paper 3 was actually filed on June 20, as shown by the below from P-TACTS.

1	Petition for Inter Partes Review of U.S. Patent No. 6,838,651	Paper	1	05/20/2025	Petitioner	Public
2	Petitioner's Power of Attorney	Paper	2	05/20/2025	Petitioner	Public
3	EXPUNGED	Paper	3	06/20/2025	Board	EXPUNGED-Public
4	EXPUNGED	Paper	4	06/20/2025	Board	EXPUNGED-Public
5	Notice: Notice filing date accorded	Paper	5	06/20/2025	Board	Public

To the extent that Petitioner maintains its untimeliness argument,¹ Patent Owner notes that Paper 5 is the notice of filing date accorded to the Petition in this matter and is dated June 20, 2025, as shown in the above from P-TACTS and in the below snippet from page 1 of Paper 5²:

¹ Petitioner has indicated that it will file a replacement discretionary denial brief that removes the untimeliness argument, but Petitioner has not yet done so.

² Patent Owner notes that the header of Paper 5 includes a notation that it is "Paper 3."

IPR2025-01019
Patent 6,838,651

Mailed: June 20, 2025

Before Andrew Kellogg, *Deputy Chief Clerk, Trials*

NOTICE OF FILING DATE ACCORDED TO PETITION
AND
TIME FOR FILING PATENT OWNER PRELIMINARY RESPONSE

Therefore, the Preliminary Response in this matter is due “no later than three months from the date of” Paper 5, *i.e.*, September 20, 2025, a Saturday, which makes the instant filing on Monday, September 22, 2025, timely per 35 U.S.C. § 21(b). *See also Samsung Elecs. Co. v. Immersion Corp.*, IPR2018-01468, Paper 10 at 14-19 (P.T.A.B. Feb. 20, 2019) (applying Section 21(b)’s “statutory grace period that applies to ‘any action’ in the PTO to a Petition for IPR”).

Further, Patent Owner’s brief on discretionary denial, pursuant to the Director’s March 26, 2025, Memorandum Regarding Interim Processes for PTAB Workload Management, was due two months from the date of Paper 5, *i.e.*, August 20, 2025, the date that Paper 9 was timely filed.

III. LEGAL STANDARDS FOR INSTITUTION

Institution requires “a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition.” 35 U.S.C.

§ 314(a). In the first instance, this showing must be made *in the Petition*. See 35 U.S.C. § 312(a) (“A petition filed under section 311 may be considered only if . . . (3) *the petition* identifies, in writing and with particularity . . . the grounds on which the challenge to each claim is based, and the evidence that supports the grounds for the challenge to each claim” (emphasis added)).

It is Petitioner who must specify “[h]ow the challenged claim is to be construed” and “[h]ow the construed claim is unpatentable,” including “specify[ing] where each element of the claim is found in the prior art patents or printed publications relied upon.” 37 CFR § 42.104(b)(3)-(4). “[I]t is Petitioner’s burden to establish, in the Petition, a reasonable likelihood of success, which includes, inter alia, explaining how a challenged claim is construed and how the prior art teaches that claim.” *World Bottling Cap, LLC v. Crown Packaging Tech., Inc.*, Case IPR2015-00296, slip op. at 5 (P.T.A.B. May 27, 2015) (Paper 8).

Key requirements and burdens applicable to the Board’s institution decision in an IPR were summarized by the Federal Circuit in *Harmonic Inc. v. Avid Tech., Inc.*, 815 F.3d 1356 (Fed. Cir. 2016):

In an IPR, the petitioner has the burden *from the onset* to show with particularity why the patent it challenges is unpatentable. See 35 U.S.C. § 312(a)(3) (requiring IPR *petitions* to identify ‘with particularity . . . the evidence that supports the grounds for the challenge to each claim.’).

Id. at 1363 (emphasis added).

This submission addresses only the issue of institution of trial. Should a trial be instituted, Patent Owner reserves any and all arguments not expressly addressed herein.

IV. BACKGROUND OF THE '651 PATENT

A. Overview of the disclosure

The '651 patent generally concerns solid-state imaging devices, such as Complementary Metal Oxide Semiconductor ("CMOS") solid-state imagers (*see* EX1001, 1:8-9), and seeks to address, *inter alia*, the problem of how to provide a high performance solid-state image sensor with very high frame rates (and excellent noise reduction). *Id.*, 2:66-3:13.

Fig. 1, reproduced below, illustrates an embodiment relevant to claims 1 and 18:

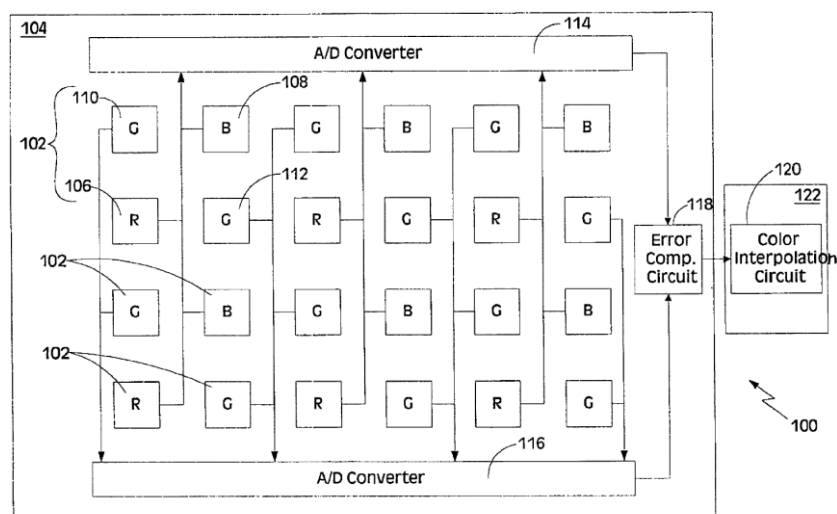


FIG. 1

EX1001, Fig. 1.

An imaging device 100 includes a two-dimensional array of image pixels 102 disposed on a chip 104 having four color channels (one red, one blue and two greens). *Id.*, 4:30-34. Each pixel 102 is either a red pixel 106, a blue pixel 108, or a green pixel 110, 112, in which green pixels 110, 112 are disposed in a checkerboard pattern. *Id.*, 4:34-37, 4:51-54. The output of each pixel 102 is a signal proportional to the amount of light incident on pixel 102. *Id.*, 4:43-44.

Green pixels 110, 112 exist in both odd rows and even rows. *Id.*, 4:51-56. Blue pixels 108 alternate with green pixels 110 in odd rows, and red pixels 106 alternate with green pixels 110 in even rows. *Id.*, 4:56-59. A first analog-to-digital (“A/D”) converter 114 is disposed on chip 104 and converts the outputs of red pixels 106 and blue pixels 108 into digital signals. *Id.*, 4:65-67. A second analog-to-digital converter 116 disposed on the chip 104 converts the outputs of green pixels 110, 112 into digital signals. *Id.*, 5:1-3.

In Figure 1, an error compensation circuit 118 provides independent gain correction for each color channel and also provides independent offsets to correct fixed pattern noise offsets for each color channel. *Id.*, 5:3-7. Color interpolation for each pixel 102 is performed by a color interpolation circuit 120. *Id.*, 5:23-25. Color interpolation circuit 120 may be located on a second chip 122, as shown in FIG. 1, or may be located on chip 104. *Id.*, 5:25-27.

B. Level of ordinary skill in the art

Petitioner alleges that a person having ordinary skill in the art (“POSITA”) would be a person with at least a bachelor’s degree in electrical engineering, physics, or materials science, and would have had at least four years of industrial or research experience in CMOS image sensor design or fabrication. Petitioner further asserts that a POSITA could alternatively have a master’s degree in electrical engineering, physics, or materials science, and at least two years of industrial or research experience in image sensor design or fabrication. Petition at 5.

For purposes of this Preliminary Response only, Patent Owner does not dispute this characterization of a POSITA. Patent Owner, however, reserves the right to more clearly characterize a POSITA should the Board decide to institute review.

V. CLAIM CONSTRUCTION

“In an *inter partes* review proceeding, a claim of a patent, or a claim proposed in a motion to amend under § 42.121, shall be construed using the same claim construction standard that would be used to construe the claim in a civil action under 35 U.S.C. 282(b), including construing the claim in accordance with the ordinary and customary meaning of such claim as understood by one of

ordinary skill in the art and the prosecution history pertaining to the patent.” 37

C.F.R. § 42.100.

For purposes of this Preliminary Response and addressing the sufficiency of the arguments presented by the Petition only, Patent Owner relies upon the claim construction positions advanced by Petitioner, and purportedly adopted by Petitioner for purposes of the Petition. Namely, Petitioner has applied constructions in which the term “circuit” connotes that the “color interpolation circuit” is hardware, and the act of “combining the first, second, third and fourth digital signals” requires combining all four digital signals. *See* Petition at 8. Notably, Petitioner has offered no theories or arguments applying the claim constructions advocated by Patent Owner in related proceedings, and therefore this response does not address Petitioner’s art under those proposals or any other constructions. Patent Owner otherwise adopts the ordinary and customary meanings for the other claim terms in this proceeding. *See Phillips v. AWH Corp.*, 415 F.3d 1303, 1313-14 (Fed. Cir. 2005).

VI. EACH ALLEGED GROUND OF UNPATENTABILITY FAILS THE “REASONABLE LIKELIHOOD” TEST

Patent Owner addresses below specific shortcomings in the Petition’s Grounds. For convenience, Patent Owner adopts the same claim element numbering scheme as used in the Petition.

A. Ground 1 – Alleged anticipation by Isogai (EX1005)

1. 1[g]: “a *color interpolation circuit* for combining the first, second, third and fourth digital signals”;

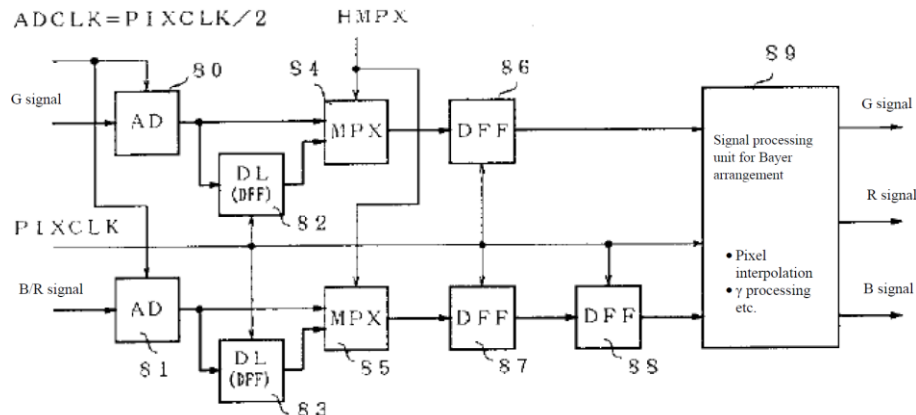
18[e]: “combining the first, second, third and fourth digital signals using a *color interpolation circuit*”

As construed by Petitioner (which construction is adopted solely for purposes herein by Patent Owner), the term “color interpolation circuit” refers to hardware. Petition at 8. According to the Petition, “*Isogai* discloses a signal processing unit 89 that combines the first, second, third, and fourth digital signals.” Petition at 21 (emphasis in original). The Petition alleges, in conclusory fashion, that:

The “signal processing unit for Bayer arrangement” shown in Figure 22 is ***a dedicated hardware component*** with inputs corresponding to the four digital signals in the Bayer filter arrangement and outputs for each of the red, green, and blue colors for each pixel that combines the four signals.

Petition at 23 (citing EX1002 ¶ 41) (emphasis added). Figure 22 from Isogai is reproduced below for reference:

FIG. 22



EX1005, Fig. 22.

According to Isogai, “FIG. 22 is a configuration diagram showing an example of a signal processing device that processes a signal output from the solid-state image sensing element according to the present invention.” EX1005 ¶ 0077.

Regarding element 89 in Figure 22 (upon which Petitioner relies), and what type of component it actually is, all Isogai has to say is that:

signal processing unit 89 is a signal processing unit for Bayer arrangement, and performs signal processing such as R / B color separation, pixel interpolation of empty grid points of each RGB color and γ processing to output RGB color signals with all pixels having RGB color signal.

Id. ¶ 0080. That is, Isogai discusses signal processing unit 89 in purely *functional* terms but does not disclose if this functionality is obtained via software or hardware, a combination of the two, or other some other means.

The Petition’s assertion that signal processing unit 89 of Isogai “is a dedicated hardware component” is thus unsupported by Isogai’s disclosure, and based upon no more than paragraph 41 of the Theuwissen declaration, EX1002. But this paragraph of the Theuwissen declaration simply repeats the allegation that “that signal processing unit for Bayer arrangement 89 shown in Figure 22 of Japanese Patent Publication 2000-12819 (‘Isogai’) is a dedicated hardware circuit,” without offering any further substantive arguments in support thereof, other than describing and reproducing Isogai’s Figure 22. *See* EX1002 ¶ 41. Expert opinions

that simply restate a petition's unsupported and conclusory assertions (such as Dr. Theuwissen's opinion in paragraph 41) are entitled to little weight. *See Xerox Corp. v. Bytemark, Inc.*, IPR2022-00624, Paper 9, at 15 (P.T.A.B. Aug. 24, 2022); *TikTok Inc. v. NTech Properties, Inc.*, IPR2024-01339, Paper 9, at 16 (P.T.A.B. Feb. 25, 2025); *see also* Patent Trial and Appeal Board Consolidated Trial Practice Guide at 36 (November 2019) ("a petitioner asserting anticipation cannot rely on its expert to supply disclosure of a claim element that is not expressly or inherently present in the reference.").

"In order to anticipate the claimed invention, a prior art reference must disclose all elements of the claim within the four corners of the document, and it must disclose those elements arranged as in the claim." *Microsoft Corp. v. Biscotti, Inc.*, 878 F.3d 1052, 1068 (Fed. Cir. 2017) (internal quotations omitted). As to inherent disclosure, which Petitioner appears to be relying upon, "[i]nherency can be established when prior art necessarily functions in accordance with, or includes, the claimed limitations, but may not be established by probabilities or possibilities." *Amgen Inc. v. Sandoz, Inc.*, 66 F.4th 952, 966 (Fed. Cir. 2023) (internal quotations and citations omitted). However, as explained further below, any reliance on inherency must also fail.

The Petition broadly alleges that a "POSA also would understand that Isogai discloses a circuit." Petition at 23 (citing EX1002 ¶¶ 41, 43-47). But regardless of

whether or not a POSITA would understand Isogai as disclosing a circuit, it does not necessarily follow from this that Isogai's signal processing unit 89 is also "a dedicated hardware circuit," as the Petition alleges.

The Petition improperly incorporates by reference paragraphs 43-47 of EX1002 (the Theuwissen declaration), insofar as it cites to these paragraphs but does not provide the underlying arguments or subject matter. *See Cisco Sys., Inc. v. C-Cation Techs., LLC*, IPR2014-00454, Paper 12, at 10 (P.T.A.B. Aug. 29, 2014) ("Accordingly, we will not consider arguments that are not made in the Petition, but are instead incorporated by reference to the cited paragraphs and claims charts of [the expert's] [d]eclaration."). But even if the Board were to entertain the arguments in these paragraphs (which it should not), they still cannot carry the day in concluding that Isogai's signal processing unit 89 is inherently hardware as Petitioner has alleged.

Paragraph 43 of EX1002 begins by noting that "as of at least 1998 that color interpolation operations *could be* performed on dedicated hardware circuitry." EX1002 ¶ 43 (emphasis added). The natural implication of this is that color interpolation *could also not* be performed on "dedicated hardware circuitry." Regardless, the Theuwissen declaration then turns *to another reference* (EX1010, Loinaz) to support the proposition that "color interpolation operations could be performed on dedicated hardware circuitry." *See id.* The Theuwissen declaration

(and the Petition’s reliance thereon) is thus, at most, relying upon an **obviousness** argument, not inherency, and is therefore inapposite to the issue of anticipation.³ See *Studiengesellschaft Kohle, m.b.H. v. Dart Indus., Inc.*, 726 F.2d 724, 726–27 (Fed. Cir. 1984) (“It is hornbook law that anticipation must be found in a single reference, device, or process.... [R]eliance on the caveat to that rule permitting the use of additional references to interpret the allegedly anticipating reference is misplaced.... [C]ombin[ing] the teachings of [other] references to build an anticipation [argument] [is] contrary to settled law....”).

Paragraphs 44-46 of EX1002 concern claim construction arguments, not Isogai, while paragraph 47 simply reiterates the conclusion that Isogai “discloses dedicated hardware that performs color interpolation,” without offering any further substantive analysis for this conclusion other than noting the presence of interconnection lines in the figures that purportedly illustrate “specific input lines for receiving the digital [sic] signals and specific output lines for outputting RGB values....” EX1002 ¶ 47. The Petition does not explain, however, why the presence of such lines in Isogai’s drawings means that the underlying functionality of signal

³ The Petition’s reliance on Loinaz (*e.g.*, Petition at 23) is similarly an improper obviousness argument that cannot support the Petition’s anticipation grounds.

processing unit 89 necessarily arises from “a dedicated hardware circuit,” as the Petition alleges.

Hence, as Isogai does not explicitly or inherently disclose a “color interpolation circuit” under Petitioner’s theory as presented, the Petition has not shown that Isogai anticipates either of claims 1 or 18, and Ground 1 should therefore be rejected.

2. 1[g]: “a color interpolation circuit for *combining the first, second, third and fourth digital signals*”;
- 18[e]: “*combining the first, second, third and fourth digital signals* using a color interpolation circuit”

As construed by Petitioner (which construction is adopted solely for purposes herein by Patent Owner, as Petitioner has offered no theory or analysis under any other construction), the term “combining the first, second, third and fourth digital signals” requires combining all four digital signals. As with the “color interpolation circuit” limitation discussed above, the Petition, at most, relies upon inherency to allege that Isogai discloses combining the first, second, third and fourth signals—stating, in conclusory fashion, that a “POSA would have understood that Isogai’s disclosure of ‘pixel interpolation’ would necessarily include combining color data corresponding to neighboring pixels in order to determine the pixel color data for the empty grid points as described by the ’651 patent.” Petition at 23. But this conclusory argument from the Petition includes no discussion, explanation, or evidence as to why “pixel interpolation” necessarily

requires combining all four digital signals (as Petitioner's adopted construction requires). This argument also fails because it seeks to inject the disclosure of the '651 patent into a discussion of what Isogai allegedly discloses. *In re Sponnoble*, 405 F.2d 578, 585 (C.C.P.A. 1969) ("we must view the prior art without reading into that art [Patent Owner's] teachings."). The Petition's reliance on paragraph 73 of EX1015 (Baker declaration from IPR2021-00437) is similarly unavailing as it, too, relies upon the disclosure of the '651 patent to interpret Isogai.

Since the Petition does not explain how or why Isogai explicitly or inherently discloses combining all four digital signals, as Petitioner has argued, the Petition has failed to show that Isogai anticipates either of claims 1 or 18, providing yet another basis for rejecting Ground 1.

B. Grounds 2 and 3 – Alleged obviousness of claims 2-5 and 19-22

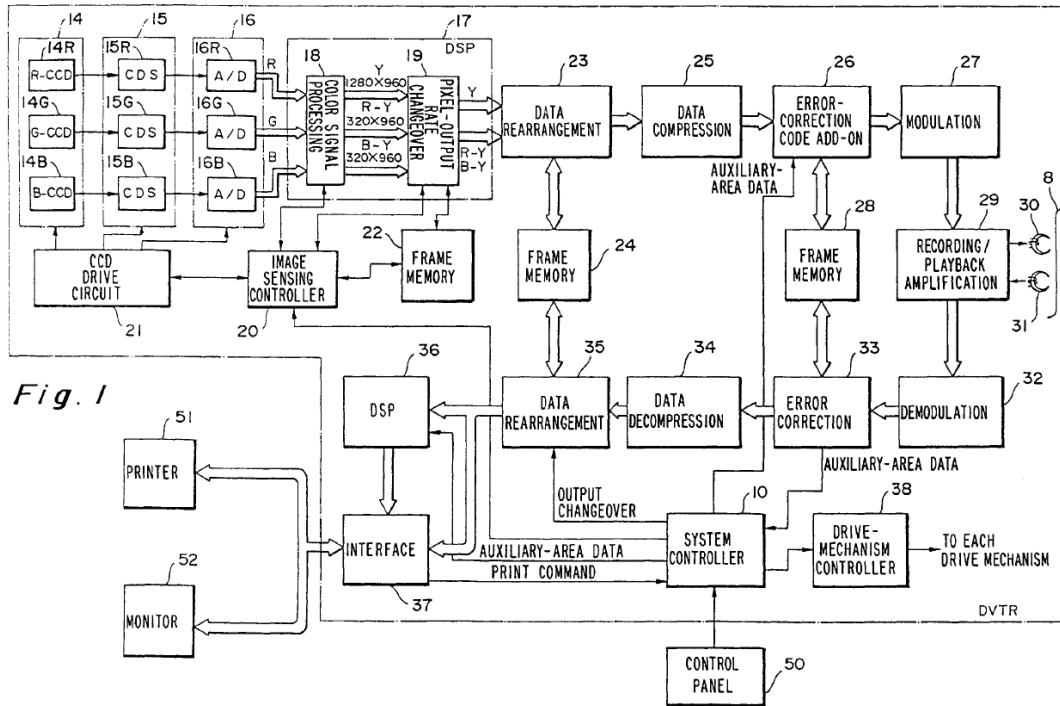
Grounds 2 and 3 do not allege obviousness of either of claims 1 or 18, but instead advance arguments that build upon Ground 1 to allege invalidity of dependent claims 2-5 and 19-22. Hence, Grounds 2 and 3 do nothing to cure the infirmities of Ground 1 and should thus be rejected for at least the reasons set forth above in connection with Ground 1.

C. Ground 4 – Alleged anticipation of claims 1-3 and 18-20 by Inuiya (EX1006)

1. 1[g]: “a color interpolation circuit for *combining the first, second, third and fourth digital signals*”;
- 18[e]: “*combining the first, second, third and fourth digital signals* using a color interpolation circuit”

As with Isogai above, the Petition fails to show a color interpolation circuit within Inuiya that combines all four digital signals (as Petitioner has argued), and thus fails to show anticipation of claims 1 and 18 by Inuiya, and by extension fails to show anticipation of claims 2 and 3 that depend from claim 1, and anticipation of claims 19 and 20 that depend from claim 18.

With respect to limitation 1[g] (the arguments for which the Petition also relies upon for limitation 18[e] (*see* Petition at 85)), the Petition begins by referring to Inuiya’s digital signal processor (“DSP”) 17 (and related color signal processing circuit 18). Petition at 75-76. Citing to Inuiya at 11:6-15, the Petition discusses those components generating luminance data from “the entered digital image data of the colors red, green and blue . . . ” EX1006, 11:8-9; *see* Petition at 75-76. A significant flaw in this argument, however, is that it draws from Figure 1 of Inuiya, which is an embodiment of a digital video tape recorder (“DVTR”) that has *only three color channels*. For reference, Figure 1 of Inuiya is repeated below:



EX1006, Fig. 1. Discussing the above Figure 1, Inuiya states:

in FIG. 1, the image sensing section of the digital video tape recorder is controlled by an image sensing controller 20, which controls a CCD drive circuit 21. An image sensing circuit 14 which includes the CCDs 14R, 14G and 14B is controlled by the CCD drive circuit 21, whereby the storage of signal charge in the CCDs 14R, 14G and 14B and the sweep-out of this signal charge is controlled.

EX1006, 10:53-59. Hence, DSP 17 and related “color signal processing” 18 of Inuiya’s Figure 1 embodiment cannot disclose “a color interpolation circuit for combining the first, second, third **and fourth** digital signals,” in the manner argued by Petitioner.

The Petition then jumps from Figure 1 of Inuiya to Figure 18, and states that “digital pixel data stored in the memories 111-113 is then processed by the color

processing block ('color interpolation circuit'), which combines the first, second, third, and fourth digital signals to produce luminance data and color difference data." Petition at 77 (citing EX1006, 26:5-19, 27:10-18). Figure 18 of Inuiya is reproduced below:

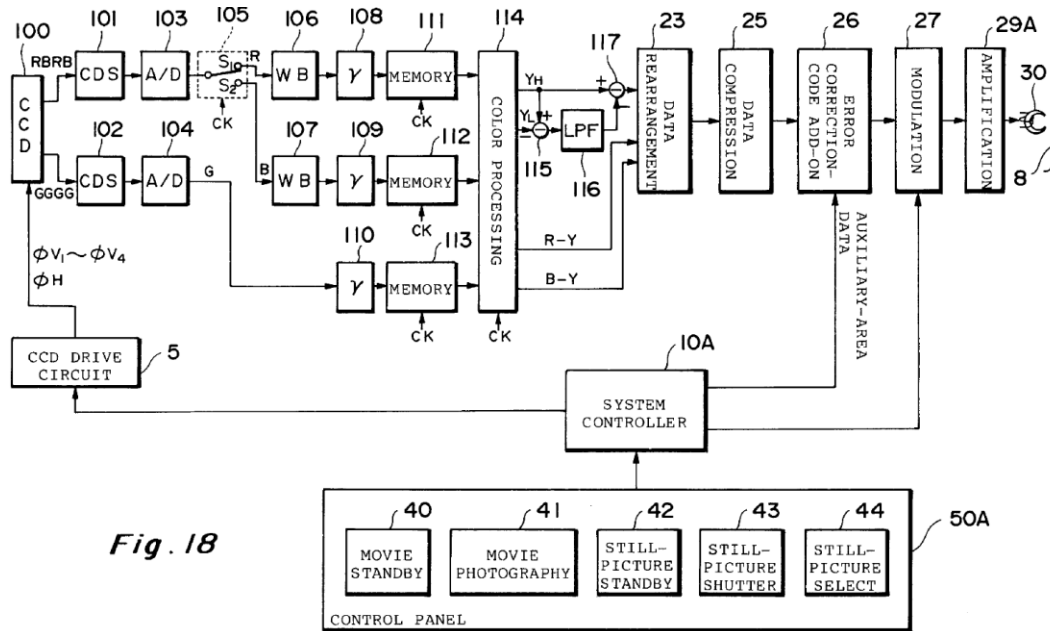


Fig. 18

EX1006, Fig. 18.

However, Inuiya states that Figure 18 is: "a block diagram illustrating the electrical configuration of a digital video tape recorder *according to another embodiment of the present invention*. Components in FIG. 18 identical with those shown in FIG. 1 are designated by like reference characters and need not be described again." EX1006, 20:12-16 (emphasis added). Inuiya then discusses at length Figure 18's CCD 100, which differs from the CCD of Inuiya's Figure 1 by employing a different color channel arrangement. *See generally* EX1006, 20:18-

24:57. Thus, Figures 1 and 18 are two different embodiments, and CCD 100 is a different component with a different arrangement than the CCD of Figure 1. As such, the Petition improperly mixes two distinct embodiments of Inuiya to allege anticipation. *See Biscotti*, 878 F.3d at 1069 (“anticipation is not proven by multiple, distinct teachings that the artisan might somehow combine to achieve the claimed invention.”) (internal quotations omitted). The Petition thus does not show anticipation of claims 1 and 18 by Inuiya, and, by extension, also fails to show anticipation by Inuiya of claims 2, 3, 19, and 20. Ground 4 should thus be rejected.

2. 1[g]: “a *color interpolation circuit* for combining the first, second, third and fourth digital signals”;
- 18[e]: “combining the first, second, third and fourth digital signals using a *color interpolation circuit*”

The Petition also fails to show a hardware color interpolation circuit within Inuiya as argued by Petitioner and thus fails to show anticipation of claims 1 and 18, and by extension, claims 2 and 3 that depend from claim 1, and claims 19 and 20 that depend from claim 18.

In support of its position that Inuiya’s color processing circuit 114 is hardware, the Petition states only that a:

POSA would understand color processing block 114 to disclose a circuit. (Ex. 1002, ¶¶42-47.) This is confirmed by its connection to the other components and specific inputs for the digital signals and RGB outputs. (*Id.*) Loinaz confirms that a POSA would know how to build such a hardware circuit. (*Id.*, ¶42; Ex. 1010, Fig. 10.)

Petition at 81. The only support for this conclusion is citation to paragraphs 42-47 of the Theuwissen declaration, EX1002, but these paragraphs (besides being improperly incorporated by reference as discussed above in Ground 1) simply repeat the same conclusion without any substantive arguments.

For example, paragraph 42 states that “in the context of entire Figure 18, the dedicated input and output lines corresponding to the color processing circuit 114 indicate that the color processing circuit 114 is also a dedicated hardware circuit for performing color interpolation of the digital signals for the red, blue, and green pixels” (EX1002 ¶ 42), but this does not explain why these inputs and outputs necessarily require a *hardware* color interpolation circuit as advanced by Petitioner.

As previously noted, paragraph 43 of EX1002 states that “as of at least 1998 that color interpolation operations could be performed on dedicated hardware circuitry” (EX1002 ¶ 43), indicating that color interpolation could also be performed *other than on* “dedicated hardware circuitry”—rendering inherency inapplicable. Moreover, the Petition (at 81) and Dr. Theuwissen’s (at paragraph 43) improper reliance upon EX1010 (Loinaz) attempts to prove anticipation through use of an unasserted obviousness argument. *Dart Indus.*, 726 F.2d at 726–27. As also previously noted, paragraphs 44-47 add nothing more to the argument,

and hence the expert's allegations are wholly conclusory and deserving of little or no weight. *Bytemark*, IPR2022-00624, Paper 9, at 15.

As Inuiya does not explicitly or inherently disclose a “color interpolation circuit” as Petitioner has argued, the Petition has failed to show that Inuiya anticipates either of claims 1 or 18, and by extension claims 2, 3, 19, and 20, and Ground 4 should thus be rejected.

D. Grounds 5 and 6 – Alleged obviousness of claims 4-5 and 21-22

Grounds 5 and 6 do not allege obviousness of either of claims 1 or 18, but instead advance arguments that build upon Ground 4 to allege invalidity of dependent claims 4, 5, 21, and 22. Hence, Grounds 5 and 6 do nothing to cure the infirmities of Ground 4 and should thus be rejected for at least the reasons set forth above in connection with Ground 4.

VII. CONCLUSION

Because Petitioner has failed to show that it is reasonably likely to invalidate at least one claim in the '651 patent, the Board should deny the Petition and decline to institute *inter partes* review of the '651 patent.

Dated: September 22, 2025

Respectfully submitted,

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CERTIFICATION UNDER 37 CFR § 42.24(d)

Pursuant to 37 CFR §42.24(d), the undersigned hereby certifies that the word count for the foregoing Patent Owner Preliminary Response totals 4,802 words, which is less than the 14,000 allowed under 37 CFR §§ 42.24(b)(1), 42.24(a)(1)(i).

Dated: September 22, 2025

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CERTIFICATE OF SERVICE

Pursuant to 37 CFR § 42.205(b), the undersigned certifies that on September 22, 2025, a complete and entire copy of this Patent Owner Preliminary Response was provided to the Petitioner by filing through the Patent Trial and Appeal Case Tracking System (P-TACTS) and via email to the below email addresses, as authorized in Petitioner's mandatory notices.

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