AO 120 (Rev. 08/10)

TO:	REPORT ON THE FILING OR DETERMINATION OF AN ACTION REGARDING A PATENT OR TRADEMARK
Mail Stop 8 Director of the U.S. Patent and Trademark Office P.O. Box 1450 Alexandria, VA 22313-1450	

In Compliance with 35 U.S.C. § 290 and/or 15 U.S.C. § 1116 you are hereby advised that a court action has been filed in the U.S. District Court Eastern District of Texas on the following

☐ Trademarks or ☑ Patents. (☐ the patent action involves 35 U.S.C. § 292.):

DOCKET NO.	DATE FILED	U.S. DISTRICT COURT
5:24-CV-00122	8/30/2024	Eastern District of Texas

PLAINTIFF	DEFENDANT
GENERAL VIDEO, LLC	LENOVO GROUP LIMITED

	PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1	6,584,443	6/24/2023	General Video, LLC.
2	7,069,224	6/27/2006	General Video, LLC.
3	7,225,282	5/29/2007	General Video, LLC.
4	7,359,437	4/15/2008	General Video, LLC.
5	9,036,010	5/19/2015	General Video, LLC.

In the above—entitled case, the following patent(s)/ trademark(s) have been included:

DATE INCLUDED	INCLUDED BY ☐ Amendment ☐ Answer ☐ Cross Bill ☐ Other Pleading	
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
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In the above—entitled case, the following decision has been rendered or judgement issued:

DECISION/JUDGEMENT

CLERK	(BY) DEPUTY CLERK	DATE

Copy 1—Upon initiation of action, mail this copy to Director Copy 3—Upon termination of action, mail this copy to Director
Copy 2—Upon filing document adding patent(s), mail this copy to Director Copy 4—Case file copy

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GENERAL VIDEO, LLC	LENOVO GROUP LIMITED

	PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1	9,843,786	12/12/2017	General Video, LLC.
2			
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In the above—entitled case, the following patent(s)/ trademark(s) have been included:

DATE INCLUDED	INCLUDED BY ☐ Amendment ☐ Answer ☐ Cross Bill ☐ Other Pleading	
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☐ Trademarks or ☑ Patents. (☐ the patent action involves 35 U.S.C. § 292.):

DOCKET NO.	DATE FILED	U.S. DISTRICT COURT
5:24-cv-00124	8/30/2024	Eastern District of Texas

PLAINTIFF	DEFENDANT
GENERAL VIDEO, LLC	DELL INC. and DELL TECHNOLOGIES INC.

	PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1	6,584,443	6/24/2023	General Video, LLC.
2	7,069,224	6/27/2006	General Video, LLC.
3	7,225,282	5/29/2007	General Video, LLC.
4	7,359,437	4/15/2008	General Video, LLC.
5	9,036,010	5/19/2015	General Video, LLC.

In the above—entitled case, the following patent(s)/ trademark(s) have been included:

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GENERAL VIDEO, LLC	LENOVO GROUP LIMITED

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PATENT ASSIGNMENT COVER SHEET

Electronic Version v1.1
Stylesheet Version v1.2

Assignment ID: PATI342200

SUBMISSION TYPE:	NEW ASSIGNMENT
NATURE OF CONVEYANCE:	ASSIGNMENT

CONVEYING PARTY DATA

Name	Execution Date
KONINKLIJKE PHILIPS N.V.	04/01/2024

RECEIVING PARTY DATA

Company Name:	GENERAL VIDEO, LLC
Street Address:	7209 LANCASTER PIKE
Internal Address:	SUITE 4
City:	HOCKESSIN
State/Country:	DELAWARE
Postal Code:	19707

PROPERTY NUMBERS Total: 8

Property Type	Number
Patent Number:	7088398
Patent Number:	6914637
Patent Number:	7257163
Patent Number:	7359437
Patent Number:	7225282
Patent Number:	9036010
Patent Number:	9462258
Patent Number:	9843786

CORRESPONDENCE DATA

Fax Number:

Correspondence will be sent to the e-mail address first; if that is unsuccessful, it will be sent using a fax number, if provided; if that is unsuccessful, it will be sent via US Mail.

Phone: +82(109)2809544
Email: dylan@generalvideo.com
Correspondent Name: MINSANG CHO
Address Line 1: 333, Godeok-ro, Gangdong-gu
Address Line 2: 115-604
Address Line 4: Seoul, KOREA, REPUBLIC OF 05224

NAME OF SUBMITTER:	Minsang Cho
SIGNATURE:	Minsang Cho

DATE SIGNED:	07/04/2024
	This document serves as an Oath/Declaration (37 CFR 1.63).
Total Attachments: 2 source=US DoA#page1.tiff source=US DoA#page2.tiff	

US

UNITED STATES OF AMERICA

ASSIGNMENT

WHEREAS, **KONINKLIJKE PHILIPS N.V.** ("ASSIGNOR"), a corporation organized under the laws of **The Netherlands** , with a place of business at **HIGH TECH CAMPUS 5 EINDHOVEN 5656 AE NETHERLANDS**, owns the United States Patent(s) (the "Patent(s)") listed on the attached Schedule A; and

WHEREAS, **General Video, LLC** ("ASSIGNEE") , a corporation organized under the laws of **U.S.A.**, with a place of business at **7209 Lancaster Pike, Suite, Hockessin, DE, 19707, U.S.A.**, desires to acquire all rights to the Patent(s);

NOW, THEREFORE, in consideration of One Dollar ($1.00) and other valuable consideration, the receipt of which ASSIGNOR acknowledges, ASSIGNOR has sold, assigned, transferred, and set over, and does, by this Assignment, sell, assign, transfer, and set over unto ASSIGNEE, all rights to the Patent(s), including reissues and extensions, to be held and enjoyed by ASSIGNEE, its successors, assigns, and legal representatives, for ASSIGNEE's own use and benefit and for the use and benefit of its successors, assigns, and legal representatives, to the end of the term(s) for which the Patent(s) has/have been granted or may be reissued or extended, as fully and entirely as the Patent(s) would have been held and enjoyed by ASSIGNOR had this assignment and sale not been made; together with all claims for profits and damages by reason of past infringement, with the right to sue for and collect the same for the use and benefit of ASSIGNEE, its successors, assigns, and legal representatives.

This Assignment is deemed to have become effective as from: April 01, 2024

IN WITNESS WHEREOF, ASSIGNOR and ASSIGNEE have caused this Assignment to be executed by its duly authorized officer or representative on the date(s) indicated below.

KONINKLIJKE PHILIPS N.V.

By: _____

Name: Paul Erik de Haan
Title: Head of IP Support
Date: June 26, 2024

General Video, LLC

By: _____

Name: ROBERT COLAO
Title: PRESIDENT
Date: JUNE 18, 2024

Schedule

Country	Application Number	IP Grant Number
U.S.A.	10171860	7088398
U.S.A.	10192296	6914637
U.S.A.	10095422	7257163
U.S.A.	10036234	7359437
U.S.A.	10171820	7225282
U.S.A.	12808685	9036010
U.S.A.	14629642	9462258
U.S.A.	15256839	9843786

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
10/036,234	12/24/2001	Seung Ho Hwang	

CONFIRMATION NO. 6063

29416
LATTICE SEMICONDUCTOR CORPORATION
111 SW 5th Avenue
Suite 700
Portland, OR 97204

POWER OF ATTORNEY NOTICE

OC000000111484398

Date Mailed: 09/27/2019

NOTICE REGARDING CHANGE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 09/12/2019.

- The Power of Attorney to you in this application has been revoked by the assignee who has intervened as provided by 37 CFR 3.71. Future correspondence will be mailed to the new address of record(37 CFR 1.33).

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at **(571) 272-4000** or **(571) 272-4200** or **1-888-786-0101**.

/trwoodson/

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
10/036,234	12/24/2001	Seung Ho Hwang	

CONFIRMATION NO. 6063

24737
PHILIPS INTELLECTUAL PROPERTY & STANDARDS
465 Columbus Avenue
Suite 340
Valhalla, NY 10595

POA ACCEPTANCE LETTER

OC000000111484428

Date Mailed: 09/27/2019

NOTICE OF ACCEPTANCE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 09/12/2019.

The Power of Attorney in this application is accepted. Correspondence in this application will be mailed to the above address as provided by 37 CFR 1.33.

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at **(571) 272-4000** or **(571) 272-4200** or **1-888-786-0101**.

/trwoodson/

PTO/AIA/80 (07-12)
Approved for use through 11/30/2014. OMB 0651-0035
U.S. Patent and Trademark Office; U.S DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

POWER OF ATTORNEY TO PROSECUTE APPLICATIONS BEFORE THE USPTO

I hereby revoke all previous powers of attorney given in the application identified in the attached statement under 37 CFR 3.73(c).

I hereby appoint:

■ Practitioners associated with Customer Number: 24737

OR

☐ Practitioner(s) named below (if more than ten patent practitioners are to be named, then a customer number must be used):

Name	Registration Number	Name	Registration Number

As attorney(s) or agent(s) to represent the undersigned before the United States Patent and Trademark Office (USPTO) in connection with any and all patent applications assigned only to the undersigned according to the USPTO assignment records or assignments documents attached to this form in accordance with 37 CFR 3.73(c).

Please change the correspondence address for the application identified in the attached statement under 37 CFR 3.73(c) to:

■ The address associated with Customer Number: 24737

OR

☐

Firm or Individual Name			
Address			
City		State	Zip
Country			
Telephone		Email	

Assignee Name and Address: Koninklijke Philips N.V.
High Tech Campus 5
Eindhoven, NL 5656 AE

A copy of this form, together with a statement under 37 CFR 3.73(c) (Form PTO/AIA/96 or equivalent) is required to be Filed in each application in which this form is used. The statement under 37 CFR 3.73(c) may be completed by one of The practitioners appointed in this form, and must identify the application in which this Power of Attorney is to be filed.

SIGNATURE of Assignee of Record

The individual whose signature and title is supplied below is authorized to act on behalf of the assignee

Signature	/David Lawrence Schreiber/	Date	September 12, 2019
Name	David Lawrence Schreiber	Telephone	914-495-9516
Title	Authorized Signatory		

This collection of information is required by 37 CFR 1.31, 1.32 and 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

PTO/AIA/96 (08-12)
Approved for use through 01/31/2013. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

STATEMENT UNDER 37 CFR 3.73(c)

Applicant/Patent Owner: KONINKLIJKE PHILIPS N.V.

Application No./Patent No.: 10/036,234 / 7,359,437 Filed/Issue Date: December 24, 2001/ April 15, 2008

Titled: ENCODING METHOD AND SYSTEM FOR REDUCING INTER-SYMBOL INTERFERENCE EFFECTS IN TRANSMISSION OVER A SERIAL LINK

KONINKLIJKE PHILIPS N.V., a Corporation

(Name of Assignee) (Type of Assignee, e.g., corporation, partnership, university, government agency, etc.)

states that, for the patent application/patent identified above, it is (choose **one** of options 1, 2, 3 or 4 below):

1. ☑ The assignee of the entire right, title, and interest.

2. ☐ An assignee of less than the entire right, title, and interest (check applicable box):

   ☐ The extent (by percentage) of its ownership interest is _____%. Additional Statement(s) by the owners holding the balance of the interest must be submitted to account for 100% of the ownership interest.

   ☐ There are unspecified percentages of ownership. The other parties, including inventors, who together own the entire right, title and interest are:

   Additional Statement(s) by the owner(s) holding the balance of the interest must be submitted to account for the entire right, title, and interest.

3. ☐ The assignee of an undivided interest in the entirety (a complete assignment from one of the joint inventors was made). The other parties, including inventors, who together own the entire right, title, and interest are:

   Additional Statement(s) by the owner(s) holding the balance of the interest must be submitted to account for the entire right, title, and interest.

4. ☐ The recipient, via a court proceeding or the like (*e.g.*, bankruptcy, probate), of an undivided interest in the entirety (a complete transfer of ownership interest was made). The certified document(s) showing the transfer is attached.

The interest identified in option 1, 2 or 3 above (not option 4) is evidenced by either (choose **one** of options A or B below):

A. ☐ An assignment from the inventor(s) of the patent application/patent identified above. The assignment was recorded in the United States Patent and Trademark Office at Reel _____, Frame _____, or for which a copy thereof is attached.

B. ☑ A chain of title from the inventor(s), of the patent application/patent identified above, to the current assignee as follows:

1. From: HWANG, SEUNG HO. ET AL To: SILICON IMAGE, INC.

   The document was recorded in the United States Patent and Trademark Office at
   Reel 012730, Frame 0562, or for which a copy thereof is attached.

2. From: SILICON IMAGE, INC. To: LATTICE SEMICONDUCTOR CORPORATION

   The document was recorded in the United States Patent and Trademark Office at
   Reel 036419, Frame 0792, or for which a copy thereof is attached.

This collection of information is required by 37 CFR 3.73(b). The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

PTO/AIA/96 (08-12)
Approved for use through 01/31/2013. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

STATEMENT UNDER 37 CFR 3.73(c)

3. From: LATTICE SEMICONDUCTOR CORPORATION To: KONINKLIJKE PHILIPS N.V.

The document was recorded in the United States Patent and Trademark Office at
Reel 050314, Frame 0434, or for which a copy thereof is attached.

4. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at
Reel _____, Frame _____, or for which a copy thereof is attached.

5. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at
Reel _____, Frame _____, or for which a copy thereof is attached.

6. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at
Reel _____, Frame _____, or for which a copy thereof is attached.

☐ Additional documents in the chain of title are listed on a supplemental sheet(s).

☑ As required by 37 CFR 3.73(c)(1)(i), the documentary evidence of the chain of title from the original owner to the assignee was, or concurrently is being, submitted for recordation pursuant to 37 CFR 3.11.

[NOTE: A separate copy (i.e., a true copy of the original assignment document(s)) must be submitted to Assignment Division in accordance with 37 CFR Part 3, to record the assignment in the records of the USPTO. See MPEP 302.08]

The undersigned (whose title is supplied below) is authorized to act on behalf of the assignee.

/David Lawrence Schreiber/	September 12, 2019
Signature	Date
David Lawrence Schreiber	Authorized Signatory Koninklijke Philips N.V.
Printed or Typed Name	Title or Registration Number

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
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Electronic Acknowledgement Receipt

EFS ID:	37147848
Application Number:	10036234
International Application Number:	
Confirmation Number:	6063
Title of Invention:	ENCODING METHOD AND SYSTEM FOR REDUCING INTER-SYMBOL INTERFERENCE EFFECTS IN TRANSMISSION OVER A SERIAL LINK
First Named Inventor/Applicant Name:	Seung Ho Hwang
Customer Number:	29416
Filer:	David Lawrence Schreiber/Patti DeMichele
Filer Authorized By:	David Lawrence Schreiber
Attorney Docket Number:	
Receipt Date:	12-SEP-2019
Filing Date:	24-DEC-2001
Time Stamp:	15:15:53
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Power of Attorney	POA_KPNV_2019Sep12.pdf	50561 5fc191a53999b20ea3c59810cac8cb77c4cfc59c	no	1

Warnings:

Information:					
2	Assignee showing of ownership per 37 CFR 3.73	2001P03252US01_373Statement.pdf	123427 1c9a50e7c78d7e8d2693c14ea06ea8bf139a8106	no	3
Warnings:					
Information:					
			Total Files Size (in bytes):	173988	

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New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PATENT ASSIGNMENT COVER SHEET

Electronic Version v1.1
Stylesheet Version v1.2

EPAS ID: PAT5533419

SUBMISSION TYPE:	NEW ASSIGNMENT
NATURE OF CONVEYANCE:	RELEASE OF SECURITY INTEREST

CONVEYING PARTY DATA

Name	Execution Date
JEFFERIES FINANCE LLC	05/17/2019

RECEIVING PARTY DATA

Name:	LATTICE SEMICONDUCTOR CORPORATION
Street Address:	5555 NE MOORE CT
City:	HILLSBORO
State/Country:	OREGON
Postal Code:	97124
Name:	SILICON IMAGE, INC.
Street Address:	5555 NE MOORE CT
City:	HILLSBORO
State/Country:	OREGON
Postal Code:	97124
Name:	SIBEAM, INC.
Street Address:	5555 NE MOORE CT
City:	HILLSBORO
State/Country:	OREGON
Postal Code:	97124
Name:	DVDO, INC.
Street Address:	5555 NE MOORE CT
City:	HILLSBORO
State/Country:	OREGON
Postal Code:	97124

PROPERTY NUMBERS Total: 1143

Property Type	Number
Patent Number:	5574678
Patent Number:	5510738
Patent Number:	5493205
Patent Number:	5617064
Patent Number:	5670907

Property Type	Number
Patent Number:	5490074
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Property Type	Number
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Application Number:	14570817
Application Number:	14589889
Application Number:	14589925
Application Number:	14591845
Application Number:	14449095
Application Number:	12842190

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SIGNATURE:	/Urmila Karandikar/
DATE SIGNED:	05/21/2019
	This document serves as an Oath/Declaration (37 CFR 1.63).

Total Attachments: 97

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RELEASE OF A SECURITY INTEREST -- PATENTS

May 17, 2019

WHEREAS, pursuant to that certain (i) Grant of Security Interest in United States Patents, dated as of March 10, 2015, Reel 035222, Frame 0866, (ii) Grant of Security Interest in United States Patents, dated as of March 10, 2015, Reel 035308, Frame 0428, (iii) Grant of Security Interest in United States Patents, dated as of March 10, 2015, Reel 035223, Frame 0001, (iv) Grant of Security Interest in United States Patents, dated as of March 10, 2015, Reel 035226, Frame 0289, (v) Grant of Security Interest in United States Patents, dated as of March 10, 2015, Reel 035223, Frame 0387, (vi) Grant of Security Interest in United States Patents, dated as of March 10, 2015, Reel 035226, Frame 0147, (vii) Grant of Security Interest in United States Patents, dated as of March 10, 2015, Reel 035220, Frame 0048, (viii) Grant of Security Interest in United States Patents, dated as of March 10, 2015, Reel 035220, Frame 0226, (ix) Grant of Security Interest in United States Patents, dated as of March 10, 2015, Reel 035309, Frame 0142, (x) Grant of Security Interest in United States Patents, dated as of March 10, 2015, Reel 035308, Frame 0345, (xi) Grant of Security Interest in United States Patents, dated as of March 10, 2015, Reel 035225, Frame 0839 and (xii) Grant of Security Interest in United States Patents, dated as of March 10, 2015, Reel 035225, Frame 0352, LATTICE SEMICONDUCTOR CORPORATION, SILICON IMAGE, INC., SIBEAM, INC. and DVDO, INC., each a Delaware corporation (each, a "Releasee"), granted to JEFFERIES FINANCE LLC, as collateral agent for the ratable benefit of the Secured Creditors (the "Releasor"), a continuing security interest in all right, title and interest of the Releasees in, to and under United States Patents listed on the attached Schedule A (the "Patents"), and all Proceeds in respect thereof (with all of the Releasee's rights listed above being collectively referred to as the "Collateral") to secure the payment, performance and observance of the Obligations;

WHEREAS, the Releasees have satisfied their Obligations; and

WHEREAS, the Releasee has requested and the Releasor has agreed to provide a document suitable for recording in the United States Patent and Trademark Office evidencing and effecting the release, relinquishment and discharge of its security interest in the Collateral.

NOW, THEREFORE, in consideration of and in exchange for good and valuable consideration, the Releasor hereby agrees as follows:

1. Defined Terms. All capitalized terms used but not otherwise defined herein have the meanings given to them in the Grants of Security Interests in United States Patents.

2. Release of Security Interest. The Releasor hereby, without any representation and warranty and without any recourse to the Releasor, releases, relinquishes and discharges all of its security interest in the Collateral.

[Signature Page Follows]

IN WITNESS WHEREOF, the undersigned has executed and delivered this Release as of the date first written above.

JEFFERIES FINANCE LLC,
as Collateral Agent and Releasor

By: _____
Name: Paul Chisholm
Title: Managing Director

[Signature Page to Release of Patent Security Interest]

SCHEDULE A

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
08/396,994	5574678	United States	Continuous Time Programmable Analog Block Architecture	Issued	Lattice Semiconductor Corporation
08/403,359	5510738	United States	CMOS Programmable Resistor-Based Transconductor	Issued	Lattice Semiconductor Corporation
08/403,354	5493205	United States	Low Distortion Differential Transconductor Output Current Mirror	Issued	Lattice Semiconductor Corporation
08/403,352	5617064	United States	Active Resistor For Stability Compensation [of Transconductor & Op-Amp Based Gain & Filter Stages]	Issued	Lattice Semiconductor Corporation
08/403,595	5670907	United States	VBB Reference for Pumped Substrates	Issued	Lattice Semiconductor Corporation
08/423,303	5490074	United States	Constant delay interconnect for coupling configurable logic blocks	Issued	Lattice Semiconductor Corporation
08/427,117	5596524	United States	CMOS memory cell with gate oxide of both NMOS and PMOS transistors as tunneling window for program and erase	Issued	Lattice Semiconductor Corporation
08/444,306	5491433	United States	Cascode array cell partitioning for a sense amplifier of a programmable logic device	Issued	Lattice Semiconductor Corporation
08/449,384	5756367	United States	Method of making a spacer based antifuse structure for low capacitance and high reliability	Issued	Lattice Semiconductor Corporation
08/447,991	5594687	United States	Completely complementary MOS memory cell with tunneling through the NMOS and PMOS transistors during program and erase	Issued	Lattice Semiconductor Corporation

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
08/453,184	5570046	United States	Lead frame with noisy and quiet Vss and Vdd leads	Issued	Lattice Semiconductor Corporation
08/453,479	5583451	United States	Polarity control circuit which may be used with a ground bounce limiting buffer	Issued	Lattice Semiconductor Corporation
08/456,946	5621650	United States	Programmable gate array with improved interconnect structure, input/output structure and configurable logic block	Issued	Lattice Semiconductor Corporation
08/459,960	5521529	United States	Very high-density complex programmable logic device with a multi-tiered hierarchical switch matrix and optimized flexible logic allocation	Issued	Lattice Semiconductor Corporation
08/459,230	5818254	United States	Multi-tiered hierarchical high speed switch matrix structure for very high-density complex programmable logic devices	Issued	Lattice Semiconductor Corporation
08/459,234	5781030	United States	Programmable uniform symmetrical distribution logic allocator for a high-density complex PLD	Issued	Lattice Semiconductor Corporation
08/459,786	5638018	United States	P-type flip flop	Issued	Lattice Semiconductor Corporation
08/458,865	5589782	United States	Macrocell and clock signal allocation circuit for a programmable logic device (PLD) enabling PLD resources to provide multiple functions	Issued	Lattice Semiconductor Corporation
08/459,570	6531890	United States	Programmable optimized-distribution logic allocator for a high-density complex PLD	Issued	Lattice Semiconductor Corporation
08/461,196	5586044	United States	Array of configurable logic blocks including cascadable lookup tables	Issued	Lattice Semiconductor Corporation
08/462,934	5469368	United States	Array of configurable logic blocks each including a first	Issued	Lattice Semiconductor

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			lookup table coupled to selectively replace an output of second lookup with an alternate function output		Corporation
08/486,178	5764078	United States	Family of multiple segmented programmable logic blocks interconnected by a high speed centralized switch matrix	Issued	Lattice Semiconductor Corporation
08/474,629	5612631	United States	An I/O macrocell for a programmable logic device	Issued	Lattice Semiconductor Corporation
08/479,872	5869981	United States	A High density programmable logic device	Issued	Lattice Semiconductor Corporation
08/486,174	5594365	United States	Architecture of a multiple array high density programmable logic device with a plurality of programmable switch matrices	Issued	Lattice Semiconductor Corporation
08/474,635	5811986	United States	Flexible synchronous/asynchronous cell structure for a high density programmable logic device	Issued	Lattice Semiconductor Corporation
08/466,438	5754471	United States	Reference for CMOS memory cell having PMOS and NMOS transistors with a common floating gate	Issued	Lattice Semiconductor Corporation
08/466,438	5754471	United States	Low power CMOS array for a PLD with program and erase using controlled avalanche injection	Issued	Lattice Semiconductor Corporation
08/473,620	5594657	United States	Field Programmable Gate Array Using Look-Up Tables, Multiplexers and Decoders	Issued	Lattice Semiconductor Corporation
08/483,623	5617042	United States	Multiple array programmable logic device with a plurality of programmable switch matrices	Issued	Lattice Semiconductor Corporation
08/492,604	5526278	United States	System for Synthesizing Field Programmable Gate Array	Issued	Lattice Semiconductor

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			Implementations From High Level Circuit Descriptions		Corporation
08/493,640	5679599	United States	Isolation using self-aligned trench formation and conventional LOCOS	Issued	Lattice Semiconductor Corporation
08/494,271	5565794	United States	Voltage range tolerant CMOS output buffer with reduced input capacitance	Issued	Lattice Semiconductor Corporation
08/497,992	5742542	United States	Nonvolatile memory cells using only positive charge to store data	Issued	Lattice Semiconductor Corporation
08/500,295	5700698	United States	Method for screening non-volatile memory and programmable logic devices	Issued	Lattice Semiconductor Corporation
08/501,230	5604370	United States	Field Implant For Semiconductor Device	Issued	Lattice Semiconductor Corporation
08/505,837	5635855	United States	Method for Simultaneous Programming of In-System Programmable Integrated Circuits	Issued	Lattice Semiconductor Corporation
08/507,893	5570039	United States	Method and Apparatus for Converting Field-Programmable Gate Array Implementations Into Mask-Programmable Logic Cell Implementations	Issued	Lattice Semiconductor Corporation
08/507,957	5559450	United States	Programmable Function Unit As Parallel Multiplier Cell	Issued	Lattice Semiconductor Corporation
08/528,030	5581126	United States	Interlaced layout configuration for differential pairs of interconnect lines	Issued	Lattice Semiconductor Corporation
08/535,362	5528170	United States	Low-Skew Signal Routing In A Programmable Array	Issued	Lattice Semiconductor Corporation
08/551,974	5615150	United States	control gate-addressed cmos non-volatile cell that programs through gates of CMOS transistors	Issued	Lattice Semiconductor Corporation

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
08/554,092	5587945	United States	CMOS EEPROM cell with tunneling window in the read path	Issued	Lattice Semiconductor Corporation
08/560,038	5666309	United States	Memory cell for a programmable logic device (PLD) avoiding pumping programming voltage above an NMOS threshold	Issued	Lattice Semiconductor Corporation
08/560,933	5587921	United States	Array of configurable logic blocks each including a lookup table having inputs coupled to a first multiplexer and having outputs to a second multiplexer	Issued	Lattice Semiconductor Corporation
08/561,306	5672521	United States	Method of forming multiple gate oxide thicknesses on a wafer substrate	Issued	Lattice Semiconductor Corporation
08/573,622	5809522	United States	Microprocessor system with process identification tag entries to reduce cache flushing after a context switch	Issued	Lattice Semiconductor Corporation
08/574,776	5739713	United States	Deconvolution input buffer compensating for capacitance of a switch matrix of a high density programmable logic device	Issued	Lattice Semiconductor Corporation
08/575,898	5736888	United States	Capacitance elimination circuit	Issued	Lattice Semiconductor Corporation
08/575,852	5719516	United States	Clock generator circuit for use with a dual edge register that provides a separate enable for each edge over an input clock signal	Issued	Lattice Semiconductor Corporation
08/596,679	5598346	United States	Array of configurable logic blocks including network means for broadcasting clock signals to different pluralities of logic blocks	Issued	Lattice Semiconductor Corporation
08/606,702	5623217	United States	Field Programmable Gate Array With Write-Port Enabled Memory	Issued	Lattice Semiconductor Corporation

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
08/614,728	5926841	United States	Segment descriptor cache for a processor	Issued	Lattice Semiconductor Corporation
08/625,403	5646901	United States	CMOS memory cell with tunneling during program and erase through the NMOS and PMOS transistors and a pass gate separating the NMOS and PMOS transistors	Issued	Lattice Semiconductor Corporation
08/632,811	5751163	United States	Parallel Programming of ISP Devices Using An Automatic Tester	Issued	Lattice Semiconductor Corporation
08/635,184	5666087	United States	Active Resistor For Stability Compensation [of Transconductor & Op-Amp Based Gain & Filter Stages]	Issued	Lattice Semiconductor Corporation
08/643,807	5748525	United States	Array cell circuit with split read/write line	Issued	Lattice Semiconductor Corporation
08/643,291	5864486	United States	Method And Apparatus For In-System Programming of A Programmable Logic Device Using a Two-Wire Interface	Issued	Lattice Semiconductor Corporation
08/653,186	5789939	United States	Very high-density complex programmable logic device with a multi-tiered hierarchical switch matrix and optimized flexible logic allocation	Issued	Lattice Semiconductor Corporation
08/659,279	5723984	United States	Field programmable gate array (FPGA) with interconnect encoding	Issued	Lattice Semiconductor Corporation
08/659,941	5808942	United States	Field programmable gate array (FPGA) having an improved configuration memory and look up table	Issued	Lattice Semiconductor Corporation
08/664,190	5830795	United States	Simplified masking process for programmable logic device manufacture	Issued	Lattice Semiconductor Corporation
08/666,193	5760609	United States	Clock signal providing circuit with enable and a pulse generator with enable for use	Issued	Lattice Semiconductor Corporation

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			in a block clock circuit of a programmable logic device		
08/668,141	5796295	United States	Reference for CMOS memory cell having PMOS and NMOS transistors with a common floating gate	Issued	Lattice Semiconductor Corporation
08/668,896	5751164	United States	Programmable logic device with multi-level power control	Issued	Lattice Semiconductor Corporation
08/683,685	5734275	United States	Programmable logic device having a sense amplifier with virtual ground	Issued	Lattice Semiconductor Corporation
08/683,373	5818294	United States	Temperature insensitive current source	Issued	Lattice Semiconductor Corporation
08/690,768	5801551	United States	Depletion mode pass gates with controlling decoder and negative power supply for a programmable logic device	Issued	Lattice Semiconductor Corporation
08/689,523	5942780	United States	An integrated circuit having, and process providing, different oxide layer thicknesses on a substrate	Issued	Lattice Semiconductor Corporation
08/696,444	5796750	United States	Method for Programming a PLD In An Automatic Tester	Issued	Lattice Semiconductor Corporation
08/700,616	5740069	United States	Logic device (PLD) having direct connections between configurable logic blocks (CLBs) and configurable input/output blocks (IOBs)	Issued	Lattice Semiconductor Corporation
08/699,401	5960274	United States	Oxide formation process for manufacturing programmable logic device	Issued	Lattice Semiconductor Corporation
08/702,846	5959336	United States	Decoder circuit with short channel depletion transistors	Issued	Lattice Semiconductor Corporation
08/710,445	5862365	United States	Configuration Pin Emulation Circuit For a Field Programmable Array	Issued	Lattice Semiconductor Corporation

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
08/723,082	5760605	United States	Programmable high speed routing switch	Issued	Lattice Semiconductor Corporation
08/726,512	5761116	United States	Vpp only scalable EEPROM memory cell having transistors with thin tunnel gate oxide	Issued	Lattice Semiconductor Corporation
08/729,117	5991907	United States	Method for Testing Field Programmable Gate Arrays	Issued	Lattice Semiconductor Corporation
08/734,888	5805607	United States	Method for user-controlled I/O switching during in-circuit programming of CPLDs through the IEEE 1149.1 test access port	Issued	Lattice Semiconductor Corporation
08/740,948	5811987	United States	Block clock and initialization circuit for a complex high density PLD	Issued	Lattice Semiconductor Corporation
08/748,041	5892962	United States	FPGA-based Processor	Issued	Lattice Semiconductor Corporation
08/745,410	5717342	United States	Output buffer incorporating shared intermediate nodes	Issued	Lattice Semiconductor Corporation
08/781,882	6028993	United States	Timed Circuit Simulation In Hardware Using FPGAs	Issued	Lattice Semiconductor Corporation
08/785,096	5841701	United States	Method of charging and discharging floating gage transistors to reduce leakage current	Issued	Lattice Semiconductor Corporation
08/799,153	5904575	United States	Method and apparatus incorporating nitrogen selectively for differential oxide growth	Issued	Lattice Semiconductor Corporation
08/799,235	5885904	United States	Method to incorporate, and a device having, oxide enhancement dopants using gas immersion laser doping (GILD) for selectively growing an oxide layer	Issued	Lattice Semiconductor Corporation

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
08/823,953	6190966	United States	Process for fabricating semiconductor memory device with high data retention including silicon nitride etch stop layer formed at high temperature with low hydrogen ion	Issued	Lattice Semiconductor Corporation
08/828,520	5905385	United States	Memory bits used to couple look up table inputs to facilitate increased availability to routing resources particularly for variable sized look up tables for a field programmable gate array (FPGA)	Issued	Lattice Semiconductor Corporation
08/831,372	5844912	United States	Fast verify for CMOS memory cell	Issued	Lattice Semiconductor Corporation
08/827,671	5835405	United States	Application Specific Modules in a Programmable Logic Device	Issued	Lattice Semiconductor Corporation
08/843,150	6087275	United States	Reduction of n-channel parasitic transistor leakage by using low power/low pressure phosphosilicate glass	Issued	Lattice Semiconductor Corporation
08/838,487	6034541	United States	In-System Programmable Interconnect Circuit	Issued	Lattice Semiconductor Corporation
08/856,926	5949279	United States	Devices for sourcing constant supply current from power supply in system with integrated circuit having variable supply current requirement	Issued	Lattice Semiconductor Corporation
08/859,761	5989957	United States	Process for fabricating semiconductor memory device with high data retention including silicon nitride etch stop layer formed at high temperature with low hydrogen ion concentration	Issued	Lattice Semiconductor Corporation
08/871,589	5978272	United States	Nonvolatile memory structure for programmable logic devices	Issued	Lattice Semiconductor Corporation

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
08/899,428	6028447	United States	FPGA Having Predictable Open-Drain Drive Mode	Issued	Lattice Semiconductor Corporation
08/912,763	6072351	United States	Output buffer for making a high voltage (5.0 volt) compatible input/output in a low voltage (2.5 volt) semiconductor process	Issued	Lattice Semiconductor Corporation
08/931,798	6359466	United States	Circuitry to provide fast carry	Issued	Lattice Semiconductor Corporation
08/938,550	6020755	United States	Hybrid Programmable Gate Arrays	Issued	Lattice Semiconductor Corporation
08/948,306	6097212	United States	Variable grain architecture for FPGA integrated circuits	Issued	Lattice Semiconductor Corporation
08/947,888	5854114	United States	Data retention of EEPROM cell with shallow trench isolation using thicker liner oxide	Issued	Lattice Semiconductor Corporation
08/949,992	6028463	United States	Programmable Clock Manager For A Programmable Logic Device that Can Generate At Least Two Different Output Clocks	Issued	Lattice Semiconductor Corporation
08/950,444	6216191	United States	Field Programmable Gate Array Having A Dedicated Processor Interface	Issued	Lattice Semiconductor Corporation
08/950,446	5986471	United States	Bi-directional Buffers and Supplemental Logic and Interconnect Cells for Programmable Logic Devices	Issued	Lattice Semiconductor Corporation
08/950,448	6060902	United States	A Programmable Clock Manager For A Programmable Logic Device that Can Be Programmed Without Reconfiguring the Device	Issued	Lattice Semiconductor Corporation
08/950,624	6049224	United States	Programmable Logic Device With Logic Cells Having A Flexible Input Structure	Issued	Lattice Semiconductor Corporation

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
08/951,128	6043677	United States	Programmable Clock Manager For A Programmable Logic Device that Can Implement Delay-Locked Loop Functions	Issued	Lattice Semiconductor Corporation
08/964,421	6389321	United States	Simultaneous Wired and Wireless Remote In-System Programming of Multiple Remote Systems	Issued	Lattice Semiconductor Corporation
08/974,799	6003150	United States	Method for Testing Field Programmable Gate Arrays	Issued	Lattice Semiconductor Corporation
08/996,361	6275064	United States	Symmetrical, extended and fast direct connections between variable grain blocks in FPGA integrated circuits	Issued	Lattice Semiconductor Corporation
08/996,049	6127843	United States	Dual port SRAM memory for run time use in FPGA integrated circuits	Issued	Lattice Semiconductor Corporation
08/995,615	6034544	United States	Programmable input/output block (IOB) in FPGA integrated circuits	Issued	Lattice Semiconductor Corporation
08/995,614	5982193	United States	Input/output block (IOB) connections to MAXL lines, NOR lines and dendrites in FPGA integrated circuits	Issued	Lattice Semiconductor Corporation
08/995,612	5990702	United States	Flexible direct connections between input/output blocks (IOBs) and variable grain blocks (VBGs) in FPGA integrated circuits	Issued	Lattice Semiconductor Corporation
08/997,221	6107823	United States	Programmable control multiplexing for input/output blocks (IOBs) in FPGA integrated circuits	Issued	Lattice Semiconductor Corporation
08/996,119	5986480	United States	Multiple input zero power and/nor gate for use in a field programmable gate array (FPGA)	Issued	Lattice Semiconductor Corporation
08/996,530	6134703	United States	A Process for Programming PLDs and Embedded Non-Volatile Memories	Issued	Lattice Semiconductor Corporation

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
08/998,978	6102963	United States	Electrically erasable and reprogrammable, nonvolatile integrated storage device with in-system programming and verification (ISPAV) capabilities for supporting in-system reconfiguring of PLD's	Issued	Lattice Semiconductor Corporation
09/008,762	6130551	United States	Synthesis-friendly FPGA architecture with variable length and variable timing interconnect	Issued	Lattice Semiconductor Corporation
09/010,000	6034538	United States	Virtual Logic System For Reconfigurable Hardware	Issued	Lattice Semiconductor Corporation
09/023,669	6025637	United States	Spacer based antifuse structure for low capacitance and high reliability and method of fabrication thereof	Issued	Lattice Semiconductor Corporation
09/023,506	6023570	United States	Sequential and Simultaneous Manufacturing Programming of Multiple In-System Programmable Systems Through a Data Network	Issued	Lattice Semiconductor Corporation
09/026,814	6093946	United States	EEPROM cell with field-edgeless tunnel window using shallow trench isolation process	Issued	Lattice Semiconductor Corporation
09/037,095	6128770	United States	Configurable logic array including IOB to longlines interconnect means for providing selectable access to plural longlines from each IOB (input/output block)	Issued	Lattice Semiconductor Corporation
09/045,128	6064225	United States	Global Signal Distribution With Reduced Routing Tracks In An FPGA	Issued	Lattice Semiconductor Corporation
09/046,404	5982683	United States	Enhanced method of testing semiconductor devices having nonvolatile elements	Issued	Lattice Semiconductor Corporation
09/053,251	6556154	United States	Offset Voltage Calibration DAC With Reduced Sensitivity To Mismatch	Issued	Lattice Semiconductor Corporation

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			Errors		
09/059,552	6108806	United States	Method of Testing and Diagnosing Field Programmable Gate Arrays	Issued	Lattice Semiconductor Corporation
09/067,320	6154050	United States	Internal tristate bus with arbitration logic	Issued	Lattice Semiconductor Corporation
09/067,318	6104207	United States	Programmable Logic Device	Issued	Lattice Semiconductor Corporation
09/069,035	6133750	United States	Combination of global clock and localized clocks	Issued	Lattice Semiconductor Corporation
09/069,768	6002610	United States	Non-Volatile Memory Element For Programmable Logic Applications and Operational Methods Therefor	Issued	Lattice Semiconductor Corporation
09/080,906	6225821	United States	Package migration for related programmable logic devices	Issued	Lattice Semiconductor Corporation
09/083,335	6304099	United States	Method and structure for dynamic in-system programming	Issued	Lattice Semiconductor Corporation
09/083,336	6066977	United States	Programmable Output Voltage Levels	Issued	Lattice Semiconductor Corporation
09/083,205	6255847	United States	Programmable Logic Device	Issued	Lattice Semiconductor Corporation
09/086,437	6087696	United States	Stacked tunneling dielectric technology for improving data retention of EEPROM cell	Issued	Lattice Semiconductor Corporation
09/109,123	6202182	United States	Method and Apparatus For Testing Field Programmable Gate Arrays	Issued	Lattice Semiconductor Corporation
09/114,385	6028758	United States	Electrostatic discharge (ESD) protection for a 5.0 volt compatible input/output (I/O) in a 2.5 volt semiconductor process	Issued	Lattice Semiconductor Corporation

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
09/114,717	6091595	United States	Electrostatic discharge (ESD) protection for NMOS pull up transistors of a 5.0 volt compatible output buffer using 2.5 volt process transistors	Issued	Lattice Semiconductor Corporation
09/114,718	6043969	United States	Ballast resistors with parallel stacked NMOS transistors used to prevent secondary breakdown during ESD with 2.5 volt process transistors	Issued	Lattice Semiconductor Corporation
09/115,683	6124732	United States	Signaling Voltage Range Discriminator	Issued	Lattice Semiconductor Corporation
09/118,200	6028446	United States	Flexible Synchronous and Asynchronus Circuits for A Very High Density Programmable Logic Device	Issued	Lattice Semiconductor Corporation
09/134,174	6064105	United States	Data retention of EEPROM cell with shallow trench isolation using thicker liner oxide	Issued	Lattice Semiconductor Corporation
09/145,793	6087854	United States	High Speed Line Driver With Direct and Complementary Outputs	Issued	Lattice Semiconductor Corporation
09/169,848	6347387	United States	Test Circuits For Multiple FPGA Systems	Issued	Lattice Semiconductor Corporation
09/169,492	6424003	United States	EEPROM cell with self-aligned tunneling window	Issued	Lattice Semiconductor Corporation
09/187,691	6228696	United States	Semiconductor-oxide-semiconductor capacitor formed in integrated circuit	Issued	Lattice Semiconductor Corporation
09/187,689	6154051	United States	Tileable and compact layout for super variable grain blocks within FPGA device	Issued	Lattice Semiconductor Corporation
09/186,917	6229336	United States	Programmable integrated circuit device with slew control and skew control	Issued	Lattice Semiconductor Corporation
09/188,778	6169432	United States	High voltage switch for	Issued	Lattice

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			providing voltages higher than 2.5 volts with transistors made using a 2.5 volt process		Semiconductor Corporation
09/192,094	6291327	United States	Optimization of S/D annealing to minimize random S/D shorts in memory array	Issued	Lattice Semiconductor Corporation
09/192,096	6221733	United States	Reduction of mechanical stress in shallow trench isolation process	Issued	Lattice Semiconductor Corporation
09/196,449	6191612	United States	Enhanced I/O control flexibility for generating control signals	Issued	Lattice Semiconductor Corporation
09/196,080	5912550	United States	Power converter with 2.5 semiconductor process components	Issued	Lattice Semiconductor Corporation
09/198,796	6218857	United States	Variable sized line driving amplifiers for input/output blocks (IOBs) in FPGA integrated circuits	Issued	Lattice Semiconductor Corporation
09/200,395	6261944	United States	Semiconductor device having high reliability passivation and fabrication method	Issued	Lattice Semiconductor Corporation
09/198,653	6009033	United States	Method of programming and erasing an EEPROM device under an elevated temperature and apparatus thereof	Issued	Lattice Semiconductor Corporation
09/199,664	6353352	United States	Clock tree topology	Issued	Lattice Semiconductor Corporation
09/201,081	6133769	United States	Phase locked loop with a lock detector	Issued	Lattice Semiconductor Corporation
09/203,149	6404006	United States	EEPROM cell with tunneling across entire separated channels	Issued	Lattice Semiconductor Corporation
09/217,647	5969992	United States	EEPROM cell using p-well for	Issued	Lattice Semiconductor Corporation
09/207,558	6175266	United States	Operational amplifier with CMOS transistors made using	Issued	Lattice Semiconductor

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			2.5 volt process transistors		Corporation
09/208,203	6163168	United States	Efficient interconnect network for use in FPGA device having variable grain architecture	Issued	Lattice Semiconductor Corporation
09/212,022	6124730	United States	Methods for configuring FPGA's having variable grain blocks and shared logic for providing time-shared access to interconnect resources	Issued	Lattice Semiconductor Corporation
09/212,330	6100715	United States	Methods for configuring FPGA's having variable grain blocks and shared logic for providing time-shared access to interconnect resources	Issued	Lattice Semiconductor Corporation
09/212,331	6081473	United States	FPGA integrated circuit having embedded SRAM memory blocks each with statically and dynamically controllable read mode	Issued	Lattice Semiconductor Corporation
09/216,662	6204686	United States	Methods for configuring FPGA's having variable grain blocks and shared logic for providing symmetric routing of result output to differently-directed and tristateable interconnect resources	Issued	Lattice Semiconductor Corporation
09/216,051	6214666	United States	Method of forming a non-volatile memory device	Issued	Lattice Semiconductor Corporation
09/217,648	6232631	United States	Floating gate memory cell structure with programming mechanism outside the read path	Issued	Lattice Semiconductor Corporation
09/217,646	6282123	United States	Method of fabricating, programming, and erasing a dual pocket two sided program/erase non-volatile memory cell	Issued	Lattice Semiconductor Corporation
09/218,987	6294810	United States	EEPROM cell with tunneling at separate edge and channel regions	Issued	Lattice Semiconductor Corporation

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
09/220,469	6157568	United States	Avalanche programmed floating gate memory cell structure with program element in first polysilicon layer	Issued	Lattice Semiconductor Corporation
09/221,360	6294809	United States	Avalanche programmed floating gate memory cell structure with program element in polysilicon	Issued	Lattice Semiconductor Corporation
09/226,702	6215700	United States	PMOS avalanche programmed floating gate memory cell structure	Issued	Lattice Semiconductor Corporation
09/227,981	6197638	United States	Oxide formation process for manufacturing programmable logic device	Issued	Lattice Semiconductor Corporation
09/235,356	6097664	United States	Multi-port SRAM cell array having plural write paths including for writing through addressable port and through serial boundary scan	Issued	Lattice Semiconductor Corporation
09/235,351	6181163	United States	FPGA integrated circuit having embedded SRAM memory blocks and interconnect channel for broadcasting address and control	Issued	Lattice Semiconductor Corporation
09/235,615	6211695	United States	FPGA integrated circuit having embedded SRAM memory blocks with registered address and data input sections	Issued	Lattice Semiconductor Corporation
09/239,072	5999449	United States	Two transistor EEPROM cell using P-well for tunneling across a channel	Issued	Lattice Semiconductor Corporation
09/240,560	6297128	United States	Process for manufacturing shallow trenches filled with dielectric material having low mechanical stress	Issued	Lattice Semiconductor Corporation
09/245,813	6294811	United States	Two transistor EEPROM cell	Issued	Lattice Semiconductor Corporation
09/255,410	6075724	United States	Method for sorting	Issued	Lattice

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			semiconductor devices having a plurality of non-volatile memory cells		Semiconductor Corporation
09/255,053	6255169	United States	Process for fabricating a high-endurance non-volatile memory device	Issued	Lattice Semiconductor Corporation
09/256,245	6133164	United States	Fabrication of oxide regions having multiple thicknesses using minimized number of thermal cycles	Issued	Lattice Semiconductor Corporation
09/261,776	6256758	United States	Fault Tolerance Operation of Field Programmable Gate Arrays	Issued	Lattice Semiconductor Corporation
09/263412	6075293	United States	Semiconductor device having a multi-layer metal interconnect structure	Issued	Lattice Semiconductor Corporation
09/268,897	6207989	United States	Non-volatile memory device having a high-reliability composite insulation layer	Issued	Lattice Semiconductor Corporation
09/276,991	6031365	United States	Band gap reference using a low voltage power supply	Issued	Lattice Semiconductor Corporation
09/276,990	6163175	United States	High voltage detector to control a power supply voltage pump for a 2.5 volt semiconductor process device	Issued	Lattice Semiconductor Corporation
09/277,441	6326663	United States	Avalanche injection EEPROM memory cell with p-type control gate	Issued	Lattice Semiconductor Corporation
09/280,887	6172392	United States	Boron doped silicon capacitor plate	Issued	Lattice Semiconductor Corporation
09/286,830	6284626	United States	Angled nitrogen ion implantation for minimizing mechanical stress on side walls of an isolation trench	Issued	Lattice Semiconductor Corporation
09/288,062	6265900	United States	High Speed Logical OR Circuit	Issued	Lattice Semiconductor Corporation
09/287,976	6413826	United States	Gate insulator process for	Issued	Lattice Semiconductor

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			nanometer MOSFETs		Corporation
09/310,071	6424000	United States	Floating gate memory apparatus and method for selected programming thereof	Issued	Lattice Semiconductor Corporation
09/316,241	6274898	United States	Triple-well EEPROM cell using p-well for tunneling across a channel	Issued	Lattice Semiconductor Corporation
09/318,570	6552595	United States	High Voltage Discharge Scheme	Issued	Lattice Semiconductor Corporation
09/320389	6118693	United States	Electrically erasable non-volatile memory cell with integrated SRAM to reduce testing time	Issued	Lattice Semiconductor Corporation
09/320,392	6067252	United States	Electrically erasable non-volatile memory cell with no static power dissipation	Issued	Lattice Semiconductor Corporation
09/326,940	6184713	United States	Scalable architecture for high density CPLD's having two-level hierarchy of routing resources	Issued	Lattice Semiconductor Corporation
09/326,140	6150841	United States	Enhanced storage macrocell module for high density CPLD architectures	Issued	Lattice Semiconductor Corporation
09/330,753	6628660	United States	Finite State Machine with Associated Memory	Issued	Lattice Semiconductor Corporation
09/334,051	6028789	United States	Zero-power CMOS non-volatile memory cell having an avalanche injection element	Issued	Lattice Semiconductor Corporation
09/334,052	6034893	United States	Non-volatile memory cell having dual avalanche injection elements	Issued	Lattice Semiconductor Corporation
09/400,029	6404226	United States	Integrated Circuit With Standard Cell Logic and Spare Gates	Issued	Lattice Semiconductor Corporation
09/405,958	6550030	United States	On-Line Testing of the Programmable Logic Blocks In Field Programmable Gate	Issued	Lattice Semiconductor Corporation

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			Arrays		
09/406,219	6574761	United States	On-Line Testing of the Programmable Interconnect Network In Field Programmable Gate Arrays	Issued	Lattice Semiconductor Corporation
09/433,642	6191609	United States	Combination of global clock and localized clocks	Issued	Lattice Semiconductor Corporation
09/440,460	6294925	United States	Programmable Logic Device	Issued	Lattice Semiconductor Corporation
09/440,207	6278311	United States	Method for minimizing instantaneous currents when driving bus signals	Issued	Lattice Semiconductor Corporation
09/441,220	6208559	United States	Method of operating EEPROM memory cells having transistors with thin gate oxide and reduced disturb	Issued	Lattice Semiconductor Corporation
09/452,017	6137738	United States	Method For In-System Programming of Serially Configured EEPROMS Using a JTAG Interface of an FPGA	Issued	Lattice Semiconductor Corporation
09/454,322	6326808	United States	Inversion of Product Term Line Before or Logic in a Programmable Logic Device (PLD)	Issued	Lattice Semiconductor Corporation
09/472,645	6150842	United States	Variable grain architecture for FPGA integrated circuits	Issued	Lattice Semiconductor Corporation
09/506,180	6362684	United States	Amplifier Having an Adjustable Resistor Network	Issued	Lattice Semiconductor Corporation
09/507,580	6424209	United States	Integrated Programmable Continuous Time Filter with Programmable Capacitor Arrays	Issued	Lattice Semiconductor Corporation
09/548,171	6351157	United States	Output buffer for making a high voltage (5.0 volt) compatible input/output in a low voltage (2.5 volt)	Issued	Lattice Semiconductor Corporation

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			semiconductor process		
09/567,898	6288937	United States	Decoded Generic Routing Pool	Issued	Lattice Semiconductor Corporation
09/578,086	6570212	United States	Complementary avalanche injection EEPROM cell	Issued	Lattice Semiconductor Corporation
09/603,119	6292930	United States	Methods for configuring FPGA's having variable grain blocks and shared logic for providing time-shared access to interconnect resources	Issued	Lattice Semiconductor Corporation
09/603,807	6216257	United States	FPGA device and method that includes a variable grain function architecture for implementing configuration logic blocks and a complimentary variable length interconnect architecture for providing configurable routing between configuration logic blocks	Issued	Lattice Semiconductor Corporation
09/611,449	6530049	United States	On-line Fault Tolerant Operation Via Incremental Reconfiguration of Field Programmable Gate Arrays	Issued	Lattice Semiconductor Corporation
09/626,094	6380759	United States	Variable grain architecture for FPGA integrated circuits	Issued	Lattice Semiconductor Corporation
09/632,319	6567969	United States	Configurable Logic Array Including Lookup Table Means For Generating Functions of Different Numbers Of Input Terms	Issued	Lattice Semiconductor Corporation
09/643,279	6627947	United States	Compact single-poly two-transistor EEPROM cell	Issued	Lattice Semiconductor Corporation
09/651,689	6433602	United States	High speed schmitt trigger with low supply voltage	Issued	Lattice Semiconductor Corporation
09/660,707	6370071	United States	High Voltage CMOS switch	Issued	Lattice Semiconductor

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
					Corporation
09/661,585	6462576	United States	Programmable Logic Device	Issued	Lattice Semiconductor Corporation
09/668,896	6701340	United States	Double Differential Comparator and Programmable Analog Block Architecture Using Same	Issued	Lattice Semiconductor Corporation
09/669,186	6249144	United States	Methods for configuring FPGA's having variable grain blocks and shared logic for providing time-shared access to interconnect resources	Issued	Lattice Semiconductor Corporation
09/671,853	6631487	United States	On-Line Testing of Field Programmable Gate Array Resources	Issued	Lattice Semiconductor Corporation
09/692,694	6470485	United States	Scalable and parallel processing methods and structures for testing configurable interconnect network in FPGA device	Issued	Lattice Semiconductor Corporation
09/704,487	6507212	United States	Wide input programmable logic system and method	Issued	Lattice Semiconductor Corporation
09/651,805	6455912	United States	Process for manufacturing shallow trenches filled with dielectric material having low mechanical stress	Issued	Lattice Semiconductor Corporation
09/712,000	6356107	United States	Method and structure for dynamic in-system programming	Issued	Lattice Semiconductor Corporation
09/721,153	6348813	United States	Scalable architecture for high density CPLD's having two-level hierarchy of routing resources	Issued	Lattice Semiconductor Corporation
09/732,216	6735706	United States	Programmable power management system and method	Issued	Lattice Semiconductor Corporation
09/731,184	6524911	United States	Combination of BPTEOS oxide film with CMP and RTA to achieve good data	Issued	Lattice Semiconductor Corporation

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			retention		
09/731,185	6287916	United States	Method for forming a semiconductor device using LPCVD nitride to protect floating gate from charge loss	Issued	Lattice Semiconductor Corporation
09/733,878	6526558	United States	Methods for configuring FPGA's having variable grain blocks and shared logic for providing symmetric routing of result output to differently-directed and tristateable interconnect resources	Issued	Lattice Semiconductor Corporation
09/775,488	6462602	United States	Voltage Level Translator Systems And Methods	Issued	Lattice Semiconductor Corporation
09/775,489	6414521	United States	Improved sense amplifier systems and methods	Issued	Lattice Semiconductor Corporation
09/818,257	6496969	United States	Programming Programmable Logic Devices Using Hidden Switches	Issued	Lattice Semiconductor Corporation
09/841,209	6590415	United States	Methods for configuring FPGA's having variable grain blocks and shared logic for providing time-shared access to interconnect resources	Issued	Lattice Semiconductor Corporation
09/863,656	6535043	United States	Clock Signal Selection System, Method of Generating A Clock Signal And Programmable Clock Manager Including Same	Issued	Lattice Semiconductor Corporation
09/864,276	6486705	United States	Signal Distribution Scheme In Field Programmable Gate Array (FPGA) or Field Programmable Systems Chip (FPSC) Including Cycle Stealing Units	Issued	Lattice Semiconductor Corporation
09/864,284	6472904	United States	Double Data Rate Input And Output In A Programmable Logic Device	Issued	Lattice Semiconductor Corporation
09/864,289	6480026	United States	Multi-functional I/O Buffers In a Field Programmable Gate	Issued	Lattice Semiconductor

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			Array (FPGA)		Corporation
09/864,277	6483342	United States	Multi-Master Multi-Slave Bus In Field Programmable Gate Array (FPGA)	Issued	Lattice Semiconductor Corporation
09/864,290	6772230	United States	Field Programmable Gate Array (FPGA) Bit Stream Format	Issued	Lattice Semiconductor Corporation
09/870,877	6498538	United States	Low Jitter Integrated Phase Locked Loop With Broad Tuning Range	Issued	Lattice Semiconductor Corporation
09/870,541	6455375	United States	EEPROM tunnel window for program injection via P+ contacted inversion	Issued	Lattice Semiconductor Corporation
09/881,950	6614291	United States	Low Voltage, High Speed CMOS CML Latch and MUX Devices	Issued	Lattice Semiconductor Corporation
09/885,243	6429692	United States	High Speed Data Sampling With Reduced Metastability	Issued	Lattice Semiconductor Corporation
09/927,289	6492877	United States	Improved Coupling For LC-Based VCO	Issued	Lattice Semiconductor Corporation
09/927,612	6525617	United States	Buffering For LC-Based Stage	Issued	Lattice Semiconductor Corporation
09/927,793	6653860	United States	Enhanced logic macrocell with expanded PT (product term) sharing capability for Use in High Density CPLD Architectures	Issued	Lattice Semiconductor Corporation
09/941,454	6489835	United States	Low Voltage Bandgap Reference Circuit	Issued	Lattice Semiconductor Corporation
09/949,112	6593222	United States	Method to improve the reliability of thermosonic gold to aluminum wire bonds	Issued	Lattice Semiconductor Corporation
09/966,967	6832231	United States	Multiple Width Random Number Generation	Issued	Lattice Semiconductor Corporation

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
10/011,549	6693830	United States	Single Poly Two-Transistor EEPROM Cell With Differentially Doped Floating Gate	Issued	Lattice Semiconductor Corporation
10/053,004	6989551	United States	Test structure for determining the minimum tunnel opening size in a non-volatile memory cell	Issued	Lattice Semiconductor Corporation
10/010,011	6515899	United States	Non-Volatile Memory Cell With Enhanced Cell Drive Current	Issued	Lattice Semiconductor Corporation
09/991,245	6611463	United States	Zero Power Programmable Memory Cell	Issued	Lattice Semiconductor Corporation
09/992,493	6489806	United States	Zero power logic cell for use in programmable logic devices	Issued	Lattice Semiconductor Corporation
10/006,559	7003066	United States	Digital Phase locked Loop with Phase Selector having Minimized Number of Phase Interpolators	Issued	Lattice Semiconductor Corporation
10/006,610	6999543	United States	Clock Data Recovery Deserializer With Programmable Sync Detect Logic	Issued	Lattice Semiconductor Corporation
10/006,516	6993108	United States	Digital Phase Locked Loop With Programmable Digital Filter	Issued	Lattice Semiconductor Corporation
10/021,873	6661254	United States	Programmable Interconnect Circuit With A Phase-Locked Loop	Issued	Lattice Semiconductor Corporation
10/017,725	6674303	United States	Programmable I/O cell with bidirectional and shift register capabilities	Issued	Lattice Semiconductor Corporation
10/017,859	6605959	United States	Structure and Method for Implementing Wide Multiplexers	Issued	Lattice Semiconductor Corporation
10/022,464	7154298	United States	Block oriented architecture for programmable interconnect circuit	Issued	Lattice Semiconductor Corporation

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
10/021,844	6703860	United States	I/O Block for Programmable Interconnect Circuit	Issued	Lattice Semiconductor Corporation
10/023,053	6653861	United States	Multi-level Routing Structure for a Programmable Interconnect Circuit	Issued	Lattice Semiconductor Corporation
10/023,226	6650141	United States	High Speed Interface For a Programmable Interconnect Circuit	Issued	Lattice Semiconductor Corporation
10/059,624	6636442	United States	Non-volatile memory element having a cascoded transistor scheme to reduce oxide field stress	Issued	Lattice Semiconductor Corporation
10/061,057	6845044	United States	Method of preventing high Icc at start-up in zero-power EEPROM cells for PLD applications	Issued	Lattice Semiconductor Corporation
10/066,031	6680625	United States	Symmetrical CML Logic Gate System	Issued	Lattice Semiconductor Corporation
10/082,050	6781170	United States	Integrated Circuit Base Transistor Structure And Associated Programmable Cell Library	Issued	Lattice Semiconductor Corporation
10/083,728	6600188	United States	An EEPROM with neutralized doping at tunnel window edge	Issued	Lattice Semiconductor Corporation
10/090,209	6621298	United States	Variable grain architecture for FPGA integrated circuits	Issued	Lattice Semiconductor Corporation
10/103,100	6795959	United States	Integrated Delay Discriminator For Use With a Field- Programmable Gate Array and A Method of Determining a Time Delay Thereof	Issued	Lattice Semiconductor Corporation
10/106,509	6907439	United States	FFT address generation method and apparatus	Issued	Lattice Semiconductor Corporation
10/108,401	6976047	United States	Skipped carry incrementer for FFT address generation	Issued	Lattice Semiconductor

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
					Corporation
10/112,370	6639431	United States	Differential Input Comparator	Issued	Lattice Semiconductor Corporation
10/128,943	6660579	United States	Zero Power Memory Cell With Improved Data Retention	Issued	Lattice Semiconductor Corporation
10/131,883	7032162	United States	Polynomial Expander for Generating Coefficients of a Polynomial from Roots of the Polynomial	Issued	Lattice Semiconductor Corporation
10/133,016	6765408	United States	Device and Method with Generic Logic Blocks	Issued	Lattice Semiconductor Corporation
10/135,308	6814296	United States	Integrated Circuit and Associated Design Method With Antenna Error Control Using Spare Gates	Issued	Lattice Semiconductor Corporation
10/135,325	6600341	United States	Integrated Circuit and Associated Design Method Using Spare Gate Islands	Issued	Lattice Semiconductor Corporation
10/146,739	6714048	United States	Input Buffer With Selectable PCL, GTL, or PECL Compatibility	Issued	Lattice Semiconductor Corporation
10/146,826	6657458	United States	Output Buffer With Feedback From An Input Buffer To Provide Selectable PCL, GTL, or PECL Compatability	Issued	Lattice Semiconductor Corporation
10/146,769	6870391	United States	Input Buffer With CMOS Driver Gate Current Control Enabling Selectable PCL, GTL, or PECL Compatibility	Issued	Lattice Semiconductor Corporation
10/147,199	6714043	United States	Output Buffer Having Programmable Drive Current And Output Voltage Limits	Issued	Lattice Semiconductor Corporation
10/146,734	6720755	United States	Band Gap Reference Circuit	Issued	Lattice Semiconductor Corporation
10/147,011	6760209	United States	Electrostatic Discharge Protection Circuit	Issued	Lattice Semiconductor

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
					Corporation
10/151,753	6798244	United States	Output Buffer With Overvoltage Protection	Issued	Lattice Semiconductor Corporation
10/150,410	6848095	United States	Method of Assigning Logic Functions To Macrocells In A Programmable Logic Device	Issued	Lattice Semiconductor Corporation
10/159,009	6583652	United States	Highly linear programmable transconductor with large input-signal range	Issued	Lattice Semiconductor Corporation
10/159,089	6717451	United States	Precision analog level shifter with programmable options	Issued	Lattice Semiconductor Corporation
10/159,681	6806771	United States	Multimode output stage converting differential to single-ended signals using current-mode input signals	Issued	Lattice Semiconductor Corporation
10/162,337	6596587	United States	Shallow junction EEPROM Device and Process for Fabricating the Device	Issued	Lattice Semiconductor Corporation
10/160,855	6794236	United States	EEPROM Device with Improved Capacitive Coupling and Fabrication Process	Issued	Lattice Semiconductor Corporation
10/161,283	6716705	United States	EEPROM Device having a Retrograde Program Junction Region And Process for Fabrication the Device	Issued	Lattice Semiconductor Corporation
10/164,484	6703305	United States	Semiconductor Device Having Metallized Interconnect Structure And Method Of Fabricaton	Issued	Lattice Semiconductor Corporation
10/187,236	6844757	United States	Converting Bits to Vectors In A Programmable Logic Device	Issued	Lattice Semiconductor Corporation
10/191,888	6650143	United States	FPGA Based Upon Transistor gate Oxide Breakdown	Issued	Lattice Semiconductor Corporation
10/194,771	7028281	United States	FPGA With Register-Intensive Architecture	Issued	Lattice Semiconductor

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
					Corporation
10/200,645	6714066	United States	Integrated Programmable Continuous Time Filter with Programmable Capacitor Arrays	Issued	Lattice Semiconductor Corporation
10/207,292	6683477	United States	Wide input programmable logic system and method	Issued	Lattice Semiconductor Corporation
10/210,367	6938197	United States	CRC Calculation System And Method For A Packet Arriving On An N-Byte Wide Bus	Issued	Lattice Semiconductor Corporation
10/211,125	6545313	United States	EEPROM tunnel window for program injection via P+ contacted inversion	Issued	Lattice Semiconductor Corporation
10/219,046	6650142	United States	Enhanced CPLD Macrocell Module Having Selectable Bypass of Steering-based Resource Allocation and Methods of Use	Issued	Lattice Semiconductor Corporation
10/233,021	7043511	United States	Performing Conditional Operations In A Programmable Logic Device	Issued	Lattice Semiconductor Corporation
10/232,912	6841447	United States	EEPROM Device Having An Isolation -Bounded Tunnel Capacitor And Fabrication Process	Issued	Lattice Semiconductor Corporation
10/235,380	6725442	United States	Scalable and parallel processing methods and structures for testing configurable interconnect network in FPGA device	Issued	Lattice Semiconductor Corporation
10/236,829	6842372	United States	EEPROM Cell Having Floating Gate Transistor Within a Cell Well And a Process For Fabricating the Memory Cell	Issued	Lattice Semiconductor Corporation
10/236,114	6833602	United States	Device Having Electrically Isolated Low Voltage And High Voltage Regions And Process For Fabricating the Device	Issued	Lattice Semiconductor Corporation

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
10/236,718	6649514	United States	EEPROM Device Having Improved Data Retention And Process for Fabricating The Device	Issued	Lattice Semiconductor Corporation
10/242,809	6738306	United States	Multiport SRAM Cell	Issued	Lattice Semiconductor Corporation
10/243,014	6917536	United States	Memory access Circuit and Method for reading and writing data with the same clock signal	Issued	Lattice Semiconductor Corporation
10/251,608	6700154	United States	EEPROM cell with trench coupling capacitor	Issued	Lattice Semiconductor Corporation
10/255,474	6907592	United States	Method of Routing In A Programmable Logic Device	Issued	Lattice Semiconductor Corporation
10/255,875	6809551	United States	Method of Optimizing Routing In A Programmable Logic Device	Issued	Lattice Semiconductor Corporation
10/255,499	6803787	United States	State Machine In A Programmable Logic Device	Issued	Lattice Semiconductor Corporation
10/255,656	6812738	United States	Vector Routing In A Programmable Logic Device	Issued	Lattice Semiconductor Corporation
10/263,251	6748575	United States	Programming Programmable Logic Devices Using Hidden Switches	Issued	Lattice Semiconductor Corporation
10/263,507	6846714	United States	Voltage Limted EEPROM Device And Process For Fabricating the Device	Issued	Lattice Semiconductor Corporation
10/266,361	6639434	United States	Low voltage differential signaling systems and methods	Issued	Lattice Semiconductor Corporation
10/269,804	7111183	United States	Expansion method for complex power-sequencing applications	Issued	Lattice Semiconductor Corporation
10/269,450	6791394	United States	Power Supply Control Circuits	Issued	Lattice Semiconductor

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
					Corporation
10/269,439	6762618	United States	Innovative verify scheme for two level GRP fuse in programmable bus switching family	Issued	Lattice Semiconductor Corporation
10/272,582	6901572	United States	Power Sequence Controller Programming Technique	Issued	Lattice Semiconductor Corporation
10/278,415	6639449	United States	Asynchronous glitch-free clock multiplexer	Issued	Lattice Semiconductor Corporation
10/282,524	7051261	United States	Turbo Encoder With Reduced Processing Delay	Issued	Lattice Semiconductor Corporation
10/283,765	6700823	United States	Programmable common mode termination for differential input/output circuits	Issued	Lattice Semiconductor Corporation
10/288,667	7000210	United States	Adaptive Adjustment Of Constraints During PLD Placement Processing	Issued	Lattice Semiconductor Corporation
10/288,668	6813754	United States	Placement Processing For Programmable Logic Devices	Issued	Lattice Semiconductor Corporation
10/300,190	6825733	United States	Low Jitter Integrated Phase Locked Loop With Broad Tuning Range	Issued	Lattice Semiconductor Corporation
10/302,439	6797568	United States	Flash Technology Transistors and Method For Forming Same	Issued	Lattice Semiconductor Corporation
10/308,420	6710641	United States	Low Voltage Bandgap Reference Circuit	Issued	Lattice Semiconductor Corporation
10/309,302	6650188	United States	Improved Coupling For LC-Based VCO	Issued	Lattice Semiconductor Corporation
10/334,642	6777979	United States	FIFO memory architecture	Issued	Lattice Semiconductor Corporation
10/338,619	6753696	United States	Programmable optimized-distribution logic allocator for	Issued	Lattice Semiconductor

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			a high-density complex PLD		Corporation
10/365,083	7034596	United States	Adaptive input logic for phase adjustments	Issued	Lattice Semiconductor Corporation
10/368,023	6915323	United States	Macrocells Supporting A Carry Cascade	Issued	Lattice Semiconductor Corporation
10/366,956	6788101	United States	Programmable input buffer for differential and single-ended signals	Issued	Lattice Semiconductor Corporation
10/367,323	6812869	United States	Noise Reduction Techniques For Programmable I/O Circuits	Issued	Lattice Semiconductor Corporation
10/370,232	6861870	United States	Dynamic Cross point Switch With Shadow Memory Architecture	Issued	Lattice Semiconductor Corporation
10/377,320	6859066	United States	Bank based input/output buffers in field programmable gate arrays with multiple reference voltages	Issued	Lattice Semiconductor Corporation
10/387,814	7305047	United States	Automatic lane assignment for Receiver	Issued	Lattice Semiconductor Corporation
10/387,243	7339952	United States	Pointer Processing For Optical Communication Systems	Issued	Lattice Semiconductor Corporation
10/391,094	6870395	United States	PLDs With Integrated Standard Cell Logic Blocks	Issued	Lattice Semiconductor Corporation
10/392,751	RE39510	United States	FPGA integrated circuit having embedded SRAM memory blocks with registered address and data input sections	Issued	Lattice Semiconductor Corporation
10/397,669	6967500	United States	Electronic Circuit With OnChip Programmable Terminations	Issued	Lattice Semiconductor Corporation
10/400,705	6873187	United States	Method and Apparatus for Controlling Signal Distribution In An Electronic	Issued	Lattice Semiconductor Corporation

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			Circuit		
10/406,050	7000212	United States	Hierarchical General Interconnect Architecture For High Density FPGA's	Issued	Lattice Semiconductor Corporation
10/409,543	6986004	United States	FIFO memory with programmable data port widths	Issued	Lattice Semiconductor Corporation
10/417,290	6879184	United States	Programmable logic device architecture based on arrays of LUT-based Boolean terms	Issued	Lattice Semiconductor Corporation
10/425,863	6903575	United States	Scalable device architecture for high-speed interfaces	Issued	Lattice Semiconductor Corporation
10/425,862	6894530	United States	Programmable And Fixed Logic Circuitry For High-Speed Interfaces	Issued	Lattice Semiconductor Corporation
10/428,889	6879182	United States	CPLD with multi-function blocks and distributed memory	Issued	Lattice Semiconductor Corporation
10/428,885	6861871	United States	Cascaded logic block architecture for complex programmable logic devices	Issued	Lattice Semiconductor Corporation
10/428,888	6864713	United States	Multi-Stage Interconnect Architecture For Complex Programmable Logic Devices	Issued	Lattice Semiconductor Corporation
10/428,982	6922078	United States	Enhanced wide and deep logic capability for high density, high performance CPLDs	Issued	Lattice Semiconductor Corporation
10/439,602	6828823	United States	Non-volatilie and reconfigurable PLDs	Issued	Lattice Semiconductor Corporation
10/441,814	7039842	United States	Measuring Propagation Delays of Programmable Logic Devices	Issued	Lattice Semiconductor Corporation
10/447,120	7301996	United States	skew cancellation for source synchronous clock and data signals	Issued	Lattice Semiconductor Corporation
10/447,451	7009433	United States	Digitally Controlled Delay Cells	Issued	Lattice Semiconductor

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
					Corporation
10/457,630	7304863	United States	Integrated Circuit Including External Electronic Components With Low Insertion Loss	Issued	Lattice Semiconductor Corporation
10/459,091	6879598	United States	Flexible Media Access Control Architecture	Issued	Lattice Semiconductor Corporation
10/460,385	6856171	United States	Synchronization of programmable multiplexers and demultiplexers	Issued	Lattice Semiconductor Corporation
10/463,781	6861868	United States	High Speed Interface For A Programmable Interconnect Circuit	Issued	Lattice Semiconductor Corporation
10/464,083	6882555	United States	Bi-directional buffering for memory data lines	Issued	Lattice Semiconductor Corporation
10/600,042	6822477	United States	Integrated Circuit And Associated Design Method Using Spare Gates	Issued	Lattice Semiconductor Corporation
10/610,253	6977408	United States	High-Performance Non-volatile Memory Device and Fabrication Process	Issued	Lattice Semiconductor Corporation
10/613,460	7132903	United States	Noise-shielding, switch-controlled load circuitry for oscillators and the like	Issued	Lattice Semiconductor Corporation
10/613,462	6952115	United States	Programmable I/O Interfaces For FPGAs And Other PLDs	Issued	Lattice Semiconductor Corporation
10/617,980	6958625	United States	PLD With Hardwired Microsequencer	Issued	Lattice Semiconductor Corporation
10/619,711	6903573	United States	Programmable Logic Device With Enhanced Wide Input Product Term Cascading	Issued	Lattice Semiconductor Corporation
10/620,286	6919736	United States	FPGA having partitionable embedded memory with configurable depth and width	Issued	Lattice Semiconductor Corporation
10/619,645	7098685	United States	Scalable Serializer-Deserializer Architecture and	Issued	Lattice Semiconductor

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			Programmable Interface		Corporation
10/620,147	7032203	United States	Algorithm to increase logic input width by cascading product terms	Issued	Lattice Semiconductor Corporation
10/624,965	6940309	United States	Programmable Logic Device With A Memory-Based Finite State Machine	Issued	Lattice Semiconductor Corporation
10/626,089	6737702	United States	Zero Power Memory Cell with Reduced Threshold Voltage	Issued	Lattice Semiconductor Corporation
10/628,656	6970047	United States	Programmable lock detector and corrector	Issued	Lattice Semiconductor Corporation
10/628,657	6924659	United States	Programmable Signal Termination for FPGAs and the Like	Issued	Lattice Semiconductor Corporation
10/629,223	7019577	United States	Clock Generator	Issued	Lattice Semiconductor Corporation
10/629,512	6903574	United States	Memory Access Via Serial Memory Interface	Issued	Lattice Semiconductor Corporation
10/629,221	6885227	United States	Clock Generator With Skew Control	Issued	Lattice Semiconductor Corporation
10/640,804	6877667	United States	Integrated Circuit And Associated Design Method With Antenna Error Control Using Spare Gates	Issued	Lattice Semiconductor Corporation
10/640,828	6838904	United States	Enhanced CPLD Macrocell Module Having Selectable Bypass of Steering-Based Resource Allocation	Issued	Lattice Semiconductor Corporation
10/641,260	6940779	United States	Programmable broadcasting initialization of embedded memory blocks on FPGA	Issued	Lattice Semiconductor Corporation
10/642,370	6924664	United States	FPGA	Issued	Lattice Semiconductor Corporation

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
10/655,686	6842037	United States	Shared Transmission Line Communication System and Method	Issued	Lattice Semiconductor Corporation
10/660,814	7038490	United States	Delay matched ASIC conversion of a PLD	Issued	Lattice Semiconductor Corporation
10/665,920	6970022	United States	Controlled hysteresis comparator with rail-to-rail input	Issued	Lattice Semiconductor Corporation
10/671,378	6943583	United States	Programmable I/O structure for FPGAs and the like having reduced pad capacitance	Issued	Lattice Semiconductor Corporation
10/671,363	6943582	United States	Programmable I/O structure for FPGAs and the Like Having Shared Circuitry	Issued	Lattice Semiconductor Corporation
10/671,756	6909663	United States	Multiport Memory With Twisted Bitlines	Issued	Lattice Semiconductor Corporation
10/676,536	7269771	United States	Semiconductor Device Adapted For Forming Multiple Scan Chains	Issued	Lattice Semiconductor Corporation
10/687,468	6809674	United States	Analog-to-digital converters	Issued	Lattice Semiconductor Corporation
10/699,321	7067883	United States	Lateral High-Voltage Junction Device	Issued	Lattice Semiconductor Corporation
10/701,005	7091763	United States	Clock generation	Issued	Lattice Semiconductor Corporation
10/704,025	7088134	United States	PLD With Flexible Memory Allocation And Routing	Issued	Lattice Semiconductor Corporation
10/726,972	7100058	United States	Programmable Power Management System And Method	Issued	Lattice Semiconductor Corporation
10/728,685	7187157	United States	Power supply remote voltage sensing	Issued	Lattice Semiconductor Corporation

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
10/737,514	6981381	United States	Linear Thermoelectric Device Driver	Issued	Lattice Semiconductor Corporation
10/744,353	7132864	United States	Method for configuring multiple-output phase-locked loop frequency synthesizer	Issued	Lattice Semiconductor Corporation
10/769,174	7024646	United States	Electrostatic Discharge Simulation	Issued	Lattice Semiconductor Corporation
10/768,643	7019584	United States	Output Stages For High Current Low Noise Bandgap Reference Circuit Implementations	Issued	Lattice Semiconductor Corporation
10/782,564	6972986	United States	Combination FPGA	Issued	Lattice Semiconductor Corporation
10/783,886	7081771	United States	Upgradeable And Reconfigurable Programmable Logic Device	Issued	Lattice Semiconductor Corporation
10/791,073	7191388	United States	Fast diagonal interleaved parity (DIP) calculator	Issued	Lattice Semiconductor Corporation
10/794,079	7257727	United States	Timer Systems and Methods	Issued	Lattice Semiconductor Corporation
10/794,524	7017063	United States	systems and methods for controlling voltage regulator module power supplies	Issued	Lattice Semiconductor Corporation
10/794,498	7028201	United States	Powering up a device having digital and analog circuitry	Issued	Lattice Semiconductor Corporation
10/797,759	7068556	United States	Sense Amplifier Systems and Methods	Issued	Lattice Semiconductor Corporation
10/809,180	7234030	United States	Table based scheduler for FIFOs and the like	Issued	Lattice Semiconductor Corporation
10/809,658	7095247	United States	Configuring FPGAs and the like using one or more serial memory devices	Issued	Lattice Semiconductor Corporation

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
10/815,403	7167032	United States	Self-adjusting schmitt trigger	Issued	Lattice Semiconductor Corporation
10/817,215	7081781	United States	Charge pump for a low-voltage wide-tuning range phase-locked loop	Issued	Lattice Semiconductor Corporation
10/829,865	6998896	United States	Dynamic gain adjustment systems and method for metastability resistance	Issued	Lattice Semiconductor Corporation
10/834,528	6998906	United States	Low pass filter systems and methods	Issued	Lattice Semiconductor Corporation
10/837,086	7307319	United States	High Voltage Protection Device And Process	Issued	Lattice Semiconductor Corporation
10/842,345	7002418	United States	Control Signal Generation ...	Issued	Lattice Semiconductor Corporation
10/841,987	7224213	United States	switched-capacitor ripple-smoothing filter	Issued	Lattice Semiconductor Corporation
10/843,708	7061269	United States	IO buffer architecture for programmable devices	Issued	Lattice Semiconductor Corporation
10/856,100	7196551	United States	Current Mode Logic Buffer	Issued	Lattice Semiconductor Corporation
10/857,667	7064973	United States	Combination FPGA	Issued	Lattice Semiconductor Corporation
10/885,419	7116585	United States	Memory Systems And Methods	Issued	Lattice Semiconductor Corporation
10/910,091	7215591	United States	Byte enable logic for memory	Issued	Lattice Semiconductor Corporation
10/912,943	7471752	United States	Data Transmission Synchronization	Issued	Lattice Semiconductor Corporation

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
10/928,563	7078286	United States	Process for fabricating a semiconductor device having electrically isolated low voltage and high voltage regions	Issued	Lattice Semiconductor Corporation
10/929,199	7484144	United States	Testing embedded memory in an integrated circuit	Issued	Lattice Semiconductor Corporation
10/944,978	7135886	United States	FPGA Using Both Volatile and NonVolatile Memory Cell Properties	Issued	Lattice Semiconductor Corporation
10/974,453	7307912	United States	Variable data width memory systems and methods	Issued	Lattice Semiconductor Corporation
10/973,750	7149129	United States	memory output data systems and methods with feedback	Issued	Lattice Semiconductor Corporation
10/974,107	7164290	United States	FPGA Logic Unit	Issued	Lattice Semiconductor Corporation
10/974,305	7129749	United States	PLD Having A Configurable DRAM With Transparent Refresh	Issued	Lattice Semiconductor Corporation
10/978,899	7376872	United States	Testing embedded memory in integrated circuits such as progammable logic circuits	Issued	Lattice Semiconductor Corporation
10/996,283	7161862	United States	Low power asynchronous sense amp	Issued	Lattice Semiconductor Corporation
11/007,954	7230810	United States	Dynamic over-voltage protection scheme for integrated circuit devices	Issued	Lattice Semiconductor Corporation
11/012,550	7215149	United States	Interface circuitry for electrical systems	Issued	Lattice Semiconductor Corporation
11/012,548	7215148	United States	Programmable current LVDS output buffer	Issued	Lattice Semiconductor Corporation
11/015,265	7177221	United States	Method of initializing configurable multi-port	Issued	Lattice Semiconductor

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			embedded memory blocks in an FPGA		Corporation
11/016,665	7187203	United States	Cascadable memory	Issued	Lattice Semiconductor Corporation
11/015,369	7177207	United States	Sense amplifier timing	Issued	Lattice Semiconductor Corporation
11/036,630	7257750	United States	Self-verification of configuration memory in PLDs	Issued	Lattice Semiconductor Corporation
11/036,738	7242053	United States	EEPROM Device with voltage-limiting charge pump circuit	Issued	Lattice Semiconductor Corporation
11/040,772	7208975	United States	Serdes with programmable I/O architecture	Issued	Lattice Semiconductor Corporation
11/041,319	7183798	United States	Synchronous memory	Issued	Lattice Semiconductor Corporation
11/044,089	7109754	United States	Synchronization of programmable multiplexers and demultiplexers	Issued	Lattice Semiconductor Corporation
11/044,149	7109756	United States	Synchronization of programmable multiplexers and demultiplexers	Issued	Lattice Semiconductor Corporation
11/044,508	7034599	United States	Clock Generator With Skew Control	Issued	Lattice Semiconductor Corporation
11/054,011	7221607	United States	Mult-port memory systems and methods for bit line coupling	Issued	Lattice Semiconductor Corporation
11/055,280	6975137	United States	PLDs With Integrated Standard Cell Logic Blocks	Issued	Lattice Semiconductor Corporation
11/054,750	7382293	United States	Data Decompression	Issued	Lattice Semiconductor Corporation
11/054,855	7589648	United States	Data Decompression	Issued	Lattice Semiconductor

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
					Corporation
11/064,477	7532646	United States	Distributed multiple channel alignment scheme	Issued	Lattice Semiconductor Corporation
11/071,356	7245154	United States	Differential Input Receiver with Programmable Failsafe	Issued	Lattice Semiconductor Corporation
11/070,926	7057397	United States	Output Impedance Measurement Techniques	Issued	Lattice Semiconductor Corporation
11/083,625	7376204	United States	Detection of Unknown symbol rate in a digitally modulated signal	Issued	Lattice Semiconductor Corporation
11/098,713	7265578	United States	In-System Programming Of a Non-Compliant Device Using Multiple Interfaces Of A PLD	Issued	Lattice Semiconductor Corporation
11/100,718	7397274	United States	In-System Programming Of a Non-Compliant Device Using Multiple Interfaces Of A PLD	Issued	Lattice Semiconductor Corporation
11/108,927	7193436	United States	Fast Processing Path Using FPGA Logic Units	Issued	Lattice Semiconductor Corporation
11/109,301	7630464	United States	Analog-to-digital systems and methods	Issued	Lattice Semiconductor Corporation
11/109,966	6977521	United States	FPGA	Issued	Lattice Semiconductor Corporation
11/121,326	7400171	United States	Electronic Switch Having Extended Voltage Range	Issued	Lattice Semiconductor Corporation
11/134,152	7009423	United States	Programmable I/O Interfaces For FPGAs And Other PLDs	Issued	Lattice Semiconductor Corporation
11/157,345	7685483	United States	Design-For-Test features for a memory in an FPGA	Issued	Lattice Semiconductor Corporation
11/157,349	7378879	United States	Decoding systems and methods	Issued	Lattice Semiconductor

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
					Corporation
11/165,709	7256613	United States	Programmable Interconnect Architecture for PLDs	Issued	Lattice Semiconductor Corporation
11/165,853	7342838	United States	PLD With A Double Data Rate SDRAM Interface	Issued	Lattice Semiconductor Corporation
11/185,242	7519139	United States	Signal monitoring systems and methods	Issued	Lattice Semiconductor Corporation
11/187,179	7342846	United States	address decoding systems and methods	Issued	Lattice Semiconductor Corporation
11/187,114	7253674	United States	Fine output clock phase alignment circuitry	Issued	Lattice Semiconductor Corporation
11/189,067	7505752	United States	Receiver used for differential signaling and reference voltage signaling with programmable common mode	Issued	Lattice Semiconductor Corporation
11/194,871	7414913	United States	Bitline twisting scheme for a multiport memory	Issued	Lattice Semiconductor Corporation
11/194,356	7262630	United States	Dynamic programmable termination for parallel and differential schemes	Issued	Lattice Semiconductor Corporation
11/199,287	7599457	United States	clock-and-data-recovery system having a multi-phase clock generator for one or more channel circuits	Issued	Lattice Semiconductor Corporation
11/200,983	7295035	United States	Programmable Logic Device With Enhanced Logic Block Architecture	Issued	Lattice Semiconductor Corporation
11/200,941	7411419	United States	I/O Systems and Methods	Issued	Lattice Semiconductor Corporation
11/202,149	7606851	United States	Correlator having user-defined processing	Issued	Lattice Semiconductor Corporation

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
11/201,620	7187586	United States	Flash memory erase verification systems and methods	Issued	Lattice Semiconductor Corporation
11/206,282	RE40311	United States	Zero Power Programmable Memory Cell	Issued	Lattice Semiconductor Corporation
11/226,695	7301182	United States	Circuit layout for improved performance while preserving or improving density	Issued	Lattice Semiconductor Corporation
11/230,087	7167405	United States	Data transfer verification systems and methods	Issued	Lattice Semiconductor Corporation
11/235,616	7376037	United States	PLD with power-saving architecture	Issued	Lattice Semiconductor Corporation
11/236,967	7405446	United States	Electrostatic Protection Systems and Methods	Issued	Lattice Semiconductor Corporation
11/243,255	7088132	United States	Configuring FPGAs and the like using one or more serial memory devices	Issued	Lattice Semiconductor Corporation
11/251,682	7196963	United States	Address isolation for user-defined configuration memory in programmable devices	Issued	Lattice Semiconductor Corporation
11/252,094	7263024	United States	Clock reset address decoder for block memory	Issued	Lattice Semiconductor Corporation
11/252,126	7061275	United States	FPGA	Issued	Lattice Semiconductor Corporation
11/257,137	7685215	United States	Fast-carry arithmetic circuit using a multi-input LUT	Issued	Lattice Semiconductor Corporation
11/257,641	7317343	United States	PULSE-GENERATION CIRCUIT HAVING PULSE GENERATORS AND SET-RESET LATCHES	Issued	Lattice Semiconductor Corporation
11/260,097	7212051	United States	Control signal generation for a low jitter switched-capacitor frequency synthesizer	Issued	Lattice Semiconductor Corporation

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
11/281,651	7495495	United States	Digital I/O Timing Control	Issued	Lattice Semiconductor Corporation
11/287,720	7327159	United States	Interface Block Architectures	Issued	Lattice Semiconductor Corporation
11/290,205	7242634	United States	Pseudo-dynamic word-line driver	Issued	Lattice Semiconductor Corporation
11/293,941	7538574	United States	Transparent Field Reconfiguration for PLDs	Issued	Lattice Semiconductor Corporation
11/302,097	7620839	United States	Jitter Tolerant Delay-Locked Loop Circuit	Issued	Lattice Semiconductor Corporation
11/300,886	7495467	United States	Temperature independent, linear on-chip termination resistance	Issued	Lattice Semiconductor Corporation
11/332,986	7382169	United States	Systems and Methods for Reducing Static Phase Error	Issued	Lattice Semiconductor Corporation
11/335,890	7439783	United States	Phase-Locked Loop Systems And Methods	Issued	Lattice Semiconductor Corporation
11/345,713	7547995	United States	dynamic over voltage protection scheme for interface circuitry	Issued	Lattice Semiconductor Corporation
11/346,817	7554357	United States	Efficient Configuration of Daisy-Chained Programmable Logic Devices	Issued	Lattice Semiconductor Corporation
11/350,436	7375549	United States	Reconfiguration of PLDs	Issued	Lattice Semiconductor Corporation
11/356,805	7277348	United States	Memory Cell Comprising And OTP NV Memory Unit And SRAM Unit	Issued	Lattice Semiconductor Corporation
11/360,337	7355441	United States	PLD with distributed memory and non-volatile memory	Issued	Lattice Semiconductor Corporation

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
11/361,584	7596744	United States	Auto recovery from volatile soft error upsets (SEUs)	Issued	Lattice Semiconductor Corporation
11/362,289	7759926	United States	dynamic phase offset measurement	Issued	Lattice Semiconductor Corporation
11/361,643	7446573	United States	Comparator Systems And Methods	Issued	Lattice Semiconductor Corporation
11/398,437	7459931	United States	PLDs with transparent field reconfiguration	Issued	Lattice Semiconductor Corporation
11/397,985	7554358	United States	PLDs with user non-volatile memory	Issued	Lattice Semiconductor Corporation
11/416,881	7623378	United States	Selective programming of non-volatile memory facilitated by security fuses	Issued	Lattice Semiconductor Corporation
11/435,956	7102934	United States	Sense Amplifier Systems and Methods	Issued	Lattice Semiconductor Corporation
11/442,186	7411417	United States	Selective loading of configuration data into configuration memory cells	Issued	Lattice Semiconductor Corporation
11/446,548	7378873	United States	PLD providing a serial peripheral interface	Issued	Lattice Semiconductor Corporation
11/445,620	7378872	United States	PLD architecture with multiple slice types	Issued	Lattice Semiconductor Corporation
11/446,542	7385417	United States	Dual slice architectures for PLDs	Issued	Lattice Semiconductor Corporation
11/446,351	7397276	United States	Logic block control architectures for PLDs	Issued	Lattice Semiconductor Corporation
11/446,308	7546498	United States	PLDs with custom identification systems and methods	Issued	Lattice Semiconductor Corporation

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
11/446,309	7495970	United States	Flexible memory architectures for PLDs	Issued	Lattice Semiconductor Corporation
11/447,591	7631223	United States	PLD methods and systems for providing multi-boot configuration data support	Issued	Lattice Semiconductor Corporation
11/452,714	7463060	United States	PLD and method of testing	Issued	Lattice Semiconductor Corporation
11/455,315	7215139	United States	Upgradeable And Reconfigurable Programmable Logic Device	Issued	Lattice Semiconductor Corporation
11/425,273	7702100	United States	Key generation for advanced encryption standard (AES) decryption and the like	Issued	Lattice Semiconductor Corporation
11/425,881	7657773	United States	Clock distribution chip for generating both zero-delay and non-zero-delay clock signals	Issued	Lattice Semiconductor Corporation
11/477,759	7348914	United States	Methods and systems to align output signals of an analog-to-digital converter	Issued	Lattice Semiconductor Corporation
11/487,647	7636259	United States	Flash memory array with independently erasable sectors	Issued	Lattice Semiconductor Corporation
11/487,751	7512015	United States	Negative voltage blocking for embedded memories	Issued	Lattice Semiconductor Corporation
11/492,687	7466190	United States	Charge pump with four-well transistors	Issued	Lattice Semiconductor Corporation
11/494,862	7521969	United States	Switch sequencing circuit systems and methods	Issued	Lattice Semiconductor Corporation
11/461,222	7411432	United States	Integrated circuits and complementary CMOS circuits for frequency dividers	Issued	Lattice Semiconductor Corporation
11/498,645	7675313	United States	Methods and systems for storing a security key using programmable fuses	Issued	Lattice Semiconductor Corporation

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
11/498,646	7605606	United States	Area efficient routing architectures for PLDs	Issued	Lattice Semiconductor Corporation
11/530,620	7456672	United States	Clock systems and methods	Issued	Lattice Semiconductor Corporation
11/533,188	7511641	United States	Efficient bitstream compression	Issued	Lattice Semiconductor Corporation
11/551,459	7831754	United States	Multiple Communication Channel Configuration Systems And Methods	Issued	Lattice Semiconductor Corporation
11/556,528	7663401	United States	Multiplexer initialization systems and methods	Issued	Lattice Semiconductor Corporation
11/593,274	7535258	United States	Programmable Voltage LVDS Output Buffer	Issued	Lattice Semiconductor Corporation
11/557,808	7725803	United States	PLD programming verification systems and methods	Issued	Lattice Semiconductor Corporation
11/638,156	7429875	United States	Low Static Current Drain Logic Circuit	Issued	Lattice Semiconductor Corporation
11/643,288	7443192	United States	Output buffer with digital slew control	Issued	Lattice Semiconductor Corporation
11/624,021	7623391	United States	Data transfer verification systems and methods	Issued	Lattice Semiconductor Corporation
11/671,948	7576563	United States	Flexible High Fan-out Signal Routing Systems and Methods	Issued	Lattice Semiconductor Corporation
11/675,246	7313025	United States	Flash memory erase verification systems and methods	Issued	Lattice Semiconductor Corporation
11/676,071	7430706	United States	Fast diagonal interleaved parity (DIP) calculator	Issued	Lattice Semiconductor Corporation

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
11/680,526	7598765	United States	Redundancy for Configuration RAM	Issued	Lattice Semiconductor Corporation
11/691,003	7536615	United States	Logic analyzer systems and methods for PLDs	Issued	Lattice Semiconductor Corporation
11/691,040	7743296	United States	Logic analyzer systems and methods for PLDs	Issued	Lattice Semiconductor Corporation
11/737,702	7509598	United States	Clock Boosting Systems and Methods	Issued	Lattice Semiconductor Corporation
11/750,790	7401280	United States	Self-verification of configuration memory in PLDs	Issued	Lattice Semiconductor Corporation
11/750,616	7632011	United States	Integrated Circuit Temperature Sensors Systems and Methods	Issued	Lattice Semiconductor Corporation
11/760,411	8065574	United States	Real Soft Error Detect Scheme for Testing	Issued	Lattice Semiconductor Corporation
11/761,221	7570078	United States	PLD Providing A Serial Peripheral Interfaces	Issued	Lattice Semiconductor Corporation
11/778,457	7573770	United States	Distributed front-end FIFO for source-synchronized interfaces with non-continuous clocks	Issued	Lattice Semiconductor Corporation
11/779,246	7446679	United States	FPGA data compression using combined RLE BE, LZ, Row LZ and BE ROW encoding	Issued	Lattice Semiconductor Corporation
11/863,016	7681160	United States	Weight based look up table collapsing for programmable logic devices	Issued	Lattice Semiconductor Corporation
11/865,556	7539076	United States	Variable data width memory systems and methods	Issued	Lattice Semiconductor Corporation
11/869,019	7616029	United States	Hysteresis-based processing for applications such as signal bias monitors	Issued	Lattice Semiconductor Corporation

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
11/872,950	7586344	United States	Dynamic delay or advance adjustment of oscillating signal phase	Issued	Lattice Semiconductor Corporation
11/875,748	7757198	United States	Scan chain systems and methods for PLDs	Issued	Lattice Semiconductor Corporation
11/877,434	7411414	United States	Single-Ended Output Driver Buffer	Issued	Lattice Semiconductor Corporation
11/924,088	8132040	United States	Channel-to-channel deskew systems and methods	Issued	Lattice Semiconductor Corporation
11/934,711	7573291	United States	Programmable Logic Device With Enhanced Logic Block Architecture	Issued	Lattice Semiconductor Corporation
11/937,328	7788620	United States	An IO placement systems and methods to reduce SSO noise	Issued	Lattice Semiconductor Corporation
11/937,300	7895555	United States	Simultaneous Switching Output Noise Estimation and Reduction Systems and Methods	Issued	Lattice Semiconductor Corporation
11/939,787	7863931	United States	Flexible Delay Cell Architecture	Issued	Lattice Semiconductor Corporation
11/941,031	7902865	United States	Compression and decompression of configuration data using repeated data frames	Issued	Lattice Semiconductor Corporation
11/941,006	7535253	United States	Method of Retaining Register Data during Field Update of PLD	Issued	Lattice Semiconductor Corporation
11/947,662	7788623	United States	Composite wire indexing for PLDs	Issued	Lattice Semiconductor Corporation
11/949,130	7586325	United States	IC having independent voltage and process/temperature control	Issued	Lattice Semiconductor Corporation
12/001,600	7728625	United States	Serial interface for PLDs	Issued	Lattice Semiconductor

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
					Corporation
11/957,598	7605609	United States	A programmable level shifter optimized for high performance and low power.	Issued	Lattice Semiconductor Corporation
11/959,329	7630259	United States	PLD with built in self test	Issued	Lattice Semiconductor Corporation
11/970,212	7646643	United States	Process charging monitor for nonvolatile memory	Issued	Lattice Semiconductor Corporation
12/019,526	7787326	United States	PLD With Mult-Rate SDRAM Interface	Issued	Lattice Semiconductor Corporation
12/021,202	8069329	United States	Dynamic Multiple Pattern Configuration Scheme For Volatile FPGAs	Issued	Lattice Semiconductor Corporation
12/044,842	7652500	United States	Reconfiguration of PLDs	Issued	Lattice Semiconductor Corporation
12/055,170	7890913	United States	Wire Mapping For PLDs	Issued	Lattice Semiconductor Corporation
12/060,776	7459935	United States	PLD With Distributed Memory	Issued	Lattice Semiconductor Corporation
12/061,885	7831856	United States	Detection of Timing Errors in Programmable Logic Devices	Issued	Lattice Semiconductor Corporation
12/099,933	7661878	United States	On-Chip Temperature Sensor For An Integrated Circuit	Issued	Lattice Semiconductor Corporation
12/100,859	7558143	United States	Programmable Logic Device With Power-Saving Architecture	Issued	Lattice Semiconductor Corporation
12/105,146	7557606	United States	Synchronization Of Data Signals And Clock Signals For Programmable Logic Devices	Issued	Lattice Semiconductor Corporation
12/105,959	7696784	United States	PLD With Multiple Slice	Issued	Lattice Semiconductor

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			Types		Corporation
12/107,883	7560953	United States	Power Management Systems And Methods for PLDs	Issued	Lattice Semiconductor Corporation
12/122,489	7897448	United States	Formation Of High Voltage Transistor With High Breakdown Voltage	Issued	Lattice Semiconductor Corporation
12/146,042	8463832	United States	Digital Signal Processing Block Architecture For PLD	Issued	Lattice Semiconductor Corporation
12/164,265	7592834	United States	Logic Block Control Architectures For PLDs	Issued	Lattice Semiconductor Corporation
12/182,940	8261160	United States	Serial data recovery out of 8 samples with FPGAs	Issued	Lattice Semiconductor Corporation
12/186,027	7579865	United States	Selective Loading Of Configuration Data Into Configuration Memory Cells	Issued	Lattice Semiconductor Corporation
12/188,120	7605602	United States	Low-Power Output Driver Buffer Circuit	Issued	Lattice Semiconductor Corporation
12/238,959	7911229	United States	Programmable Signal Routing Systems	Issued	Lattice Semiconductor Corporation
12/273,868	7663419	United States	Clock Systems And Methods	Issued	Lattice Semiconductor Corporation
12/277,217	8112731	United States	Congestion-driven placement based on region interconnection for FPGA	Issued	Lattice Semiconductor Corporation
12/323,974	7992120	United States	congestion estimation based on pass probability net estimation process	Issued	Lattice Semiconductor Corporation
12/327,128	7656193	United States	Programmable Logic Device And Method Of Testing	Issued	Lattice Semiconductor Corporation
12/337,502	8856718	United States	Precise Congestion Estimation for FPGA Router	Issued	Lattice Semiconductor

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
					Corporation
12/341,929	8181139	United States	Multi-Priority Placement	Issued	Lattice Semiconductor Corporation
12/370,039	7714608	United States	Temperature-Independent, Linear On-Chip Termination Resistance	Issued	Lattice Semiconductor Corporation
12/389,149	7957208	United States	Flexible memory architectures for PLDs	Issued	Lattice Semiconductor Corporation
12/402,751	7844243	United States	Receiver used for differential signaling and reference voltage signaling with programmable common mode	Issued	Lattice Semiconductor Corporation
12/406,772	8069431	United States	An alternative method for pin swapping in FPGA routing	Issued	Lattice Semiconductor Corporation
12/408,047	8086986	United States	Clock Boosting Systems And Methods	Issued	Lattice Semiconductor Corporation
12/409,757	7675321	United States	Dual-Slice Architectures For PLDs	Issued	Lattice Semiconductor Corporation
12/413,787	7808405	United States	Efficient Bitstream Compression	Issued	Lattice Semiconductor Corporation
12/430,848	7741865	United States	Soft Error Upset Hardened Integrated Circuit Systems And Methods	Issued	Lattice Semiconductor Corporation
12/464,822	7876125	United States	Method of Retaining Register Data during Field Update of PLD	Issued	Lattice Semiconductor Corporation
12/465,444	7868654	United States	Economical way to improve volatile FPGA boot up data throughput by utilizing one or more SPI boot PROMs w/o sacrificing additional FPGA pins	Issued	Lattice Semiconductor Corporation
12/467,800	7737723	United States	Transparent Field Reconfiguration for PLDs	Issued	Lattice Semiconductor

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
					Corporation
12/476,155	8044682	United States	FPGA Having Low Power, Fast Carry Chain	Issued	Lattice Semiconductor Corporation
12/480,565	7702977	United States	PLDs with custom identification systems and methods	Issued	Lattice Semiconductor Corporation
12/494,822	8165164	United States	Circuit For In-System Reconfigurable Mapping Of IQ Data Into A CPRI Basic Frame	Issued	Lattice Semiconductor Corporation
12/502,141	7724029	United States	Power Management For Integrated Circuits Such As Programmable Logic Devices	Issued	Lattice Semiconductor Corporation
12/511,388	7768300	United States	PLD Providing A Serial Peripheral Interfaces	Issued	Lattice Semiconductor Corporation
12/512,944	8255733	United States	Method of selecting precise delay or skew shifts	Issued	Lattice Semiconductor Corporation
12/512,961	7969248	United States	VCO digital center frequency coarse tune algorithm	Issued	Lattice Semiconductor Corporation
12/538,810	7808855	United States	Distributed front-end FIFO for source-synchronized interfaces with non-continuous clocks	Issued	Lattice Semiconductor Corporation
12/561,140	8010871	United States	Auto recovery from volatile soft error upsets (SEUs)	Issued	Lattice Semiconductor Corporation
12/564,781	7746107	United States	Redundancy for Configuration RAM	Issued	Lattice Semiconductor Corporation
12/578,470	8122277	United States	Clock distribution chip	Issued	Lattice Semiconductor Corporation
12/578,492	8112656	United States	Clock distribution chip	Issued	Lattice Semiconductor Corporation

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
12/607,868	7989911	United States	STI with trench liner of increased thickness	Issued	Lattice Semiconductor Corporation
12/607,333	7985656	United States	STI with trench liner of increased thickness	Issued	Lattice Semiconductor Corporation
12/611,262	8059470	United States	Flash memory array with independently erasable sectors	Issued	Lattice Semiconductor Corporation
12/626,289	7944765	United States	PLD with built in self test	Issued	Lattice Semiconductor Corporation
12/630,163	8060784	United States	PLD And Methods For Providing Multi-Boot Configuration Data Support	Issued	Lattice Semiconductor Corporation
12/637,884	8200179	United States	Combined Variable Gain Amplifier And Linear Equalizer With Independent Gain And Frequency Control	Issued	Lattice Semiconductor Corporation
12/698,283	8040152	United States	IO Ring Configuration Scheme with sharing of BC7 register	Issued	Lattice Semiconductor Corporation
12/706,227	7924054	United States	Latency measurement circuit for wireless communications applications	Issued	Lattice Semiconductor Corporation
12/709,685	7834652	United States	Methods and systems for storing a security key using programmable fuses	Issued	Lattice Semiconductor Corporation
12/729,952	8040159	United States	High Speed Comparator with Data Dependent Jitter Mitigation	Issued	Lattice Semiconductor Corporation
12/752,455	8384427	United States	Serial Peripheral Interface Daisy Chaining using a Flow-Through Option	Issued	Lattice Semiconductor Corporation
12/757,087	8664774	United States	A Method for Arranging IC Bondwires for the Reduction of Crosstalk	Issued	Lattice Semiconductor Corporation
12/786,359	8108754	United States	PLD programming verification systems and methods	Issued	Lattice Semiconductor Corporation

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
12/813,540	8164499	United States	Shared-Array Multiple-Output Digital to Analog Converter	Issued	Lattice Semiconductor Corporation
12/813,573	8441292	United States	Method of delaying data from clock in 1UI steps	Issued	Lattice Semiconductor Corporation
12/818,544	7868646	United States	Soft Error Upset Hardened Integrated Circuit Systems And Methods	Issued	Lattice Semiconductor Corporation
12/871,764	8286116	United States	Composite Wire Indexing For PLDs	Issued	Lattice Semiconductor Corporation
12/977,011	8522126	United States	Method Of Blocking PLC Distributed SRAM Readback In User Mode	Issued	Lattice Semiconductor Corporation
12/976,412	8351287	United States	Bitline Floating Circuit For Power Reduction On SRAM Array	Issued	Lattice Semiconductor Corporation
12/976,520	8477549	United States	Strobed And Latched Readback Of SRAM Bits In A FPGA	Issued	Lattice Semiconductor Corporation
12/987,393	8274412	United States	Low Power SerDes With Built- In Word Alignment For Odd And Even Gearing Ratios	Issued	Lattice Semiconductor Corporation
13/006,622	8384428	United States	Programmable IO Pad - embedded function block	Issued	Lattice Semiconductor Corporation
13/007,804	8248136	United States	Low Power And Glitch-less Delay Element For High Speed Receiver Interface	Issued	Lattice Semiconductor Corporation
13/007,688	8324934	United States	Programmable Ratio Input Buffer	Issued	Lattice Semiconductor Corporation
13/026,555	8104009	United States	Wire Mapping For Programmable Logic Devices	Issued	Lattice Semiconductor Corporation
13/034,174	8058898	United States	Compression and Decompression Of Configuration Data Using	Issued	Lattice Semiconductor Corporation

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			Repeated Data Frames		
13/038,259	8368424	United States	Wakeup from sleep mode using slave I2C port or slave SPI port with powered down core logic	Issued	Lattice Semiconductor Corporation
13/038,270	8816718	United States	Slow Respond Mode Protocol For Synchronous Read	Issued	Lattice Semiconductor Corporation
13/037,703	8654600	United States	Current Sense Amplifier With Low Voltage Operation	Issued	Lattice Semiconductor Corporation
13/052,142	8553463	United States	Positive-To-Negative Voltage Discharge Circuit	Issued	Lattice Semiconductor Corporation
13/076,300	8319521	United States	Safe programming of key information into NV memory	Issued	Lattice Semiconductor Corporation
13/079,578	8314634	United States	Power Saving Standby Mode With Glitch-Less Output Controls	Issued	Lattice Semiconductor Corporation
13/079,595	8531222	United States	PLL Switchable Feedback Loops Among Internal And External Feedback Paths	Issued	Lattice Semiconductor Corporation
13/083,889	8138790	United States	Latency measurement circuit for wireless communications applications	Issued	Lattice Semiconductor Corporation
13/154,885	8441284	United States	Flexible Way To Incrementally Update Multi-Bit Data Registers	Issued	Lattice Semiconductor Corporation
13/155,547	8547075	United States	Filter And Stability Capacitor Reuse For On-Chip Dual Output Voltage Regulators	Issued	Lattice Semiconductor Corporation
13/164,108	8555217	United States	Cross-Probing Technology Between Software Plug-In Modules	Issued	Lattice Semiconductor Corporation
13/178,599	8539409	United States	Multiple silicon products from a common base set of masks	Issued	Lattice Semiconductor Corporation
13/178,536	8495264	United States	Packet And Control Symbol	Issued	Lattice Semiconductor

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			Alignment Circuit For SRIO		Corporation
13/193,984	8314632	United States	Placing ICs Into Ultra-Low Voltage Mode For Standby Purposes	Issued	Lattice Semiconductor Corporation
13/212,121	8451679	United States	Bit-Line Clamping Circuit To Improve Write Performance Of Dual-Port SRAM	Issued	Lattice Semiconductor Corporation
13/275,102	8169237	United States	High Speed Comparator with Data Dependent Jitter Mitigation	Issued	Lattice Semiconductor Corporation
13/299,507	8370691	United States	Testing of Soft Error Detection Logic For PLDs	Issued	Lattice Semiconductor Corporation
13/452,060	8823561	United States	In-System Reconfigurable Circuit For Mapping Data Words Of Different Lengths	Issued	Lattice Semiconductor Corporation
13/585,142	8461894	United States	Low Power And Glitch-less Delay Element For High Speed Receiver Interface	Issued	Lattice Semiconductor Corporation
13/616,173	8912933	United States	Low Power SerDes With Built- In Word Alignment For Odd And Even Gearing Ratios	Issued	Lattice Semiconductor Corporation
13/653,827	8710898	United States	Bandgap Reference Circuit Design With Triple-Trim Methodology For Mass Production	Issued	Lattice Semiconductor Corporation
13/680,947	8643398	United States	Placing ICs Into Low Voltage Mode For Standby Purposes	Issued	Lattice Semiconductor Corporation
13/685,385	8643168	United States	Input Capacitance Compensation In Package	Issued	Lattice Semiconductor Corporation
13/721,867	8686773	United States	In-System Margin Measurement Circuit	Issued	Lattice Semiconductor Corporation
13/738,265	8797064	United States	Low power, optimized H-bridge and CML driver	Issued	Lattice Semiconductor Corporation

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
13/764,221	RE45200	United States	Programmable Signal Routing Systems Having Low Static Leakage	Issued	Lattice Semiconductor Corporation
13/857,919	8786482	United States	Analog-To-Digital-Converter	Issued	Lattice Semiconductor Corporation
13/892,948	8648636	United States	Method of Delaying Data from Clock in 1UI steps	Issued	Lattice Semiconductor Corporation
14/040,955	8829944	United States	Dynamic Power Supply Switching For Clock Signals	Issued	Lattice Semiconductor Corporation
13/155,261		United States	JTAG Based Parallel Measuring And Trimming for Time Based Parameters	Pending	Lattice Semiconductor Corporation
13/412,408		United States	Double Rate Throughput Processing Booster For DSP Slices	Pending	Lattice Semiconductor Corporation
13/466,463		United States	Early Match FIFO	Pending	Lattice Semiconductor Corporation
13/681,782		United States	Multi-channel transmitter synchronization circuitry	Pending	Lattice Semiconductor Corporation
13/777,243		United States	RAM Data Path Sense Leakage Abatement Circuit	Pending	Lattice Semiconductor Corporation
13/858,422		United States	Method To Enable And Disable Scan Test Mode Reliably Through JTAG Port With Maximum Scan Coverage	Pending	Lattice Semiconductor Corporation
13/868,738		United States	Loss of signal detection in high-speed serial link	Pending	Lattice Semiconductor Corporation
13/901,853		United States	Dual-Port SRAM With Bit Line Clamping	Pending	Lattice Semiconductor Corporation
13/904,861		United States	Bring up sequence for configurable PCIe IP in an	Pending	Lattice Semiconductor

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			FPGA		Corporation
13/947,553		United States	Method For Hot Swapping Or Hot Plugging With Stable Supply-Side Reference Over Wide Voltage Range	Pending	Lattice Semiconductor Corporation
14/021,513		United States	Phase Locked Loop Circuit With Selectable Feedback Paths	Pending	Lattice Semiconductor Corporation
14/043,920		United States	Robust Serialized State-machine Interface Architecture Optimized for Implementation in Programmable Devices	Pending	Lattice Semiconductor Corporation
14/053,026		United States	ASB SW modeling methodology	Pending	Lattice Semiconductor Corporation
14/070,975		United States	Method to enable system board pin escape for tight ball pitch packages	Pending	Lattice Semiconductor Corporation
14/095,310		United States	A Novel ESD Implementation for 40nm FPGA	Pending	Lattice Semiconductor Corporation
14/136,482		United States	Automatic Quadrant Clock Assignment For Programmable Logic Devices	Pending	Lattice Semiconductor Corporation
14/137,443		United States	Using Critical Groups in FPGA Routing	Pending	Lattice Semiconductor Corporation
14/147,796		United States	A Hot Socket Implementation for General Purpose IO for 40nm FPGA	Pending	Lattice Semiconductor Corporation
14/172,678		United States	All Mosfet Circuit for Generating Accurate Collector Currents	Pending	Lattice Semiconductor Corporation
14/179,651		United States	LOW-VOLTAGE CURRENT SENSE AMPLIFIER	Pending	Lattice Semiconductor Corporation
14/194,484		United States	Logic Element Placement with Repacking Optimization	Pending	Lattice Semiconductor Corporation

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
14/220,377		United States	DPHY using FPGA differential & single ended I/Os	Pending	Lattice Semiconductor Corporation
14/223,096		United States	DPHY using FPGA differential & single ended I/Os	Pending	Lattice Semiconductor Corporation
14/245,920		United States	Deterministic Dynamic Element Matching for Generating Precise Current Ratios	Pending	Lattice Semiconductor Corporation
14/271,331		United States	Inline Defect To Sort Test Correlation In Semiconductor Manufacturing	Pending	Lattice Semiconductor Corporation
14/271,955		United States	Performance-focused Adaptive Automatic Incremental Flow	Pending	Lattice Semiconductor Corporation
14/283,329		United States	Configuration logic controlled memory BIST (built-in self-test) for back-to-back initialization and readback of embedded block RAMs in FPGAs	Pending	Lattice Semiconductor Corporation
14/308,747		United States	A novel Output Driver drive strength and termination resistor continuously calibrating PVT compensation scheme	Pending	Lattice Semiconductor Corporation
14/313,443		United States	FPGA Hardware debug during post-config power-up and before logic analyzer connect	Pending	Lattice Semiconductor Corporation
14/313,778		United States	IOLOGIC Delay Cell Stealing for Holdtime Correction	Pending	Lattice Semiconductor Corporation
14/316,049		United States	Mapping Constant Multipliers To ICE Devices	Pending	Lattice Semiconductor Corporation
14/319,481		United States	Incrementer Absorption into Multiplier Logic	Pending	Lattice Semiconductor Corporation
14/320,169		United States	Method to Implement Mixed-	Pending	Lattice

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			Width Mode Memory in Fixed-Mode Memory Architecture with Masking		Semiconductor Corporation
14/320,074		United States	Two Level Voltage Regulator scheme for SRAM Operation	Pending	Lattice Semiconductor Corporation
14/327,811		United States	Implementing Dual Boot For XO2 and Multiple ASCs	Pending	Lattice Semiconductor Corporation
14/339,164		United States	A unique method to optimize clock to out path	Pending	Lattice Semiconductor Corporation
14/339,229		United States	New method on bus-based clock_to_out timing optimization	Pending	Lattice Semiconductor Corporation
14/482,001		United States	Physically-aware Programmable Multiport Memory BIST with on-the-fly ATE-configurable memory tests	Pending	Lattice Semiconductor Corporation
14/509,564		United States	Dont-care based mux absorption into ice40 carry chain	Pending	Lattice Semiconductor Corporation
14/525,240		United States	Level shifter that eliminates static power dissipation	Pending	Lattice Semiconductor Corporation
14/535,454		United States	Low power and high performance class AB amplifier control common mode in SerDes Transmitter	Pending	Lattice Semiconductor Corporation
14/535,351		United States	ICO metastability prevention during start-up	Pending	Lattice Semiconductor Corporation
14/558,851		United States	Low Power and Flexible TX FFE With Programmable Tap Positions And Coefficients Driver Architecture	Pending	Lattice Semiconductor Corporation
14/576,348		United States	Reconfigurable and Scalable Hardware Management Architecture	Pending	Lattice Semiconductor Corporation

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
14/576,245		United States	Methodology that allows multiple hardware or hardware-software controllers with different bus interfaces to share a common resource	Pending	Lattice Semiconductor Corporation
14/604,515		United States	Enhancement of FPGA hardware debugger to be used as a design controller/exerciser with user registers	Pending	Lattice Semiconductor Corporation
14/609,181		United States	Algorithm to Optimize Hot Swapping	Pending	Lattice Semiconductor Corporation
14/610,074		United States	Ripple Mode using 3-LUT for Generate	Pending	Lattice Semiconductor Corporation
14/610,127		United States	Combine OFX with LUT output and SUM into a single output to reduce number of signals to routing block	Pending	Lattice Semiconductor Corporation
14/611,069		United States	High speed complementary NMOS LUT logic	Pending	Lattice Semiconductor Corporation
14/611,095		United States	Shared Logic for Multiple Registers with asynchronous initialization with preload	Pending	Lattice Semiconductor Corporation
11/949,454	7,427,874	United States	Interface block architectures	Issued	Lattice Semiconductor Corporation
11/676,196	7,327,160	United States	SERDES with programmable I/O architecture	Issued	Lattice Semiconductor Corporation
6,786,564	6,786,564	United States	Inkjet printer, drive method and drive device for same	Issued	Lattice Semiconductor Corporation
11/839,107	7,856,050	United States	Receiver and transmitter calibration to compensate for frequency dependent I/Q imbalance	Issued	Lattice Semiconductor Corporation
07/679,370	5,255,221	United States	Fully configurable versatile field programmable function	Issued	Lattice Semiconductor

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			element		Corporation
06/551,735	4,642,797	United States	High speed first-in-first-out memory	Issued	Lattice Semiconductor Corporation
08/042,533	5,394,037	United States	Sense amplifiers and sensing methods	Issued	Lattice Semiconductor Corporation
08/115,533	5,404,055	United States	Input routing pool	Issued	Lattice Semiconductor Corporation
08/115,723	5,394,033	United States	Structure and method for implementing hierarchical routing pools in a programmable logic circuit	Issued	Lattice Semiconductor Corporation
08/342,675	5,506,517	United States	Output enable structure and method for a programmable logic device	Issued	Lattice Semiconductor Corporation
07/911,841	5,357,156	United States	Active clamp circuit scheme for CMOS devices	Issued	Lattice Semiconductor Corporation
08/179,887	5,886,378	United States	Single polysilicon layer flash E.sup.2 PROM cell	Issued	Lattice Semiconductor Corporation
07/853,453	5,231,316	United States	Temperature compensated CMOS voltage to current converter	Issued	Lattice Semiconductor Corporation
08/108,363	5,353,246	United States	Programmable semiconductor antifuse structure and method of fabricating	Issued	Lattice Semiconductor Corporation
07/785,442	5,281,906	United States	Tunable voltage reference circuit to provide an output voltage with a predetermined temperature coefficient independent of variation in supply voltage	Issued	Lattice Semiconductor Corporation
07/696,453	5,251,169	United States	Non-volatile erasable and programmable interconnect cell	Issued	Lattice Semiconductor Corporation
07/538,211	5,255,203	United States	Interconnect structure for programmable logic device	Issued	Lattice Semiconductor

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
					Corporation
08/106,263	5,412,260	United States	Multiplexed control pins for in-system programming and boundary scan state machines in a high density programmable logic device	Issued	Lattice Semiconductor Corporation
08/033,934	5,418,390	United States	Single polysilicon layer E.sup.2 PROM cell	Issued	Lattice Semiconductor Corporation
07/993,711	5,452,229	United States	Programmable integrated-circuit switch	Issued	Lattice Semiconductor Corporation
07/957,311	5,329,179	United States	Arrangement for parallel programming of in-system programmable IC logical devices	Issued	Lattice Semiconductor Corporation
07/288,945	4,896,296	United States	Programmable logic device configurable input/output cell	Issued	Lattice Semiconductor Corporation
06/882,602	4,887,239	United States	One-time programmable data security system for programmable logic device	Issued	Lattice Semiconductor Corporation
06/871,063	4,766,569	United States	Programmable logic array	Issued	Lattice Semiconductor Corporation
06/862,815	4,879,688	United States	In-system programmable logic device	Issued	Lattice Semiconductor Corporation
06/707,670	4,833,646	United States	Programmable logic device with limited sense currents and noise reduction	Issued	Lattice Semiconductor Corporation
07/236,348	4,852,044	United States	Programmable data security circuit for programmable logic device	Issued	Lattice Semiconductor Corporation
11/400,924	7411424	United States	Programmable logic function generator using non-volatile programmable memory switches	Issued	Lattice Semiconductor Corporation
13/403,146		United States	Surface Mountable Integrated Circuit Packaging Scheme	Pending	SiBEAM, Inc.

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
12/242,665		United States	High Speed Integrated Circuit Interface	Pending	SiBEAM, Inc.
14/196,978		United States	Calibration of Single-Ended High-Speed Interfaces	Pending	Silicon Image, Inc.
14/474,005		United States	Inter-Device Conflict Resolution on a Multimedia Link	Pending	Silicon Image, Inc.
61/989,417		United States	Control Target Selection	Pending	Silicon Image, Inc.
61/988,812		United States	Lip Sync Delay Compensation	Pending	Silicon Image, Inc.
61/989,415		United States	Streaming Data and Metadata Synchronization	Pending	Silicon Image, Inc.
61/991,126		United States	Stream Creation with Limited Topology Information	Pending	Silicon Image, Inc.
61/989,411		United States	Topology Discovery	Pending	Silicon Image, Inc.
14/463,146		United States	Radio Frequency Interference Reduction In Multimedia Interfaces	Pending	Silicon Image, Inc.
14/578,266		United States	Control Target Selection	Pending	Silicon Image, Inc.
14/578,257		United States	System for Dynamic Audio Visual Capabilities Exchange	Pending	Silicon Image, Inc.
62/089,767		United States	High-Bandwidth Digital Content Protection over Audio Return Channel	Pending	Silicon Image, Inc.
12/573,492	8482462	United States	MULTI-ANTENNA BEAM-FORMING SYSTEM FOR TRANSMITTING CONSTANT ENVELOPE SIGNALS DECOMPOSED FROM A VARIABLE ENVELOPE SIGNAL	Issued	Silicon Image, Inc.
12/678,463	8207892	United States	TECHNIQUE FOR DETERMINING AN ANGLE OF ARRIVAL IN A COMMUNICATION SYSTEM	Issued	Silicon Image, Inc.

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
12/675,269	8374558	United States	ANTENNA ARRAY WITH FLEXIBLE INTERCONNECT FOR A MOBILE WIRELESS DEVICE	Issued	Silicon Image, Inc.
12/333,134	8213872	United States	TECHNIQUE FOR LOW-POWER OPERATION OF A WIRELESS DEVICE	Issued	Silicon Image, Inc.
12/933,876	8256123	United States	DISPLACEMENT SENSING USING A FLEXIBLE SUBSTRATE	Issued	Silicon Image, Inc.
14/196,993		United States	Calibration of Single-Ended High-Speed Interfaces	Pending	Silicon Image, Inc.
13/988,047		United States	INTEGRATED PHASE-SHIFTING-AND-COMBINING CIRCUITRY TO SUPPORT MULTIPLE ANTENNAS	Pending	Silicon Image, Inc.
14/002,353		United States	TRACKING SYSTEM WITH ORTHOGONAL POLARIZATIONS AND A RETRO-DIRECTIVE ARRAY	Pending	Silicon Image, Inc.
13/726,822		United States	HIGH-ACCURACY DETECTION IN COLLABORATIVE TRACKING SYSTEMS	Pending	Silicon Image, Inc.
13/859,764		United States	ANTENNA SELECTION AND PILOT COMPRESSION IN MIMO SYSTEMS	Pending	Silicon Image, Inc.
62/100,841		United States	I/Q Imbalance Correction for the Combination of Multiple Radio Frequency Frontends	Pending	Silicon Image, Inc.
12/532,107	8571126	United States	MULTI-ANTENNA TRANSMITTER FOR MULTI-TONE SIGNALING	Issued	Silicon Image, Inc.
14/065,420		United States	MULTI-ANTENNA TRANSMITTER FOR MULTI-TONE SIGNALING	Pending	Silicon Image, Inc.
12/679,764	8605823	United States	COMMUNICATION USING	Issued	Silicon Image,

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			CONTINUOUS-PHASE MODULATED SIGNALS		Inc.
14/101,274		United States	COMMUNICATION USING CONTINUOUS-PHASE MODULATED SIGNALS	Pending	Silicon Image, Inc.
12/746,526	8484277	United States	TRANSFORMING SIGNALS USING PASSIVE CIRCUITS	Issued	Silicon Image, Inc.
13/498,884	8610474	United States	SIGNAL DISTRIBUTION NETWORKS AND RELATED MET	Issued	Silicon Image, Inc.
14/089,094		United States	SIGNAL DISTRIBUTION NETWORKS AND RELATED METHODS	Pending	Silicon Image, Inc.
13/519,302		United States	Phase Detection Circuits and Methods	Pending	Silicon Image, Inc.
13/574,586	8795082	United States	DIRECTIONAL BEAM STEERING SYSTEM AND METHOD TO DETECT LOCATION AND MOTION	Issued	Silicon Image, Inc.
14/331,144		United States	DIRECTIONAL BEAM STEERING SYSTEM AND METHOD TO DETECT LOCATION AND MOTION	Pending	Silicon Image, Inc.
13/704,564		United States	Methods and Systems for Near-Field MIMO Communications	Pending	Silicon Image, Inc.
14/235,783		United States	HIGH-ACCURACY AND LOW-POWER TRACKING SYSTEM FOR MOBILE DEVICES	Pending	Silicon Image, Inc.
14/234,623		United States	LOW-COST TRACKING SYSTEM	Pending	Silicon Image, Inc.
14/240,405		United States	CALIBRATING A RETRO-DIRECTIVE ARRAY FOR AN ASYMMETRIC WIRELESS LINK	Pending	Silicon Image, Inc.
14/364,002		United States	COLLABORATIVE CHANNEL SOUNDING IN MULTI-ANTENNA	Pending	Silicon Image, Inc.

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			SYSTEMS		
08/815,486	6,157,360	United States	System And Method For Driving Columns Of An Active Matrix Display	Issued	Silicon Image, Inc.
08/920,336	5,955,929	United States	Voltage-Controlled Oscillator Resistant To Supply Voltage Noise	Issued	Silicon Image, Inc.
09/007,707	5,969,552	United States	Dual Loop Delay-Locked Loop	Issued	Silicon Image, Inc.
09/298,647	6,259,427	United States	Scaling Multi-Dimensional Signals Using Variable Weighting Factors	Issued	Silicon Image, Inc.
09/298,369	6,374,361	United States	Skew-Insensitive Low Voltage Differential Receiver	Issued	Silicon Image, Inc.
09/393,849	6,738,417	United States	Method And Apparatus For Bidirectional Data Transfer Between A Digital Display And A Computer	Issued	Silicon Image, Inc.
09/326,503	6,940,496	United States	Display Module Driving System And Digital To Analog Converter For Driving Display	Issued	Silicon Image, Inc.
09/392,229	6,564,269	United States	Bi-Directional Data Transfer Using The Video Blanking Period In A Digital Data Stream	Issued	Silicon Image, Inc.
09/393,234	6,307,543	United States	Bi-Directional Data Transfer Using Two Pair Of Differential Lines As A Single Additional Differential Pair	Issued	Silicon Image, Inc.
09/947,008	6,492,984	United States	Bi-Directional Data Transfer Using Two Pair Of Differential Lines As A Single Additional Differential Pair	Issued	Silicon Image, Inc.
09/759,624	6,891,910	United States	Baud-Rate Timing Recovery	Issued	Silicon Image, Inc.
09/574,571	6,326,826	United States	Wide Frequency-Range Delay- Locked Loop Circuit	Issued	Silicon Image, Inc.

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
09/881,271	6,954,491	United States	Methods And Systems For Sending Side-Channel Data During Data Inactive Period	Issued	Silicon Image, Inc.
09/922,990	6,961,095	United States	Digital Display Jitter Correction Apparatus And Method	Issued	Silicon Image, Inc.
11/219,323	7,557,863	United States	Digital Display Jitter Correction Apparatus And Method	Issued	Silicon Image, Inc.
09/989,587	6,717,478	United States	Multi-Phase Voltage Controlled Oscillator (VCO) With Common Mode Control	Issued	Silicon Image, Inc.
10/371,220	7,231,009	United States	Data Synchronization Across An Asynchronous Boundary Using, For Example, Multi-Phase Clocks	Issued	Silicon Image, Inc.
09/989,580	7,103,013	United States	Bi-Directional Bridge Circuit Having High Common Mode Rejection And High Input Sensitivity	Issued	Silicon Image, Inc.
11/441,669	7,599,316	United States	Bi-Directional Bridge Circuit Having High Common Mode Rejection And High Input Sensitivity	Issued	Silicon Image, Inc.
12/573,847	8,116,240	United States	Bi-Directional Bridge Circuit Having High Common Mode Rejection And High Input Sensitivity	Issued	Silicon Image, Inc.
10/045,297	7,257,129	United States	Memory Architecture With Multiple Serial Communications Ports	Issued	Silicon Image, Inc.
11/828,286	7,903,684	United States	Communications Architecture For Transmission Of Data Between Memory Bank Caches And Ports	Issued	Silicon Image, Inc.
09/167,527	6,380,978	United States	Digital Video System And Methods For Providing Same	Issued	DVDO, INC. and Silicon Image, Inc.
10/032,136	7,215,376	United States	Digital Video System And Methods For Providing Same	Issued	DVDO, INC. and Silicon Image, Inc.

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
10/942,740	7,359,624	United States	Portable DVD Player	Issued	Silicon Image, Inc.
09/372,713	6,489,998	United States	Method And Apparatus For Deinterlacing Digital Video	Issued	Silicon Image, Inc.
09/941,949	6,909,469	United States	Interlace Motion Artifact Detection Using Vertical Frequency Detection And Analysis	Issued	Silicon Image, Inc.
10/251,642	7,027,099	United States	Method And Apparatus For Deinterlacing Digital Video Images	Issued	Silicon Image, Inc.
11/054,748	7,391,481	United States	Interlace Motion Artifact Detection Using Vertical Frequency Detection And Analysis	Issued	Silicon Image, Inc.
11/357,364	7,499,103	United States	Method And Apparatus For Detecting Frequency In Digital Video Images	Issued	Silicon Image, Inc.
11/932,808	7,633,559	United States	Interlace Motion Artifact Detection Using Vertical Frequency Detection And Analysis	Issued	Silicon Image, Inc.
09/410,543	6,700,622	United States	Method And Apparatus For Detecting The Source Format Of Video Images	Issued	Silicon Image, Inc.
09/396,993	6,515,706	United States	Method And Apparatus For Detecting And Smoothing Diagonal Features In Video Images	Issued	Silicon Image, Inc.
10/191,764	6,829,013	United States	Method And Apparatus For Detecting And Smoothing Diagonal Features In Video Images	Issued	Silicon Image, Inc.
09/363,312	6,681,059	United States	Method And Apparatus For Efficient Video Scaling	Issued	Silicon Image, Inc.
09/359,530	6,587,158	United States	Method And Apparatus For Reducing On-Chip Memory In Vertical Video Processing	Issued	Silicon Image, Inc.
09/226,776	6,219,747	United States	Methods And Apparatus For Variable Length SDRAM	Issued	Silicon Image, Inc.

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			Transfers		
09/805,588	6,385,692	United States	Methods and Apparatus for Variable Length SDRAM Transfers	Issued	Silicon Image, Inc.
09/227,502	6,393,505	United States	Methods And Apparatus For Data Bus Arbitration	Issued	Silicon Image, Inc.
09/226,381	6,473,476	United States	Method And Apparatus For Providing Deterministic Resets For Clock Divider Systems	Issued	Silicon Image, Inc.
09/837,894	6,867,814	United States	Method, System And Article Of Manufacture For Identifying The Source Type And Quality Level Of A Video Sequence	Issued	Silicon Image, Inc.
09/478,122	7,203,557	United States	Audio Signal Delay Apparatus And Method	Issued	Silicon Image, Inc.
10/663,413	7,408,992	United States	Detection And Repair Of MPEG-2 Chroma Upconversion Artifacts	Issued	Silicon Image, Inc.
09/905,318	7,123,307	United States	Clock Jitter Limiting Scheme In Video Transmission Through Multiple Stages	Issued	Silicon Image, Inc.
09/905,615	6,944,804	United States	System And Method For Measuring Pseudo Pixel Error Rate	Issued	Silicon Image, Inc.
09/904,783	6,625,560	United States	Method Of Testing Serial Interface	Issued	Silicon Image, Inc.
09/989,590	6,845,461	United States	High-Speed Bus With Embedded Clock Signals	Issued	Silicon Image, Inc.
09/989,645	6,809,567	United States	System And Method For Multiple-Phase Clock Generation	Issued	Silicon Image, Inc.
09/905,511	7,062,004	United States	Method And Apparatus For Adaptive Control Of PLL Loop Bandwidth	Issued	Silicon Image, Inc.
10/057,823	7,023,487	United States	Deinterlacing Of Video Sources Via Image Feature Edge Detection	Issued	Silicon Image, Inc.

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
09/954,663	7,558,326	United States	Method And Apparatus For Sending Auxiliary Data On A TMDS-Like Link	Issued	Silicon Image, Inc.
10/036,234	7,359,437	United States	Encoding Method And System For Reducing Inter-Symbol Interference Effects In Transmission Over A Serial Link	Issued	Silicon Image, Inc.
10/095,422	7,257,163	United States	Method And System For Reducing Inter-Symbol Interference Effects In Transmission Over A Serial Link With Mapping Of Each Word In A Cluster Of Received Words To A Single Transmitted Word	Issued	Silicon Image, Inc.
10/171,860	7,088,398	United States	Method And Apparatus For Regenerating A Clock For Auxiliary Data Transmitted Over A Serial Link With Video Data	Issued	Silicon Image, Inc.
10/192,296	6,914,637	United States	Method And System For Video And Auxiliary Data Transmission Over A Serial Link	Issued	Silicon Image, Inc.
10/357,750	7,283,566	United States	Method And Circuit For Generating Time Stamp Data From An Embedded-Clock Audio Data Stream And A Video Clock	Issued	Silicon Image, Inc.
10/016,247	6,714,206	United States	Method And System For Spatial-Temporal Dithering For Displays With Overlapping Pixels	Issued	Silicon Image, Inc.
10/133,813	7,136,484	United States	Cryptosystems Using Commuting Pairs In A Monoid	Issued	Silicon Image, Inc.
10/047,772	7,109,958	United States	Supporting Circuitry And Method For Controlling Pixels	Issued	Silicon Image, Inc.
10/045,393	7,039,121	United States	Method And System For Transition-Controlled Selective Block Inversion	Issued	Silicon Image, Inc.

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			Communications		
08/656,032	6,018,456	United States	Enclosure For Removable Computer Peripheral Equipment	Issued	CMD Technology Inc. and Silicon Image, Inc.
08/906,775	5,991,546	United States	System And Method For Interfacing Manually Controllable Input Devices To A Universal Computer Bus System	Issued	CMD Technology Inc. and Silicon Image, Inc.
10/171,820	7,225,282	United States	Method And Apparatus For A Two-Wire Serial Command Bus Interface	Issued	Silicon Image, Inc.
11/713,241	7,441,065	United States	Adaptive Beam-Steering Methods To Maximize Wireless Link Budget And Reduce Delay-Spread Using Multiple Transmit And Receive Antennas	Issued	Silicon Image, Inc.
10/210,839	7,171,525	United States	Method And System For Arbitrating Priority Bids Sent Over Serial Links To A Multi-Port Storage Device	Issued	Silicon Image, Inc.
09/688,536	6,380,783	United States	Cyclic Phase Signal Generation From A Single Clock Source Using Current Phase Interpolation	Issued	Silicon Image, Inc.
09/847,837	6,535,029	United States	Fully Differential Continuous-Time Current-Mode High Speed CMOS Comparator	Issued	Silicon Image, Inc.
10/270,882	7,009,827	United States	Voltage Swing Detection Circuit For Hot Plug Event Or Device Detection Via A Differential Link	Issued	Silicon Image, Inc.
10/162,046	6,843,674	United States	Method And Apparatus For Connecting Serial ATA Storage Components	Issued	Silicon Image, Inc.
09/945,278	7,131,004	United States	Method And Apparatus For Encrypting Data Transmitted Over A Serial Link	Issued	Silicon Image, Inc.
11/499,124	7,900,047	United States	Method And Apparatus For Encrypting Data Transmitted	Issued	Silicon Image,

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			Over A Serial Link		Inc.
11/543,501	7,757,085	United States	Method And Apparatus For Encrypting Data Transmitted Over A Serial Link	Issued	Silicon Image, Inc.
10/224,995	7,218,737	United States	System And Method For An Adaptive State Machine To Control Signal Filtering In A Serial Link	Issued	Silicon Image, Inc.
09/991,057	7,242,766	United States	Method And System For Encrypting And Decrypting Data Using An External Agent	Issued	Silicon Image, Inc.
10/085,177	7,035,290	United States	Method And System For Temporary Interruption Of Video Data Transmission	Issued	Silicon Image, Inc.
10/036,794	6,976,201	United States	Method And System For Host Handling Of Communications Errors	Issued	Silicon Image, Inc.
10/053,461	7,113,507	United States	Method And System For Communicating Control Information Via Out-Of-Band Symbols	Issued	Silicon Image, Inc.
10/045,625	7,746,798	United States	Method And System For Integrating Packet Type Information With Synchronization Symbols	Issued	Silicon Image, Inc.
10/035,911	7,154,905	United States	Method And System For Nesting Of Communications Packets	Issued	Silicon Image, Inc.
10/045,600	6,771,192	United States	Method And System For DC-Balancing At The Physical Layer	Issued	Silicon Image, Inc.
10/045,601	7,340,558	United States	Multisection Memory Bank System	Issued	Silicon Image, Inc.
09/989,647	7,058,121	United States	Logic Gates Including Diode-Connected Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs) To Control Input Threshold Voltage Levels And Switching Transients Of	Issued	Silicon Image, Inc.

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			Output Logic Signals		
09/989,487	6,985,005	United States	Differential Amplifiers Using Asymmetric Transfer Characteristics To Suppress Input Noise In Output Logic Signals	Issued	Silicon Image, Inc.
11/330,047	7,456,648	United States	Differential Amplifiers Using Asymmetric Transfer Characteristics To Suppress Input Noise In Output Logic Signals	Issued	Silicon Image, Inc.
12/275,686	7,847,583	United States	Transmitter And Receiver Using Asymmetric Transfer Characteristics In Differential Amplifiers To Suppress Noise	Issued	Silicon Image, Inc.
10/403,477	6,819,166	United States	Continuous-Time, Low-Frequency-Gain/High-Frequency-Boosting	Issued	Silicon Image, Inc.
10/417,712	7,348,991	United States	Video Graphics Text Mode Enhancement Method For Digitally Processed Data	Issued	Silicon Image, Inc.
10/287,976	6,873,341	United States	Detection Of Video Windows And Graphics Windows	Issued	Silicon Image, Inc.
10/298,722	7,539,304	United States	Integrated Circuit Having Self Test Capability Using Message Digest And Method For Testing Integrated Circuit Having Message Digest Generation Circuitry	Issued	Silicon Image, Inc.
10/215,936	6,717,468	United States	Dynamically Biased Full-Swing Operation Amplifier For An Active Matrix Liquid Crystal Display Driver	Issued	Silicon Image, Inc.
10/268,832	7,412,053	United States	Cryptographic Device With Stored Key Data And Method For Using Stored Key Data To Perform An Authentication Exchange Of Self Test	Issued	Silicon Image, Inc.
11/950,088	7,797,536	United States	Cryptographic Device With Stored Key Data And Method	Issued	Silicon Image, Inc.

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			For Using Stored Key Data To Perform An Authentication Exchange Of Self Test		
10/244,152	6,814,583	United States	Through-Broad PCB Edge Connector, System And Method	Issued	Silicon Image, Inc.
10/247,675	8,064,508	United States	Equalizer With Controllably Weighted Parallel High Pass And Low Pass Filters And Receiver Including Such An Equalizer	Issued	Silicon Image, Inc.
11/796,175	8,275,026	United States	Equalizer With Controllably Weighted Parallel High Pass And Low Pass Filters And Receiver Including Such An Equalizer	Issued	Silicon Image, Inc.
10/651,500	7,551,909	United States	CMOS Transceiver With Dual Current Path VCO	Issued	Silicon Image, Inc.
10/099,533	7,158,593	United States	Combining A Clock Signal And A Data Signal	Issued	Silicon Image, Inc.
10/642,259	7,409,031	United States	Data Sampling Method And Apparatus With Alternating Edge Sampling Phase Detection For Loop Characteristic Stabilization	Issued	Silicon Image, Inc.
10/459,989	7,187,307	United States	Method And System For Encapsulation Of Multiple Levels Of Communication Protocol Functionality Within Line Codes	Issued	Silicon Image, Inc.
10/794,015	7,502,411	United States	Method And Circuit For Adaptive Equalization Of Multiple Signals In Response To A Control Signal Generated From One Of The Equalized Signals	Issued	Silicon Image, Inc.
10/459,992	6,747,580	United States	Method And Apparatus For Encoding Or Decoding Data In Accordance With An Nb/(N+1)B Block Code, And Method For Determining Such A Block Code	Issued	Silicon Image, Inc.

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
10/781,405	7,269,673	United States	Cable With Circuitry For Asserting Stored Cable Data Or Other Information To An External Device Or User	Issued	Silicon Image, Inc.
11/848,758	7,500,032	United States	Cable With Circuitry For Asserting Stored Cable Data Or Other Information To An External Device Or User	Issued	Silicon Image, Inc.
11/123,353	7,375,960	United States	Apparatus For Removably Securing Storage Components In An Enclosure	Issued	Silicon Image, Inc.
10/763,905	7,236,553	United States	Reduced Dead-Cycle, Adaptive Phase Tracking Method And Apparatus	Issued	Silicon Image, Inc.
10/835,301	6,897,793	United States	Method And Apparatus For Run Length Limited TMDS-Like Encoding Of Data	Issued	Silicon Image, Inc.
10/842,231	7,991,096	United States	Data Sampling Method And Apparatus Using Through-Transition Counts To Reject Worst Sampling Position	Issued	Silicon Image, Inc.
10/439,446	7,031,858	United States	Method And Circuit For DC Measurement Of Phase Uniformity Of Multi-Phase Clocks	Issued	Silicon Image, Inc.
10/302,436	7,274,690	United States	An Age Selection Switching Scheme For Data Traffic In A Crossbar Switch	Issued	Silicon Image, Inc.
10/645,786	7,505,422	United States	Preference Programmable First-One Detector And Quadrature Based Random Grant Generator	Issued	Silicon Image, Inc.
10/645,787	7,461,167	United States	A Method For Multicast Service In A Crossbar Switch	Issued	Silicon Image, Inc.
10/762,950	7,352,764	United States	Content Addressable Merged Queue Architecture For Switching Data	Issued	Silicon Image, Inc.
10/434,785	7,519,066	United States	A Method For Switching Data In A Crossbar Switch	Issued	Silicon Image, Inc.
11/372,866	7,694,204	United States	Error Detection In Physical	Issued	Silicon Image,

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			Interfaces For Point-To-Point Communications Between Integrated Circuits		Inc.
12/712,124	7,937,644	United States	Error Detection In Physical Interfaces For Point-To-Point Communications Between Integrated Circuits	Issued	Silicon Image, Inc.
13/099,254	8,099,648	United States	Error Detection In Physical Interfaces For Point-To-Point Communications Between Integrated Circuits	Issued	Silicon Image, Inc.
11/669,416	7,844,762	United States	Parallel Interface Bus To Communicate Video Data Encoded For Serial Data Links	Issued	Silicon Image, Inc.
11/056,995	7,102,446	United States	Phase Lock Loop With Coarse Control Loop Having Frequency Lock Detector And Device Including Same	Issued	Silicon Image, Inc.
11/643,388	7,589,559	United States	Current Mode Circuitry To Modulate A Common Mode Voltage	Issued	Silicon Image, Inc.
12/555,300	7,872,498	United States	Current Mode Circuitry to Modulate a Common Mode Voltage	Issued	Silicon Image, Inc.
11/477,049	7,793,179	United States	Test Clock Control Structures To Generate Configurable Test Clocks For Scan-Based Testing Of Electronic Circuits Using Programmable Test Clock Controllers	Issued	Silicon Image, Inc.
11/856,640	7,782,934	United States	Parameter Scanning For Signal Over-Sampling	Issued	Silicon Image, Inc.
11/592,792	7,450,038	United States	Determining Oversampled Data To Be Included In Unit Intervals	Issued	Silicon Image, Inc.
11/510,254	8,595,434	United States	Smart Scalable Storage Switch Architecture	Issued	Silicon Image, Inc.
14/067,363		United States	Smart Scalable Storage Switch Architecture	Pending	Silicon Image, Inc.

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
11/314,162	7,571,269	United States	A Covert Channel For Conveying Supplemental Messages In A Protocol-Defined Link For A System Of Storage Devices	Issued	Silicon Image, Inc.
11/637,254	7,602,253	United States	Adaptive Bandwidth Phase Locked Loop With Feedforward Divider	Issued	Silicon Image, Inc.
11/656,331	7,984,369	United States	Concurrent Code Checker And Hardware Efficient High-Speed I/O Having Built-In Self-Test And Debug Features	Issued	Silicon Image, Inc.
11/694,819	7,949,863	United States	Multi-Port Memory Device Having Variable Port Speeds	Issued	Silicon Image, Inc.
11/694,813	7,639,561	United States	Power-Saving Clocking Technique	Issued	Silicon Image, Inc.
11/690,629	7,831,778	United States	Mechanism For Streaming Media Data Over Wideband Wireless Networks	Issued	Silicon Image, Inc.
11/476,457	7,840,861	United States	Scan-Based Testing Of Devices Implementing A Test Clock Control Structure (â€œTCCSâ€)	Issued	Silicon Image, Inc.
11/861,175	8,160,192	United States	Signal Interleaving for Serial Clock and Data Recovery	Issued	Silicon Image, Inc.
11/690,642	7,908,501	United States	Shared Nonvolatile Memory Architecture	Issued	Silicon Image, Inc.
11/742,358	7,698,088	United States	Interface Test Circuitry And Methods	Issued	Silicon Image, Inc.
11/848,641	8,233,432	United States	Ensuring Physical Locality Of Entities Sharing Data	Issued	Silicon Image, Inc.
11/683,608	7,831,877	United States	Method And Apparatus For A Two-Wire Serial Command Bus Interface	Issued	Silicon Image, Inc.
11/690,659	7,849,339	United States	Progressive Power Control Of A Multi-Port Memory Device	Issued	Silicon Image, Inc.
11/567,514	7,365,659	United States	Method Of Context Adaptive Binary Arithmetic Coding	Issued	Silicon Image, Inc.

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			And Coding Apparatus Using The Same		
12/778,882		United States	Multi-Level Port Expansion For Port Multipliers	Pending	Silicon Image, Inc.
12/147,248	7,836,223	United States	Operation Of Media Interface To Provide Bidirectional Communications	Issued	Silicon Image, Inc.
11/849,163	8,695,034	United States	Delivering On Screen Display Data To Existing Display Devices	Issued	Silicon Image, Inc.
11/828,219	8,599,315	United States	On Screen Displays Associated With Remote Video Source Devices	Issued	Silicon Image, Inc.
14/070,373		United States	On Screen Displays Associated With Remote Video Source Devices	Pending	Silicon Image, Inc.
11/829,800	7,903,550	United States	Bandwidth Reservation For Data Flows In Interconnection Networks	Issued	Silicon Image, Inc.
11/828,223	8,149,711	United States	Data Stream Control For Network Devices	Issued	Silicon Image, Inc.
13/541,390	8,924,509	United States	Automated Service Discovery And Dynamic Connection Management	Issued	Silicon Image, Inc.
11/836,082	8,468,212	United States	Network Repository For Metadata	Issued	Silicon Image, Inc.
13/919,773		United States	Network Repository For Metadata	Pending	Silicon Image, Inc.
11/829,790	7,911,956	United States	Packet Level Prioritization In Interconnection Networks	Issued	Silicon Image, Inc.
11/828,226		United States	Streaming Data Content In A Network	Pending	Silicon Image, Inc.
11/848,153	7,936,790	United States	Synchronizing Related Data Streams In Interconnection Networks	Issued	Silicon Image, Inc.
11/952,052	8,001,334	United States	Bank Sharing And Refresh In A Shared Multi-Port Memory Device	Issued	Silicon Image, Inc.

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
12/075,954	7,979,589	United States	Method, Apparatus, And System For Port Multiplier Enhancement	Issued	Silicon Image, Inc.
13/298,001		United States	Iddq Testing Of CMOS Devices	Pending	Silicon Image, Inc.
10/788,704	6,944,086	United States	Semiconductor Memory Device	Issued	Silicon Image, Inc.
10/876,231	7,016,255	United States	Multi-Port Memory Device	Issued	Silicon Image, Inc.
10/877,318	7,089,465	United States	Multi-Port Memory Device Having Serial I/O Interface	Issued	Silicon Image, Inc.
12/075,906	7,904,566	United States	Method, Apparatus, And System For Employing An Enhanced Port Multiplier	Issued	Silicon Image, Inc.
12/497,391	8,386,867	United States	Computer Memory Test Structure	Issued	Silicon Image, Inc.
13/776,508	8,667,354	United States	Computer Memory Test Structure	Issued	Silicon Image, Inc.
14/145,751	8,924,805	United States	Computer Memory Test Structure	Issued	Silicon Image, Inc.
12/197,020	8,086,886	United States	Group Power Management Of Network Devices	Issued	Silicon Image, Inc.
12/683,365	8,543,873	United States	Multi-Site Testing Of Computer Memory Devices And Serial I/O Ports	Issued	Silicon Image, Inc.
14/035,795	8,839,058	United States	Multi-Site Testing Of Computer Memory Devices And Serial I/O Ports	Issued	Silicon Image, Inc.
11/969,847	8,090,030	United States	Method, Apparatus And System For Generating And Facilitating Mobile High-Definition Multimedia Interface	Issued	Silicon Image, Inc.
11/969,852	7,856,520	United States	Control Bus For Connection Of Electronic Devices	Issued	Silicon Image, Inc.
11/969,865	7,921,231	United States	Discovery Of Electronic Devices Utilizing A Control	Issued	Silicon Image, Inc.

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			Bus		
12/172,187	8,238,653	United States	Methods And Mechanisms For Probabilistic Color Correction	Issued	Silicon Image, Inc.
12/392,000		United States	Method, Apparatus, And System For Pre-Authentication And Processing Of Data Streams	Pending	Silicon Image, Inc.
12/391,987	8,644,504	United States	Method, Apparatus, And System For Deciphering Media Content Stream	Issued	Silicon Image, Inc.
12/605,134	8,407,427	United States	Method And System For Improving Serial Port Memory Communication Latency And Reliability	Issued	Silicon Image, Inc.
13/850,147	8,892,825	United States	Method and System for Improving Serial Port Memory Communication Latency and Reliability	Issued	Silicon Image, Inc.
12/260,970	8,036,248	United States	Method, Apparatus, And System For Automatic Data Aligner For Multiple Serial Receivers	Issued	Silicon Image, Inc.
12/359,025	8,026,726	United States	Fault Testing For Interconnections	Issued	Silicon Image, Inc.
12/486,969	8,793,723	United States	Detection Of Encryption Utilizing Error Detection For Received Data	Issued	Silicon Image, Inc.
12/570,874	8,644,334	United States	Messaging To Provide Data Link Integrity	Issued	Silicon Image, Inc.
12/260,972	7,777,652	United States	Coding System For Memory Systems Employing High-Speed Serial Links	Issued	Silicon Image, Inc.
12/847,416	7,978,099	United States	17b/20b Coding System	Issued	Silicon Image, Inc.
12/351,698	8,374,346	United States	Method, Apparatus, And System For Pre-Authentication And Keep-Authentication Of Content Protected Ports	Issued	Silicon Image, Inc.

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
12/316,305	8,347,081	United States	Method, Apparatus And System For Employing A Content Protection System	Issued	Silicon Image, Inc.
12/577,707	8,275,914	United States	Method And System For Transmitting Or Receiving N-Bit Video Data Over A Serial Link	Issued	Silicon Image, Inc.
12/606,096	8,176,214	United States	Transmission Of Alternative Content Over Standard Device Connectors	Issued	Silicon Image, Inc.
12/351,712	8,185,739	United States	Method And System For Detecting Successful Authentication Of Multiple Ports In A Time Based Roving Architecture	Issued	Silicon Image, Inc.
12/512,877	8,458,343	United States	Signaling For Transitions Between Modes Of Data Transmission	Issued	Silicon Image, Inc.
12/983,233	8,489,784	United States	Adaptive Interconnection Scheme For Multimedia Devices	Issued	Silicon Image, Inc.
13/004,359	8,755,431	United States	Transmission And Detection Of Multi-Channel Signals In Reduced Channel Format	Issued	Silicon Image, Inc.
12/650,357		United States	Method, Apparatus, And System For Simultaneously Previewing Contents From Multiple Protected Sources	Pending	Silicon Image, Inc.
12/712,933	8,692,937	United States	Video Frame Synchronization	Issued	Silicon Image, Inc.
12/966,194		United States	Transmission And Handling Of Three-Dimensional Video Content	Pending	Silicon Image, Inc.
12/873,124	8,325,757	United States	De-Encapsulation Of Data Streams Into Multiple Links	Issued	Silicon Image, Inc.
12/704,417	8,510,487	United States	Hybrid Interface For Serial And Parallel Communication	Issued	Silicon Image, Inc.
13/934,147	8,751,709	United States	Hybrid Interface For Serial And Parallel Communication	Issued	Silicon Image, Inc.

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
12/842,165	8,930,692	United States	Mechanism For Internal Processing Of Content Through Partial Authentication On Secondary Channel	Issued	Silicon Image, Inc.
12/842,190		United States	Mechanism For Partial Encryption Of Data Streams	Pending	Silicon Image, Inc.
13/021,958		United States	Determination Of Physical Connectivity Status Of Devices Based On Electrical Measurement	Allowed	Silicon Image, Inc.
12/898,528	8,598,898	United States	Testing Of High-Speed Input-Output Devices	Issued	Silicon Image, Inc.
13/434,273		United States	Method, Apparatus And System For Transitioning An Audio/Video Device Between A Source Mode And A Sink Mode	Pending	Silicon Image, Inc.
12/848,037	8,624,960	United States	Multi-View Display System	Issued	Silicon Image, Inc.
14/094,668		United States	Multi-View Display System	Pending	Silicon Image, Inc.
12/816,437	8,698,958	United States	Mechanism For Memory Reduction In Picture-In-Picture Video Generation	Issued	Silicon Image, Inc.
13/753,408		United States	Communication Bridging Between Devices Via Multiple Bridge Elements	Pending	Silicon Image, Inc.
13/198,584		United States	Conversion Of Multimedia Data Streams For Use By Connected Devices	Pending	Silicon Image, Inc.
12/906,939	8,537,201	United States	Combining Video Data Streams Of Differing Dimensionality For Concurrent Display	Issued	Silicon Image, Inc.
13/172,745	8,484,387	United States	Detection Of Cable Connections For Electronic Devices	Issued	Silicon Image, Inc.
13/172,742	8,601,173	United States	Detection Of Cable Connections For Electronic	Issued	Silicon Image, Inc.

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			Devices		
13/362,930		United States	Mechanism For Low Power Standby Mode Control Circuit	Allowed	Silicon Image, Inc.
13/217,138	8,379,145	United States	Conversion And Processing Of Deep Color Video In A Single Clock Domain	Issued	Silicon Image, Inc.
12/979,995	8,874,820	United States	Mechanism For Facilitating A Configurable Port-Type Peripheral Component Interconnect Express/Serial Advanced Technology Attachment Host Controller Architecture	Issued	Silicon Image, Inc.
12/950,850	8,504,672	United States	Discovery Of Electronic Devices In A Combined Network	Issued	Silicon Image, Inc.
13/959,592	8,799,443	United States	Discovery of Electronic Devices in a Combined Network	Issued	Silicon Image, Inc.
13/348,378		United States	Proxy Device Operation In Command And Control Network	Pending	Silicon Image, Inc.
12/950,867		United States	Transfer Of Control Bus Signaling On Packet-Switched Network	Pending	Silicon Image, Inc.
13/339,339		United States	Mechanism For Recovering Clock For Streaming Content Over A Packetized Network	Pending	Silicon Image, Inc.
13/302,452		United States	Multimedia I/O System Architecture for Advanced Digital Television	Pending	Silicon Image, Inc.
13/107,031		United States	Audio And Video Data Multiplexing For Multimedia Stream Switch	Pending	Silicon Image, Inc.
13/174,630		United States	Single-Ended Configurable Multi-Mode Driver	Pending	Silicon Image, Inc.
13/173,302		United States	Fine-Grained Self Refresh Control For DRAM Devices	Pending	Silicon Image, Inc.
13/174,616	8,760,188	United States	Configurable Multi-Dimensional Driver And	Issued	Silicon Image,

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			Receiver		Inc.
13/083,399	8,611,486	United States	Adjustment Of Clock Signals Regenerated From A Data Stream	Issued	Silicon Image, Inc.
11/437,357	7,982,798	United States	Edge Detection	Issued	Silicon Image, Inc.
13/153,230	8,446,525	United States	Edge Detection	Issued	Silicon Image, Inc.
10/753,909	7,400,359	United States	Video Stream Routing And Format Conversion Unit With Audio Delay	Issued	Silicon Image, Inc.
10/889,855	7,710,501	United States	Time Base Correction And Frame Rate Conversion	Issued	Silicon Image, Inc.
11/487,144	8,004,606	United States	Original Scan Line Detection	Issued	Silicon Image, Inc.
11/941,050	8,086,067	United States	Noise Cancellation	Issued	Silicon Image, Inc.
11/512,754	8,120,703	United States	Source-Adaptive Video Deinterlacer	Issued	Silicon Image, Inc.
12/204,760	8,559,746	United States	System, Method And Apparatus For Smoothing Of Edges In Images To Remove Irregularities	Issued	Silicon Image, Inc.
14/054,575		United States	System, Method and Apparatus for Smoothing of Edges in Images to Remove Irregularities	Pending	Silicon Image, Inc.
12/703,623	8,452,117	United States	Block Noise Detection And Filtering	Issued	Silicon Image, Inc.
13/899,222	8,891,897	United States	Block Noise Detection And Filtering	Issued	Silicon Image, Inc.
13/335,398		United States	Ringing Suppression In Video Scalers	Pending	Silicon Image, Inc.
13/546,904		United States	Transmission Of Multiple Protocol Data Elements Via An Interface Utilizing A Data Tunnel	Pending	Silicon Image, Inc.

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
11/202,995	7,904,117	United States	Wireless Communication Device Using Adaptive Beamforming	Issued	SiBEAM, Inc.
11/706,711	7,710,319	United States	HD Physical Layer Of A Wireless Communication Device	Issued	SiBEAM, Inc.
12/748,276	7,982,669	United States	Adaptive Beam-Steering Methods To Maximize Wireless Link Budget And Reduce Delay-Spread Using Multiple Transmit And Receive Antennas	Issued	SiBEAM, Inc.
11/706,470	8,014,416	United States	Inter-Port Communication In A Multi-Port Memory Device	Issued	Silicon Image, Inc.
11/689,386	7,881,258	United States	Circuitry To Prevent Peak Power Problems During Scan Shift	Issued	SiBEAM, Inc.
11/726,874	8,155,712	United States	Low Power Very High-Data Rate Device	Issued	SiBEAM, Inc.
11/588,472	8,022,887	United States	Planar Antenna	Issued	SiBEAM, Inc.
11/752,073		United States	A Compact Millimeter Wave Vertical Interconnection Scheme By Combining Flip-Chip, Layer Transition	Pending	SiBEAM, Inc.
11/752,083	7,675,465	United States	Surface Mountable Integrated Circuit Packaging Scheme	Issued	SiBEAM, Inc.
12/215,959		United States	Mechanism For Communication With Multiple Wireless Video Area Networks	Pending	SiBEAM, Inc.
11/981,935		United States	Wireless HD Mac Frame Format	Pending	SiBEAM, Inc.
11/938,126	8,170,522	United States	Multi-Transformer Architecture For An RF Active Circuit	Issued	SiBEAM, Inc.
11/999,810	8,750,241	United States	Concurrent Association With Multiple WVAN Network	Issued	SiBEAM, Inc.
12/079,133	8,831,225	United States	Data Security	Issued	SiBEAM, Inc.

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
12/011,404	7,948,961	United States	Wireless Proximity Estimation	Issued	SiBEAM, Inc.
11/982,209	8,279,784	United States	Wireless HD AV Packet Format	Issued	SiBEAM, Inc.
12/055,160	8,170,617	United States	Extensions To Adaptive BeamSteering Method	Issued	SiBEAM, Inc.
12/164,757		United States	Exchanging Information Between Components Coupled With An I2C Bus Via Separate Banks	Pending	SiBEAM, Inc.
12/167,195	8,229,352	United States	Wireless Architecture For 60 GHz	Issued	SiBEAM, Inc.
11/901,069	7,986,753	United States	Modified Branch Metric For Decoders And Equalizers	Issued	SiBEAM, Inc.
12/059,757	7,915,909	United States	RF Integrated Circuit Test Methodology And System	Issued	SiBEAM, Inc.
12/164,907		United States	Dispatch Capability Using A Single Physical Interface	Pending	SiBEAM, Inc.
12/165,468		United States	Bitmap Device Identification In A Wireless Communication System	Pending	SiBEAM, Inc.
12/165,472	8,897,719	United States	Initializing A Transceiver In A Wireless Communication System	Issued	SiBEAM, Inc.
12/164,849	8,341,271	United States	Device Discovery In A Wireless Communication System	Issued	SiBEAM, Inc.
12/164,810	8,116,333	United States	Connection Control In A Wireless Communication System	Issued	SiBEAM, Inc.
12/699,758	8,588,193	United States	Enhanced Wireless Data Rates Using Multiple Beams	Issued	SiBEAM, Inc.
12/699,781	8,457,026	United States	Enhanced Wireless Data Rates Using Multiple Beams	Issued	SiBEAM, Inc.
13/113,318		United States	Apparatus, System, And Method For A Compact Symmetrical Transition Structure For Radio	Allowed	SiBEAM, Inc.

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			Frequency Applications		
14/128,551		United States	Method To Drive HDMI Or MHL Or USB Data Through One Set Of Pins	Pending	Silicon Image, Inc.
13/984,018		United States	Concept And Method Of Reducing Data Dependent Jitter	Pending	Silicon Image, Inc.
13/269,450		United States	Identification And Handling Of Data Streams Using Coded Preambles	Allowed	Silicon Image, Inc.
13/611,786		United States	Combining Video And Audio Streams Utilizing Pixel Repetition Bandwidth	Pending	Silicon Image, Inc.
14/118,832		United States	Compensation Scheme For MHL Common Mode Clock Swing	Pending	Silicon Image, Inc.
13/773,534		United States	Transmitting Multiple Differential Signals Over a Reduced Number of Physical Channels	Pending	Silicon Image, Inc.
13/460,393		United States	Cost-Efficient And Low-Latency Motion Picture Encoding For Limited Channel Bandwidth	Pending	Silicon Image, Inc.
13/791,494	8,925,003	United States	Mechanism For Facilitating Syncronization Of Audio And Video Between Multiple Media Devices	Issued	Silicon Image, Inc.
13/622,286	8,885,435	United States	Interfacing Between Integrated Circuits With Asymmetric Voltage Swing	Issued	Silicon Image, Inc.
13/770,984		United States	Configurable Single Ended Driver	Pending	Silicon Image, Inc.
13/779,372	8,920,188	United States	Integrated Connector/Flex Cable	Issued	Silicon Image, Inc.
13/834,927		United States	Simultaneous Transmission Of Clock And Bidirectional Data Over A Communication Channel	Allowed	Silicon Image, Inc.

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
13/605,708	8,841,974	United States	Test Solution For Ring Oscillators	Issued	Silicon Image, Inc.
14/193,932		United States	Test Solution for a Random Number Generator	Pending	Silicon Image, Inc.
13/787,664		United States	Auxiliary Data Encoding In Video Data	Pending	Silicon Image, Inc.
13/738,768		United States	Method And Apparatus For Reducing Digital Video Image Data	Pending	Silicon Image, Inc.
13/736,765	8,832,338	United States	Mechanism For Facilitating Dynamic Timestamp-Less Clock Regeneration For Transmitting Media Streams Over Shared Channels	Issued	Silicon Image, Inc.
14/123,037		United States	Timing Controlled Cascade Feed-Through High Speed Line Driver	Pending	Silicon Image, Inc.
13/776,577		United States	Apparatus, System And Method For Providing Clock And Data Signaling	Pending	Silicon Image, Inc.
13/940,038		United States	Integrated Mobile Desktop	Pending	Silicon Image, Inc.
13/915,586		United States	Multiple Protocol Tunneling Using Time Division Operations	Pending	Silicon Image, Inc.
13/891,842	8,786,776	United States	Method, Apparatus And System For Communicating Sideband Data With Non-Compressed Video	Issued	Silicon Image, Inc.
13/671,527		United States	Methods And Apparatuses To Provide And Electro-Optical Alignment	Pending	Silicon Image, Inc.
14/371,973		United States	Charge Pump Calibration for Dual-Path Phase-Locked Loop	Pending	Silicon Image, Inc.
14/115,324		United States	Mechanism for Facilitating Dynamic Phase Detection with High Jitter Tolerance for Images of Media Streams	Allowed	Silicon Image, Inc.

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
14/135,470		United States	Apparatus, System and Method for Formatting Audio-Video Information	Pending	Silicon Image, Inc.
13/839,671		United States	Full Frame Buffer To Improve Video Performance In Low- Latency Video Communication Systems	Pending	Silicon Image, Inc.
12/057,051		United States	Bi-Directional Digital Interface For Video And Audio (DIVA)	Pending	Silicon Image, Inc.
11/760,164	7,940,809	United States	Digital Video Interface With Bi-Directional Half-Duplex Clock Channel Used As Auxiliary Data Channel	Issued	Silicon Image, Inc.
11/865,621	7,916,780	United States	Adaptive Equalizer For Use With Clock And Data Recovery Circuit Of Serial Communication Link	Issued	Silicon Image, Inc.
12/222,745	7,737,802	United States	Passive Equalizer With Negative Impedance To Increase A Gain	Issued	Silicon Image, Inc.
12/636,063	8,680,712	United States	Power Delivery Over Digital Interactive Interface For Video And Audio (DIIVA)	Issued	Silicon Image, Inc.
13/521,739		United States	Multi-Media USB Data Transfer Over Digital Interaction Interface for Video and Audio (DIIVA)	Pending	Silicon Image, Inc.
13/521,762		United States	Video Management And Control In Home Multimedia Network	Pending	Silicon Image, Inc.
14/381,186		United States	Linear Regulator with Improved Power Supply Ripple Rejection	Pending	Silicon Image, Inc.
13/844,152		United States	Electronic Alignment Of Optical Signals	Pending	Silicon Image, Inc.
14/391,382		United States	Frequency Response Compensation in a Digital to Analog Converter	Pending	Silicon Image, Inc.
14/165,340		United States	Apparatus, System and	Pending	Silicon Image,

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			Method for Providing Switching with a T-Coil Circuit		Inc.
13/836,895	8,928,411	United States	Integration Of Signal Sampling Within Transistor Amplifier Stage	Issued	Silicon Image, Inc.
14/165,345		United States	Apparatus, Method and System for Asymmetric Full-Duplex Communication	Pending	Silicon Image, Inc.
14/209,785		United States	Method And Apparatus For Implementing Wide Data Range And Wide Common-Mode Receivers	Pending	Silicon Image, Inc.
14/296,377		United States	Transmitting Apparatus with Source Termination	Pending	Silicon Image, Inc.
14/368,781		United States	Caching of Capabilities Information of Counterpart Device for Efficient Handshaking Operation	Pending	Silicon Image, Inc.
14/163,981		United States	Mechanism for Facilitating Dynamic Counter Synchronization and Packetization in High-Definition Multimedia Interface and Mobile High-Definition Link	Pending	Silicon Image, Inc.
14/253,808		United States	Communication of Multimedia Data Streams Over Multiple Communication Lanes	Pending	Silicon Image, Inc.
14/279,316		United States	HDCP2.2 Authentication Engine and Stream Cipher Engine Sharing in Digital Content Protection Architectures	Pending	Silicon Image, Inc.
14/383,865		United States	Techniques for Fractional-N Phase Locked Loops	Pending	Silicon Image, Inc.
61/949,901		United States	Compressed Video Transfer Over HDMI and MHL	Pending	Silicon Image, Inc.
14/563,797		United States	Electrical Duplex to Optical Conversion	Pending	Silicon Image, Inc.

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
14/470,750		United States	Arbitration Signaling within a Multimedia High Definition Link (MHL 3) Device	Pending	Silicon Image, Inc.
14/275,692		United States	Error Detection and Mitigation in Video Channels	Pending	Silicon Image, Inc.
14/339,393		United States	Phase-Modulated On-Off Keying for Millimeter Wave Spectrum Control	Pending	Silicon Image, Inc.
14/145,715		United States	Messaging to Provide Data Link Integrity	Pending	Silicon Image, Inc.
14/145,736	8,854,548	United States	Mechanism for Memory Reduction in Picture-In-Picture Video Generation	Issued	Silicon Image, Inc.
14/470,613		United States	Compressed Video Transfer Over a Multimedia Link	Pending	Silicon Image, Inc.
14/184,647		United States	Video Frame Synchronization	Pending	Silicon Image, Inc.
14/181,446		United States	Power Delivery Over Digital Interaction Interface for Video and Audio (DiiVA)	Pending	Silicon Image, Inc.
14/470,804		United States	Phase Relationship Control for Control Channel of a Multimedia Communication Link	Pending	Silicon Image, Inc.
14/470,809		United States	Retry Disparity for Control Channel of a Multimedia Communication Link	Pending	Silicon Image, Inc.
61/943,267		United States	Pre-Processor and Post-Processor for Compression of 4:2:0 Encoded Video Streams with Video Compression Codecs Embedded within an Audio/Video Standard	Pending	Silicon Image, Inc.
14/278,255		United States	Encoding Guard Band Data for Transmission Via a Communications Interface Utilizing Transition-Minimized Differential Signaling (Tmds) Coding	Pending	Silicon Image, Inc.
14/322,753		United States	Calibration Of Single-Ended	Pending	Silicon Image,

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			High-Speed Interfaces		Inc.
61/947,704		United States	Reversible Connector	Pending	Silicon Image, Inc.
14/460,737		United States	System and Method for Transcoding Data	Pending	Silicon Image, Inc.
14/502,928		United States	Electrical Connector with Optical Channel	Pending	Silicon Image, Inc.
14/322,753		United States	Cable with Circuitry for Communicating Performance Information	Pending	Silicon Image, Inc.
61/973,837		United States	Error Correction for Transmission of Compressed Video Data Over Standards-Defined Coded Audio/Video Links	Pending	Silicon Image, Inc.
61/975,517		United States	(MHL) Connector Cable Detect, Cable Orientation Detect and/or Lane Re-Mapping	Pending	Silicon Image, Inc.
61/979,477		United States	MHL3 Router without HDCP2.2 Decryption and Encryption Operation	Pending	Silicon Image, Inc.
61/979,483		United States	TDD over 5-Pin Interface	Pending	Silicon Image, Inc.
14/470,620		United States	Compressed Blanking Period Transfer Over a Multimedia Link	Pending	Silicon Image, Inc.
14/273,400		United States	Transmission and Detection of Multi-Channel Signals in Reduced Channel Format	Pending	Silicon Image, Inc.
61/989,409		United States	System for Dynamic Capabilities, Status, and Metadata Exchange	Pending	Silicon Image, Inc.
14/300,166		United States	Configurable Multi-Dimensional Driver and Receiver	Pending	Silicon Image, Inc.
14/483,013		United States	Enhanced Communication Link Using Synchronization Signal as Link Command	Pending	Silicon Image, Inc.

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
62/043,218		United States	Run Length Programmable Unified Built-In Self-Test (BIST) Scheme for Various High-Speed Serial IO Standards	Pending	Silicon Image, Inc.
14/559,523		United States	Determination of Physical Connectivity Status of Devices Based on Electrical Measurement	Pending	Silicon Image, Inc.
14/516,136		United States	Method and System for Improving Serial Port Memory Communication Latency and Reliability	Pending	Silicon Image, Inc.
62/061,630		United States	Secure Control Communication Between an Application Processor and a Transmitter	Pending	Silicon Image, Inc.
62/075,554		United States	Metadata Transfer for HDMI/MHL	Pending	Silicon Image, Inc.
14/570,817		United States	Mechanism for Facilitating Dynamic Phase Detection with High Jitter Tolerance for Images of Media Streams	Pending	Silicon Image, Inc.
14/589,889		United States	Displaying Multiple Videos on Sink Device Using Display Information of Source Device	Pending	Silicon Image, Inc.
14/589,925		United States	Lower Power Operations in a Wireless Tunneling Transceiver	Pending	Silicon Image, Inc.
14/591,845		United States	Simultaneous Transmission of Clock and Bidirectional Data Over a Communication Channel	Pending	Silicon Image, Inc.
14/449095	20150036756	United States	Radio Frequency Interference Reduction In Multimedia Interfaces	Pending	Silicon Image, Inc.

UNITED STATES PATENT AND TRADEMARK OFFICE

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United States Patent and Trademark Office
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P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
10/036,234	12/24/2001	Seung Ho Hwang	

CONFIRMATION NO. 6063

29416
LATTICE SEMICONDUCTOR CORPORATION
111 SW 5th Avenue
Suite 700
Portland, OR 97204

POA ACCEPTANCE LETTER

OC000000090033769

Date Mailed: 03/21/2017

NOTICE OF ACCEPTANCE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 03/17/2017.

The Power of Attorney in this application is accepted. Correspondence in this application will be mailed to the above address as provided by 37 CFR 1.33.

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at **(571) 272-4000** or **(571) 272-4200** or **1-888-786-0101**.

/deelliott/

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
10/036,234	12/24/2001	Seung Ho Hwang	SII-1000 [SIMG0115]

CONFIRMATION NO. 6063

60974
GIRARD & EQUITZ LLP
1539 Taraval St.
SUITE 202
SAN FRANCISCO, CA 94116

POWER OF ATTORNEY NOTICE

OC000000090033636

Date Mailed: 03/21/2017

NOTICE REGARDING CHANGE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 03/17/2017.

- The Power of Attorney to you in this application has been revoked by the assignee who has intervened as provided by 37 CFR 3.71. Future correspondence will be mailed to the new address of record(37 CFR 1.33).

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at **(571) 272-4000** or **(571) 272-4200** or **1-888-786-0101**.

/deelliott/

Doc Code: PA..

Document Description: Power of Attorney

PTO/AIA/82B(07-12)
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POWER OF ATTORNEY BY APPLICANT

I hereby revoke all previous powers of attorney given in the application identified in the attached transmittal letter.

■ I hereby appoint Practitioner(s) associated with the following Customer Number as my/our attorney(s) or agent(s), and to transact all business in the United States Patent and Trademark Office connected therewith for the application referenced in the attached transmittal letter (form PTO/AIA/82A or equivalent):

29416

OR

☐ I hereby appoint Practitioner(s) named below as my/our attorney(s) or agent(s), and to transact all business in the United States Patent and Trademark Office connected therewith for the application referenced in the attached transmittal letter (form PTO/AIA/82A or equivalent):

Name	Registration Number	Name	Registration Number

Please recognize or change the correspondence address for the application identified in the attached transmittal letter to:

■ The address associated with the above-mentioned Customer Number.

OR

☐ The address associated with Customer Number:

OR

☐ Firm or Individual Name					
Address					
City		State		Zip	
Country					
Telephone		Email			

I am the Applicant:

☐ Inventor or Joint Inventor

☐ Legal Representative of a Deceased or Legally Incapacitated Inventor

■ Assignee or Person to Whom the Inventor is Under an Obligation to Assign

☐ Person Who Otherwise Shows Sufficient Proprietary Interest (*e.g.*, a petition under 37 CFR 1.46(b)(2) was granted in the application or is concurrently being filed with this document)

SIGNATURE of Applicant for Patent

Signature		Date	1-23-2013
Name	Byron W. Milstead	Telephone	503.268.8555
Title and Company	Corporate Vice President, Lattice Semiconductor Corporation		

NOTE: Signature - This form must be signed by the applicant in accordance with 37 CFR 1.33. See 37 CFR 1.4 for signature requirements and certifications. Submit multiple forms for more than one signature, see below *.

■ *Total of 1 forms are submitted.

This collection of information is required by 37 CFR 1.31, 1.32 and 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: **Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Electronic Acknowledgement Receipt

EFS ID:	28666385
Application Number:	10036234
International Application Number:	
Confirmation Number:	6063
Title of Invention:	ENCODING METHOD AND SYSTEM FOR REDUCING INTER-SYMBOL INTERFERENCE EFFECTS IN TRANSMISSION OVER A SERIAL LINK
First Named Inventor/Applicant Name:	Seung Ho Hwang
Customer Number:	60974
Filer:	Michael S. Garrabrants
Filer Authorized By:	
Attorney Docket Number:	SII-1000 [SIMG0115]
Receipt Date:	17-MAR-2017
Filing Date:	24-DEC-2001
Time Stamp:	16:29:44
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Assignee showing of ownership per 37 CFR 3.73	077USCIPsb96.pdf	381754 513964fc1c18b4943d48a3074593b34a6b3b25b7	no	2

Warnings:

Information:					
2	Power of Attorney	POA-29416Lattice.pdf	145556 df2026a33f42d818a11342c4c57b855d6bcb2496	no	1
Warnings:					
Information:					
			Total Files Size (in bytes):	527310	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PTO/SB/96 (07-09)
Approved for use through 07/31/2012. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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STATEMENT UNDER 37 CFR 3.73(b)

Applicant/Patent Owner: Lattice Semiconductor Corporation

Application No./Patent No.: 10/036,234 (7,359,437) Filed/Issue Date: 12/24/2001 (4/15/2008)

Titled: ENCODING METHOD AND SYSTEM FOR REDUCING INTER-SYMBOL INTERFERENCE EFFECTS IN TRANSMISSION OVER A SERIAL LINK

Lattice Semiconductor Corporation , a Corporation

(Name of Assignee) (Type of Assignee, e.g., corporation, partnership, university, government agency, etc.

states that it is:

1. [x] the assignee of the entire right, title, and interest in;

2. [ ] an assignee of less than the entire right, title, and interest in (The extent (by percentage) of its ownership interest is _____ %); or

3. [ ] the assignee of an undivided interest in the entirety of (a complete assignment from one of the joint inventors was made)

the patent application/patent identified above, by virtue of either:

A. [ ] An assignment from the inventor(s) of the patent application/patent identified above. The assignment was recorded in the United States Patent and Trademark Office at Reel _____, Frame _____, or for which a copy therefore is attached.

OR

B. [x] A chain of title from the inventor(s), of the patent application/patent identified above, to the current assignee as follows:

1. From: Jano Banks, Paul D. Wolf, Eric Lee and Baegir To: Silicon Image, Inc.

The document was recorded in the United States Patent and Trademark Office at
Reel 12730 , Frame 0562 , or for which a copy thereof is attached.

2. From: Albert Scalise To: Silicon Image, Inc.

The document was recorded in the United States Patent and Trademark Office at
Reel 12964 , Frame 0599 , or for which a copy thereof is attached.

3. From: Silicon Image, Inc. To: Lattice Semiconductor Corporation

The document was recorded in the United States Patent and Trademark Office at
Reel 36419 , Frame 0792 , or for which a copy thereof is attached.

[ ] Additional documents in the chain of title are listed on a supplemental sheet(s).

[x] As required by 37 CFR 3.73(b)(1)(i), the documentary evidence of the chain of title from the original owner to the assignee was, or concurrently is being, submitted for recordation pursuant to 37 CFR 3.11.

[NOTE: A separate copy (*i.e.*, a true copy of the original assignment document(s)) must be submitted to Assignment Division in accordance with 37 CFR Part 3, to record the assignment in the records of the USPTO. See MPEP 302.08]

The undersigned (whose title is supplied below) is authorized to act on behalf of the assignee.

/michael garrabrants/ 3/17/2017

Signature Date

Michael S. Garrabrants IP Counsel

Printed or Typed Name Title

This collection of information is required by 37 CFR 3.73(b). The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

AO 120 (Rev. 08/10)

TO:	REPORT ON THE FILING OR DETERMINATION OF AN ACTION REGARDING A PATENT OR TRADEMARK
Mail Stop 8 Director of the U.S. Patent and Trademark Office P.O. Box 1450 Alexandria, VA 22313-1450	

In Compliance with 35 U.S.C. § 290 and/or 15 U.S.C. § 1116 you are hereby advised that a court action has been filed in the U.S. District Court Northern District of California on the following

☐ Trademarks or ☑ Patents. (☐ the patent action involves 35 U.S.C. § 292.):

DOCKET NO.	DATE FILED	U.S. DISTRICT COURT Northern District of California
PLAINTIFF Lattice Semiconductor Corporation.		DEFENDANT TECHNICOLOR SA,TECHNICOLOR, INC., TECHNICOLOR USA INC., TECHNICOLOR CONNECTED HOME USA LLC.

PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1 6,587,525	7/1/2003	Lattice Semiconductor Corporation
2 6,914,637	7/5/2005	Lattice Semiconductor Corporation
3 7,035,290	4/25/2006	Lattice Semiconductor Corporation
4 7,088,398	8/8/2006	Lattice Semiconductor Corporation
5 7,359,437	4/15/2008	Lattice Semiconductor Corporation

In the above—entitled case, the following patent(s)/ trademark(s) have been included:

DATE INCLUDED	INCLUDED BY ☐ Amendment ☐ Answer ☐ Cross Bill ☐ Other Pleading	
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1		
2		
3		
4		
5		

In the above—entitled case, the following decision has been rendered or judgement issued:

DECISION/JUDGEMENT

CLERK	(BY) DEPUTY CLERK	DATE

Copy 1—Upon initiation of action, mail this copy to Director **Copy 3—Upon termination of action, mail this copy to Director**
Copy 2—Upon filing document adding patent(s), mail this copy to Director **Copy 4—Case file copy**

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/036,234	12/24/2001	Seung Ho Hwang	SII-1000 [SIMG0115]	6063

60974 7590 03/28/2008

GIRARD & EQUITZ LLP
400 MONTGOMERY STREET
SUITE 1110
SAN FRANCISCO, CA 94104

EXAMINER	
HA, DAC V	
ART UNIT	PAPER NUMBER
2611	

MAIL DATE	DELIVERY MODE
03/28/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Supplemental Notice of Allowability	Application No. 10/036,234	Applicant(s) HWANG ET AL.	
	Examiner Dac V. Ha	Art Unit 2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *supplemental IDS filed on 08/01/07*.

2. ☒ The allowed claim(s) is/are *2-10, 27, 76-78, 11-14, 21, 25, 26, 28-32, 34-44, 81, 48, 52, 53, 56-63, 79, 80, 69, 73, 74, renumbered as 1-53, respectively*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date 08/01/07
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☐ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

SUPPLEMENTAL ACTION

1. This supplemental action is in response to the IDS filed on 08/01/07.

2. The following is a statement of reasons for the indication of allowable subject matter:

Upon consideration of IDS filed on 08/01/07, claims 2-10, 27, 76-78, 11-14, 21, 25, 26, 28-32, 34-44, 81, 48, 52, 53, 56-63, 79, 80, 69, 73, 74, renumbered as 1-53, respectively, are allowed as previously indicated.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dac V. Ha whose telephone number is 571-272-3040. The examiner can normally be reached on 4/4.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Payne can be reached on 571-272-3024. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Dac V. Ha/
Primary Examiner, Art Unit 2611

O I P E IAP17 AUG 01 2007 PATENT & TRADEMARK OFFICE
O I P E IAP17 AUG 03 2007 PATENT & TRADEMARK OFFICE

FORM PTO-1449 (Modified) U.S Dept. of Commerce (Rev. 7-80) Patent and Trademark Office **INFORMATION DISCLOSURE CITATION** (Use several sheets if necessary)	Atty Docket No. SII-1000 [SIMG0077cip1]	Appln. No. 10/036,234
	Applicant(s) SEUNG HO HWANG, et al.	
	Filing Date December 24, 2001	Group 2611

U.S. PATENT DOCUMENTS

*Examiner Initials		Document Number	Date	Name	Class	Subclass	Filing Date
/DH/	AA	5,491,479	02/13/96	Wilkinson, James H.	341	58	09/02/93
/DH/	AB	5,703,580	12/30/97	Ko, Jung-wan	341	59	07/15/96
	AC						

FOREIGN PATENT DOCUMENTS

*Examiner Initials		Document Number	Date	Country	Class	Subclass	Translation YES	NO
	AD							
	AE							

OTHER DOCUMENTS

/DH/	AF	"White Paper on the MB810 Line Code for 10GbE", Dae Young Kim, Changoo Lee, Chun Sik Shin, Hae Won Jung, and Hyeong Ho Lee, IEEE 802.3 high Speed Study Group, September 1999 Interim meeting, 09/29/99.
	AG	

Examiner	Date Considered
/Dac Ha/	03/17/2008

* Examiner: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/036,234	04/15/2008	7359437	SII-1000 [SIMG0115]	6063

60974 7590 03/26/2008

GIRARD & EQUITZ LLP
400 MONTGOMERY STREET
SUITE 1110
SAN FRANCISCO, CA 94104

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment is 1333 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site http://pair.uspto.gov for additional applicants):

Seung Ho Hwang, Palo Alto, CA;
Jano Banks, Cupertino, CA;
Paul Daniel Wolf, San Carlos, CA;
Eric Lee, San Jose, CA;
Baegin Sung, Sunnyvale, CA;
Albert M. Scalise, San Jose, CA;

Notice of Allowability	Application No.	Applicant(s)	
	10/036,234	HWANG ET AL.	
	Examiner	Art Unit	
	Dac V. Ha	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *amendment filed on 03/19/07*.

2. ☒ The allowed claim(s) is/are *2-10, 27, 76-78, 11-14, 21, 25-26, 28-32, 34-44, 81, 48, 52, 53, 56-63, 79-80, 69, 73, 74, renumbered as 1-53, respectively*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

Dac V. Ha
Primary Examiner
Art Unit: 2611

DETAILED ACTION

1. This office action is in response to the amendment filed on 03/19/07.

Allowable Subject Matter

2. Claims 2-10, 27, 76-78, 11-14, 21, 25-26, 28-32, 34-44, 81, 48, 52, 53, 56-63, 79-80, 69, 73, 74, renumbered as 1-53, respectively, are allowed.

3. The following is an examiner's statement of reasons for allowance:

Applicant has amended the claims in accordance to the office action dated 11/28/06. Upon further consideration, amended claims 2-10, 11-14, 21, 25, 26, 28-32, 34-44, 48, 52, 53, 56-63, 69, 73, 74 and newly added dependent claims 76-81 are allowed. Particularly, prior art of record (closest reference, Myers – US 5, 625,644), taking individually or collectively, fails suggest a motivation for incorporating in an apparatus and method for serial link between a transmitter and receiver, including the claimed subject matter "the transmitter is coupled to receive video data and configured to generate a sequence of video code words by encoding the video data, and the transmitter is configured to transmit to the receiver over the serial link a first burst of the video code words followed by a burst of the selected code words followed by a second burst of the video code words, wherein each of the video code words is a member of the full code word set and at least one of the video code words is not a member of the robust subset" in independent claim 2 and similarly in independent claims 11, 34 (claims 3-10, 27, 76-78, 12-14, 35-44, 81) depend therefrom); "the transmitter is coupled to receive source words of the input data, where each of the source words comprises N bits, N is less than L, and N is greater than M, and the transmitter is configured to pack

the source words into M-bit words of the input data and to encode each of the M-bit words of the input data as one of the selected code words" in independent claim 21 and similarly in independent claims 48, 69; "wherein each of the selected code words is indicative of a sequence of L binary bits, and the selected code words have fewer contiguous zero bits and contiguous one bits per code word on the average than do the code words of the full code word set excluding the selected code words" in independent claim 25 and similarly in independent claims 52 & 73; "wherein each of the selected code words is indicative of a different sequence of binary bits, the transmitter is configured to transmit the sequence of selected code words to the receiver over the serial link as a sequence of rising and falling voltage transitions, and the selected code words have bit patterns that implement DC balancing by limiting voltage drift of the serial link during transmission of said sequence of selected code words to a predetermined amount" in independent claim 26 and similarly in independent claims 53 & 74; "wherein the input data determined by the burst of the selected code words can be encoded as a first conventional sequence of the code words of the full code word set, the input data determined by the second burst of the selected code words can be encoded as a second conventional sequence of the code words of the full code word set, and the input data determined by the third burst of the selected code words can be encoded as a third conventional sequence of the code words of the full code word set, and wherein said burst of the selected code words is less susceptible to inter-symbol interference during transmission over the serial link than would be the first conventional sequence, said second burst of the selected code words is less susceptible to inter-

symbol interference during transmission over the second serial link than would be the second conventional sequence, and said third burst of the selected code words is less susceptible to inter-symbol interference during transmission over the third serial link than would be the third conventional sequence" independent claim 28 (claims 29-32 depend therefrom); "generating bursts of encoded control words by encoding control bits; and transmitting over the link a first burst of the encoded control words between at-l~ first burst of the video code words and the burst of the selected code words, and a second burst of the encoded control words between the burst of the selected code words and athe second burst of the video code words" in independent claim 56 (claims 57-63, 79 – 80 depend therefrom). Thus, claims 2-10, 27, 76-78, 11-14, 21, 25-26, 28-32, 34-44, 81, 48, 52, 53, 56-63, 79-80, 69, 73, 74 are found to be novel and unobvious over prior art of record.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dac V. Ha whose telephone number is 571-272-3040. The examiner can normally be reached on 5/4.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jay Patel can be reached on 571-272-2988. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Dac V. Ha
Primary Examiner
Art Unit 2611

Issue Classification	Application/Control No.	Applicant(s)/Patent under Reexamination	
	10/036,234	HWANG ET AL.	
	Examiner	Art Unit	
	Dac V. Ha	2611	

ISSUE CLASSIFICATION

ORIGINAL					CROSS REFERENCE(S)						
CLASS				SUBCLASS	CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)					
375				240	375	240.01	240.23	246	254	296	
INTERNATIONAL CLASSIFICATION					348	423.1	470				
H	0	4	B	1/66							
				/							
				/							
				/							
				/							

(Assistant Examiner) (Date)	Dac V. Ha (Primary Examiner) (Date)	Total Claims Allowed: 53	
(Legal Instruments Examiner) (Date)		O.G. Print Claim(s): 1	O.G. Print Fig.: 2

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
	1		31		61		91		121		151		181
	2		32		62		92		122		152		182
	3		33		63		93		123		153		183
	4		34		64		94		124		154		184
	5		35		65		95		125		155		185
	6		36		66		96		126		156		186
	7		37		67		97		127		157		187
	8		38		68		98		128		158		188
	9		39		69		99		129		159		189
	10		40		70		100		130		160		190
	11		41		71		101		131		161		191
	12		42		72		102		132		162		192
	13		43		73		103		133		163		193
	14		44		74		104		134		164		194
	15		45		75		105		135		165		195
	16		46		76		106		136		166		196
	17		47		77		107		137		167		197
	18		48		78		108		138		168		198
	19		49		79		109		139		169		199
	20		50		80		110		140		170		200
	21		51		81		111		141		171		201
	22		52		82		112		142		172		202
	23		53		83		113		143		173		203
	24		54		84		114		144		174		204
	25		55		85		115		145		175		205
	26		56		86		116		146		176		206
	27		57		87		117		147		177		207
	28		58		88		118		148		178		208
	29		59		89		119		149		179		209
	30		60		90		120		150		180		210

Office Action Summary	Application No.	Applicant(s)	
	10/036,234	HWANG ET AL.	
	Examiner	Art Unit	
	Dac V. Ha	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 December 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-54 and 56-74* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-74* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *1/10/05, 10/04/04, 7/30/02*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claims 56-63 are objected to because of the following informalities:

The dependency of claims 56-63 needs to be corrected since claim 55 has been cancelled.

Claim 56, lines 3, 4, the recitation "the first burst of the video code words" should be changed to, i.e. "a first burst of a video code words" to avoid antecedent problem. Applicant is required to find and correct all other similar problem in other claims.

Appropriate correction is required.

Double Patenting

2. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

3. Claims 1-54, 56-74 are provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1-75 of copending Application No. 10/095,422. Although the conflicting claims are not identical, they are not patentably distinct from each other because despite slight different in use of claimed language, they cover essentially the same subject matter.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. **Claims 1, 33, 54** are rejected under 35 U.S.C. 102(b) as being anticipated by Myers (US 5,625,644).

Regarding claims 1, Myers discloses the claimed subject matter "a receiver; a transmitter; and a serial link between the transmitter and the receiver, wherein the transmitter is coupled to receive input data, configured to generate a sequence of selected code words by encoding the input data, and configured to transmit the sequence of selected code words to the receiver over the serial link, wherein each of the selected code words is a member of a robust subset of a full code word set, the input data can be encoded as a conventional sequence of code words of the full code word set, and the sequence of selected code words is less susceptible to inter-symbol

interference during transmission over the link than would be the conventional sequence of code words" in Fig. 2; col. 6, line 65 to col. 9, line 2, wherein the selection a "sub-set" of the code words would yield a signal with less susceptible to ISI.

Regarding claims 33, 54, see claim 1.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. **Claims 15-20, 22-24, 45-47, 49-51, 64-68, 70-72** are rejected under 35 U.S.C. 103(a) as being unpatentable over Myers.

Regarding claims 15-20, 22-24, 45-47, 49-51, 64-68, 70-72, theses claimed subject matter would have been obvious to one skilled in the art as intended use and application specific.

Allowable Subject Matter

8. **Claims 2-14, 21, 25-27, 34-44, 48, 51-53, 56-63, 69, 73-74**, are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

9. **Claims 28-32** are allowed.

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Tsang et al. (US 6,052,072) discloses System And Scheme For Maximum Transition Run Length Codes With Location Dependent Constraints.

Paterson (US 6,301,221) discloses Methods And Apparatus For Encoding Data.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dac V. Ha whose telephone number is 571-272-3040. The examiner can normally be reached on 5/4.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jay Patel can be reached on 571-272-3086. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Dac V. Ha
Primary Examiner
Art Unit 2611

Notice of References Cited	Application/Control No. 10/036,234	Applicant(s)/Patent Under Reexamination HWANG ET AL.	
	Examiner Dac V. Ha	Art Unit 2611	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-5,625,644	04-1997	Myers, David J.	375/242
*	B	US-6,052,072	04-2000	Tsang et al.	341/59
*	C	US-6,301,221	10-2001	Paterson, Kenneth Graham	370/208
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Index of Claims

Application/Control No.	Applicant(s)/Patent under Reexamination
10/036,234	HWANG ET AL.
Examiner	**Art Unit**
Dac V. Ha	2611

√	Rejected	–	(Through numeral) Cancelled	N	Non-Elected	A	Appeal
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Search Notes

Application/Control No.	Applicant(s)/Patent under Reexamination	
10/036,234	HWANG ET AL.	
Examiner	**Art Unit**	
Dac V. Ha	2611	

SEARCHED			
Class	Subclass	Date	Examiner
375	219, 220	11/16/2006	DH
	240		
	240.01		
	240.23		
	244, 246		
	253, 254		
	260, 285		
	295, 296		
	346, 348		
348	388		
	398.1		
	423.1		
	470, 476		
	477, 487		

INTERFERENCE SEARCHED			
Class	Subclass	Date	Examiner

SEARCH NOTES (INCLUDING SEARCH STRATEGY)		
	DATE	EXMR
BRS	11/16/2006	DH

Supplemental Notice of Allowability	Application No. 10/036,234	Applicant(s) HWANG ET AL.	
	Examiner Dac V. Ha	Art Unit 2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *Printer Rush dated 06/11/07*.

2. ☒ The allowed claim(s) is/are *2-10, 27, 76-78, 11-14, 21,25-26, 28-32, 34-44, 81,48, 52, 53, 56-63, 79-80,69, 73, 74, renumbered as 1-53, respectively* .

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☐ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

Dac V. Ha
Primary Examiner
Art Unit: 2611

SUPPLEMENTAL ACTION

1. This supplemental office action is to provide a copy of page 2 of the IDS filed on 07/30/02, which was inadvertently left out previously.

2. The following is a statement of reasons for the indication of allowable subject matter:

Claims 2-10, 27, 76-78, 11-14, 21,25-26, 28-32, 34-44, 81,48, 52, 53, 56-63, 79-80,69, 73, 74, renumbered as 1-53, are allowed as previously indicated.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dac V. Ha whose telephone number is 571-272-3040. The examiner can normally be reached on 4/4.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Payne can be reached on 571-272-3024. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Dac V. Ha
Primary Examiner
Art Unit 2611

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/036,234	12/24/2001	Seung Ho Hwang	SII-1000 [SIMG0115]	6063

60974 7590 03/14/2008

GIRARD & EQUITZ LLP
400 MONTGOMERY STREET
SUITE 1110
SAN FRANCISCO, CA 94104

EXAMINER	
HA, DAC V	
ART UNIT	PAPER NUMBER
2611	

MAIL DATE	DELIVERY MODE
03/14/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Supplemental Notice of Allowability	**Application No.** 10/036,234	**Applicant(s)** HWANG ET AL.	
	Examiner Dac V. Ha	**Art Unit** 2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *IDS filed on 08/01/07*.

2. ☒ The allowed claim(s) is/are *2-10, 27, 76-78, 11-14, 21, 25, 26, 28-32, 34-44, 81, 48, 52, 53, 56-63, 79, 80, 69, 73, 74, renumbered as 1-53, respectively*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
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   * Certified copies not received: _____.

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THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

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   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
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   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

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5. ☐ Notice of Informal Patent Application
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☐ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

SUPPLEMENTAL ACTION

1. This supplemental action is in response to the IDS filed on 08/01/07.

2. The following is a statement of reasons for the indication of allowable subject matter:

Upon consideration of IDS filed on 08/01/07, claims 2-10, 27, 76-78, 11-14, 21, 25, 26, 28-32, 34-44, 81, 48, 52, 53, 56-63, 79, 80, 69, 73, 74, renumbered as 1-53, respectively, are allowed as previously indicated.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dac V. Ha whose telephone number is 571-272-3040. The examiner can normally be reached on 4/4.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Payne can be reached on 571-272-3024. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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/Dac V. Ha/
Primary Examiner, Art Unit 2611

O I P E IAP17 AUG 01 2007 PATENT & TRADEMARK OFFICE
O I P E IAP17 AUG 03 2007 PATENT & TRADEMARK OFFICE

FORM PTO-1449 (Modified) U.S Dept. of Commerce (Rev. 7-80) Patent and Trademark Office	Atty Docket No.	Appln. No.
INFORMATION DISCLOSURE CITATION (Use several sheets if necessary)	SII-1000 [SIMG0077cip1]	10/036,234
	Applicant(s) SEUNG HO HWANG, et al.	
	Filing Date December 24, 2001	Group 2611

U.S. PATENT DOCUMENTS

*Examiner Initials		Document Number	Date	Name	Class	Subclass	Filing Date
/DH/	AA	5,491,479	02/13/96	Wilkinson, James H.	341	58	09/02/93
/DH/	AB	5,703,580	12/30/97	Ko, Jung-wan	341	59	07/15/96
	AC						

FOREIGN PATENT DOCUMENTS

*Examiner Initials		Document Number	Date	Country	Class	Subclass	Translation YES	NO
	AD							
	AE							

OTHER DOCUMENTS

/DH/	AF	"White Paper on the MB810 Line Code for 10GbE", Dae Young Kim, Changoo Lee, Chun Sik Shin, Hae Won Jung, and Hyeong Ho Lee, IEEE 802.3 high Speed Study Group, September 1999 Interim meeting, 09/29/99.
	AG	

Examiner	Date Considered
/Dac Ha/	03/04/2008

* Examiner: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

Girard & Equitz LLP
INTELLECTUAL PROPERTY ATTORNEYS

August 30, 2007

VIA FACSIMILE - 571-273-6500

U.S. Patent and Trademark Office
Deposit Accounts

Re: U.S. Patent Application No.: 10/036,234
Our File: SII-1000 (SIMG0115)

Dear Sir/Madam:

We recently downloaded from the USPTO website a Deposit Account Statement (copy enclosed) for our Deposit Account No. 501697, dated August 2007. This Statement shows a charge in the amount of $180 (Fee Code 1806) to our Deposit Account for the above-referenced application. The fee (with Fee Code 1806) is for filing of the Information Disclosure Statement (filed on August 1, 2007), after receipt of a Notice of Allowance. We also filed a check (our check no. 103) in the amount of $130 on August 1, 2007 with the Information Disclosure Statement ("IDS"). The attached copy of the return postcard filed with the $130 check and IDS evidences that the USPTO received the $130 check on August 3, 2007. This $130 payment should either be applied toward the $180 fee due for filing the IDS, or refunded to us.

Unless the $130 paid by check (on August 1, 2007) is refunded to us, we request that our Deposit Account be credited in the amount of $130 to correct an erroneous overcharge (in the amount of $130) of the $180 fee due (Fee Code 1806) for filing the IDS. Thank you for your attention to this matter.

Very truly yours,

GIRARD & EQUITZ L.L.P.

Alfred A. Equitz
aequitz@gelip.com

Enclosures

400 MONTGOMERY STREET, SUITE 1110 • SAN FRANCISCO, CALIFORNIA 94104 • TELEPHONE (415) 433-2250 • FACSIMILE (415) 433-2255

United States Patent and Trademark Office

Deposit Account Statement

Requested Statement Month:	August 2007
Deposit Account Number:	501697
Name:	GIRARD & EQUITZ LLP
Attention:	PHILIP GIRAD
Street Address 1:	400 MONTGOMERY STREET
Street Address 2:	SUITE 1110
City:	SAN FRANCISCO
State:	CA
Zip:	94104
Country:	UNITED STATES

DATE	SEQ	POSTING REF TXT	ATTORNEY DOCKET NBR	FEE CODE	AMT	BAL
08/02	1	10668058	PRKR-4500	2202	$25.00	$1,533.00
08/03	641	E-REPLENISHMENT		9203	-$500.00	$2,033.00
08/22	11542	77261464	OFRI-0201	7001	$325.00	$1,708.00
08/22	11620	77261481	OFRI-0201A	7001	$325.00	$1,383.00
08/28	8977	E-REPLENISHMENT		9203	-$600.00	$1,983.00
08/29	26	10036234	SII-1000 [SIMG0115]	1806	$180.00	$1,803.00
08/30	31	10642259	SII-2510 [SIMG0155]	1252	$450.00	$1,353.00
08/31	13036	E-REPLENISHMENT		9203	-$1,000.00	$2,353.00

START BALANCE	SUM OF CHARGES	SUM OF REPLENISH	END BALANCE
$1,558.00	$1,305.00	$2,100.00	$2,353.00

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PAGE 3/4 * RCVD AT 8/31/2007 1:35:16 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-6/7 * DNIS:2736500 * CSID:4154332255 * DURATION (mm-ss):01-58

Serial/Patent/Reg. No. 10/036,234 G & E File No.: SII-1000 By: AAE/jsz
In the Matter of the Application of SEUNG HO HWANG, et al.
Title/Mark: ENCODING METHOD AND SYSTEM FOR REDUCING INTER-SYMBOL INTERFERENCE EFFECTS IN TRANSMISSION OVER A SERIAL LINK
Date Mailed: August 1, 2007 Due Date:

The following has been received in the U.S. Patent and Trademark Office on the date stamped hereon:

___ Transmittal Letter
___ Patent Application _____
_____ pgs. specification including ____ pgs claims
___ Drawings _____ sheets _____ formal _____ informal
___ Oath/Declaration
___ Assignment w/ Form PTO-1595
___ Power of Attorney
___ Small Entity Declaration
X Deposit Account Authorization (in duplicate)
X Information Disclosure Statement, PTO-1449 w/ ... references
X Check $ 130
___ Amendment/Response
___ Request for Extension of Time (_____ months)(patent)
___ Terminal Disclaimer
___ Notice of Appeal
___ Appeal Brief (in triplicate)
___ Letter to Official Draftsman
___ Issue Fee Transmittal
___ Maintenance Fee Transmittal
___ Request for _____

___ Trademark (Use) Appln., Drawing and _____ Specimens
___ ITU Trademark Application and Drawing
___ _____ Request for Extension of Time (trademark)
(Notice of Allowance: _____)
___ Statement of Use/Amendment to Allege Use
___ Section 8 and 15 Declaration
___ Trademark Renewal Application and _____ Specimen
___ Opposition to _____
___ Petition for Cancellation
X Certificate of Mailing
___ Express Mail Certificate No. _____
___ Certificate under §3.73(b)
___ Certificate of Correction (PTO Form 1050)
___ Petition for _____
X Other: Return postcard

OTHER MAIL ROOM AUG 03 2007 PATENT & TRADEMARK OFFICE

FACSIMILE COVER SHEET

Girard Equitz

INTELLECTUAL PROPERTY ATTORNEYS

TO:	U.S. Patent and Trademark Office Deposit Accounts
FAX:	571-273-6500

400 Montgomery Street, Suite 1110
San Francisco, CA 94104
Telephone: (415) 433-2250
Facsimile: (415) 433-2255

FROM:	ALFRED A. EQUITZ 400 Montgomery Street, Suite 1110 San Francisco, California 94104 Telephone: (415) 433-2250 Facsimile: (415) 433-2255 Email: aequitz@gellp.com
DATE:	August 30, 2007
TIME:	
PAGES:	4 (including cover)

If you did not receive all of the pages in this fax, please contact Alfred Equitz at (415) 433-2250 x103.

OUR FILE NUMBER: SII-1000

RETURN TO aae

MESSAGE:

Deposit Account refund request is attached.

The documents accompanying this facsimile transmission contain information from the law firm of Girard & Equitz LLP which is confidential or privileged. The information is intended to be for the use of the individual or entity named on this transmission sheet. If you are not the intended recipient, be aware that any disclosure, copying, distribution or use of the contents of this faxed information is prohibited. If you have received this facsimile in error, please notify us by telephone immediately so that we can arrange for the return of the original documents to us.

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CANCELLED
GIPE IAP17 AUG 03 2007 PATENT & TRADEMARK OFFICE

PATENT

THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of

SEUNG HO HWANG, et al.

Application No. 10/036,234

Filed: December 24, 2001

For: **ENCODING METHOD AND SYSTEM FOR REDUCING INTER-SYMBOL INTERFERENCE EFFECTS IN TRANSMISSION OVER A SERIAL LINK**

Group Art Unit: 2611

Confirmation No.: 6063

Examiner: Dac V. Ha

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

400 Montgomery Street
Suite 1110
San Francisco, CA 94104
(415) 433-2250

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to Mail Stop Issue Fee, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on August 1, 2007.

GIRARD & EQUITZ LLP Date: 08/01/07

By: _____
Jacob S. Zweig

Mail Stop Issue Fee
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Applicants submit herewith patents, publications or other information [attached hereto and listed on the attached Form PTO-1449 (modified)] of which they are aware, which they believe may be material to the examination of this application and in respect of which there may be a duty to disclose in accordance with 37 CFR § 1.56.

This Information Disclosure Statement:

(a) [] accompanies the new patent application submitted herewith. 37 CFR § 1.97(a).

(b) [] is filed within three months after the filing date of the application or within three months after the date of entry of the national stage of a PCT application as set forth in 37 CFR § 1.491.

(c) [ ] as far as is known to the undersigned, is filed before the mailing date of a first Office Action on the merits.

08/02/2007 CHEGA1 00000001 10036234
01 FC:1464 130.00 OP

Adjustment date: 09/18/2007 SDIRETA1
08729/2007 RCLEMONS 00000023 501697 10036234
01 FC:1806 180.00 CR

09/18/2007 SDIRETA1 00000001 501697 10036234
01 FC:1806 50.00 DA 130.00 OP

Adjustment date: 09/18/2007 SDIRETA1
08707/2007 CNEGA1 00000001 10036234
01 FC:1464 -130.00 OP

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

60974 7590 05/22/2007

GIRARD & EQUITZ LLP
400 MONTGOMERY STREET
SUITE 1110
SAN FRANCISCO, CA 94104



Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission
I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

Jacob S. Zweig	(Depositor's name)
	(Signature)
August 7, 2007	(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/036,234	12/24/2001	Seung Ho Hwang	SII-1000 [SIMG0115]	6063

TITLE OF INVENTION: ENCODING METHOD AND SYSTEM FOR REDUCING INTER-SYMBOL INTERFERENCE EFFECTS IN TRANSMISSION OVER A SERIAL LINK

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1400	$300	$0	$1700	08/22/2007

EXAMINER	ART UNIT	CLASS-SUBCLASS
HA, DAC V	2611	375-240000

08/09/2007 MGEBREM2 00000072 10036234
01 FC:1581 1400.00 CP
02 FC:1504 300.00 CP

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) the names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 GIRARD & EQUITZ LLP
2
3

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE: SILICON IMAGE, INC.

(B) RESIDENCE: (CITY and STATE OR COUNTRY): SUNNYVALE, CALIFORNIA

Please check the appropriate assignee category or categories (will not be printed on the patent) : ☐ Individual ☒ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:
☒ Issue Fee
☒ Publication Fee (No small entity discount permitted)
☐ Advance Order - # of Copies _____

4b. Payment of Fee(s): **(Please first reapply any previously paid issue fee shown above)**
☒ A check is enclosed.
☐ Payment by credit card. Form PTO-2038 is attached.
☒ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number 50-1697 (enclose an extra copy of this form).

Deficiencies Only

5. **Change in Entity Status** (from status indicated above)
☐ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27.
☐ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature Alfred A. Equitz Date August 7, 2007

Typed or printed name Alfred A. Equitz Registration No. 30,922

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

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OIPE IAP17 AUG 03 2007 PATENT & TRADEMARK OFFICE

08-03-07

IFW 2611

PATENT

THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of

SEUNG HO HWANG, et al.

Application No. 10/036,234

Filed: December 24, 2001

For: **ENCODING METHOD AND SYSTEM FOR REDUCING INTER-SYMBOL INTERFERENCE EFFECTS IN TRANSMISSION OVER A SERIAL LINK**

Group Art Unit: 2611

Confirmation No.: 6063

Examiner: Dac V. Ha

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

400 Montgomery Street
Suite 1110
San Francisco, CA 94104
(415) 433-2250

CERTIFICATE OF MAILING

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GIRARD & EQUITZ LLP Date: 08/01/07

By: _____
Jacob S. Zweig

Mail Stop Issue Fee
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Applicants submit herewith patents, publications or other information [attached hereto and listed on the attached Form PTO-1449 (modified)] of which they are aware, which they believe may be material to the examination of this application and in respect of which there may be a duty to disclose in accordance with 37 CFR § 1.56.

This Information Disclosure Statement:

(a) [] accompanies the new patent application submitted herewith. 37 CFR § 1.97(a).

(b) [] is filed within three months after the filing date of the application or within three months after the date of entry of the national stage of a PCT application as set forth in 37 CFR § 1.491.

(c) [ ] as far as is known to the undersigned, is filed before the mailing date of a first Office Action on the merits.

08/07/2007 CHEGA1 00000001 10036234
01 FC:1464 130.00 OP

(d) [] is filed after the first office action and more than three months after the application's filing date or PCT national stage date of entry filing but, as far as is known to the undersigned, prior to the mailing date of either a final rejection or a notice of allowance, whichever occurs first, and is accompanied by either the fee ($180) set forth in 37 CFR § 1.17(p) **or** a certification as specified in 37 CFR § 1.97(e), as checked below.

(e) [X] is filed after the mailing date of either a final rejection or a notice of allowance, whichever occurred first, and the Issue Fee has not been paid, and is accompanied by the fee ($130) set forth in 37 CFR § 1.17(i)(1) and a certification as specified in 37 CFR § 1.97(e), as checked below. This document is to be considered as a petition requesting consideration of the information disclosure statement.

[If either of boxes (d) or (e) are checked above, the following "certification" under 37 CFR § 1.97(e) may need to be completed.] The undersigned certifies that:

(f) [X] Each item of information contained in the information disclosure statement was cited in a communication mailed from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this information disclosure statement.

(g) [] No item of information contained in this information disclosure statement was cited in a communication mailed from a foreign patent office in a counterpart foreign application or, to the knowledge of the undersigned after making reasonable inquiry, was known to any individual designated in 37 CFR § 1.56(c) more than three months prior to the filing of this information disclosure statement.

A list of the patent(s) or publication(s) is set forth on the attached Form PTO-1449 (Modified).

A copy of the items on PTO-1449 (Modified) is supplied herewith:

(h) [ ] each (i) [] none (j) [X] all except for U.S. Patent documents.

A concise explanation of relevance of the items listed on form PTO-1449 (Modified) is that each listed item was cited in an International Search report (copy attached) issued in a corresponding PCT

International Application. The Search Report refers to relevent portions of the references.

While the information and references disclosed in this Information Disclosure Statement may be "material" pursuant to 37 CFR § 1.56, it is not intended to constitute an admission that any patent, publication or other information referred to therein is "prior art" for this invention unless specifically designated as such.

In accordance with 37 CFR §.1.97(g), the filing of this Information Disclosure Statement shall not be construed to mean that a search has been made or that no other material information as defined in 37 CFR § 1.56(a) exists. It is submitted that the Information Disclosure Statement is in compliance with 37 CFR § 1.98 and MPEP § 609 and the Examiner is respectfully requested to consider the listed references.

[X] The Commissioner is hereby authorized to charge our Deposit Account No. **50-1697** for any fees required in connection with the filing of this Information Disclosure Statement. **A duplicate copy of this Notice is enclosed for this purpose.**

Respectfully submitted,

Dated: 8/1/07 By _____

Alfred A. Equitz
Registration No. 30,922
Tel. No. 415/433-2250

Our File: SII-1000 [SIMG0077cip1]

O I P E IAP17 AUG 01 2007 PATENT & TRADEMARK OFFICE
O I P E IAP17 AUG 03 2007 PATENT & TRADEMARK OFFICE

FORM PTO-1449 (Modified) U.S Dept. of Commerce (Rev. 7-80) Patent and Trademark Office	Atty Docket No.	Appln. No.
INFORMATION DISCLOSURE CITATION (Use several sheets if necessary)	SII-1000 [SIMG0077cip1]	10/036,234
	Applicant(s) SEUNG HO HWANG, et al.	
	Filing Date December 24, 2001	Group 2611

U.S. PATENT DOCUMENTS

*Examiner Initials		Document Number	Date	Name	Class	Subclass	Filing Date
	AA	5,491,479	02/13/96	Wilkinson, James H.	341	58	09/02/93
	AB	5,703,580	12/30/97	Ko, Jung-wan	341	59	07/15/96
	AC						

FOREIGN PATENT DOCUMENTS

*Examiner Initials		Document Number	Date	Country	Class	Subclass	Translation YES	NO
	AD							
	AE							

OTHER DOCUMENTS

	AF	"White Paper on the MB810 Line Code for 10GbE", Dae Young Kim, Changoo Lee, Chun Sik Shin, Hae Won Jung, and Hyeong Ho Lee, IEEE 802.3 high Speed Study Group, September 1999 Interim meeting, 09/29/99.
	AG	

Examiner	Date Considered

* Examiner: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/036,234	12/24/2001	Seung Ho Hwang	SII-1000 [SIMG0115]	6063

60974 7590 07/13/2007

GIRARD & EQUITZ LLP
400 MONTGOMERY STREET
SUITE 1110
SAN FRANCISCO, CA 94104

EXAMINER	
HA, DAC V	

ART UNIT	PAPER NUMBER
2611	

MAIL DATE	DELIVERY MODE
07/13/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

SF

Supplemental Notice of Allowability	Application No. 10/036,234	Applicant(s) HWANG ET AL.	
	Examiner Dac V. Ha	Art Unit 2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *Printer Rush dated 06/11/07*.

2. ☒ The allowed claim(s) is/are *2-10, 27, 76-78, 11-14, 21,25-26, 28-32, 34-44, 81,48, 52, 53, 56-63, 79-80,69, 73, 74, renumbered as 1-53, respectively*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☐ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

Dac V. Ha
Primary Examiner
Art Unit: 2611

SUPPLEMENTAL ACTION

1. This supplemental office action is to provide a copy of page 2 of the IDS filed on 07/30/02, which was inadvertently left out previously.

2. The following is a statement of reasons for the indication of allowable subject matter:

Claims 2-10, 27, 76-78, 11-14, 21,25-26, 28-32, 34-44, 81,48, 52, 53, 56-63, 79-80,69, 73, 74, renumbered as 1-53, are allowed as previously indicated.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dac V. Ha whose telephone number is 571-272-3040. The examiner can normally be reached on 4/4.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Payne can be reached on 571-272-3024. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.



Dac V. Ha
Primary Examiner
Art Unit 2611

FORM PTO-1449 (Modified) U.S Dept. of Commerce (Rev. 7-80) Patent and Trademark Office **INFORMATION DISCLOSURE CITATION** (Use several sheets if necessary)	Atty Docket No. SII-1000 [SIMG0115]	Appln. No. 10/036,234
	Applicant(s) SEUNG HO HWANG, et al.	
	Filing Date December 24, 2001	Group 2614

JUL 30 2002 PATENT & TRADEMARK OFFICE

RECEIVED AUG 05 2002 Technology Center 2600

U.S. PATENT DOCUMENTS

*Examiner Initials		Document Number	Date	Name	Class	Subclass	Filing Date
	AA	5,974,464	10/26/99	SHIN et al.	709	231	09/30/96
	BB	5,905,769	05/18/99	LEE et al.	375	376	05/07/96
	CC	6,191,822 B1	02/20/01	SMYERS	348	552	06/20/97
	DD	5,506,932	04/09/96	HOLMES et al.	395	2.14	04/16/93
	EE	5,541,662	07/30/96	ADAMS et al.	348	460	09/30/94
	FF	5,523,795	06/04/96	UEDA	348	480	08/16/94
	GG	5,150,211	09/22/92	CHARBONNEL et al.	358	143	08/28/90
	HH	5,199,030	03/30/93	UEDA	370	68	09/05/91
	II	5,940,070	08/17/99	KOO	345	302	05/13/96

FOREIGN PATENT DOCUMENTS

*Examiner Initials		Document Number	Date	Country	Class	Subclass	Translation YES	Translation NO
	JJ	WO 00/16525	23.03.2000	PCT	H04L	25/02		

OTHER DOCUMENTS

	KK	*High-Bandwidth Digital Content Protection System,* Revision 1.0, by Intel Corporation, February 17, 2000, pages 1-60.

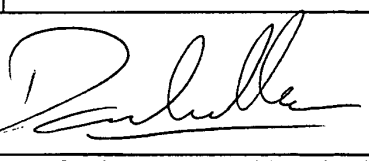
Examiner	Date Considered

* Examiner: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

FORM PTO-1449 (Modified) U.S Dept. of Commerce (Rev. 7-80) Patent and Trademark Office **INFORMATION DISCLOSURE CITATION** (Use several sheets if necessary)	Atty Docket No. SII-1000 [SIMG0115]	Appln. No. 10/036,234
JUL 30 2002 TECHNOLOGY CENTER 2600	Applicant(s) SEUNG HO HWANG, et al.	
	Filing Date December 24, 2001	Group ~~2614~~ 2611

OTHER DOCUMENTS

DH	NN	*High-Bandwith Digital Content Protection System Revision 1.0 Erratum,* by Intel Corporation, March 19, 2001, pages 1-9.
DH	OO	*Upstream Link for High-bandwidth Digital Content Protection,* Revision 1.00, by Intel Corporation, January 26, 2001, pages 1-38.
DH	PP	Lieberman, David "*PC Video Interface Looks to Add Audio Capability*", EE Times (03/26/01, 11:57 a.m. EST), pages 1-3, downloaded from the Internet on May 23, 2001 from http://www.eetimes.com/story/OEG20010326S0029.
DH	QQ	Silicon Image, Inc., "*Silicon Image First to Couple Digital Audio and Video on the DVI Link*", Sunnyvale, January 16, 2001, pages 1-4, downloaded from the Internet on May 22, 2001 from http://www.siimage.com/press/01_16_01.asp.
DH	RR	Silicon Image, Inc., "*CE Industry Heavyweights Proclaim DVI HDCP as the Interface for HDTV-Further Propelling Silicon Image into the CE Space*", Las Vegas, January 4, 2001, pages 1-4, downloaded from the Internet on May 22, 2001 from http://www.siimage.com/press/01_04_01a.asp.
	SS	

Examiner	Date Considered
	11/16/06

* Examiner: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

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BIBDATASHEET

Bib Data Sheet

CONFIRMATION NO. 6063

SERIAL NUMBER	FILING OR 371(c) DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
10/036,234	12/24/2001 RULE	375	2611	SII-1000 [SIMG0115]

APPLICANTS

Seung Ho Hwang, Palo Alto, CA;
Jano Banks, Cupertino, CA;
Paul Daniel Wolf, San Carlos, CA;
Eric Lee, San Jose, CA;
Baegin Sung, Sunnyvale, CA;
Albert M. Scalise, San Jose, CA;

JB 6/11

**** CONTINUING DATA ***************************

This application is a CIP of 09/954,663 09/12/2001

**** FOREIGN APPLICATIONS ********************

IF REQUIRED, FOREIGN FILING LICENSE GRANTED
** 02/06/2002

		STATE OR COUNTRY	SHEETS DRAWING	TOTAL CLAIMS	INDEPENDENT CLAIMS
Foreign Priority claimed	☐ yes ☐ no	CA	5	79	4
35 USC 119 (a-d) conditions met	☐ yes ☐ no ☐ Met after Allowance				
Verified and Acknowledged	Examiner's Signature Initials				

ADDRESS
60974

TITLE
ENCODING METHOD AND SYSTEM FOR REDUCING INTER-SYMBOL INTERFERENCE EFFECTS IN TRANSMISSION OVER A SERIAL LINK

FILING FEE RECEIVED		
4016	FEES: Authority has been given in Paper No. _____ to charge/credit DEPOSIT ACCOUNT No. _____ for following:	☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit

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NOTICE OF ALLOWANCE AND FEE(S) DUE

60974 7590 05/22/2007

GIRARD & EQUITZ LLP
400 MONTGOMERY STREET
SUITE 1110
SAN FRANCISCO, CA 94104

EXAMINER	
HA, DAC V	
ART UNIT	PAPER NUMBER
2611	

DATE MAILED: 05/22/2007

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/036,234	12/24/2001	Seung Ho Hwang	SII-1000 [SIMG0115]	6063

TITLE OF INVENTION: ENCODING METHOD AND SYSTEM FOR REDUCING INTER-SYMBOL INTERFERENCE EFFECTS IN TRANSMISSION OVER A SERIAL LINK

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1400	$300	$0	$1700	08/22/2007

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the SMALL ENTITY status shown above.

If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:

A. If the status is the same, pay the TOTAL FEE(S) DUE shown above.

B. If the status above is to be removed, check box 5b on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and twice the amount of the ISSUE FEE shown above, or

If the SMALL ENTITY is shown as NO:

A. Pay TOTAL FEE(S) DUE shown above, or

B. If applicant claimed SMALL ENTITY status before, or is now claiming SMALL ENTITY status, check box 5a on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and 1/2 the ISSUE FEE shown above.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PTOL-85 (Rev. 07/06) Approved for use through 05/31/2007.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

60974 7590 05/22/2007

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SAN FRANCISCO, CA 94104

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission
I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/036,234	12/24/2001	Seung Ho Hwang	SII-1000 [SIMG0115]	6063

TITLE OF INVENTION: ENCODING METHOD AND SYSTEM FOR REDUCING INTER-SYMBOL INTERFERENCE EFFECTS IN TRANSMISSION OVER A SERIAL LINK

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1400	$300	$0	$1700	08/22/2007

EXAMINER	ART UNIT	CLASS-SUBCLASS
HA, DAC V	2611	375-240000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) the names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.
1 _____
2 _____
3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ☐ Individual ☐ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:
☐ Issue Fee
☐ Publication Fee (No small entity discount permitted)
☐ Advance Order - # of Copies _____

4b. Payment of Fee(s): **(Please first reapply any previously paid issue fee shown above)**
☐ A check is enclosed.
☐ Payment by credit card. Form PTO-2038 is attached.
☐ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)
☐ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27. ☐ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
HA, DAC V	
ART UNIT	PAPER NUMBER
2611	

DATE MAILED: 05/22/2007

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 1355 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 1355 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

PTOL-85 (Rev. 07/06) Approved for use through 05/31/2007.

Notice of Allowability	Application No.	Applicant(s)	
	10/036,234	HWANG ET AL.	
	Examiner	Art Unit	
	Dac V. Ha	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *amendment filed on 03/19/07*.

2. ☒ The allowed claim(s) is/are *2-10, 27, 76-78, 11-14, 21, 25-26, 28-32, 34-44, 81, 48, 52, 53, 56-63, 79-80, 69, 73, 74, renumbered as 1-53, respectively*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

Dac V. Ha
Primary Examiner
Art Unit: 2611

DETAILED ACTION

1. This office action is in response to the amendment filed on 03/19/07.

Allowable Subject Matter

2. Claims 2-10, 27, 76-78, 11-14, 21, 25-26, 28-32, 34-44, 81, 48, 52, 53, 56-63, 79-80, 69, 73, 74, renumbered as 1-53, respectively, are allowed.

3. The following is an examiner's statement of reasons for allowance:

Applicant has amended the claims in accordance to the office action dated 11/28/06. Upon further consideration, amended claims 2-10, 11-14, 21, 25, 26, 28-32, 34-44, 48, 52, 53, 56-63, 69, 73, 74 and newly added dependent claims 76-81 are allowed. Particularly, prior art of record (closest reference, Myers – US 5, 625,644), taking individually or collectively, fails suggest a motivation for incorporating in an apparatus and method for serial link between a transmitter and receiver, including the claimed subject matter "the transmitter is coupled to receive video data and configured to generate a sequence of video code words by encoding the video data, and the transmitter is configured to transmit to the receiver over the serial link a first burst of the video code words followed by a burst of the selected code words followed by a second burst of the video code words, wherein each of the video code words is a member of the full code word set and at least one of the video code words is not a member of the robust subset" in independent claim 2 and similarly in independent claims 11, 34 (claims 3-10, 27, 76-78, 12-14, 35-44, 81) depend therefrom); "the transmitter is coupled to receive source words of the input data, where each of the source words comprises N bits, N is less than L, and N is greater than M, and the transmitter is configured to pack

the source words into M-bit words of the input data and to encode each of the M-bit words of the input data as one of the selected code words" in independent claim 21 and similarly in independent claims 48, 69; "wherein each of the selected code words is indicative of a sequence of L binary bits, and the selected code words have fewer contiguous zero bits and contiguous one bits per code word on the average than do the code words of the full code word set excluding the selected code words" in independent claim 25 and similarly in independent claims 52 & 73; "wherein each of the selected code words is indicative of a different sequence of binary bits, the transmitter is configured to transmit the sequence of selected code words to the receiver over the serial link as a sequence of rising and falling voltage transitions, and the selected code words have bit patterns that implement DC balancing by limiting voltage drift of the serial link during transmission of said sequence of selected code words to a predetermined amount" in independent claim 26 and similarly in independent claims 53 & 74; "wherein the input data determined by the burst of the selected code words can be encoded as a first conventional sequence of the code words of the full code word set, the input data determined by the second burst of the selected code words can be encoded as a second conventional sequence of the code words of the full code word set, and the input data determined by the third burst of the selected code words can be encoded as a third conventional sequence of the code words of the full code word set, and wherein said burst of the selected code words is less susceptible to inter-symbol interference during transmission over the serial link than would be the first conventional sequence, said second burst of the selected code words is less susceptible to inter-

symbol interference during transmission over the second serial link than would be the second conventional sequence, and said third burst of the selected code words is less susceptible to inter-symbol interference during transmission over the third serial link than would be the third conventional sequence" independent claim 28 (claims 29-32 depend therefrom); "generating bursts of encoded control words by encoding control bits; and transmitting over the link a first burst of the encoded control words between at- l~ first burst of the video code words and the burst of the selected code words, and a second burst of the encoded control words between the burst of the selected code words and athe second burst of the video code words" in independent claim 56 (claims 57-63, 79 – 80 depend therefrom). Thus, claims 2-10, 27, 76-78, 11-14, 21, 25-26, 28-32, 34-44, 81, 48, 52, 53, 56-63, 79-80, 69, 73, 74 are found to be novel and unobvious over prior art of record.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dac V. Ha whose telephone number is 571-272-3040. The examiner can normally be reached on 5/4.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jay Patel can be reached on 571-272-2988. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.



Dac V. Ha
Primary Examiner
Art Unit 2611

Issue Classification	Application/Control No.	Applicant(s)/Patent under Reexamination	
	10/036,234	HWANG ET AL.	
	Examiner	Art Unit	
	Dac V. Ha	2611	

ISSUE CLASSIFICATION

ORIGINAL					CROSS REFERENCE(S)						
CLASS				SUBCLASS	CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)					
375				240	375	240.01	240.23	246	254	296	
INTERNATIONAL CLASSIFICATION					348	423.1	470				
H	0	4	B	1/66							
				/							
				/							
				/							
				/							

(Assistant Examiner) (Date)

(Legal Instruments Examiner) (Date)

5/11/07

Dac V. Ha

(Primary Examiner) (Date)

Total Claims Allowed: 53

O.G. Print Claim(s)	O.G. Print Fig.
1	2

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☒ T.D. ☐ R.1.47

Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
	1	24	31	46	61		91		121		151		181
1	(2)	25	32	47	62		92		122		152		182
2	3		~~33~~	48	63		93		123		153		183
3	4	26	(34)		64		94		124		154		184
4	5	27	35		65		95		125		155		185
5	6	28	36		66		96		126		156		186
6	7	29	37		67		97		127		157		187
7	8	30	38		68		98		128		158		188
8	9	31	39	51	(69)		99		129		159		189
9	10	32	40		70		100		130		160		190
14	(11)	33	41		71		101		131		161		191
15	12	34	42		72		102		132		162		192
16	13	35	43	52	(73)		103		133		163		193
17	14	36	44	53	(74)		104		134		164		194
	15		45		~~75~~		105		135		165		195
	16		46	11	76		106		136		166		196
	17		47	12	77		107		137		167		197
	18	38	(48)	13	78		108		138		168		198
	19		49	49	79		109		139		169		199
	20		50	50	80		110		140		170		200
18	(21)		51	37	81		111		141		171		201
	22	39	(52)		82		112		142		172		202
	23	40	(53)		83		113		143		173		203
	24		54		84		114		144		174		204
19	(25)		55		85		115		145		175		205
20	(26)	41	(56)		86		116		146		176		206
10	27	42	57		87		117		147		177		207
21	(28)	43	58		88		118		148		178		208
22	29	44	59		89		119		149		179		209
23	30	45	60		90		120		150		180		210

U.S. Patent and Trademark Office

Part of Paper No. 20070506

Index of Claims

Application/Control No.	Applicant(s)/Patent under Reexamination
10/036,234	HWANG ET AL.
Examiner	**Art Unit**
Dac V. Ha	2611

√	Rejected	–	(Through numeral) Cancelled	N	Non-Elected	A	Appeal
=	Allowed	+	Restricted	I	Interference	O	Objected

Claim Final	Claim Original	11/16/06	5/11/07
	(1)	√	
1	(2)		=
2	3		
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38	(48)		=
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Claim Final	Claim Original	11/16/06	5/11/07
	~~51~~	√	
39	(52)	√	=
40	(53)	√	=
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41	(56)	√	=
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52	(73)		=
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Claim Final	Claim Original	Date
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Bib Data Sheet

CONFIRMATION NO. 6063

SERIAL NUMBER	FILING OR 371(c) DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
10/036,234	12/24/2001 RULE	375	2611	SII-1000 [SIMG0115]

APPLICANTS

Seung Ho Hwang, Palo Alto, CA;
Jano Banks, Cupertino, CA;
Paul Daniel Wolf, San Carlos, CA;
Eric Lee, San Jose, CA;
Baegin Sung, Sunnyvale, CA;

** CONTINUING DATA **********

This application is a CIP of 09/954,663 09/12/2001 OK! DH

** FOREIGN APPLICATIONS **********

NONE! DH

IF REQUIRED, FOREIGN FILING LICENSE GRANTED
** 02/06/2002 OK! DH

		STATE OR COUNTRY	SHEETS DRAWING	TOTAL CLAIMS	INDEPENDENT CLAIMS
Foreign Priority claimed	☐ yes ☑ no	CA	5	53	4
35 USC 119 (a-d) conditions met	☐ yes ☑ no ☐ Met after Allowance				
Verified and Acknowledged	Examiner's Signature / Initials				

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60974

TITLE
Encoding method and system for reducing inter-symbol interference effects in transmission over a serial link

FILING FEE RECEIVED	FEES: Authority has been given in Paper	
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Search Notes

Application/Control No.	Applicant(s)/Patent under Reexamination
10/036,234	HWANG ET AL.
Examiner	**Art Unit**
Dac V. Ha	2611

SEARCHED			
Class	Subclass	Date	Examiner
375	219, 220	11/16/2006	DH
	240		
	240.01		
	240.23		
	244, 246		
	253, 254		
	260, 285		
	295, 296		
	346, 348		
348	388		
	398.1		
	423.1		
	470, 476		
	477, 487		

INTERFERENCE SEARCHED			
Class	Subclass	Date	Examiner
* Same as above		5/6/07	DH

SEARCH NOTES (INCLUDING SEARCH STRATEGY)		
	DATE	EXMR
BRS	11/16/2006	DH
* Update	5/06/07	DH

Application Number	Application/Control No.	Applicant(s)/Patent under Reexamination	
	10/036,234	HWANG ET AL.	

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TERMINAL DISCLAIMER	☒ APPROVED	☐ DISAPPROVED
Date Filed : 3/19/07	This patent is subject to a Terminal Disclaimer	

Approved/Disapproved by:
andre ROBINSON

U.S. Patent and Trademark Office



THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of

SEUNG HO HWANG, et al.

Application No. 10/036,234

Filed: December 24, 2001

For: **ENCODING METHOD AND SYSTEM FOR REDUCING INTER-SYMBOL INTERFERENCE EFFECTS IN TRANSMISSION OVER A SERIAL LINK**

Group Art Unit: 2611

Confirmation No.: 6063

Examiner: Dac V. Ha

RESPONSE TO OFFICE ACTION MAILED ON NOVEMBER 28, 2006

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CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to Mail Stop Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on March 15, 2007.

GIRARD & EQUITZ LLP Date: 03/15/07

By: _____
Jacob S. Zweig

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

This is in response to the Office Action mailed on November 28, 2006.

Amend the claims to read as in the listing of claims which begins on page 2 of this paper.

Remarks begin at page 15 of this paper.

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LISTING OF CLAIMS:

The following listing of claims will replace all prior versions, and listings, of claims in the application:

1. (canceled)

2. (currently amended) ~~The system of claim 1~~ A communication system, including:

a receiver;

a transmitter; and

a serial link between the transmitter and the receiver, wherein the transmitter is coupled to receive input data, configured to generate a sequence of selected code words by encoding the input data, and configured to transmit the sequence of selected code words to the receiver over the serial link, wherein each of the selected code words is a member of a robust subset of a full code word set, the input data can be encoded as a conventional sequence of code words of the full code word set, and the sequence of selected code words is less susceptible to inter-symbol interference during transmission over the link than would be the conventional sequence of code words, wherein the input data are auxiliary data, the transmitter is coupled to receive video data and configured to generate a sequence of video code words by encoding the video data, and the transmitter is configured to transmit to the receiver over the serial link a first burst of the video code words followed by a burst of the selected code words followed by a second burst of the video code words, wherein each of the video code words is a member of the full code word set and at least one of the video code words is not a member of the robust subset.

3. (original) The system of claim 2, wherein the transmitter is also coupled to receive control bits, configured to generate bursts of encoded control words by encoding the control bits, and configured to transmit to the receiver over the serial link a first burst of the encoded control words between the first burst of the video code words and the burst of the selected code words, and a second burst of the encoded control words between the burst of the selected code words and the second burst of the video code words.

4. (original) The system of claim 3, wherein the selected code words include at least one guard band word, the burst of the selected code words has an initial word, and the initial word is the guard band word.

5. (original) The system of claim 3, wherein the selected code words include at least one guard

band word, the burst of the selected code words has an initial set of words, and each word of the initial set of words is one said guard band word.

6. (original) The system of claim 3, wherein the selected code words include at least one guard band word, the burst of the selected code words has a final word, and the final word is the guard band word.

7. (original) The system of claim 3, wherein the selected code words include at least one guard band word, the burst of the selected code words has a final set of words, and each word of the final set of words is one said guard band word.

8. (original) The system of claim 3, wherein the serial link is a TMDS link, and the selected code words consist of seventeen different, transition-minimized TMDS code words, including at least one transition-minimized TMDS code word used as a guard band word.

9. (original) The system of claim 3, wherein the selected code words include at least two guard band words, including a first guard band word and a second guard band word, the second burst of the video code words has an initial word, the initial word of the second burst of the video code words is the first guard band word, the burst of the selected code words has an initial word, and the initial word of the burst of the selected code words is the second guard band word.

10. (original) The system of claim 9, wherein the serial link is a TMDS link, and the selected code words consist of seventeen different, transition-minimized TMDS code words, including one transition-minimized TMDS code word used only as said second guard band word and another transition-minimized TMDS code word used as said first guard band and also used as one of the selected code words in said burst of the selected code words.

11. (currently amended) ~~The system of claim 1~~ A communication system, including:

a receiver;

a transmitter; and

a serial link between the transmitter and the receiver, wherein the transmitter is coupled to receive input data, configured to generate a sequence of selected code words by encoding the input data, and configured to transmit the sequence of selected code words to the receiver over the serial link, wherein each of the selected code words is a member of a robust subset of a full code word set, the input data can be encoded as a conventional sequence of code words of the full code word set,

and the sequence of selected code words is less susceptible to inter-symbol interference during transmission over the link than would be the conventional sequence of code words, wherein the input data are auxiliary data, the transmitter is coupled to receive video data and configured to generate a sequence of video code words by encoding the video data, and the transmitter is configured to transmit to the receiver over the serial link a burst of the selected code words followed by a burst of the video code words, wherein each of the video code words is a member of the full code word set and at least one of the video code words is not a member of the robust subset.

12. (original) The system of claim 11, wherein the transmitter is also coupled to receive control bits, configured to generate bursts of encoded control words by encoding the control bits, and configured to transmit to the receiver over the serial link a burst of the encoded control words between the burst of the selected code words and the burst of the video code words.

13. (original) The system of claim 12, wherein the selected code words include at least one guard band word, the burst of the video code words has an initial word, and the initial word is the guard band word.

14. (original) The system of claim 12, wherein the selected code words include at least one guard band word, the burst of the video code words has an initial set of words, and each word of the initial set of words is one said guard band word.

15-20. (canceled)

21. (currently amended) ~~The system of claim 19~~ A communication system, including:

a receiver;

a transmitter; and

a serial link between the transmitter and the receiver, wherein the transmitter is coupled to receive input data, configured to generate a sequence of selected code words by encoding the input data, and configured to transmit the sequence of selected code words to the receiver over the serial link, wherein each of the selected code words is a member of a robust subset of a full code word set, the input data can be encoded as a conventional sequence of code words of the full code word set, and the sequence of selected code words is less susceptible to inter-symbol interference during transmission over the link than would be the conventional sequence of code words, wherein each of the selected code words is an L-bit binary word, each of at least a subset of the selected code words is indicative of an M-bit word of the input data, L = 10, M = 4, and the transmitter is coupled to receive source words of the input data, where each of the source words comprises N bits, N is less than L, and N is greater than M, and the transmitter is configured to pack the source words into M-bit words of the input data and to encode each of the M-bit words of the input data as one of the selected code words.

22-24. (canceled)

25. (currently amended) ~~The system of claim 1~~ A communication system, including:

a receiver;

a transmitter; and

a serial link between the transmitter and the receiver, wherein the transmitter is coupled to receive input data, configured to generate a sequence of selected code words by encoding the input data, and configured to transmit the sequence of selected code words to the receiver over the serial link, wherein each of the selected code words is a member of a robust subset of a full code word set, the input data can be encoded as a conventional sequence of code words of the full code word set, and the sequence of selected code words is less susceptible to inter-symbol interference during transmission over the link than would be the conventional sequence of code words, wherein each of the selected code words is indicative of a sequence of L binary bits, and the selected code words have fewer contiguous zero bits and ~~continuous~~ contiguous one bits per code word on the average than do the code words of the full code word set excluding the selected code words.

26. (currently amended) ~~The system of claim 1~~ A communication system, including:

a receiver;

a transmitter; and

a serial link between the transmitter and the receiver, wherein the transmitter is coupled to receive input data, configured to generate a sequence of selected code words by encoding the input data, and configured to transmit the sequence of selected code words to the receiver over the serial link, wherein each of the selected code words is a member of a robust subset of a full code word set, the input data can be encoded as a conventional sequence of code words of the full code word set, and the sequence of selected code words is less susceptible to inter-symbol interference during transmission over the link than would be the conventional sequence of code words, wherein each of the selected code words is indicative of a different sequence of binary bits, the transmitter is configured to transmit the sequence of selected code words to the receiver over the serial link as a sequence of rising and falling voltage transitions, and the selected code words have bit patterns that implement DC balancing by limiting voltage drift of the serial link during transmission of said sequence of selected code words to a predetermined amount.

27. (currently amended) The system of claim 2~~1~~, wherein the input data are auxiliary data, the transmitter is coupled to receive video data and configured to generate a sequence of video code words by encoding the video data, and the transmitter is configured to transmit to the receiver over the serial link the~~a~~ first burst of the video code words followed by at least two bursts of the selected code words followed by the~~a~~ second burst of the video code words~~, wherein each of the video code words is a member of the full code word set and at least one of the video code words is not a member of the robust subset~~.

28. (original) A communication system, including:

a receiver;

a transmitter; and

a serial link, a second serial link, and a third serial link between the transmitter and the receiver, wherein the transmitter is coupled to receive input data and video data, configured to generate sequences of selected code words by encoding the input data and to generate sequences of video code words by encoding the video data, and configured to transmit to the receiver over the serial link a burst of the selected code words followed by a burst of the video code words, to transmit to the receiver over the second serial link a second burst of the selected code words followed by a second burst of the video code words, and to transmit to the receiver over the third serial link a third burst of the selected code words followed by a third burst of the video code words,

wherein each of the selected code words is a member of a robust subset of a full code word set, each of the video code words is a member of the full code word set, and at least one of the video code words is not a member of the robust subset, and

wherein the input data determined by the burst of the selected code words can be encoded as a first conventional sequence of the code words of the full code word set, the input data determined by the second burst of the selected code words can be encoded as a second conventional sequence of the code words of the full code word set, and the input data determined by the third burst of the selected code words can be encoded as a third conventional sequence of the code words of the full code word set, and wherein said burst of the selected code words is less susceptible to inter-symbol interference during transmission over the serial link than would be the first conventional sequence, said second burst of the selected code words is less susceptible to inter-symbol interference during transmission over the second serial link than would be the second conventional sequence, and said third burst of the selected code words is less susceptible to inter-symbol interference during transmission over the third serial link than would be the third conventional sequence.

29. (original) The system of claim 28, wherein the transmitter is also coupled to receive control bits, configured to generate sequences of encoded control words by encoding the control bits, and configured to transmit to the receiver over the serial link a burst of the encoded control words between the burst of the selected code words and the burst of the video code words, to transmit to the receiver over the second serial link a second burst of the encoded control words between the second burst of the selected code words and the second burst of the video code words, and to transmit to the receiver over the third serial link a third burst of the encoded control words between the third burst of the selected code words and the third burst of the video code words.

30. (original) The system of claim 28, wherein the serial link is a first video channel of a TMDS link, the second serial link is a second video channel of the TMDS link, and the third serial link is a third video channel of the TMDS link.

31. (currently amended) The system of claim 30, wherein the selected code words consist of seventeen different TMDS code words, including at least one TMDS code word used only as a guard band word.

32. (currently amended) The system of claim 30, wherein the selected code words consist of seventeen, different, transition-minimized TMDS code words, including at least one transition-minimized TMDS code word used only as a guard band word.

33. (canceled)

34. (currently amended) ~~The transmitter of claim 33~~ A transmitter for use in data transmission over a serial link, said transmitter including:

at least one input for receiving input data;

an output configured to be coupled to a channel of the link; and

circuitry, coupled to each said input and to the output, and configured to generate a sequence of selected code words by encoding the input data and to assert the sequence of selected code words to the output in response to the input data, wherein each of the selected code words is a member of a robust subset of a full code word set, the input data can be encoded as a conventional sequence of code words of the full code word set, and the sequence of selected code words is less susceptible to inter-symbol interference during transmission over the link than would be the conventional sequence of code words, wherein the input data include auxiliary data and video data, and the circuitry is configured to generate a sequence of video code words by encoding the video data, and to assert to the output a first burst of the video code words followed by a burst of the selected code words followed by a second burst of the video code words, wherein each of the video code words is a member of the full code word set and at least one of the video code words is not a member of the robust subset.

35. (original) The transmitter of claim 34, wherein the circuitry is also coupled to receive control bits, configured to generate bursts of encoded control words by encoding the control bits, and to assert to the output a first burst of the encoded control words between the first burst of the video code words and the burst of the selected code words, and a second burst of the encoded control words between the burst of the selected code words and the second burst of the video code words.

36. (original) The transmitter of claim 35, wherein the selected code words include at least one guard band word, the burst of the selected code words has an initial word, and the initial word is the guard band word.

37. (original) The transmitter of claim 35, wherein the selected code words include at least one guard band word, the burst of the selected code words has an initial set of words, and each word of the initial set of words is one said guard band word.

38. (original) The transmitter of claim 35, wherein the selected code words include at least one

guard band word, the burst of the selected code words has a final word, and the final word is the guard band word.

39. (original) The transmitter of claim 35, wherein the selected code words include at least one guard band word, the burst of the selected code words has a final set of words, and each word of the final set of words is one said guard band word.

40. (original) The transmitter of claim 35, wherein the serial link is a TMDS link, and the selected code words consist of seventeen different, transition-minimized TMDS code words, including at least one transition-minimized TMDS code word used as a guard band word.

41. (original) The transmitter of claim 35, wherein the selected code words include at least two guard band words, including a first guard band word and a second guard band word, the second burst of the video code words has an initial word, the initial word of the second burst of the video code words is the first guard band word, the burst of the selected code words has an initial word, and the initial word of the burst of the selected code words is the second guard band word.

42. (original) The transmitter of claim 41, wherein the serial link is a TMDS link, and the selected code words consist of seventeen different, transition-minimized TMDS code words, including one transition-minimized TMDS code word used only as said second guard band word and another transition-minimized TMDS code word used as said first guard band and also used as one of the selected code words in said burst of the selected code words.

43. (currently amended) The transmitter of claim 34, wherein the serial link is a TMDS link, and the selected code words consist of seventeen different TMDS code words, including at least one TMDS code word used only as a guard band word.

44. (currently amended) The transmitter of claim 43, wherein the selected code words consist of seventeen different, transition-minimized TMDS code words, including at least one transition-minimized TMDS code word used only as the guard band word.

45-47. (canceled)

48. (currently amended) ~~The transmitter of claim 46~~ A transmitter for use in data transmission over a serial link, said transmitter including:

at least one input for receiving input data;

an output configured to be coupled to a channel of the link; and

circuitry, coupled to each said input and to the output, and configured to generate a sequence of selected code words by encoding the input data and to assert the sequence of selected code words to the output in response to the input data, wherein each of the selected code words is a member of a robust subset of a full code word set, the input data can be encoded as a conventional sequence of code words of the full code word set, and the sequence of selected code words is less susceptible to inter-symbol interference during transmission over the link than would be the conventional sequence of code words, wherein each of the selected code words is an L-bit binary word, each of at least a subset of the selected code words is indicative of an M-bit word of the input data, L = 10, M = 4, and the circuitry is coupled to receive source words of the input data, where each of the source words comprises N bits, N is less than L, and N is greater than M, and the circuitry is configured to pack the source words into M-bit words of the input data and to encode each of the M-bit words of the input data as one of the selected code words.

49-51. (canceled)

52. (currently amended) ~~The transmitter of claim 33~~ A transmitter for use in data transmission over a serial link, said transmitter including:

at least one input for receiving input data;

an output configured to be coupled to a channel of the link; and

circuitry, coupled to each said input and to the output, and configured to generate a sequence of selected code words by encoding the input data and to assert the sequence of selected code words to the output in response to the input data, wherein each of the selected code words is a member of a robust subset of a full code word set, the input data can be encoded as a conventional sequence of code words of the full code word set, and the sequence of selected code words is less susceptible to inter-symbol interference during transmission over the link than would be the conventional sequence of code words, wherein each of the selected code words is indicative of a sequence of L binary bits, and the selected code words have fewer contiguous zero bits and ~~continuous~~ contiguous one bits per code word on the average than do the code words of the full code word set excluding the selected code words.

53. (currently amended) ~~The transmitter of claim 33~~ A transmitter for use in data transmission over a serial link, said transmitter including:

at least one input for receiving input data;

an output configured to be coupled to a channel of the link; and

circuitry, coupled to each said input and to the output, and configured to generate a sequence of selected code words by encoding the input data and to assert the sequence of selected code words to the output in response to the input data, wherein each of the selected code words is a member of a robust subset of a full code word set, the input data can be encoded as a conventional sequence of code words of the full code word set, and the sequence of selected code words is less susceptible to inter-symbol interference during transmission over the link than would be the conventional sequence of code words, wherein each of the selected code words is indicative of a different sequence of binary bits, the circuitry is configured to assert the sequence of selected code words as a sequence of rising and falling voltage transitions, and the selected code words have bit patterns that implement DC balancing by limiting voltage drift of the serial link during transmission of said sequence of selected code words to a predetermined amount.

54-55. (canceled)

56. (currently amended) ~~The method of claim 55, also~~ A method for encoding data for transmission over a serial link, said method including the steps of:

(a) providing words of input data capable of being encoded as a conventional sequence of code words of a full code word set;

(b) generating a sequence of selected code words by encoding the input data, wherein each of the selected code words is a member of a robust subset of the full code word set, and the sequence of selected code words is less susceptible to inter-symbol interference during transmission over the link than would be the conventional sequence of code words;

generating bursts of encoded control words by encoding control bits; and

transmitting over the link a first burst of the encoded control words between a~~the~~ first burst of the video code words and the burst of the selected code words, and a second burst of the encoded control words between the burst of the selected code words and athe second burst of the video code words.

57. (original) The method of claim 56, wherein the selected code words include at least one guard band word, the burst of the selected code words has an initial word, and the initial word is the guard band word.

58. (original) The method of claim 56, wherein the selected code words include at least one guard band word, the burst of the selected code words has an initial set of words, and each word of

the initial set of words is one said guard band word.

59. (original) The method of claim 56, wherein the selected code words include at least one guard band word, the burst of the selected code words has a final word, and the final word is the guard band word.

60. (original) The method of claim 56, wherein the selected code words include at least one guard band word, the burst of the selected code words has a final set of words, and each word of the final set of words is one said guard band word.

61. (original) The method of claim 56, wherein the selected code words consist of seventeen different, transition-minimized TMDS code words, including at least one transition-minimized TMDS code word used as a guard band word.

62. (original) The method of claim 56, wherein the selected code words include at least two guard band words, including a first guard band word and a second guard band word, the second burst of the video code words has an initial word, the initial word of the second burst of the video code words is the first guard band word, the burst of the selected code words has an initial word, and the initial word of the burst of the selected code words is the second guard band word.

63. (original) The method of claim 62, wherein the selected code words consist of seventeen different, transition-minimized TMDS code words, including one transition-minimized TMDS code word used only as said second guard band word and another transition-minimized TMDS code word used as said first guard band and also used as one of the selected code words in said burst of the selected code words.

64-68. (canceled)

69. (currently amended) ~~The method of claim 67~~ A method for encoding data for transmission over a serial link, said method including the steps of:

(a) providing words of input data capable of being encoded as a conventional sequence of code words of a full code word set; and

(b) generating a sequence of selected code words by encoding the input data, wherein each of the selected code words is a member of a robust subset of the full code word set, and the sequence of selected code words is less susceptible to inter-symbol interference during transmission over the link

than would be the conventional sequence of code words, wherein each of the selected code words is an L-bit binary word, each of at least a subset of the selected code words is indicative of an M-bit word of the input data, L = 10, M = 4, and step (a) includes the step of providing source words of the input data, where each of the source words comprises N bits, N is less than L, and N is greater than M, and step (b) includes the steps of packing the source words into M-bit words of the input data and encoding each of the M-bit words of the input data as one of the selected code words.

70-72. (canceled)

73. (currently amended) ~~The method of claim 54~~ A method for encoding data for transmission over a serial link, said method including the steps of:

(a) providing words of input data capable of being encoded as a conventional sequence of code words of a full code word set; and

(b) generating a sequence of selected code words by encoding the input data, wherein each of the selected code words is a member of a robust subset of the full code word set, and the sequence of selected code words is less susceptible to inter-symbol interference during transmission over the link than would be the conventional sequence of code words, wherein each of the selected code words is indicative of a sequence of L binary bits, and the preferred words have fewer contiguous zero bits and ~~continuous~~ contiguous one bits per code word on the average than do the non-preferred words of the full set.

74. (currently amended) ~~The method of claim 54~~ A method for encoding data for transmission over a serial link, said method including the steps of:

(a) providing words of input data capable of being encoded as a conventional sequence of code words of a full code word set; and

(b) generating a sequence of selected code words by encoding the input data, wherein each of the selected code words is a member of a robust subset of the full code word set, and the sequence of selected code words is less susceptible to inter-symbol interference during transmission over the link than would be the conventional sequence of code words, wherein each of the selected code words is indicative of a different sequence of binary bits, and also including the step of:

transmitting the sequence of selected code words over the serial link as a sequence of rising and falling voltage transitions, wherein the selected code words have bit patterns that implement DC balancing by limiting voltage drift of the serial link during transmission of said sequence of selected code words to a predetermined amount.

75. (canceled)

76. (New) The system of claim 27, wherein the transmitter is also coupled to receive control bits, configured to generate bursts of encoded control words by encoding the control bits, and configured to transmit to the receiver over the serial link a first burst of the encoded control words between the first burst of the video code words and the bursts of the selected code words, and a second burst of the encoded control words between the bursts of the selected code words and the second burst of the video code words.

77. (New) The system of claim 76, wherein the selected code words include at least one guard band word, a first one of the bursts of the selected code words has an initial word, and the initial word is the guard band word.

78. (New) The system of claim 76, wherein the selected code words include at least one guard band word, a first one of the bursts of the selected code words has an initial set of words, and each word of the initial set of words is one said guard band word.

79. (New) The method of claim 56, wherein the input data are auxiliary data, and also including the steps of:

generating a sequence of video code words by encoding video data; and

transmitting over the link a first burst of the video code words followed by a burst of the selected code words followed by a second burst of the video code words, wherein each of the video code words is a member of the full code word set and at least one of the video code words is not a member of the robust subset.

80. (New) The method of claim 56, wherein the input data are auxiliary data, and also including the steps of:

generating a sequence of video code words by encoding video data; and

transmitting over the link a first burst of the video code words followed by at least two bursts of the selected code words followed by a second burst of the video code words.

81. (New) The transmitter of claim 34, wherein the circuitry is configured to assert to the output the first burst of the video code words followed by at least two bursts of the selected code words followed by the second burst of the video code words.

REMARKS:

The Preliminary amendment filed on February 13, 2002 canceled claims 55 and 75, amended claims 16, 17, 25, 31, 32, 43, 44, 52, 64, 65, and 73, and added new claims 76-78. Since that amendment was apparently not entered, the preliminary amendment of the uncanceled ones of claims 16, 17, 25, 31, 32, 43, 44, 52, 64, 65, and 73, and addition of claims 76-78 is repeated in the present response to office action. New claims 79-81 added hereby are similar to claims 79-81 set forth in the Preliminary amendment.

Applicants request entry of the amendments to the specification and abstract set forth in the Preliminary amendment, if these amendments have not already been entered. Applicants request approval of the proposed amendment to the drawings set forth in the Preliminary amendment, if it has not already been approved.

Claims 28-32 have been allowed as originally filed. The Office Action also indicates that claims 2-14, 21, 25-27, 34-44, 48, 52-53, 56-63, 69, and 73-74 would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. The uncanceled ones of these claims as amended, and new claims 76-81, are believed to be in condition for allowance.

In response to the objection to claims 56-63, claim 56 is amended to place it in independent form and provide antecedent basis for all recited elements.

Claims 1-54 and 56-74 stand provisionally rejected on the ground of nonstatutory obviousness-type double patenting over claims of pending Application No. 10/095,422. In response to the provisional rejection of the uncanceled ones of these claims, a terminal disclaimer is being filed herewith. The terminal disclaimer is believed to overcome the double patenting rejection.

Claims 1, 33, and 54 stand rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent 5,625,644 ("Myers") and claims 15-20, 22-24, 45-47, 49-51, 64-68, and 70-72 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Myers. In response, these claims are canceled.

Respectfully submitted,

Dated: 3/15/07

By _____
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Our File: SII-1000 [SIMG0077cip1]



TERMINAL DISCLAIMER TO OBVIATE A PROVISIONAL DOUBLE PATENTING REJECTION OVER A PENDING PATENT APPLICATION AND CERTIFICATE UNDER 37 C.F.R. § 3.73(b)

In re Patent Application of: Seung Ho Hwang, et al.
Application No. 10/036,234
Filed: December 24, 2001
For: ENCODING METHOD AND SYSTEM FOR REDUCING INTER-SYMBOL INTERFERENCE EFFECTS IN TRANSMISSION OVER A SERIAL LINK

Petitioner, Silicon Image, Inc., is the owner of a 100 percent interest in the instant application by an assignment recorded in the Patent and Trademark Office on June 6, 2002, at Reel 012964, Frame 0599 and an assignment recorded in the Patent and Trademark Office on March 11, 2002, at Reel 012730, Frame 0562, and in pending second Application Number 10/095,422, filed on March 12, 2002, by an assignment recorded in the Patent and Trademark Office on May 17, 2002, at Reel 012903, Frame 0869. Petitioner hereby disclaims, except as provided below, the terminal part of the statutory term of any patent granted on the instant application, which would extend beyond the expiration date of the full statutory term defined in 35 U.S.C. § 154 to § 156 and § 173, as shortened by any terminal disclaimer filed before grant, of any patent granted on pending second Application Number 10/095,422. Petitioner hereby agrees that any patent so granted on the instant application shall be enforceable only for and during such period that it and any patent granted on the second application are commonly owned. This agreement runs with any patent granted on the instant application and is binding upon the grantee, its successors or assigns.

In making the above disclaimer, petitioner does not disclaim the terminal part of any patent granted on the instant application that would extend to the expiration date of the full statutory term as defined in 35 U.S.C. § 154 to § 156 and § 173 of any patent granted on the second application, as shortened by any terminal disclaimer filed prior to the patent grant, in the event that any such granted patent: expires for failure to pay a maintenance fee, is held unenforceable, is found invalid by a court of competent jurisdiction, is statutorily disclaimed in whole or terminally disclaimed under 37 CFR § 1.321, has all claims cancelled by a reexamination certificate, is reissued, or is in any manner terminated prior to the expiration of its full statutory term as presently shortened by any terminal disclaimer filed prior to its grant.

The undersigned has reviewed all the documents in the chain of title of the patent application identified above and certifies that, to the best of undersigned's knowledge and belief, title is in the assignee identified above.

For submissions on behalf of an organization (e.g., corporation, partnership, university, government agency, etc.), the undersigned (whose title is supplied below) is empowered to act on behalf of the organization.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so

03/20/2007 EHAILE1 00000025 501697 10036234
03 FC:1814 10.00 DA 120.00 OP

made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Date: March 14, 2007

Signature

Burch Harper, Associate General Counsel
Typed or printed name, and title

☒ Terminal disclaimer fee under 37 CFR 1.20(d) included.

Atty Docket No.: SII-1000 (SIMG0077cip1)

OIPE
MAR 19 2007
PATENT & TRADEMARK OFFICE

IFW 2611

GIRARD & EQUITZ LLP
400 Montgomery Street, Suite 1110
San Francisco, CA 94104
(415) 433-2250

In re Patent Application of: SEUNG HO HWANG, ET AL. Attorney's Docket No. SII-1000 [SIMG0077cip1]

Application No. 10/036,234 Group Art Unit: 2611

Confirmation No.: 6063

Filed December 24, 2001 Examiner: Dac V. Ha

For: ENCODING METHOD AND SYSTEM FOR REDUCING INTER-SYMBOL INTERFERENCE EFFECTS IN TRANSMISSION OVER A SERIAL LINK

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Transmitted herewith are (1) a *Response to Office Action*; (2) a *Petition for One Month Extension of Time to Respond*; (3) *Terminal Disclaimer*; and (4) a Return Postcard in the above-identified application.

The fee has been calculated as shown below.

	Claims Remaining After Amendment	Highest Number Previously Paid For	Present Extra	Rate	Additional Fee
Total	53	79	0	$50	$0
Independent	14	4	10	$200	$2000
☐First Presentation of Multiple Dependent Claims				$360	$0
				Total	$2000
☐ Small Entity 50 percent Filing Fee Reduction (if applicable)					$0

1. ☐ No additional fee is required.

2. ☒ Checks in the amount of $2000 (to cover the additional claims fee), $120 (to cover the fee under 37 CFR 1.20(d) for filing the terminal disclaimer), and $120 (to cover the One Month Extension of Time to Respond fee) are attached.

3. ☒ Please charge any additional fees, including any fees necessary for extensions of time, or credit overpayment to Deposit Account No. 50-1697. **A duplicate copy of this sheet is enclosed.**

4. ☐ Petition for extension of time. The undersigned attorney of record hereby petitions for an extension of time pursuant to 37 C.F.R. § 1.136(a), as may be required, to file this response.

GIRARD & EQUITZ LLP

3/15/07
Date

By: Alfred A. Equitz
Alfred A. Equitz
Registration Number 30,922
Attorney(s) or Agent(s) of Record

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Mail Stop Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on March 15, 2007.

Dated: 3-15-07

By: Jacob Zweig
Jacob Zweig

OIPE
MAR 19 2007
PATENT & TRADEMARK OFFICE

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of

SEUNG HO HWANG, et al.

Application No. 10/036,234

Filed: December 24, 2001

For: **ENCODING METHOD AND SYSTEM FOR REDUCING INTER-SYMBOL INTERFERENCE EFFECTS IN TRANSMISSION OVER A SERIAL LINK**

Group Art Unit: 2614

Confirmation No.: 6063

Examiner: Dac V. Ha

PETITION FOR A ONE MONTH EXTENSION OF TIME TO RESPOND UNDER 37 C.F.R. 1.136(a)

400 Montgomery Street, Suite 1110
San Francisco, CA 94104
(415) 433-2250

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to Mail Stop Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on March 15, 2007.

GIRARD & EQUITZ LLP Date: 03/15/07

By: _____
Jacob S. Zweig

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Applicants hereby petition for a one month extension of time to respond to the Office Action mailed on November 28, 2006 in the above-referenced patent application. Please find enclosed a check in the amount of $120.00 to cover the extension fee.

The Commissioner is hereby authorized to charge payment of any fees associated with this communication or credit any overpayment to Deposit Account No. 50-1697. **A duplicate copy of this sheet is enclosed.**

Respectfully submitted,

GIRARD & EQUITZ LLP

Dated: 3/15/07 By: _____

Alfred A. Equitz
Reg. No. 30,922

Attorneys for Applicant(s)

Attorney Docket No. SII-1000 [SIMG0077cip1]

03/20/2007 EHAILE1 00000025 501697 10036234
02 FC:1251 120.00 OP

10076234

PATENT APPLICATION FEE DETERMINATION RECORD
Effective October 1, 2001

Application or Docket Number: 511-1000

CLAIMS AS FILED - PART I

	(Column 1)		(Column 2)
TOTAL CLAIMS	75		
FOR	NUMBER FILED		NUMBER EXTRA
TOTAL CHARGEABLE CLAIMS	75 minus 20=	*	55
INDEPENDENT CLAIMS	4 minus 3 =	*	1
MULTIPLE DEPENDENT CLAIM PRESENT			☐

* If the difference in column 1 is less than zero, enter "0" in column 2

SMALL ENTITY TYPE ☐		OR	OTHER THAN SMALL ENTITY	
RATE	FEE		RATE	FEE
BASIC FEE	370.00	OR	BASIC FEE	740.00
X$ 9=		OR	X$18=	990
X42=		OR	X84=	84
+140=		OR	+280=	—
TOTAL		OR	TOTAL	

CLAIMS AS AMENDED - PART II

3-18-07

AMENDMENT A

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	* 53	Minus	** 75	= 0
Independent	* 14	Minus	*** 4	= 10
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				☐

SMALL ENTITY		OR	OTHER THAN SMALL ENTITY	
RATE	ADDITIONAL FEE		RATE	ADDITIONAL FEE
X$ 9=		OR	X$18=	
X42=		OR	X84=	2000
+140=		OR	+280=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	2000

AMENDMENT B

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	*	Minus	**	=
Independent	*	Minus	***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				☐

RATE	ADDITIONAL FEE		RATE	ADDITIONAL FEE
X$ 9=		OR	X$18=	
X42=		OR	X84=	
+140=		OR	+280=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

AMENDMENT C

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	*	Minus	**	=
Independent	*	Minus	***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				☐

RATE	ADDITIONAL FEE		RATE	ADDITIONAL FEE
X$ 9=		OR	X$18=	
X42=		OR	X84=	
+140=		OR	+280=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20."
***If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3."
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/036,234	12/24/2001	Seung Ho Hwang	SII-1000 [SIMG0115]	6063

60974 7590 11/28/2006

GIRARD & EQUITZ LLP
400 MONTGOMERY STREET
SUITE 1110
SAN FRANCISCO, CA 94104

EXAMINER	
HA, DAC V	

ART UNIT	PAPER NUMBER
2611	

DATE MAILED: 11/28/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 10/03)

Office Action Summary	Application No.	Applicant(s)	
	10/036,234	HWANG ET AL.	
	Examiner	Art Unit	
	Dac V. Ha	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 December 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-54 and 56-74* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-74* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *1/10/05, 10/04/04, 7/30/02*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claims 56-63 are objected to because of the following informalities:

The dependency of claims 56-63 needs to be corrected since claim 55 has been cancelled.

Claim 56, lines 3, 4, the recitation "the first burst of the video code words" should be changed to, i.e. "a first burst of a video code words" to avoid antecedent problem. Applicant is required to find and correct all other similar problem in other claims.

Appropriate correction is required.

Double Patenting

2. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

3. Claims 1-54, 56-74 are provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1-75 of copending Application No. 10/095,422. Although the conflicting claims are not identical, they are not patentably distinct from each other because despite slight different in use of claimed language, they cover essentially the same subject matter.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. **Claims 1, 33, 54** are rejected under 35 U.S.C. 102(b) as being anticipated by Myers (US 5,625,644).

Regarding claims 1, Myers discloses the claimed subject matter "a receiver; a transmitter; and a serial link between the transmitter and the receiver, wherein the transmitter is coupled to receive input data, configured to generate a sequence of selected code words by encoding the input data, and configured to transmit the sequence of selected code words to the receiver over the serial link, wherein each of the selected code words is a member of a robust subset of a full code word set, the input data can be encoded as a conventional sequence of code words of the full code word set, and the sequence of selected code words is less susceptible to inter-symbol

interference during transmission over the link than would be the conventional sequence of code words" in Fig. 2; col. 6, line 65 to col. 9, line 2, wherein the selection a "sub-set" of the code words would yield a signal with less susceptible to ISI.

Regarding claims 33, 54, see claim 1.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. **Claims 15-20, 22-24, 45-47, 49-51, 64-68, 70-72** are rejected under 35 U.S.C. 103(a) as being unpatentable over Myers.

Regarding claims 15-20, 22-24, 45-47, 49-51, 64-68, 70-72, theses claimed subject matter would have been obvious to one skilled in the art as intended use and application specific.

Allowable Subject Matter

8. **Claims 2-14, 21, 25-27, 34-44, 48, 51-53, 56-63, 69, 73-74**, are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

9. **Claims 28-32** are allowed.

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Tsang et al. (US 6,052,072) discloses System And Scheme For Maximum Transition Run Length Codes With Location Dependent Constraints.

Paterson (US 6,301,221) discloses Methods And Apparatus For Encoding Data.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dac V. Ha whose telephone number is 571-272-3040. The examiner can normally be reached on 5/4.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jay Patel can be reached on 571-272-3086. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Dac V. Ha
Primary Examiner
Art Unit 2611

OIPE JC48 JAN 19 2005 PATENT & TRADEMARK OFFICE

FORM PTO-1449 (Modified) U.S Dept. of Commerce (Rev. 7-80) Patent and Trademark Office **INFORMATION DISCLOSURE CITATION** (Use several sheets if necessary)	Atty Docket No. SII-1000 [SIMG0115]	Appln. No. 10/036,234
	Applicant(s) SEUNG HO HWANG, et al.	
	Filing Date December 24, 2001	Group 2614

U.S. PATENT DOCUMENTS

*Examiner Initials		Document Number	Date	Name	Class	Subclass	Filing Date
DH	AA	6,241,778	06/05/01	de Lind van Wijngaarden, et al.	341	58	6/18/99
	BB						
	CC						
	DD						
	EE						

FOREIGN PATENT DOCUMENTS

*Examiner Initials		Document Number	Date	Country	Class	Subclass	Translation YES	NO
	FF							

OTHER DOCUMENTS

DH	GG	Goldie, John, "*LVDS based FPD-Link spans industries with Gigabits @ milliwatts!*", National Semiconductor Corporation, Online!, May 1, 2001, pages 1 to 6, from http://www.national.com/nationaledge/may01/lvds.html.
DH	HH	Siegel, P.H., "*Recording Codes For Digital Magnetic Storage*", IEEE Transactions On Magnetics, MAG-21, no. 5, September 1985, pages 1344-1349.

Examiner	Date Considered
/Dac Ha/ (11/16/2006)	11/16/2006

* Examiner: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

OIPE JC141 OCT 04 2006 PATENT & TRADEMARK OFFICE

FORM PTO-1449 (modified) U.S Dept. of Commerce (Rev. 7-80) Patent and Trademark Office **INFORMATION DISCLOSURE CITATION** (Use several sheets if necessary)	Atty Docket No. SII-1000 [SIMG0115]	Appln. No. 10/036,234
	Applicant(s) SEUNG HO HWANG, et al.	
	Filing Date December 24, 2001	Group 2614

U.S. PATENT DOCUMENTS

*Examiner Initials		Document Number	Date	Name	Class	Subclass	Filing Date
DH	AA	6,141,691	10/31/00	Frink et al.	709	233	04/03/98
DH	BB	6,185,250	12/12/00	Wang et al.	66	62	02/14/00
	CC						
	DD						
	EE						
	FF						
	GG						
	HH						
	II						

FOREIGN PATENT DOCUMENTS

*Examiner Initials		Document Number	Date	Country	Class	Subclass	Translation YES	NO
	JJ							

OTHER DOCUMENTS

	KK	

Examiner	Date Considered
/Dac Ha/ (11/16/2006)	11/16/2006

* Examiner: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

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	Filing Date December 24, 2001	Group 2614

JUL 30 2002 PATENT & TRADEMARK OFFICE

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U.S. PATENT DOCUMENTS

*Examiner Initials		Document Number	Date	Name	Class	Subclass	Filing Date
DH	AA	5,974,464	10/26/99	SHIN et al.	709	231	09/30/96
DH	BB	5,905,769	05/18/99	LEE et al.	375	376	05/07/96
DH	CC	6,191,822 B1	02/20/01	SMYERS	348	552	06/20/97
DH	DD	5,506,932	04/09/96	HOLMES et al.	395	2.14	04/16/93
DH	EE	5,541,662	07/30/96	ADAMS et al.	348	460	09/30/94
DH	FF	5,523,795	06/04/96	UEDA	348	480	08/16/94
DH	GG	5,150,211	09/22/92	CHARBONNEL et al.	358	143	08/28/90
DH	HH	5,199,030	03/30/93	UEDA	370	68	09/05/91
DH	II	5,940,070	08/17/99	KOO	345	302	05/13/96

FOREIGN PATENT DOCUMENTS

*Examiner Initials		Document Number	Date	Country	Class	Subclass	Translation YES	NO
DH	JJ	WO 00/16525	23.03.2000	PCT	H04L	25/02		

OTHER DOCUMENTS

DH	KK	*High-Bandwidth Digital Content Protection System,* Revision 1.0, by Intel Corporation, February 17, 2000, pages 1-60.

Examiner	Date Considered
/Dac Ha/ (11/16/2006)	

* Examiner: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

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DEC 23 2002
PATENT & TRADEMARK OFFICE

FORM PTO-1449 (Modified) U.S Dept. of Commerce (Rev. 7-80) Patent and Trademark Office **INFORMATION DISCLOSURE CITATION** (Use several sheets if necessary)	Atty Docket No. SII-1000 [SIMG0115]	Appln. No. 10/036,234
	Applicant(s) SEUNG HO HWANG, et al	
	Filing Date December 24, 2001	Group 2614

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Technology Center 2600

U.S. PATENT DOCUMENTS

*Examiner Initials		Document Number	Date	Name	Class	Subclass	Filing Date
DH	AA	6,208,715 B1	03/27/01	Haavisto	379	88.07	10/30/96
DH	AB	6,249,669 B1	06/19/01	Ogino et al.	455	63	02/28/00
	AC						

FOREIGN PATENT DOCUMENTS

*Examiner Initials		Document Number	Date	Country	Class	Subclass	Translation YES	NO
	AD							
	AE							

OTHER DOCUMENTS

	AF	
	AG	

Examiner	Date Considered
/Dac Ha/ (11/16/2006)	11/16/2006

* Examiner: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

Notice of References Cited	Application/Control No. 10/036,234	Applicant(s)/Patent Under Reexamination HWANG ET AL.	
	Examiner Dac V. Ha	Art Unit 2611	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-5,625,644	04-1997	Myers, David J.	375/242
*	B	US-6,052,072	04-2000	Tsang et al.	341/59
*	C	US-6,301,221	10-2001	Paterson, Kenneth Graham	370/208
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
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	S					
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NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
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	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Index of Claims

Application/Control No.	Applicant(s)/Patent under Reexamination
10/036,234	HWANG ET AL.
Examiner	**Art Unit**
Dac V. Ha	2611

√	Rejected	–	(Through numeral) Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

Claim		Date
Final	Original	11/16/06
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Claim		Date
Final	Original	11/16/06
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Claim		Date
Final	Original	
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Bib Data Sheet

CONFIRMATION NO. 6063

SERIAL NUMBER	FILING OR 371(c) DATE / RULE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
10/036,234	12/24/2001	375	2611	SII-1000 [SIMG0115]

APPLICANTS

Seung Ho Hwang, Palo Alto, CA;
Jano Banks, Cupertino, CA;
Paul Daniel Wolf, San Carlos, CA;
Eric Lee, San Jose, CA;
Baegin Sung, Sunnyvale, CA;

**** CONTINUING DATA ***************************

This application is a CIP of 09/954,663 09/12/2001 OK! DH

**** FOREIGN APPLICATIONS **********************

NONE! DH

IF REQUIRED, FOREIGN FILING LICENSE GRANTED

** 02/06/2002 OK! DH

		STATE OR COUNTRY	SHEETS DRAWING	TOTAL CLAIMS	INDEPENDENT CLAIMS
Foreign Priority claimed	☐ yes ☑ no				
35 USC 119 (a-d) conditions met	☐ yes ☑ no ☐ Met after Allowance	CA	5	79	4
Verified and Acknowledged	Examiner's Signature / Initials				

ADDRESS

60974

TITLE

Encoding method and system for reducing inter-symbol interference effects in transmission over a serial link

FILING FEE RECEIVED	FEES: Authority has been given in Paper No. _____ to charge/credit DEPOSIT ACCOUNT No. _____ for following:	☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit
2016		

Search Notes

Application/Control No.	Applicant(s)/Patent under Reexamination	
10/036,234	HWANG ET AL.	
Examiner	**Art Unit**	
Dac V. Ha	2611	

SEARCHED			
Class	Subclass	Date	Examiner
375	219, 220	11/16/2006	DH
	240		
	240.01		
	240.23		
	244, 246		
	253, 254		
	260, 285		
	295, 296		
	346, 348		
348	388		
	398.1		
	423.1		
	470, 476		
	477, 487		

INTERFERENCE SEARCHED			
Class	Subclass	Date	Examiner

SEARCH NOTES (INCLUDING SEARCH STRATEGY)		
	DATE	EXMR
BRS	11/16/2006	DH

EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L5	12	("6241778" "6141691" "6185250" "5974464" "5905769" "6191822" "5506932" "5541662" "5523795" "5150211" "5199030" "5940070").pn.	US-PGPUB; USPAT	OR	ON	2006/11/16 14:42
L6	5018	(code near1 word) same (encod$4)	US-PGPUB; USPAT	OR	ON	2006/11/16 14:42
L7	1	5 and 6	US-PGPUB; USPAT	OR	ON	2006/11/16 14:43
L8	0	7 and (isi (symbol adj interfer$5))	US-PGPUB; USPAT	OR	ON	2006/11/16 14:44
L9	24	6 same (isi (symbol adj interfer$5))	US-PGPUB; USPAT	OR	ON	2006/11/16 14:44
L10	5018	(code near1 word) same (encod$4)	US-PGPUB; USPAT	OR	ON	2006/11/16 14:44
L11	265	L10 same (subset (sub adj set))	US-PGPUB; USPAT	OR	ON	2006/11/16 14:44
L12	1103	L10 and (subset (sub adj set))	US-PGPUB; USPAT	OR	ON	2006/11/16 14:44
L13	83	12 and(isi (symbol adj interfer$5))	US-PGPUB; USPAT	OR	ON	2006/11/16 14:45
L14	83	12 and (isi (symbol adj interfer$5))	US-PGPUB; USPAT	OR	ON	2006/11/16 14:45
L15	5018	(code near1 word) same (encod$4)	US-PGPUB; USPAT	OR	ON	2006/11/16 14:45
L16	265	L15 same (subset (sub adj set))	US-PGPUB; USPAT	OR	ON	2006/11/16 14:48
L17	15	L16 and (isi (symbol adj interfer$5))	US-PGPUB; USPAT	OR	ON	2006/11/16 14:48
L18	15	L17 and ("714"/$.ccls. "375"/$.ccls. "348"/$.ccls. "370"/$.ccls. "341"/$.ccls.)	US-PGPUB; USPAT	OR	ON	2006/11/16 14:46
L20	215	L15 and (isi (symbol adj interfer$5))	US-PGPUB; USPAT	OR	ON	2006/11/16 14:48
L21	15	L18 and (subset (sub adj set))	US-PGPUB; USPAT	OR	ON	2006/11/16 14:48
L22	1052	tmds	USPAT	OR	ON	2006/11/16 15:22
L23	2102	tmds	US-PGPUB; USPAT	OR	ON	2006/11/16 15:23
L24	4	16 and 22	US-PGPUB; USPAT	OR	ON	2006/11/16 15:23

EAST Search History

L25	8	15 and 22	US-PGPUB; USPAT	OR	ON	2006/11/16 15:23
S1	1	"20030048851"	US-PGPUB; USPAT	OR	ON	2006/11/15 15:02
S2	12	("6241778" "6141691" "6185250" "5974464" "5905769" "6191822" "5506932" "5541662" "5523795" "5150211" "5199030" "5940070").pn.	US-PGPUB; USPAT	OR	ON	2006/11/16 14:42
S3	290	("6241778" "6141691" "6185250" "5974464" "5905769" "6191822" "5506932" "5541662" "5523795" "5150211" "5199030" "5940070")	US-PGPUB; USPAT	OR	ON	2006/11/15 15:03
S4	13	(code near1 word) with (isi (symbol adj intereferece))	US-PGPUB; USPAT	OR	ON	2006/11/15 15:33
S5	0	S2 and S4	US-PGPUB; USPAT	OR	ON	2006/11/15 15:33
S6	22	(code near1 word) same (isi (symbol adj intereferece))	US-PGPUB; USPAT	OR	ON	2006/11/15 15:33
S7	36	(code near1 word) same (isi (symbol adj interference))	US-PGPUB; USPAT	OR	ON	2006/11/15 15:34
S8	36	(code near1 word) same (isi (symbol adj interfer$5))	US-PGPUB; USPAT	OR	ON	2006/11/15 17:21
S9	0	S2 and S8	US-PGPUB; USPAT	OR	ON	2006/11/15 15:34
S10	5014	(code near1 word) same (encod$4)	US-PGPUB; USPAT	OR	ON	2006/11/16 14:42
S11	265	S10 same (subset (sub adj set))	US-PGPUB; USPAT	OR	ON	2006/11/16 09:11
S12	41	S11 and (code near1 word).ab.	US-PGPUB; USPAT	OR	ON	2006/11/15 15:35
S13	39	S12 and (code near1 word).clm.	US-PGPUB; USPAT	OR	ON	2006/11/15 15:57
S14	11181	(375/219 375/220 375/340 375/240.01 375/240.23 375/244 375/246 375/253 375/254 375/260 375/285 375/295 375/296 375/346 375/348).ccls.	US-PGPUB; USPAT	OR	ON	2006/11/15 16:03
S15	556	(348/398.1 348/423.1 348/470 348/476 348/477 348/387 348/388).ccls.	US-PGPUB; USPAT	OR	ON	2006/11/15 16:10
S16	11697	S14 S15	US-PGPUB; USPAT	OR	ON	2006/11/15 16:10
S17	8	S11 and S16	US-PGPUB; USPAT	OR	ON	2006/11/15 16:10

EAST Search History

S18	508	S10 same serial$4	US-PGPUB; USPAT	OR	ON	2006/11/15 16:16
S19	38	S18 same ((code near1 word) with set)	US-PGPUB; USPAT	OR	ON	2006/11/15 16:16
S20	3	S19 and S16	US-PGPUB; USPAT	OR	ON	2006/11/15 16:16
S21	7	"5625644" and S10	US-PGPUB; USPAT	OR	ON	2006/11/15 17:19
S22	1	"5625644" and S8	US-PGPUB; USPAT	OR	ON	2006/11/15 17:18
S23	12	"5625644"	US-PGPUB; USPAT	OR	ON	2006/11/15 17:19
S24	4	S11 same (isi (symbol adj interfer$5))	US-PGPUB; USPAT	OR	ON	2006/11/15 17:20
S25	15	S11 and (isi (symbol adj interfer$5))	US-PGPUB; USPAT	OR	ON	2006/11/16 09:04
S26	15	S25 and ("375"/$.ccls. "348"/$. ccls. "370"/$.ccls. "341"/$.ccls.)	US-PGPUB; USPAT	OR	ON	2006/11/16 14:45
S27	2	("2003/0048852").URPN.	USPAT	OR	ON	2006/11/15 17:50
S28	4	("5196933" | "5425050" | "5745525" | "5949796").PN.	US-PGPUB; USPAT; USOCR	OR	ON	2006/11/15 17:50
S29	5	("5425050" | "5610908" | "5694389" | "5784363" | "5953311").PN.	US-PGPUB; USPAT; USOCR	OR	ON	2006/11/15 17:50
S30	14	("6052072").URPN.	USPAT	OR	ON	2006/11/15 17:50
S31	7	("5341386" | "5451943" | "5502735" | "5553169" | "5576707" | "5731768" | "5859601").PN.	US-PGPUB; USPAT; USOCR	OR	ON	2006/11/15 17:50
S32	10	("5625644").URPN.	USPAT	OR	ON	2006/11/15 17:50
S33	25	("3995264" | "4261019" | "4348659" | "4387364" | "4394641" | "4486739" | "4501000" | "4509164" | "4517552" | "4530088" | "4569050" | "4598326" | "4626826" | "4675650" | "4677421" | "4750138" | "4760378" | "4811361" | "4827475" | "4864303" | "4881076" | "4924463" | "4969146" | "5016258" | "5025256").PN.	US-PGPUB; USPAT; USOCR	OR	ON	2006/11/15 17:50
S34	1	("5452310").URPN.	USPAT	OR	ON	2006/11/15 17:50
S35	31	("4811361").URPN.	USPAT	OR	ON	2006/11/15 17:50

EAST Search History

S36	4	("5416801" | "6035044" | "6130918" | "6301221").PN.	US-PGPUB; USPAT; USOCR	OR	ON	2006/11/16 09:10
S37	1	"5625644" and (isi (symbol adj interfer$5))	US-PGPUB; USPAT	OR	ON	2006/11/16 09:11
S38	2	("2003/0048852").URPN.	USPAT	OR	ON	2006/11/16 09:11
S39	4	("5196933" | "5425050" | "5745525" | "5949796").PN.	US-PGPUB; USPAT; USOCR	OR	ON	2006/11/16 09:11
S40	5	("5425050" | "5610908" | "5694389" | "5784363" | "5953311").PN.	US-PGPUB; USPAT; USOCR	OR	ON	2006/11/16 09:11
S41	14	("6052072").URPN.	USPAT	OR	ON	2006/11/16 09:11
S42	7	("5341386" | "5451943" | "5502735" | "5553169" | "5576707" | "5731768" | "5859601").PN.	US-PGPUB; USPAT; USOCR	OR	ON	2006/11/16 09:11
S43	10	("5625644").URPN.	USPAT	OR	ON	2006/11/16 09:11
S44	25	("3995264" | "4261019" | "4348659" | "4387364" | "4394641" | "4486739" | "4501000" | "4509164" | "4517552" | "4530088" | "4569050" | "4598326" | "4626826" | "4675650" | "4677421" | "4750138" | "4760378" | "4811361" | "4827475" | "4864303" | "4881076" | "4924463" | "4969146" | "5016258" | "5025256").PN.	US-PGPUB; USPAT; USOCR	OR	ON	2006/11/16 09:11
S45	1	("5452310").URPN.	USPAT	OR	ON	2006/11/16 09:11
S46	31	("4811361").URPN.	USPAT	OR	ON	2006/11/16 09:11
S47	95	S38 S39 S40 S41 S42 S43 S44 S45 S46	US-PGPUB; USPAT; USOCR	OR	ON	2006/11/16 09:11
S48	15	S47 and (isi (symbol adj interfer$5))	US-PGPUB; USPAT	OR	ON	2006/11/16 09:12
S49	5018	(code near1 word) same (encod$4)	US-PGPUB; USPAT	OR	ON	2006/11/16 09:11
S50	265	S49 same (subset (sub adj set))	US-PGPUB; USPAT	OR	ON	2006/11/16 14:44
S51	1	S48 and S50	US-PGPUB; USPAT	OR	ON	2006/11/16 09:13

EAST Search History

S52	23	("4811361" | "5150211" | "5199030" | "5220568" | "5392299" | "5506932" | "5523795" | "5541662" | "5625644" | "5905769" | "5940070" | "5974464" | "6052072" | "6191822" | "6198582" | "6204781" | "6208715" | "6249669" | "6288655" | "6480125" | "6504493" | "6543023" | "6804805").PN.	US-PGPUB; USPAT; USOCR	OR	ON	2006/11/16 09:12
S53	4	S52 and (isi (symbol adj interfer$5))	US-PGPUB; USPAT	OR	ON	2006/11/16 14:43
S54	1	S53 and S50	US-PGPUB; USPAT	OR	ON	2006/11/16 09:13
S55	4	S53 and S49	US-PGPUB; USPAT	OR	ON	2006/11/16 09:13

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APPLICATION NUMBER	PATENT NUMBER	GROUP ART UNIT	FILE WRAPPER LOCATION
10/036,234		2611	06B0

Correspondence Address / Fee Address Change

The following fields have been set to Customer Number 60974 on 03/16/2006

- Correspondence Address

The address of record for Customer Number 60974 is:
GIRARD & EQUITZ LLP
400 MONTGOMERY STREET
SUITE 1110
SAN FRANCISCO,CA 94104

OIPE
JAN 10 2005
PATENT & TRADEMARK OFFICE
JC48

2614

PATENT

THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of

SEUNG HO HWANG, et al.

Application No. 10/036,234

Filed: December 24, 2001

For: **ENCODING METHOD AND SYSTEM FOR REDUCING INTER-SYMBOL INTERFERENCE EFFECTS IN TRANSMISSION OVER A SERIAL LINK**

Group Art Unit: 2614

Examiner: Unknown

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

400 Montgomery Street
Suite 1110
San Francisco, CA 94104
(415) 433-2250

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to Mail Stop Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on January 6, 2005.

GIRARD & EQUITZ LLP Date: 01/06/05

By: _____
Jacob S. Zweig

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Applicants submit herewith patents, publications or other information [attached hereto and listed on the attached Form PTO-1449 (modified)] of which they are aware, which they believe may be material to the examination of this application and in respect of which there may be a duty to disclose in accordance with 37 CFR § 1.56.

This Information Disclosure Statement:

(a) [] accompanies the new patent application submitted herewith. 37 CFR § 1.97(a).

(b) [] is filed within three months after the filing date of the application or within three months after the date of entry of the national stage of a PCT application as set forth in 37 CFR § 1.491.

(c) [X] as far as is known to the undersigned, is filed before the mailing date of a first Office Action on the merits.

(d) [] is filed after the first office action and more than three months after the application's filing date or PCT national stage date of entry filing but, as far as is known to the undersigned, prior to the mailing date of either a final rejection or a notice of allowance, whichever occurs first, and is accompanied by either the fee ($180) set forth in 37 CFR § 1.17(p) **or** a certification as specified in 37 CFR § 1.97(e), as checked below.

(e) [] is filed after the mailing date of either a final rejection or a notice of allowance, whichever occurred first, and the Issue Fee has not been paid, and is accompanied by the fee ($130) set forth in 37 CFR § 1.17(i)(1) and a certification as specified in 37 CFR § 1.97(e), as checked below. This document is to be considered as a petition requesting consideration of the information disclosure statement.

[If either of boxes (d) or (e) are checked above, the following "certification" under 37 CFR § 1.97(e) may need to be completed.] The undersigned certifies that:

(f) [] Each item of information contained in the information disclosure statement was cited in a communication mailed from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this information disclosure statement.

(g) [] No item of information contained in this information disclosure statement was cited in a communication mailed from a foreign patent office in a counterpart foreign application or, to the knowledge of the undersigned after making reasonable inquiry, was known to any individual designated in 37 CFR § 1.56(c) more than three months prior to the filing of this information disclosure statement.

A list of the patent(s) or publication(s) is set forth on the attached Form PTO-1449 (Modified).

A copy of the items on PTO-1449 (Modified) is supplied herewith:

(h) [X] each (i) [] none (j) [] only those listed below:

Those patent(s) or publication(s) which are marked with an asterisk (*) in the attached form PTO-1449 (Modified) are not supplied because they were previously cited by or submitted to the Office in a prior application

no. , filed and relied upon in this application for an earlier filing date under 35 U.S.C. § 120.

A concise explanation of relevance of the items listed on form PTO-1449 (Modified) is as follows: each item was cited by the European Patent Office in prosecution of a foreign counterpart to this application.

While the information and references disclosed in this Information Disclosure Statement may be "material" pursuant to 37 CFR § 1.56, it is not intended to constitute an admission that any patent, publication or other information referred to therein is "prior art" for this invention unless specifically designated as such.

In accordance with 37 CFR § 1.97(g), the filing of this Information Disclosure Statement shall not be construed to mean that a search has been made or that no other material information as defined in 37 CFR § 1.56(a) exists. It is submitted that the Information Disclosure Statement is in compliance with 37 CFR § 1.98 and MPEP § 609 and the Examiner is respectfully requested to consider the listed references.

[X] The Commissioner is hereby authorized to charge our Deposit Account No. **50-1697** for any fees required in connection with the filing of this Information Disclosure Statement. **A duplicate copy of this Notice is enclosed for this purpose.**

Respectfully submitted,

Dated: 1/6/05 By Alfred A. Equitz

Alfred A. Equitz
Registration No. 30,922
Tel. No. 415/433-2250

Our File: SII-1000 [SIMG0115]

OIPE JC48 JAN 10 2005 PATENT & TRADEMARK OFFICE

FORM PTO-1449 (Modified) U.S Dept. of Commerce (Rev. 7-80) Patent and Trademark Office **INFORMATION DISCLOSURE CITATION** (Use several sheets if necessary)	Atty Docket No. SII-1000 [SIMG0115]	Appln. No. 10/036,234
	Applicant(s) SEUNG HO HWANG, et al.	
	Filing Date December 24, 2001	Group 2614

U.S. PATENT DOCUMENTS

*Examiner Initials		Document Number	Date	Name	Class	Subclass	Filing Date
	AA	6,241,778	06/05/01	de Lind van Wijngaarden, et al.	341	58	6/18/99
	BB						
	CC						
	DD						
	EE						

FOREIGN PATENT DOCUMENTS

*Examiner Initials		Document Number	Date	Country	Class	Subclass	Translation YES	NO
	FF							

OTHER DOCUMENTS

	GG	Goldie, John, "*LVDS based FPD-Link spans industries with Gigabits @ milliwatts!*", National Semiconductor Corporation, Online!, May 1, 2001, pages 1 to 6, from http://www.national.com/nationaledge/may01/lvds.html.
	HH	Siegel, P.H., "*Recording Codes For Digital Magnetic Storage*", IEEE Transactions On Magnetics, MAG-21, no. 5, September 1985, pages 1344-1349.

Examiner	Date Considered

* Examiner: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

OIPE JG141 OCT 04 2004 PATENT & TRADEMARK OFFICE

PATENT 2614 -TFW

THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of

SEUNG HO HWANG, et al.

Application No. 10/036,234

Filed: December 24, 2001

For: **ENCODING METHOD AND SYSTEM FOR REDUCING INTER-SYMBOL INTERFERENCE EFFECTS IN TRANSMISSION OVER A SERIAL LINK**

Group Art Unit: 2614

Examiner: Unknown

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

400 Montgomery Street
Suite 1110
San Francisco, CA 94104
(415) 433-2250

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on October 1, 2004.

GIRARD & EQUITZ LLP Date: 10/01/04

By: _____
Jacob S. Zweig

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Applicants submit herewith patents, publications or other information [attached hereto and listed on the attached Form PTO-1449 (modified)] of which they are aware, which they believe may be material to the examination of this application and in respect of which there may be a duty to disclose in accordance with 37 CFR § 1.56.

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(a) [] accompanies the new patent application submitted herewith. 37 CFR § 1.97(a).

(b) [] is filed within three months after the filing date of the application or within three months after the date of entry of the national stage of a PCT application as set forth in 37 CFR § 1.491.

(c) [X] as far as is known to the undersigned, is filed before the mailing date of a first Office Action on the merits.

(d) [] is filed after the first office action and more than three months after the application's filing date or PCT national stage date of entry filing but, as far as is known to the undersigned, prior to the mailing date of either a final rejection or a notice of allowance, whichever occurs first, and is accompanied by either the fee ($180) set forth in 37 CFR § 1.17(p) **or** a certification as specified in 37 CFR § 1.97(e), as checked below.

(e) [] is filed after the mailing date of either a final rejection or a notice of allowance, whichever occurred first, and the Issue Fee has not been paid, and is accompanied by the fee ($130) set forth in 37 CFR § 1.17(i)(1) and a certification as specified in 37 CFR § 1.97(e), as checked below. This document is to be considered as a petition requesting consideration of the information disclosure statement.

[If either of boxes (d) or (e) are checked above, the following "certification" under 37 CFR § 1.97(e) may need to be completed.] The undersigned certifies that:

(f) [] Each item of information contained in the information disclosure statement was cited in a communication mailed from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this information disclosure statement.

(g) [] No item of information contained in this information disclosure statement was cited in a communication mailed from a foreign patent office in a counterpart foreign application or, to the knowledge of the undersigned after making reasonable inquiry, was known to any individual designated in 37 CFR § 1.56(c) more than three months prior to the filing of this information disclosure statement.

A list of the patent(s) or publication(s) is set forth on the attached Form PTO-1449 (Modified).

A copy of the items on PTO-1449 (Modified) is supplied herewith:

(h) [] each (i) [X] none (j) [] only those listed below:

Those patent(s) or publication(s) which are marked with an asterisk (*) in the attached form PTO-1449 (Modified) are not supplied because they were previously cited by or submitted to the Office in a prior application

no. , filed and relied upon in this application for an earlier filing date under 35 U.S.C. § 120.

A concise explanation of relevance of the items listed on form PTO-1449 (Modified) is as follows: each item was cited by the Candian Patent Office in prosecution of a foreign counterpart to this application.

The Examiner is reminded that a "concise explanation of the relevance" of the submitted items "may be nothing more than identification of the particular figure or paragraph of the patent or publication which has some relation to the claimed invention," MPEP § 609.

While the information and references disclosed in this Information Disclosure Statement may be "material" pursuant to 37 CFR § 1.56, it is not intended to constitute an admission that any patent, publication or other information referred to therein is "prior art" for this invention unless specifically designated as such.

In accordance with 37 CFR § 1.97(g), the filing of this Information Disclosure Statement shall not be construed to mean that a search has been made or that no other material information as defined in 37 CFR § 1.56(a) exists. It is submitted that the Information Disclosure Statement is in compliance with 37 CFR § 1.98 and MPEP § 609 and the Examiner is respectfully requested to consider the listed references.

[X] The Commissioner is hereby authorized to charge our Deposit Account No. **50-1697** for any fees required in connection with the filing of this Information Disclosure Statement. **A duplicate copy of this Notice is enclosed for this purpose.**

Respectfully submitted,

Dated: 10/1/04 By Alfred A. Equitz

Alfred A. Equitz
Registration No. 30,922
Tel. No. 415/433-2250

Our File: SII-1000 [SIMG0115]

OIPE JC141 OCT 04 2004 PATENT & TRADEMARK OFFICE

FORM PTO-1449 (Modified) U.S Dept. of Commerce (Rev. 7-80) Patent and Trademark Office **INFORMATION DISCLOSURE CITATION** (Use several sheets if necessary)	Atty Docket No. SII-1000 [SIMG0115]	Appln. No. 10/036,234
	Applicant(s) SEUNG HO HWANG, et al.	
	Filing Date December 24, 2001	Group 2614

U.S. PATENT DOCUMENTS

*Examiner Initials		Document Number	Date	Name	Class	Subclass	Filing Date
	AA	6,141,691	10/31/00	Frink et al.	709	233	04/03/98
	BB	6,185,250	12/12/00	Wang et al.	66	62	02/14/00
	CC						
	DD						
	EE						
	FF						
	GG						
	HH						
	II						

FOREIGN PATENT DOCUMENTS

*Examiner Initials		Document Number	Date	Country	Class	Subclass	Translation YES	NO
	JJ							

OTHER DOCUMENTS

	KK	

Examiner	Date Considered

* Examiner: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

OIPE
DEC 23 2002
PATENT & TRADEMARK OFFICE

PATENT

THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of

SEUNG HO HWANG, et al.

Application No. 10/036,234

Filed: December 24, 2001

For: **ENCODING METHOD AND SYSTEM FOR REDUCING INTER-SYMBOL INTERFERENCE EFFECTS IN TRANSMISSION OVER A SERIAL LINK**

Group Art Unit: 2614

Examiner: Unknown

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

RECEIVED
DEC 26 2002
Technology Center 2600

400 Montgomery Street
Suite 1110
San Francisco, CA 94104
(415) 433-2250

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to Commissioner for Patents, Washington, DC 20231, on December 16, 2002.

GIRARD & EQUITZ LLP Date: 12/16/02

By: Marsha A. Townsend
Marsha A. Townsend

Commissioner for Patents
Washington, D.C. 20231

RECEIVED
DEC 31 2002
GROUP 2600

Sir:

Applicants submit herewith patents, publications or other information [attached hereto and listed on the attached Form PTO-1449 (modified)] of which they are aware, which they believe may be material to the examination of this application and in respect of which there may be a duty to disclose in accordance with 37 CFR § 1.56.

This Information Disclosure Statement:

(a) [] accompanies the new patent application submitted herewith. 37 CFR § 1.97(a).

(b) [] is filed within three months after the filing date of the application or within three months after the date of entry of the national stage of a PCT application as set forth in 37 CFR § 1.491.

(c) [X] as far as is known to the undersigned, is filed before the mailing date of a first Office Action on the merits.

(d) [] is filed after the first office action and more than three months after the application's filing date or PCT national stage date of entry filing but, as far as is known to the undersigned, prior to the mailing date of either a final rejection or a notice of allowance, whichever occurs first, and is accompanied by either the fee ($180) set forth in 37 CFR § 1.17(p) **or** a certification as specified in 37 CFR § 1.97(e), as checked below.

(e) [] is filed after the mailing date of either a final rejection or a notice of allowance, whichever occurred first, and the Issue Fee has not been paid, and is accompanied by the fee ($130) set forth in 37 CFR § 1.17(i)(1) and a certification as specified in 37 CFR § 1.97(e), as checked below. This document is to be considered as a petition requesting consideration of the information disclosure statement.

[If either of boxes (d) or (e) are checked above, the following "certification" under 37 CFR § 1.97(e) may need to be completed.] The undersigned certifies that:

(f) [] Each item of information contained in the information disclosure statement was cited in a communication mailed from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this information disclosure statement.

(g) [] No item of information contained in this information disclosure statement was cited in a communication mailed from a foreign patent office in a counterpart foreign application or, to the knowledge of the undersigned after making reasonable inquiry, was known to any individual designated in 37 CFR § 1.56(c) more than three months prior to the filing of this information disclosure statement.

A list of the patent(s) or publication(s) is set forth on the attached Form PTO-1449 (Modified).

A copy of each of the items on PTO-1449 (Modified) is supplied herewith.

A concise explanation of relevance of the items listed on form PTO-1449 (Modified) is that each listed item was cited in an International Search report (copy attached) issued in a corresponding PCT International Application. The Search Report refers to relevent portions of the references.

While the information and references disclosed in this Information Disclosure Statement may be "material" pursuant to 37 CFR § 1.56, it is not intended to constitute an admission that any patent, publication or other information referred to therein is "prior art" for this invention unless specifically designated as such.

In accordance with 37 CFR § 1.97(g), the filing of this Information Disclosure Statement shall not be construed to mean that a search has been made or that no other material information as defined in 37 CFR § 1.56(a) exists. It is submitted that the Information Disclosure Statement is in compliance with 37 CFR § 1.98 and MPEP § 609 and the Examiner is respectfully requested to consider the listed references.

[X] The Commissioner is hereby authorized to charge our Deposit Account No. **50-1697** for any fees required in connection with the filing of this Information Disclosure Statement. **A duplicate copy of this Notice is enclosed for this purpose.**

Respectfully submitted,

Dated: 12/16/02 By Alfred A Equitz

Alfred A. Equitz
Registration No. 30,922
Tel. No. 415/433-2250

Our File: SII-1000 [SIMG0115]

OIPE
DEC 23 2002
PATENT & TRADEMARK OFFICE

FORM PTO-1449 (Modified) U.S Dept. of Commerce (Rev. 7-80) Patent and Trademark Office **INFORMATION DISCLOSURE CITATION** (Use several sheets if necessary)	Atty Docket No. SII-1000 [SIMG0115]	Appln. No. 10/036,234
	Applicant(s) SEUNG HO HWANG, et al	
	Filing Date December 24, 2001	Group 2614

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DEC 26 2002
Technology Center 2600

U.S. PATENT DOCUMENTS

*Examiner Initials		Document Number	Date	Name	Class	Subclass	Filing Date
	AA	6,208,715 B1	03/27/01	Haavisto	379	88.07	10/30/96
	AB	6,249,669 B1	06/19/01	Ogino et al.	455	63	02/28/00
	AC						

FOREIGN PATENT DOCUMENTS

*Examiner Initials		Document Number	Date	Country	Class	Subclass	Translation YES	NO
	AD							
	AE							

OTHER DOCUMENTS

	AF	
	AG	

Examiner	Date Considered

* Examiner: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

OIPE JC180 OCT 29 2002 PATENT & TRADEMARK OFFICE

2614

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of

SEUNG HO HWANG, et al.

Application No. 10/036,234

Filed: December 24, 2001

For: **ENCODING METHOD AND SYSTEM FOR REDUCING INTER-SYMBOL INTERFERENCE EFFECTS IN TRANSMISSION OVER A SERIAL LINK**

Group Art Unit: 2614

Examiner: Unknown

TRANSMITTAL OF REQUEST TO RESCIND PREVIOUS NONPUBLICATION REQUEST UNDER 35 U.S.C. 122(b)(2)(B)(ii)

400 Montgomery Street, Suite 1110
San Francisco, CA 94104
(415) 433-2250

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to Box PG Pub, Commissioner for Patents, Washington, DC 20231, on October 18, 2002.

GIRARD & EQUITZ LLP Date: 10/18/02

By: Marsha A. Townsend

Marsha A. Townsend

RECEIVED
OCT 30 2002
Technology Center 2600

Box PG Pub
Commissioner for Patents
Washington, D.C. 20231

Sir:

Enclosed is an executed *Request To Rescind Previous Nonpublication Request Under 35 U.S.C. 122(b)(2)(B)(ii)* to be made of record in the above-referenced case.

The Commissioner is hereby authorized to charge payment of any fees associated with this communication or credit any overpayment to Deposit Account No. 50-1697. **A duplicate copy of this sheet is enclosed**.

Respectfully submitted,

GIRARD & EQUITZ LLP

Dated: 10/18/02 By: Alfred A. Equitz

Alfred A. Equitz
Reg. No.30,922
Attorneys for Applicant(s)

Attorney Docket No. SII-1000 [SIMG0115]

OIPE JC180 OCT 29 2002 PATENT & TRADEMARK OFFICE

10
59
11/7/02

PTO/SB/36 (10-01)
Approved for use through 10/31/2002. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

REQUEST TO RESCIND PREVIOUS NONPUBLICATION REQUEST 35 U.S.C. 122(b)(2)(B)(ii)

Application Number	10/036,234
Filing Date	December 24, 2001
First Named Inventor	SEUNG HO HWANG
Title	Encoding Method and System for Reducing Inter-Symbol Interference Effects in...
Atty Docket Number	SII-1000 [SIMG0115]
Group Art Unit	2614
Examiner	Unknown

RECEIVED
OCT 30 2002
Technology Center 2600

I hereby **rescind** the previous request that the above-identified application not be published under 35 U.S.C. 122(b).

October 18, 2002
Date

Alfred A. Equitz
Signature

ALFRED A. EQUITZ, Reg. No. 30, 922
Typed or printed name

This request must be signed in compliance with 37 CFR 1.33(b).

Note: Filing this rescission of a previous nonpublication request is considered the notice of a subsequent foreign or International filing required by 35 USC 122(b)(2)(B)(iii) and 37 CFR 1.213(c) if this rescission if filed no later than forty-five days (45) days after the date of filing of such foreign or international application. See 37 CFR 1.137(f) if a notice of subsequent foreign or International filing required by 35 USC 122(b)(2)(B)(iii) and 37 CFR 1.213(c) is **not** filed within forty-five days (45) days after the date of filing of the foreign or international application.

CERTIFICATE OF MAILING OR TRANSMISSION

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Commissioner For Patents, Box PG Pub, Washington, DC 20231, or facsimile transmitted to the U.S. Patent and Trademark Office on:

Name *(Print/Type)*	Marsha A. Townsend		
Signature	Marsha A. Townsend	***Date***	October 18, 2002

Burden Hour Statement: This collection of information is required by 37 CFR 1.213(b). The information is used by the public to rescind a previously filed request that an application not be published under 35 U.S.C. 122 (b) (and the PTO to process that rescission). Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This form is estimated to take 6 minutes to complete. This time will vary depending upon the needs of the individual case. Any comments on the amount of time you are required to complete this form should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, Washington, DC 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Assistant Commissioner for Patents, Washington, DC 20231.

OIPE JC55
SEP 23 2002
PATENT & TRADEMARK OFFICE

261 #9
10-26-02
PATENT
Withdrawn

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of

SEUNG HO HWANG, et al.

Application No. 10/036,234

Filed: December 24, 2001

For: **ENCODING METHOD AND SYSTEM FOR REDUCING INTER-SYMBOL INTERFERENCE EFFECTS IN TRANSMISSION OVER A SERIAL LINK**

Group Art Unit: 2614

Examiner: Unknown

TRANSMITTAL OF FORMAL DRAWINGS

400 Montgomery Street, Suite 1110
San Francisco, CA 94104
(415) 433-2250

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CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to ATTN: Official Draftsman, Commissioner for Patents, Washington, DC 20231, on September 18, 2002.

GIRARD & EQUITZ LLP Date: 09/18/02

By: Marsha A. Townsend
Marsha A. Townsend

ATTN: Official Draftsman
Commissioner for Patents
Washington, D.C. 20231

Sir:

Enclosed are five sheets of formal drawings for filing in the above-referenced case.

The Commissioner is hereby authorized to charge payment of any **additional** fees associated with this communication or credit any overpayment to Deposit Account No. 50-1697. **A duplicate copy of this sheet is enclosed**.

Respectfully submitted,

GIRARD & EQUITZ LLP

Dated: 9/18/02 By: Alfred A Equitz

Alfred A. Equitz
Reg. No.30,922

Attorneys for Applicant(s)

Attorney Docket No. SII-1000 [SIMG0115]

Rev. 02/14/01

OIPE
SEP 23 2002
PATENT & TRADEMARK OFFICE

Application No.: 10/036,234
Inventors' Name: SEUNG HO HWANG, et al.
Docket No.: SII-1000 [SIMG0115]
Alfred A. Equitz/(415) 433-2250
Group Art Unit: 2614
Sheet 1 of 5

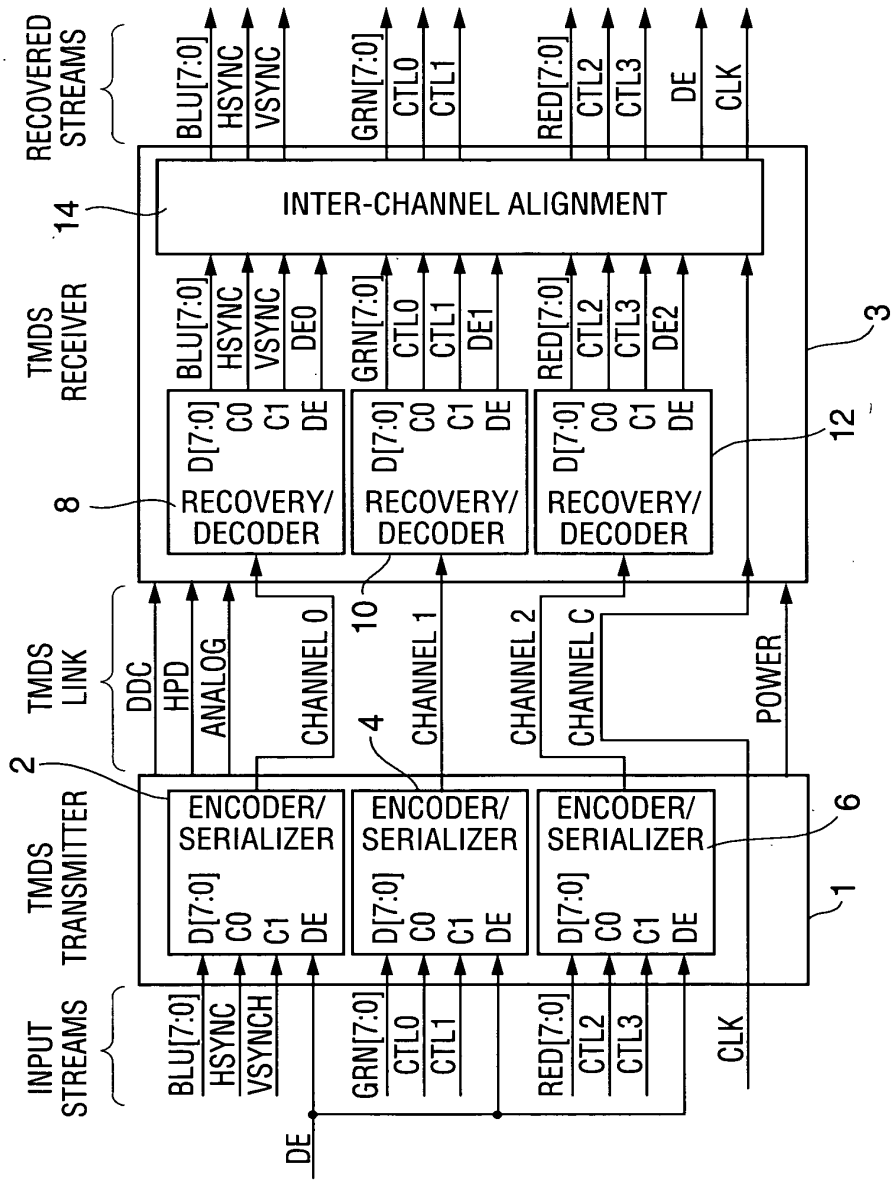


FIG. 1
(PRIOR ART)

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PATENT & TRADEMARK OFFICE

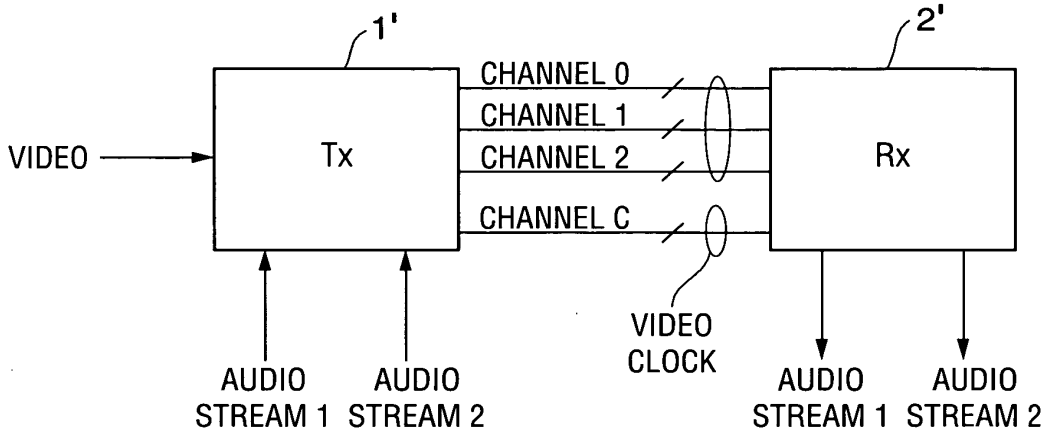


FIG. 2

	Input D7–D0	Hex	TMDS pattern
PRE-DATA GUARD BAND for Aux data	01010101	55	1100110010
AD0	01011011	5B	0011100101
AD1	10110101	B5	0110001101
AD2	11010011	D3	0010011101
AD3	11011001	D9	0100011101
AD4	01101101	6D	0111000101
AD5	10100100	A4	0011100110
AD6	10010010	92	0111000110
AD7	01000100	44	0011110010
AD8	00100010	22	0111100010
AD9	01001011	4B	1001110010
AD10	10010011	93	1000111010
GUARD BAND for video data and POST-DATA GUARD BAND for Aux data (and AD11)	10101011	AB	0011001101
AD12	01011010	5A	1100011001
AD13	01101100	6C	1000111001
AD14	10100101	A5	1100011010
AD15	10111010	BA	1100001101

FIG. 4

PATENT & TRADEMARK OFFICE
SEP 23 2002
U.S. PTO

Application No.: 10/036,234
Inventors' Name: SEUNG HO HWANG, et al.
Docket No.: SII-1000 [SIMG0115]
Alfred A. Equitz/(415) 433-2250
Group Art Unit: 2614
Sheet 3 of 5

Specific CTL	CTL [1:0]	Preamble (q0:q9)	Guardband (q0:q9)	GB (d7:d0)	Purpose
R (CTL [3:2])	00	0010101011	0011001101	0xAB	Video Preamble/Video Guardband/Post-Data Aux Guardband
G (CTL [1:0])	00	0010101011	0011001101	0xAB	Video Preamble/Video Guardband/Post-Data Aux Guardband
B (VSYNC:HSYNC)	XX	1 of 4 values	0011001101	0xAB	Video Preamble/Video Guardband
R (CTL [3:2])	01	1101010100	1100110010	0x55	Aux Preamble/Pre-Data Aux Guardband
G (CTL [1:0])	10	0010101010	1100110010	0x55	Aux Preamble/Pre-Data Aux Guardband
B (VSYNC:HSYNC)	XX	1 of 4 values	1 of 4 values	0x5B, 0xB5, 0xD3, 0xD9	Aux Preamble/Pre- or Post-Data Aux Guardband
R (CTL [3:2])	10	0010101010			VSync Window, HDCP enabled
G (CTL [1:0])	00	0010101011			VSync Window, HDCP enabled
B (VSYNC:HSYNC)	XX	1 of 4 values			VSync Window, HDCP enabled

FIG. 3

SEP 2 3 2002
PATENT & TRADEMARK OFFICE

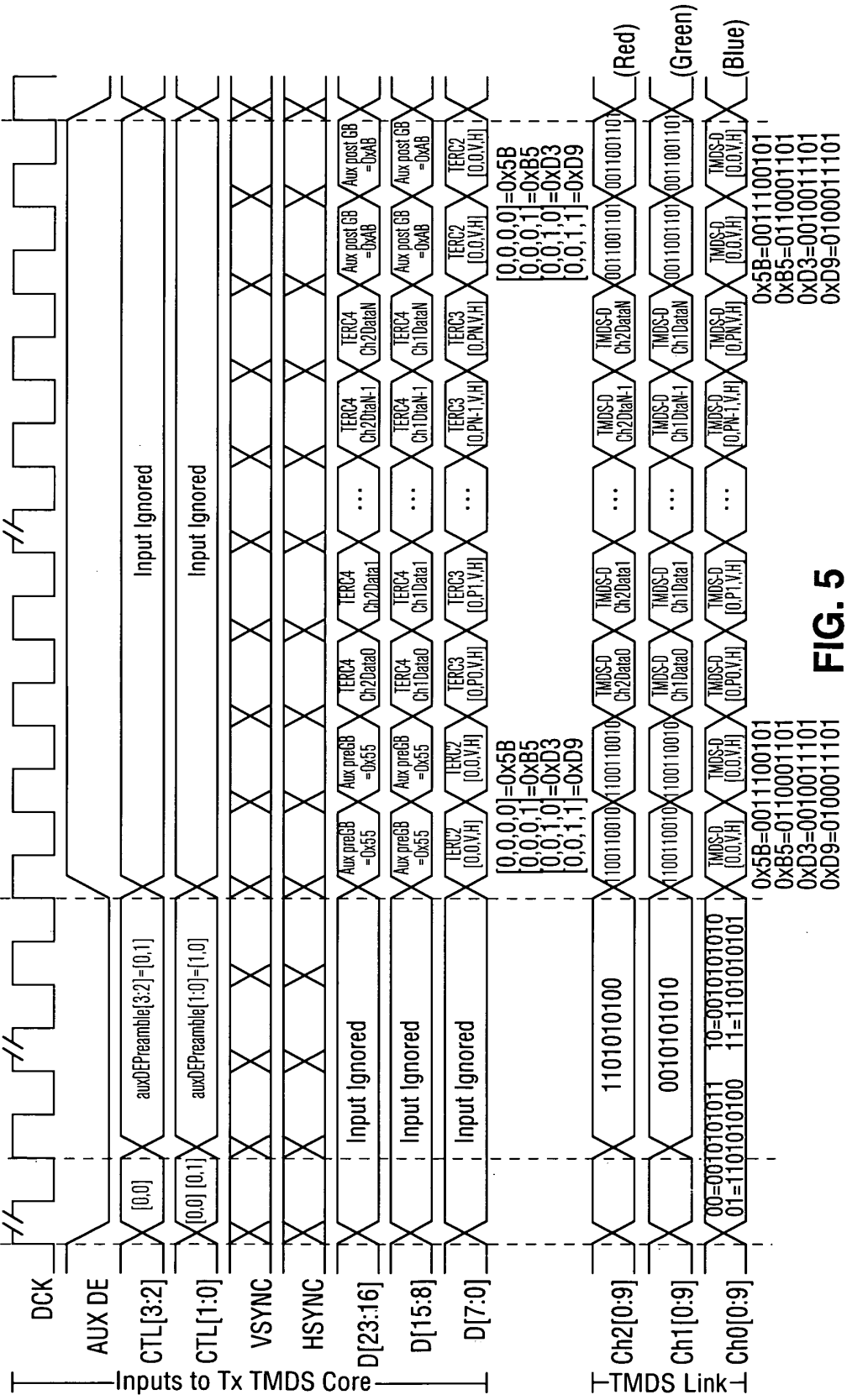


FIG. 5

OIPE
SEP 23 2002
PATENT & TRADEMARK OFFICE

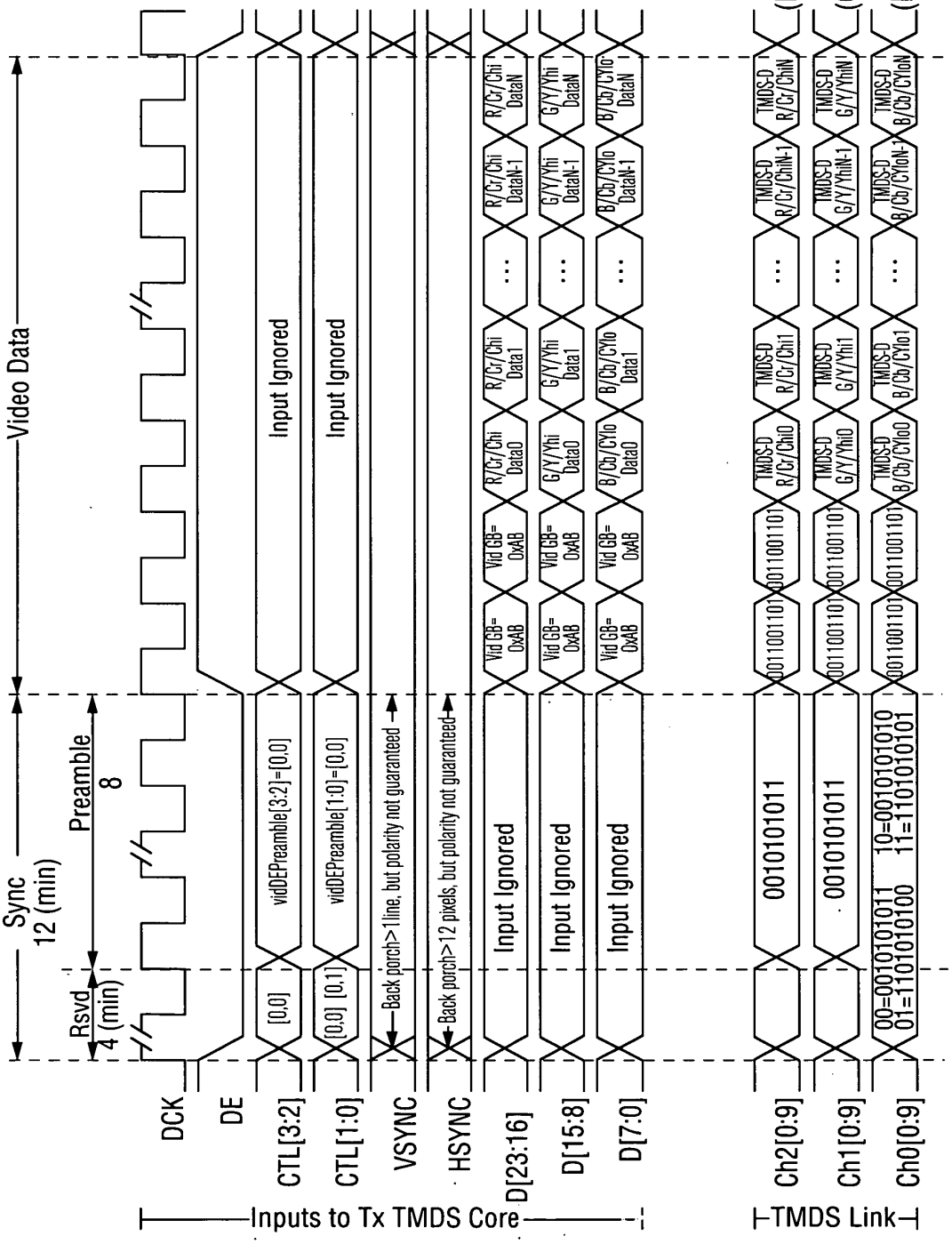


FIG. 6

OIPE JC44
JUL 30 2002
PATENT & TRADEMARK OFFICE

2614

PATENT

THE UNITED STATES PATENT AND TRADEMARK OFFICE

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AUG 05 2002
Technology Center 2600

In re Patent Application of

SEUNG HO HWANG, et al.

Application No. 10/036,234

Filed: December 24, 2001

For: **ENCODING METHOD AND SYSTEM FOR REDUCING INTER-SYMBOL INTERFERENCE EFFECTS IN TRANSMISSION OVER A SERIAL LINK**

Group Art Unit: 2614

Examiner: Unknown

INFORMATION DISCLOSURE STATEMENT

400 Montgomery Street
Suite 1110
San Francisco, CA 94104
(415) 433-2250

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to Commissioner for Patents, Washington, DC 20231, on July 26, 2002.

GIRARD & EQUITZ LLP Date: 07/26/02

By: Marsha A. Townsend
Marsha A. Townsend

Commissioner for Patents
Washington, D.C. 20231

Sir:

Applicants submit herewith patents, publications or other information [attached hereto and listed on the attached Form PTO-1449 (modified)] of which they are aware, which they believe may be material to the examination of this application and in respect of which there may be a duty to disclose in accordance with 37 CFR § 1.56.

This Information Disclosure Statement:

(a) [] accompanies the new patent application submitted herewith. 37 CFR § 1.97(a).

(b) [] is filed within three months after the filing date of the application or within three months after the date of entry of the national stage of a PCT application as set forth in 37 CFR § 1.491.

(c) [X] as far as is known to the undersigned, is filed before the mailing date of a first Office Action on the merits.

(d) [] is filed after the first office action and more than three months after the application's filing date or PCT national stage date of entry filing but, as far as is known to the undersigned, prior to the mailing date of either a final rejection or a notice of allowance, whichever occurs first, and is accompanied by either the fee ($180) set forth in 37 CFR § 1.17(p) **or** a certification as specified in 37 CFR § 1.97(e), as checked below.

(e) [] is filed after the mailing date of either a final rejection or a notice of allowance, whichever occurred first, and the Issue Fee has not been paid, and is accompanied by the fee ($130) set forth in 37 CFR § 1.17(i)(1) and a certification as specified in 37 CFR § 1.97(e), as checked below. This document is to be considered as a petition requesting consideration of the information disclosure statement.

[If either of boxes (d) or (e) are checked above, the following "certification" under 37 CFR § 1.97(e) may need to be completed.] The undersigned certifies that:

(f) [] Each item of information contained in the information disclosure statement was cited in a communication mailed from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this information disclosure statement.

(g) [] No item of information contained in this information disclosure statement was cited in a communication mailed from a foreign patent office in a counterpart foreign application or, to the knowledge of the undersigned after making reasonable inquiry, was known to any individual designated in 37 CFR § 1.56(c) more than three months prior to the filing of this information disclosure statement.

A list of the patent(s) or publication(s) is set forth on the attached Form PTO-1449 (Modified).

A copy of the items on PTO-1449 (Modified) is supplied herewith:

(h) [X] each (i) [] none (j) [] only those listed below:

Those patent(s) or publication(s) which are marked with an asterisk (*) in the attached form PTO-1449 (Modified) are not supplied because they were previously cited by or submitted to the Office in a prior application

no. , filed and relied upon in this application for an earlier filing date under 35 U.S.C. § 120.

A concise explanation of relevance of the items listed on form PTO-1449 (Modified) is:

(k) [X] not given

(l) [] given for each listed item

(m) [] given for only non-English language listed item(s) [Required]

(n) [] is in the form of an English language copy of a Search Report from a foreign patent office, issued in a counterpart application, which refers to the relevant portions of the references [copy attached].

The Examiner is reminded that a "concise explanation of the relevance" of the submitted items "may be nothing more than identification of the particular figure or paragraph of the patent or publication which has some relation to the claimed invention," MPEP § 609.

While the information and references disclosed in this Information Disclosure Statement may be "material" pursuant to 37 CFR § 1.56, it is not intended to constitute an admission that any patent, publication or other information referred to therein is "prior art" for this invention unless specifically designated as such.

In accordance with 37 CFR § 1.97(g), the filing of this Information Disclosure Statement shall not be construed to mean that a search has been made or that no other material information as defined in 37 CFR § 1.56(a) exists. It is submitted that the Information Disclosure Statement is in compliance with 37 CFR § 1.98 and MPEP § 609 and the Examiner is respectfully requested to consider the listed references.

[X] The Commissioner is hereby authorized to charge our Deposit Account No. **50-1697** for any fees required in connection with the filing of this Information Disclosure Statement. **A duplicate copy of this Notice is enclosed for this purpose.**

Respectfully submitted,

Dated: 7/26/02 By _____

Alfred A. Equitz
Registration No. 30,922
Tel. No. 415/433-2250

Our File: SII-1000 [SIMG0115]

FORM PTO-1449 (Modified) U.S Dept. of Commerce (Rev. 7-80) Patent and Trademark Office **INFORMATION DISCLOSURE CITATION** (Use several sheets if necessary)	Atty Docket No. SII-1000 [SIMG0115]	Appln. No. 10/036,234
	Applicant(s) SEUNG HO HWANG, et al.	
	Filing Date December 24, 2001	Group 2614

JUL 30 2002 PATENT & TRADEMARK OFFICE

RECEIVED AUG 05 2002 Technology Center 2600

U.S. PATENT DOCUMENTS

*Examiner Initials		Document Number	Date	Name	Class	Subclass	Filing Date
	AA	5,974,464	10/26/99	SHIN et al.	709	231	09/30/96
	BB	5,905,769	05/18/99	LEE et al.	375	376	05/07/96
	CC	6,191,822 B1	02/20/01	SMYERS	348	552	06/20/97
	DD	5,506,932	04/09/96	HOLMES et al.	395	2.14	04/16/93
	EE	5,541,662	07/30/96	ADAMS et al.	348	460	09/30/94
	FF	5,523,795	06/04/96	UEDA	348	480	08/16/94
	GG	5,150,211	09/22/92	CHARBONNEL et al.	358	143	08/28/90
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*Examiner Initials		Document Number	Date	Country	Class	Subclass	Translation YES	NO
	JJ	WO 00/16525	23.03.2000	PCT	H04L	25/02		

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	KK	*High-Bandwidth Digital Content Protection System,* Revision 1.0, by Intel Corporation, February 17, 2000, pages 1-60.

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* Examiner: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

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	NN	*High-Bandwith Digital Content Protection System Revision 1.0 Erratum,* by Intel Corporation, March 19, 2001, pages 1-9.
	OO	*Upstream Link for High-bandwidth Digital Content Protection,* Revision 1.00, by Intel Corporation, January 26, 2001, pages 1-38.
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Published

(54) Title: A SYSTEM AND METHOD FOR SENDING AND RECEIVING DATA SIGNALS OVER A CLOCK SIGNAL LINE

(54) Titre: SYSTEME ET PROCEDE D'ENVOI ET DE RECEPTION DE SIGNAUX DE DONNEES PAR UNE LIGNE DE SIGNAL D'HORLOGE

(57) Abstract

The system preferably includes a unique transmitter that sends both clock and data signals over the same transmission line. The receiver uses the same transmission line to send data signals back to the transmitter. The transmitter comprises a clock generator, a decoder and a line interface. The clock generator produces a clock signal that includes a variable position falling edge. The falling edge position is decoded by the receiver to extract data from the clock signal. The receiver comprises a clock re-generator, a data decoder and a return channel encoder. The clock re-generator monitors the transmission line, receives signals, filters them and generates a clock signal at the receiver from the signal on the transmission line. The return channel encoder generates signals and asserts them on the transmission line. The signal is asserted or superimposed over the clock and data signal provided by the transmitter.

(57) Abrégé

L'invention concerne un système comprenant de préférence un émetteur unique qui envoie des signaux d'horloge et de données par la même ligne de transmission. Le récepteur utilise la même ligne de transmission pour renvoyer des signaux de données à l'émetteur. L'émetteur comprend un générateur d'horloge, un décodeur et une interface de ligne. Le générateur d'horloge produit un signal d'horloge comprenant un flanc arrière à position variable. Le récepteur décode la position du flanc arrière pour extraire des données du signal d'horloge. Le récepteur comprend un re-générateur d'horloge, un décodeur de données et un codeur de canal retour. Le re-générateur d'horloge contrôle la ligne de transmission, reçoit des signaux, les filtre et génère dans le récepteur un signal d'horloge provenant du signal dans la ligne de transmission. Le codeur de canal retour génère des signaux et les active dans la ligne de transmission. Le signal est activé ou superposé au signal d'horloge et de données émis par l'émetteur.

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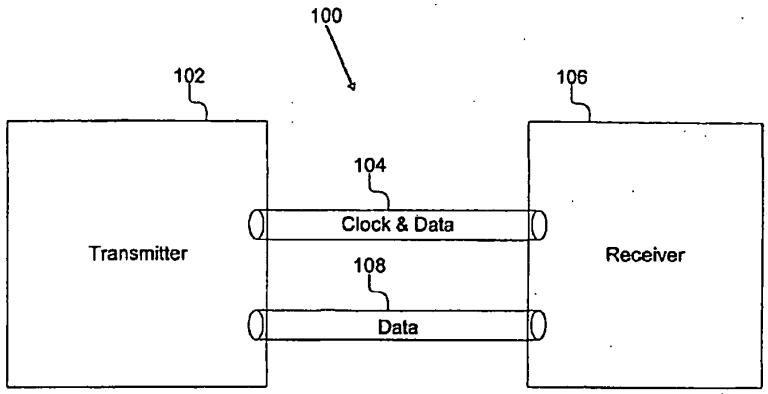
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(54) Title: A SYSTEM AND METHOD FOR SENDING AND RECEIVING DATA SIGNALS OVER A CLOCK SIGNAL LINE



(57) Abstract

The system preferably includes a unique transmitter that sends both clock and data signals over the same transmission line. The receiver uses the same transmission line to send data signals back to the transmitter. The transmitter comprises a clock generator, a decoder and a line interface. The clock generator produces a clock signal that includes a variable position falling edge. The falling edge position is decoded by the receiver to extract data from the clock signal. The receiver comprises a clock re-generator, a data decoder and a return channel encoder. The clock re-generator monitors the transmission line, receives signals, filters them and generates a clock signal at the receiver from the signal on the transmission line. The return channel encoder generates signals and asserts them on the transmission line. The signal is asserted or superimposed over the clock and data signal provided by the transmitter.

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Description

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A System and Method For Sending and Receiving Data Signals Over a Clock Signal Line

Inventors: Gyudong Kim, Min-Kyu Kim & Seung Ho Hwang

Cross-References To Related Applications

This application is a utility conversion of U.S. Patent No. 60/099,770, entitled "Embedded Back Channel For TMDS" by Gyudong Kim, filed September 10, 1998.

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates generally to the field of data communications, and more particularly, to the transmission of clock and data signals. Still more particularly, the present invention relates to the transmission of clock signals and data signals on the same transmission line in transition minimized differential signaling (TMDS) system.

2. Description of the Background Art

There are a variety of prior art systems and method for transmitting data between a transmitter and a receiver. Various serial links and other methods for transmitting data and clock signals are well known. However, most such schemes provide a single line or channel dedicated for the transmission of the clock signals and other signal lines or channels dedicated for the transmission of data. Once such system is described by Kyeongho Lee, Sungjoon Kim, Gijung Ahn, and Deog-kyoon Jeong in "A CMOS Serial Link For Fully Duplexed Data Communication," IEEE Journal of Solid State Circuits, Vol. 30, No. 4 pp. 353-364, April 1995.

The present invention will be discussed in the context of transition minimized differential signaling (TMDS), however, those skilled in the art will recognize that the present invention is applicable in various other data communication contexts. In TMDS, four signal lines are provided, and each signal line is preferably a differential pair. One signal line

is a for a low speed clock signal and the three other signal lines are for high-speed data transmission.

One important aspect of all data communication systems is to maximize the bandwidth provided by the data channels. However, most systems include a variety of control signals that must be sent between the transmitter and the receiver to ensure proper operation, and maintain synchronization between the transmitter and the receiver. For example, it is not uncommon for as much as 20% of the bandwidth to be used for framing an synchronization in serial communication. One problem is that the bandwidth available for data is typically reduced because the data signal lines must be used to transmit these control signals between the transmitter and receiver. Yet another problem is latency in transmitting the control signals to the recipient. Especially in video data communication, much of the data must be transmitted in blocks during which control signals cannot be sent. For example, when transmitting data from a controller to a flat panel, the data is transmitted, and then there is a data enable period corresponding to the blanking period in CRT display that is used to send control and synchronization signal. Only during that data enable period can the control signals be sent under most protocols. Therefore, there is latency imposed on transmitting control signals to the receiver. Thus, there is need for a system that can provide for control signaling between the transmitter and the receiver without decreasing the available bandwidth for data transfer, and while reducing the latency in sending control signals.

Yet another problem in the prior art is that most systems do not provide a mechanism to get signals from the receiver back to the transmitter. In other words, there is not a return channel for communication. Some systems have provided additional signal lines, however, their addition and interface add significant complication, require re-wiring and create other problems that make the addition of a physical line unworkable. Another approach is to add a second transmitter, second receiver and signal lines. However, this essentially doubles the hardware

requirements making such a solution too expensive. Furthermore, such duplication is overkill for the amount of data that needs to be sent between the transmitter and the receiver, especially when the application is one of sending video data from a transmitter to a receiver such as communication between a graphic controller and a video display device.

Therefore, there is a need for a system and method for that uses the clock signal line also for transmitting data signals between the transmitter and the receiver and vice-versa.

SUMMARY OF THE INVENTION

The present invention overcomes the deficiencies and limitations of the prior art with a unique data communication system. The system preferably includes a unique transmitter and receiver coupled by a transmission line. The transmitter sends both a clock signal and data signals over the transmission line to the receiver. The receiver uses the same transmission line to send data signals back to the transmitter.

The transmitter preferably comprises a clock generator, a decoder and a line interface. The clock generator produces a clock signal that includes a variable position falling edge. The falling edge position is decoded by the receiver to extract data in addition to the clock signal. The line interface couples the output of the clock generator to the transmission line. The line interface also couples the transmission line to the decoder and in doing so removes the signals from the clock generator. The decoder receives the signals from the line interface and decodes the signal to determine the data being sent from the receiver to the transmitter on the same line used to send the clock and data from the transmitter to the receiver.

The receiver preferably comprises a line interface, a clock re-generator, a data decoder and a return channel encoder. The clock re-generator, the data decoder and the return channel encoder are coupled to the transmission line by the line interface. The clock re-generator monitors the transmission line, receives signals, filters them and generates a clock signal at the receiver from the signal on the transmission line.

The data decoder similarly is coupled to receive the signals on the transmission line, and filters and decodes the signals to produce data signals. This is preferably done by determining the position of the falling edge of the clock signal and translating the falling edge position into bit values. In contrast, the return channel encoder generates signals and asserts them on the transmission line. These signals are asserted or superimposed over the clock & data signals provided by the transmitter.

These and other features and advantages of the present invention may be better understood by considering the following detailed description of a preferred embodiment of the invention. In the course of this description, reference will frequently be made to the attached drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a block diagram of system including the combined clock and data signal line of the present invention.

Figure 2 is a block diagram of a portion of the transmitter showing a clock generator, decoder and a line interface.

Figure 3 is a block diagram of a preferred embodiment of the clock generator constructed in accordance with the present invention.

Figure 4 is a timing diagram illustrating various clock signals that the clock generator of the present invention produces.

Figure 5A is a block diagram of a preferred embodiment of the line interface constructed in accordance with the present invention.

Figure 5B is a circuit diagram of the preferred embodiment of the line interface constructed in accordance with the present invention.

Figure 6A is a block diagram of a first embodiment of the decoder at the transmitter constructed in accordance with the present invention.

Figure 6B is a block diagram of a second embodiment of the decoder at the transmitter constructed in accordance with the present invention.

Figure 7 is a block diagram of a first embodiment of portions of the receiver relating to the present invention.

Figure 8 is a block diagram of a first embodiment of a clock re-generator of the receiver.

Figure 9 is a block diagram of a preferred embodiment of a data decoder of the receiver.

Figure 10A is a block diagram of a first embodiment of a return channel encoder of the receiver.

Figure 10B is a block diagram of a second and alternate embodiment of a return channel encoder of the receiver.

Figure 11A is a timing diagram illustrating signals on the transmission line, and the clock and data signals generated by the transmitter for return to zero signaling.

Figure 11B is a timing diagram illustrating signals on the transmission line, the data signal sent by the receiver, and the clock and data signals recovered by the receiver for return to zero signaling.

Figure 12A is a timing diagram illustrating signals on the transmission line, and the clock and data signals generated by the transmitter for non-return to zero signaling.

Figure 12B is a timing diagram illustrating signals on the transmission line, the data signal sent by the receiver, and the clock and data signals recovered by the receiver for non-return to zero signaling.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Referring now to Figure 1, a block diagram of system 100 including the combined clock and data signal line of the present invention is shown. The system 100 preferably includes a transmitter 102, a clock transmission line 104, a receiver 106 and one or more data transmission lines 108. The transmitter 102 preferably provides a clock signal as well as data signals to the receiver 106 via the clock transmission line 104. These data signals are in addition to those provided to the receiver

106 via the high speed data transmission lines 108. The receiver 106 receives the signals on the transmission line 104 and from them, generates the clock and data signals at the receiver 106. These data signals on the clock line 104 are again in addition to the data signals that the receiver 106 recovers from the data transmission line 108. The transmitter 102 and the receiver 106 include logic for sending and receiving the data from data transmission line 108. This logic preferably includes transition control, DC balancing, and encoding/decoding in a conventional manner. For example, in addition to the components of the present invention for receiving and sending data and clock signals on the clock transmission line 104 that will be described below, the transmitter 102 and the receiver 106 respectively include conventional data transmission logic for TMDS such as that provided in PanelLink by Silicon Image of Cupertino, California. For ease of understanding that logic and the data transmission line 108 are omitted from the discussion below and the remaining figures. Those skilled in the art will also realize that while shown as a single line, the clock transmission line 104 and the data transmission line 108 are preferably each a differential pair of signal lines, and the signal is carried on the differential pair of lines. Furthermore, those skilled in the art will understand the preferred embodiment for the data transmission line 108 is three pairs of data lines.

Transmitter

Referring now to Figure 2, a preferred embodiment of the transmitter 102 is shown in more detail. The transmitter 102 preferably comprises a clock generator 200, a line interface 204, and a decoder 202.

The clock generator 200 has a first input, a second input and an output. The clock generator 200 produces a clock signal that is encoded with data. The data is encoded into the clock signal by varying the modulation of the falling edge of the clock signal. In other words, the position of the falling edge of the clock relative to the rising edge indicates different

data values. This is particularly advantageous because it preserves the rising edge of the clock for clock recovery. All the activity for a bi-directional data link on the clock transmission line 104 is centered around the falling edge of the clock from the transmitter 102. While most of the present invention will be described in the context of the falling edge of the clock having two different positions, Figures 3 and 4 will also be described in the context of the falling edge of the clock having five different positions. Each of the four positions representing two bit values and one position representing no data. The first input of the clock generator 200 is coupled to line 214 to receive a clock signal either from another portion of the transmitter 102 or from a oscillator or other conventional clock source. The second input of the clock generator 200 is coupled to line 216 to receive control/data signals. These control/data signals dictate the data or no data that is transmitted as part of the clock signal. These control/data signals may be from another portion of the transmitter 102 or from off chip control logic. The output of the clock generator 200 is provided on line 210 that is coupled to an input of the line interface 204. The output of the clock generator 200 provides a CGOut signal.

While the present invention is described throughout this application as preserving the rising edge for the clock signal and centering all the bi-directional data transmission about the falling edge, those skilled in the art will realize that an inverse scheme where the falling edge is preserved for recovering the clock and changes in position of the rising edge is used for encoding data is within the spirit and scope of the present invention.

The line interface 204 has an input, an output and a bi-directional port. The line interface 204 couples the clock generator 200 and the decoder 202 to the clock transmission line 104. The input of the line interface 204 preferably couples line 210 to the clock transmission line 104 so that the CGOut signal may be asserted over the clock transmission line 104. The

output of the line interface 204 is coupled to the input of the decoder 202 by line 212. The line interface 204 advantageously receives the signal on the clock transmission line 104, removes the CGOut signal as will be described below with reference to Figures 5A and 5B, and sends the filtered signal as the input to the decoder 202. The bi-directional port of the line interface 204 is coupled to the clock transmission line 104.

The decoder 202 receives the filtered signals from the transmission line 104 and decodes the signals to generate the data sent by the receiver 106. The decoder 202 preferably performs an inverse function to the encoder 704 (See Figure 7) of the receiver 106 as will be described below.

Referring now to Figures 3 and 4, the preferred embodiment for the clock generator 200 will be described. While the clock generator 200 will now be described as providing a clock signal having a falling edge in five possible locations to send two bits of data or no data in addition to the clock signal, those skilled in the art will recognize that this is only by way of example. The clock generator 200 could be configured to send from 1 to *n* bits of data per clock cycle depending on the clock frequency and the number of possible locations for the falling edge of the clock signal. In general, *n* locations of the falling edge will allow up to $\log_2 n$ bits of data to be transferred per clock cycle. The number of locations for the falling edge is limited only in that the first location must be such that the pulse width is greater than the logic-threshold crossing time of the rising edge, which may be viewed to be jitter by the phase-locked loop at the receiver 106. In other words, the thresholds for set up and hold time in the logic must be sufficient to recognize a rising edge as the beginning of the clock cycle.

The clock generator 200 preferably generates a clock signal at the dot clock frequency, or the frequency used by device (not shown) connected to the receiver 106 for the display of the data. The maximum symbol rate provided by data transfer as part of the clock signal matches the dot clock frequency. For

example, if the dot clock is 100 MHz, the symbol rate is 100 Msymbols/s. The actual data rate will depend on the modulation methods and the number of bits per clock or symbol that can sent. If simple binary modulation is used, then the bit rate is the same and the clock rate with would provide an additional 100Mb/s for control signals.

The clock generator 200 preferably comprises a monostable multivibrator 306, a delay-locked loop 300, a multiplexer 302, a first NAND gate 304 and a second NAND gate 306. The clock generator 200 preferably uses only return to zero signaling for sending the clock and data signals. Non-return to zero signaling cannot be used for sending from the transmitter 102. The clock signal is received on line 214 and provided as input to the input of the one shot or monostable multivibrator 306. The monostable multivibrator 306 is provided to generate a signal with a narrower pulse width than the clock signal. This is advantageous for use in other portions of the clock generator 200. In an alternated embodiment, the one shot 306, may be replaced by a plurality of monostable multivibrators each respectively coupled in series with an output signal line 308 of the delay locked loop 300. Such an alternate embodiment provides more flexibility in the design of the delay locked loop 300 at the cost of additional monostable multivibrator as will be understood by those skilled in the art. The output of the monostable multivibrator 306 is coupled to the input to the delay-locked loop 300. The delay-locked loop 300 is of a conventional type and in response to a signal at its input, provides a plurality of outputs, each output being the same as the input only shifted in phase. The falling edge is modulated using a delay-locked loop 300. The falling edge is chosen from one of the phases provided by the delay-locked loop 300. It is preferable that the selected phases from the delay-locked loop 300 be the ones close to a 50% duty cycle. The delay-locked loop 300 preferably provides five output signals: $\phi 0$, $\phi 1$, $\phi 2$, $\phi 3$, $\phi 4$, and ϕn. The $\phi 0$ signal is the clock signal unchanged. The $\phi 1$, $\phi 2$, $\phi 3$, $\phi 4$, and ϕn are each phase shifted more with

respect to the previous ϕ signal. The $\phi 0$ is coupled to a first input of the first NAND gate 304. The output of the first NAND gate 304 is provided on line 210 and provides the CGOut signal. The first NAND gate 304 is cross coupled with the second NAND gate 306 to form a set-reset latch. A rising edge on the $\phi 0$ causes the output of first NAND gate 304 to be set high or asserted until reset to low by the second NAND gate 306. The remaining signals from the delay-locked loop 300, $\phi 1$, $\phi 2$, $\phi 3$, $\phi 4$, and ϕn are coupled to respective data inputs of the multiplexer 302. The control input of the multiplexer 302 is coupled to line 216 to receive control/data signals. In response to the control/data signals on line 216, the multiplexer 302 will couple one of the signals from the delay-locked loop 300, $\phi 1$, $\phi 2$, $\phi 3$, $\phi 4$, and ϕn, to the input of the second NAND gate 306. Thus, the rising edge on the selected signal from the delay-locked loop 300, $\phi 1$, $\phi 2$, $\phi 3$, $\phi 4$, and ϕn, will cause the latch to be reset and create a falling edge on the output of the first NAND gate 304, and thus, line 210. Thus, it is apparent that using the control/data signals to select one of the signals, the position of the falling edge can be selected. For example control signals such as shown in Table I may be used to control the position of the falling edge.

Control/data Signal(216)	NAND-gate 306 input	Falling edge Position	Data Sent
000	$\phi 1$	T0	00
001	$\phi 2$	T1	01
100	$\phi 3$	T2	00
010	$\phi 4$	T3	10
011	ϕn	T4	11

Table I

Those skilled in the art will recognize how the clock generator 200 could be modified to create any number of different falling edge positions for the CGOut signal. Referring also to Figure

4, a timing diagram of the clock/ϕ0, ϕ1, ϕ2, ϕ3, ϕ4, and ϕn and the possible CGOut signals are shown. There are five possible CGOut signals. First, the clock/ϕ0 signal is unchanged which is just a the input signal with falling edge at time T2 and sending no data. The remaining CGOut1-CGOut4 signals are have a falling edge with an adjusted position to times T0, T1, T3, T4 respectively each representing a different two bit value. Thus, the preferred embodiment is able to transfer two bits per clock from the transmitter 102 to the receiver 106 in addition to the clock signal. Since the receiver 106 uses only the rising edge to detect and define clock cycles, the present invention uses this to achieve the data transfer without any performance disadvantages. For the receiver 106 embodiments described below where only one bit of data per clock is sent, the clock generator 200 would output falling edges at times T1 and T3.

The ability of the present invention to use the clock transmission line 104 to send data from the transmitter 102 to the receiver 104 is particularly advantageous because it eliminates signal latency present in the prior art. With the present invention as applied to TMDS, the transmitter 102 does not need to wait for the next available data enable (DE) low period to send the signals. This greatly decreases the maximum transfer latency. Moreover, the present invention can be used in other serial links that require very short latency. For example, if a fixed bit location is assigned for each link (a fixed bandwidth per fixed dot clock) the synchronization overhead for those channels can be minimized. In this way, the latency of such links can be reduced to 1 frame cycle and the cable flight time. The other bits of the payload can be used with variable bandwidth but the synchronization latency or delay could be longer.

Yet another advantage of the forward channel for sending data from the transmitter 102 to the receiver 106 is that it is fully backward compatible with prior TMDS designs and protocols. Thus, whether the receiver 106 is able to receive data from the transmitter 102 or not, the clock signal is unaffected by the

addition of data to the signal. Moreover, a receiver 106 will not have problem recovering the clock even if data (for either the transmitter 102 or the receiver 106) is added in accordance with the present invention to the signal on the transmission line 104. Therefore, the transmitter 102 of the present invention can still be used even if the receiver does not have the capability to receive the data signal.

Referring now to Figure 5A and 5B, the preferred embodiment for the line interface 204 is shown. The line interface preferably comprises a first amplifier 502, a second amplifier 506, a differential amplifier 504 and a line terminator or pull-up resistor 508. The line interface 204 is essentially a bi-directional bridge that allows transmission of data while receiving data from the receiver 106. The input of the first amplifier 502 is coupled to line 210 to receive the CGOut signal. The input of the second amplifier 506 is similarly coupled. The output of the first amplifier 502 is coupled to apply an amplified version of the CGOut signal to clock transmission line 104. The clock transmission line 104 is also coupled by the pull-up resistor 508 to high voltage to form a line terminator. The pull-up resistor 508 could instead be coupled to ground or half V_{DD} as will be understood to those skilled in the art for alternate embodiments of the line terminator. The clock transmission line 104 is also coupled an input of the differential amplifier 504. The other input of the differential amplifier 504 is coupled to the output of the second amplifier 506. The second amplifier 506 also receives the CGOut signal and amplifies the signal, but to the same or lesser extent than the first amplifier 502. The differential amplifier 504 subtracts the CGOut signal from the signal received from the clock transmission line 104. Thus, the output of the differential amplifier 504 that is provided on line 212 includes predominately the signals asserted by the receiver 106 on the clock transmission line 104 and not the CGOut signal. It should be noted that an identical circuit with inputs and output

coupled differently may also be used in the receiver 106 as will be described below with reference to Figure 7.

Referring also now to Figure 5B, a circuit diagram for one exemplary embodiment for the line interface 204 is shown. The connections to the signal lines 210 and 104 are shown with reference numerals for clarity and ease of understanding. The signals preferably use differential pairs are indicated by reference numerals "a" and "b" as will be understood to those skilled in the art. The transistors and other components forming the second amplifier 506 and the differential amplifier 504 are shown grouped within dashed boxes as will be understood to those skilled in the art. The remaining transistors and other components from the first amplifier (not labeled in Figure 5B). It should be noted that some of the transistors in the second amplifier 506 are for impedance matching, and have their gates coupled to signal line 522 to be biased for impedance matching in a conventional manner. Some of the transistors in the differential amplifier 504 are also coupled to line 520 for biasing. In alternate embodiments, the outputs of the differential amplifier 504 could be coupled to line 520 and thereby provide a single output signal as will be realized by those skilled in the art. Those skilled in the art will further recognize that in alternative embodiments, various other conventional bi-directional buffers could be used in place of the circuits shown in Figures 5A and 5B.

Referring now to Figures 6A and 6B, two alternate embodiments for the decoder 202 are shown. The embodiment for the decoder 202 is dependent on the type of signaling being used by the corresponding encoder 704 (See Figure 7 and below) in the receiver 106. Figure 6A shows a block diagram of the first embodiment of the decoder 202a at the transmitter 106 for use when the receiver 106 sends the data in a non-return to zero (NRZ) signaling. As shown in Figure 6A, when the receiver 106 sends data in NRZ (non-return to zero) manner and toggles data at the fictitious falling edge (since the clock toggles its falling edge randomly in accordance with the present invention),

since the delay is a function of cable delay, at the transmitter side, it is not predictable where the relative location of the data transition will be, even thought it may have been obvious at the receiver side. Because of this ambiguous delay, the decoder 202a oversamples the data provided from the clock transmission line 104/212. Since the incoming data rate is the same is outgoing data rate, the present invention generates multiple phases of clocks from the clock signal on line 214. Using these clocks, the signal line 212 is sampled multiple times per data period to locate a data transition. Once the transition is detected, it is used as the data boundary.

As shown in Figure 6A, the first embodiment of the decoder 202a preferably comprises a delay-locked loop 602, a sampling unit 604, a data generator and a transition detector 608. The delay-locked loop 602 has an input coupled to receive the clock signal on line 214. The same delay-locked loop could be used in both the clock generator 200 and the decoder 202. The delay-locked loop 602 is of a conventional type and provides a plurality of version of the clock signal phase shifted. Outputs of the delay-locked loop 602 are coupled to respective inputs of the sampling unit 604. The sampling unit 604 includes control logic for generating a signal on a first output that controls when the transition detector 608 samples and latches the signal on line 212. For example, the sampling unit 604 can generate this control signal for every rising edge seen at the input from the delay-locked loop 602. The first output is coupled to an input of the transition detector 608. The sampling unit 604 also provides a time signal on a second output indicating the signals from the delay-locked loop 602 that have transitioned, and thus, the time within the clock cycle. The second output of the sampling detector 604 is coupled to an input of the data generator 606. The transition detector 608 has an input coupled to line 212 to receive the signal from the receiver 106. The transition detector 608 detects transitions in the signals on the line 212. When a transition is present the transition detector 608 asserts its output. The data generator 606 is

coupled to the sampling unit 604 to receive a signal indicating the time within the clock cycle and the transition detector 608 to identify when the transition occurs. Using this information, the data generator 606 outputs the bit values corresponding to when the transitions occur. For example if the transition is before the time for a falling edge of the clock if it had a 50% duty cycle then the data generator 606 may output a 1 if after the data generator 606 could output a 0 if the data rate were one bit per clock cycle. Those skilled in the art will recognize how the data generator 606 could be modified according to the number of bits per clock cycle transmitted by the receiver 106. The output of the data generator 606 is provided on line 218 for use by the transmitter 102.

Figure 6B shows an alternate embodiment for the decoder 202a. When receiver 106 sends data in return to zero (RZ) manner, the rising edge of the incoming clock is preferably used as the data reference point, and a phase in the middle of those consecutive rising edges is generated and used to sample the incoming data at that point. Thus, the decoder 202a comprises merely a delay-locked loop 650 and a flip-flop 620. The delay-locked loop 650 preferably provides a signal that has a rising edge in about the middle of the clock cycle such as $\phi 3$. This signal is coupled to the clock input of the flip-flop 620 to cause the flip-flop 620 to latch near the middle of the clock cycle. The data input of the flip-flop 620 is coupled to line 212 to receive the data signal sent by the receiver 106 and the D output of the flip-flop 620 provides the data output and is coupled to line 218.

Those skilled in the art will recognize that the decoder 202 may alternatively formed as an integrator type receiver where the period of the clock is subdivided and the integrator integrates over the subdivided time periods and compares the integration results. The signal is effectively integrated and dumped for comparison to determine the data values.

Receiver

Figure 7 shows a preferred embodiment for the receiver 106 constructed in accordance with the present invention. The receiver 106 preferably comprises a line interface 706, a clock re-generator 700, a data decoder 702, a delay compensator 708 and a return channel encoder 704.

The line interface 706 is preferably identical to that described above with reference to Figure 5A and 5B. However, for the receiver 106, the line interface 706 is completely optional and the receiver 106 can operate without it. The line interface 706 buffers the signals and filters them for better use in recovery. The line interface 706 has an input, an output and a bi-directional port. The bi-directional port is coupled to the clock transmission line 104. The input of the line interface 706 is coupled to line 720 to receive the output of the return channel encoder 704. The output of the line interface 706 is coupled to line 722 to provide input signals to the clock re-generator 700 and the data decoder 702. For ease of understanding reference numerals for the line interface 706 have been added to Figure 5A.

The clock re-generator 700 has an input and an output. The input of the clock re-generator 700 is coupled to receive the signals on the clock transmission line 104 via line 722 from the line interface 706. The clock re-generator 700 monitors the transmission line 104, receives signals, filters them and generates a clock signal at the receiver 106. The output of the clock re-generator 700 is coupled to line 710 and provides the clock signal for the receiver 106 to use in recovering data from the data channels 108. The clock re-generator 700 advantageously only uses the rising edges of the signals on the transmission line 104 to regenerate the clock signal at the receiver 106. This allows the falling edge position and voltage level to be used for other data transfer. The preferred embodiment for the clock re-generator 700 is simply an amplifier that can provide and amplified version of the signal to other digital logic receiving the clock. Referring now also to Figure 8, another embodiment for the clock re-generator 700 is shown.

In Figure 8, the clock re-generator 700 is a phase-locked loop 800 that has an input that is coupled to the transmission line 104 and an output that provides the clock as a square wave. The phase-locked loop 800 is a conventional type and includes a phase detector 802, an amplifier and filter 804 and a voltage controlled oscillator 806. These components 802, 804, 806 are coupled in a conventional manner with the input of the phase detector 802 coupled to line 104 and the output of the voltage controlled oscillator providing the clock signal and being feed back to the phase detector 802. Those skilled in the art will recognize that various other embodiments of phase-locked loops could be used for the clock re-generator 700 since it is only necessary to detect the rising edges on the transmission line 104 and produce a clock signal therefrom. Alternate embodiments for the clock re-generator 700 could also use a delay-locked loop.

The data decoder 702, like the clock re-generator 700, has an input coupled to receive the signals on the transmission line 104 via line 722 from the line interface 706. The data decoder 702 filters and decodes the signals to produce data signals that are output on line 712. The data decoder 702 also has another input coupled to line 710 to receive the recovered clock signal from the clock re-generator 700. This is preferably done by determining the position of the falling edge of the clock signal and translating the falling edge position into bit values. The data being sent from the transmitter 102 to the receiver 106 is valid on the falling edge of the clock. Referring also now to Figure 9, a preferred embodiment for the data decoder 702 will be discussed. The preferred embodiment of the data decoder 702 is very similar to the second embodiment of the decoder 202b of the transmitter 102. The data decoder 702 differs only in its coupling to other components which is shown in Figure 9. The data decoder 702 includes a delay-locked loop 650 and a flip-flop 620. The clock input of the delay-locked loop 650 is coupled to line 710 to receive the regenerated clock signal. The data input to the flip-flop 620 is coupled to line 722 to

receive the filter data signals from the transmission line 104. The output of the flip-flop 620 provides the data output and is coupled to line 712. The operation is same as has been described above with reference to Figure 6B.

The delay compensator 708 is coupled to line 710 to receive the recovered clock signal. The delay compensator 708 adjusts the recovered clock signal to compensate for propagation delay over the transmission line 104 and propagation delay in recovering the clock such that the signal used to time the sending of data back to the transmitter 102 will have timing that matches the original clock signal on the transmitter side of the clock transmission line 104. The output of the delay compensator 708 provides an adjusted clock signal and is used by the return channel encoder 704. In a preferred embodiment, the delay compensator 708 is a phase-locked loop with a delay circuit in the feedback loop between the voltage-controlled oscillator and the phase detector, as will be understood to those skilled in the art. Such a configuration provides negative delay so that the clock signal for return channel signals is moved ahead so that with propagation delay it will matches the timing of the CGOut signal at the transmitter 102.

The return channel encoder 704 generates signals and asserts them on the transmission line 104 via line 720 and the line interface 706. The return channel encoder 704 has a data input coupled to line 714 to receive the control and data signals to for the data to be sent on the return channel. The return channel encoder 704 also has a clock input coupled by line 724 to the output of the delay compensator 708 to receive a modified clock signal for timing the assertion of data and change in data states. These signals are asserted or superimposed over the clock & data signals provided by the transmitter 102. The return channel encoder 704 advantageously sends data back to the transmitter 106 on the falling edge of the clock thereby preventing the return channel 704 from causing any jitter on the clock signal. More specifically, the return channel encoder 704 minimizes transition activity only around

the rising edge of the clock, and minimizes activity by fixing the polarity around the rising edge. This is accomplished by including a delay-locked loop in the return channel encoder 704. The return channel encoder 704 advantageously places data on the transmission line 104 or clock pair in the form of voltage signal and not edge position, thus reducing any interference and effect on the transmission of the clock and data signals by the transmitter 102.

Referring now to Figure 10A, a first embodiment of the return channel encoder 704a is shown. The first embodiment return channel encoder 704a provides the minimum functionality for transmission. For example, the return channel encoder 704a could be a 1-bit link. This has a low data rate and does not allow DC balancing, however it is advantageous because there is no latency (once the data is at the transmitter there is no latency due to decoding) in getting the data and it is simple to implement. The first embodiment of the return channel encoder 704a includes a rising edge detector 1002, a delay circuit 1004 and a latch 1008. The rising edge detector 1002 has an input coupled to line 724 to receive a signal for timing the changing of the data output. The rising edge detector 1002 detects the rising edge and then asserts its output upon receiving rising edge. The output of the rising edge detector 1002 is coupled to the input of a delay circuit 1004. The delay circuit delays the signal output of the rising edge detector 1002, such as by half the clock period. Thus, the output of the delay circuit 1004 is at a time of an ideal falling edge if the clock were to have a 50% duty cycle. The output of the delay circuit 1004 is used to control or latch the latch 1008. Thus, the data will only change state on an ideal falling edge of the input timing signal on line 724. The latch 1008 also has a data input and a data output. The data input is coupled to line 714 to receive the data, and the data output is coupled to line 720 for assertion by the line interface 706. Those skilled in the art will understand how to construct other return channel encoders such

as when more that one bit is send back to the transmitter 102 per clock cycle.

Furthermore, those skilled in the art will realize that the rising edge detector 1002 and the delay circuit 1004 may be replaced by a delay-locked loop or a phase-locked loop as will now be discussed with reference to Figure 10B. Referring now to Figure 10B, a second embodiment of the return channel encoder 704b is shown. The second embodiment of the return channel encoder 704b includes a delayed locked loop 650 and a flip-flop 620. This is identical in operation to Figure 6B, and it operation has been described above. The input to the delayed locked loop 650 is coupled to line 724 and the data input of the flip-flop 620 is coupled to line 714. The data output of the flip-flop 620 provides the data output on line 720.

Is should be understood that the either embodiment of the return channel encoder 704a, 704b could also include an encoder for providing encoding of the data before transmission over the return channel. The addition of an encoder such as 4bit/5bit encoder or a 9bit/10bit encoder is advantageous because it increases the amount of data that can be sent per clock cycle. It also provides DC balancing and transition control. However, it makes the transmitter and receiver designs more complicated and adds latency to the availability of the data.

Referring now to Figures 11A, 11B, 12A, and 12B, timing diagrams for the key signals of the present invention are shown. The timing diagram includes: 1) the CGOut signal on line 210 which is asserted on the clock transmission line 104; 2) the signal on the clock transmission line 104; 3) the re-generated clock signal on line 710; 4) the recovered data signal on line 712; and 5) the return channel signal asserted by the return channel encoder 704 on the clock transmission line 104. Figure 11A illustrates the signals at the transmitter 102 using a return to zero signaling method. Similarly, Figure 11B illustrates signals on the transmission line, and signal in the receiver 106 using a return to zero signaling method. In contrast, Figures 12A and 12B show the signal relationships for

a non-return to zero signaling method. Figure 12A shows the signals at the transmitter 102 and Figure 12B shows the signals at the receiver 106.

These timing diagrams demonstrate a number of features of the combined clock and bi-directional data link of the present invention. First, that transition activity and polarity activity by either the transmitter 102 or the receiver 106 is minimized or eliminated close to the rising edge of the CGOut signal. Second, the transmission of data from the transmitter 102 to the receiver 106 is through the position of the falling edge of the clock signal. Third, the transmission of data from the receiver 106 to the transmitter 102 is by current or voltage level adjustment and any changes are not made near the rising edge of the clock signal from the transmitter 102. Fourth, the effect of assertion of data signals by the receiver 106 does not impact the edges in the signals from the transmitter 102.

Clock Multiplication

One important advantage of the present invention is that no modification to any portions of the present invention need to be changed to be operable with or without clock multiplication. In some cases, the transmitter 102 and the receiver 106 have the ability to increase the data transmission rate by increasing the clock rate through clock multiplication (sending multiple clock signals within one period of the clock signal). In such a case, the transmitter 102 asks the receiver 106 if it can handle clock multiplication. The receiver 106 indicates to the transmitter 102 what if any levels of clock multiplication can be handled. The transmitter then sends on the highest clock multiplication level possible. In clock multiplication, the transmitter 106 just sends a multiplied clock, however, the receiver 106 has to divide that multiplied clock down to the original pixel clock so that the main data channel can make use of the clock. The phase information on the clock is also important in some data links and it can also be conveyed through the data link provided with the present invention. In the transmitter 102, a DLL/PLL is used to multiply the clock at the integer multiple of the incoming clock. For some

transmission lines, since the jitter information is important, only integer multiple is allowed. However, if this is not that important, rational number multiples can also be used to save the bandwidth.

It is to be understood that the specific mechanisms and techniques that have been described are merely illustrative of one application of the principles of the invention. Numerous additional modifications may be made to the apparatus described above without departing from the true spirit of the invention.

WHAT IS CLAIMED IS:

1. An apparatus for transmitting a clock signal and data signals over a signal line, the apparatus comprising a clock generator having a first input, a second input and an output, the clock generator modulating a falling edge of an output signal to indicate different data values, the first input of the clock generator coupled to receive a clock signal, and the second input of the clock generator coupled to receive a control signal indicating a data value to be transmitted.

2. The apparatus of claim 1, further comprising a data decoder for extracting data signals, the data decoder having a input and an output, the data decoder for extracting data signals, the input of the data decoder coupled to the signal line, the output providing data from the signal line.

3. The apparatus of claim 2, further comprising a line interface for asserting signals on and extracting signals from the signal line, the line interface having an input, an output and a bi-directional port, the bi-directional port coupled to the signal line, the input of the line interface coupled to the output of the clock generator, the output of the line interface coupled to the input of the decoder.

4. The apparatus of claim 3, wherein the line interface further comprises a first amplifier coupling the output of the clock generator to the signal line, a differential amplifier having a first input coupled to the signal line, a second amplifier coupling the clock generator to a second input of the differential amplifier, and the output of the differential amplifier providing the output of the line interface.

5. The apparatus of claim 1, wherein the clock generator further comprises:

a delay-locked loop having an input and a plurality of outputs for outputting signals shifted in phase from

an input signal, the input of the delay-locked loop coupled to receive the clock signal;

a multiplexer having a plurality of inputs and an output for selecting one of the plurality of input signals for output, the plurality of inputs of the multiplexer coupled to respective outputs of the delay-locked loop; and

a latch having a first input and a second input, the first input coupled to an output of the delay-locked loop, and the second input coupled to output of the multiplexer.

6. The apparatus of claim 5, further comprising a monostable multivibrator having an input and an output, the input of the monostable multivibrator to receive the clock signal, the output of the monostable multivibrator coupled to the input of the delay locked loop.

7. The apparatus of claim 5, wherein the latch further comprising a pair of cross coupled NAND gates.

8. The apparatus of claim 2, wherein the decoder further comprises

a delay-locked loop having an input and a plurality of outputs for outputting signals shifted in phase from an input signal, the input of the delay-locked loop coupled to receive the clock signal;

a sampling unit having a plurality of inputs, a first output and a second output, the sampling unit for controlling when signals are sampled and for indicating the time at which signals are sampled, the plurality of inputs coupled to respective outputs of the delay-locked loop;

a transition detector for determining when there is a transition in a signal, the transition detector having a data input, a control input and a data output, the

data input of the transition detector coupled to the signal line, the control input of the transition detector coupled to the first output of the sampling unit; and

a data generator having a first input, a second input and an output, data generator for producing bit values corresponding to when transitions occur on the signal line, the first input of the data generator coupled to the second output of the sampling unit, the second input of the data generator coupled to the output of the transition detector.

9. The apparatus of claim 2, wherein the decoder further comprises

a delay-locked loop having an input and a plurality of outputs for outputting signals shifted in phase from an input signal, the input of the delay-locked loop coupled to receive the clock signal;

a flip-flop having an control input, a data input and an output, the control input of flip-flop coupled to one of the plurality of outputs of the delay-locked loop, and the data input of the flip-flop coupled to the signal line.

10. The apparatus of claim 1, wherein the apparatus is coupled by the signal line to a receiver, and wherein the receiver further comprises:

a clock re-generator having an input and an output for recovering a clock signal from the signal line, the input of the clock re-generator coupled to the signal line;

a second decoder for extracting data signals, the second decoder having a first input, a second input and an output, the second decoder for extracting data signals, the first input of the second decoder coupled to the signal line, the second input of the second

decoder coupled to the output of the clock re-generator and the output providing data from the signal line.

11. The apparatus of claim 10, wherein the clock re-generator of the receiver is an amplifier.

12. The apparatus of claim 10, wherein the clock re-generator of the receiver is an phase-locked loop.

13. The apparatus of claim 10, wherein the second decoder further comprises

a delay-locked loop having an input and a plurality of outputs for outputting signals shifted in phase from an input signal, the input of the delay-locked loop coupled to output of the clock re-generator;

a sampling unit having a plurality of inputs, a first output and a second output, the sampling unit for controlling when signals are sampled and for indicating the time at which signals are sampled, the plurality of inputs coupled to respective outputs of the delay-locked loop;

a transition detector for determining when there is a transition in a signal, the transition detector having a data input, a control input and a data output, the data input of the transition detector coupled to the signal line, the control input of the transition detector coupled to the first output of the sampling unit; and

a data generator having a first input, a second input and an output, data generator for producing bit values corresponding to when transitions occur on the signal line, the first input of the data generator coupled to the second output of the sampling unit, the second input of the data generator coupled to the output of the transition detector.

14. The apparatus of claim 10, wherein the second decoder further comprises

a delay-locked loop having an input and a plurality of outputs for outputting signals shifted in phase from an input signal, the input of the delay-locked loop coupled to the output of the clock re-generator;

a flip-flop having an control input, a data input and an output, the control input of flip-flop coupled to one of the plurality of outputs of the delay-locked loop, and the data input of the flip-flop coupled to the signal line.

15. The apparatus of claim 10, further comprising a second line interface for asserting signals on and extracting signals from the signal line, the second line interface having an input, an output and a bi-directional port, the bi-directional port coupled to the signal line, the output of the line interface coupled to the input of the second decoder and the clock re-generator.

16. The apparatus of claim 10, further comprising a delay compensator having an input and an output for adjusting a recovered clock signal to compensate for propagation delay, the input of the delay compensator coupled to the output of the clock re-generator.

17. The apparatus of claim 16, further comprising a return channel encoder having a first input, a second input and an output, for sending signals on the signal line, the first input of the return channel encoder coupled to receive data for transmission, the second input of the return channel encoder coupled to the output of the delay compensator, and the output of the return channel encoder coupled to the signal line.

18. The apparatus of claim 17, wherein the return channel encoder further comprises:

a delay-locked loop having an input and a plurality of outputs for outputting signals shifted in phase from

an input signal, the input of the delay-locked loop coupled to the output of the delay compensator;

a flip-flop having an control input, a data input and an output, the control input of flip-flop coupled to one of the plurality of outputs of the delay-locked loop, and the data input of the flip-flop coupled to the signal line.

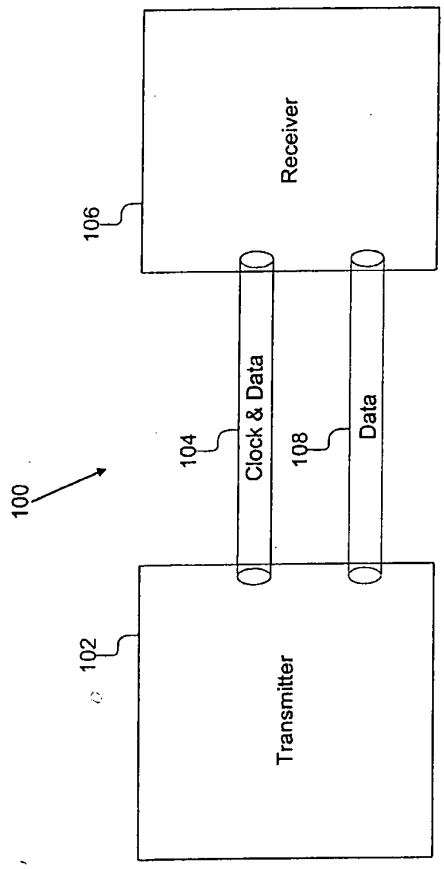


Figure 1

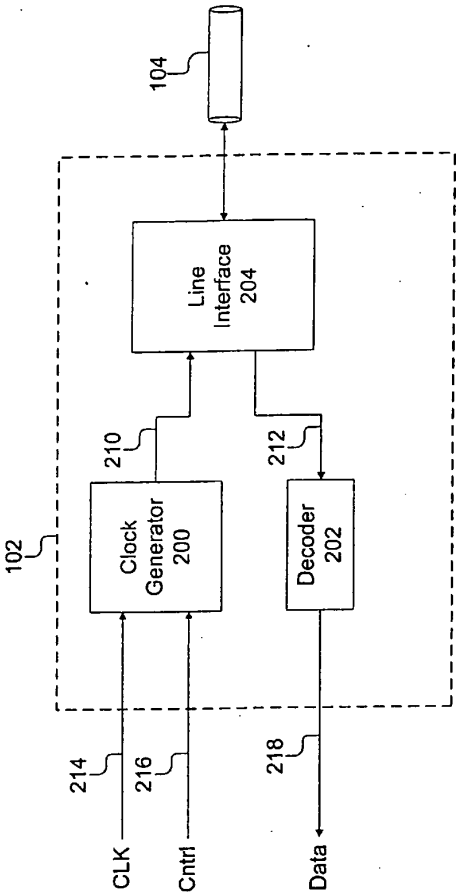

104
Line Interface 204
210
212
Clock Generator 200
Decoder 202
102
214
216
218
CLK
Cntrl
Data

Figure 2

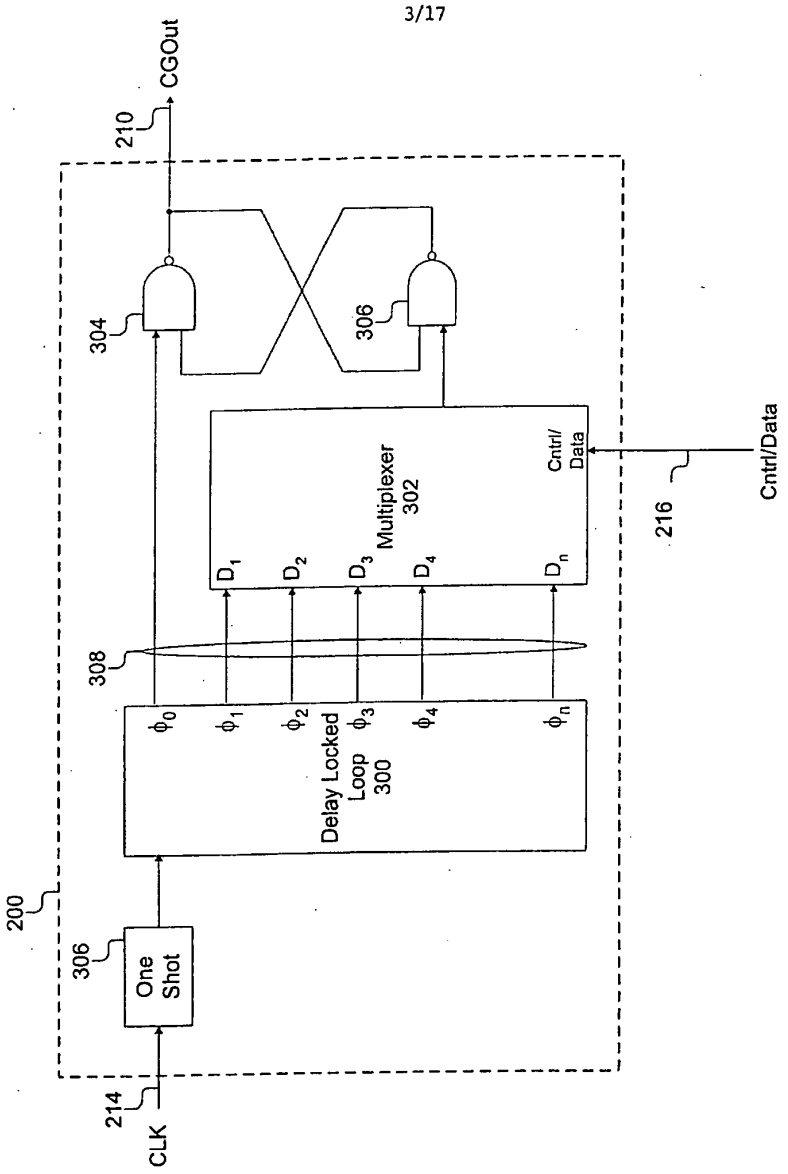

CGOut
210
304
306
Multiplexer
302
Cntrl/
Data
D1
D2
D3
D4
Dn
216
Cntrl/Data
308
ϕ0
ϕ1
ϕ2
ϕ3
ϕ4
ϕn
Delay Locked
Loop
300
200
306
One
Shot
214
CLK

Figure 3

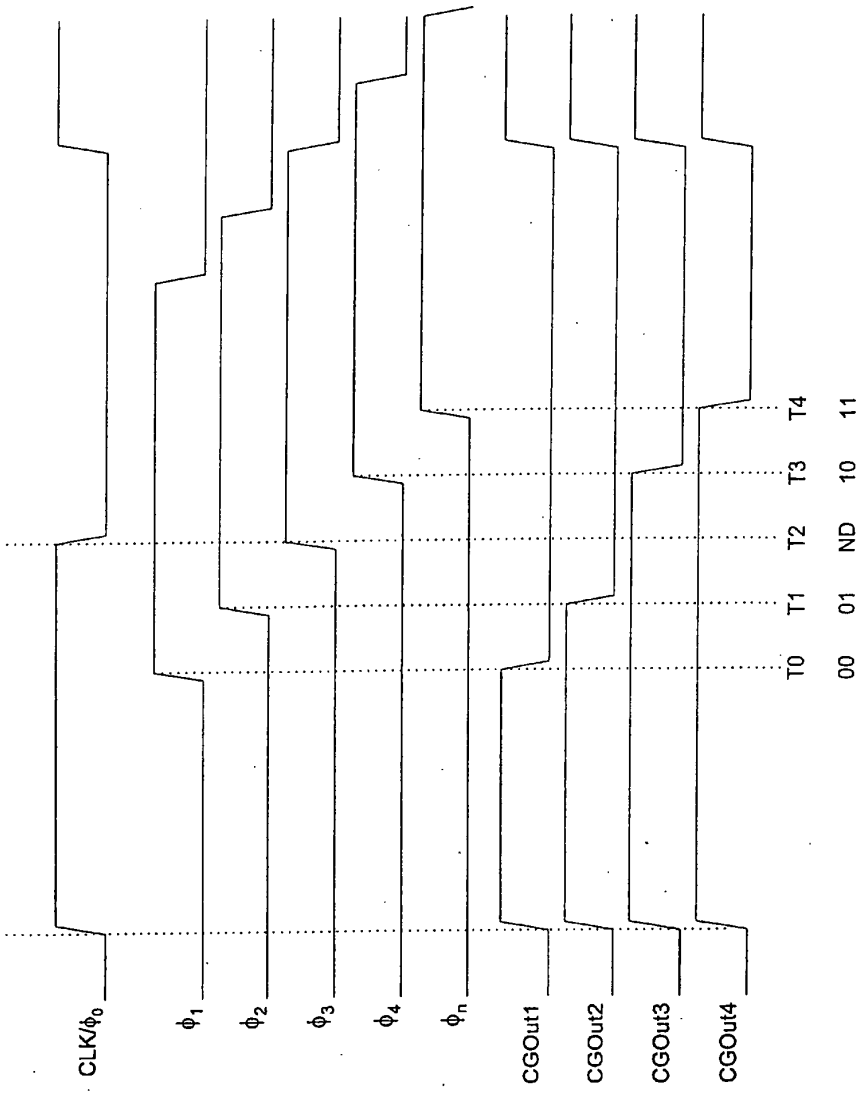

CLK/ϕ_0
ϕ_1
ϕ_2
ϕ_3
ϕ_4
ϕ_n
CGOut1
CGOut2
CGOut3
CGOut4
T0
T1
T2
T3
T4
00
01
ND
10
11

Figure 4

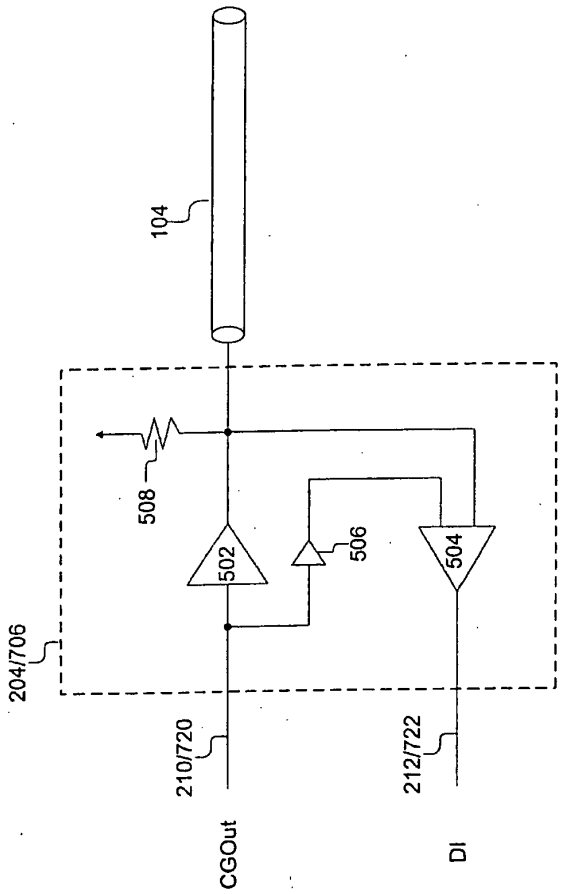


Figure 5A

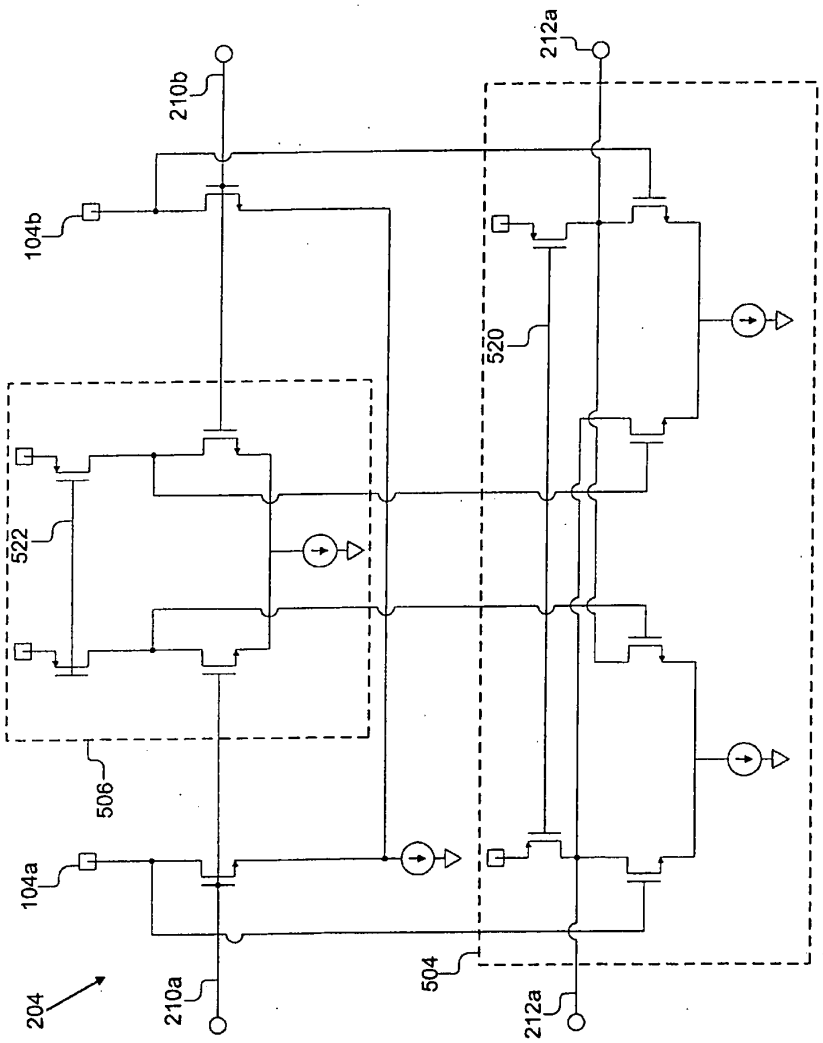


Figure 5B

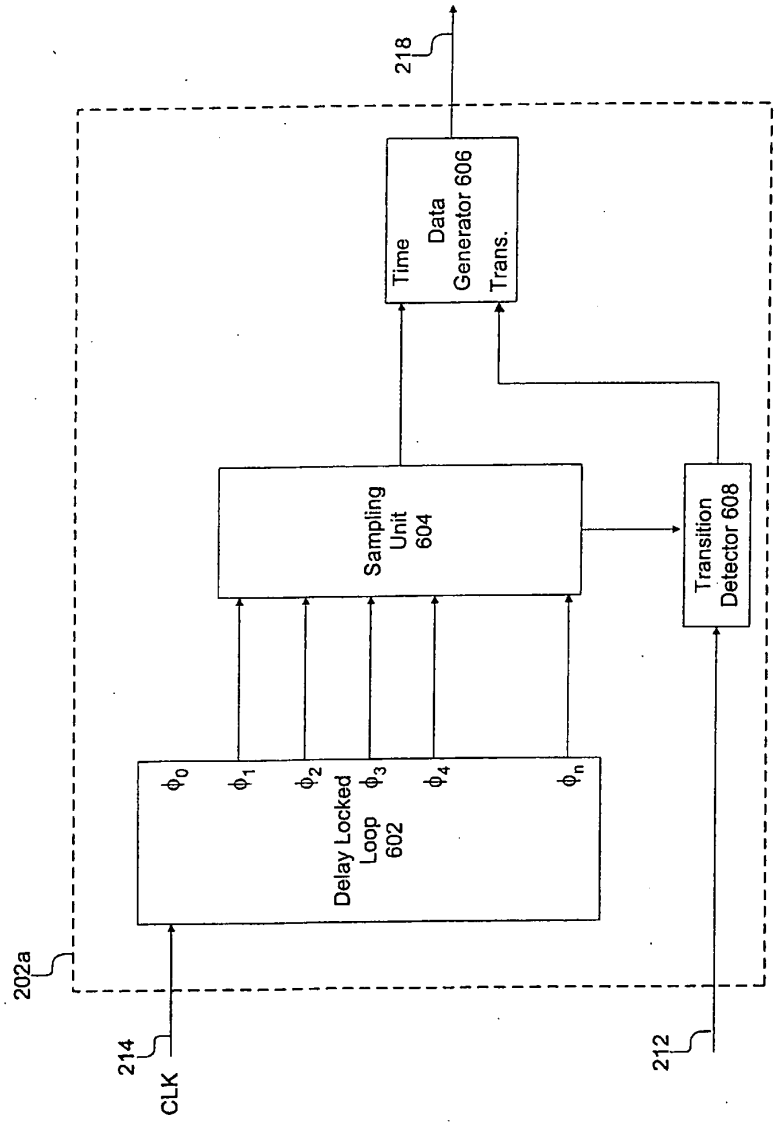

218
Time Data Generator 606 Trans.
Sampling Unit 604
Transition Detector 608
ϕ_0 ϕ_1 ϕ_2 ϕ_3 ϕ_4 ϕ_n
Delay Locked Loop 602
202a
214
CLK
212

Figure 6A

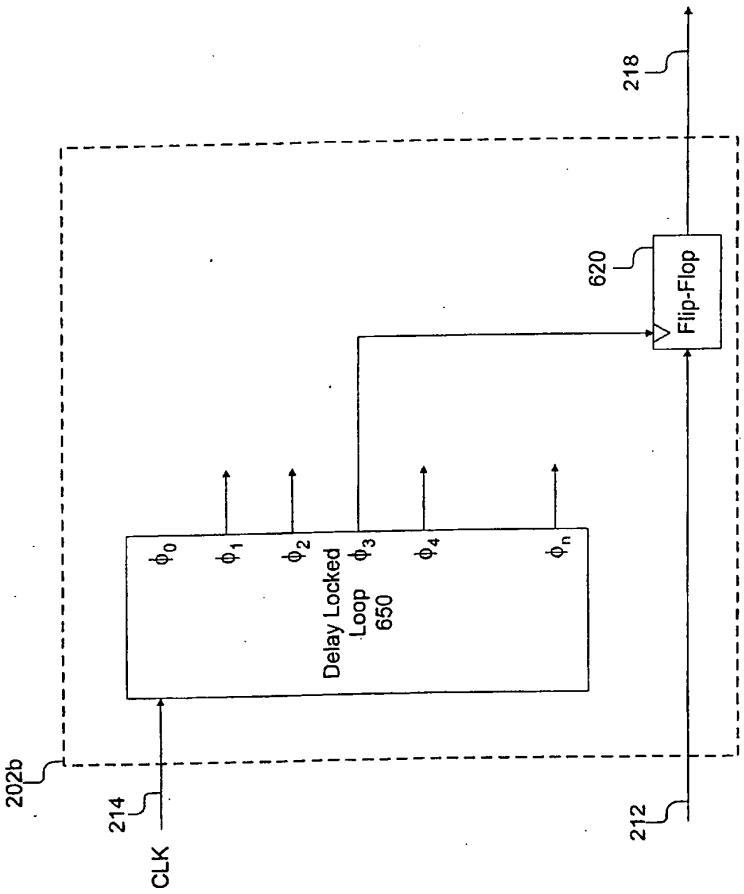

218
620
Flip-Flop
ϕ_0
ϕ_1
ϕ_2
ϕ_3
ϕ_4
ϕ_n
Delay Locked Loop 650
202b
214
CLK
212

Figure 6B

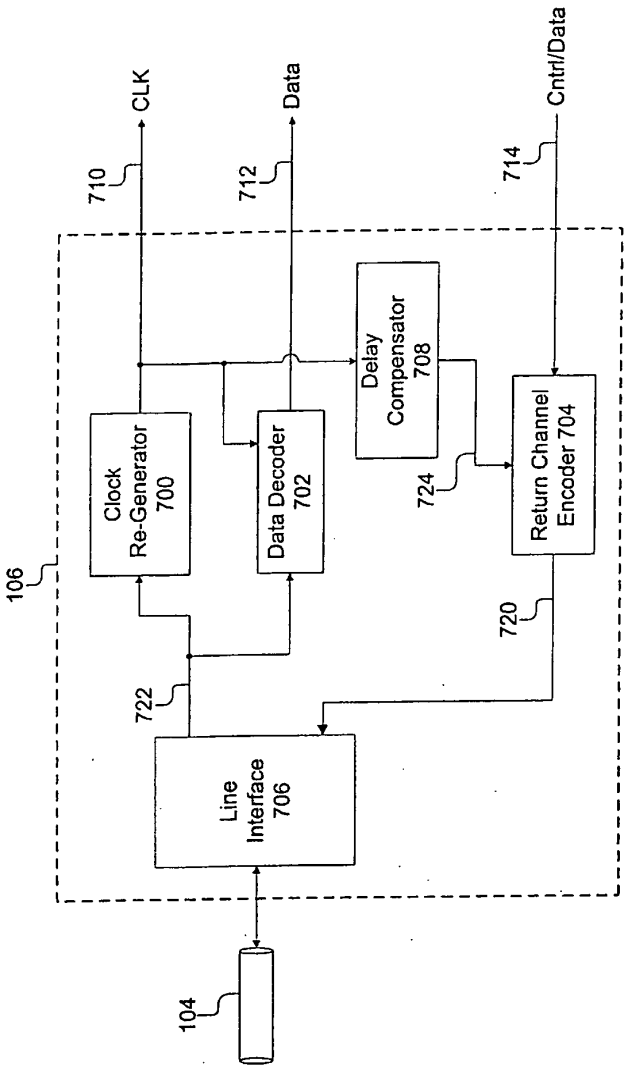

CLK
Data
Cntrl/Data
710
712
714
Clock Re-Generator 700
Data Decoder 702
Delay Compensator 708
Return Channel Encoder 704
724
720
722
Line Interface 706
106
104

Figure 7

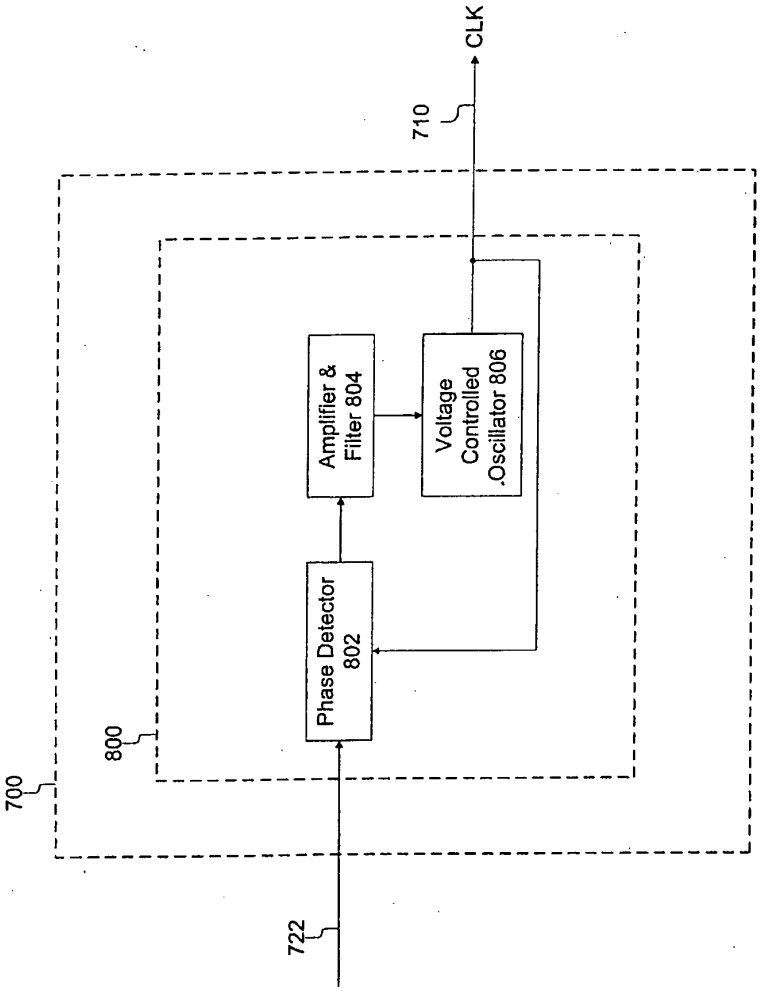

CLK
710
Amplifier & Filter 804
Voltage Controlled .Oscillator 806
Phase Detector 802
800
700
722

Figure 8

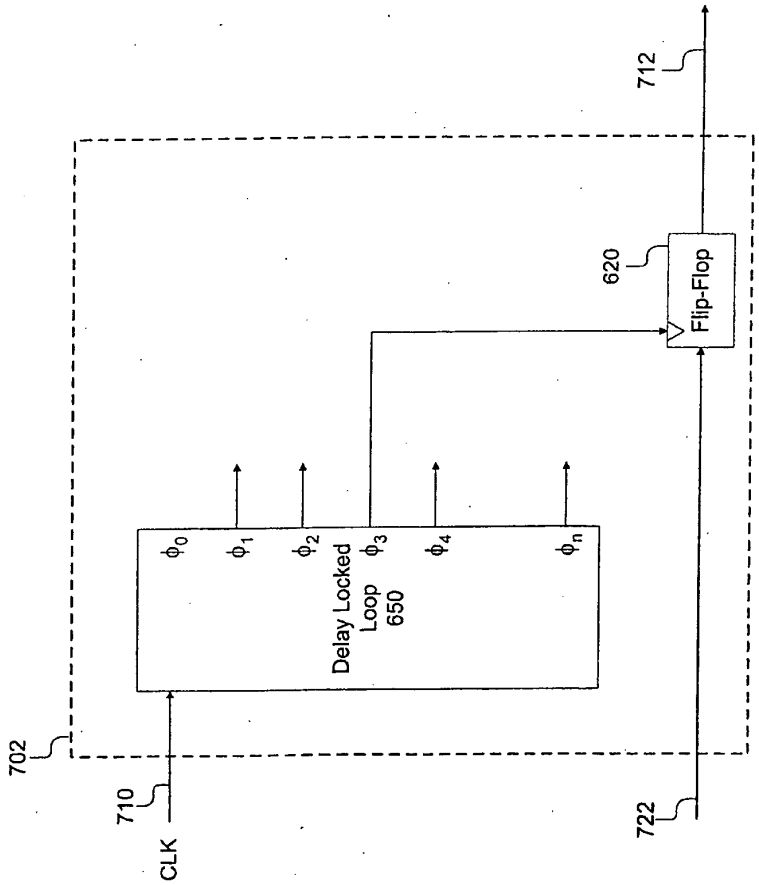

712
620
Flip-Flop
ϕ_0
ϕ_1
ϕ_2
ϕ_3
ϕ_4
ϕ_n
Delay Locked Loop 650
702
710
CLK
722

Figure 9

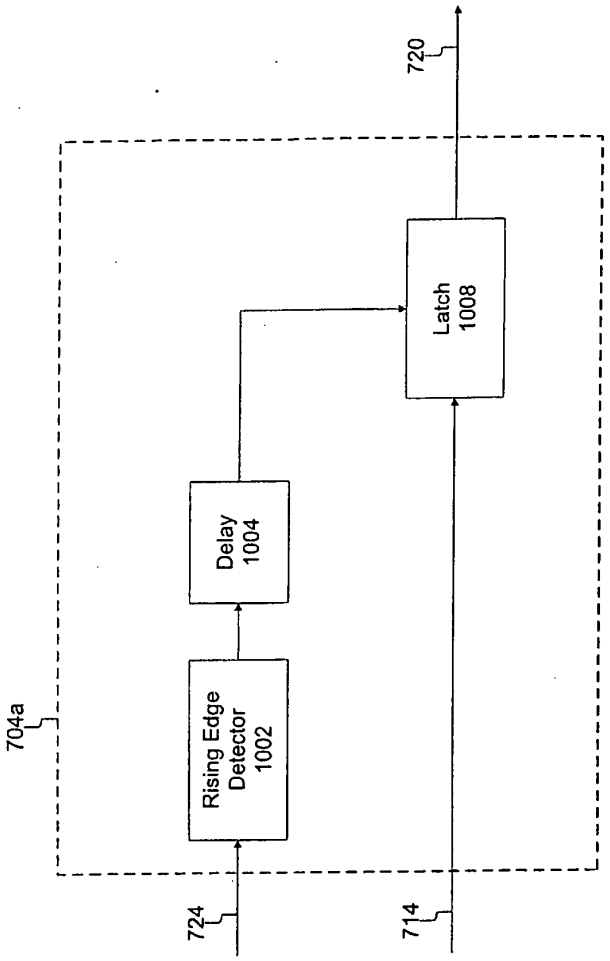

720
Latch
1008
Delay
1004
Rising Edge
Detector
1002
704a
724
714

Figure 10A

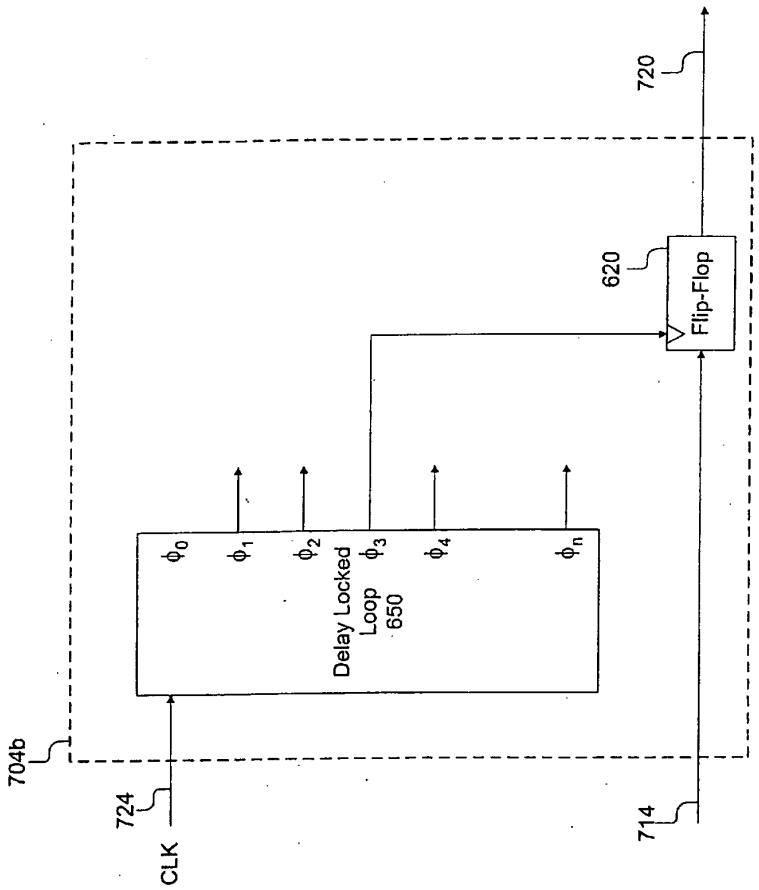

720
620
Flip-Flop
ϕ_0
ϕ_1
ϕ_2
ϕ_3
ϕ_4
ϕ_n
Delay Locked Loop 650
704b
724
CLK
714

Figure 10B

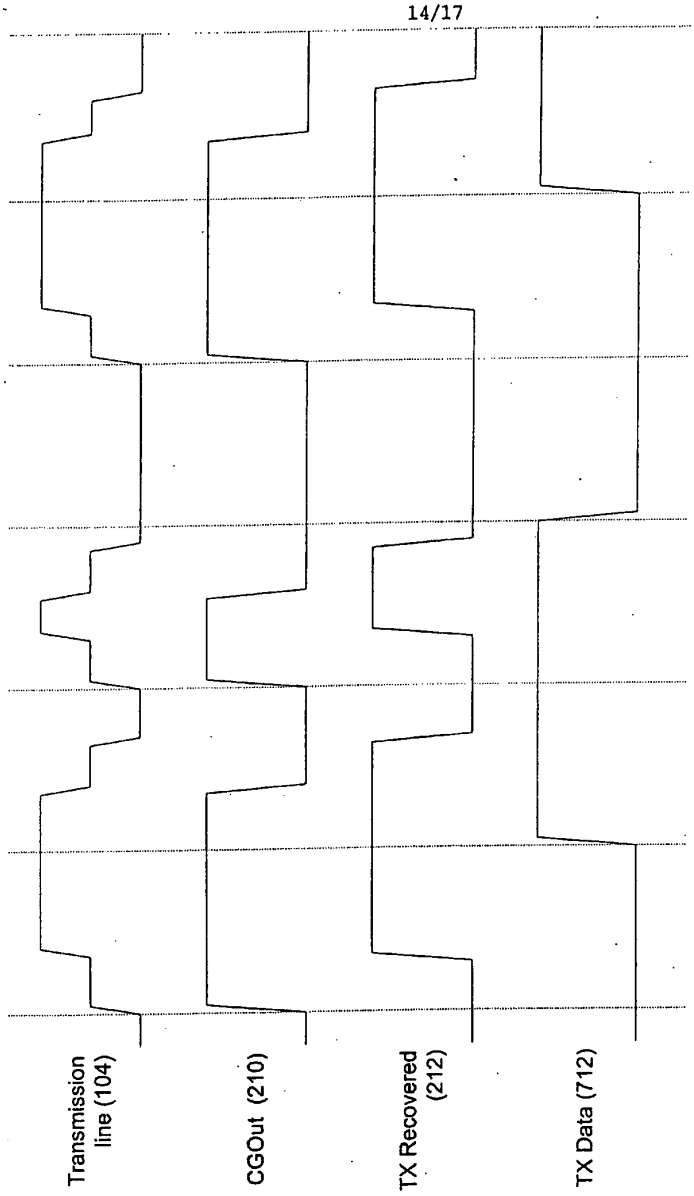

Transmission line (104)
CGOut (210)
TX Recovered (212)
TX Data (712)

Figure 11A

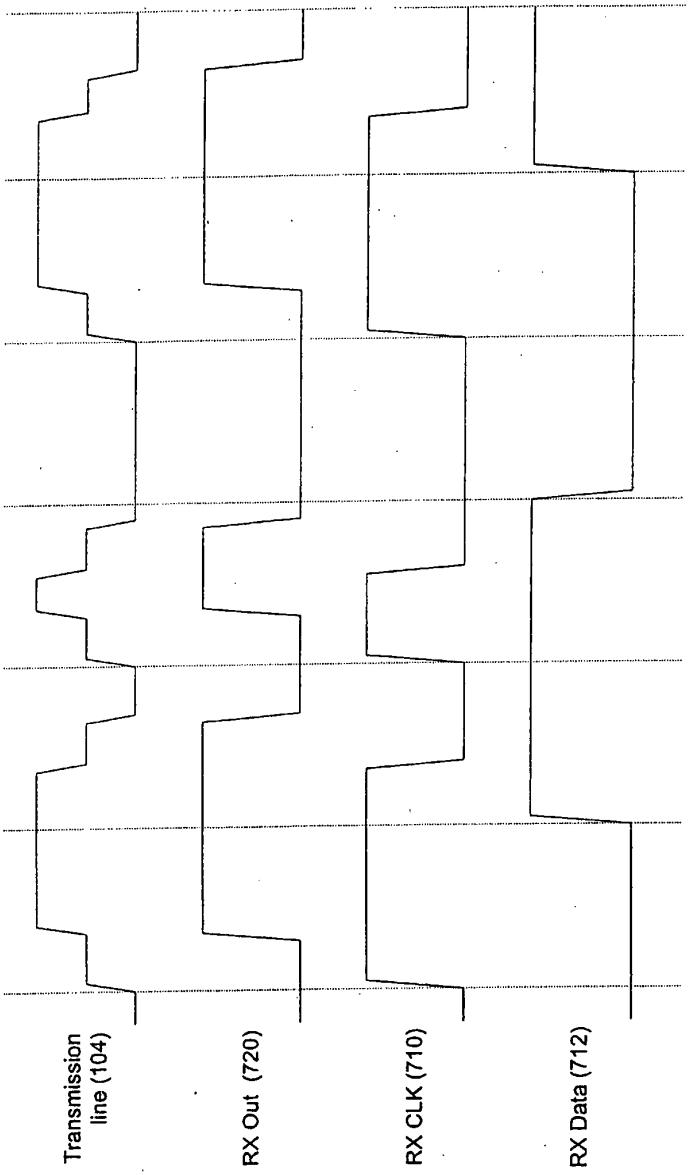


Figure 11B

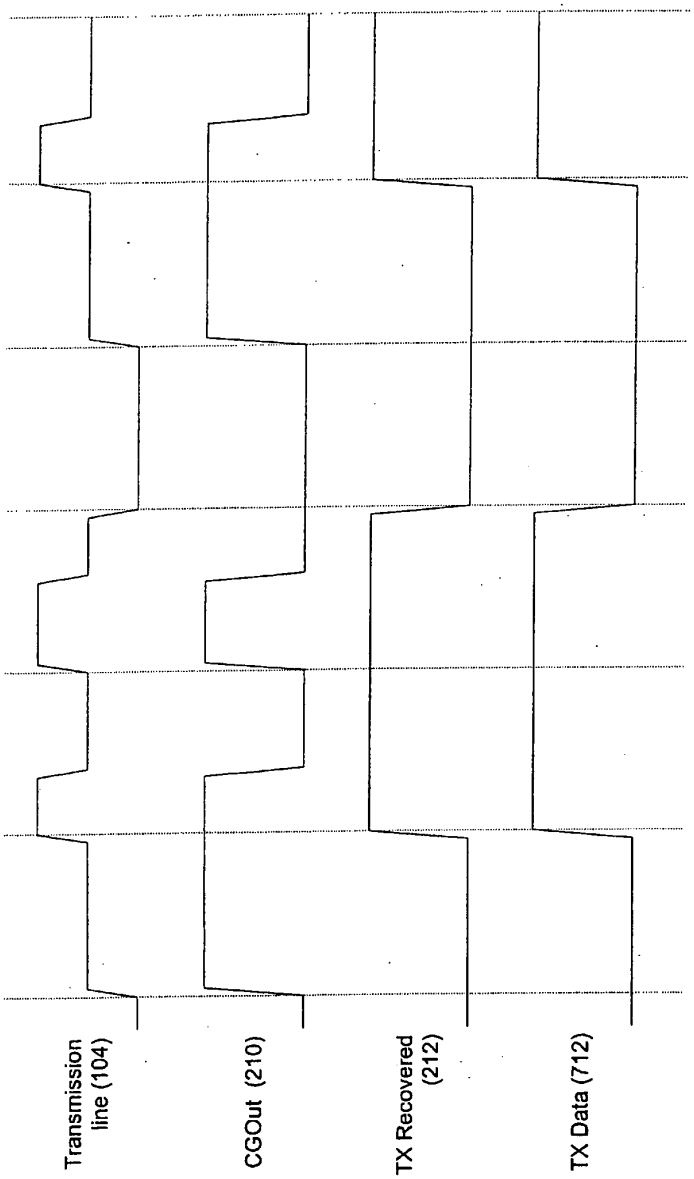

Transmission line (104)
CGOut (210)
TX Recovered (212)
TX Data (712)

Figure 12A

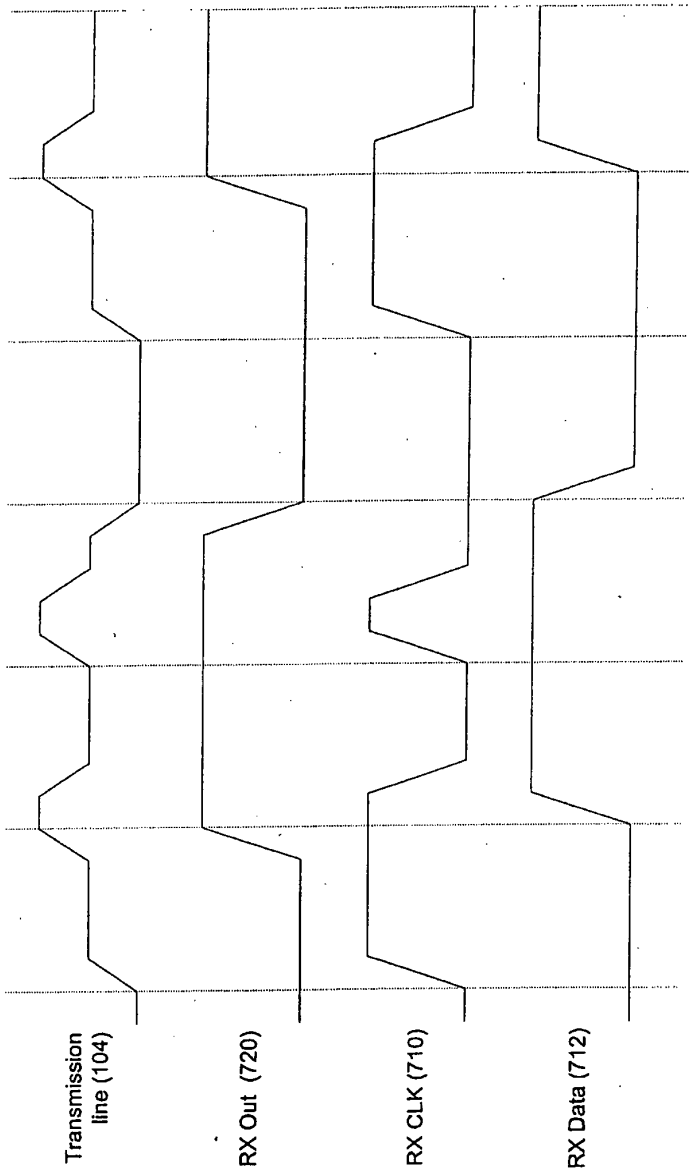


Figure 12B

INTERNATIONAL SEARCH REPORT

Inte .onal Application No
PCT/US 99/20488

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H04L25/02 H04L25/49

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H04L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	KAZUTAKA NOGAMI ET AL: "PHASE MODULATION I/O INTERFACE CIRCUIT" IEEE INTERNATIONAL SOLID STATE CIRCUITS CONFERENCE, vol. 37, February 1994 (1994-02), pages 108-109,318, XP000507077 New York, USA ISSN: 0193-6530 left-hand column, paragraph 2 left-hand column, last paragraph right-hand column, paragraph 2 - paragraph 3 figures 2,3	1-15
Y		16-18
	--- -/--	

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
3 February 2000	10/02/2000

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Orozco Roura, C

2

Form PCT/ISA/210 (second sheet) (July 1992)

INTERNATIONAL SEARCH REPORT

Inte onal Application No
PCT/US 99/20488

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication,where appropriate, of the relevant passages	Relevant to claim No.
X	EP 0 798 901 A (SGS THOMSON MICROELECTRONICS) 1 October 1997 (1997-10-01) column 1, line 43 - line 47 column 4, line 25 - line 34 column 9, line 14 - line 35 column 10, line 17 - line 19	1-15
A		16-18

X	US 4 459 591 A (HAUBNER GEORG ET AL) 10 July 1984 (1984-07-10) column 2, line 61 - line 65 column 3, line 40 - line 43 column 3, line 65 - line 67 column 5, line 61 -column 6, line 27 figure 1	1-4,10, 11,15
A		5-9, 12-14, 16-18

X	US 5 577 071 A (GEHRKE JAMES K ET AL) 19 November 1996 (1996-11-19) abstract column 3, line 32 - line 46	1
A		2-18

Y	FR 2 251 139 A (FUJITSU LTD) 6 June 1975 (1975-06-06) page 4, line 19 - line 21 page 5, line 6 - line 7	16-18

2

Form PCT/ISA/210 (continuation of second sheet) (July 1992)

INTERNATIONAL SEARCH REPORT

Information on patent family members

Inte onal Application No
PCT/US 99/20488

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
EP 0798901 A	01-10-1997	FR 2746995 A	03-10-1997
		DE 69700112 D	25-03-1999
		DE 69700112 T	17-06-1999
		JP 10051501 A	20-02-1998
		US 5903607 A	11-05-1999
US 4459591 A	10-07-1984	DE 3103884 A	02-09-1982
		FR 2499344 A	06-08-1982
US 5577071 A	19-11-1996	NONE	
FR 2251139 A	06-06-1975	JP 944008 C	20-03-1979
		JP 50080019 A	28-06-1975
		JP 53021963 B	06-07-1978
		BE 822021 A	03-03-1975
		CA 1027252 A	28-02-1978
		CH 592984 A	15-11-1977
		DE 2453628 A	22-05-1975
		GB 1480937 A	27-07-1977
		IT 1024810 B	20-07-1978
		NL 7414662 A,B,	14-05-1975
		SE 407887 B	23-04-1979
		SE 7413980 A	13-05-1975
		SU 1258340 A	15-09-1986
		US 3967058 A	29-06-1976

Form PCT/ISA/210 (patent family annex) (July 1992)

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OIPE SC144 JUN 06 2002 PATENT & TRADEMARK OFFICE

Attorney Docket No. SII-1000 [SIMG0115]

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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In re Patent Application of

SEUNG HO HWANG , et al.

Application No. 10/036,234

Filed: December 24, 2001

For: **ENCODING METHOD AND SYSTEM FOR REDUCING INTER-SYMBOL INTERFERENCE EFFECTS IN TRANSMISSION OVER A SERIAL LINK**

Group Art Unit: 2614

Examiner: Unknown

AMENDMENT, PETITION AND FEE TO ADD TO ORIGINAL ERRONEOUSLY NAMED OR NOT NAMED INVENTOR(S) IN -- NONPROVISIONAL APPLICATION – DECLARATION UNDER 37 C.F.R. § 1.48 (a)

400 Montgomery Street, Suite 1110
San Francisco, CA 94104
(415) 433-2250

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to Assistant Commissioner for Patents, Washington, DC 20231, on May 21, 2002.

GIRARD & EQUITZ LLP Date: 05/21/02

By Marsha A. Townsend

Marsha A. Townsend

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

1. This amendment and petition under 37 C.F.R. § 1.48(a) is to correct the incorrect original naming of inventors in the declaration as set forth and filed on February 25, 2002.

2. Addition and/or Deletion of Inventors

☒ Add the following previously unnamed person as inventor of this application:

ALBERT M. SCALISE

3. Attached is

(a) A statement from each person being added as an inventor that the error in inventorship occurred without deceptive intention on his part. 37 C.F.R. § 1.48(a)(1).

(b) a declaration by each of the actual inventors as required by 37 C.F.R. § 1.63 (or as permitted by § § 1.42, 1.43, OR 1.47). 37 C.F.R. § 1.48(a)(2).

06/11/2002 ZJUHAR1 00000056 10036234

01 FC:122 130.00 OP

(c) written assent of the assignee [37 C.F.R. § 1.48(a)(4)] and statement under 37 C.F.R. § 3.73(b).

4. Fee Payment (37 C.F.R. § 1.17(i))

The fee required is paid as follows:

☒ Attached is a check in the amount of $130.00.

☒ Charge any additional fees required by this paper or credit any overpayment to Deposit Account No. 50-1697.

Respectfully submitted,

GIRARD & EQUITZ LLP

Dated: 5/21/02 By: Alfred A Equitz

Alfred A. Equitz
Reg. No.30,922

Telephone No. (415) 433-2250

Customer No.: 27872

Attorneys for Applicant(s)

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of

SEUNG HO HWANG , et al.

Application No. 10/036,234

Filed: December 24, 2001

For: ENCODING METHOD AND SYSTEM FOR REDUCING INTER-SYMBOL INTERFERENCE EFFECTS IN TRANSMISSION OVER A SERIAL LINK

Group Art Unit: 2614

Examiner: Unknown

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STATEMENT BY PERSON BEING NAMED AS INVENTOR UNDER **37 C.F.R. § 1.48(a)(1)**

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San Francisco, CA 94104
(415) 433-2250

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GIRARD & EQUITZ LLP Date 05 21 /02

By: Marsha A. Townsend

Marsha A. Townsend

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

I, ALBERT M. SCALISE, hereby declare that I am an inventor of the above-referenced patent application, and that the unsigned declaration originally filed with the application and the executed declaration filed on February 25, 2002, erroneously failed to name me as an inventor. The error, in failing to name me as an inventor in each declaration, arose without any deceptive intention on my part.

Dated: May 6, 2002

Albert M. Scalise

ALBERT M. SCALISE

3107 Elaine Drive
San Jose, California 95124
Tel: (408) 616-1464

O I P E JC14
JUN 0 6 2002
PATENT & TRADEMARK OFFICE

Atty Docket No. SII-1000 [SIMG0115]

DECLARATION FOR PATENT APPLICATION

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name,

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

ENCODING METHOD AND SYSTEM FOR REDUCING INTER-SYMBOL INTERFERENCE EFFECTS IN TRANSMISSION OVER A SERIAL LINK

the specification of which (check one) __ is attached hereto or X was filed on December 24, 2001 as Application No. 10/036,234 .

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose all information which is material to patentability as defined in 37 CFR § 1.56.

I hereby claim foreign priority benefits under 35 U.S.C. § 119(a)-(d) or § 365(b) of any foreign application(s) for patent or inventor's certificate, or § 365(a) of any PCT International application which designated at least one country other than the United States, listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Prior Foreign Application(s)			Priority Claimed Yes	No
Number	Country	Day/Month/Year Filed		
Number	Country	Day/Month/Year Filed		

I hereby claim the benefit under 35 U.S.C. § 119(e) of any United States provisional application(s) below.

Application Number	Filing Date
Application Number	Filing Date

I hereby claim the benefit under 35 U.S.C. § 120 of any United States application(s), or § 365(c) of any PCT International application designating the United States, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of 35 U.S.C. § 112, I acknowledge the duty to disclose all information which is material to patentability as defined in 37 CFR § 1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application:

Application Number	Filing Date	Status: Patented, Pending, Abandoned
09/954,663	09/12/2001	Pending
Application Number	Filing Date	Status: Patented, Pending, Abandoned

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment or both, under 18 U.S.C. § 1001 and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full name of sole or first inventor SEUNG HO HWANG

Inventor's signature _____ 5/6/02
Date

Residence 1690 Edgewood Drive, Palo Alto, CA 94303

Citizenship USA

Post Office Address 1690 Edgewood Drive, Palo Alto, CA 94303

Full name of second joint inventor, if any, JANO BANKS

Inventor's signature _____ 5/6/02
Date

Residence 19621 La Mar Court, Cupertino, CA 95014

Citizenship USA

Post Office Address 19621 La Mar Court, Cupertino, CA 95014

Full name of third joint inventor, if any, PAUL DANIEL WOLF

Inventor's signature _____ 5/16/02
Date

Residence 2696 Eaton Avenue, San Carlos, CA 94070

Citizenship USA

Post Office Address 2696 Eaton Avenue, San Carlos, CA 94070

Full name of fourth joint inventor, if any, ERIC LEE

Inventor's signature _____ 5-6-02
Date

Residence 1028 South De Anza Blvd., Apt. B208, San Jose, CA 95129

Citizenship USA

Post Office Address P.O. Box 64395, Sunnyvale, CA 94088

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment or both, under 18 U.S.C. § 1001 and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full name of fifth joint inventor, if any, BAEGIN SUNG

Inventor's signature _____ 5-6-02
Date

Residence 1657 Ontario Drive, #12, Sunnyvale, CA 94087

Citizenship KOREA

Post Office Address 1657 Ontario Drive, #12, Sunnyvale, CA 94087

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment or both, under 18 U.S.C. § 1001 and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full name of sixth joint inventor, if any, ALBERT M. SCALISE

Inventor's signature _____ May 6, 2002
Date

Residence 3107 Elaine Drive, San Jose, CA 95124

Citizenship USA

Post Office Address 3107 Elaine Drive, San Jose, CA 95124

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In re Patent Application of

SEUNG HO HWANG , et al.

Application No. 10/036,234

Filed: December 24, 2001

For: ENCODING METHOD AND SYSTEM FOR REDUCING INTER-SYMBOL INTERFERENCE EFFECTS IN TRANSMISSION OVER A SERIAL LINK

Group Art Unit: 2614

Examiner: Unknown

ASSENT OF ASSIGNEE TO ADDITION OF INVENTOR UNDER **37 C.F.R. § 1.48(a)(4)** AND STATEMENT UNDER **37 C.F.R. § 3.73(b)**

400 Montgomery Street, Suite 1110
San Francisco, CA 94104
(415) 433-2250

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GIRARD & EQUITZ LLP Date: 05/21/02

By: Marsha A. Townsend

Marsha A. Townsend

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

The Assignee of the referenced application is SILICON IMAGE, INC., whose address is 1060 E. Arques Avenue, Sunnyvale, California 94085, by the Assignment dated February 20, 2002 and February 21, 2002, submitted to the U.S. Patent and Trademark Office for recordation with Form PTO 1595 on February 25, 2002 (copy attached), and by the Assignment dated May 6, 2002, submitted to Box Assignments, U.S. Patent and Trademark Office, simultaneously with this mailing for recordation with Form PTO 1595 (copy attached).

Assignee hereby assents to the correction of inventorship filed herewith.

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ASSIGNEE STATEMENT

37 C.F.R. § 3.73(b)

The Assignee certifies that it has reviewed each above-identified Assignment and to the best of the Assignee's knowledge and belief, title is in the Assignee.

SILICON IMAGE, INC.

Dated: 5-16-02 By: Badar Bajwi

Name: Badar Bajwi

Title: Executive V.P., Engineering

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1. Name of conveying party(ies):

SEUNG HO HWANG
JANO BANKS
PAUL DANIEL WOLF
ERIC LEE
BAEGIN SUNG

OIPE
JUN 06 2002
PATENT & TRADEMARK OFFICE

Additional name(s) of conveying party(ies) attached? __ Yes X No

3. Nature of conveyance:
X Assignment __ Merger
__ Security Agreement __ Change of Name
__ Other

Execution Date: 02/20/2002 and 02/21/2002

2. Name and address of receiving party(ies):

Name: SILICON IMAGE, INC.

Street Address: 1060 E. Arques Avenue

Internal Address:

City: Sunnyvale State: CA Zip: 94085

Additional name(s) & address(es) attached? ____ Yes X No

4. Application number(s) or registration number(s):

A. Patent Application No.(s) 10/036,234

B. Patent No.(s)

Additional numbers attached? __ Yes X No

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GIRARD & EQUITZ LLP Date: 02/25/02

By: Marsha A. Townsend
Marsha A. Townsend

5. Name and address of party to whom correspondence concerning document should be mailed:

Name: Alfred A. Equitz

Internal Address: GIRARD & EQUITZ LLP

Street Address: 400 Montgomery Street #1110

City: San Francisco State: CA Zip: 94104

Telephone: (415) 433-2250
Facsimile: (415) 433-2255

Attorney Docket No. SII-1000 [SIMG0115]

6. Total number of applications and patents involved: 1

7. Total fee (37 C.F.R. 3.41)---------- $ 40.00
X **Check Enclosed**

__ Authorized to be charged to deposit account

8. Deposit account number:
50-1697

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9. Statement and signature.
To the best of my knowledge and belief, the foregoing information is true and correct and any attached copy is a true copy of the original document.

Alfred A. Equitz Reg. No. 30,922
Name of Person Signing

Alfred A Equitz
Signature

2/25/02
Date

Total number of pages including cover sheet, attachments and document: 3

Mail documents to be recorded with required cover sheet information to:
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Washington, D.C. 20231

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Attorney Docket No. SII-1000 [SIMG0115]

ASSIGNMENT

WHEREAS, WE, Seung Ho Hwang, Jano Banks, Paul Daniel Wolf, Eric Lee, and Baegin Sung hereinafter referred to as "ASSIGNORS", have invented certain new and useful improvements as described and set forth in the below-identified application for United States Letters Patent:

Title of Invention: **ENCODING METHOD AND SYSTEM FOR REDUCING INTER-SYMBOL INTERFERENCE EFFECTS IN TRANSMISSION OVER A SERIAL LINK**

Filing Date: December 24, 2001 Application No.: 10/036,234

WHEREAS, SILICON IMAGE, INC., a corporation of the State of Delaware, 1060 E. Arques Avenue, Sunnyvale, CA 94085 hereinafter referred to as "ASSIGNEE", is desirous of acquiring the entire right, title and interest in the said invention and application and in any Letters Patent which may be granted on the same;

NOW, THEREFORE, TO ALL WHOM IT MAY CONCERN: Be it known that, for One Dollar ($1.00) and other good and valuable consideration, receipt of which is hereby acknowledged by Assignors, Assignors have sold, assigned and transferred, and by these presents do sell, assign and transfer unto the said Assignee, and Assignee's successors and assigns, all right, title and interest in and to the said invention, said application for United States Letters Patent, and any Letters Patent which may hereafter be granted on the same in the United States and all countries throughout the world including any divisions, renewals, continuations in whole or in part, substitutions, conversions, reissues, prolongations or extensions thereof, said interest to be held and enjoyed by said Assignee as fully and exclusively as it would have been held and enjoyed by said Assignors had this assignment and transfer not been made, to the full end and term of any such Letters Patent.

Assignors further agree that they will, without charge to said Assignee, but at Assignee's expense, cooperate with Assignee in the prosecution of said application and/or applications, execute, verify, acknowledge and deliver all such further papers, including applications for Letters Patent and for the reissue thereof, and instruments of assignment and transfer thereof, and will perform such other acts as Assignee lawfully may request, to obtain or maintain Letters Patent for said invention and improvement in any and all countries, and to vest title thereto in said Assignee, or Assignee's successors and assigns.

IN TESTIMONY WHEREOF, Assignor has hereunto signed his/her name to this assignment on the date indicated below.

Date: 2/20/02

Seung Ho Hwang

IN TESTIMONY WHEREOF, Assignor has hereunto signed his/her name to this assignment on the date indicated below.

Date: 2/21/02

Jano Banks

IN TESTIMONY WHEREOF, Assignor has hereunto signed his/her name to this assignment on the date indicated below.

Date: 2/21/02

Paul Daniel Wolf

IN TESTIMONY WHEREOF, Assignor has hereunto signed his/her name to this assignment on the date indicated below.

Date: 2-20-02

Eric Lee

IN TESTIMONY WHEREOF, Assignor has hereunto signed his/her name to this assignment on the date indicated below.

Date: 2-021-02

Baegin Sung

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PTO/SB/30 (Rev 6-93)
JUN 06 2002
U.S. PATENT & TRADEMARK OFFICE

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OMB No. 0651-0011 (exp. 4/94)

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ALBERT M. SCALISE

Additional name(s) of conveying party(ies) attached? X Yes __ No

3. Nature of conveyance:
X Assignment __ Merger
__ Security Agreement __ Change of Name
__ Other

Execution Date: May 6, 2002

2. Name and address of receiving party(ies):

Name: SILICON IMAGE, INC.
Street Address: 1060 E. Arques Avenue
Internal Address:
City: Sunnyvale State: CA Zip: 94085

Additional name(s) & address(es) attached? ____ Yes X No

4. Application number(s) or registration number(s):

A. Patent Application No.(s) 10/036,234

B. Patent No.(s)

Additional numbers attached? __ Yes X No

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GIRARD & EQUITZ LLP Date: 05/21/02

By: Marsha A. Townsend
Marsha A. Townsend

5. Name and address of party to whom correspondence concerning document should be mailed:

Name: Alfred A. Equitz
Internal Address: GIRARD & EQUITZ LLP
Street Address: 400 Montgomery Street #1110
City: San Francisco State: CA Zip: 94104

Telephone: (415) 433-2250
Facsimile: (415) 433-2255

Attorney Docket No. SII-1000 [SIMG0115]

6. Total number of applications and patents involved: 1

7. Total fee (37 C.F.R. 3.41) $ 40.00
X **Check Enclosed**

__ Authorized to be charged to deposit account

8. Deposit account number:
50-1697

DO NOT USE THIS SPACE

9. Statement and signature.
To the best of my knowledge and belief, the foregoing information is true and correct and any attached copy is a true copy of the original document.

Alfred A. Equitz Reg. No. 30,922
Name of Person Signing

Alfred A. Equitz
Signature

5/21/02
Date

Total number of pages including cover sheet, attachments and document: 2

Mail documents to be recorded with required cover sheet information to:
Box Assignment, Director – U.S. Patent and Trademark Office
Washington, D.C. 20231

COPY

Attorney Docket No. SII-1000 [SIMG0115]

ASSIGNMENT

WHEREAS, I, ALBERT M. SCALISE, hereinafter referred to as "ASSIGNOR", have invented, with SEUNG HO HWANG, JANO BANKS, PAUL DANIEL WOLF, ERIC LEE, and BAEGIN SUNG, certain new and useful improvements as described and set forth in the below-identified application for United States Letters Patent:

Title of Invention: **ENCODING METHOD AND SYSTEM FOR REDUCING INTER-SYMBOL INTERFERENCE EFFECTS IN TRANSMISSION OVER A SERIAL LINK**

Filing Date: December 24, 2001 Application No.: 10/036,234

WHEREAS, SILICON IMAGE, INC., a corporation of the State of Delaware, 1060 E. Arques Avenue, Sunnyvale, CA 94085 hereinafter referred to as "ASSIGNEE", is desirous of acquiring the entire right, title and interest in the said invention and application and in any Letters Patent which may be granted on the same;

NOW, THEREFORE, TO ALL WHOM IT MAY CONCERN: Be it known that, for One Dollar ($1.00) and other good and valuable consideration, receipt of which is hereby acknowledged by Assignor, Assignor has sold, assigned and transferred, and by these presents does sell, assign and transfer unto the said Assignee, and Assignee's successors and assigns, all of Assignor's right, title and interest in and to the said invention, said application for United States Letters Patent, and any Letters Patent which may hereafter be granted on the same in the United States and all countries throughout the world including any divisions, renewals, continuations in whole or in part, substitutions, conversions, reissues, prolongations or extensions thereof, said interest to be held and enjoyed by said Assignee as fully and exclusively as it would have been held and enjoyed by said Assignor had this assignment and transfer not been made, to the full end and term of any such Letters Patent.

Assignor further agrees that he will, without charge to said Assignee, but at Assignee's expense, cooperate with Assignee in the prosecution of said application and/or applications, execute, verify, acknowledge and deliver all such further papers, including applications for Letters Patent and for the reissue thereof, and instruments of assignment and transfer thereof, and will perform such other acts as Assignee lawfully may request, to obtain or maintain Letters Patent for said invention and improvement in any and all countries, and to vest title thereto in said Assignee, or Assignee's successors and assigns.

IN TESTIMONY WHEREOF, Assignor has hereunto signed his/her name to this assignment on the date indicated below.

Date: May 6, 2002

Albert M. Scalise

ALBERT M. SCALISE

OIPE JC177 APR 23 2002 PATENT & TRADEMARK OFFICE

COPY OF PAPERS
ORIGINALLY FILED

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of

SEUNG HO HWANG, et al.

Application No. 10/036,234

Filed: December 24, 2001

For: **ENCODING METHOD AND SYSTEM FOR REDUCING INTER-SYMBOL INTERFERENCE EFFECTS IN TRANSMISSION OVER A SERIAL LINK**

Group Art Unit: 2614

Examiner: Unknown

RESPONSE TO NOTICE OF INCOMPLETE REPLY TO NOTICE TO FILE MISSING PARTS OF APPLICATION

400 Montgomery Street, Suite 1110
San Francisco, CA 94104
(415) 433-2250

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to BOX MISSING PARTS, Commissioner for Patents, Washington, DC 20231, on April 15, 2002.

GIRARD & EQUITZ LLP Date: 04/15/02

By: Marsha A. Townsend

Marsha A. Townsend

BOX MISSING PARTS
Commissioner for Patents
Washington, DC 20231

Sir:

This is in response to the *Notice of Incomplete Reply (Nonprovisional)* mailed April 10, 2002 (copy enclosed) regarding the Notice to File Missing Parts of Application mailed February 7, 2002. In response, Applicants submit the enclosed Abstract.

The attached Abstract replaces the abstract originally filed on December 24, 2001, as page 44 of the application.

Also enclosed herewith is a *Petition for One Month Extension of Time to Respond*, in duplicate, together with a check in the amount of $110.00.

The Commissioner is hereby authorized to charge payment of any **additional** fees associated with this communication, or credit any overpayment to Deposit Account No. 50-1697. **A duplicate copy of this sheet is enclosed.**

Respectfully submitted,

GIRARD & EQUITZ LLP

Dated: 4/15/02 By: Alfred A. Equitz

Alfred A. Equitz
Reg. No. 30,922

Attorneys for Applicant(s)

Attorney Docket No. SII-1000 [SIMG0115]

OIPE JC177 APR 23 2002 PATENT & TRADEMARK OFFICE

UNITED STATES PATENT AND TRADEMARK OFFICE

COMMISSIONER FOR PATENTS
UNITED STATES PATENT AND TRADEMARK OFFICE
WASHINGTON, D.C. 20231
www.uspto.gov

APPLICATION NUMBER	FILING/RECEIPT DATE	FIRST NAMED APPLICANT	ATTORNEY DOCKET NUMBER
10/036,234	12/24/2001	Seung Ho Hwang	SII-1000 [SIMB0115]

CONFIRMATION NO. 6063

FORMALITIES LETTER

OC000000007838488

Alfred A. Equitz
GIRARD & EQUITZ LLP
Suite 1110
400 Montgomery Street
San Francisco, CA 94104

COPY OF PAPERS ORIGINALLY FILED

Date Mailed: 04/10/2002

NOTICE OF INCOMPLETE REPLY (NONPROVISIONAL)

Filing Date Granted

The U.S. Patent and Trademark Office has received your reply on 03/05/2002 to the Notice to File Missing Parts (Notice) mailed 02/07/2002 and it has been entered into the nonprovisional application. The reply, however, does not include the following items required in the Notice.

The period of reply remains as set forth in the Notice. You may, however, obtain EXTENSIONS OF TIME under the provisions of 37 CFR 1.136 (a) accompanied by the appropriate fee (37 CFR 1.17(a)).

A complete reply must be timely filed to prevent ABANDONMENT of the above-identified application.

The application is informal since it does not comply with the regulations for the reason(s) indicated below.

The required item(s) identified below must be timely submitted to avoid abandonment:

- Abstract must be on a separate sheet.

A copy of this notice MUST be returned with the reply.

Customer Service Center
Initial Patent Examination Division (703) 308-1202
PART 2 - COPY TO BE RETURNED WITH RESPONSE

PATENT

ABSTRACT OF THE DISCLOSURE

A communication system including a transmitter, a receiver, and a serial link, in which encoded data (e.g., encoded video data and encoded auxiliary data) are transmitted from the transmitter to the receiver. Other aspects of the invention are transmitters for use in encoding data for transmission over a serial link, and methods for sending encoded data over a serial link. In accordance with the invention, the data to be transmitted are encoded using a subset (sometimes referred to as a selected set of code words) of a full set of code words. The selected set of code words is selected such that each stream of encoded data (comprising only such code words) transmitted over a serial link has a bit pattern that is less susceptible to inter-symbol interference ("ISI") during transmission than is the bit pattern determined by a conventionally encoded version of the same data.

EXHIBIT 1002 - Page 353 of 443

OIPE JC177
APR 23 2002
PATENT & TRADEMARK OFFICE

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#8 0360

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of

SEUNG HO HWANG, et al.

Application No. 10/036,234

Filed: December 24, 2001

For: ENCODING METHOD AND SYSTEM FOR REDUCING INTER-SYMBOL INTERFERENCE EFFECTS IN TRANSMISSION OVER A SERIAL LINK

Group Art Unit: 2614

Examiner: Unknown

PETITION FOR A ONE MONTH EXTENSION OF TIME TO RESPOND UNDER 37 C.F.R. 1.136(a)

400 Montgomery Street, Suite 1110
San Francisco, CA 94104
(415) 433-2250

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to BOX MISSING PARTS, Commissioner for Patents, Washington, DC 20231, on April 15, 2002.

GIRARD & EQUITZ LLP Date: 04/15/02

By: Marsha A. Townsend

Marsha A. Townsend

BOX MISSING PARTS
Commissioner for Patents
Washington, DC 20231

Sir:

Applicants hereby petition for a one month extension of time to respond to the *Notice of Incomplete Reply (Nonprovisional)* mailed April 10, 2002 regarding the *Notice to File Missing Parts of Application* mailed February 7, 2002 in the above-referenced patent application. Please find enclosed a check in the amount of $110.00 to cover the extension fee.

The Commissioner is hereby authorized to charge payment of any fees associated with this communication or credit any overpayment to Deposit Account No. 50-1697. A **duplicate copy of this sheet is enclosed.**

04/24/2002 MROCHA1 00000007 10036234
01 FC:115 110.00 OP

Respectfully submitted,

GIRARD & EQUITZ LLP

Dated: 4/15/02

By: Alfred A. Equitz

Alfred A. Equitz
Reg. No. 30,922

Attorneys for Applicant(s)

Attorney Docket No. SII-1000 [SIMG0115]

Rev.02/14/01

UNITED STATES PATENT AND TRADEMARK OFFICE

COMMISSIONER FOR PATENTS
UNITED STATES PATENT AND TRADEMARK OFFICE
WASHINGTON, D.C. 20231
www.uspto.gov

APPLICATION NUMBER	FILING/RECEIPT DATE	FIRST NAMED APPLICANT	ATTORNEY DOCKET NUMBER
10/036,234	12/24/2001	Seung Ho Hwang	SII-1000 [SIMB0115]

CONFIRMATION NO. 6063

FORMALITIES LETTER

OC000000007838488

Alfred A. Equitz
GIRARD & EQUITZ LLP
Suite 1110
400 Montgomery Street
San Francisco, CA 94104

Date Mailed: 04/10/2002

NOTICE OF INCOMPLETE REPLY (NONPROVISIONAL)

Filing Date Granted

The U.S. Patent and Trademark Office has received your reply on 03/05/2002 to the Notice to File Missing Parts (Notice) mailed 02/07/2002 and it has been entered into the nonprovisional application. The reply, however, does not include the following items required in the Notice.

The period of reply remains as set forth in the Notice. You may, however, obtain EXTENSIONS OF TIME under the provisions of 37 CFR 1.136 (a) accompanied by the appropriate fee (37 CFR 1.17(a)).

A complete reply must be timely filed to prevent ABANDONMENT of the above-identified application.

The application is informal since it does not comply with the regulations for the reason(s) indicated below.

The required item(s) identified below must be timely submitted to avoid abandonment:

- Abstract must be on a separate sheet.

A copy of this notice MUST be returned with the reply.

Customer Service Center
Initial Patent Examination Division (703) 308-1202

PART 3 - OFFICE COPY

OIPE JC100 MAR 2 5 2002 PATENT & TRADEMARK OFFICE

GP 2614 (8)

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

RECEIVED MAR 2 8 2002 Technology Center 2600

In re Patent Application of

SEUNG HO HWANG, et al.

Application No. 10/036,234

Filed: December 24, 2001

For: **ENCODING METHOD AND SYSTEM FOR REDUCING INTER-SYMBOL INTERFERENCE EFFECTS IN TRANSMISSION OVER A SERIAL LINK**

Group Art Unit: 2614

Examiner: Unknown

TRANSMITTAL OF POWER OF ATTORNEY BY ASSIGNEE

400 Montgomery Street, Suite 1110
San Francisco, CA 94104
(415) 433-2250

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to Commissioner for Patents, Washington, DC 20231, on March 13, 2002.

GIRARD & EQUITZ LLP Date: 03/13/02

By: Marsha A. Townsend

Marsha A. Townsend

Commissioner for Patents
Washington, D.C. 20231

Sir:

The *Power of Attorney by Assignee and Establishment of Right of Assignee to Prosecute Under 37 C.F.R. § 3.73(b)* is hereby submitted in the above application and it is respectfully requested that it be made of record.

Respectfully submitted,

GIRARD & EQUITZ LLP

Dated: 3/13/02 By: Alfred A Equitz

Alfred A. Equitz
Reg. No.30,922

Attorneys for Applicant(s)

Attorney Docket No. SII-1000 [SIMG0115]

OIPE JC40
MAR 2 5 2002
PATENT & TRADEMARK OFFICE

Attorney Docket No.: SII-1000 [SIMG0115]

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

RECEIVED
MAR 2 8 2002
Technology Center 2600

APPLICATION FOR UNITED STATES PATENT

In re Patent Application of

SEUNG HO HWANG, et al.

Application No. 10/036,234

Filed: December 24, 2001

For: **ENCODING METHOD AND SYSTEM FOR REDUCING INTER-SYMBOL INTERFERENCE EFFECTS IN TRANSMISSION OVER A SERIAL LINK**

Group Art Unit: 2614

Examiner: Unknown

POWER OF ATTORNEY BY ASSIGNEE AND CERTIFICATE BY ASSIGNEE UNDER 37 C.F.R. §3.73(b)

400 Montgomery Street, Suite 1110
San Francisco, CA 94104
(415) 433-2250

Commissioner for Patents
Washington, DC 20231

Sir:

SILICON IMAGE, INC., assignee of the entire right title and interest in the above-identified application by assignment dated February 20, 2002 and February 21, 2002, which assignment is [ ] recorded in the Patent and Trademark Office at Reel _____, Frame _____, or **[X] a copy of which is submitted herewith**, and hereby appoints the members of the firm of GIRARD & EQUITZ LLP, a firm composed of

Philip A. Girard 28,848 Alfred A. Equitz 30,922

400 Montgomery Street, Suite 1110, San Francisco, CA 94104, (415) 433-2250, FAX (415) 433-2255, as its attorneys/agents with full power of substitution to prosecute this application and to transact all business in the Patent and Trademark Office in connection therewith. The undersigned is empowered to sign this statement and appointment on behalf of assignee.

Please direct all correspondence regarding this application to the following:

GIRARD & EQUITZ LLP
Attn: Alfred A. Equitz
400 Montgomery Street. Suite 1110
San Francisco, CA 94104
Telephone: (415) 433-2250
Facsimile: (415) 433-2255

The assignee certifies that it has reviewed the assignment and to the best of the assignee's knowledge and belief, title is in the assignee.

SILICON IMAGE, INC.

Dated: 3/7/02 By: Badar Bagai

Name: Badar Bagai
Title: Executive V.P., Engineering

Attorney Docket No. SII-1000 [SIMG0115]

ASSIGNMENT

WHEREAS, WE, Seung Ho Hwang, Jano Banks, Paul Daniel Wolf, Eric Lee, and Baegin Sung hereinafter referred to as "ASSIGNORS", have invented certain new and useful improvements as described and set forth in the below-identified application for United States Letters Patent:

Title of Invention: **ENCODING METHOD AND SYSTEM FOR REDUCING INTER-SYMBOL INTERFERENCE EFFECTS IN TRANSMISSION OVER A SERIAL LINK**

Filing Date: December 24, 2001 Application No.: 10/036,234

WHEREAS, SILICON IMAGE, INC., a corporation of the State of Delaware, 1060 E. Arques Avenue, Sunnyvale, CA 94085 hereinafter referred to as "ASSIGNEE", is desirous of acquiring the entire right, title and interest in the said invention and application and in any Letters Patent which may be granted on the same;

NOW, THEREFORE, TO ALL WHOM IT MAY CONCERN: Be it known that, for One Dollar ($1.00) and other good and valuable consideration, receipt of which is hereby acknowledged by Assignors, Assignors have sold, assigned and transferred, and by these presents do sell, assign and transfer unto the said Assignee, and Assignee's successors and assigns, all right, title and interest in and to the said invention, said application for United States Letters Patent, and any Letters Patent which may hereafter be granted on the same in the United States and all countries throughout the world including any divisions, renewals, continuations in whole or in part, substitutions, conversions, reissues, prolongations or extensions thereof, said interest to be held and enjoyed by said Assignee as fully and exclusively as it would have been held and enjoyed by said Assignors had this assignment and transfer not been made, to the full end and term of any such Letters Patent.

Assignors further agree that they will, without charge to said Assignee, but at Assignee's expense, cooperate with Assignee in the prosecution of said application and/or applications, execute, verify, acknowledge and deliver all such further papers, including applications for Letters Patent and for the reissue thereof, and instruments of assignment and transfer thereof, and will perform such other acts as Assignee lawfully may request, to obtain or maintain Letters Patent for said invention and improvement in any and all countries, and to vest title thereto in said Assignee, or Assignee's successors and assigns.

IN TESTIMONY WHEREOF, Assignor has hereunto signed his/her name to this assignment on the date indicated below.

Date: 2/20/02

Seung Ho Hwang

IN TESTIMONY WHEREOF, Assignor has hereunto signed his/her name to this assignment on the date indicated below.

Date: 2/21/02

Jano Banks

IN TESTIMONY WHEREOF, Assignor has hereunto signed his/her name to this assignment on the date indicated below.

Date: 2/21/02

Paul Daniel Wolf

IN TESTIMONY WHEREOF, Assignor has hereunto signed his/her name to this assignment on the date indicated below.

Date: 2-20-02

Eric Lee

IN TESTIMONY WHEREOF, Assignor has hereunto signed his/her name to this assignment on the date indicated below.

Date: 2-021-02

Baegin Sung

OIPE
MAR 1 1 2002
PATENT & TRADEMARK OFFICE

HH

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of

SEUNG HO HWANG, et al.

Application No. 10/036,234

Filed: December 24, 2001

For: **ENCODING METHOD AND SYSTEM FOR REDUCING INTER-SYMBOL INTERFERENCE EFFECTS IN TRANSMISSION OVER A SERIAL LINK**

Group Art Unit: 2614

Examiner: Unknown

RESPONSE TO NOTICE TO FILE MISSING PARTS OF APPLICATION AND SUBMISSION OF DECLARATION

400 Montgomery Street, Suite 1110
San Francisco, CA 94104
(415) 433-2250

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to BOX MISSING PARTS, Commissioner for Patents, Washington, DC 20231, on February 25, 2002.

GIRARD & EQUITZ LLP Date: 02/25/02

By: Marsha A. Townsend

Marsha A. Townsend

BOX MISSING PARTS
Commissioner for Patents
Washington, DC 20231

Sir:

In response to the Notice to File Missing Parts of Application mailed February 7, 2002 (copy enclosed), Applicant submits the enclosed Declaration for Patent Application.

A check in the amount of $130.00 is enclosed herewith to cover the surcharge for filing missing parts of an application.

The Commissioner is hereby authorized to charge payment of any **additional** fees associated with this communication, or credit any overpayment to Deposit Account No. 50-1697. **A duplicate copy of this sheet is enclosed.**

Respectfully submitted,

GIRARD & EQUITZ LLP

Dated: 2/25/02 By: Alfred A Equitz

Alfred A. Equitz
Reg. No. 30,922

Attorneys for Applicant(s)

Attorney Docket No. SII-1000 [SIMG0115]

Rev.02/14/01

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PATENT & TRADEMARK OFFICE
JC35

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of

SEUNG HO HWANG, et al.

Application No. 10/036,234

Filed: December 24, 2001

For: **ENCODING METHOD AND SYSTEM FOR REDUCING INTER-SYMBOL INTERFERENCE EFFECTS IN TRANSMISSION OVER A SERIAL LINK**

Group Art Unit: 2614

Examiner: Unknown

RESPONSE TO NOTICE TO FILE MISSING PARTS OF APPLICATION AND SUBMISSION OF DECLARATION

400 Montgomery Street, Suite 1110
San Francisco, CA 94104
(415) 433-2250

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to BOX MISSING PARTS, Commissioner for Patents, Washington, DC 20231, on February 25, 2002.

GIRARD & EQUITZ LLP Date: 02/25/02

By: Marsha A. Townsend

Marsha A. Townsend

BOX MISSING PARTS
Commissioner for Patents
Washington, DC 20231

Sir:

In response to the Notice to File Missing Parts of Application mailed February 7, 2002 (copy enclosed), Applicant submits the enclosed Declaration for Patent Application.

A check in the amount of $130.00 is enclosed herewith to cover the surcharge for filing missing parts of an application.

The Commissioner is hereby authorized to charge payment of any **additional** fees associated with this communication, or credit any overpayment to Deposit Account No. 50-1697. **A duplicate copy of this sheet is enclosed.**

Respectfully submitted,

GIRARD & EQUITZ LLP

Dated: 2/25/02 By: Alfred A. Equitz

Alfred A. Equitz
Reg. No. 30,922

Attorneys for Applicant(s)

Attorney Docket No. SII-1000 [SIMG0115]

Rev.02/14/01

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JC35
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UNITED STATES PATENT AND TRADEMARK OFFICE

COMMISSIONER FOR PATENTS
UNITED STATES PATENT AND TRADEMARK OFFICE
WASHINGTON, D.C. 20231
www.uspto.gov

APPLICATION NUMBER	FILING/RECEIPT DATE	FIRST NAMED APPLICANT	ATTORNEY DOCKET NUMBER
10/036,234	12/24/2001	Seung Ho Hwang	SII-1000

CONFIRMATION NO. 6063

FORMALITIES LETTER

OC000000007434854

Alfred A. Equitz
GIRARD & EQUITZ LLP
Suite 1110
400 Montgomery Street
San Francisco, CA 94104

Date Mailed: 02/07/2002

NOTICE TO FILE MISSING PARTS OF NONPROVISIONAL APPLICATION

03/12/2002 SZEWDIE1 00000045 10036234
01 FC:105 130.00 OP

FILED UNDER 37 CFR 1.53(b)

Filing Date Granted

An application number and filing date have been accorded to this application. The item(s) indicated below, however, are missing. Applicant is given **TWO MONTHS** from the date of this Notice within which to file all required items and pay any fees required below to avoid abandonment. Extensions of time may be obtained by filing a petition accompanied by the extension fee under the provisions of 37 CFR 1.136(a).

- The oath or declaration is unsigned.
- To avoid abandonment, a late filing fee or oath or declaration surcharge as set forth in 37 CFR 1.16(l) of $130 for a non-small entity, must be submitted with the missing items identified in this letter.
- **The balance due by applicant is $ 130.**

The application is informal since it does not comply with the regulations for the reason(s) indicated below.

The required item(s) identified below must be timely submitted to avoid abandonment:

- Substitute drawings in compliance with 37 CFR 1.84 because:
    - drawing sheets do not have the appropriate margin(s) (see 37 CFR 1.84(g)). Each sheet must include a top margin of at least 2.5 cm. (1 inch), a left side margin of at least 2.5 cm. (1 inch), a right side margin of at least 1.5 cm. (5/8 inch), and a bottom margin of at least 1.0 cm. (3/8 inch);
- An Abstract not to exceed 150 words in length, commencing on a separate sheet (37 CFR 1.72(b)).

A copy of this notice <u>MUST</u> be returned with the reply.

Customer Service Center
Initial Patent Examination Division (703) 308-1202
PART 2 - COPY TO BE RETURNED WITH RESPONSE

Electronic Acknowledgement Receipt



#2

Atty Docket No. SII-1000 [SIMG0115]

DECLARATION FOR PATENT APPLICATION

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name,

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

ENCODING METHOD AND SYSTEM FOR REDUCING INTER-SYMBOL INTERFERENCE EFFECTS IN TRANSMISSION OVER A SERIAL LINK

the specification of which (check one) __ is attached hereto or X was filed on December 24, 2001 as Application No. 10/036,234 .

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose all information which is material to patentability as defined in 37 CFR § 1.56.

I hereby claim foreign priority benefits under 35 U.S.C. § 119(a)-(d) or § 365(b) of any foreign application(s) for patent or inventor's certificate, or § 365(a) of any PCT International application which designated at least one country other than the United States, listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Prior Foreign Application(s)			Priority Claimed Yes	No
Number	Country	Day/Month/Year Filed	____	____
Number	Country	Day/Month/Year Filed	____	____

I hereby claim the benefit under 35 U.S.C. § 119(e) of any United States provisional application(s) below.

Application Number	Filing Date
Application Number	Filing Date

I hereby claim the benefit under 35 U.S.C. § 120 of any United States application(s), or § 365(c) of any PCT International application designating the United States, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of 35 U.S.C. § 112, I acknowledge the duty to disclose all information which is material to patentability as defined in 37 CFR § 1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application:

Application Number	Filing Date	Status: Patented, Pending, Abandoned
09/954,663	09/12/2001	Pending
Application Number	Filing Date	Status: Patented, Pending, Abandoned

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment or both, under 18 U.S.C. § 1001 and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full name of sole or first inventor SEUNG HO HWANG

Inventor's signature _____ 2/20/02
Date

Residence 1690 Edgewood Drive, Palo Alto, CA 94303

Citizenship USA

Post Office Address 1690 Edgewood Drive, Palo Alto, CA 94303

Full name of second joint inventor, if any, JANO BANKS

Inventor's signature _____ 2/21/02
Date

Residence 19621 La Mar Court, Cupertino, CA 95014

Citizenship USA

Post Office Address 19621 La Mar Court, Cupertino, CA 95014

Full name of third joint inventor, if any, PAUL DANIEL WOLF

Inventor's signature _____ 2/21/02
Date

Residence 2696 Eaton Avenue, San Carlos, CA 94070

Citizenship USA

Post Office Address 2696 Eaton Avenue, San Carlos, CA 94070

Full name of fourth joint inventor, if any, ERIC LEE

Inventor's signature _____ 2-20-02
Date

Residence 1028 South De Anza Blvd., Apt. B208, San Jose, CA 95129

Citizenship USA

Post Office Address P.O. Box 64395, Sunnyvale, CA 94088

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment or both, under 18 U.S.C. § 1001 and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full name of fifth joint inventor, if any, BAEGIN SUNG

Inventor's signature Baegin Sung 2-21-02
Date

Residence 1657 Ontario Drive, #12, Sunnyvale, CA 94087

Citizenship KOREA

Post Office Address 1657 Ontario Drive, #12, Sunnyvale, CA 94087

MAR 0 5 2002
PATENT &

2614

GIRARD & EQUITZ LLP
400 Montgomery Street, Suite 1110
San Francisco, CA 94104
(415) 433-2250

COPY OF PAPERS ORIGINALLY FILED

In re Patent Application of: SEUNG HO HWANG, et al. Attorney's Docket No. SII-1000 [~~SIMG~~0115]

Application No. 10/036,234 Group Art Unit: 2614

Filed December 24, 2001 Examiner: Unknown

For: **ENCODING METHOD AND SYSTEM FOR REDUCING INTER-SYMBOL INTERFERENCE EFFECTS IN TRANSMISSION OVER A SERIAL LINK**

RECEIVED
MAR 1 4 2002
Technology Center 2600

Commissioner for Patents
Washington, DC 20231

Sir:

Transmitted herewith is a ***Preliminary Amendment*** in the above-identified application.

The fee has been calculated as shown below.

	Claims Remaining After Amendment	Highest Number Previously Paid For	Present Extra	Rate	Additional Fee
Total	79	75	4	$18	$72.00
Independent	4	4	0	$84	$
☐ First Presentation of Multiple Dependent Claims				$280	$
				Total	$72.00
☐ Small Entity 50 percent Filing Fee Reduction (if applicable)					$

1. ☐ No additional fee is required.

2. ☒ A check in the amount of $72.00 is attached.

3. ☒ Please charge any additional fees, including any fees necessary for extensions of time, or credit overpayment to Deposit Account No. 50-1697. **A duplicate copy of this sheet is enclosed.**

4. ☐ Petition for extension of time. The undersigned attorney of record hereby petitions for an extension of time pursuant to 37 C.F.R. § 1.136(a), as may be required, to file this response.

GIRARD & EQUITZ LLP

February 13, 2002
Date

By: Alfred A Equitz
Alfred A. Equitz
Registration Number 30,922
Attorney(s) or Agent(s) of Record

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Dated: FEBRUARY 13, 2002

By: Marsha A. Townsend
Marsha A. Townsend

Amendment Application Transmittal Form
Rev. Date 02/14/2001

EA

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GIRARD & EQUITZ LLP
400 Montgomery Street, Suite 1110
San Francisco, CA 94104
(415) 433-2250

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In re Patent Application of: SEUNG HO HWANG, et al.

Attorney's Docket No. SII-1000 [SIMG0115]

Application No. 10/036,234

Group Art Unit: 2614

Filed December 24, 2001

Examiner: Unknown

For: **ENCODING METHOD AND SYSTEM FOR REDUCING INTER-SYMBOL INTERFERENCE EFFECTS IN TRANSMISSION OVER A SERIAL LINK**

Commissioner for Patents
Washington, DC 20231

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Sir:

Transmitted herewith is a ***Preliminary Amendment*** in the above-identified application.

The fee has been calculated as shown below.

	Claims Remaining After Amendment	Highest Number Previously Paid For	Present Extra	Rate	Additional Fee
Total	79	75	4	$18	$72.00
Independent	4	4	0	$84	$
☐ First Presentation of Multiple Dependent Claims				$280	$
				Total	$72.00
☐ Small Entity 50 percent Filing Fee Reduction (if applicable)					$

1. ☐ No additional fee is required.

2. ☒ A check in the amount of $72.00 is attached.

3. ☒ Please charge any additional fees, including any fees necessary for extensions of time, or credit overpayment to Deposit Account No. 50-1697. **A duplicate copy of this sheet is enclosed.**

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GIRARD & EQUITZ LLP

February 13, 2002
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Registration Number 30,922
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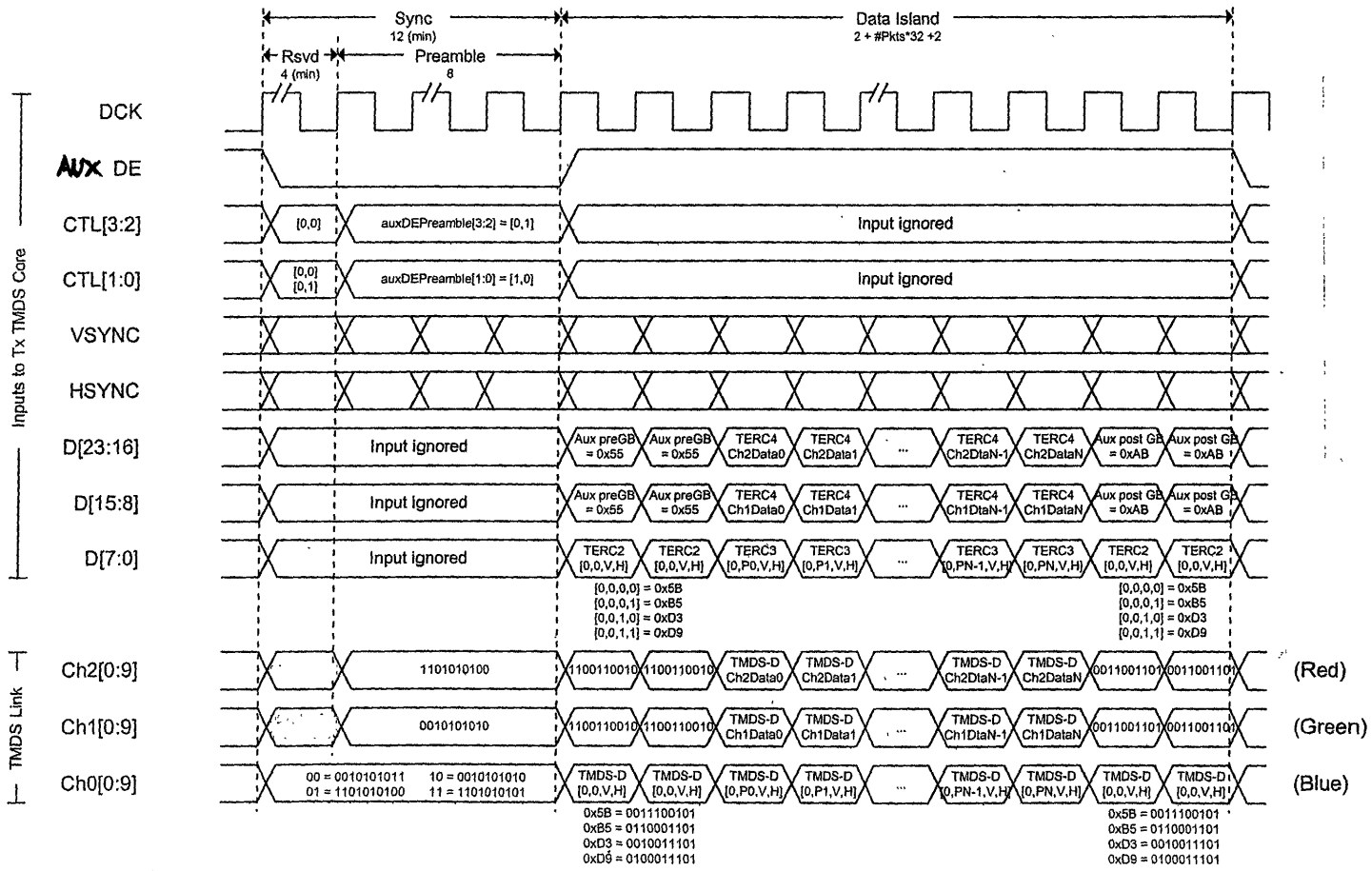
Dated: FEBRUARY 13, 2002

By: Marsha A. Townsend
Marsha A. Townsend

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Fig. 5



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5/8 Pg 1 of 12

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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In re Patent Application of

SEUNG HO HWANG, et al.

Application No. 10/036,234

Filed: December 24, 2001

For: **ENCODING METHOD AND SYSTEM FOR REDUCING INTER-SYMBOL INTERFERENCE EFFECTS IN TRANSMISSION OVER A SERIAL LINK**

Group Art Unit: 2614

Examiner: Unknown

PRELIMINARY AMENDMENT

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GIRARD & EQUITZ LLP Date: 02/13/02

By: Marsha A. Townsend

Marsha A. Townsend

Commissioner for Patents
Washington, D.C. 20231

Sir:

This is a preliminary amendment in the referenced application. Please amend the application as follows.

IN THE ABSTRACT:

Replace the originally filed abstract with the following abstract:

A communication system including a transmitter, a receiver, and a serial link, in which encoded data (e.g., encoded video data and encoded auxiliary data) are transmitted from the transmitter to the receiver. The serial link can but need not be a TMDS or TMDS-like link. In typical embodiments, alternating bursts of encoded video data and encoded auxiliary data are transmitted over each of one or more channels of the link. Other aspects of the invention are transmitters for use in encoding data for transmission over a serial link, and methods for sending encoded data over a serial link. In accordance with the invention, the data to be transmitted are encoded using a subset (sometimes referred to as a selected set of

B1

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code words) of a full set of code words. The selected set of code words is selected such that each stream of encoded data (comprising only such code words) transmitted over a serial link has a bit pattern that is less susceptible to inter-symbol interference ("ISI") during transmission than is the bit pattern determined by a conventionally encoded version of the same data (comprising not only the selected set of code words but also other members of the full set). In general, the best choice for the selected set of code words selected from a full set of binary code words depends on the particular coding implemented by the full set. Typically, the selected set of code words includes words whose serial patterns (during transmission) have fewer contiguous zeros and ones (and thus are less susceptible to ISI during transmission) than do those code words in the full set that are not selected. In preferred embodiments in which the bits of the selected set of code words are transmitted over a serial link as sequences of rising and falling voltage transitions, the bit pattern of each transmitted stream of the selected set of code words implements DC balancing to limit the voltage drift over time.

IN THE SPECIFICATION:

[attached is an Appendix including a marked up version of the amended sections of the specification showing the differences between the text as originally filed, and the text as hereby amended]:

Replace page 2, line 14, with the following text: --over conductor pairs);--

Replace page 23, line 22, with the following text: --the bottom of Fig. 6) is transmitted--.

Replace page 27, line 4, with the following text: -- available the appropriate number of guard band words is a factor in the selection of the--.

Replace page 29, line 9, with the following text: --bits). Each possible value of the M-bit source data has a preselected code in the 2^M --.

Replace page 29, line 11, with the following text: --are mapped to inventive code words in the 2^M word space which are then transmitted--.

Replace page 29, line 31, with the following text: --and Q[8]) present greater error risks than do the other bits. Any bit error occurring--.

IN THE CLAIMS:

Delete original claims 55 and 75.

Amend claims 16, 17, 25, 31, 32, 43, 44, 52, 64, 65, and 73 to read as follows [attached is an Appendix including a marked up version of the amended claims showing the differences between the claims as originally filed, and the claims as hereby amended]:

16. (Amended) The system of claim 15, wherein the selected code words consist of seventeen different TMDS code words, including at least one TMDS code word used only as a guard band word.

B5

17. (Amended) The system of claim 15, wherein the selected code words consist of seventeen different, transition-minimized TMDS code words, including at least one transition-minimized TMDS code word used only as a guard band word.

B6

25. (Amended) The system of claim 1, wherein each of the selected code words is indicative of a sequence of L binary bits, and the selected code words have fewer contiguous zero bits and contiguous one bits per code word on the average than do the code words of the full code word set excluding the selected code words.

B7

31. (Amended) The system of claim 30, wherein the selected code words consist of seventeen different TMDS code words, including at least one TMDS code word used only as a guard band word.

32. (Amended) The system of claim 30, wherein the selected code words consist of seventeen, different, transition-minimized TMDS code words, including at least one transition-minimized TMDS code word used only as a guard band word.

43. (Amended) The transmitter of claim 34, wherein the serial link is a TMDS link, and the selected code words consist of seventeen different TMDS code words, including at least one TMDS code word used only as a guard band word.

B8

44. (Amended) The transmitter of claim 43, wherein the selected code words consist of seventeen different, transition-minimized TMDS code words, including at least one transition-minimized TMDS code word used only as the guard band word.

B9

52. (Amended) The transmitter of claim 33, wherein each of the selected code words is indicative of a sequence of L binary bits, and the selected code words have fewer contiguous zero bits and contiguous one bits per code word on the average than do the code words of the full code word set excluding the selected code words.

64. (Amended) The method of claim 54, wherein the selected code words consist of seventeen different TMDS code words, including at least one TMDS code word used only as a guard band word.

B10

65. (Amended) The method of claim 54, wherein the selected code words consist of seventeen different, transition-minimized TMDS code words, including at least one transition-minimized TMDS code word used only as a guard band word.

B11

73. (Amended) The method of claim 54, wherein each of the selected code words is indicative of a sequence of L binary bits, and the selected code words have fewer contiguous zero bits and contiguous one bits per code word on the average than do the code words of the full code word set excluding the selected code words.

Add the following new claims:

76. (New) The system of claim 27, wherein the transmitter is also coupled to receive control bits, configured to generate bursts of encoded control words by encoding the control bits, and configured to transmit to the receiver over the serial link a first burst of the encoded control words between the first burst of the video code words and the bursts of the selected code words, and a second burst of the encoded control words between the bursts of the selected code words and the second burst of the video code words.

77. (New) The system of claim 76, wherein the selected code words include at least one guard band word, a first one of the bursts of the selected code words has an initial word, and the initial word is the guard band word.

78. (New) The system of claim 76, wherein the selected code words include at least one guard band word, a first one of the bursts of the selected code words has an initial set of words, and each word of the initial set of words is one said guard band word.

B12

79. (New) The method of claim 54, wherein the input data are auxiliary data, and also including the steps of:

generating a sequence of video code words by encoding video data; and

transmitting over the link a first burst of the video code words followed by a burst of the selected code words followed by a second burst of the video code words, wherein each of the video code words is a member of the full code word set and at least one of the video code words is not a member of the robust subset.

80. (New) The method of claim 54, wherein the input data are auxiliary data, and also including the steps of:

generating a sequence of video code words by encoding video data; and

transmitting over the link a first burst of the video code words followed by at least two bursts of the selected code words followed by a second burst of the video code words, wherein each of the video code words is a member of the full code word set and at least one of the video code words is not a member of the robust subset.

81. (New) The transmitter of claim 33, wherein the input data include auxiliary data and video data, and the circuitry is configured to generate a sequence of video code words by encoding the video data, and to assert to the output a first burst of the video code words followed by at least two bursts of the selected code words followed by a second burst of the video code words, wherein each of the video code words is a member of the full code word set and at least one of the video code words is not a member of the robust subset.

REMARKS:

Please enter the foregoing amendments and add new claims 76-81.

Also, attached for review and approval by the Examiner are proposed revised versions of Figs. 2, 3, and 5 with the proposed changes shown in red ink. The proposed revised drawings are being submitted simultaneously to the Official Draftsman for review. The proposed change to Fig. 2 is to conform Fig. 2 to the description thereof at page 16, last paragraph, of the specification. The proposed change to Fig.3 is to conform Fig. 3 to the description at page 22, last line to page 23, line 3, and page 23, last paragraph, of the specification. The proposed change to Fig. 5 is to conform to the description at page 22, lines 11-25, of the specification.

Respectfully submitted,

GIRARD & EQUITZ LLP

Dated: 2/13/02 By: Alfred A. Equitz

Alfred A. Equitz
Reg. No.30,922

Attorneys for Applicant(s)

Attorney Docket No. SII-1000 [SIMG-0115]

MAR 0 5 2002 PATENT & TRADEMARK OFFICE
MAR 0 5 2002 OIPE JC87

APPENDIX

Replace page 2, line 14, with the following text: --over conductor pairs [without the presence of a ground line]);--.

Replace page 23, line 22, with the following text: --the bottom of Fig. 6 [, or a polarity inverted version of this code word]) is transmitted--.

Replace page 27, line 4, with the following text: -- available the appropriate number of guard band [word] words is a factor in the selection of the

Replace page 29, line 9, with the following text: --bits). Each possible value of the M-bit source data has a preselected code in the 2^M[-] --.

Replace page 29, line 11, with the following text: --are mapped to inventive code words in the 2^M [-] word space which are then transmitted--.

Replace page 29, line 31, with the following text: --and [E[8]] Q[8]) present greater error risks than do the other bits. Any bit error occurring-

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Amend claims 16, 17, 25, 31, 32, 43, 44, 52, 64-65, and 71 to read as follows:

16. (Amended) The system of claim 15, wherein the selected code words consist of seventeen different TMDS code words, including at least one TMDS code word used only as a guard band word.

17. (Amended) The system of claim 15, wherein the selected code words consist of seventeen different, transition-minimized TMDS code words, including at least one transition-minimized TMDS code word used only as a guard band word.

25. (Amended) The system of claim 1, wherein each of the selected code words is indicative of a sequence of L binary bits, and the selected code words have fewer contiguous zero bits and [continuous] contiguous one bits per code word on the average than do the code words of the full code word set excluding the selected code words.

31. (Amended) The system of claim 30, wherein the selected code words consist of seventeen different TMDS code words, including at least one TMDS code word used only as a guard band word.

32. (Amended) The system of claim 30, wherein the selected code words consist of seventeen, different, transition-minimized TMDS code words, including at least one transition-minimized TMDS code word used only as a guard band word.

43. (Amended) The transmitter of claim 34, wherein the serial link is a TMDS link, and the selected code words consist of seventeen different TMDS code words, including at least one TMDS code word used only as a guard band word.

44. (Amended) The transmitter of claim 43, wherein the selected code words consist of seventeen different, transition-minimized TMDS code words, including at least one transition-minimized TMDS code word used only as the guard band word.

52. (Amended) The transmitter of claim 33, wherein each of the selected code words is indicative of a sequence of L binary bits, and the selected code words have fewer contiguous zero bits and [continuous] contiguous one bits per code word on the average than do the code words of the full code word set excluding the selected code words.

64. (Amended) The method of claim 54, wherein the selected code words consist of seventeen different TMDS code words, including at least one TMDS code word used only as a guard band word.

65. (Amended) The method of claim 54, wherein the selected code words consist of seventeen different, transition-minimized TMDS code words, including at least one transition-minimized TMDS code word used only as a guard band word.

73. (Amended) The method of claim 54, wherein each of the selected code words is indicative of a sequence of L binary bits, and the selected code words have fewer contiguous zero bits and [continuous] contiguous one bits per code word on the average than do the code words of the full code word set excluding the selected code words.

Specific CTL	CTL [1:0]	Preamble (q0 : q9)	Guardband (q0 : q9)	GB (d7 : d0)	Purpose
R (CTL [3:2])	00	0010101011	0011001101	0xAB	Video Preamble/Video Guardband/Post-Data Aux Guardband
G (CTL [1:0])	00	0010101011	0011001101	0xAB	Video Preamble/Video Guardband/Post-Data Aux Guardband
B (VSYNC:HSYNC)	XX	1 of 4 values	0011001101	0xAB	Video Preamble/Video Guardband
R (CTL [3:2])	01	1101010100	1100110010	0x55	Aux Preamble/Pre-Data Aux Guardband
G (CTL [1:0])	10	0010101010	1100110010	0x55	Aux Preamble/Pre-Data Aux Guardband
B (VSYNC:HSYNC)	XX	1 of 4 values	1 of 4 values	0x5B,0xB5, 0xD3, 0xD9	Aux Preamble/Pre- or Post-Data Aux Guardband
R (CTL [3:2])	10	0010101010			VSync Window, HDCP enabled
G (CTL [1:0])	00	0010101011			VSync Window, HDCP enabled
B (VSYNC:HSYNC)	1X	1 of 2 values			VSync Window, HDCP enabled

XX

4

FIG. 3

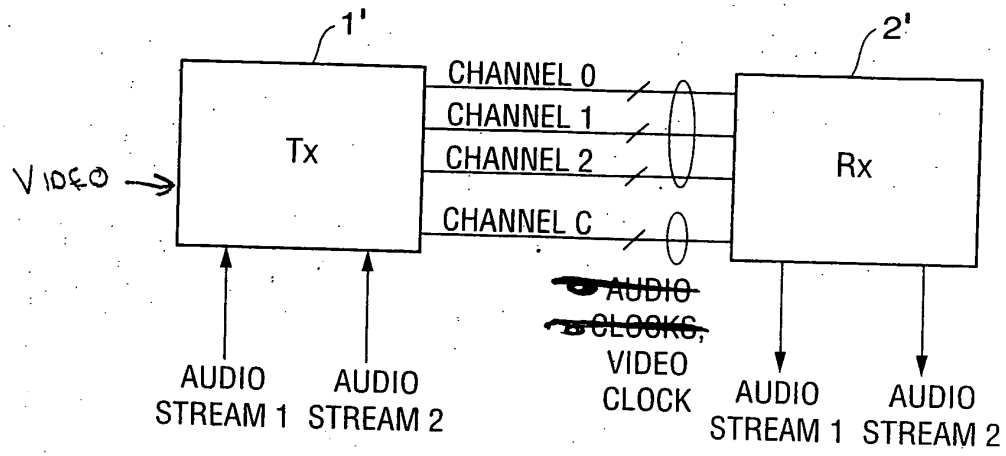
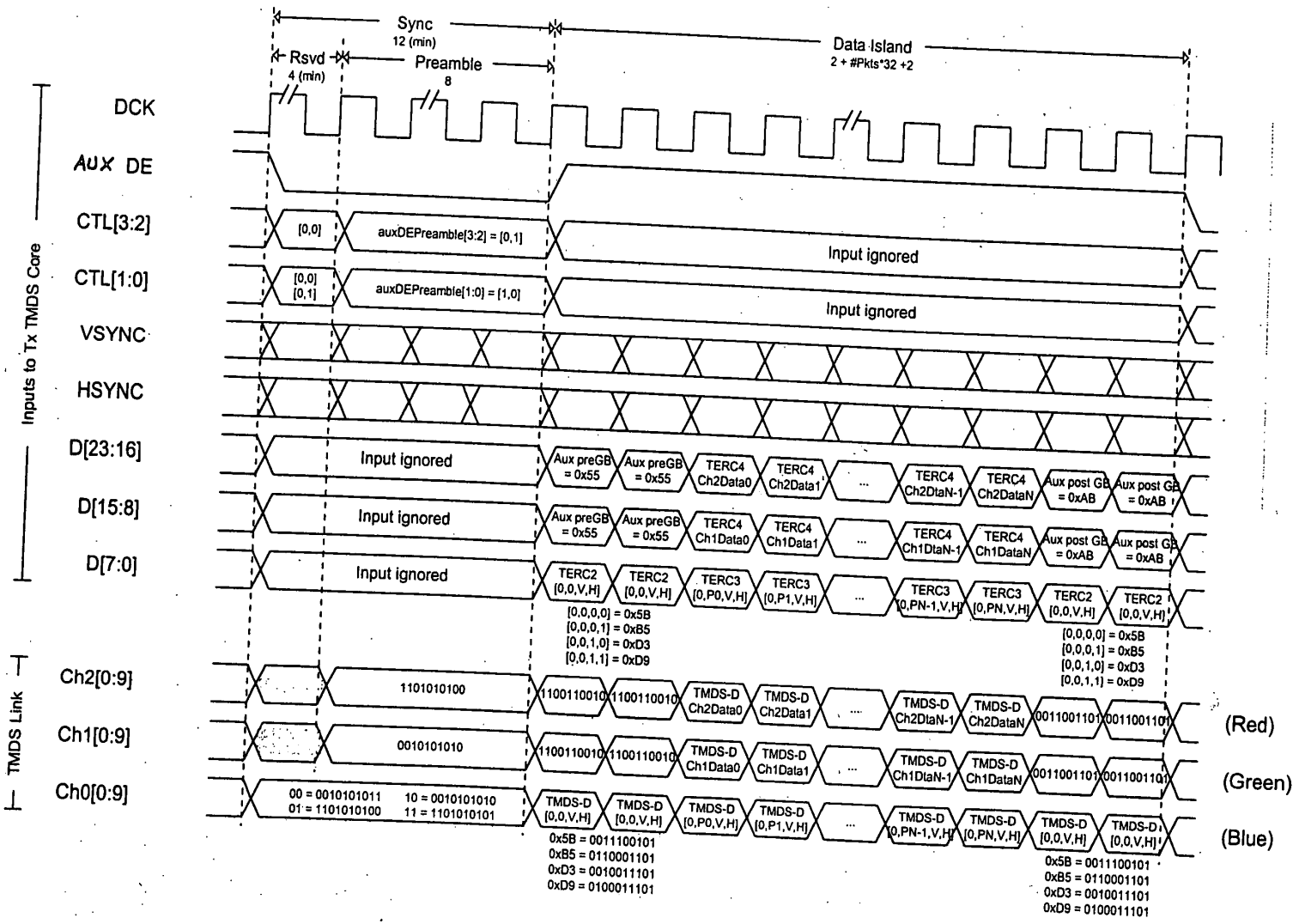


FIG. 2

	Input D7-D0	Hex	TMDS pattern
PRE-DATA GUARD BAND for Aux data	01010101	55	1100110010
AD0	01011011	5B	0011100101
AD1	10110101	B5	0110001101
AD2	11010011	D3	0010011101
AD3	11011001	D9	0100011101
AD4	01101101	6D	0111000101
AD5	10100100	A4	0011100110
AD6	10010010	92	0111000110
AD7	01000100	44	0011110010
AD8	00100010	22	0111100010
AD9	01001011	4B	1001110010
AD10	10010011	93	1000111010
GUARD BAND for video data and POST-DATA GUARD BAND for Aux data (and AD11)	10101011	AB	0011001101
AD12	01011010	5A	1100011001
AD13	01101100	6C	1000111001
AD14	10100101	A5	1100011010
AD15	10111010	BA	1100001101

FIG. 4

FIG. 5


Sync
12 (min)
Rsvd
4 (min)
Preamble
8
Data Island
2 + #Pkts*32 +2
Inputs to Tx TMDS Core
DCK
AUX DE
CTL[3:2]
CTL[1:0]
VSYNC
HSYNC
D[23:16]
D[15:8]
D[7:0]
TMDS Link
Ch2[0:9]
Ch1[0:9]
Ch0[0:9]
[0,0]
auxDEPreamble[3:2] = [0,1]
Input ignored
[0,0]
[0,1]
auxDEPreamble[1:0] = [1,0]
Aux preGB = 0x55
TERC4 Ch2Data0
TERC4 Ch2Data1
TERC4 Ch2DtaN-1
TERC4 Ch2DataN
Aux post GB = 0xAB
TERC4 Ch1Data0
TERC4 Ch1Data1
TERC4 Ch1DtaN-1
TERC4 Ch1DataN
TERC2 [0,0,V,H]
TERC3 [0,P0,V,H]
TERC3 [0,P1,V,H]
TERC3 [0,PN-1,V,H]
TERC3 [0,PN,V,H]
[0,0,0,0] = 0x5B
[0,0,0,1] = 0xB5
[0,0,1,0] = 0xD3
[0,0,1,1] = 0xD9
1101010100
1100110010
TMDS-D Ch2Data0
TMDS-D Ch2Data1
TMDS-D Ch2DtaN-1
TMDS-D Ch2DataN
0011001101
0010101010
TMDS-D Ch1Data0
TMDS-D Ch1Data1
TMDS-D Ch1DtaN-1
TMDS-D Ch1DataN
00 = 0010101011
01 = 1101010100
10 = 0010101010
11 = 1101010101
TMDS-D [0,0,V,H]
TMDS-D [0,P0,V,H]
TMDS-D [0,P1,V,H]
TMDS-D [0,PN-1,V,H]
TMDS-D [0,PN,V,H]
0x5B = 0011100101
0xB5 = 0110001101
0xD3 = 0010011101
0xD9 = 0100011101
(Red)
(Green)
(Blue)

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PATENT

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In re Patent Application of

SEUNG HO HWANG, et al.

Application No. 10/036,234

Filed: December 24, 2001

For: **ENCODING METHOD AND SYSTEM FOR REDUCING INTER-SYMBOL INTERFERENCE EFFECTS IN TRANSMISSION OVER A SERIAL LINK**

Group Art Unit: 2614

Examiner: Unknown

LETTER TO OFFICIAL DRAFTSMAN

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GIRARD & EQUITZ LLP Date: 02/13/02

By: Marsha A. Townsend

Marsha A. Townsend

Attn: OFFICIAL DRAFTSMAN
Commissioner for Patents
Washington, D.C. 20231

Sir:

Attached are revised proposed versions of Figs. 2, 3, and 5 in the above-captioned patent application with the proposed changes shown in red ink. Copies of these revised proposed versions of Figs. 2, 3, and 5 have simultaneously been submitted to the Examiner for review and approval. [The proposed change to Fig. 2 is to conform Fig. 2 to the description thereof at page 16, last paragraph of the specification. The proposed change to Fig.3 is to conform Fig. 3 to the description at page 22, last line to page 23, line 3, and page 23, last paragraph of the specification. The proposed change to Fig. 5 is to conform to the description at page 22, lines 11-25 of the specification.]

The Commissioner is hereby authorized to charge payment of any fees associated with this communication or credit any overpayment to Deposit Account No. 50-1697. **A duplicate copy of this sheet is enclosed.**

Respectfully submitted,

GIRARD & EQUITZ LLP

Dated: 2/13/02 By: Alfred A. Equitz

Alfred A. Equitz
Reg. No.30,922

Attorneys for Applicant(s)

Attorney Docket No. SII-1000 [SIMB0115]

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APPLICATION NUMBER	FILING/RECEIPT DATE	FIRST NAMED APPLICANT	ATTORNEY DOCKET NUMBER
10/036,234	12/24/2001	Seung Ho Hwang	SII-1000

CONFIRMATION NO. 6063

FORMALITIES LETTER

OC0000000007434854

Alfred A. Equitz
GIRARD & EQUITZ LLP
Suite 1110
400 Montgomery Street
San Francisco, CA 94104

Date Mailed: 02/07/2002

NOTICE TO FILE MISSING PARTS OF NONPROVISIONAL APPLICATION

FILED UNDER 37 CFR 1.53(b)

Filing Date Granted

An application number and filing date have been accorded to this application. The item(s) indicated below, however, are missing. Applicant is given **TWO MONTHS** from the date of this Notice within which to file all required items and pay any fees required below to avoid abandonment. Extensions of time may be obtained by filing a petition accompanied by the extension fee under the provisions of 37 CFR 1.136(a).

- The oath or declaration is unsigned.
- To avoid abandonment, a late filing fee or oath or declaration surcharge as set forth in 37 CFR 1.16(l) of $130 for a non-small entity, must be submitted with the missing items identified in this letter.
- **The balance due by applicant is $ 130.**

The application is informal since it does not comply with the regulations for the reason(s) indicated below.

The required item(s) identified below must be timely submitted to avoid abandonment:

- Substitute drawings in compliance with 37 CFR 1.84 because:
    - drawing sheets do not have the appropriate margin(s) (see 37 CFR 1.84(g)). Each sheet must include a top margin of at least 2.5 cm. (1 inch), a left side margin of at least 2.5 cm. (1 inch), a right side margin of at least 1.5 cm. (5/8 inch), and a bottom margin of at least 1.0 cm. (3/8 inch);
- An Abstract not to exceed 150 words in length, commencing on a separate sheet (37 CFR 1.72(b)).

A copy of this notice MUST be returned with the reply.

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A

JC887 U.S. PTO
12/24/01

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400 Montgomery Street, Suite 1110, San Francisco, CA 94104
415/433-2250

JC979 U.S. PTO
10/036234
12/24/01

Address to:
Box PATENT APPLICATION
Commissioner for Patents
Washington, D.C. 20231

Attorney's Docket No. SII-1000

First Named Inventor SEUNG HO HWANG

UTILITY PATENT APPLICATION TRANSMITTAL
(under 37 CFR 1.53(b))

SIR:

Transmitted herewith for filing is the patent application entitled:
ENCODING METHOD AND SYSTEM FOR REDUCING INTER-SYMBOL INTERFERENCE EFFECTS IN TRANSMISSION OVER A SERIAL LINK

CERTIFICATION UNDER 37 CFR § 1.10

I hereby certify that this New Application and the documents referred to as enclosed herein are being deposited with the United States Postal Service on this date December 24, 2001 in an envelope bearing "Express Mail Post Office To Addressee" Mailing Label Number EF 246132842 US addressed to: Box PATENT APPLICATION, Assistant Commissioner for Patents, Washington, D.C. 20231.

Jacob S. Zweig _____ J. Zweig
(Name of person mailing paper) (Signature)

Enclosed are:

I. X Transmittal Form (two copies required)

II. The papers required for filing date under CFR § 1.53(b):
i. 44 Pages of specification (including claims and abstract);
ii. 5 Sheets of drawings.
__ formal X informal

III. Declaration or oath

a. X New original - [UNSIGNED]

b. _ Copy from a prior application (37 CFR 1.63(d))
(for continuation/divisional with Item 12 completed)

_ Incorporation By Reference (to be used if Item 3b is checked)

The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Item 3b, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein.

i. __ DELETION OF INVENTOR(S)
Signed statement attached deleting inventor(s) named in the prior application, see 37 CFR 1.63(d)(2) and 1.33(b)

IV. __ Microfiche Computer Program (Appendix, see 37 CFR 1.96)

V. __ Nucleotide and/or Amino Acid Sequence Submission (if applicable, all necessary)

ACCOMPANYING APPLICATION PARTS

VI. _ An assignment of the invention to __ is attached (including Form PTO-1595).

__ The prior application is assigned of record to ;
Assignment recorded in PTO on _, Reel _, Frame(s) _.
__ The prior application is assigned, and the assignment (copy attached) was submitted to PTO for recording on _.
i. __ 37 CFR 3.73(b) Statement (when there is an assignee)

VII. __ Power of Attorney

VIII. __ An Information Disclosure Statement (IDS) is enclosed, including a PTO-1449 and _ references.

IX. __ Preliminary Amendment.

X. X Return Receipt Postcard (MPEP 503 -- should be specifically itemized)

XI. X Other - Request and Certification Under 35 U.S.C. 122(b)(2)(B)(i).

XII. If a CONTINUING APPLICATION, *check appropriate box and supply the requisite information*

_ Continuation
_ Divisional
X Continuation-In-Part (CIP)

of immediately prior application No. **09/954,663**, filed **September 12, 2001**.

i. RELATE BACK - 35 USC 120: If one of the above boxes are checked, please amend the specification by inserting before the first line the sentence: --This is a continuation-in-part of Application No. 09/954,663, filed September 12, 2001.--

[Note to form user: lines for item 12 are intentionally spaced to permit Examiner amendments.]

ii. MAINTENANCE OF COPENDENCY OF PRIOR APPLICATION
(This item must be completed and the necessary papers filed in the prior application if the period set in the prior application has run).
[] A petition, fee and response has been filed to extend the term in the pending prior application until _.

iii. CONDITIONAL PETITIONS FOR EXTENSION OF TIME IN PRIOR APPLICATION
(Complete this item and file conditional petition in prior application if previous item (ii) not applicable).
[] A conditional petition for extension of time is being filed in the pending prior application.

XIII. FOREIGN PRIORITY
[] Priority of application no. _ filed on _ in _ is claimed under 35 USC 119.

XIV. **FEE CALCULATION**

a. _ Amendment changing number of claims or deleting multiple dependencies is enclosed.

b. _ Cancel in this application original Claims _ of the prior application before calculating the filing fee.

CLAIMS AS FILED

	Number Filed	Number Extra	Rate	Basic Fee ($740)
Total Claims	75 – 20	*55	x $18.00	990.00
Independent Claims	4 – 3	*1	x $84.00	84.00
_ Multiple dependent claim(s), if any			$280.00	

*If less than zero, enter "0".

Filing Fee Calculation $1,814.00

50% Filing Fee Reduction (if applicable). . . . . $

XV. Small Entity Status

a. _ A small entity statement is enclosed.

b. _ A small entity statement was filed in the prior nonprovisional application and such status is still proper and desired.

c. _ is no longer claimed.

XVI. Other Fees

_ Recording Assignment [$40.00].....$

_ Other fees

Specify _____ .....$

Total Fees Enclosed.....$1,814.00

XVII. Payment of Fees

X A check in the amount of $1,814.00 is enclosed.

Charge Account No. 50-1697 in the amount of $.

A duplicate of this transmittal is attached.

XVIII. All correspondence regarding this application should be forwarded to the undersigned attorney:

Alfred A. Equitz
GIRARD & EQUITZ LLP
400 Montgomery Street, Suite 1110
San Francisco, CA 94104
Telephone: 415/433-2250
Facsimile: 415/433-2255

XIX. Authorization to Charge Additional Fees

X The Commissioner is hereby authorized to charge any additional fees (or credit any overpayment) associated with this communication and which may be required under 37 CFR § 1.16 or § 1.17 to Account No. 50-1697. **A duplicate of this transmittal is attached**.

GIRARD & EQUITZ LLP

December 24, 2001
(Date)

Attorney Docket No. SII-1000

By: Alfred A Equitz
Alfred A. Equitz
Registration No. 30,922
Attorney(s) or Agent(s) of Record

EXPRESS MAIL

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REQUEST AND CERTIFICATION UNDER 35 U.S.C. 122(b)(2)(B)(i)		
	First Named Inventor	SEUNG HO HWANG
	Title	Encoding Method and System for Reducing Inter-Symbol Interference Effects in Transmission...
	Atty Docket Number	SII-1000

I hereby certify that the invention disclosed in the attached application **has not and will not be** the subject of an application filed in another country, or under a multilateral agreement, that requires publication at eighteen months after filing. I hereby request that the attached application not be published under 35 U.S.C. 122(b).

December 24, 2001
Date

Alfred A Equitz
Signature

Alfred A. Equitz, Reg. No. 30,922
Typed or printed name

This request must be signed in compliance with 37 CFR 1.33(b) and submitted with the application **upon filing.**

Applicant may rescind this nonpublication request at any time. If applicant rescinds a request that an application not be published under 35 U.S.C. 122(b), the application will be scheduled for publication at eighteen months from the earliest claimed filing date for which a benefit is claimed.

If applicant subsequently files an application directed to the invention disclosed in the attached application in another country, or under a multilateral international agreement, that requires publication of applications eighteen months after filing, the applicant **must** notify the United States Patent and Trademark Office of such filing within forty-five (45) days after the date of the filing of such foreign or international application. **Failure to do so will result in abandonment of this application (35 U.S.C. 122(b)(2)(B)(iii)).**

Burden Hour Statement: This collection of information is required by 37 CFR 1 213(a) The information is used by the public to request that an application not be published under 35 U S.C 122(b) (and the PTO to process that request) Confidentiality is governed by 35 U.S C. 122 and 37 CFR 1 14 This form is to take 6 minutes to complete This time will vary depending upon the needs of the individual case. Any comments on the amount of time you are required to complete this form should be sent to the Chief Information Officer, U.S Patent and Trademark Office, Washington, DC 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS SEND TO: Assistant Commissioner for Patents, Washington, DC 20231

ENCODING METHOD AND SYSTEM FOR REDUCING INTER-SYMBOL INTERFERENCE EFFECTS IN TRANSMISSION OVER A SERIAL LINK

CROSS-REFERENCE TO RELATED APPLICATION

This application is a continuation-in-part of pending U.S. Patent Application No. 09/954,663, filed on September 12, 2001, and assigned to the assignee of the present application.

TECHNICAL FIELD OF THE INVENTION

The invention pertains to transmission of encoded data (e.g., one or both of video data and auxiliary data such as audio data) over a serial link, in such a manner as to reduce the bit error rate resulting from inter-symbol interference or other error-causing effects during transmission. In some embodiments, the serial link is a transition minimized differential signaling ("TMDS") link, or a link having some but not all of the characteristics of a TMDS link.

BACKGROUND OF THE INVENTION

Elements of this invention are based upon properties of a serial link. Various serial links for transmitting data and clock signals are well known.

One conventional serial link, used primarily for high-speed transmission of video data from a host processor (e.g., a personal computer) to a monitor, is known as a transition minimized differential signaling interface ("TMDS" link). The characteristics of a TMDS link include the following:

1. video data are encoded and then transmitted as encoded words (each 8-bit word of digital video data is converted to an encoded 10-bit word before transmission);

   a. the encoding determines a set of "in-band" words and a set of "out-of-band" words (the encoder can generate only "in-band" words in response to video data, although it can generate "out-of-band" words in response to control or sync signals. Each in-band word is an encoded word resulting from encoding of one input video data word. All words transmitted over the link that are not in-band words are "out-of-band" words);

b. the encoding of video data is performed such that the in-band words are transition minimized (a sequence of in-band words has a reduced or minimized number of transitions);

c. the encoding of video data is performed such that the in-band words are DC balanced (the encoding prevents each transmitted voltage waveform that is employed to transmit a sequence of in-band words from deviating by more than a predetermined threshold value from a reference potential. Specifically, the tenth bit of each "in-band" word indicates whether eight of the other nine bits thereof have been inverted during the encoding process to correct for an imbalance between running counts of ones and zeroes in the stream of previously encoded data bits);

2. the encoded video data and a video clock signal are transmitted as differential signals (the video clock and encoded video data are transmitted as differential signals over conductor pairs without the presence of a ground line);

3. three conductor pairs are employed to transmit the encoded video, and a fourth conductor pair is employed to transmit the video clock signal; and

4. signal transmission occurs in one direction, from a transmitter (typically associated with a desktop or portable computer, or other host) to a receiver (typically an element of a monitor or other display device).

A use of the TMDS serial link is the "Digital Visual Interface" interface ("DVI" link) adopted by the Digital Display Working Group. It will be described with reference to Fig. 1. A DVI link can be implemented to include two TMDS links (which share a common conductor pair for transmitting a video clock signal) or one TMDS link, as well as additional control lines between the transmitter and receiver. The DVI link of Fig. 1 includes transmitter 1, receiver 3, and the following conductors between the transmitter and receiver: four conductor pairs (Channel 0, Channel 1, and Channel 2 for video data, and Channel C for a video clock signal), Display Data Channel ("DDC") lines for bidirectional communication between the transmitter and a monitor associated with the receiver in accordance with the conventional Display Data Channel standard (the Video Electronics Standard Association's "Display Data Channel Standard," Version 2, Rev. 0, dated April 9, 1996), a Hot Plug Detect (HPD) line (on which the monitor transmits a signal that enables a processor associated with the transmitter to identify the monitor's presence), Analog lines (for transmitting analog video to the receiver), and Power lines (for providing DC power to the receiver and a monitor

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associated with the receiver). The Display Data Channel standard specifies a protocol for bidirectional communication between a transmitter and a monitor associated with a receiver, including transmission by the monitor of an Extended Display Identification ("EDID") message that specifies various characteristics of the monitor, and transmission by the transmitter of control signals for the monitor. Transmitter 1 includes three identical encoder/serializer units (units 2, 4, and 6) and additional circuitry (not shown). Receiver 3 includes three identical recovery/decoder units (units 8, 10, and 12) and inter-channel alignment circuitry 14 connected as shown, and additional circuitry (not shown).

As shown in Fig. 1, circuit 2 encodes the data to be transmitted over Channel 0, and serializes the encoded bits. Similarly, circuit 4 encodes the data to be transmitted over Channel 1 (and serializes the encoded bits), and circuit 6 encodes the data to be transmitted over Channel 2 (and serializes the encoded bits). Each of circuits 2, 4, and 6 responds to a control signal (an active high binary control signal referred to as a "data enable" or "DE" signal) by selectively encoding either digital video words (in response to DE having a high value) or a control or synchronization signal pair (in response to DE having a low value). Each of encoders 2, 4, and 6 receives a different pair of control or synchronization signals: encoder 2 receives horizontal and vertical synchronization signals (HSYNC and VSYNC); encoder 4 receives control bits CTL0 and CTL1; and encoder 6 receives control bits CTL2 and CTL3. Thus, each of encoders 2, 4, and 6 generates in-band words indicative of video data (in response to DE having a high value), encoder 2 generates out-of-band words indicative of the values of HSYNC and VSYNC (in response to DE having a low value), encoder 4 generates out-of-band words indicative of the values of CTL0 and CTL1 (in response to DE having a low value), and encoder 6 generates out-of-band words indicative of the values of CTL2 and CTL3 (in response to DE having a low value). In response to DE having a low value, each of encoders 4 and 6 generates one of four specific out-of-band words indicative of the values 00, 01, 10, or 11, respectively, of control bits CTL0 and CTL1 (or CTL2 and CTL3).

It has been proposed to encrypt video data transmitted over a serial link. For example, it has been proposed to use a cryptographic protocol known as "High-bandwidth Digital Content Protection" ("HDCP") to encrypt digital video to be transmitted over a DVI link and to decrypt the data at the DVI receiver. A DVI transmitter implementing HDCP outputs a 24-bit bus, known as *cout*[23:0], during the

video active period (i.e. when DE is high). This 24-bit *cout* data is "Exclusive Ored" (in logic circuitry in the transmitter) with the 24-bit RGB video data input to the transmitter in order to encrypt the video data. The encrypted data is then encoded (according to the TMDS standard) for transmission. The same *cout* data is also generated in the receiver. After the encoded and encrypted data received at the receiver undergoes TMDS decoding, the *cout* data is processed together with the decoded video in logic circuitry in order to decrypt the decoded data and recover the original input video data.

Before the transmitter begins to transmit HDCP encrypted, encoded video data, the transmitter and receiver communicate bidirectionally with each other to execute an authentication protocol (to verify that the receiver is authorized to receive protected content, and to establish shared secret values for use in encryption of input data and decryption of transmitted encrypted data). After the receiver has been authenticated, the transmitter calculates the initial set of encryption keys (for encrypting the first line of input video data) in response to a control signal and sends the control signal to the receiver (during each vertical blanking period, when DE is low) to cause the receiver to calculate an initial set of decryption keys (for decrypting the first received and decoded line of transmitted video data). Following generation of the initial set of encryption/decryption keys, each of the transmitter and receiver performs a re-keying operation during each blanking (vertical or horizontal) interval to generate a new set of keys for encrypting (or decrypting) the next line of video data, and actual encryption of input video data (or decryption of received, decoded video data) is performed using the latest set of keys only when DE is high (not during the blanking intervals).

Each of the transmitter and receiver includes an HDCP cipher circuit (sometimes referred to herein as an "HDCP cipher") including a linear feedback shift register (LFSR) module, a block module coupled to the output of the LFSR module, and an output module coupled to an output of the block module. The LFSR module is employed to re-key the block module in response to each assertion of an enable signal, using a session key (*Ks*) and frame key (*Ki*). The block module generates (and provides to the LFSR module) the key *Ks* at the start of a session and generates (and applies to the LFMS module) a new value of key *Ki* at the start of each frame of video data (in response to a rising edge of a control signal which occurs in the first vertical blanking interval of a frame).

The block module comprises two halves, known as "Round Function K" and "Round Function B." Round Function K includes 28-bit registers Kx, Ky, and Kz, seven S-Boxes (each a 4 input bit by 4 output bit S-Box including a look-up table), and a linear transformation unit K. Round Function B includes 28-bit registers Bx, By, and Bz, seven S-Boxes (each a 4 input bit by 4 output bit S-Box including a look-up table), and a linear transformation unit B. Round Function K and Round Function B are similar in design, but Round Function K performs one round of a block cipher per clock cycle to assert (to the output module) a different pair of 28-bit round keys (*Ky* and *Kz*) each clock cycle in response to the output of the LFSR module, and Round Function B performs one round of a block cipher per clock cycle, in response to each 28-bit round key *Ky* from Round Function K and the output of the LFSR module, to assert (to the output module) a different pair of 28-bit round keys (*By* and *Bz*) each clock cycle. The transmitter generates value *An* at the start of the authentication protocol and the receiver responds to it during the authentication procedure. The value *An* is used to randomize the session key. The block module operates in response to the authentication value (*An*) and an initialization value (*Mi*, also referred to as an integrity verification key) which is updated by the output module at the start of each frame.

Each of linear transformation units K and B outputs 56 bits per clock cycle. These output bits are the combined outputs of eight diffusion networks in each transformation unit. Each diffusion network of linear transformation unit K produces seven output bits in response to seven of the current output bits of registers Ky and Kz. Each of four of the diffusion networks of linear transformation unit B produces seven output bits in response to seven of the current output bits of registers By, Bz, and Ky, and each of the four other diffusion networks of linear transformation unit B produces seven output bits in response to seven of the current output bits of registers By and Bz.

The output module performs a compression operation on the 28-bit keys (*By*, *Bz*, *Ky* and *Kz*) asserted to it (a total of 112 bits) by the block module during each clock cycle, to generate one 24-bit block of pseudo-random bits *cout[23:0]* per clock cycle. Each of the 24 output bits of the output module consists of the exclusive OR ("XOR") of nine terms.

In the transmitter, logic circuitry receives each 24-bit block of *cout* data and each input 24-bit RGB video data word, and performs a bitwise XOR operation thereon in order to encrypt the video data, thereby generating a word of encrypted RGB video data. Typically, the encrypted data subsequently undergoes TMDS encoding before it

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is transmitted to a receiver. In the receiver, logic circuitry receives each 24-bit block of *cout* data and each recovered 24-bit RGB video data word (after the recovered data has undergone TMDS decoding), and performs a bitwise XOR operation thereon in order to decrypt the recovered video data.

Throughout the specification the expression "TMDS-like link" will sometimes be used to denote a serial link capable of transmitting encoded data (e.g., encoded digital video data) and a clock for the encoded data, from a transmitter to a receiver, and optionally also capable of transmitting (bidirectionally or unidirectionally) one or more additional signals (e.g., encoded digital audio data or other encoded data) between the transmitter and receiver, that is or includes either a TMDS link or a link having some but not all of the characteristics of a TMDS link. There are several conventional TMDS-like links.

Some TMDS-like links encode input video data (and other data) to be transmitted into encoded words comprising more bits than the incoming data using a coding algorithm other than the specific algorithm used in a TMDS link, and transmit the encoded video data as in-band characters and the other encoded data as out-of-band characters. The characters need not be classified as in-band or out-of-band characters based according to whether they satisfy transition minimization and DC balance criteria. Rather, other classification criteria could be used. An example of an encoding algorithm, other than that used in a TMDS link but which could be used in a TMDS-like link, is IBM 8b10b coding. The classification (between in-band and out-of-band characters) need not be based on just a high or low number of transitions. For example, the number of transitions of each of the in-band and out-of-band characters could (in some embodiments) be in a single range (e.g., a middle range defined by a minimum and a maximum number of transitions).

The data transmitted between the transmitter and receiver of a TMDS-like link can, but need not, be transmitted differentially (over a pair of conductors). Also, although a TMDS link has four differential pairs (in the single pixel version), three for video data and the other for a video clock, a TMDS-like link could have a different number of conductors or conductor pairs.

Typically, the primary data transmitted by a TMDS link are video data. What is often significant about this is that the video data are not continuous, and instead have blanking intervals. These blanking intervals provide an opportunity (exploited in some embodiments of the present invention) for auxiliary data to be transported, and they

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represent unused bandwidth. However, many serial links do not transmit data having blanking intervals, and thus do not encode input data (for transmission) in response to a data enable signal. For example, audio serial links would typically transmit continuous data.

The expression "auxiliary data" is used in a broad sense herein to denote digital audio data or any other type of data other than video data and timing information for video data (e.g., a video clock). For example, timing information for audio data (e.g., a clock for recovering transmitted audio data) falls within the scope of "auxiliary data." Other examples of "auxiliary data" transmitted in accordance with the invention include computer keyboard signals, still image data (generated by a camera, for example), text data, control signals for a power supply, picture in picture data, monitor control information (audio volume, brightness, power state), control signals for indicator lights on a monitor or keyboard, non-audio or video control information, etc.

The term "stream" of data, as used herein, denotes that all the data are of the same type and is transmitted with the same clock frequency. The term "channel," as used herein, refers to that portion of a serial link that is employed to transmit data (e.g., a particular conductor or conductor pair between the transmitter and receiver over which the data are transmitted, and specific circuitry within the transmitter and/or receiver used for transmitting and/or recovery of the data) and to the technique employed to transmit the data over the link. Because it is desirable to transmit many different streams of auxiliary data in important applications of the invention, preferred embodiments of the invention provide multiple channels for transmission of auxiliary data, including channels for transmission of auxiliary data in both directions over the link (that is, with and against the direction of the video data). In some implementations, a channel is employed to transmit one stream of auxiliary data. In other implementations, a channel is employed to transmit more than one stream of auxiliary data. In some embodiments of the invention, two (or more than two) streams of serial video data are transmitted (over one, two, or more than two channels), and either one, two, or more than two streams of serial auxiliary data are also transmitted.

U.S. Patent 5,999,571, issued December 7, 1999, teaches (e.g., at col. 5) that, when the code words (indicative of video data) transmitted over a TMDS link are transition minimized words (a first subset of a set of code words), synchronization words (distinguishable from the transition minimized code words) can be transmitted over the link during "preamble" periods in which encoded video data are not

transmitted. The synchronization words can be transition maximized words that are members of a second subset (disjoint from the first subset) of the set of code words. U.S. 5,999,571 teaches that several (e.g., three) repetitions of a synchronization word should be transmitted consecutively, to allow the decoder (in the receiver) rapidly and accurately to identify a specific transition (e.g., the leading edge) of one of the synchronization words and thus to accomplish synchronization with the encoder (in the transmitter.

U.S. Patent 6,151,334, issued November 21, 2000, teaches transmission (over a TMDS link) of several different types of encoded control words, each distinguishable from transition minimized code words indicative of data. At least some of the control words can be transition maximized words. One of the control words is a "data stream separation" word that is transmitted before or after a burst of data and is indicative of the start or end of a burst and the type of data transmitted during the burst. Another one of the control words is an "isochronous data transfer" word that is a synchronization character typically transmitted at the beginning or end of a blanking interval and indicates the type of the blanking interval (e.g., horizontal or vertical) and distinguishes between the beginning and the end of the blanking interval. For example, a first isochronous data transfer word indicates the start of a vertical blanking interval, a first data stream separation word then indicates the start of a burst of data in the vertical blanking interval, a second data stream separation word then indicates the end of such data burst, and a second isochronous data transfer word then indicates the end of the vertical blanking interval. Each of the first isochronous data transfer word, the first data stream separation word, the second data stream separation word, and the second isochronous data transfer word is a transition maximized code word, a transition minimized code word can indicate each word of data of the data burst (transmitted in the vertical blanking interval), and the vertical blanking interval can be followed by an active video period comprising a third data stream separation word (indicative of the start of a stream of video data) followed by a stream of transition minimized code words indicative of the video data itself.

SUMMARY OF THE INVENTION

In a class of embodiments, the invention is a communication system including a transmitter, a receiver, and a serial link (which can but need not be a TMDS or TMDS-like link), in which encoded data (e.g., encoded video data and optionally also encoded

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auxiliary data) are transmitted from the transmitter to the receiver. The serial link can but need not be a TMDS or TMDS-like link. In typical embodiments, alternating bursts of encoded video data and encoded auxiliary data are transmitted over each of one or more channels of the link. Other aspects of the invention are transmitters for use in encoding data for transmission over a serial link, and methods for sending encoded data over a serial link.

In accordance with the invention, the data to be transmitted are encoded using a subset (a "robust" subset) of a full set of code words. Typically, the code words in the full set have equal length (e.g., each consists of N bits). The robust subset will sometimes be referred to herein as a "selected" (or "inventive") set of code words, and the code words in the robust subset will sometimes referred to as the "inventive" code words. The robust subset is selected such that each stream of encoded data (comprising only inventive code words) transmitted over a serial link has a bit pattern that is less susceptible to inter-symbol interference ("ISI") during transmission than is the bit pattern determined by a transmitted, conventionally encoded version of the same data (comprising not only inventive code words but also members of the full set that are not inventive code words). Since the inventive code words are a subset of the full code word set and each inventive code word determines one source data word, the bit rate at which source data can be transmitted over the link is lower if the transmitted data are encoded using only the inventive code words than if the transmitted data are encoded conventionally using the full code word set. This is because, in general, a set of source data bits can be grouped into a fewer number of longer source data words (each different source data word to be encoded as a different L-bit code word) when more different L-bit code words are available for encoding the source data.

In general, the best choice for the particular inventive code word set selected from a full set of binary code words depends on the particular coding implemented by the full set (i.e., the details of which bits of each code word in the full set are zeroes and which are ones). In preferred embodiments, the inventive code words are selected to be those whose serial patterns (during transmission) have fewer contiguous zeros and ones (e.g., on the average), and thus are less susceptible to ISI during transmission, than do those code words in the full set that are not selected (e.g., the average number of contiguous zeros and ones, per code word, of the inventive code words is less than the average number of contiguous zeros and ones, per code word, of the code words in the full set that are not selected as the inventive code words). Also, when the bits of

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the inventive code words are transmitted over a serial link as sequences of rising and falling voltage transitions, the bit pattern of each transmitted stream of the inventive code words preferably implements DC balancing (the voltage drift over time is limited).

Typically, the full set comprises 2^N binary code words (each having a length of L bits) and thus can be efficiently used to encode data words of N-bit length for transmission. Also typically, the robust subset comprises 2^M of these code words (each having a length of L bits), where $M < N$, and thus can be efficiently used to encode data words of M-bit length for transmission. In this case, in order to encode N-bit source words using the inventive code words, the N-bit source words can be buffered and packed into M-bit format. Each resulting M-bit source word can then be encoded (as an L-bit encoded word) using one of the inventive code words. Assuming that the same time is required to transmit and decode each L-bit encoded word (regardless of whether the word is a member of the robust subset), fewer source data bits can be transmitted per unit time when the source words are encoded using the inventive code words than when the source words are conventionally encoded using the full code word set. For example, to encode 8-bit source data words, the full code word set can be the set of 10-bit code words employed in a conventional TMDS link (each such code word comprising one of 256, transition-minimized, 9-bit patterns whose most significant bit indicates that the pattern is transition-minimized, concatenated with a tenth bit indicating whether the eight least-significant bits have or have not been inverted in accordance with a DC balancing algorithm). In some embodiments, the robust subset consists of sixteen selected 10-bit code words of this full set, and the nine least-significant bits of each code word in the robust subset are indicative of a different one of the 256, transition-minimized, 9-bit patterns. Thus, to encode the 8-bit source words using only the sixteen inventive code words, each 8-bit source word is split into two 4-bit portions and each 4-bit portion separately encoded as one of the inventive 10-bit code words. Thus, the rate at which the 8-bit source data can be transmitted (after being encoded using only the inventive code words) is only half the rate at which the same data can be transmitted after being encoded conventionally using the full code word set. However, the conventionally encoded data would be subject to higher rates of error (e.g., error due to ISI) during transmission than would the same data if transmitted after being encoded using only the inventive code words.

Attorney Docket No. P18525

In general, by reducing the ratio of M to N in the example (in which the robust subset comprises 2^M code words), lower bit-error rates (BER) can be achieved in accordance with the invention at the cost of reducing the rate at which the source data can be transmitted. Conversely, increasing the ratio of M to N results in an increased source data transmission rate at the cost of a higher BER.

Encoding of data in accordance with the invention is particularly beneficial in applications in which encoded data are to be transmitted over very long conductors or under other conditions in which there would otherwise be a high risk of error due to ISI during transmission.

In some embodiments of the invention, encoded data are transmitted in bursts over the serial link, and at least one of the inventive code words is used as a "guard band" word that is transmitted at the start or end (or the start and end) of a burst of encoded data (to identify the leading and/or trailing edge of the burst) or at the start or end (or at the start and end) of each burst of encoded data of a specific type. In some such embodiments, two different guard band words are used: one for transmission at the start of each encoded data burst (to identify the leading edge of the burst); the other for transmission at the end of each encoded data burst (to identify the trailing edge of the burst). In preferred embodiments, bursts of at least two different types of encoded data (e.g., audio data or other auxiliary data, and video data) are transmitted over the serial link and P different ones (where P is greater than or equal to 2) of the inventive code words are used as P different guard band words, including: one guard band word for transmission at the start of each burst of encoded data of a first type (to identify the leading edge of such burst); and another guard band word for transmission at the start of each burst of encoded data of a second type (to identify the leading edge of such burst). For example, in some embodiments bursts of encoded video data (each identified by a first guard band word) are transmitted during active video periods, and bursts of auxiliary data (each identified by a second guard band word) are transmitted during blanking intervals between the active video periods.

In a class of systems that embody the invention, 8-bit video data words (each encoded according to the TMDS encoding algorithm as a 10-bit code word) are transmitted over a TMDS link (or other TMDS-like link having multiple channels for transmitting serial video) during active video periods in which a control signal (DE) is high, and control words (each indicative of two bits: CTL0 and CTL1, or CTL2 and CTL3) or synchronization words (each indicative of two bits: HSYNC and VSYNC)

Attorney Docket No. 15436-1250

are transmitted over each of at least some of the video transmission channels during blanking intervals (in which DE is low) between the active video periods. The system is operable in a mode in which each transmitted video data word is conventionally encoded as a transition-minimized, 10-bit TMDS code word. Each such transition-minimized code word determines one of 256 different nine-bit patterns, having a most significant bit indicating that the pattern is transition-minimized, concatenated with a tenth bit indicating whether the eight least-significant bits of the nine-bit pattern have or have not been inverted in accordance with a DC balancing algorithm. Each transmitted control word (CTL1:CTL0 or CTL3:CTL2) and synchronization word (HSYNC:VSYNC) is a distinctive, 10-bit, transition-maximized word. In preferred embodiments, 4-bit words of auxiliary data (encoded in accordance with the invention) are transmitted during the blanking intervals at times when no control words or synchronization words are transmitted. The auxiliary data are typically but not necessarily audio data. In other embodiments, the system is operable in a mode in which 4-bit words of video data (encoded in accordance with the invention) are transmitted during the active video periods. To provide at least one guard band word, and for use in encoding auxiliary data in accordance with the invention for transmission in blanking intervals between active video periods, a robust subset of 17 different, transition-minimized code words is selected from the full conventional TMDS code space: sixteen 10-bit code words (each indicative of a different 4-bit auxiliary data word, and one of which is optionally also used as a guard band word at the start and end of each burst of encoded auxiliary data); and one 10-bit code word used as a guard band word (at the start and end of each active video period). Alternatively, a robust subset of 18 different, transition-minimized code words is selected from the full conventional TMDS code space: sixteen 10-bit code words (each indicative of a different 4-bit source word); and two 10-bit code words (each used as a guard band word).

In some embodiments of the invention, bursts of encoded auxiliary data and bursts of encoded video data are transmitted over a serial link, and the auxiliary data are encoded in accordance with the invention using a set of inventive code words. The set of inventive code words includes a "video" guard band word that is transmitted at the start of each encoded video data burst, and an "auxiliary" guard band word that is transmitted at the start of each encoded auxiliary data burst. In some implementations, at least one of the guard band words is also used for a second purpose: to encode

auxiliary data. In preferred implementations of such embodiments, the encoded video data are transmitted during active video periods in which a control signal, DE, is high (DE = 1), and encoded control (or synchronization) signals and encoded auxiliary data are transmitted during blanking intervals (in which DE = 0) between active video periods. At least one video guard band word is transmitted at the start of each active video period. Each blanking interval comprises at least one auxiliary data period (each comprising at least one auxiliary guard band word followed by a burst of encoded auxiliary data), a preamble period (or "front porch") between the falling edge of DE (at the start of the blanking interval) and the start of the first (or only) auxiliary data period (and optionally also an additional front porch before each subsequent auxiliary data period in the blanking interval), and a final period (a "back porch") between the last auxiliary data period and the next active video period. Control (or sync) signals of a specific type are transmitted during each front porch. Control signals of another specific type are transmitted in the back porch.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a block diagram of a conventional system including a Digital Visual Interface ("DVI") link.

Fig. 2 is a block diagram of a first embodiment of the inventive system.

Fig. 3 is a table showing data patterns transmitted in "front porch" and "back porch" portions of a blanking interval, and the inventive guard band code words transmitted after such front porch and back porch portions, in a preferred embodiment of the invention.

Fig. 4 is a table showing a set of seventeen of the inventive code words (including one guard band word) employed in a preferred embodiment of the invention.

Fig. 5 is a timing diagram of signals input to the transmitter during a video blanking interval of an embodiment of the inventive system, and encoded signals transmitted over a TMDS link of such system in response thereto.

Fig. 6 is a timing diagram of signals input to the transmitter during the back porch portion of a video blanking interval (and during a subsequent active video period) of an embodiment of the inventive system, and encoded signals transmitted over a TMDS link of such system in response thereto.

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DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

During transmission of data over a serial link from a transmitter to a receiver, inter-symbol interference ("ISI") can give rise to errors that cause the received data to differ from the transmitted data. The rate at which such errors occur depends on such factors as the channel medium, and when the data are patterns of binary bits, the particular bit patterns that are transmitted. In accordance with the invention, data are encoded for transmission over a serial link with bit patterns that are less susceptible to ISI during transmission over the link than are the patterns determined by conventionally encoded versions of the same data. Thus, the data are transmitted more reliably in accordance with the invention, and with reduced error rate, than are conventionally encoded versions of the same data. More specifically, data are encoded in accordance with the invention using a subset (a "robust" subset) of a full set of code words. Typically, the code words in the full set have equal length (e.g., each consists of N bits). The robust subset will sometimes be referred to herein as a "selected" or "inventive" set of code words, and the code words in the robust subset will sometimes referred to as the "inventive" code words. The robust subset is selected such that each transmitted stream of encoded data (coded using only members of the inventive code word set) has patterns that are less susceptible to ISI during transmission over the serial link than are patterns determined by a transmitted, conventionally encoded version of the same data (that has been coded using code words of the full set other than members of the inventive code word set, as well as members of the inventive code word set). Since there are more code words in the full set than there are inventive code words, fewer words of data can be transmitted over the link per unit time if the transmitted data are encoded using only the inventive code words than if the transmitted data are encoded conventionally using the full set of code words.

Encoding of data in accordance with the invention is particularly beneficial in applications in which the encoded data are transmitted over very long conductors or under other conditions in which there would otherwise be a high risk of error due to ISI during transmission.

It should be appreciated that the term "transmitter" is used herein in a broad sense to denote any unit capable of encoding data and transmitting the encoded data over a serial link (and optionally also encrypting the data to be transmitted), and the term "receiver" is used herein in a broad sense to denote any unit capable of receiving data and decoding that has been transmitted over a serial link (and optionally also

decrypting the received data). For example, the term transmitter can denote a transceiver that performs the functions of a receiver as well as the functions of a transmitter. In a more specific example, the term transmitter (with reference to a unit that transmits non-audio auxiliary data over a TMDS-like link or other serial link) can denote a transceiver that is configured to receive video data and audio data over the link and to transmit the non-audio auxiliary data over the link.

As noted above, the term "stream" of data (as used herein) denotes that all the data are of the same type and are transmitted with the same clock frequency, and the term "channel" (as used herein) refers to that portion of a serial link that is employed to transmit data (e.g., a particular conductor or conductor pair between the transmitter and receiver over which the data are transmitted, and specific circuitry within the transmitter and/or receiver used for transmitting and/or recovery of the data) and to the technique employed to transmit the data over the link.

When transmitting audio (or other auxiliary) data via a serial link, is it often desired to transmit multiple streams of the auxiliary data, and it is often valuable for multiple channels of the link to be available for transmission of the auxiliary data. For example, there can be two audio streams (left and right streams of stereo audio), six streams (e.g., those of "5.1" surround sound), or up to eight streams (e.g., those of "7.1" surround sound). Alternatively, it may be desired to transmit even more streams of audio data with video, or to transmit streams of non-audio auxiliary data (for providing non-audio effects that are synchronized to the video) with audio and video. All such streams of auxiliary data are typically on the same time base, but alternatively there can be a need for some of the audio (or other auxiliary) data to be based upon another time base, or to have a different sampling rate. For example transmission of six streams of pulse code modulated (PCM) audio data over the link can be based upon one clock. Another two streams of compressed audio data, possibly a down-mix (for playback on a reduced number of speakers), might be transmitted with the video and PCM data as well.

In high-speed serial digital data transmission the data are often encoded to maximize or minimize the number of transitions and to also balance the DC level. For example, in systems including at least one of the above-referenced TMDS links, transition-minimized, DC-balanced, TMDS encoded video data are transmitted over each of three channels of at least one TMDS link, and encoded auxiliary data (e.g., audio data) can be transmitted over one or more of these three channels during blanking

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intervals between the active video periods. When the bandwidth requirement of the auxiliary data is lower than that of the primary data (video data) and the auxiliary data channel has significant ISI (which can result from a long cable), then the auxiliary data are desirably encoded using the inventive encoding scheme to achieve a lower bit-error rate during transmission.

In a class of preferred embodiments, auxiliary data are encoded in accordance with the invention (for transmission over a TMDS link) using a subset of the transition-minimized TMDS code words that are conventionally used to encode video data for transmission over the link. These and/or other embodiments of the invention can be implemented by a system of a type to be described with reference to Fig. 2. The Fig. 2 system is identical to that of Fig. 1, except in that it is configured to encode auxiliary data (or other auxiliary data) in accordance with the invention (and also to encode video data in the same conventional manner as in the Fig. 1 system), transmit the encoded data over one or more of Channel 0, Channel 1, and Channel 2 (and also to transmit encoded video data over each such channel), and decode the encoded auxiliary data (as well as the encoded video data). Transmitter 1' and receiver 2' of Fig. 2 correspond, respectively, to transmitter 1 and receiver 3 of Fig. 1 (but perform auxiliary data encoding, transmission, and decoding functions that are not performed by transmitter 1 and receiver 3 of Fig. 1). The TMDS link between transmitters 1' and 2' in Fig. 2 is identical to the TMDS link between transmitters 1 and 3 in Fig. 1, although some of the conductors thereof are shown in Fig. 1 but not in Fig. 2 (for simplicity).

The Fig. 2 system preferably transmits a video clock over a conductor pair (labeled "Channel C in Fig. 2) of the TMDS link, and also transmits a clock for the auxiliary data over at least one channel of the link. For example, transmitter 1' transmits video data to receiver 2' over Channels 0, 1, and 2 (which are identical to the identically numbered channels of the Fig. 1 system) except during video blanking intervals, transmits two streams of audio data (e.g., left and right stereo signals) over any two of Channels 0, 1, and 2 to receiver 2' during the video blanking intervals, continuously transmits a video clock (e.g., determined by the rising edges of a binary waveform) over Channel C, and transmits time stamp data with each burst of the audio data. The time stamp data determine a clock for the audio data, as described in above-cited U.S. Patent Application No. 09/954,663, filed on September 12, 2001. Receiver 2' is configured to process the time stamp data to recover the audio clock employed to transmit the audio data.

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Typically the clock for a stream of audio data has a much lower frequency than the pixel clock for a stream of video. However, in most applications the audio clock needs to be more accurate than the pixel clock, to reduce jitter. This is true since distortion in analog audio (that has been generated from digital audio data having jitter) is more easily discernible (to one experiencing the analog audio) than is the distortion in a displayed video program generated from digital video having the same amount of jitter.

In the Fig. 2 system, 8-bit source words of video data are encoded into 10-bit code words which are then serialized and transmitted over a channel medium (one of the conductor pairs identified as Channels 0, 1, and 2). In receiver 2', each 10-bit code word is decoded back to the original 8-bit word if no errors are present. Each code word comprises a 9-bit base pattern (a transition-minimized member of a set of 2^9 nine-bit patterns, whose most significant bit indicates that the base pattern is transition-minimized, concatenated with a tenth bit indicating whether the eight least-significant bits of the base pattern have or have not been inverted in accordance with a DC balancing algorithm). In transmitter 1', each 8-bit source word is first encoded to one of the 9-bit base patterns, and a stream of the 9-bit base patterns are then encoded as a stream of the 10-bit code words (in a manner that achieves improved DC balancing of the transmitted stream of 10-bit code words). However, the decoded video data can include errors (especially when the relevant channel has significant ISI), depending on the specific channel media and the specific data patterns of the transmitted serial bit stream.

If transmitter 1' and receiver 2' were operated to encode and decode the auxiliary data in the same way that they encode and decode the video data, and to send both types of encoded data over the same channel of the serial link, the decoded auxiliary data would be subject to error at the same error rate. This error rate can be unacceptably high for auxiliary data (especially when the auxiliary data are audio data), even if it is acceptable for video data. To reduce the error rate for the auxiliary data, transmitter 1' can be configured to encode the auxiliary data in accordance with the invention. Optionally, transmitter 1' can be configured also to encode the video data in accordance with the invention (or to be operable in a mode in which it encodes both the video data and auxiliary data in accordance with the invention). However, since data encoded in accordance with the invention (with a robust subset of a "full set" of code words) necessarily has a lower data transmission rate than the same data

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encoded in a conventional manner (using the same "full set" of code words, assuming that both streams of encoded bits are transmitted with the same clock frequency). In many applications, video data cannot practically be transmitted at an adequate rate if encoded in accordance with the invention. Thus, typical implementations of the Fig. 2 system will encode auxiliary data (but not video data) in accordance with the invention.

In a class of embodiments, transmitter 1' is configured to encode the auxiliary data in accordance with the invention as follows. A subset of the full set of 10-bit TMDS code words is selected as the "inventive" code word set such that each transmitted stream of 10-bit words of encoded auxiliary data (consisting only of the inventive code words) has a pattern that is less susceptible to inter-symbol interference than is the pattern determined by a transmitted stream of a TMDS-encoded version of the same data (including not only inventive code words but also members of the full set that are not inventive code words).

In some embodiments, a 2^M–bit subset (where $M < 8$) of the full set of 10-bit TMDS code words is selected to be the inventive code word set. Optionally, the inventive code word set also includes one or more code words of the full set that are used as guard band words. The 17 inventive code words (each comprising 10 bits) to be described below with reference to Figs. 3 and 4 are an example of such a 2^M–bit subset (where $M = 4$) supplemented by one additional guard band word. Receiver 2' is implemented to decode each received one of the inventive 10-bit code words as an auxiliary data word of length M bits. Receiver 2' performs the same decoding operations on the encoded auxiliary words received during blanking intervals that it performs on the conventionally encoded video words received during the active video periods. However, during the encoding of source auxiliary data (using the inventive code words), transmitter 1' does not perform the conventional DC balancing steps that it performs during its conventional encoding of source video data (in which the eight least significant bits of the "N+1"th encoded video word are inverted, and the resulting nine bits are concatenated with a distinctive tenth, most significant bit when the cumulative DC drift of the N previous encoded video words reaches a predetermined threshold, and otherwise does not invert the eight least significant bits of the "N+1"th encoded video word and instead concatenates the word with another distinctive, tenth, most significant bit). Rather, transmitter 1' is configured simply to replace each 4-bit source word of auxiliary data with the corresponding one of the inventive code words, regardless of the cumulative DC drift of the resulting stream of inventive code words

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(and regardless of whether the MSB of the inventive code word is a one or zero). The inventive code words are preferably chosen so that when the bits of a stream of the inventive code words are transmitted over a serial link as sequence of rising and falling voltage transitions, the bit pattern of such stream of the inventive code words is DC balanced (or is likely to be DC balanced) in the sense that the voltage drift that it determines over time is limited to an acceptable amount.

In other embodiments, transmitter 1' does perform the same DC balancing steps during its encoding of source auxiliary data (using the inventive code words) and during its conventional encoding of source video data. This is taken into consideration in the selection of the inventive code word set. Specifically, each code word of the inventive code word set has a 9-bit base pattern that is a member of a selected subset of the 9-bit base pattern space of the full set of 10-bit TMDS code words, and during encoding of 4-bit words of source auxiliary data (to replace them with the inventive 10-bit code words), the eight least-significant bits of this 9-bit base pattern are either inverted and the resulting pattern concatenated with a tenth (and most significant) bit having a first value, or the base pattern is not inverted and is instead concatenated with a tenth (and most significant) bit having a second value, depending on whether the cumulative DC drift of the stream of previously encoded auxiliary words has reached a predetermined threshold. In these embodiments, receiver 2' is implemented to perform the same decoding operations on the encoded auxiliary data words received during blanking intervals that it performs on the conventionally encoded video data words received during the active video periods, and then to map each 8-bit word (generated as a result of conventional decoding of one of the 10-bit encoded auxiliary data words) to one of the 2^M auxiliary data words each having M-bit length.

In the described embodiments of the Fig. 2 system, the size of the auxiliary data encoding space (the number of different auxiliary data words that can be encoded with the inventive code word set) is reduced from 2^8 (= 256) to 2^M (where $M < 8$) in accordance with the invention, and thus the effective rate at which the auxiliary data (encoded in accordance with the invention) can be transmitted is reduced from 8 bits per clock period per channel to M bits per clock period per channel. By reducing the value M (i.e., selecting a smaller inventive set of code words from the full set), a lower bit-error rate (BER) can be achieved but the data rate will also be reduced. Conversely, increasing the parameter M results in an increased data rate but at the cost of increased BER.

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We next describe an embodiment of the inventive code word set with reference to Figs. 3 and 4. This code word set is a subset of the full set of conventional TMDS 10-bit code words, and is useful for encoding 4-bit words of auxiliary data for transmission over a TMDS (or TMDS-like) link over which 8-bit video words (conventionally encoded using the full set of TMDS 10-bit code words) are also transmitted, in cases when it is adequate to transmit the auxiliary data at half the data rate as the video data. Typically, 8-bit input words of binary auxiliary data are buffered, the four least-significant bits of each are encoded (e.g., in transmitter 1' of Fig. 2) as one of the sixteen 8-bit words "AD0-AD15" in the left column (labeled "Input D7-D0") of Fig. 4, and the four most significant bits of each 8-bit input word are also encoded as the appropriate one of the sixteen 8-bit words AD0-AD15. Each of the words AD0-AD15 has the hexadecimal representation shown in the center column of Fig. 4. Each of the words AD0-AD15 is then encoded (e.g., in transmitter 1') as the corresponding one of the 10-bit patterns shown in the right column of Fig. 4.

In Fig. 4 (and Fig. 3), the left bit of each code word is the LSB and (in the case of each 10-bit code word) is the first bit to be transmitted over the serial link. Also, the right bit of each code word is the MSB and (in the case of each 10-bit code word) is the last bit to be transmitted over the serial link.

For example, an input auxiliary data word 10000000 (whose LSB is 1) would be split into two halves (1000 and 0000) and the two halves then encoded as AD1 and AD0, respectively. Then, the 8-bit word AD0 is encoded as the 10-bit inventive word "0011100101" and the 8-bit word AD1 is encoded as the 10-bit inventive word "0110001101." The two inventive words would then be serialized transmitted over the serial link sequentially, with the bits "0011100101" indicative of the "most significant" half (0000) of the input word being transmitted before the bits "0110001101" that are indicative of the least significant half (1000) of the input word. At the receiver, each 10-bit inventive word is decoded into one of the 8-bit words AD0-AD15, and the original 8-bit input auxiliary data words can be reconstructed from the recovered words AD0-AD15 since there is a one-to-one mapping between each word AD0-AD15 and one half (four bits) of each 8-bit input auxiliary data word.

Of course, the input auxiliary data asserted to the transmitter (e.g., transmitter 1') can be 4-bit words, in which case the transmitter would not need to split (or otherwise pack) received input auxiliary data words into 4-bit format before encoding them as a sequence of the words AD0-AD15. Alternatively, the input auxiliary data

can be pre-encoded as a sequence of 8-bit words AD0-AD15, and the pre-encoded auxiliary data then provided to the transmitter in the form of a sequence of the 8-bit words AD0-AD15.

Typically, the encoded auxiliary data are transmitted in the same channels (CH0, CH1, and CH2) of a TMDS link in which video data are transmitted, but the auxiliary data are transmitted during the blanking intervals (in which DE = 0) between the active video periods (in which DE = 1) of video data transmission. Figs. 5 and 6 are timing diagrams of signals transmitted during such an embodiment of the invention. The upper nine signals of Fig. 5 represent signals input to the transmitter during a blanking interval, and the lower three signals of Fig. 5 represent the auxiliary data (encoded using the 10-bit words of Fig. 4) and encoded control and sync signals (to be discussed below) that are transmitted over channels CH0, CH1, and CH2 during the blanking interval in response to the upper nine signals. Similarly, the upper nine signals of Fig. 6 represent signals input to the transmitter at the end of the blanking interval (of Fig. 5) and during the active video period that follows such blanking interval, and the lower three signals of Fig. 6 represent the auxiliary data (encoded using the 10-bit words of Fig. 4), video data (conventionally encoded), and encoded control and sync signals (to be discussed below) that are transmitted over channels CH0, CH1, and CH2 in response to the upper nine signals.

In Figs. 5 and 6:

24-bit words of input data are provided to the encoding circuitry of the transmitter for encoding. Fig. 5 pertains to those of such words (each identified as D[23:0] in Fig. 5) that are words of auxiliary data. Fig. 6 pertains to those of such words (each identified as D[23:0] in Fig. 6) that are words of video data. Eight bits of each input word (D[23:16]) are encoded, serialized, and transmitted on channel CH2 (as 10-bit encoded words CH2[0:9]), another eight bits of each such word (D[15:8]) are encoded, serialized, and transmitted on channel CH1 (as 10-bit encoded words CH1[0:9]) and another eight bits of each such word (D[7:0]) are encoded, serialized, and transmitted on channel CH0 (as 10-bit encoded words CH0[0:9]). In some implementations, the video data are in RGB format (and the red, green, and blue pixels are transmitted on channels CH2, CH1, and CH0, respectively). In view of this, channels CH2, CH1, and CH0, are sometimes referred to herein (such as in Fig. 3) as the red (or "R") channel, the green (or "G" channel), and the blue (or "B") channel,

respectively. Alternatively, the video data that are encoded (and then transmitted) are in luminance-chrominance format;

the waveform "DCK" indicates the data clock. During each cycle of the data clock, the ten bits of each one of the inventive code words indicative of auxiliary data (or a guard band), or each of the conventional TMDS 10-bit code words indicative of video data, are sequentially transmitted over the relevant one of channels CH0, CH1, and CH2. In an actual implementation, a clock having ten times the frequency of DCK (but in phase with DCK) would be used to clock the encoding, transmission, and decoding operations, and one code bit would be transmitted during each cycle of this faster clock;

the waveform "DE" (of Fig. 6) is the video data enable signal, and the waveform "AUX DE" (of Fig. 5) is the auxiliary data enable signal. When DE = 1 and AUX DE = 0, video data (identified as D[23:16], D[15:8], and D[7:0] in Fig. 6) are encoded, and serialized 10-bit words of the encoded video are transmitted over channels CH0, CH1, and CH2. When DE = 0 and AUX DE = 1, auxiliary data (identified as D[23:16], D[15:8], and D[7:0] in Fig. 5) are encoded, and serialized 10-bit words of the encoded auxiliary data are transmitted over channels CH0, CH1, and CH2. When DE = 0 and AUX DE = 0, the transmitter ignores signals asserted to its data inputs and instead encodes (as 10-bit TMDS code words) control bit pairs asserted to its control inputs (bits CTL3 and CTL2, indicated as "CTL[3:2]" in Figs. 5 and 6, and bits CTL1 and CTL0, indicated as "CTL[1:0]" in Figs. 5 and 6), serializes these code words, and transmits the serialized code words over channels CH1 and CH2, and encodes (as 10-bit transition-maximized words) sync bit pairs (HSYNC and VSYNC) asserted to its sync inputs, serializes these code words, and transmits the serialized code words over channel CH0.

More specifically, each blanking interval (each interval in which DE = 0) has at least three portions: an initial portion (a "front porch") followed by an auxiliary data portion followed by a final portion (a "back porch"). Optionally, there are two or more auxiliary data periods in a blanking interval (each comprising at least one auxiliary guard band word followed by a burst of a different channel of encoded auxiliary data), a front porch between the falling edge of DE (at the start of the blanking interval) and the start of the first auxiliary data portion, an additional front porch before each subsequent auxiliary data period in the blanking interval, and a back porch between the last auxiliary data period and the next active video period. During each front porch,

repetitions of code words indicative of specific patterns of control bits CTL3, CTL2, CTL1, and CTL0, repetitions of code words indicative of any pattern of sync bits HSYNC and VSYNC, and optionally also initial bit patterns (e.g., patterns in the time interval labeled "Rsvd" in Fig. 5 at the start of the front porch of channels CH2 and CH1) are transmitted. During the back porch, repetitions of code words indicative of other specific patterns of control bits CTL3, CTL2, CTL1, and CTL0, repetitions of code words indicative of any pattern of sync bits HSYNC and VSYNC, and optionally also initial bit patterns (e.g., patterns in the time interval labeled "Rsvd" in Fig. 6 at the start of the back porch of channels CH2 and CH1) are transmitted. During the auxiliary data portion, the inventive code words (indicative of encoded auxiliary data) and guard band words are transmitted.

More specifically, the following signals are transmitted during the back porch (as indicated in Figs. 3 and 6): repetitions of a code word, "0010101011" indicative of CTL3 =0, CTL2=0 are transmitted on CH2 (preferably after an initial bit pattern in the "Rsvd" interval), repetitions of the same code word, "0010101011" indicative of CTL1 =0, CTL0=0 are transmitted on CH1(preferably after an initial bit pattern), and repetitions of a code word indicative of one of the four possible combinations of sync bits HSYNC and VSYNC are transmitted on CH0. Normally, during the final 12 pixel clock cycles of the back porch (just before the 0-to-1 transition of DE as shown in Fig. 6), both sync bits HSYNC and VSYNC have the value 0, so that the code word indicative of HSYNC = 0, VSYNC = 0 (namely the code word "0010101011" shown at the bottom of Fig. 6, or a polarity inverted version of this code word) is transmitted over the channel CH0.

The following signals are transmitted during the front porch (as indicated in Figs. 3 and 5): repetitions of a code word, "1101010100" indicative of CTL3 = 0, CTL2 = 1 are transmitted on CH2 (preferably after an initial bit pattern in the "Rsvd" interval), repetitions of the code word, "0010101010" indicative of CTL1 = 1, CTL0 = 0 are transmitted on CH1 (preferably after an initial bit pattern), and repetitions of a code word indicative of one of the four possible combinations of sync bits HSYNC and VSYNC are transmitted on CH0. Typically, during a "VSYNC" period of the front porch (the VSYNC window of Fig. 3), code words of specific values of CTL3, CTL2, CTL1, CTL0, VSYNC, and HSYNC (as shown in Fig. 3) are transmitted on channels CH2, CH1, and CH0.

Although Figs. 5 and 6 have been described with reference to two data enable signals, "DE" and "AUX DE," it is contemplated that the transmitter can be implemented with a portion (a "core") configured to perform all the described encoding, serialization, and transmission in response to a single data enable signal (e.g., a combined enable signal indicative of the result of performing a logical "OR" operation on the signals DE and AUX DE), and a single set of data inputs (D[23:0]) indicative of either video or auxiliary data. Additional circuitry of the transmitter outside the core is configured to receive separate sets of auxiliary data (e.g., 24-bit auxiliary data words) and video data (e.g., 24-bit video data words), and both a video data enable signal DE, and an auxiliary data enable signal "AUX DE." The signals DE and AUX DE occur in the repeating sequence (DE = 0, AUX DE = 0), (DE = 1, AUX DE = 0), (DE = 0, AUX DE = 0), and (DE = 0, AUX DE = 1), and the additional circuitry includes logic circuitry that "ORs" together the signals DE and AUX DE to produce a combined data enable signal. The additional circuitry also packs the auxiliary data into 4-bit format, encodes each 4-bit portion of the auxiliary data as one of the words AD0-AD15 shown in Fig. 4, adds guard band words with appropriate timing into the stream of AD0-AD15 auxiliary data words, and replaces (with appropriate timing) words of the video data with video guard band words. The additional circuitry asserts alternating bursts of the video data (with video guard band words) and auxiliary data (with guard band words) to the core, and also asserts the combined data enable signal to the core. The core performs all the encoding, serialization, and transmission operations described with reference to Figs. 5 and 6 in response to the combined data enable signal (rather than separate DE and AUX DE signals) and the alternating bursts of video and auxiliary data.

In each of at least one channel of a serial link (e.g., in each of channels CH2 and CH1 in the case of data transmission in accordance with the invention over a TMDS link), an appropriate one of the inventive code words is (or two or more appropriate ones of the inventive guard band words are) preferably transmitted (as a guard band word or set of guard band words) at the start of each burst of encoded auxiliary data (i.e., immediately after each "front porch" of each blanking interval), at the end of each burst of encoded auxiliary data (i.e., immediately before each "back porch" of each blanking interval), and at the start of each burst of encoded video data (i.e., immediately after each "back porch" of each blanking interval).

Each guard band word should have a bit pattern which allows the receiver to

more reliably identify the relevant transition (indicated by the guard band word or words) between encoded control (or sync) word transmission and encoded data transmission. Thus, an additional factor in the selection of the inventive code word set is that it preferably includes appropriate guard band words. For example, the set of 17 inventive code words shown in Fig. 4 includes a special auxiliary guard band word (having bit pattern "1100110010," and shown in Fig. 4 as the uppermost one of the 17 code words shown) that is used to identify the start of an auxiliary data burst. As shown in Fig. 5, two repetitions of this "pre-data" auxiliary guard band word are preferably transmitted at the start of each burst of encoded auxiliary data (i.e., just after each front porch) in each of channels CH2 and CH1. Since the last bit of each specific encoded control word transmitted in channels CH2 and CH1 (during the front porch) is "0" as explained above, the first transmitted bit of the code word chosen as the pre-data auxiliary guard band word is "1" to increase the reliability with which the receiver can identify the start of a transmitted burst of auxiliary data.

The set of 17 inventive code words shown in Fig. 4 also includes a word (the word "0011001101" that corresponds to input word AD11) that is used to identify the end of an auxiliary data burst, and is also used as a video guard band word. As shown in Fig. 5, two repetitions of this "post-data" auxiliary guard band word are preferably transmitted at the end of each burst of encoded auxiliary data (i.e., just before each back porch) in each of channels CH2 and CH1.

The pre-data auxiliary guard band word need not be repeated (transmitted twice) at the start of each auxiliary data burst, and the post-data auxiliary guard band word need not be repeated at the end of each auxiliary data burst. In the preferred embodiment (indicated by Fig. 5), each is repeated in order to allow the receiver more easily to recognize and correct for data shift errors between channels that can occur during transmission and recovery of the data (e.g., error in the phase of the received data on channel CH1 relative to that of the data received on channel CH2). In other embodiments of the invention, an auxiliary guard band word is repeated more than twice (or is transmitted only once) at the start of each auxiliary data burst and/or more than twice (or is transmitted only once) at the end of each auxiliary data burst.

With reference to Fig. 4, the inventive code word "0011001101" (that corresponds to input word AD11) is used as a video guard band word to identify the start of a video data burst, in addition to being used as a code word for encoding the four-bit quantity of auxiliary data indicated by input word AD11, and as a post-data

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auxiliary guard band word. As shown in Fig. 6, two repetitions of this video guard band word are preferably transmitted at the start of each burst of encoded video data (i.e., just after each back porch). Since the last two bits of the encoded control or sync word transmitted in each of channels CH0, CH1, and CH2 (at the end of the back porch) are likely to be "11" as explained above, the first two transmitted bits of the video guard band word are chosen to be "00" to increase the reliability with which the receiver can identify the start of a transmitted burst of video data.

The video guard band word need not be repeated (transmitted twice) at the start of each video data burst. In the preferred embodiment shown in Fig. 6, it is repeated in order to ensure transmission (on each of channels CH0, CH1, and CH2) of code words indicative of an even number of pixels during the burst. In other embodiments, a video guard band word is repeated more than twice (or is transmitted only once) at the start of each video data burst.

In some embodiments of the invention, two (or more than two) streams of video data are transmitted (over one, two, or more than two channels). For example, two or more streams of video data can be transmitted in time-multiplexed fashion over each of one or more of Channels 0, 1, and 2 of Fig. 2. If bursts of different streams of video data are sequentially transmitted over one channel, different video guard band words can be transmitted at the start (and/or the end) of each burst, with each different stream being identified by a different video guard band word. Similarly, two (or more than two) streams of auxiliary data can be transmitted over one, two, or more than two channels). If bursts of different streams of auxiliary data are sequentially transmitted over one channel, different auxiliary guard band words can be transmitted at the start (and/or the end) of each burst, with each different stream being identified by a different guard band word.

Where encoded data are transmitted serially over multiple independent channels, DE shifts in individual channels can be corrected independently (in accordance with the invention) by using guard band words in each channel. Since there can be misalignment between the DE transitions indicated by the bits transmitted over multiple channels of a TMDS link (or TMDS-like link or other serial link) by one pixel clock cycle in either direction (due to ISI or other noise sources on the link), a set of identical guard band words (each a member of the set of inventive code words) is preferably transmitted in accordance with the invention at the start or end of each burst of data encoded using the inventive code words that is transmitted over each channel

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(e.g., at the end of the front porch of each channel, and/or at the start of the back porch of each channel, and/or at the end of the back porch of each channel). This can improve the channel to channel alignment and data integrity. The need to have available the appropriate number of guard band word is a factor in the selection of the inventive set of code words.

The purpose of repeating the transmission of a guard band word (either at the transition between an expected bit pattern and a burst of data encoded in accordance with the invention following such pattern, or at the transition between a burst of data encoded in accordance with the invention and an expected bit pattern that follows such data) is to prevent two types of misidentification of transitions: identifying the transition too early and identifying the transition too late. By transmitting a repeating sequence of N guard band words, the invention prevents such pixel shift errors up to N-1 pixels in either direction. For example, if a sequence of N post-data guard band words is appended to an encoded data burst, the invention ensures that when there is an N-1 pixel shift to the left, the last data value is not lost (only the post-data guard band word is lost). Generally, a sequence of only N-1 post-data guard band words is needed for use with a sequence of N pre-data guard band words.

In the preferred embodiment (indicated by Fig. 5), the auxiliary guard band words transmitted at the start and end of each auxiliary data burst on channels CH2 and CH1 are not transmitted at the start and end of each auxiliary data burst on channel CH0. Rather, special encoding is used to determine the first two and last two 10-bit inventive code words transmitted in each auxiliary data burst on channel CH0. Specifically, each of the first input auxiliary data packet to be encoded and the last input auxiliary data packet to be encoded comprises two bits (whereas all the other packet comprise four bits as described above). The first 2-bit input auxiliary packet is encoded as one of the words AD0, AD1, AD2, and AD3 in Fig. 4. The first two 10-bit words transmitted in the burst are repeated versions of the inventive code word that is indicative of this one of words AD0, AD1, AD2, and AD3 (and are thus indicative of the first two bits of input auxiliary data). Similarly, the last 2-bit input auxiliary packet is encoded as one of the words AD0, AD1, AD2, and AD3 in Fig. 4. The last two 10-bit words transmitted in the burst are repeated versions of the inventive code word that is indicative of this one of words AD0, AD1, AD2, and AD3 (and are thus indicative of the last two bits of input auxiliary data.

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More generally, control or synchronization bits (e.g., the 10-bit control characters indicative of bits CTL0:CTL1 or CTL2:CTL3 in the TMDS specification) can produce different errors on video (or auxiliary) data bits that are transmitted just after the control characters, when ISI is present on the serial data transmission channel. This is preferably recognized and used as a factor in selecting the inventive code word set for use in transmitting the video (or auxiliary) data. Alternatively, the control codes sent just before the data (encoded in accordance with the invention) are controlled to reduce the ISI effect.

In other embodiments of the invention, bursts of encoded auxiliary data and bursts of encoded video data are transmitted over a serial link (which need not be a TMDS link), and the auxiliary data are encoded in accordance with the invention using a set of inventive code words. The set of inventive code words includes a "video" guard band word that is transmitted at the start of each encoded video data burst, and an "auxiliary" guard band word that is transmitted at the start of each encoded auxiliary data burst. In some implementations, the video guard band word is also used for a second purpose: to encode auxiliary data. In preferred implementations of such embodiments, the encoded video data are transmitted during active video periods in which a control signal "DE" is high (DE = 1), and encoded control (or synchronization) signals and encoded auxiliary data are transmitted during blanking intervals (in which DE = 0) between active video periods. A video guard band word is transmitted at the start of each active video period. Each blanking interval comprises a preamble (or "front porch") period (between the falling edge of DE and the start of a burst of auxiliary data) in which control (or sync) signals of a specific type are transmitted, an auxiliary data period (after the preamble period) comprising an auxiliary guard band word followed by a burst of encoded auxiliary data, and a "back porch" period between the auxiliary data period and the next active video period. In general, the purpose of using guard band words in accordance with the invention is to guarantee that the receiver can recognize the transition between the first guard band word transmitted at the start of an encoded data burst and the last bit transmitted before such guard band word, and between the last guard band word transmitted at the end of an encoded data burst and the first bit transmitted after such guard band word.

In a class of embodiments of the invention, a conventional encoding algorithm is used to encode primary data (which can but need not be video data) for transmission in bursts over a serial link, and auxiliary data (e.g., audio data or data of another type

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that can be transmitted with a lower data rate than the primary data) are encoded in accordance with the invention for transmission in bursts (between bursts of the encoded primary data) over a serial link. The full set of code words used for encoding the primary data has at least one code word for each of 2^N different words of the primary data (sometimes referred to as source data words). The inventive subset of such full set has at least one code word for each of not more than 2^M different words (where $M < N$) of the auxiliary data (also referred to sometimes as source data words). The auxiliary data are buffered and packed into M-bit format (i.e., into words each consisting of M bits). Each possible value of the M-bit source data has a preselected code in the 2^M-word space provided by the inventive code words. The M-bit words of auxiliary data are mapped to inventive code words in the 2^M-word space which are then transmitted over the link. The process by which the inventive set of code words is selected from a full set of code words is very important. The inventive set of code words is selected such that each stream of encoded data (comprising only inventive code words) transmitted over a serial link has a bit pattern that is less susceptible to ISI during transmission than is the bit pattern determined by a transmitted, conventionally encoded version of the same data (comprising not only inventive code words but also members of the full set that are not inventive code words). In general, the best choice for the particular inventive code words selected from a full set of binary code words depends on the particular coding implemented by the full set (i.e., the details of which bits of each code word in the full set are zeroes and which are ones). In preferred embodiments, the inventive code words are selected to be those whose serial patterns (during transmission over a serial link) have fewer contiguous zeros and ones (and thus are less susceptible to ISI during transmission) than do those code words in the full set that are not selected.

In choosing which of the inventive code words to employ to transmit encoded data (e.g. auxiliary data distinct from video data) in accordance with the invention, it is important to consider that some bits (of multi-bit encoded words) present greater risks of error than other such bits. For example, when using TMDS-encoded words to transmit auxiliary data, the DC balancing bits and transition control bits (e.g., bits Q[9] and E[8]) present greater error risks than do the other bits. Any bit error occurring during processing of the DC balancing and transition control bits can affect other bits of the multi-bit encoded words. Hence a one-bit error in one of the critical bits is

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translated into a burst error. This effect is preferably considered in selecting the inventive code words from a full set of TMDS-encoded words.

It should be understood that while certain forms of the present invention are illustrated and described herein, the invention is defined by the claims and is not to be limited to the specific embodiments described and shown.

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CLAIMS

What is claimed is:

1. A communication system, including:

a receiver;

a transmitter; and

a serial link between the transmitter and the receiver, wherein the transmitter is coupled to receive input data, configured to generate a sequence of selected code words by encoding the input data, and configured to transmit the sequence of selected code words to the receiver over the serial link, wherein each of the selected code words is a member of a robust subset of a full code word set, the input data can be encoded as a conventional sequence of code words of the full code word set, and the sequence of selected code words is less susceptible to inter-symbol interference during transmission over the link than would be the conventional sequence of code words.

2. The system of claim 1, wherein the input data are auxiliary data, the transmitter is coupled to receive video data and configured to generate a sequence of video code words by encoding the video data, and the transmitter is configured to transmit to the receiver over the serial link a first burst of the video code words followed by a burst of the selected code words followed by a second burst of the video code words, wherein each of the video code words is a member of the full code word set and at least one of the video code words is not a member of the robust subset.

3. The system of claim 2, wherein the transmitter is also coupled to receive control bits, configured to generate bursts of encoded control words by encoding the control bits, and configured to transmit to the receiver over the serial link a first burst of the encoded control words between the first burst of the video code words and the burst of the selected code words, and a second burst of the encoded control words between the burst of the selected code words and the second burst of the video code words.

4. The system of claim 3, wherein the selected code words include at least one guard band word, the burst of the selected code words has an initial word, and the initial word is the guard band word.

5. The system of claim 3, wherein the selected code words include at least one guard band word, the burst of the selected code words has an initial set of words, and each word of the initial set of words is one said guard band word.

6. The system of claim 3, wherein the selected code words include at least one guard band word, the burst of the selected code words has a final word, and the final word is the guard band word.

7. The system of claim 3, wherein the selected code words include at least one guard band word, the burst of the selected code words has a final set of words, and each word of the final set of words is one said guard band word.

8. The system of claim 3, wherein the serial link is a TMDS link, and the selected code words consist of seventeen different, transition-minimized TMDS code words, including at least one transition-minimized TMDS code word used as a guard band word.

9. The system of claim 3, wherein the selected code words include at least two guard band words, including a first guard band word and a second guard band word, the second burst of the video code words has an initial word, the initial word of the second burst of the video code words is the first guard band word, the burst of the selected code words has an initial word, and the initial word of the burst of the selected code words is the second guard band word.

10. The system of claim 9, wherein the serial link is a TMDS link, and the selected code words consist of seventeen different, transition-minimized TMDS code words, including one transition-minimized TMDS code word used only as said second guard band word and another transition-minimized TMDS code word used as said first guard band and also used as one of the selected code words in said burst of the selected code words.

11. The system of claim 1, wherein the input data are auxiliary data, the transmitter is coupled to receive video data and configured to generate a sequence of

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video code words by encoding the video data, and the transmitter is configured to transmit to the receiver over the serial link a burst of the selected code words followed by a burst of the video code words, wherein each of the video code words is a member of the full code word set and at least one of the video code words is not a member of the robust subset.

12. The system of claim 11, wherein the transmitter is also coupled to receive control bits, configured to generate bursts of encoded control words by encoding the control bits, and configured to transmit to the receiver over the serial link a burst of the encoded control words between the burst of the selected code words and the burst of the video code words.

13. The system of claim 12, wherein the selected code words include at least one guard band word, the burst of the video code words has an initial word, and the initial word is the guard band word.

14. The system of claim 12, wherein the selected code words include at least one guard band word, the burst of the video code words has an initial set of words, and each word of the initial set of words is one said guard band word.

15. The system of claim 1, wherein the serial link is a TMDS link.

16. The system of claim 15, wherein the selected code words consist of seventeen different TMDS code words, including one TMDS code word used only as a guard band word.

17. The system of claim 15, wherein the selected code words consist of seventeen different, transition-minimized TMDS code words, including one transition-minimized TMDS code word used only as a guard band word.

18. The system of claim 1, wherein each of the selected code words is an L-bit binary word.

19. The system of claim 1, wherein each of the selected code words is an L-bit binary word, and each of at least a subset of the selected code words is indicative of an M-bit word of the input data, where M is less than L.

20. The system of claim 19, wherein L = 10, and M = 4.

21. The system of claim 19, wherein the transmitter is coupled to receive source words of the input data, where each of the source words comprises N bits, N is less than L, and N is greater than M, and the transmitter is configured to pack the source words into M-bit words of the input data and to encode each of the M-bit words of the input data as one of the selected code words.

22. The system of claim 1, wherein each of the selected code words is an L-bit binary word, a first subset of the selected code words is indicative of an M-bit word of the input data, where M is less than L, and a second subset of the selected code words is indicative of an N-bit word of the input data, where N is less than M.

23. The system of claim 22, wherein L = 10, M = 4, and N = 2.

24. The system of claim 1, wherein the full code word set is a set of 10-bit, transition-minimized, TMDS code words.

25. The system of claim 1, wherein each of the selected code words is indicative of a sequence of L binary bits, and the selected code words have fewer contiguous zero bits and continuous one bits per code word on the average than do the code words of the full code word set excluding the selected code words.

26. The system of claim 1, wherein each of the selected code words is indicative of a different sequence of binary bits, the transmitter is configured to transmit the sequence of selected code words to the receiver over the serial link as a sequence of rising and falling voltage transitions, and the selected code words have bit patterns that implement DC balancing by limiting voltage drift of the serial link during transmission of said sequence of selected code words to a predetermined amount.

27. The system of claim 1, wherein the input data are auxiliary data, the transmitter is coupled to receive video data and configured to generate a sequence of video code words by encoding the video data, and the transmitter is configured to transmit to the receiver over the serial link a first burst of the video code words followed by at least two bursts of the selected code words followed by a second burst of the video code words, wherein each of the video code words is a member of the full code word set and at least one of the video code words is not a member of the robust subset.

28. A communication system, including:

a receiver;

a transmitter; and

a serial link, a second serial link, and a third serial link between the transmitter and the receiver, wherein the transmitter is coupled to receive input data and video data, configured to generate sequences of selected code words by encoding the input data and to generate sequences of video code words by encoding the video data, and configured to transmit to the receiver over the serial link a burst of the selected code words followed by a burst of the video code words, to transmit to the receiver over the second serial link a second burst of the selected code words followed by a second burst of the video code words, and to transmit to the receiver over the third serial link a third burst of the selected code words followed by a third burst of the video code words,

wherein each of the selected code words is a member of a robust subset of a full code word set, each of the video code words is a member of the full code word set, and at least one of the video code words is not a member of the robust subset, and

wherein the input data determined by the burst of the selected code words can be encoded as a first conventional sequence of the code words of the full code word set, the input data determined by the second burst of the selected code words can be encoded as a second conventional sequence of the code words of the full code word set, and the input data determined by the third burst of the selected code words can be encoded as a third conventional sequence of the code words of the full code word set, and wherein said burst of the selected code words is less susceptible to inter-symbol interference during transmission over the serial link than would be the first conventional sequence, said second burst of the selected code words is less susceptible

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to inter-symbol interference during transmission over the second serial link than would be the second conventional sequence, and said third burst of the selected code words is less susceptible to inter-symbol interference during transmission over the third serial link than would be the third conventional sequence.

29. The system of claim 28, wherein the transmitter is also coupled to receive control bits, configured to generate sequences of encoded control words by encoding the control bits, and configured to transmit to the receiver over the serial link a burst of the encoded control words between the burst of the selected code words and the burst of the video code words, to transmit to the receiver over the second serial link a second burst of the encoded control words between the second burst of the selected code words and the second burst of the video code words, and to transmit to the receiver over the third serial link a third burst of the encoded control words between the third burst of the selected code words and the third burst of the video code words.

30. The system of claim 28, wherein the serial link is a first video channel of a TMDS link, the second serial link is a second video channel of the TMDS link, and the third serial link is a third video channel of the TMDS link.

31. The system of claim 30, wherein the selected code words consist of seventeen different TMDS code words, including one TMDS code word used only as a guard band word.

32. The system of claim 30, wherein the selected code words consist of seventeen, different, transition-minimized TMDS code words, including one transition-minimized TMDS code word used only as a guard band word.

33. A transmitter for use in data transmission over a serial link, said transmitter including:

at least one input for receiving input data;

an output configured to be coupled to a channel of the link; and

circuitry, coupled to each said input and to the output, and configured to generate a sequence of selected code words by encoding the input data and to assert the sequence of selected code words to the output in response to the input data,

wherein each of the selected code words is a member of a robust subset of a full code word set, the input data can be encoded as a conventional sequence of code words of the full code word set, and the sequence of selected code words is less susceptible to inter-symbol interference during transmission over the link than would be the conventional sequence of code words.

34. The transmitter of claim 33, wherein the input data include auxiliary data and video data, and the circuitry is configured to generate a sequence of video code words by encoding the video data, and to assert to the output a first burst of the video code words followed by a burst of the selected code words followed by a second burst of the video code words, wherein each of the video code words is a member of the full code word set and at least one of the video code words is not a member of the robust subset.

35. The transmitter of claim 34, wherein the circuitry is also coupled to receive control bits, configured to generate bursts of encoded control words by encoding the control bits, and to assert to the output a first burst of the encoded control words between the first burst of the video code words and the burst of the selected code words, and a second burst of the encoded control words between the burst of the selected code words and the second burst of the video code words.

36. The transmitter of claim 35, wherein the selected code words include at least one guard band word, the burst of the selected code words has an initial word, and the initial word is the guard band word.

37. The transmitter of claim 35, wherein the selected code words include at least one guard band word, the burst of the selected code words has an initial set of words, and each word of the initial set of words is one said guard band word.

38. The transmitter of claim 35, wherein the selected code words include at least one guard band word, the burst of the selected code words has a final word, and the final word is the guard band word.

39. The transmitter of claim 35, wherein the selected code words include at least one guard band word, the burst of the selected code words has a final set of words, and each word of the final set of words is one said guard band word.

40. The transmitter of claim 35, wherein the serial link is a TMDS link, and the selected code words consist of seventeen different, transition-minimized TMDS code words, including at least one transition-minimized TMDS code word used as a guard band word.

41. The transmitter of claim 35, wherein the selected code words include at least two guard band words, including a first guard band word and a second guard band word, the second burst of the video code words has an initial word, the initial word of the second burst of the video code words is the first guard band word, the burst of the selected code words has an initial word, and the initial word of the burst of the selected code words is the second guard band word.

42. The transmitter of claim 41, wherein the serial link is a TMDS link, and the selected code words consist of seventeen different, transition-minimized TMDS code words, including one transition-minimized TMDS code word used only as said second guard band word and another transition-minimized TMDS code word used as said first guard band and also used as one of the selected code words in said burst of the selected code words.

43. The transmitter of claim 34, wherein the serial link is a TMDS link, and the selected code words consist of seventeen different TMDS code words, including one TMDS code word used only as a guard band word.

44. The transmitter of claim 43, wherein the selected code words consist of seventeen different, transition-minimized TMDS code words, including one transition-minimized TMDS code word used only as the guard band word.

45. The transmitter of claim 33, wherein each of the selected code words is an L-bit binary word.

46. The transmitter of claim 33, wherein each of the selected code words is an L-bit binary word, and each of at least a subset of the selected code words is indicative of an M-bit word of the input data, where M is less than L.

47. The transmitter of claim 46, wherein L = 10, and M = 4.

48. The transmitter of claim 46, wherein the circuitry is coupled to receive source words of the input data, where each of the source words comprises N bits, N is less than L, and N is greater than M, and the circuitry is configured to pack the source words into M-bit words of the input data and to encode each of the M-bit words of the input data as one of the selected code words.

49. The transmitter of claim 33, wherein each of the selected code words is an L-bit binary word, a first subset of the selected code words is indicative of an M-bit word of the input data, where M is less than L, and a second subset of the selected code words is indicative of an N-bit word of the input data, where N is less than M.

50. The transmitter of claim 49, wherein L = 10, M = 4, and N = 2.

51. The transmitter of claim 33, wherein the full code word set is a set of 10-bit, transition-minimized, TMDS code words.

52. The transmitter of claim 33, wherein each of the selected code words is indicative of a sequence of L binary bits, and the selected code words have fewer contiguous zero bits and continuous one bits per code word on the average than do the code words of the full code word set excluding the selected code words.

53. The transmitter of claim 33, wherein each of the selected code words is indicative of a different sequence of binary bits, the circuitry is configured to assert the sequence of selected code words as a sequence of rising and falling voltage transitions, and the selected code words have bit patterns that implement DC balancing by limiting voltage drift of the serial link during transmission of said sequence of selected code words to a predetermined amount.

54. A method for encoding data for transmission over a serial link, said method including the steps of:

(a) providing words of input data capable of being encoded as a conventional sequence of code words of a full code word set; and

(b) generating a sequence of selected code words by encoding the input data, wherein each of the selected code words is a member of a robust subset of the full code word set, and the sequence of selected code words is less susceptible to inter-symbol interference during transmission over the link than would be the conventional sequence of code words.

55. The method of claim 54, wherein the input data include auxiliary data and video data, and also including the steps of:

generating a sequence of video code words by encoding the video data; and

transmitting over the link a first burst of the video code words followed by a burst of the selected code words followed by a second burst of the video code words, wherein each of the video code words is a member of the full code word set and at least one of the video code words is not a member of the robust subset.

56. The method of claim 55, also including the steps of:

generating bursts of encoded control words by encoding control bits; and

transmitting over the link a first burst of the encoded control words between the first burst of the video code words and the burst of the selected code words, and a second burst of the encoded control words between the burst of the selected code words and the second burst of the video code words.

57. The method of claim 56, wherein the selected code words include at least one guard band word, the burst of the selected code words has an initial word, and the initial word is the guard band word.

58. The method of claim 56, wherein the selected code words include at least one guard band word, the burst of the selected code words has an initial set of words, and each word of the initial set of words is one said guard band word.

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59. The method of claim 56, wherein the selected code words include at least one guard band word, the burst of the selected code words has a final word, and the final word is the guard band word.

60. The method of claim 56, wherein the selected code words include at least one guard band word, the burst of the selected code words has a final set of words, and each word of the final set of words is one said guard band word.

61. The method of claim 56, wherein the selected code words consist of seventeen different, transition-minimized TMDS code words, including at least one transition-minimized TMDS code word used as a guard band word.

62. The method of claim 56, wherein the selected code words include at least two guard band words, including a first guard band word and a second guard band word, the second burst of the video code words has an initial word, the initial word of the second burst of the video code words is the first guard band word, the burst of the selected code words has an initial word, and the initial word of the burst of the selected code words is the second guard band word.

63. The method of claim 62, wherein the selected code words consist of seventeen different, transition-minimized TMDS code words, including one transition-minimized TMDS code word used only as said second guard band word and another transition-minimized TMDS code word used as said first guard band and also used as one of the selected code words in said burst of the selected code words.

64. The method of claim 54, wherein the selected code words consist of seventeen different TMDS code words, including one TMDS code word used only as a guard band word.

65. The method of claim 54, wherein the selected code words consist of seventeen different, transition-minimized TMDS code words, including one transition-minimized TMDS code word used only as a guard band word.

66. The method of claim 54, wherein each of the selected code words is an L-bit binary word.

67. The method of claim 54, wherein each of the selected code words is an L-bit binary word, and each of at least a subset of the selected code words is indicative of an M-bit word of the input data, where M is less than L.

68. The method of claim 67, wherein L = 10, and M = 4.

69. The method of claim 67, wherein step (a) includes the step of providing source words of the input data, where each of the source words comprises N bits, N is less than L, and N is greater than M, and step (b) includes the steps of packing the source words into M-bit words of the input data and encoding each of the M-bit words of the input data as one of the selected code words.

70. The method of claim 54, wherein each of the selected code words is an L-bit binary word, a first subset of the selected code words is indicative of an M-bit word of the input data, where M is less than L, and a second subset of the selected code words is indicative of an N-bit word of the input data, where N is less than M.

71. The method of claim 70, wherein L = 10, M = 4, and N = 2.

72. The method of claim 54, wherein the full code word set is a set of 10-bit, transition-minimized, TMDS code words.

73. The method of claim 54, wherein each of the selected code words is indicative of a sequence of L binary bits, and the selected code words have fewer contiguous zero bits and continuous one bits per code word on the average than do the code words of the full code word set excluding the selected code words.

74. The method of claim 54, wherein each of the selected code words is indicative of a different sequence of binary bits, and also including the step of:

transmitting the sequence of selected code words over the serial link as a sequence of rising and falling voltage transitions, wherein the selected code words have

bit patterns that implement DC balancing by limiting voltage drift of the serial link during transmission of said sequence of selected code words to a predetermined amount.

75. The method of claim 54, wherein the input data include auxiliary data and video data, and also including the steps of:

generating a sequence of video code words by encoding the video data; and

transmitting over the link a first burst of the video code words followed by at least two bursts of the selected code words followed by a second burst of the video code words, wherein each of the video code words is a member of the full code word set and at least one of the video code words is not a member of the robust subset.

Docket No. P10525

Attorney Docket No. 42390.P10504

ABSTRACT OF THE DISCLOSURE

A communication system including a transmitter, a receiver, and a serial link, in which encoded data (e.g., encoded video data and encoded auxiliary data) are transmitted from the transmitter to the receiver. The serial link can but need not be a TMDS or TMDS-like link. In typical embodiments, alternating bursts of encoded video data and encoded auxiliary data are transmitted over each of one or more channels of the link. Other aspects of the invention are transmitters for use in encoding data for transmission over a serial link, and methods for sending encoded data over a serial link. In accordance with the invention, the data to be transmitted are encoded using a subset (sometimes referred to as a selected set of code words) of a full set of code words. The selected set of code words is selected such that each stream of encoded data (comprising only using such code words) transmitted over a serial link has a bit pattern that is less susceptible to inter-symbol interference ("ISI") during transmission than is the bit pattern determined by a conventionally encoded version of the same data (comprising not only the selected set of code words but also other members of the full set). In general, the best choice for the selected set of code words selected from a full set of binary code words depends on the particular coding implemented by the full set. Typically, the selected set of code words includes words whose serial patterns (during transmission) have fewer contiguous zeros and ones (and thus are less susceptible to ISI during transmission) than do those code words in the full set that are not selected. In preferred embodiments in which the bits of the selected set of code words are transmitted over a serial link as sequences of rising and falling voltage transitions, the bit pattern of each transmitted stream of the selected set of code words implements DC balancing to limit the voltage drift over time.

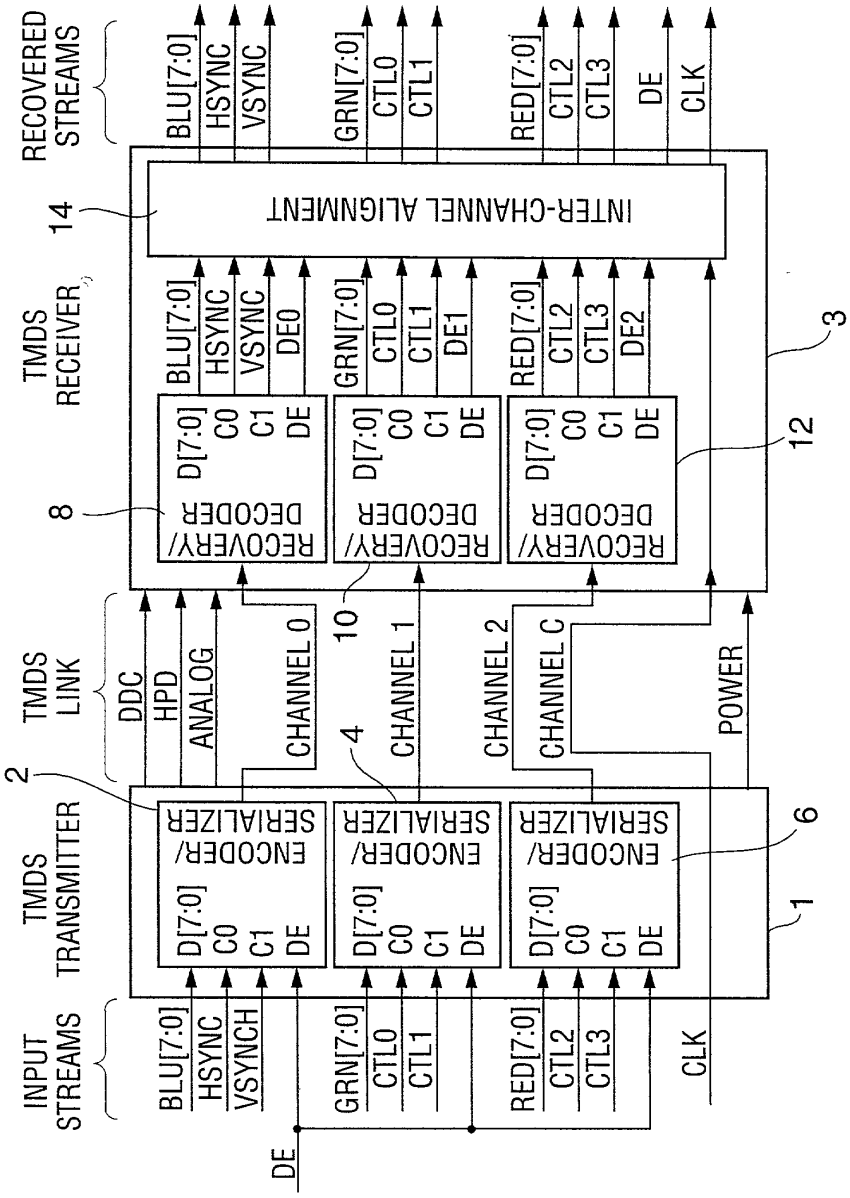


FIG. 1
(PRIOR ART)

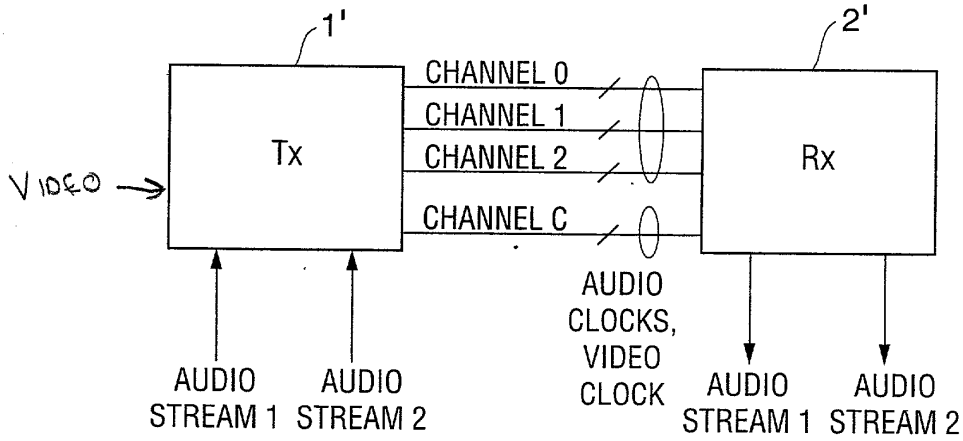


FIG. 2

	Input D7-D0	Hex	TMDS pattern
PRE-DATA GUARD BAND for Aux data	01010101	55	1100110010
AD0	01011011	5B	0011100101
AD1	10110101	B5	0110001101
AD2	11010011	D3	0010011101
AD3	11011001	D9	0100011101
AD4	01101101	6D	0111000101
AD5	10100100	A4	0011100110
AD6	10010010	92	0111000110
AD7	01000100	44	0011110010
AD8	00100010	22	0111100010
AD9	01001011	4B	1001110010
AD10	10010011	93	1000111010
GUARD BAND for video data and POST-DATA GUARD BAND for Aux data (and AD11)	10101011	AB	0011001101
AD12	01011010	5A	1100011001
AD13	01101100	6C	1000111001
AD14	10100101	A5	1100011010
AD15	10111010	BA	1100001101

FIG. 4

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ENCODING METHOD AND SYSTEM FOR
REDUCING INTER-SYMBOL...
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Specific CTL	CTL [1:0]	Preamble (q0 : q9)	Guardband (q0 : q9)	GB (d7 : d0)	Purpose
R (CTL [3:2])	00	0010101011	0011001101	0xAB	Video Preamble/Video Guardband/Post-Data Aux Guardband
G (CTL [1:0])	00	0010101011	0011001101	0xAB	Video Preamble/Video Guardband/Post-Data Aux Guardband
B (VSYNC:HSYNC)	XX	1 of 4 values	0011001101	0xAB	Video Preamble/Video Guardband
R (CTL [3:2])	01	1101010100	1100110010	0x55	Aux Preamble/Pre-Data Aux Guardband
G (CTL [1:0])	10	0010101010	1100110010	0x55	Aux Preamble/Pre-Data Aux Guardband
B (VSYNC:HSYNC)	XX	1 of 4 values	1 of 4 values	0x5B,0xB5, 0xD3, 0xD9	Aux Preamble/Pre- or Post-Data Aux Guardband
R (CTL [3:2])	10	0010101010			VSync Window, HDCP enabled
G (CTL [1:0])	00	0010101011			VSync Window, HDCP enabled
B (VSYNC:HSYNC)	1X	1 of 2 values			VSync Window, HDCP enabled

FIG. 3

FIG.5

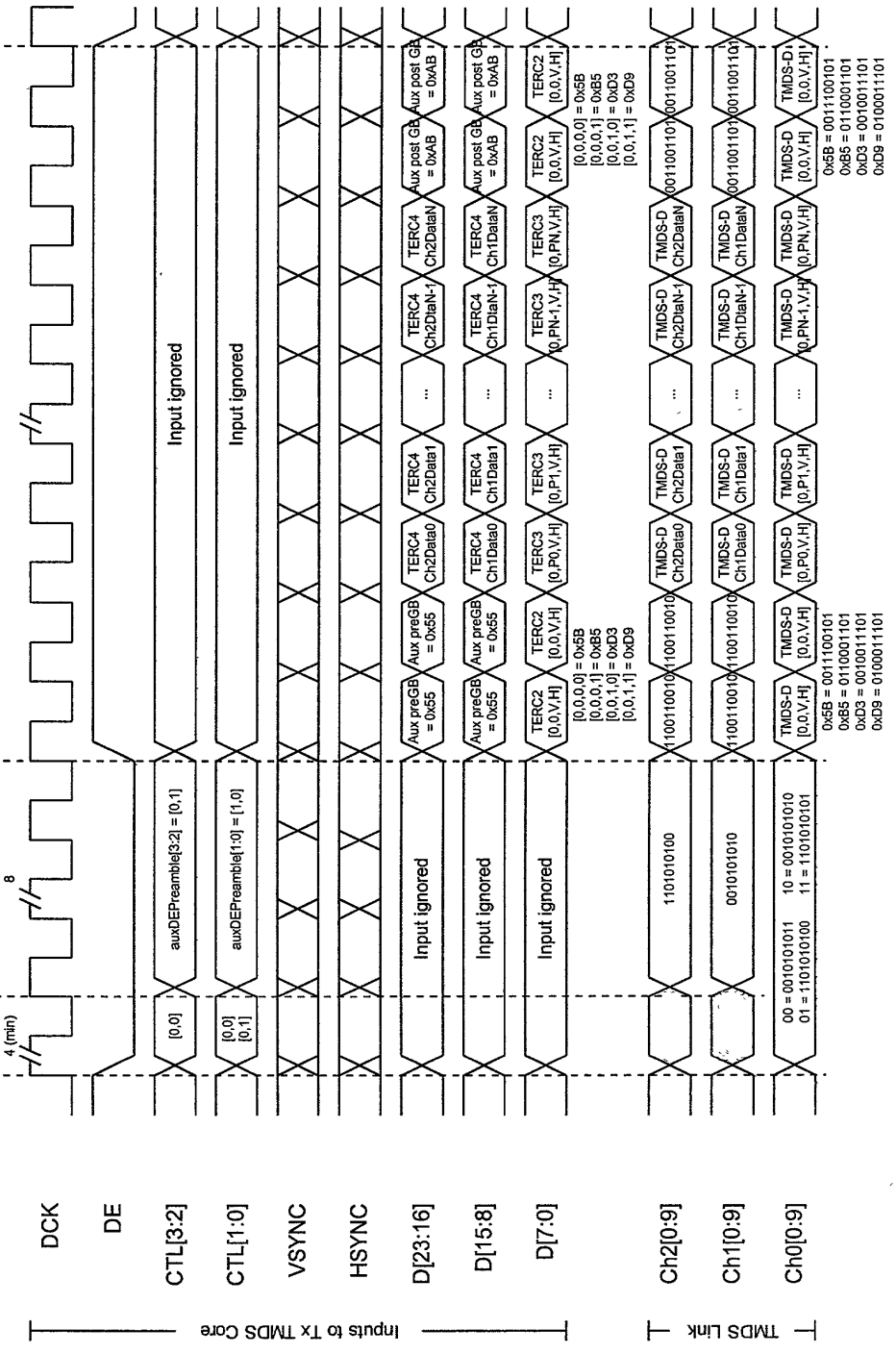
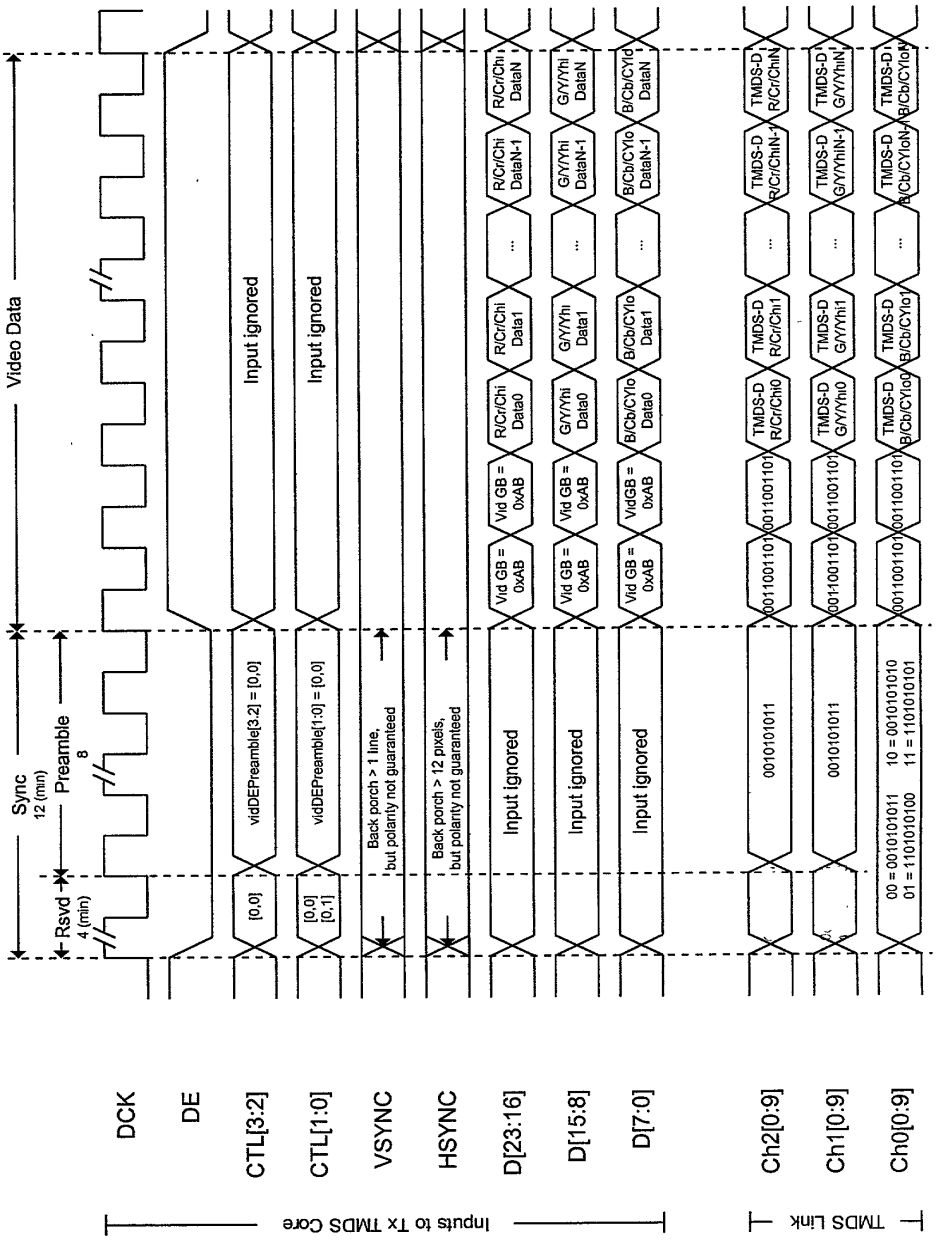

Inputs to Tx TMDS Core
TMDS Link
DCK
DE
CTL[3:2]
CTL[1:0]
VSYNC
HSYNC
D[23:16]
D[15:8]
D[7:0]
Ch2[0:9]
Ch1[0:9]
Ch0[0:9]
Sync
12 (min)
Preamble
8
Rsvd
4 (min)
Data Island
2 + #Pkts*32 +2
auxDEPreamble[3:2] = [0,1]
auxDEPreamble[1:0] = [1,0]
[0,0]
[0,1]
Input ignored
Aux preGB = 0x55
Aux post GB = 0xAB
TERC4 Ch2Data0
TERC4 Ch2Data1
TERC4 Ch2DataN-1
TERC4 Ch2DataN
TERC4 Ch1Data0
TERC4 Ch1Data1
TERC4 Ch1DataN-1
TERC4 Ch1DataN
TERC2 [0,0,V,H]
TERC3 [0,P1,V,H]
TERC3 [0,PN-1,V,H]
TERC3 [0,PN,V,H]
[0,0,0,0] = 0x5B
[0,0,0,1] = 0xB5
[0,0,1,0] = 0xD3
[0,0,1,1] = 0xD9
TMDS-D Ch2Data0
TMDS-D Ch2Data1
TMDS-D Ch2DataN-1
TMDS-D Ch2DataN
TMDS-D Ch1Data0
TMDS-D Ch1Data1
TMDS-D Ch1DataN-1
TMDS-D Ch1DataN
TMDS-D [0,0,V,H]
TMDS-D [0,P0,V,H]
TMDS-D [0,P1,V,H]
TMDS-D [0,PN-1,V,H]
TMDS-D [0,PN,V,H]
1101010100
0010101010
00 = 0010101011
01 = 1101010100
10 = 0010101010
11 = 1101010101
0x5B = 0011100101
0xB5 = 0110001101
0xD3 = 0010011101
0xD9 = 0100011101
(Red)
(Green)
(Blue)

FIG. 6


Video Data
Sync
12 (min)
Preamble
8
Rsvd
4 (min)
DCK
DE
CTL[3:2]
CTL[1:0]
VSYNC
HSYNC
D[23:16]
D[15:8]
D[7:0]
Ch2[0:9]
Ch1[0:9]
Ch0[0:9]
Inputs to Tx TMDS Core
TMDS Link
(Red)
(Green)
(Blue)
Input ignored
vidDEPreamble[3:2] = [0,0]
vidDEPreamble[1:0] = [0,0]
[0,0]
[0,1]
Back porch > 1 line,
but polarity not guaranteed
Back porch > 12 pixels,
but polarity not guaranteed
Vid GB = 0xAB
VidGB = 0xAB
R/Cr/Chi Data0
G/YYhi Data0
B/Cb/CYlo Data0
R/Cr/Chi Data1
G/YYhi Data1
B/Cb/CYlo Data1
R/Cr/Chi DataN-1
G/YYhi DataN-1
B/Cb/CYlo DataN-1
R/Cr/Chi DataN
G/YYhi DataN
B/Cb/CYlo DataN
0010101011
0011001101
0011001100
TMDS-D R/Cr/Chi0
TMDS-D R/Cr/Chi1
TMDS-D R/Cr/ChiN-1
TMDS-D R/Cr/ChiN
TMDS-D G/YYhi0
TMDS-D G/YYhi1
TMDS-D G/YYhiN-1
TMDS-D G/YYhiN
TMDS-D B/Cb/CYlo0
TMDS-D B/Cb/CYlo1
TMDS-D B/Cb/CYloN-1
TMDS-D B/Cb/CYloN
00 = 0010101011 10 = 0010101010
01 = 1101010100 11 = 1101010101

Express Mail Number EF 246 132 842 US

Atty Docket No. SII-1000

DECLARATION FOR PATENT APPLICATION

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name,

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

ENCODING METHOD AND SYSTEM FOR REDUCING INTER-SYMBOL INTERFERENCE EFFECTS IN TRANSMISSION OVER A SERIAL LINK

the specification of which (check one) _X_ is attached hereto or __ was filed on ____ as Application No. _____.

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose all information which is material to patentability as defined in 37 CFR § 1.56.

I hereby claim foreign priority benefits under 35 U.S.C. § 119(a)-(d) or § 365(b) of any foreign application(s) for patent or inventor's certificate, or § 365(a) of any PCT International application which designated at least one country other than the United States, listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Prior Foreign Application(s)			Priority Claimed Yes	No
Number	Country	Day/Month/Year Filed	____	____
Number	Country	Day/Month/Year Filed	____	____

I hereby claim the benefit under 35 U.S.C. § 119(e) of any United States provisional application(s) below.

Application Number	Filing Date
Application Number	Filing Date

I hereby claim the benefit under 35 U.S.C. § 120 of any United States application(s), or § 365(c) of any PCT International application designating the United States, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of 35 U.S.C. § 112, I acknowledge the duty to disclose all information which is material to patentability as defined in 37 CFR § 1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application:

09/954,663	09/12/2001	Pending
Application Number	Filing Date	Status: Patented, Pending, Abandoned
Application Number	Filing Date	Status: Patented, Pending, Abandoned

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment or both, under 18 U.S.C. § 1001 and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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Citizenship USA

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Inventor's signature _____

Date

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Inventor's signature _____

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Inventor's signature _____

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Citizenship USA

Post Office Address P.O. Box 64395, Sunnyvale, CA 94088

Ex.1002 / Page 439 of 443
Intel Corp. et al

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment or both, under 18 U.S.C. § 1001 and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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Inventor's signature _____

Date

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Citizenship KOREA

Post Office Address 1657 Ontario Drive, #12, Sunnyvale, CA 94087

Please type a plus sign (+) inside this box

PATENT APPLICATION SERIAL NO. _____

U.S. DEPARTMENT OF COMMERCE
PATENT AND TRADEMARK OFFICE
FEE RECORD SHEET

01/09/2002 MAHMED1 00000024 10036234

01 FC:101	740.00 OP
02 FC:102	84.00 OP
03 FC:103	990.00 OP

PTO-1556
(5/87)

*U.S. GPO: 2000-468-987/39595

PATENT APPLICATION FEE DETERMINATION RECORD
Effective October 1, 2001

Application or Docket Number: 511-1000

CLAIMS AS FILED - PART I

	(Column 1)	(Column 2)
TOTAL CLAIMS	75	
FOR	NUMBER FILED	NUMBER EXTRA
TOTAL CHARGEABLE CLAIMS	75 minus 20=	* 55
INDEPENDENT CLAIMS	4 minus 3 =	* 1
MULTIPLE DEPENDENT CLAIM PRESENT		☐

* If the difference in column 1 is less than zero, enter "0" in column 2

SMALL ENTITY TYPE ☐		OR	OTHER THAN SMALL ENTITY	
RATE	FEE		RATE	FEE
BASIC FEE	370.00	OR	BASIC FEE	740.00
X$ 9=		OR	X$18=	990
X42=		OR	X84=	84
+140=		OR	+280=	—
TOTAL		OR	TOTAL	

CLAIMS AS AMENDED - PART II

AMENDMENT A

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	*	Minus	**	=
Independent	*	Minus	***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				☐

SMALL ENTITY		OR	OTHER THAN SMALL ENTITY	
RATE	ADDITIONAL FEE		RATE	ADDITIONAL FEE
X$ 9=		OR	X$18=	
X42=		OR	X84=	
+140=		OR	+280=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

AMENDMENT B

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	*	Minus	**	=
Independent	*	Minus	***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				☐

RATE	ADDITIONAL FEE		RATE	ADDITIONAL FEE
X$ 9=		OR	X$18=	
X42=		OR	X84=	
+140=		OR	+280=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

AMENDMENT C

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	*	Minus	**	=
Independent	*	Minus	***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				☐

RATE	ADDITIONAL FEE		RATE	ADDITIONAL FEE
X$ 9=		OR	X$18=	
X42=		OR	X84=	
+140=		OR	+280=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20."
***If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3."
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

CLAIMS ONLY

SERIAL NO.	FILING DATE
	1-8-02

APPLICANT(S)

CLAIMS

	AS FILED		AFTER 1st AMENDMENT		AFTER 2nd AMENDMENT	
	IND.	DEP.	IND.	DEP.	IND.	DEP.
1	1					
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4		1				
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49		1				
50		1				
TOTAL IND.						
TOTAL DEP.						
TOTAL CLAIMS						

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	IND.	DEP.	IND.	DEP.	IND.	DEP.
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55		1				
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TOTAL IND.	4		4			
TOTAL DEP.	71		75			
TOTAL CLAIMS	75		79			

* MAY BE USED FOR ADDITIONAL CLAIMS OR ADMENDMENTS

FORM PTO-2022 (1-98)

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*U.S. GPO: 1998-443-593/89152