

A New Route to Zero-Barrier Metal Source/Drain MOSFETs

Daniel Connelly, Carl Faulkner, D. E. Grupp, and J. S. Harris

Abstract—A new method for dramatically lowering the Schottky barrier resistance at a metal/Si interface by interposing an ultrathin insulator is demonstrated for the first time, with thermionic barriers less than those reported to date with silicides. Results with Er and near-monolayer thermal SiN_x at the interface are consistent with simulations of effective metal Fermi level separations from the silicon conduction band of 0.15 V for *n*-type Si and 45 mV for *p*-type Si. Simulations of advanced metal source/drain (S/D) ultrathin-body CMOS devices in comparison with competitive doped S/D devices show a significant performance advantage with a barrier to the conduction band of up to 0.1 V.

Index Terms—Nanotechnology, Schottky barriers, Schottky diodes, Schottky logic circuits, Schottky logic devices, silicon-on-insulator (SOI) technology.

I. INTRODUCTION

METAL source/drain (S/D) MOSFETs promise to bypass the scaling limitations of doped S/D profile control, sheet resistance, and contact resistivity. One option, the Schottky S/D field-effect transistor, uses a metal layer in direct contact with Si channel. Schottky S/D technology, with PtSi for PFETs and ErSi_{1.7} for NFETs yielding the best results so far, has been used on a range of devices, including bulk FETs [1], thin-body SOI [2], [3], and FinFETs [4].

However, the challenge has been to realize a sufficiently low band offset between the metal to the channel [5]. Silicide Schottky S/D devices continue to be performance-limited by the thermionic barrier [6], with barrier heights of 0.24 V for both PMOS [2] and NMOS [7].

As we will show below, the critical barrier height for metal S/D performance to surpass that expected for future doped S/D technologies, in the example of dual-gate ultrathin-body CMOS, is approximately 0.1 V to 0.15 V.¹ To date, Schottky S/D technologies have fallen short of this target. In this work, we present experimental results which show a lower thermionic barrier than has been achieved with silicides.

The approach we use is to interpose an ultrathin insulator between the metal and the silicon. An insulator of a thickness sufficient to block the penetration of metal states which cause pin-

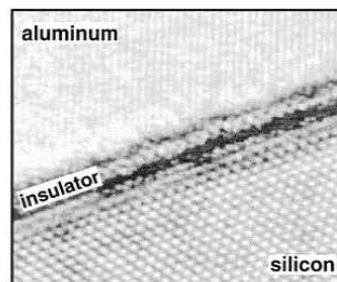


Fig. 1. Transmission electron micrograph of an Al/SiN_x/Si junction, showing the ultrathin interfacial layer.

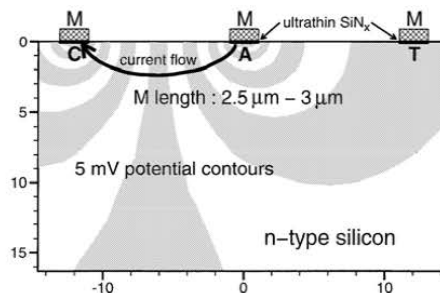


Fig. 2. Schematic cross section of metal/*n*-type Si junction structure. All contacts are metal (M). Current is sent into the "anode" (A) and taken out of the "cathode" (C). Voltage is measured with the "tap" (T), from which the voltage across the anode junction can be determined. There is some voltage drop associated with current transport through the Si in the vicinity of the contact, essentially an extrinsic resistance. In actual devices, the metal overlapped a field SiO₂ layer in the vicinity of the contact, and contact-to-contact separation was 16 μm center to center. Devices were also made without the ultrathin SiN_x.

ning in the Si, yet less than a thickness which yields a substantial tunneling resistance to free carriers, dramatically lowers the resistance of metal/silicon contacts. Using this approach, results consistent with simulations of barriers to the conduction band of less than 0.2 V were achieved. With Er, results consistent with simulations of an effective metal Fermi level separation from the Si conduction band of only 45 mV for Er on *p*-type Si, and approximately 0.15 V with Er on *n*-type Si, were observed.

II. EXPERIMENT

Two device types were considered here. The first is a contact between a test metal and doped silicon, with or without an interfacial insulator (see, for example, Fig. 1). A schematic of the test structure is shown in Fig. 2. Current was sent into the anode and extracted from the cathode. Junction voltage was measured

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¹We will later publish work which demonstrates an approach to extend this target barrier height.

between the anode and the tap. This approach reduces the effective substrate resistance versus a simple measurement between the anode and the wafer backside. The contours of constant potential show an effective substrate series resistance between the anode and the tap, due to their lateral separation. Typical junctions were $2\ \mu\text{m} \times 10\ \mu\text{m}$ drawn, with wet etching of the contacts increasing each dimension by approximately $0.5\text{--}1\ \mu\text{m}$. Junctions were spaced $16\ \mu\text{m}$ center to center.

Yb S/D transistors were also fabricated, processed on SOITEC bonded silicon-on-insulator wafers, with $340\ \text{nm}$ of $14\text{--}22\text{-}\Omega\text{-cm}$ p-type Si on a 400-nm buried SiO_2 . Before mesa formation, a 290-nm cap SiO_2 was grown, leaving $210\ \text{nm}$ of silicon. For simplicity in processing, back-gating was used, with the $5\text{--}10\text{-}\Omega\text{-cm}$ p-type substrate acting as the gate. For forward gate biases, the substrate was thus essentially in accumulation. The thick gate oxide generated a relatively uniform inversion layer in the channel, allowing a less ambiguous interpretation of measured results.

III. JUNCTIONS

A. Effect of Interfacial Nitride

Fig. 3 shows the result of applying an insulator, in this case thermal SiN_x , to the interface between Al and Si.² The nitride was grown at a fixed temperature, with time variable. Plotted in the figure is the incremental resistance interpolated for zero junction bias. As the insulator thickness is increased, resistance dramatically decreases. However, a minimum is reached; for thicker nitrides, resistance increases.

Results with $\text{Er/SiN}_x/\text{n}^+\text{Si}$, where Er has a substantially lower bulk workfunction than Al, are shown in Fig. 4 for a variety of interfacial SiN_x layers. In this experiment, only a few growth times were used. However, the wafer was not rotated, and nonuniform gas flows in the system yielded significant variation in nitride thickness across each wafer. In the figure, a different presentation is used from Fig. 3. The x axis shows two parameters—in Fig. 3(a), the symmetry of the junction $I\text{--}V$ curve is represented as the ratio of forward to reverse voltage magnitudes needed to yield a current magnitude of $50\ \text{mA}$. In Fig. 3(b), the location of the $I\text{--}V$ inflection point is used. The symmetry provides an indication of the current-limiting mechanism. In each case, there is a transition from a thermionic-barrier-limited to an insulator-tunneling-limited behavior, with the minimum resistance in devices with nearly symmetric $I\text{--}V$. In the thermionic limit, the metal Fermi level is pinned significantly below the conduction band of the n^+Si and, thus, forward biased current occurs for a positive junction voltage. When current is limited by the interfacial insulator, however, it is generally higher for negative voltages from the metal to the substrate.

The lowest measured resistance values in Fig. 3 are consistent with substrate-limited resistance for these samples. Thus the specific contact resistivity cannot be directly determined

²Thermal SiN_x was chosen for a variety of factors, including thermal stability, clear applicability to conventional CMOS processing, availability of essentially self-limited growth, and a barrier to both conduction and valence bands sufficiently small to allow electron and/or hole tunneling but sufficiently large to substantially block the formation of metal-induced gap states (MIGS) [8], [9].

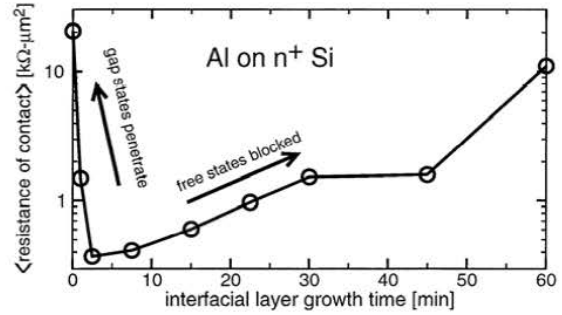


Fig. 3. Measured Al contacts on n^+Si show a clear minimum. As interfacial treatment is increased, resistance drops sharply as gap states are blocked and the Fermi level is liberated. A further increase in the interfacial thickness, however, results in increased resistance due to the blocking of free carriers. Tunneling in Si due to high substrate doping reduces the contrast of thermionic barrier shifts. The wet-etched contacts are approximately $3\ \mu\text{m} \times 21\ \mu\text{m}$.

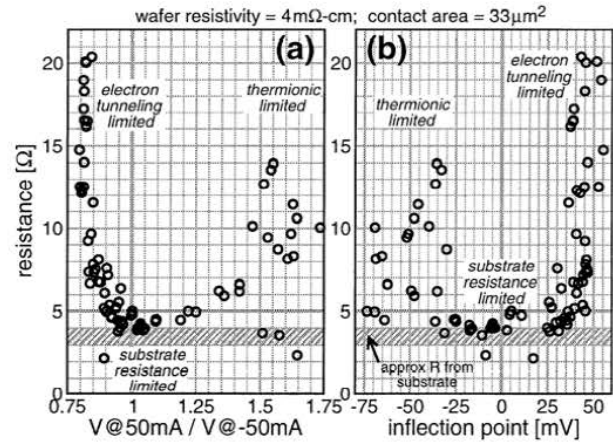


Fig. 4. Measured $\text{Er/SiN}_x/\text{n}^+\text{Si}$ for a variety of SiN_x layers. The simulated substrate resistance component is indicated as a y -axis band, dependent on degree of contact overetch. The wet-etched contacts are approximately $3\ \mu\text{m} \times 11\ \mu\text{m}$. (a) As the ratio of forward to reverse $|V| = 50\ \text{mA}$ crosses unity, the transport goes from tunneling limited, through substrate resistance limited, and toward thermionic limited. (b) A similar trend is observed using the $I\text{--}V$ inflection point.

from the measurements. These results suggest the promise of ultra-low resistance contacts to doped silicon as an application of this technology.

More lightly doped wafers, due to the reduction in thermionic field emission relative to highly doped wafers, are more sensitive to the metal/Si thermionic barrier. Fig. 5 shows how inserting an insulator can dramatically reduce the resistance of a metal/Si contact with Si doping approximately $1.7 \times 10^{16}/\text{cm}^3$ n-type. Al/Si junctions experience up to a $10\,000$ -fold decrease with the use of SiN_x at the interface. Yb, like Er, has a substantially lower bulk workfunction than Al. Yb/Si junctions go from thermionic-emission-limited current with a direct contact, to substrate-limited current with the addition of the interfacial SiN_x layer. These junction results are consistent with a thermionic barrier of at most $0.2\ \text{V}$, significantly less than $0.24\ \text{V}$ reported for $\text{ErSi}_{1.7}/\text{Si}$ [7].

A transmission electron micrograph of the interface of an Al/ SiN_x /Si junction, with thicker-than-optimal SiN_x , is shown in Fig. 1. The SiN_x layer is only a few monolayers thick. This

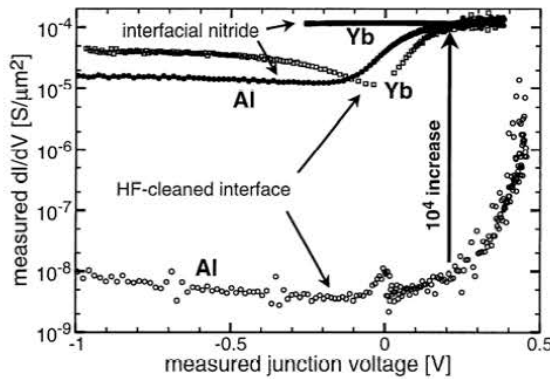


Fig. 5. Measured data showing 10^4 increase in conductance at small positive bias when an ultrathin nitride is formed before Al deposition on n-type Si. The same experiment with Yb and an interfacial nitride results in substantially improved conductance, limited by the substrate resistance.

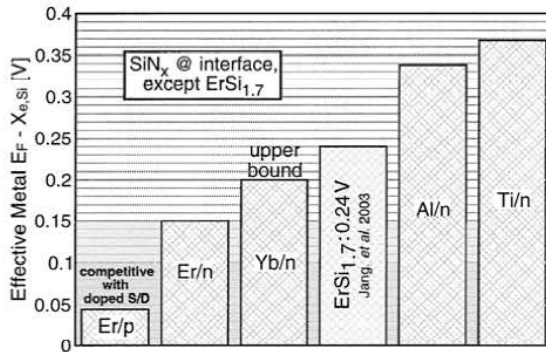


Fig. 6. Extracted workfunctions for a variety of metal/ SiN_x /Si junctions, with moderately doped n-type substrates. The Yb value is an upper bound, as the measured junction I - V was limited by the relatively large substrate resistance used in that experiment. Er results are shown for both n-type and p-type Si; the latter yielding results consistent with simulations of a Fermi level separation to the Si conduction band of 45 mV. The target for performance competitive with a doped S/D technology for UTB-SOI applications is shaded; we will later present work which extends this region to higher barriers.

shows that optimal interfacial nitrides are at most a few monolayers.

B. Barrier Heights

A variety of metal/ SiN_x /Si junctions were fabricated, with substrate doping from $1.7 \times 10^{16}/\text{cm}^3$ to $1.5 \times 10^{17}/\text{cm}^3$ n-type, with interfacial SiN_x thicknesses estimated at 1–2 monolayers. Dessis 8.5.5 [10], using the thermionic field emission model of Jeong *et al.* [11], was used to find a workfunction which closely fit measured I - V characteristics. Given the difficulty of determining the bandstructure of the near-monolayer interfacial nitride layers used, the interfacial nitride was not modeled—the metal was considered to be in intimate contact with the substrate. Indeed, attempts to model the WKB-barrier of the interfacial layer degraded the quality of the agreement of simulations to experiment.

Effective barrier heights extracted for the tested metals, with near-optimal nitrides, are plotted in Fig. 6. Also shown in the

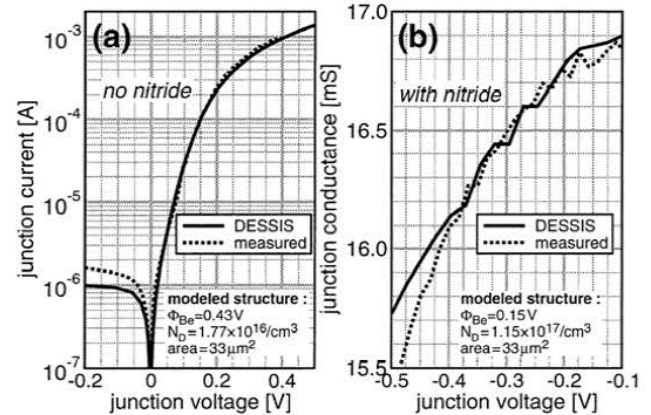


Fig. 7. Example of workfunction fitting, using Dessis to model the measured I - V . Note substrate doping, and therefore substrate-limited resistance, differs in the two samples. (a) Er with an H_2 -annealed interface. (b) Er with SiN_x at the interface.

figure is the result reported for $\text{ErSi}_{0.17}/\text{Si}$ [7]. Er results are shown for both n-type and p-type Si, with the latter yielding a smaller effective metal Fermi level offset relative to the Si conduction band, as determined by Dessis simulations. As will be shown later, the target for performance competitive with doped S/Ds in 25-nm dual-gate technology is 0.1–0.15 V, depending on the assumed doped S/D contact resistivity.³ An example of a fit, as applied to Er, is shown in Fig. 7. With the nitride at the interface, the contact is nearly ohmic; the thermionic resistance is largely masked by the substrate resistance, due to the small barrier height. While resolution of the extracted workfunction is limited, increasing the barrier results in an increasing dependence of the conductance on the voltage between the anode and tap. By a simulated barrier of 0.2 V, the disagreement between simulation and experiment is substantial.

With p-type substrates, current was sent from the frontside contact to the wafer backside, with voltage measured across the same two terminals. Results for Er, with nitride at the interface, are shown in Fig. 8. Measured data are matched by a simulation with a metal Fermi level only 45 mV from the Si conduction band. This is even closer to the conduction band than was extracted for the n-type wafer. Work is ongoing to reduce the relatively high degree of generation/recombination current observed in this device; a possible contributing factor is the overlap by the Er of the field oxide, which can deplete and even invert the Si at the junction perimeter. A surface recombination velocity of $v_{\text{rec}} = 10^3$ cm/s was assumed. Lower values have little effect, while substantially larger values would imply an even lower effective metal workfunction.

IV. FERMI-LEVEL DEPINNING

Pinning in metal/semiconductor contacts has been shown to be caused by intrinsic, metal-induced gap states (MIGS), in addition to defects associated with physical nonidealities of the interface such as dangling bonds [12]. For metal/Si contacts, this pinning was shown to approximately result in an effective metal

³See Footnote 1.

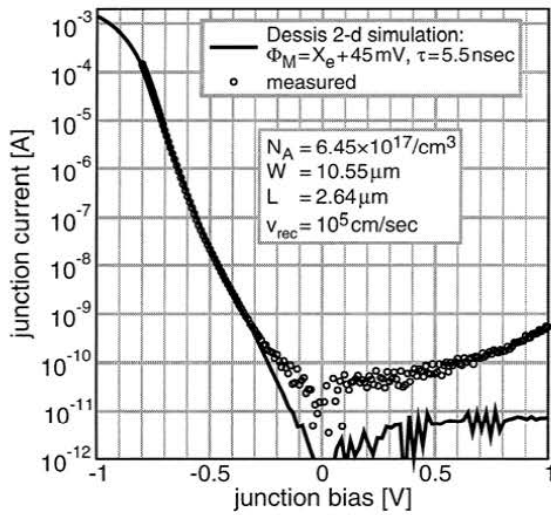


Fig. 8. Fit to Er/SiN_x/p-type Si junction data, indicating a workfunction consistent with a barrier to the conduction band of only 45 mV. Width (*W*) and length (*L*) were measured via scanning electron microscopy. Substrate doping (*N_A*) was determined from measured substrate resistivity and the Dessis bulk Si mobility model.

workfunction $\Phi_{M,eff}$ which is pulled from the ideal value Φ_M , toward Φ_{CNL} , the charge neutral level associated with Si

$$\Phi_{M,eff} = S\Phi_M + (1 - S)\Phi_{CNL} \quad (1)$$

where $S \approx 17\%$ [13]. This yields an effective barrier height between the metal and the Si conduction band

$$\Phi_{Be} = \Phi_{M,eff} - X_e \quad (2)$$

where X_e is the Si electronegativity. Data from [9] showed larger S , and therefore less pinning, associated with metal/insulator interfaces.

This reduction in the Fermi-level pinning when the metal is in contact with an insulator opens the possibility to reduce the effective barrier between a metal and Si. With an insulator thin enough to readily allow tunneling of free carriers, but thick enough to block the MIGS in the Si and to provide a low-defect interface, a reduced effective barrier metal S/D can be achieved. A schematic band diagram illustrating this effect is shown in Fig. 9. When the metal is in direct contact with the interface, represented in Fig. 9(a), a substantial charge dipole forms in the Si due to the influence of the metal. Imposing an interfacial insulator reduces this dipole, thus effectively reducing the thermionic barrier associated with the Si conduction band. However, it does so by introducing a thin barrier through which electrons must tunnel to reach the Si conduction band.

The resistance in such a junction is the result of a competition between a thicker tunnel barrier and a lower thermionic barrier. It is apparent from our experimental results that the reduction in current due to the tunnel barrier presented by the insulator is less than the increase in current due to the significantly lowered thermionic barrier.

One possible explanation is that states at the pinning point within the Si bandgap are blocked by the insulator more strongly than states at the Si conduction band. This is because the tun-

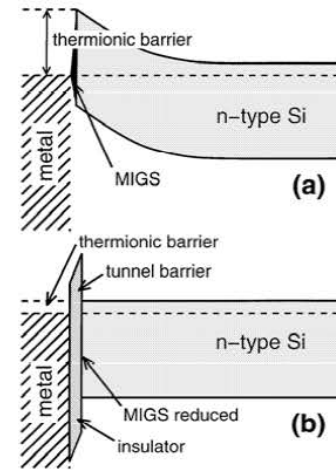


Fig. 9. Band diagrams of metal/silicon contacts with and without interfacial insulators. (a) The metal is in direct contact with the Si. The Si in the direct vicinity of the metal acquires a dipole moment due to the influence of metal-induced gap states, generating a barrier to electron injection. (b) An ultrathin insulator at the interface trades a reduction in the thermionic barrier for a tunneling barrier. The key is to reduce the thermionic barrier while limiting the tunneling barrier.

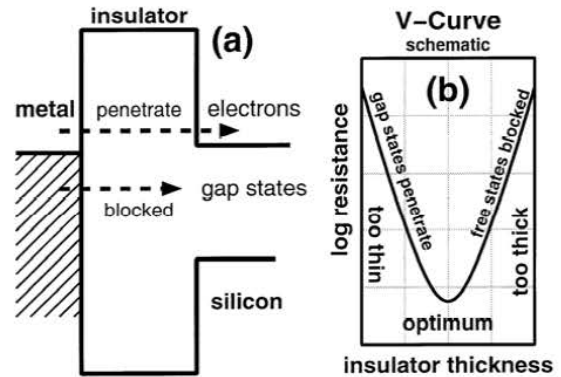


Fig. 10. Tunneling through an interfacial insulator. (a) The band diagram shows deep states face a larger minimum barrier than do free carrier states, and thus are more rapidly attenuated (indicated by arrow length), allowing free carriers to tunnel while blocking the MIGS. (b) The optimum insulator thickness is where the gap states are effectively blocked while free carrier tunneling is still sufficient.

neling probability is lower (exponentially) further from the top of a barrier. Thus, the insulator prevents metal states from penetrating into the Si gap and producing MIGS, while minimally blocking the flow of electrons into or out of the Si conduction band. This is schematically shown in Fig. 10(a). The challenge, illustrated in Fig. 10(b), is to avoid insulators which are too thin, allowing MIGS to penetrate into the Si, or which are too thick, substantially blocking the transport of free carriers.

The reduction in resistance with increasing insulator thickness, for thin insulators, may also be explained by the possibility of a rapid depinning of the effective metal Fermi level due to the low density of states of MIGS at the neutral point. This may result in the thermionic barrier dropping rapidly with small changes in insulator thickness. Thus, the current flow is enhanced by the lower barrier more rapidly than it is attenuated by the tunnel barrier presented by the insulator.

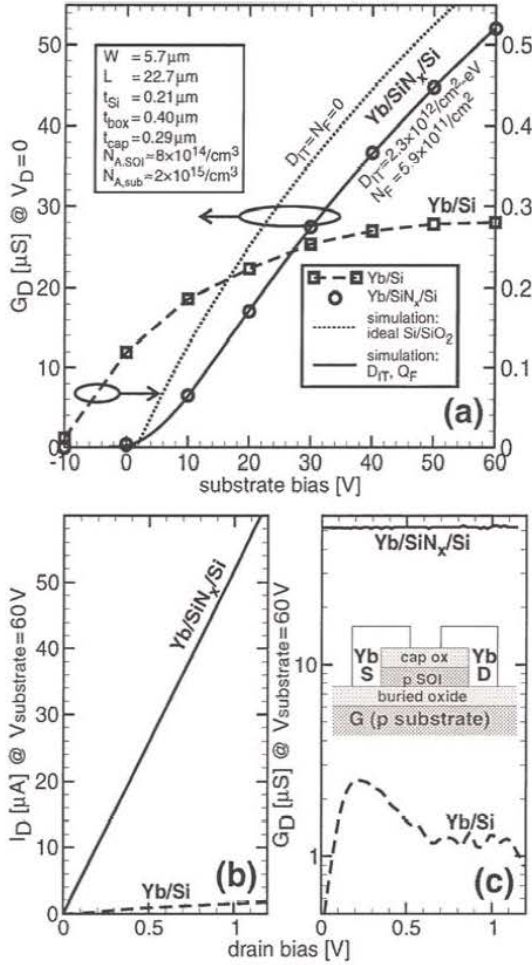


Fig. 11. Results from a Yb S/D test transistor, showing transition from S/D-limited (dashed) to channel-limited (solid) resistance when SiN_x is added to the metal/Si interface. (a) Output conductance at $V_D = 0$ versus gate voltage. The measured data for the SiN_x interface is plotted as symbols, with lines showing device simulation with and without interface modeling. The simulation assumes negligible resistance associated with the interfacial SiN_x. (b) Drain current versus drain voltage. Low, nonlinear current in no-nitride device gives way to a linear, higher current with SiN_x at the interface. (c) Output conductance dependence on drain voltage, showing linearity more clearly. Device schematic is inset.

Recall from Fig. 8 that the barrier to the conduction band was less for p-type substrates than for n-type. This is consistent with a higher surface electric field reducing the charge at the insulator/Si interface, thus reducing the MIGS dipole moment across the interfacial insulator.

V. TRANSISTOR MEASUREMENTS AND DISCUSSION

Input characteristics of Yb transistors are shown in Fig. 11(a). Key parameters include: channel width $W = 5.7 \mu m$, channel length $L = 22.7 \mu m$, silicon thickness $t_{Si} = 0.21 \mu m$, buried oxide thickness $t_{box} = 0.40 \mu m$, SOI doping $N_{A,SOI} \approx 8 \times 10^{14}/cm^3$ p-type, and substrate doping $N_{A,sub} \approx 2 \times 10^{15}/cm^3$ p-type. The g_D versus V_G characteristics of the device with nitride at the interface are well modeled by a Prophet [14] simulation of a zero-barrier device, using the mobility model of

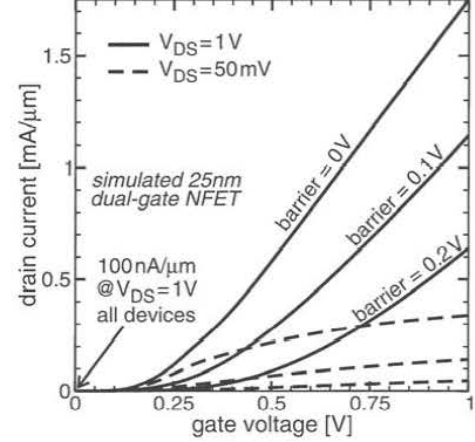


Fig. 12. Predicted performance of 25-nm dual-gate transistor with 3-nm S/D underlap, 1-nm gate oxide, and 6-nm Si for various S/D barriers.

[15], with an interface state density of $2.3 \times 10^{12}/eV - cm^2$ and a fixed charge density of $7.2 \times 10^{11}/cm^2$. Rather than use the interface charge scattering model from [15], mobility was uniformly scaled by approximately 50% to match the measured data. The reduction in slope with increasing V_G is consistent with mobility reduction with transverse electric field [16], as is evident in the agreement with the simulation. The measured results are consistent with a simulation in which the interfacial SiN_x has a negligible contribution to device resistance.

The output characteristics of the same device are shown in Fig. 11(b) and (c). The addition of the interfacial SiN_x takes the device from thermionic-barrier-limited (g_D a strong function of V_D) to channel-resistance-limited (g_D a weak function of V_D) current. As with the Yb/SiN_x/n-type Si junction results, Dessis simulations shows the SiN_x data are consistent with a thermionic barrier of no greater than 0.2 V; larger barriers yield a significant increase in the V_D dependence of g_D . In contrast, the direct Yb/Si contacts yield nonlinear behavior consistent with current limited by thermionic emission or thermionic field emission, with notable S/D asymmetry.

The S/D of the interface is a dry-etched (110) The S/D interface of the Yb FET is a dry-etched (110) sidewall, rather than the pristine (001) surface used in planar junctions. The success of the Yb/SiN_x/Si S/Ds testifies to the robustness of the process.

VI. TRANSISTOR SIMULATIONS

Fig. 12 shows simulations of 25-nm dual-gate NFETs for various effective metal S/D workfunctions. The simulations were performed with Dessis, in a manner similar to that used with the junctions. The mobility model of [17] was used, with velocity saturation parameters calibrated to Monte Carlo simulations of sub-100-nm channels [18]. The threshold voltage was set, via an assumed tunable-workfunction metal gate technology, to maintain an off-current of 100 nA/ μm . To maintain a saturation current of at least 1 mA/ μm for a supply voltage of 1 V, simulations predict the thermionic barrier should be no greater than 0.1 V, assuming no performance-limiting resistance associated with tunneling through the interfacial

layer.⁴ Work is ongoing to demonstrate barriers consistent with this target.⁵

Dessis NAND-chain mixed-mode simulations were performed for a 25-nm nominal-gate-length dual-gate technology, with fan-out of two. PFETs were assumed to have an S/D thermionic barrier to the valence band equal to the NFET S/D thermionic barrier to the conduction band; thus, it was assumed a complementary metal S/D process was available. Gate workfunctions for NFETs and PFETs were independently adjusted to yield a leakage current in $1\text{-}\sigma$ subnominal length devices of $20\text{ nA}/\mu\text{m}$, with an assumed gate length σ of 4 nm. Performance was assessed using $2\text{-}\sigma$ supernominal gate length transistors.⁶ These simulations are an extension of those presented in [21]. More comparisons of metal S/D and doped S/D devices, including both dual-gate and single-gate silicon-on-insulator CMOS, is available in [22]. Circuit delay results are shown in Fig. 13. A schematic of the two-stage NAND chain used for the device benchmarking is in the figure inset.

With S/D placement optimized, metal S/D devices with a barrier of 0.1 V show a clear advantage over doped S/D devices with circa 2008 contact resistivity [19]. Zero-barrier metal S/D CMOS is more than 50% faster than that with even circa 2015 doped S/D contact resistivity. An advantage in performance can be traded off for reduced power operation [23]. With a larger thermionic barrier of 0.2 V, still significantly lower than that achieved to date with silicide S/D devices, performance of the metal S/D technology lags that of the doped S/D technology with the circa 2015 contact resistivity.

VII. CONCLUSION

The main challenge to metal S/D technology is reducing the S/D metal-to-channel barrier to near zero. For 25-nm dual-gate CMOS, simulations show a barrier of 0.1 V or less results in performance comparable to or better than doped S/D technology with circa 2015 contact resistivity. An approach to depinning the Fermi level, and therefore to reducing the barrier, is an ultrathin interfacial insulator. This yields a substantially reduced, but

⁴Modeling of both the Yb/SiN_x/Si transistor and of the M/SiN_x/Si junctions showed that for near-optimal nitrides, the characteristics are well modeled with an effective metal workfunction, without an explicit consideration of the effect of tunneling through the ultrathin insulator. Of course, as the insulator is made thicker, this approximation becomes an upper bound prediction on performance, presenting a necessary but insufficient performance target.

⁵The effective thermionic barriers into an ultrathin-body FET channel, and across a planar junction, may differ. Guo *et al* [5] point out that the electron ground state energy in the Si channel will be above the conduction band minimum due to confinement. However the energy of the MIGS will also be affected by confinement. Crystal orientation may also play a role if (011) S/Ds are used. Therefore, while planar junctions, and large-scale MOSFETs, provide guidance, barriers associated with ultrathin-body channels must still be independently determined. In this work, thermionic field emission in ultrathin-body devices is modeled with the light transverse electron effective mass, under the assumption the sixfold conduction band degeneracy is reduced to twofold $\Delta_{\perp}$ degeneracy by the confinement, where the $\Delta_{\perp}$ valleys exhibit the transverse effective mass in the channel plane. In planar junctions, the isotropic effective mass is used.

⁶Gate lengths were assumed to be normally distributed with standard deviation $\sigma = 4$ nm about a mean length of 25 nm. All forms of device variability, including silicon thickness variation, width variation, gate oxide thickness variation, etc., were abstracted into gate length variation. The motivation behind this analysis is the assumption that leakier-than-average devices disproportionately contribute to net static leakage current, while slower-than-average devices will dominate the clock-limiting circuit path [20].

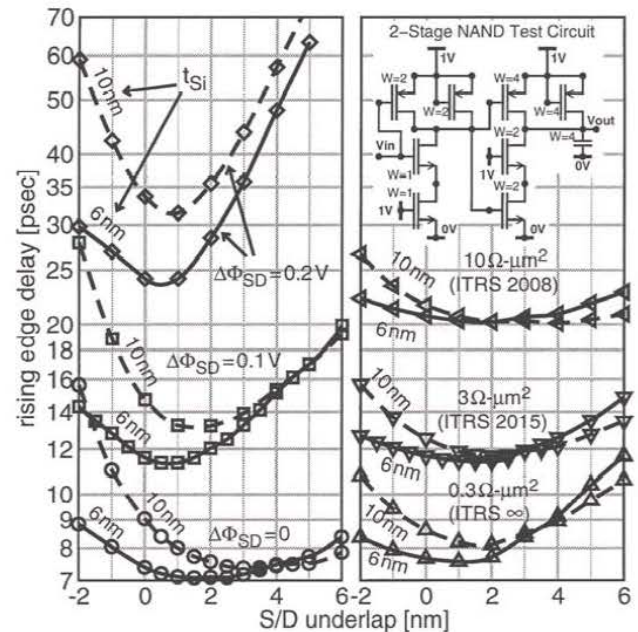


Fig. 13. Circuit delays simulated for NAND chains of 25-nm dual-gate CMOS (see inset schematic) versus S/D offset for metal and doped S/D, with $t_{Si} = 6$ nm or 10 nm. NFET $\Phi_{SD} = X_c + \Delta\Phi_{SD}$, PFET $\Phi_{SD} = X_h - \Delta\Phi_{SD}$. Metal S/D shows a performance advantage for $\Delta\Phi_{SD} < 0.1$ V, assuming 2015 projected $\rho_{SD} = 3 \Omega - \mu m^2$ [19]. Ultralow resistance contacts (e.g., $0.3 \Omega - \mu m^2$) are needed if doped S/D is to be competitive.

still significant, thermionic barrier with Al/Si. However, lower workfunction metals like Yb and Er yield thermionic barriers with the Si conduction band of less than or equal to 0.2 V, significantly less than what has been reported with silicides. Results of Er on p-type Si were consistent with simulations of an effective metal Fermi level only 45 mV from the Si conduction band, while Er on n-type Si matched simulated results for a barrier of 0.15 V. Improvement upon these early results may be possible. For example, if the insulator is sufficiently nonuniform, localized Fermi level pinning in the thin regions may occur, increasing the overall effective barrier. Using interfacial insulators, the considerable potential of metal S/Ds may finally be achieved.

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