2022-1539 (Lead), 2022-1540, 2022-1541, 2022-1542

United States Court of Appeals for the Federal Circuit

SAMSUNG ELECTRONICS CO., LTD.,

Appellant,

v.

ACORN SEMI, LLC,

Appellee.

APPEALS FROM THE UNITED STATES PATENT AND TRADEMARK OFFICE, PATENT TRIAL AND APPEAL BOARD IN INTER PARTES REVIEW NOS. IPR2020-01206, IPR2020-01207, IPR2020-01279, IPR2020-01282

OPENING BRIEF OF APPELLANT SAMSUNG ELECTRONICS CO., LTD.

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U.S. PATENT NO. 9,905,691

REPRESENTATIVE CLAIM 6 (CORRECTED)

6. The structure of claim 3, wherein the metal oxide layer comprises an oxide of titanium.

U.S. PATENT NO. 10,090,395

REPRESENTATIVE CLAIM 11

11. The electrical junction of claim 1, wherein said metal oxide comprises an oxide of titanium.

REPRESENTATIVE CLAIM 17

17. An electrical junction, comprising:

a source or drain of a transistor, said source or drain comprising a semiconductor,

a metal electrical contact to said source or drain, and

an interface layer disposed between and in contact with said source or drain and said metal electrical contact, said source or drain being electrically connected to said metal electrical contact through said interface layer and said interface layer comprising an oxide of titanium and an oxide of the semiconductor.

CERTIFICATE OF INTEREST

Pursuant to Federal Circuit Rules 26.1, 28(a)(1), and 47.4, counsel for appellant certifies the following:

1. The full name of every entity represented in this case by me is:

   Samsung Electronics Co., Ltd.

2. The name of every real party in interest, if that entity is not the real party in interest, is:

   Samsung Electronics America, Inc.
   Samsung Semiconductor, Inc.
   Samsung Austin Semiconductor, LLC

3. All parent corporations and every publicly held corporation that owns 10 percent or more of the stock of the entity represented by me are:

   N/A

4. The names of all law firms, partners, and associates that have not entered an appearance in this appeal, and appeared for the entity in the trial court or are expected to appear for the entity in this court are:

   Desmarais LLP: Theodoros Konstantakopoulos; Kevin K. McNish (former); Christian Dorman (former)

5. The title and number of any case known to counsel to be pending in this or any other court or agency that will directly affect or be directly affected by this court's decision in the pending appeal include:

   Acorn Semi, LLC v. Samsung Electronics Co., Ltd., No. 2022-1499 (Fed. Cir.)
   Acorn Semi, LLC v. Samsung Electronics Co., Ltd., Civil Action No. 2:19-cv-347 (E.D. Tex.)

6. Provide any information required under Fed. R. App. P. 26.1(b) (organizational victims in criminal cases) and 26.1(c) (bankruptcy case debtors and trustees):

N/A

Dated: June 24, 2022 /s/ *Cosmin Maier*

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STATEMENT OF RELATED CASES

No appeal in or from the same proceedings before the USPTO Patent Trial and Appeal Board ("Board") was previously before this Court or any other appellate court. Acorn Semi, LLC ("Acorn") has asserted U.S. Patent Nos. 9,905,691 (the "'691 patent") and 10,090,395 (the "'395 patent") (collectively, the "Challenged Patents") in the following case:

Acorn Semi, LLC v. Samsung Electronics Co., Ltd. et al., No. 2:19-cv-0347-JRG (E.D. Tex.), on appeal as No. 2022-1499 (Fed. Cir.).

Counsel for Appellant Samsung Electronics Co., Ltd. ("Samsung") are not aware of any other case in this Court, in any other court, or before the Board that will directly affect or be directly affected by this Court's decision in this appeal.

INTRODUCTION

The Challenged Patents are directed to multilayer structures comprising, from top to bottom, metal, metal oxide, semiconductor oxide, and semiconductor. Across four *inter partes* review ("IPR") proceedings, the Board found numerous challenged claims unpatentable. But the Board also found a subset of the challenged claims not unpatentable. In doing so, the Board made fundamental mistakes in each proceeding.

In IPR2020-01206 and IPR2020-01207, the Board made a critical claim construction error. Each challenged claim requires a "metal oxide" layer. Samsung argued that the claimed "metal oxide" lacks written description support in certain parent applications, such that the challenged claims are not entitled to priority earlier than "Grupp '483,"[1] rendering Grupp '483 anticipatory prior art. The Board agreed that many of the challenged claims could not predate Grupp '483 for lack of written description of a "metal oxide" and, accordingly, found those claims unpatentable. But the Board interpreted a subset of the claims—which recite a "metal oxide" layer that "***comprises*** an oxide of titanium" (the "Comprises Claims")—to ***limit*** the metal oxide layer to ***only*** an oxide of titanium, to the exclusion of any metal oxides other than oxides of titanium. In the Board's view, that narrow construction solved the

[1] U.S. Patent No. 7,176,483. Appx3141-3160.

written description issue with respect to the Comprises Claims. But it "is well understood in patent law" that the words *comprises* and *comprising* mean "including ***but not limited to***." *Exergen Corp. v. Wal-Mart Stores, Inc.*, 575 F.3d 1312, 1319 (Fed. Cir. 2009).[2] Accordingly, the Comprises Claims, properly construed, encompass a "metal oxide" layer that must include an "oxide of titanium" but that can ***also*** include the other metal oxides that the Board found were not described. Under the proper construction of "comprises," Grupp '483 is anticipatory prior art and this Court should reverse.

The Board made another error in IPR2020-01206. In its Final Written Decision ("FWD"), the Board correctly determined that certain challenged claims of the '691 patent are not enabled by any parent applications, and therefore those claims could not predate Grupp '483, rendering Grupp '483 anticipatory prior art. But when summarizing its conclusions regarding patentability, the Board overlooked its earlier finding that Grupp '483 ***is*** prior art and did ***not*** apply Grupp '483 as prior art to those claims. That oversight requires reversal.

In IPR2020-01279, the Board violated the Administrative Procedure Act ("APA") by sidestepping the parties' disputes regarding motivations to combine and instead relying on an irrelevant finding from a different IPR proceeding involving a

[2] All emphasis added unless otherwise noted.

different patent and different prior art. In particular, the Board relied on its finding in IPR2020-01264 (not one of the four IPRs at issue herein), that a prior art reference called "Kim"[3] does not support Samsung's proposed combination of the "Goodnick"[4] and "Taubenblatt"[5] references because Kim does not teach a "layer" of metal oxide or titanium oxide. But Samsung did not rely on Kim to teach a "layer" of metal oxide or titanium oxide. Instead, Samsung relied on Goodnick's and Taubenblatt's express teachings for that layer. The Board's analysis of Kim's disclosure of layers in another IPR is irrelevant. The Board dismissed Samsung's actual motivation to combine theory in a single sentence without analysis. That fails to comply with the APA and warrants remand.

Finally, in IPR2020-01282, the Board deviated from *KSR*'s flexible approach to obviousness and overlooked critical evidence. The Board made four errors. First, the Board improperly compared Samsung's proposed Goodnick-Taubenblatt combination to a purportedly superior structure taught by Kim. But obviousness "does not require that a particular combination must be the preferred, or the most

[3] U.S. Patent No. 4,845,050. Appx26846-26851.

[4] S.M. Goodnick et al., *Effects of a thin SiO2 layer on the formation of metal-silicon contacts*, 18 J. VAC. SCI. & TECH. 949 (1981). Appx26815-26821.

[5] M.A. Taubenblatt & C.R. Helms, *Silicide and Schottky barrier formation in the Ti-Si and the Ti-SiO_x-Si systems*, 53 J. APPLIED PHYS. 6308 (1982). Appx26827-26835.

desirable, combination described in the prior art in order to provide motivation for the [purported] invention." *In re Fulton*, 391 F.3d 1195, 1200 (Fed. Cir. 2004). The Board should have instead compared the advantages of the Goodnick-Taubenblatt combination to the structure that the combination modifies (Goodnick alone). Second, the Board erroneously found that Kim teaches away from ***ever*** using titanium as the metal layer in the claimed structures because the Board misread Kim and overlooked Acorn's expert's admission that using titanium in the claimed structures was "common[]." Appx28179 (65:16-24). Third, the Board improperly stopped its motivation analysis short when it could not compare—using numerical calculations and common units—the combination's electrical properties to those of Goodnick alone. But in doing so, the Board never reached the qualitative evidence and the background knowledge of a POSITA, as required by *KSR*. Fourth, for a subset of the challenged claims of the '395 patent (20-21 and 26-27), the Board never addressed Samsung's actual combination. In particular, the Board found no motivation to combine because it read Kim to teach away from using "pure titanium" as the metal layer of the claimed structures. Appx0213. But Samsung's combinations for claims 20-21 and 26-27 ***do not use*** pure titanium as the claimed metal layer—rather, those combinations use Kim's titanium/tungsten alloy, which the Board determined was superior to pure titanium. The Board never separately

addressed those titanium/tungsten alloy combinations. Those errors warrant remand.

JURISDICTIONAL STATEMENT

Samsung appeals from the Board's FWDs in Nos. IPR2020-01206, IPR2020-01279, IPR2020-01207, and IPR2020-01282. In those IPRs, Samsung challenged certain claims of the '691 and '395 patents after Acorn sued Samsung for infringement of claims 1-4, 6, 8, 10-13, 15-20, 22, and 25-30 of the '691 patent and claims 1-6, 8-9, 11-12, and 14-28 of the '395 patent in the Eastern District of Texas. Appx3623-3624. The Board had jurisdiction under 35 U.S.C. §§ 311-319. As summarized below, the Board held certain claims unpatentable and certain other claims not unpatentable:

IPR	Patent	FWD Date	Claims Found Unpatentable	Claims Found Not Unpatentable	Appendix
-1206	'691	1/12/2022	1-4, 13, 20, 22, 25	6, 8, 10-12, 15-19, 26-29	Appx0001-0052
-1279	'691	1/12/2022	1-4, 13	6, 8, 10-12, 15-20, 22, 25-29	Appx0111-0164
-1207	'395	2/9/2022	1-6, 8-9, 15, 16	11-12, 14	Appx0053-0104; Appx0105-0110
-1282	'395	2/9/2022	1-5, 8-9	6, 11-12, 14-28	Appx0165-0229; Appx0230-0236

Samsung filed timely notices of appeal on March 14, 2022. Appx0528-0551; 37 C.F.R. § 90.3(a)(1). This Court consolidated the appeals on March 21, 2022. D.I. 2. After the Board corrected its -1207 and -1282 FWDs, Samsung filed timely amended notices of appeal on April 28, 2022. Appx8898-8904; Appx24258-24264; *see also* Order, D.I. 13; 37 C.F.R. § 90.3(b)(1). This Court has jurisdiction under 35

U.S.C. § 141(c) and 28 U.S.C. § 1295(a)(4).

The remaining claims on appeal are claims 6, 8, 10-12, 15-19, and 26-29 of the '691 patent, and claims 11-12, 14, and 17-28 of the '395 patent (collectively, the "Challenged Claims"). Acorn asserted each of the Challenged Claims against Samsung in its infringement suit, including in Acorn's infringement contentions and expert reports. Appx3623-3624. Acorn narrowed the claims it elected to present at trial. Appx5826. The jury's infringement verdict and lump-sum award covering the '691 and '395 patents (Appx7886-7893) are not yet final because Samsung's appeal from that litigation is pending before this Court in No. 2022-1499. And Samsung has not received a license or covenant-not-to-sue from Acorn. Thus, Samsung has standing to appeal the Board's adverse determinations as to all Challenged Claims. *See, e.g.*, *Google LLC v. Conversant Wireless Licensing S.A.R.L.*, 753 F. App'x 890, 894-95 (Fed. Cir. 2018) (nonprecedential) (holding that appellants had standing where they had been sued for infringement); *Grit Energy Sols., LLC v. Oren Techs., LLC*, 957 F.3d 1309, 1320 & n.3 (Fed. Cir. 2020) (finding standing in part because appellee had previously sued appellant and did not stipulate not to sue).

STATEMENT OF THE ISSUES

I. In the -1206 and 1207 IPRs, for claims 6, 8, 10-12, 15-19, and 26-29 of the '691 patent and claims 11-12, and 14 of the '395 patent—dependent claims that recite a "metal oxide" layer that "***comprises*** an oxide of titanium" (collectively, the "Comprises Claims"):

A. Whether the Board incorrectly interpreted "comprises" to mean that the claimed "metal oxide" layer ***consists only of*** titanium oxide and ***excludes*** any metal oxides other than oxides of titanium, and whether Grupp '483 is prior art that anticipates the claims under the correct construction of "comprises"; and

B. Alternatively, whether the Board abused its discretion by refusing to consider Samsung's Reply arguments and evidence demonstrating that the Comprises Claims lack written description support in certain parent applications even under the Board's incorrect interpretation of "comprises."

II. In the -1206 IPR, for claims 18 and 26-29 of the '691 patent, whether the Board erred by neglecting to apply Grupp '483 as prior art in its anticipation analysis despite concluding in another portion of its FWD that Grupp '483 ***is*** prior art.

III. In the -1279 IPR, for claims 6, 8, 10-12, 15-19, and 26-29 of the '691 patent, whether the Board failed to provide an adequate explanation—as the APA

requires—for its determination that a POSITA would not have combined Goodnick with Taubenblatt.

IV. In the -1282 IPR:

A. For claims 6, 11-12, and 14-28 of the ’395 patent:

a. Whether the Board applied an incorrect legal standard by comparing the proposed combination to an allegedly superior structure disclosed in the art;

b. Whether the Board’s finding that Kim teaches away from the claimed invention lacks substantial evidence; and

c. Whether the Board committed legal error by requiring numerical calculations or estimates to prove that the combination reduces resistance, and ignoring the qualitative, background knowledge of a POSITA.

B. For claims 20-21 and 26-27 of the ’395 patent, whether the Board erred because it relied on its determination that a POSITA would not have been motivated to use pure titanium for the claimed metal layer—even though the proposed combinations for these claims ***do not use pure titanium***, but instead use a titanium/tungsten alloy.

STATEMENT OF THE CASE

I. FACTUAL BACKGROUND

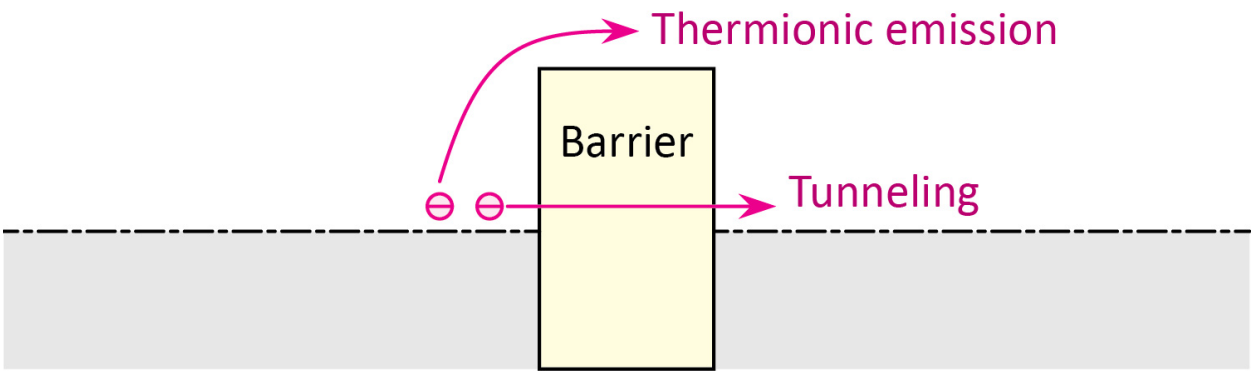
A. Technology Background

Metal-semiconductor ("MS") junctions are "[o]ne of the most basic electrical junctions used in modern devices." Appx0247 (1:33-34). MS junctions are formed by bringing a metal into contact with a semiconductor. Appx0247 (1:34-36). Electrical current flows through a MS junction when electrons cross from the metal to the semiconductor or vice versa. *See* Appx0250 (7:27-38). A MS junction's ability to conduct current depends on a "barrier at the surface of contact between the metal and the semiconductor." Appx0247 (1:46-63). That barrier is characterized by a "barrier height," which describes the amount of energy required for an electron to cross the barrier. *Id.* The barrier height "determines the electrical properties of the junction," including the junction's resistivity (which describes the degree to which electrical current can flow across the junction). Appx0248 (3:4-6); Appx26896 ¶99; Appx26841 (Chang).

The barrier height is affected by, among other things, the properties of the interface between the metal and the semiconductor. Appx26870 ¶34. For example, the barrier height is affected by the presence of "dangling bonds," which arise from semiconductor atoms at the interface that do not have a bonding partner with another semiconductor atom. Appx26870-26872 ¶¶35-38; Appx0241 fig.1; Appx0247 (2:7-

18). The barrier height also depends on the proximity of the metal to the semiconductor: the closer the metal is to the semiconductor, the more likely the metal will induce energy states called "metal-induced gap states" or "MIGS" in the bandgap of the semiconductor, which increase the barrier height. Appx26872 ¶39; Appx0247 (2:41-57). A larger barrier height at the interface can limit the flow of electrons across the barrier, thereby increasing the resistivity.

Electrons can cross a barrier via two transport mechanisms (illustrated below): (1) "tunneling" and (2) "thermionic emission." Appx29019; Appx28991 ¶109. Tunneling is a quantum-mechanical process that transports electrons ***through*** the barrier. Appx28991 ¶109; Appx29524. An electron's ability to pass through a barrier via tunneling is characterized by the "tunneling probability." Tunneling probability describes the likelihood that an electron can traverse the barrier. Lowering the barrier height increases the tunneling probability, which means that electrons can flow across the barrier more readily. Appx28995-28996 ¶¶120-121. Thermionic emission is a process by which electrons with sufficient energy go ***over*** the barrier. Appx28991 ¶109. But this phenomenon occurs only when the barrier height is sufficiently low relative to the energy level of the electron. *Id.*



Appx28991-28992 (⊖ represents an electron).

The junction's resistance to current is often measured as a "specific contact resistivity"/"specific contact resistance" ("SCR") value that has units of ohms times micrometers-squared ($\Omega \cdot \mu m^2$). *See* Appx0269 (3:42-45); Appx26880 ¶58, Appx26885 ¶¶71-72; Appx29501-29502 ¶¶70-71. The Challenged Patents use the terms "specific contact resistivity" and "specific contact resistance" interchangeably when referencing SCR values. *Id.*; *see also* Appx0176-0177. The resistivity of the metal and semiconductor layers (referred to as "bulk resistivity") can affect the junction's electrical properties to varying degrees, including its SCR. But the barrier height at the interface predominantly "determines the electrical properties of the junction." Appx0248 (3:4-6).

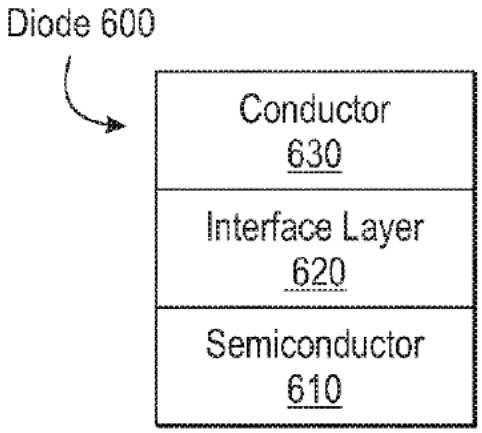
Various techniques to control the barrier height—which, in turn, controls SCR—were developed in the art before the Challenged Patents. One well-known approach to reduce SCR was to add an interface layer between a MS junction's metal and semiconductor layers to lower the barrier height. Appx0248 (3:10-12);

Appx3185-3189 ¶¶52-63 (citing Appx3394-3396 (Iwaguro) at [0005]-[0006], [0012]-[0014], fig.3); Appx26990-26991 ¶319 ("Iwaguro taught that an interface layer could reduce specific contact resistance by a factor of at least 100."). That structure is known as a metal–interface layer–semiconductor ("MIS") junction. Appx0247 (1:28-29).

B. Challenged Patents

U.S. Patent No. 9,905,691 issued from an application filed on February 19, 2016. Appx0237-0238. U.S. Patent No. 10,090,395 is a continuation of the '691 patent and issued from an application filed on January 23, 2018. Appx0258-0259. The '691 and '395 patents share the same specification. Appx11485-11486 ¶¶100-101. They claim priority, through a long chain of continuations and divisionals, to a 2002 parent application that issued as U.S. Patent No. 7,084,423 (the "'423 patent"). Appx11470-11471 ¶65; Appx0237-0238, [60]; Appx0258-0259, [60].

The '691 and '395 patents relate to MIS junctions. According to the patents, the interface layer separates the semiconductor from the metal and limits the effects of dangling bonds and MIGS. Appx0248 (3:30-35, 3:62-4:1); Appx0250 (7:48-56). Figure 6 shows an interface layer (620) between the metal (conductor 630) and semiconductor (610):



Appx0244 fig.6; Appx0265 fig.6.

The claims focus exclusively on MIS structures in which the interface layer comprises: (1) a metal oxide layer; and (2) a semiconductor oxide layer. *E.g.*, Appx0255 ('691 claim 1); Appx0276 ('395 claim 1). The claimed semiconductor oxide portion of the interface layer is a "passivation layer," which terminates the undesirable dangling bonds on the semiconductor surface and displaces the metal from the semiconductor to reduce the effects of MIGS. Appx0149; Appx0248 (3:47-53); Appx0251 (9:42-62, 10:3-11); *see* Appx0250 (8:10-58) (describing passivating function of the layer). The claimed metal oxide portion of the interface layer is a "separation layer" or "spacer layer," which further displaces the metal from the semiconductor to further reduce the effects of MIGS. Appx0018-0019; Appx0149; *see* Appx0248 (3:47-50); Appx0251 (9:49-62); Appx0253 (14:55-58); Appx0255 (17:60-62).

Both patents claim a metal–metal oxide–semiconductor oxide–semiconductor structure. *E.g.*, Appx0255 ('691 claim 1); Appx0276 ('395 claim 1). The specifications identify many metals for the metal layer, including aluminum, titanium, gold, and others. Appx0253 (13:45-67). The specifications also identify many materials for the passivation layer, including silicon dioxide (represented as SiO_2), silicon nitride, and other nitrides, "oxides, hydrides, arsenides and/or fluorides." Appx0250-0252 (8:12-48, 8:54-58, 9:63-10:2, 10:51-12:42).

But the specifications identify only ***one*** metal oxide species for the separation/spacer layer: titanium dioxide (represented as TiO_2). Appx0255 (17:60-62) ("Spacer layers may be used with lower barriers (e.g., TiO_2 has a barrier of less than 1 eV).").

The semiconductor (bottom) layer is always "a silicon-based semiconductor." *E.g.*, Appx0248-0249 (3:20-22, 4:66-5:15).

The preferred embodiment is a structure comprising, from top to bottom, titanium, titanium dioxide, silicon dioxide, and silicon, represented as Ti-TiO_2-SiO_2-Si. *E.g.*, Appx0256 ('691 claim 19); Appx0277 ('395 claims 12, 25); *see also* Appx0255-0256 ('691 claims 6, 10, 12, 15-16, 26).

C. Claims On Appeal

Claim 6 (which depends from claim 1 via claim 3, both of which were found unpatentable) is representative of the issues involving the '691 patent.

> 6. The structure of claim 3, wherein the *metal oxide layer comprises an oxide of titanium*.

Appx0255, Appx0257 (Certificate of Correction).

Claims 11 (which depends from claim 1, which was found unpatentable) and 17 are representative of the issues involving the '395 patent.

> 11. The electrical junction of claim 1, wherein said *metal oxide comprises an oxide of titanium*.
>
> 17. An electrical junction, comprising:
>
> a source or drain of a transistor, said source or drain comprising a semiconductor,
>
> a metal electrical contact to said source or drain, and
>
> an interface layer disposed between and in contact with said source or drain and said metal electrical contact, said source or drain being electrically connected to said metal electrical contact through said interface layer and said interface layer comprising *an oxide of titanium* and an oxide of the semiconductor.

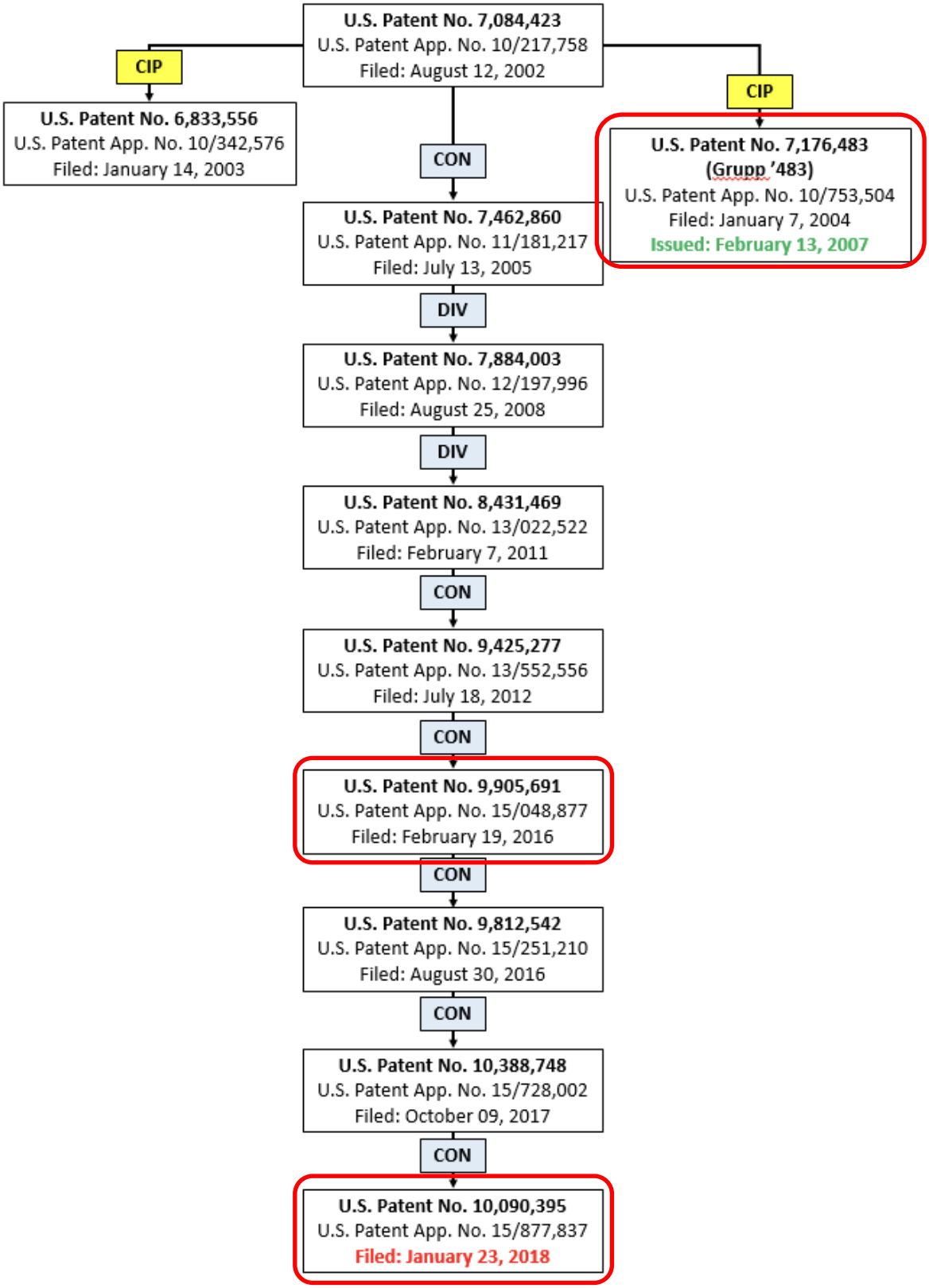
Appx0277.

D. Prior Art

1. Grupp '483 (IPR2020-01206; IPR2020-01207)

Grupp '483 issued on February 13, 2007 and is a continuation-in-part of the '423 patent (the same parent application to which the '691 and '395 patents purport to claim priority). Appx3141. Grupp '483 has the same specification as the '423

patent except that it: (1) corrects minor typographical errors; and (2) discloses additional metals and semiconductors that could be used to form the metal and semiconductor portions of the MIS junction. *See* Appx3408-3441 (redline); Appx3196 ¶79; Appx0685-0686. The relationship between Grupp '483 and the Challenged Patents is shown below:

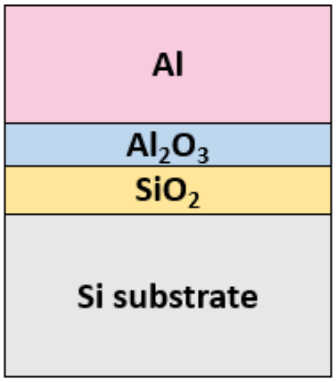


Appx11471 (annotated).

Because Grupp '483 has, in relevant part, the same specification as the Challenged Patents, Grupp '483 anticipates all Challenged Claims that cannot predate Grupp '483's February 13, 2007 issue date. *See* Appx0935 (-1206 POR) ("There are no disputes in this IPR regarding whether the 'prior art' reference (Acorn's own Grupp '483 patent) teaches any of the claim limitations."); Appx8429 (-1207 POR) (same).

2. Goodnick (IPR2020-01279; IPR2020-01282)

Goodnick is an article directed to "the influence of thin SiO_2 layers on the chemical formation of metal-silicon contacts." Appx26816. Goodnick discloses a metal–metal oxide–semiconductor oxide–semiconductor junction, which, in one example, is aluminum–aluminum oxide–silicon dioxide–silicon (represented as Al-Al_2O_3-SiO_2-Si). Appx26820. Goodnick describes growing a 30 angstrom SiO_2 layer on a silicon substrate and depositing aluminum on the SiO_2 layer. *Id.*; Appx26816-26817. The aluminum reacts with a portion of the SiO_2 layer to form an Al_2O_3 layer. Appx26820; Appx26889-26890 ¶¶84-85. The resulting structure is shown below:

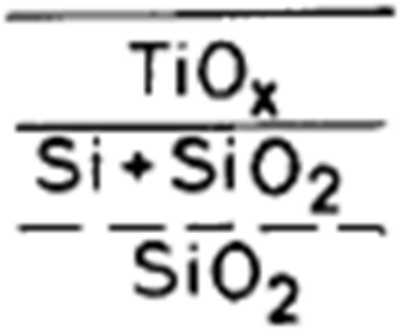


After Al metallization

Appx26890; Appx26887-26890 ¶¶79-87.

3. Taubenblatt[6] (IPR2020-01279; IPR2020-01282)

Taubenblatt is an article that describes MIS structures that include distinct titanium oxide (represented in that reference as TiO_x[7]) and SiO_2 layers in the interface layer. Appx26828. In one example, Taubenblatt describes depositing titanium on a "thick" (more than 20 angstroms) layer of SiO_2 and annealing (heating) at 700-900°C. Appx26834 fig.11 (row 3). Taubenblatt explains that the titanium reacts with the thick layer of SiO_2 to form an interface layer that includes distinct layers of TiO_x and SiO_2, shown below, between the titanium layer and the semiconductor:



[6] The Petition cites this reference as "Taubenblatt 1982" to distinguish it from another reference by the same author cited as "Taubenblatt 1984." Taubenblatt 1984 is not at issue in this appeal.

[7] This brief will also refer to Taubenblatt's titanium oxide as "TiO_x."

Id.; Appx26833-26834. Specifically, under the parameters Taubenblatt describes, "in the reaction of Ti with a thicker [*i.e.*, more than 20 angstroms] SiO_2 layer, Ti oxide forms . . . ." Appx26835. Once the TiO_x layer forms, it prevents subsequent reactions between the titanium and the SiO_2, leaving a layer of unreacted titanium atop the TiO_x layer and a layer of unreacted SiO_2 below the TiO_x layer (with a layer of Si + SiO_2 between the TiO_x and SiO_2 layers). Appx26894-26895 ¶¶95-97.

II. PROCEDURAL HISTORY

A. "Priority IPRs" (IPR2020-01206; IPR2020-01207)

In the Priority IPRs, Samsung challenged claims 1-4, 6, 8, 10-13, 15-20, 22, and 25-29 of the '691 patent and claims 1-6, 8-9, 11-12, and 14-16 of the '395 patent. Appx0571; Appx8079. Samsung argued that Grupp '483 anticipates each of those claims because they are not entitled to priority before Grupp '483's February 13, 2007 issue date due to lack of written description and/or lack of enablement. Appx0565-0566; Appx8073-8074.

1. Lack Of Written Description

Samsung argued that no challenged claim is entitled to priority to any application earlier than U.S. Patent Appl. No. 13/022,522 (the "'522 application"), filed on February 7, 2011, because none of the earlier applications in the priority chain (the "pre-2011 parent applications") provides written description support for the "metal oxide" layer recited in each claim. Appx0565, Appx0582; Appx8073,

Appx8090. In particular, the '522 application was the first application in the priority chain to arguably describe a generic "metal oxide" layer by including claims that recite a "metal oxide." Appx0565, Appx0580 (citing Appx2292); Appx8091. In contrast, no pre-2011 parent application discloses a generic "metal oxide" layer or a "representative number of species falling within the scope of the genus or structural features common to the members of the genus so that one of skill in the art can 'visualize or recognize' the members of the genus." Appx0582-0584 (quoting *Ariad Pharms., Inc. v. Eli Lilly & Co.*, 598 F.3d 1336, 1350 (Fed. Cir. 2010)); Appx8090-8094. At best, the pre-2011 parent applications disclose a ***single*** species of metal oxide: TiO_2 (titanium dioxide). Appx0583-0585; Appx8092-8094.

The Board agreed with Samsung and concluded that the pre-2011 parent applications do not provide written description for the claimed "metal oxide" genus and, accordingly, determined that claims 1-4, 13, 20, 22, and 25 of the '691 patent and claims 1-6, 8-10, and 15-16 of the '395 patent (collectively, the "Metal Oxide Claims") are not entitled to a priority date earlier than February 7, 2011—rendering Grupp '483 anticipatory prior art. Appx0024; Appx0078. Acorn did not appeal those findings, which are now final.

The Board, however, determined that a subset of the challenged claims are narrower than the Metal Oxide Claims and have written description support based on the pre-2011 parent applications' disclosure of TiO_2. In particular, the Board

determined that claims 6, 8, 10-12, 15-19, and 26-29 of the '691 patent and claims 11-12 and 14 of the '395 patent—which recite a "metal oxide [that] ***comprises*** an oxide of titanium" (the "Comprises Claims")—"narrow the recited class to an oxide of titanium, which is a far narrower class." Appx0026; Appx0080. Therefore, the Board did not apply Grupp '483 as prior art to the Comprises Claims and found those claims not unpatentable. Appx0026-0027, Appx0050; Appx0080-0081, Appx0102.

2. Lack Of Enablement

Samsung separately argued that claims 18 and 26-29 of the '691 patent (the "SCR Claims") recite SCR ranges that the parent applications do not enable and, for that independent reason, those claims are not entitled to earlier priority dates. Appx0585-0590; Appx8094-8098. In particular, the SCR Claims require "a specific contact resistivity" that "is less than 1 $\Omega \cdot \mu m^2$." Appx0256. None of the parent applications enables structures with SCR ranges significantly below 1 $\Omega \cdot \mu m^2$ and approaching as low as 0 $\Omega \cdot \mu m^2$. Appx0586-0590.

The Board agreed with Samsung and determined that because the parent applications fail to enable the claimed SCR ranges, the SCR Claims could not claim priority to any parent application, rendering Grupp '483 anticipatory prior art. Appx0038-0039 ("Thus, Grupp '483 ***is prior art*** for each of challenged claims 18, and 25-29."). But when the Board determined, in summation, whether Grupp '483 anticipates claims 18 and 26-29, the Board overlooked its earlier finding, and

inconsistently determined that Grupp '483 is ***not*** prior art for those claims. Appx0043, Appx0045-0046; *see also* Appx0050 (table).

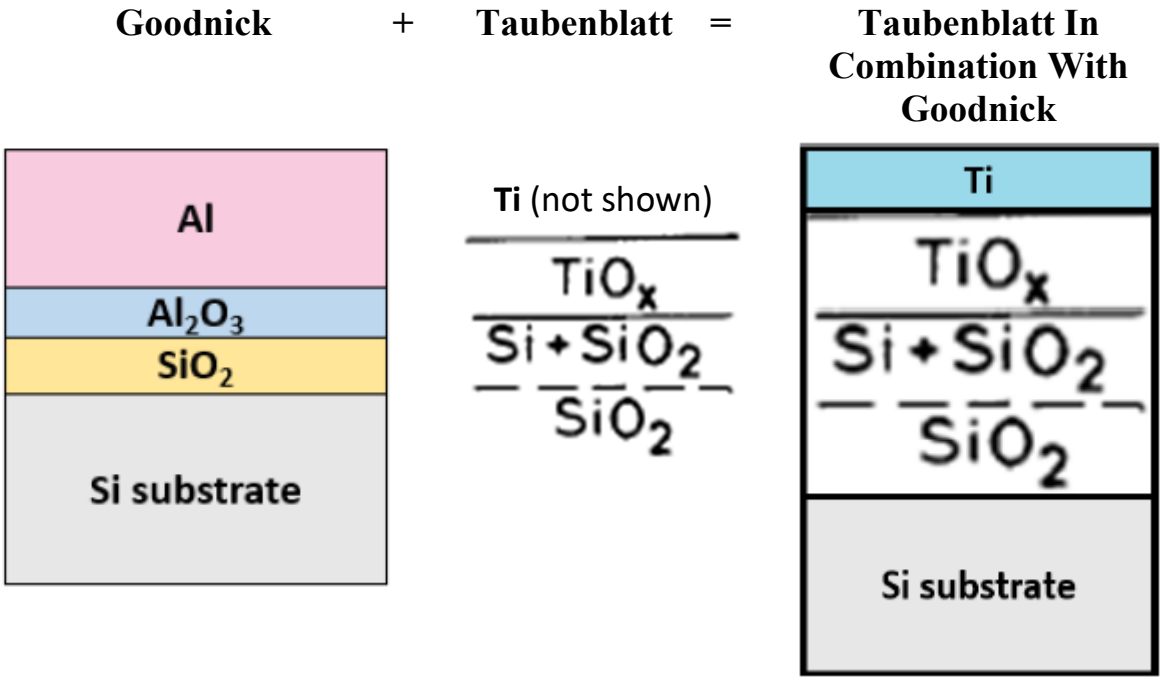
B. "Prior Art IPRs" (IPR2020-01279; IPR2020-01282)

In the Prior Art IPRs, Samsung challenged, among others, claims 6, 8, 10-12, 15-19, and 26-29 of the '691 patent and claims 11-12, 14, and 17-28 of the '395 patent. *See* Appx16352; Appx23278-23279. Each of those claims recites (or depends from a claim that recites) an "oxide of titanium." Appx0255-0256; Appx0277.

Samsung relied on Goodnick combined with Taubenblatt for the "oxide of titanium" limitation. In particular, Samsung explained that depositing Taubenblatt's titanium on Goodnick's thick (30 angstroms), thermally grown SiO_2 layer forms a layer of TiO_x between the titanium and SiO_2 upon "annealing at 700°C – 900°C." Appx23304-23305; *see also* Appx26816.

As shown below on the left, Goodnick discloses a contact structure with a metal oxide layer (aluminum oxide (Al_2O_3)) that is formed by depositing aluminum (Al) onto a semiconductor oxide layer (silicon dioxide (SiO_2)). Appx16364, Appx16375; Appx23286-23287, Appx23303. As shown below in the middle, just like Goodnick, Taubenblatt discloses a structure with a metal oxide layer (titanium oxide (TiO_x)) that is formed by depositing titanium (Ti) onto a thick, thermally grown SiO_2 layer on silicon (Si), and annealing at 700-900°C. Appx19149-19151

¶¶93-95 (citing Appx26834 fig.11); Appx26831, Appx26833-26835. The structure that results from substituting Taubenblatt's titanium for Goodnick's aluminum is shown below on the right. Appx16376-16378; Appx23304-23306.



Appx19145 ¶83, Appx19149-19151 ¶¶93-94, Appx19153 ¶104, Appx19167-19168 ¶¶137-138; Appx26834 (Taubenblatt) fig.11.

Samsung explained that a POSITA would have been motivated to use Taubenblatt's TiO_x interface layer in Goodnick's contact structure because it "would have been expected to reduce the specific contact resistivity" of the structure, which in turn would "reduce the power consumption of a device incorporating a contact with that interface layer." Appx16378-16381; Appx23306-23309; *see also* Appx26945 ¶213 ("Due to its higher bandgap energy, Al_2O_3 is less conductive than TiO_2.").

Samsung also cited several background references, including Kim. In the -1279 IPR (directed to the '691 patent), however, Samsung did not include Kim in any combination. *See* Appx16357 (Grounds). Rather, Samsung cited Kim only as ***background art*** to show that "an interface layer could reduce the SCR of a metal-semiconductor junction." Appx16378. In the -1282 IPR (directed to the '395 patent), Samsung relied on Kim as background art and in the combinations directed to claims 20-21 and 26-27 because those claims require a metal layer that "includes tungsten," which Kim's preferred embodiment discloses. Appx23278-23279 (Grounds), Appx23289, Appx23330-23331.

The Board determined that a POSITA would not have been motivated to combine Goodnick and Taubenblatt. Because the Board's motivation to combine analysis drastically differed between the -1279 and -1282 FWDs, they are addressed separately below.

IPR2020-01279 FWD

In the -1279 FWD, the Board's motivation-to-combine analysis was sparse. Samsung demonstrated that the combination's Ti-TiO_x layers improve upon Goodnick's Al-Al_2O_3 layers due to (1) the increased tunneling probability through TiO_x as compared to Al_2O_3 and (2) the ability for current to flow through the combination's interface via thermionic emission (which Goodnick's Al_2O_3 interface does not permit). *See* Appx16829-16832. The Board ignored that evidence in its

analysis and instead focused on a single issue: whether ***Kim*** provides motivation to combine Goodnick and Taubenblatt. Appx0144-0145. That was peculiar because, as the Board acknowledged, Samsung did not include Kim in any proposed combination in the -1279 IPR, but rather cited Kim only as background art. Appx0144.

The Board pointed to its analysis of Kim in the non-institution decision of another proceeding (IPR2020-01264, not at issue in this appeal), where the Board determined that Kim does not teach "a metal oxide layer or a layer of titanium dioxide." Appx0144-0145. The Board concluded that "[c]onsistent with" its finding in the -1264 IPR, "we are not persuaded that ***Kim*** would have suggested to a person of ordinary skill replacing Goodnick's aluminum with Taubenblatt's titanium in a layered structure." Appx0145.

After concluding that Kim does not provide a motivation to combine Goodnick and Taubenblatt, the Board dismissed the rest of the motivation-to-combine evidence in a single sentence: "Notwithstanding the bulk resistivity and tunneling effect evidence discussed above, there is insufficient evidence to conclude that a person of ordinary skill would have combined the teachings of Goodnick and Taubenblatt as proposed by Petitioner." Appx0145.

The Board did not reach any of the other prior art combinations or arguments, relying solely on its determination that there was no motivation to combine

Goodnick with Taubenblatt to find claims 6, 8, 10-12, 15-20, 22, and 25-29[8] not unpatentable. Appx0147-0150, Appx0162.

IPR2020-01282 FWD

In the -1282 FWD, the Board considered two issues in its motivation to combine analysis. First, the Board observed that neither Goodnick nor Taubenblatt suggests replacing aluminum with titanium and that neither conclusively demonstrates whether a Ti-TiO_x structure has lower SCR than an Al-Al_2O_3 structure. Appx0212. The Board then discussed whether Kim supports Samsung's motivation to combine Goodnick with Taubenblatt. *Id.*

Although the Board acknowledged that Kim teaches that titanium provides an improvement over aluminum, the Board decided that Kim teaches away from the proposed combination because Kim teaches that "pure titanium" is not suitable due to the difference in the thermal coefficient of expansion between pure titanium and silicon in view of a purportedly superior choice: a titanium/tungsten alloy. Appx0212-0213. The Board also broadly read Kim to teach away not only from using titanium in "direct contact" with silicon, as Samsung argued, but to teach away from ever using titanium in a contact. Appx0213-0214.

[8] The Board found claims 20, 22, 25 unpatentable in the -1206 IPR, Appx0050, so those claims are not at issue in this appeal.

Second, the Board determined that Samsung did not prove that the combination results in a lower SCR relative to Goodnick's structure, but it did not weigh the specific competing evidence. In particular, Acorn argued that the bulk resistivity of the combination's titanium "is about 16 times greater than that of aluminum," so, according to Acorn, a POSITA would not substitute Taubenblatt's titanium for Goodnick's aluminum. Appx23637. In response, Samsung demonstrated why Acorn's argument was a red herring: the bulk resistivity of the metal layer—regardless of whether it is titanium or aluminum—is insignificant in the context of the entire structure because the structure's bulk resistivity is dominated by the other layers, such as the silicon substrate, which can be ***10 billion***[9] times larger than the bulk resistivity of the metal layer. Appx23748. Samsung went on to explain that the ***interface layer*** provides the most important resistance contribution to the structure's SCR (Appx28989-28990 ¶108; *see also* Appx29527 ¶117), and that the combination's TiO_x layer improves upon Goodnick's Al_2O_3. Specifically, Samsung demonstrated that electrical current moves across the combination's Ti-TiO_x layers primarily by tunneling, and that the tunneling

[9] Acorn argued that in highly doped semiconductors, the semiconductor's bulk resistivity is 100 times greater than the metal layer's bulk resistivity (rather than 10 billion times greater). Appx23813-23814, Appx23816. But in any case, Acorn's calculations concede that the semiconductor's bulk resistivity is orders of magnitude greater than the metal layer's bulk resistivity.

probability is 30 times[10] better through the Ti-TiO_x interface (in the combination) as compared to the Al-Al_2O_3 interface (in Goodnick). Appx23749, Appx23750 (figure showing electrical properties of each layer); Appx28994-28996 ¶¶114-121 (providing calculations). In addition, Samsung explained that electrical current moves across the combination's Ti-TiO_x interface via ***both*** tunneling and thermionic emission, whereas electrical current moves across Goodnick's Al-Al_2O_3 interface via ***only*** tunneling—facts Acorn did not dispute. Appx23750-23751; *see* Appx23817.

The Board never reached the merits of those disputes. *See* Appx0214-0216. Instead, the Board stopped its analysis when it observed that it could not directly compare—in common units of "ohms" (Ω) and with precise numbers—the SCR increase due to the 16-fold increase in the metal layer's bulk resistivity, on the one hand, and the SCR decrease due to the 30-fold increase in tunneling probability and the combination's ability to pass current by thermionic emission, on the other hand. Appx0214-0216.

[10] Acorn argued that the increase in tunneling probability is only 1.66 times greater in the combination than in Goodnick's structure (rather than 30 times greater). Appx24140 (Hr'g Tr.) (71:9-10); Appx23813-23814, Appx23816. But in any case, Acorn's calculations concede that the tunneling probability through the combination's Ti-TiO_x interface is higher (better) than through Goodnick's Al-Al_2O_3 interface. *See* Appx24140 (71:9-10) (using Acorn's numbers, "that 30x advantage drops down to something like 1.66.").

SUMMARY OF THE ARGUMENT

Although the Board agreed with Samsung that many claims of the '691 and '395 patents are unpatentable, each of the four decisions found some claims not unpatentable. Those determinations, however, resulted from clear errors of law, lacked adequate analysis, or are unsupported by substantial evidence.

First, in the -1206 and -1207 IPRs, the Board incorrectly interpreted the term "comprises." Specifically, the Board erred by interpreting the Comprises Claims[11] to limit the claimed metal oxide layer to ***only*** an oxide of titanium and to ***exclude*** all other metal oxides (which the Board separately found lack written description support) from the interface layer. The Board erred because "comprises" is an open-ended transitional phrase. Correctly interpreted, the Comprises Claims encompass a metal oxide layer that includes "an oxide of titanium" (which is required) but that may ***also*** include other metal oxides. By limiting the claimed metal oxide layer to ***only*** an "oxide of titanium," the Board erroneously replaced the open-ended transitional phrase "comprises" with the closed-ended phrase "consisting of." That clear claim-construction error requires reversal. When properly construed, the

[11] As a reminder, the "Comprises Claims" are claims 6, 8, 10-12, 15-19, and 26-29 of the '691 patent and claims 11-12, and 14 of the '395 patent, which recite a "metal oxide" layer that "***comprises*** an oxide of titanium." Appx0255-0256; Appx0277.

claims lack written description support to any pre-2011 parent applications, rendering Grupp '483 anticipatory prior art.

In addition, the Board improperly refused to consider Samsung's Replies showing that—even under the interpretation of "comprises" that the Board ultimately adopted—the pre-2011 parent applications fail to provide written description support for the "oxide of titanium" genus. That was error because Samsung's Replies were properly responsive to a claim construction argument that Acorn raised for the first time post-institution in its PORs.

Second, in the -1206 IPR, the Board's anticipation analysis concluded that Grupp '483 is not prior art to claims 18 and 26-29 of the '691 patent because the Board rejected Samsung's lack-of-written-description argument. But in doing so, the Board overlooked its separate finding that Grupp '483 ***is prior art*** because those claims are not ***enabled*** by any parent applications. That clear error warrants reversal. When Grupp '483 is properly considered prior art, it anticipates claims 18 and 26-29.

Third, in the -1279 IPR, the Board failed to adequately explain, as required by the APA, why it determined Samsung had not shown that a POSITA would have been motivated to combine Goodnick with Taubenblatt. In particular, the Board sidestepped—in a single sentence—Samsung's motivation to combine evidence and instead relied on its discussion of a ***different*** prior art reference (Kim) involved in a

different combination (Kim + Jammy, not Goodnick + Taubenblatt) in a ***different*** IPR proceeding (IPR2020-01264). That analysis is arbitrary and untethered to either party's position in this IPR, and requires remand.

Fourth, in the -1282 IPR, the Board deviated from *KSR*'s flexible standard to find that Samsung had not met its burden to show a motivation to combine Goodnick with Taubenblatt. In particular, the Board erred by: (1) comparing the Goodnick-Taubenblatt combination's thermal properties to a purportedly optimal structure disclosed in Kim, rather than properly examining whether the combination improves upon the base reference (Goodnick) that the combination modifies; (2) overbroadly reading Kim to teach away from ever using titanium in ***any*** contact structure, despite Acorn's expert's admission that using titanium in MIS structures was "common[]" (Appx28179 (65:16-24)); (3) failing to consider the qualitative evidence regarding the background knowledge of a POSITA about the importance of the various layers in a junction, and instead improperly requiring Samsung to prove—with mathematical precision—that the combination achieves a net reduction in SCR; and (4) applying its conclusion that a POSITA would not use "pure titanium" to the combinations for claims 20-21 and 26-27 even though those combinations ***do not use*** pure titanium, but instead use Kim's preferred titanium/tungsten alloy.

For those reasons, this Court should reverse (or at least vacate) the Board's determinations in the Priority IPRs, and vacate the Board's determinations in the

Prior Art IPRs and remand to allow the Board to analyze the actual disputes between the parties under the correct standards.

ARGUMENT

STANDARDS OF REVIEW

In appeals from IPRs, this Court "review[s] the Board's conclusions of law *de novo* and the Board's findings of fact for substantial evidence." *Homeland Housewares, LLC v. Whirlpool Corp.*, 865 F.3d 1372, 1374 (Fed. Cir. 2017). "Claim construction is an issue of law," particularly where "there is no relevant extrinsic evidence." *Id.* This Court also "review[s] the Board's compliance with the governing legal standards de novo." *Gen. Elec. Co. v. Raytheon Techs. Corp.*, 983 F.3d 1334, 1344-45 (Fed. Cir. 2020) (quoting *Belden Inc. v. Berk-Tek LLC*, 805 F.3d 1064, 1073 (Fed. Cir. 2015)).

For factual issues, "[a] finding is supported by substantial evidence if a reasonable mind might accept the evidence." *In re Ethicon, Inc.*, 844 F.3d 1344, 1349 (Fed. Cir. 2017). The substantial evidence inquiry examines "the 'record as a whole, taking into account evidence that both justifies and detracts from an agency's decision.'" *Canfield Sci., Inc. v. Melanoscan, LLC*, 987 F.3d 1375, 1378 (Fed. Cir. 2021).

"Obviousness is a question of law with underlying factual issues," including the "scope and content of the prior art, differences between the prior art and the claims at issue, the level of ordinary skill in the pertinent art, [and] the motivations to modify or combine prior art." *See Intel Corp. v. Qualcomm Inc.*, No. 2020-2092,

2022 WL 880681, at *3 (Fed. Cir. Mar. 24, 2022) (nonprecedential); *Belden*, 805 F.3d at 1073.

"Decisions related to compliance with the Board's procedures," including whether reply arguments are properly responsive under 37 C.F.R. § 42.23(b), are reviewed for abuse of discretion. *Ericsson Inc. v. Intellectual Ventures I LLC*, 901 F.3d 1374, 1379 (Fed. Cir. 2018).

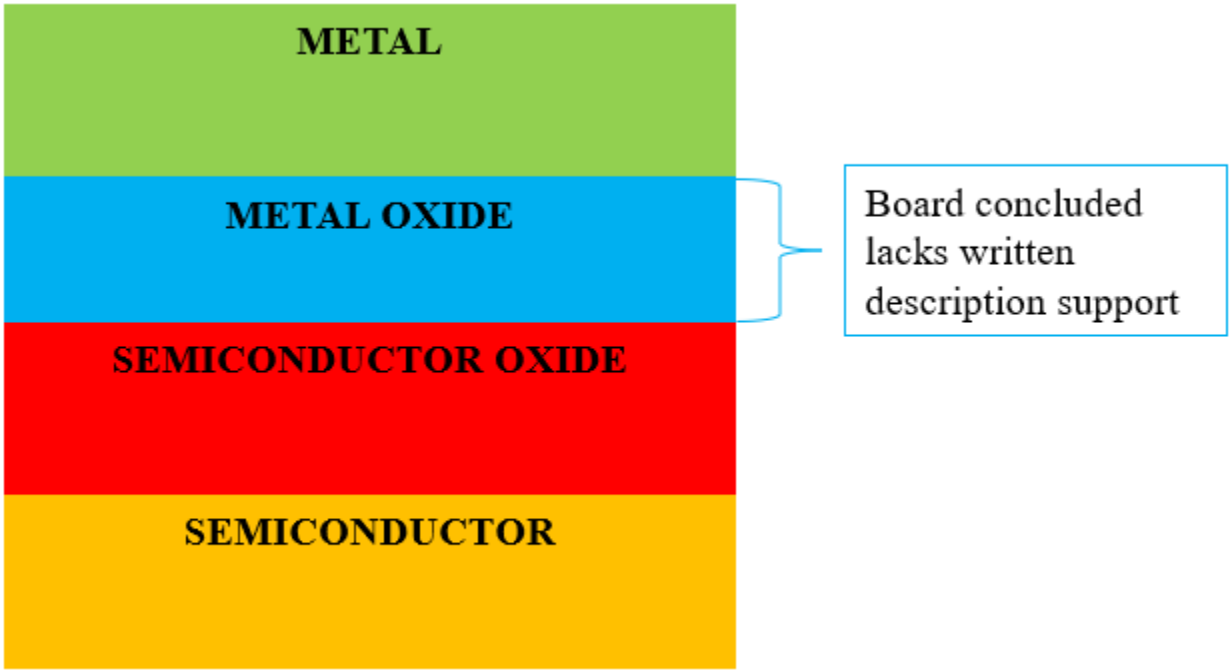
For this Court to see that the agency has done its job, "the Board is obligated to 'articulate a satisfactory explanation for its action including a rational connection between the facts found and the choice made.'" *Alacritech, Inc. v. Intel Corp.*, 966 F.3d 1367, 1372-73 (Fed. Cir. 2020) (quoting *In re Nuvasive, Inc*., 842 F.3d 1376, 1382 (Fed. Cir. 2016)).

I. IN THE -1206 AND -1207 IPRS, THE "COMPRISES CLAIMS" LACK WRITTEN DESCRIPTION SUPPORT IN THE PRE-2011 PARENT APPLICATIONS AND ARE THEREFORE ANTICIPATED BY GRUPP '483

A. The Phrase "*Comprises* An Oxide Of Titanium" Does Not Narrow The Claims For Purposes Of Written Description Because "Comprises" Does Not Exclude Other Metal Oxides From The "Metal Oxide" Layer

In the Priority IPRs, the Board determined that the "metal oxide" layer of the claimed metal–metal oxide–semiconductor oxide–semiconductor structure lacks written description support in the pre-2011 parent applications, rendering Grupp

'483 anticipatory prior art. Appx0024; Appx0069, Appx0078. This structure is illustrated below. Acorn did not appeal those determinations.



The Board, however, determined that the Comprises Claims,[12] which recite a "metal oxide" layer that "***comprises*** an oxide of titanium," have written description support based on the pre-2011 parent applications' disclosure of a single species of titanium oxide—TiO_2—because, according to the Board, those claims "narrow the recited class to an oxide of titanium, which is a far narrower class." Appx0026; Appx0080. The Board thus adopted Acorn's claim interpretation that the Comprises Claims are limited to a metal oxide layer that consists ***only*** of an oxide of titanium and that ***excludes*** any metal oxides other than oxides of titanium. Accordingly, the

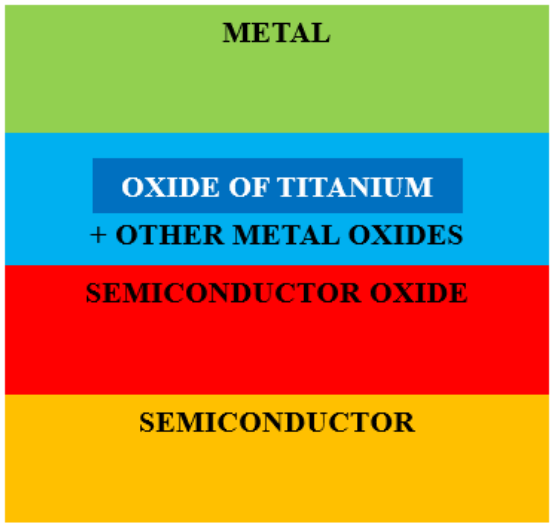
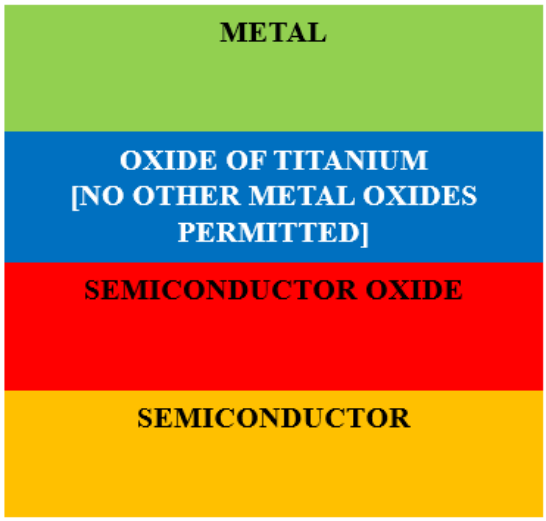
[12] *See supra* n.11.

Board determined that Samsung had not proven that the Comprises Claims are not entitled to an earlier priority date based on lack of written description for the "metal oxide." Appx0026-0027; Appx0080-0081.

The question on appeal is whether requiring the claimed "metal oxide" layer—which the Board found lacks written description—to further "***comprise***[] an oxide of titanium" remedies the lack of written description. It does not. And because this question turns on the proper interpretation of the transitional phrase "comprises," this is a claim construction issue that this Court reviews *de novo*. *Homeland Housewares*, 865 F.3d at 1374.

It is true that for purposes of infringement or prior art-based invalidity, the Comprises Claims require an infringing product or invalidating reference to include an "oxide of titanium" within the "metal oxide" layer. But with respect to the written description requirement, the Comprises Claims encompass a layer that includes the myriad metal oxides that the Board correctly found lack written description support (in addition to the required oxide of titanium). That is, the Comprises Claims are not limited to a metal oxide layer that contains ***only*** titanium oxide and that excludes the unsupported metal oxides, but rather encompasses a layer that includes a titanium oxide (which is required) ***and*** other metal oxides that the Board found lack written description support.

The following illustrations demonstrate the error. The illustration on the left shows how—under the proper interpretation of the term "comprises"—the claimed structure can encompass the myriad metal oxides that the Board determined lack adequate written description in the pre-2011 parent applications (in addition to the required oxide of titanium). The illustration on the right shows the interpretation that Acorn advanced and that the Board implicitly adopted when it determined that the Comprises Claims "narrow the recited class to an oxide of titanium, which is a far narrower class." Appx0026; Appx0080.

<table>
<tr><th colspan="2">"a metal oxide [that] comprises an oxide of titanium"</th></tr>
<tr><th>Samsung</th><th>Acorn/Board</th></tr>
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</td></tr>
</table>

Acorn's interpretation of the claims—which the Board adopted—is legally incorrect. The transitional phrase "comprises" is open-ended and indicates that although the "named elements are essential," "other elements may be added and still form a construct within the scope of the claim." *Genentech, Inc. v. Chiron Corp.*,

112 F.3d 495, 501 (Fed. Cir. 1997). In other words, as shown above on the left, although the Comprises Claims require the "metal oxide" layer to include an "oxide of titanium," the Comprises Claims encompass a metal oxide layer containing an oxide of titanium ***and*** any of the other metal oxides that the Board found lack written description support in the pre-2011 parent applications. Thus, adding the clause "***comprises*** an oxide of titanium" does not obviate the need for adequate written description of the recited "metal oxide" genus—which the Board found lacking.

In contrast, as shown above on the right, Acorn incorrectly interprets the limitation "comprises an oxide of titanium" to limit the claimed "metal oxide" layer to ***only*** an oxide of titanium and to ***exclude*** any other metal oxides. Appx1058. Acorn bases that incorrect interpretation on each claim's recitation of "***a*** metal oxide" that further "comprises an oxide of titanium." Appx1058 (emphasis in original); *id.* ("[T]he claim language is not susceptible to an interpretation permitting an oxide of titanium plus another metal oxide. Each relevant independent claim says '***a*** metal oxide' and it is ***that*** metal oxide that the relevant dependent claims narrow to an oxide of titanium." (emphases in original)); Appx8540. Acorn's interpretation—which the Board incorrectly adopted—violates two tenets of claim construction.

First, it is axiomatic that "a" means "one or more." *Baldwin Graphic Sys., Inc. v. Siebert, Inc.*, 512 F.3d 1338, 1342 (Fed. Cir. 2008) ("[T]his court has

repeatedly emphasized that an indefinite article 'a' or 'an' in patent parlance carries the meaning of 'one or more' in open-ended claims containing the transitional phrase 'comprising.'" (quoting *KCJ Corp. v. Kinetic Concepts, Inc.*, 223 F.3d 1351, 1356 (Fed. Cir. 2000))). "That 'a' or 'an' can mean 'one or more' is best described as a ***rule***, rather than merely as a presumption or even a convention" and the "exceptions to this rule are extremely limited." *Id*. In accordance with that "rule," reciting "a" metal oxide does not limit the claimed metal oxide layer to a ***single*** type of metal oxide, such as titanium dioxide; rather, those claims encompass layers that include ***multiple*** metal oxides, including those that the Board found lack written description support.

Second, Acorn's (and the Board's) interpretation effectively replaces the transitional phrase "comprises" with "consisting of." Claim drafting conventions provide that a claim that uses the transitional phrase "consisting of"—rather than "comprises" or "comprising"—narrows an otherwise open-ended limitation to the particular element that follows. *See* MPEP § 2111.03 ("The transitional term 'comprising' [is] open-ended and does not exclude additional, unrecited elements or method steps. . . . The transitional phrase 'consisting of' excludes any element, step, or ingredient not specified in the claim.") (collecting cases); *Exergen Corp. v. Wal-Mart Stores, Inc.*, 575 F.3d 1312, 1319 (Fed. Cir. 2009) ("The claim uses the term 'comprising,' which is well understood in patent law to mean 'including but not

limited to.'"). If the applicant here had instead claimed a "metal oxide" layer "***consisting of*** an oxide of titanium," the claimed metal oxide layer would be limited to oxides of titanium and would exclude the myriad metal oxides that the Board found lack written description support.

But that is not what these claims recite. Instead, the Comprises Claims use the open-ended "comprises"—not "consisting of"—and therefore do not narrow the "metal oxide" to ***only*** an "oxide of titanium" (to the exclusion of the other unsupported metal oxides). Even Acorn's expert agrees that claims that use the transitional phrase "comprising" do not exclude other metal oxides: "***I do not believe it excludes anything***, nor does it have a list of which oxides are included, so I don't think it's specific about the oxide. It simply says '***comprising*** an oxide of titanium.'" Appx3845 (118:4-14).

Accordingly, under the proper claim construction, the Comprises Claims are not narrowed in a way that remedies the written-description defect with the "metal oxide" layer.

1. Without Written Description Support, The Comprises Claims Are Not Entitled To Priority Earlier Than February 7, 2011, And Grupp '483 Therefore Anticipates Them

Properly construed, the Comprises Claims encompass the myriad metal oxides that the Board already determined lack written description support in the pre-

2011 parent applications. Accordingly, those claims are not entitled to a priority date earlier than February 7, 2011 (*i.e.*, the same date as the Metal Oxide Claims).

Grupp '483 therefore qualifies as prior art that anticipates the Comprises Claims because it teaches a TiO_2 separation/spacer layer. Appx0593, Appx0604-0608, Appx0616-0618; Appx8112-8116. Indeed, Acorn conceded that Grupp '483 anticipates if it qualifies as prior art. *See* Appx0935 ("There are no disputes in this IPR regarding whether . . . Grupp '483 . . . teaches any of the claim limitations."); Appx8429 (same). On that record, there is no need to remand as to the Comprises Claims because only one outcome is possible: Grupp '483 anticipates.

* * *

Based on the Board's claim construction error, Samsung respectfully requests that this Court: (1) reverse the Board's finding that the Comprises Claims are entitled to a priority date earlier than February 7, 2011; (2) reverse the Board's finding that Grupp '483 is not prior art to the Comprises Claims; and (3) hold that Grupp '483 anticipates the Comprises Claims. Alternatively, at a minimum, this Court should remand for the Board to consider whether the pre-2011 parent applications provide written description support for the Comprises Claims under the correct construction of "comprises."

B. The Board Improperly Refused To Consider Responsive Arguments And Evidence Demonstrating That The Comprises Claims Lack Written Description Support Even Under Acorn's Interpretation

The Board improperly refused to consider Samsung's Reply arguments showing that the Comprises Claims lack written description even under Acorn's argument that they are "narrower" than the Metal Oxide Claims, finding that those were belated arguments that should have been raised in the Petitions. Appx0025-0026 (citing, *inter alia*, 37 C.F.R. § 42.23(b)); Appx0079-0080 (same). That was an abuse of discretion warranting remand for two reasons.[13]

First, Samsung's Reply arguments were proper, and should have been considered, because they were responsive to a new construction Acorn first raised in its PORs (Appx0926-0927; Appx8421). *See Ericsson Inc. v. Intellectual Ventures I LLC*, 901 F.3d 1374, 1380 (Fed. Cir. 2018). In *Ericsson*, which is analogous to this case, the petition, POPR, and institution decision each examined the claims under the broadest reasonable interpretation. *Id.* at 1377-78. In the POR, the patent owner correctly pointed out that the claims should be construed under *Phillips*. *Id.* at 1378. The Board adopted a different construction in its FWD applying the *Phillips* standard, but declined to consider the petitioner's reply arguments demonstrating

[13] The Court need not reach this issue if it agrees with Samsung's arguments in Section I.A.

how the prior art satisfied the claims under the *Phillips* constructions advanced by the patent owner in its POR. *Id*. at 1378-80. This Court held that, because the Board adopted a different construction than the construction the parties (and the Board) had applied through institution, the petitioner should have been permitted to present arguments and evidence in its reply under those "changed circumstances." *Id*. at 1380.

Similarly, Samsung's Petitions argued that all challenged claims—including those that recite a "metal oxide" that further "comprises an oxide of titanium"—lack written description because the pre-2011 parent applications do not support claims encompassing the "metal oxide" genus. Samsung could not, and should not have been expected to, predict or preemptively address the construction Acorn would ultimately advance post-institution. Indeed, Acorn's POPRs did not include any discussion of a so-called "narrower" construction of the Comprises Claims, so the Institution Decisions did not address that interpretation. *See generally* Appx0716-0733; Appx8219-8236; Appx0813-0823; Appx8313-8320. But in its PORs, Acorn ***for the first time*** asserted that—despite the use of "comprises"—the Comprises Claims are "narrower" for purposes of written description than the Metal Oxide Claims:

> While the petition argues that the written-description support for "metal oxide" is inadequate, the petition has not even attempted to do so for "an oxide of titanium," ***which is considerably narrower than "a metal oxide"*** and in much closer conformance with the undisputed

> written description of the '423 Patent (teaching a separation layer of titanium dioxide (TiO_2), which is an oxide of titanium).

Appx0922-0923, Appx0925-0927; Appx8421; *see also* Appx7561-7562 ¶114; Appx15834-15835 ¶114.

In reply, Samsung explained not only why that construction is wrong (as explained in Section I.A above), but also why—even under Acorn's new, post-institution construction—the pre-2011 parent applications fail to provide written description support for the Comprises Claims. Appx0982-0987; Appx8476-8481. In particular, Samsung properly demonstrated that—just like the metal oxide genus—the titanium oxide genus includes species with "vastly different characteristics" and even Acorn's expert could not identify how many titanium oxide species exist. Appx0982-0985 (quoting Appx3841 (114:10-18) ("Q. Dr. Kuhn, what are the different species in the titanium oxide genus? A. . . . I don't know how many chemical compounds exist within the Ti oxide family.")); Appx8476-8479. Acorn's expert even testified that a titanium oxide that had not been discovered would be encompassed by the claims. Appx3826 (99:6-23) ("Let's say that someone discovered . . . a ***new species of Ti oxide***, and demonstrated that in a metal-insulator-semiconductor/drain junction, ***I certainly believe that would fall within the claims***."). Thus, Samsung's Replies appropriately showed that even under Acorn's new, post-institution interpretation of the Comprises Claims, the pre-2011 parent

applications' single example of TiO_2 fails to provide written description support for the full genus of "oxides of titanium."

Under *Ericsson*, the Board is not free to adopt a different interpretation of the claims post-institution while denying the petitioner an opportunity to address the claims' invalidity under that new interpretation. 901 F.3d at 1380. The Board's refusal to consider Samsung's reply evidence, which was directly responsive to Acorn's new interpretation—raised for the first time post-institution—was an abuse of discretion.

Second, Samsung's reply arguments were proper, and should have been considered, because they advanced the same theory as the Petitions. *Cf. Apple Inc. v. Andrea Elecs. Corp.*, 949 F.3d 697, 705-07 (Fed. Cir. 2020) (holding that replies may include arguments that are "responsive to arguments originally raised in [the] petition"). Samsung's reply arguments simply elaborate on "the ***same legal argument***" advanced in the Petitions (*id.* at 706): that the sole example of TiO_2 in the pre-2011 parent applications is insufficient to provide written description support for the claims, and hence Grupp '483 anticipates the challenged claims.

Accordingly, even if this Court determines that Acorn's interpretation—that the Comprises Claims limit the claimed metal oxide layer to an "oxide of titanium" (to the exclusion of other metal oxides found to lack written description support)—

is correct, this Court should vacate and remand so that the Board may consider Samsung's Reply arguments and evidence under that interpretation.

II. IN THE -1206 IPR, THE BOARD OVERLOOKED ITS OWN FINDINGS THAT CLAIMS 18 AND 26-29 OF THE '691 PATENT ARE NOT ENABLED AND, THEREFORE, GRUPP '483 QUALIFIES AS ANTICIPATORY PRIOR ART

The Board made an obvious error regarding claims 18 and 26-29 of the '691 patent (collectively, the "SCR Claims"). Those claims require "a specific contact resistivity" that "is less than 1 $\Omega \cdot \mu m^2$." Appx0256. The Board found that claims 18 and 26-29 cannot obtain priority to any parent applications because the parent applications do not enable the claimed SCR ranges ("less than 1 $\Omega \cdot \mu m^2$")—rendering Grupp '483 prior art to each of those claims. Appx0038-0039 ("Thus, Grupp '483 ***is prior art*** for each of challenged claims 18, and 25-29."). But when the Board determined, in summation, whether Grupp '483 anticipates claims 18 and 26-29, the Board overlooked its earlier finding, and inconsistently determined that Grupp '483 is ***not*** prior art for those claims. Appx0043, Appx0045-0046; *see also* Appx0050 (table).

The Board's oversight appears to stem from the fact that Samsung presented two independent arguments showing that Grupp '483 qualifies as anticipatory prior art: (1) lack of written description; and (2) lack of enablement. *See* Appx0582-0585 (written description); Appx0585-0590 (enablement). The Board disagreed with Samsung's written description argument for those claims. Appx0024-0027. But the

Board ***agreed*** with Samsung's lack of enablement argument. Appx0037-0038. In particular, the Board agreed with Samsung that none of the parent applications enable structures with the claimed SCR ranges of "less than 1 $\Omega \cdot \mu m^2$". Appx0027-0039. Thus, because the Board ***agreed*** that the parent applications do not enable those claims, it correctly determined that Grupp '483 qualifies as prior art; but it erred by overlooking that finding in its ultimate anticipation analysis. Appx0039.

Acorn did not appeal or cross-appeal the Board's lack-of-enablement finding. And because Acorn did not dispute that Grupp '483 anticipates all challenged claims if Grupp '483 qualifies as prior art, the Board should have found that Grupp '483 anticipates the claims. *See* Appx0606-0608, Appx0614-0618 (Petition) (demonstrating how Grupp '483 anticipates); Appx0935 (Acorn conceding that "[t]here are no disputes in this IPR regarding whether . . . Grupp '483 . . . teaches any of the claim limitations"); *see generally* Appx0896-0921 (POR).

Thus, the Board's ultimate finding of no anticipation for claims 18 and 26-29 lacks substantial evidence. Indeed, its oversight of its own lack-of-enablement finding is arbitrary and capricious because there is no "rational connection" between the Board's findings and its ultimate determination. *See* 5 U.S.C. § 706(2)(A); *In re Gartside*, 203 F.3d 1305, 1312 (Fed. Cir. 2000). Accordingly, this Court should

reverse and hold claims 18 and 26-29 unpatentable, because that is the only result that the record supports.[14]

III. IN THE -1279 IPR, THE BOARD FAILED TO PROVIDE AN ADEQUATE EXPLANATION FOR ITS DETERMINATION THAT A POSITA WOULD NOT HAVE BEEN MOTIVATED TO COMBINE GOODNICK WITH TAUBENBLATT

"[T]he Board is obligated to 'articulate a satisfactory explanation for its action including a rational connection between the facts found and the choice made.'" *Alacritech*, 966 F.3d at 1372-73 (quoting *In re Nuvasive*, 842 F.3d at 1382). Where the Board fails to provide an administrative record that sets forth the evidence and the agency's reasoning, this Court must set aside those conclusions and remand. *Id.* (remanding under APA); *In re Van Os*, 844 F.3d 1359, 1362 (Fed. Cir. 2017); 5 U.S.C. § 706(2)(A), (E). Here, the Board failed to analyze the actual disputes over Samsung's asserted motivation to combine, and instead arbitrarily addressed an unasserted argument that was untethered to either party's position in this proceeding.

In the Petition, Samsung argued that a POSITA would have been motivated to replace Goodnick's Al-Al_2O_3 layers with Taubenblatt's Ti-TiO_x layers because it would have resulted in a structure with reduced SCR. Appx16378-16381. Acorn countered that the bulk resistivity of the combination's titanium is 16 times higher than that of Goodnick's aluminum. Appx16718. In response, Samsung:

[14] This Court has authority to correct that error. 5 U.S.C. § 706(2).

(1) explained that Acorn's argument was an irrelevant red herring because the metal layer (regardless of whether it is titanium or aluminum) contributes negligible resistance in the context of the overall structure; (2) demonstrated that the combination's TiO_x layer provides a 30-fold increase in tunneling probability as compared with Goodnick's Al_2O_3 layer, resulting in lower overall SCR; (3) explained that, unlike Goodnick's Al-Al_2O_3 layers, the combination's Ti-TiO_x layers permit current to pass via thermionic emission; and (4) showed that the combination's TiO_x is more conductive than Goodnick's Al_2O_3. Appx16828-16832; Appx21085-21090 ¶¶105-112.

Although the Board summarized the parties' arguments (Appx0135-0144), the FWD sidestepped those disputes in a single sentence: "***Notwithstanding*** the bulk resistivity and tunneling effect evidence discussed above, there is insufficient evidence to conclude that a person of ordinary skill would have combined the teachings of Goodnick and Taubenblatt as proposed by Petitioner." Appx0145. That was an abuse of discretion. The Board may not simply "summarize and reject arguments without explaining why [it] accepts the prevailing argument." *In re NuVasive*, 842 F.3d at 1383.

The Board did not examine, for example: (1) whether the bulk resistivity of the metal layer is negligible when compared to the bulk resistivity of the semiconductor layer (as Samsung argued); or (2) whether the increased tunneling

probability that results from substituting TiO_x for Al_2O_3 reduces the junction's overall resistance (as Samsung argued). And the Board did not address the other effects, such as thermionic emission, that enable current to flow through the Ti-TiO_x interface and thereby lower overall resistance. Thus, the FWD does not adequately address the parties' disputes and provides no explanation for this Court to "see that the agency has done its job." *Alacritech*, 966 F.3d at 1371 (quoting *In re NuVasive*, 842 F.3d at 1383).

Instead of addressing Samsung's ***actual*** motivation arguments, the Board based its conclusion on its own discussion of Kim from a ***different*** IPR (IPR2020-01264), where it found that Samsung "had not shown that Kim teaches a metal oxide layer or a layer of titanium dioxide." Appx0144-0145. That analysis is arbitrary and capricious because the -1264 IPR was directed to a different patent (U.S. Patent No. 8,766,336) and involved a different combination (Jammy[15] and Kim—***not Goodnick and Taubenblatt***). *See* Decision Denying Institution, *Samsung Elecs. Co., Ltd. v. Acorn Semi, LLC*, IPR2020-01264, 2021 WL 130614, at *3 (PTAB Jan. 13, 2021).[16]

[15] U.S. Patent No. 6,724,088. Appx19079-19083.

[16] The Board denied institution in the -1264 IPR, but it found all challenged claims of the '336 patent unpatentable in another proceeding. Final Written Decision, *Samsung Elecs. Co., Ltd. v. Acorn Semi, LLC*, IPR2020-01204, 2022 WL 130888, at *23 (PTAB Jan. 12, 2022).

The Board's determination in the -1264 IPR that Kim does not disclose a "layer" of titanium oxide is irrelevant here because the -1279 Petition ***did not rely on Kim in any of the Grounds***, let alone to teach a "layer" of titanium oxide. *See* Appx16357. Rather, Samsung relied on Goodnick and Taubenblatt—not Kim—to show a "layer" of titanium oxide. Appx16377-16378. Acorn never disputed that the Goodnick-Taubenblatt combination would disclose such a layer.

The Board's choice ***not*** to analyze Samsung's asserted motivation, and instead to rely on a wholly irrelevant discussion of Kim in another proceeding—directed to a different combination of different prior art references—is arbitrary and capricious, and its ultimate conclusions are unsupported by substantial evidence. *See Andrea Elecs. Corp. v. Apple Inc.*, No. 2021-1248, 2022 WL 1197341, at *5 (Fed. Cir. Apr. 22, 2022) (nonprecedential) (finding Board's motivation-to-combine analysis "inadequate for the same reason, *i.e.*, the failure to address the specific motivation issues argued by the parties"). At a minimum, those errors require remand. *See Alacritech*, 966 F.3d at 1372 (remanding where Board's analysis was "untethered to either party's position" in that proceeding).

IV. IN THE -1282 IPR, THE BOARD ERRED IN CONCLUDING THAT A POSITA WOULD NOT HAVE BEEN MOTIVATED TO COMBINE GOODNICK WITH TAUBENBLATT

In the -1282 IPR, the Board determined that a POSITA would not have combined Goodnick with Taubenblatt to achieve a titanium–titanium oxide–silicon

dioxide–silicon structure for two reasons. First, the Board found that a POSITA would not have replaced Goodnick's aluminum with Taubenblatt's titanium because Kim teaches that pure titanium has less preferable thermal properties than a titanium/tungsten alloy and, for that reason, determined that Kim teaches away from using titanium as the junction's metal layer. Appx0212-0214. Second, the Board determined that Samsung did not conclusively demonstrate a motivation to combine because Samsung supposedly failed to prove with mathematical certainty that the substitution of Taubenblatt's Ti-TiO_x for Goodnick's Al-Al_2O_3 layers would have decreased the structure's SCR. Appx0214-0217.

As explained below, the Board's conclusions regarding Kim constitute legal error and lack substantial evidence. And the Board's SCR analysis was predicated on an incorrect test. Moreover, the Board's analysis—focused solely on the Goodnick-Taubenblatt combination's use of ***titanium*** as the metal layer (presented for claims 1, 11-12, 15, 23-25, and 28)—is wholly inapplicable to the proposed combinations for claims 20-21 and 26-27 because those combinations ***do not include Taubenblatt's titanium as the metal layer***. Rather, the combinations for those claims rely on Kim's titanium/tungsten alloy.

A. The Board's Analysis Of Kim To Find No Motivation To Combine And Teaching Away Constitutes Legal Error And Is Unsupported By Substantial Evidence

The Board's determination that Kim contradicts Samsung's motivation to combine and teaches away from combining Goodnick and Taubenblatt should be vacated for two reasons. First, the Board improperly compared the proposed combination to Kim's allegedly superior structure, rather than comparing the proposed combination to Goodnick's unmodified structure (upon which the combination undisputedly improves). Second, the Board's reading of Kim to teach away from ***ever*** using titanium as the metal layer of a MIS junction is unsupported by substantial evidence. Indeed, Acorn's expert's concession that using titanium in a MIS junction was "common[]" contradicts the Board's conclusion. Appx28179 (65:16-24).

1. The Board Applied An Incorrect Legal Standard By Comparing The Proposed Combination (Goodnick + Taubenblatt) To *Kim's* Preferred Structure, Rather Than Comparing The Proposed Combination To The *Unmodified Structure* (Goodnick Alone)

"[A]n obviousness showing 'does not require that a particular combination must be the preferred, or the most desirable, combination described in the prior art in order to provide motivation for the [purported] invention.'" *Intel*, 2022 WL 880681, at *4 (citation omitted); *In re Fulton*, 391 F.3d 1195, 1200 (Fed. Cir. 2004); *see also In re Gurley*, 27 F.3d 551, 552-53 (Fed. Cir. 1994).

Samsung argued that a POSITA would have been motivated to replace Goodnick's Al-Al_2O_3 layers with Taubenblatt's Ti-TiO_x layers. Appx23305-23306. The Board relied on a different reference, Kim, to find that a POSITA would not have been motivated to use Taubenblatt's titanium in place of Goodnick's aluminum, because Kim suggests that titanium's thermal properties make it "not suitable" in view of something purportedly better: Kim's titanium/tungsten alloy. In particular, the Board interpreted Kim as describing that "[p]ure titanium" is "not suitable" for use as a "direct contact between titanium and silicon" due to differences in their linear thermal coefficients of expansion. Appx0212 (citing Appx26849 (1:24-30)). In layman's terms, in a structure that includes pure titanium in direct contact with silicon, titanium expands more rapidly than silicon when heated, which can cause defects. Appx26849 (1:24-30). The Board then contrasted pure titanium with ***Kim's*** preferred structure—which instead uses a titanium/tungsten alloy that has a thermal coefficient of expansion closer to that of silicon—and found that a POSITA would have understood Kim to teach away from using pure titanium. Appx0213 (citing Appx26849-26850).

But in so concluding, the Board erred by applying an incorrect legal standard. Specifically, the Board incorrectly compared the thermal properties of the proposed combination's titanium to the thermal properties of Kim's purportedly superior titanium/tungsten alloy. Appx0213. The proper inquiry should instead have been

whether a POSITA would have expected the proposed combination to improve upon ***Goodnick's structure***, which uses aluminum.

In *In re Gurley*, the claims recited an "epoxy based printed circuit material." 27 F.3d at 552. The Examiner rejected the claims as obvious in view of "Yamaguchi" and other prior art. *Id*. Yamaguchi disclosed a circuit board with "an epoxy-impregnated fibrous substrate," but described that epoxy-based material as "inferior to circuit boards made with his polyester-imide resins." *Id*. at 552-53. Although Yamaguchi described epoxy-based materials as "inferior," this Court found that Yamaguchi still demonstrated that the "use of epoxy was known," and concluded that Yamaguchi did not "teach away" from an epoxy-based material because "[a] known or obvious composition does not become patentable simply because it has been described as somewhat inferior to some other product for the same use." *Id*. at 553; *see also In re Fulton*, 391 F.3d at 1200; *In re Mouttet*, 686 F.3d 1322, 1334 (Fed. Cir. 2012) ("[J]ust because better alternatives exist in the prior art does not mean that an inferior combination is inapt for obviousness purposes.").

Here, as in *In re Gurley*, Kim's statement that pure titanium is unsuitable when compared to a purportedly better titanium/tungsten alloy is irrelevant because it is not necessary that the proposed combination "be the preferred, or the most desirable, combination described in the prior art in order to provide motivation for the current invention." *In re Fulton*, 391 F.3d at 1200. Under the proper inquiry, the evidence

is uncontroverted that the proposed Goodnick-Taubenblatt combination improves upon Goodnick's structure because substituting Taubenblatt's titanium for Goodnick's aluminum ***improves*** the thermal match with silicon almost threefold. Appx23753-23754; Appx28993 ¶113 ("[T]he CTE [coefficient of thermal expansion] of Ti offers a ***better match*** with Si than does the CTE of Al. Specifically, the CTE of Si is 2.6×10^{-6} K^{-1}. The CTE of Al is 23.1×10^{-6} K^{-1}. And the CTE of Ti is 8.6×10^{-6} K^{-1}." (emphasis in original) (citing Appx29016-29017)). In other words, when comparing the proposed Goodnick-Taubenblatt combination to Goodnick alone (the structure that the combination modifies), the thermal properties improve. *Id.*

Accordingly, the Board's analysis rests on an improper comparison and warrants remand so that the Board can carry out the obviousness analysis under the correct legal framework—*i.e.*, by comparing the Goodnick-Taubenblatt combination to Goodnick (the base reference that the combination improves upon) rather than to Kim's purportedly more optimal structure.

2. Kim Does Not Teach Away From Using Titanium In A Junction That *Separates* The Titanium From The Silicon With An Interface Layer

"A reference does not teach away" if it "does not criticize, discredit, or otherwise discourage investigation into ***the invention claimed***." *Galderma Labs., L.P. v. Tolmar, Inc.*, 737 F.3d 731, 738 (Fed. Cir. 2013). "While a prior art reference

may indicate that a particular combination is undesirable for its own purposes, the reference can nevertheless teach that combination if it remains suitable ***for the claimed invention***." *Idemitsu Kosan Co. v. SFC Co.*, 870 F.3d 1376, 1381-82 (Fed. Cir. 2017) (emphasis in original) (quoting *In re Zhang*, 654 F. App'x 488, 490 (Fed. Cir. 2016) (nonprecedential)). The analysis is viewed through the lens of a POSITA. *Meiresonne v. Google, Inc.*, 849 F.3d 1379, 1382 (Fed. Cir. 2017).

The Board relied solely on the following statement in Kim to conclude that Kim teaches away from ***ever*** using titanium as the metal layer in a junction:

> Pure titanium, however, is not suitable for contacts as ***direct contact*** between titanium and silicon has shown poor reproducibility due to the large difference in the linear thermal coefficient to expansions of titanium and silicon (the linear coefficient of expansion of titanium being three times the linear coefficient of expansion of silicon).

Appx0212 (quoting Appx26849 (1:24-30)). However, that statement does not support the Board's conclusion.

First, by its very terms, that passage at most suggests that titanium is "not suitable" for contacts because "***direct*** contact between titanium and silicon" results in unmatched thermal properties between those two materials. The passage cannot be read to teach away from using titanium in a M***I***S junction that intentionally ***separates*** the titanium from the silicon with an interface layer—which is what the Goodnick-Taubenblatt combination envisions and what the challenged claims require. *See* Appx23754 n.1. In other words, Kim provides a reason for its statement

that titanium is unsuitable, and that reason is inapplicable to the proposed combination. Indeed, the paragraph cited by the Board explains that it is important to "remov[e]" any oxide from the surface of the silicon, resulting in a direct metal-to-semiconductor contact. Appx26849 (1:12-18) ("[I]t is advantageous to . . . remov[e] the native oxide from the ***metal-silicon*** interface."). Thus, the context surrounding Kim's statement regarding the unsuitability of titanium shows that Kim's teaching is limited to ***direct*** metal-to-semiconductor contacts, not the claimed M***I***S junctions.

Second, a POSITA would not read Kim to teach away from using titanium as the metal in a contact because—as Acorn's expert conceded—"[t]itanium has commonly been used as the metal" in MIS junctions:

> Q. Prior to 2002, were POSITAs aware that they could use titanium as the metal layer in a metal–interface layer–semiconductor junction?
>
> A. ***Titanium has commonly been used as the metal*** often in the form of Ti nitride or ***even pure Ti***. So that was known prior to 2002. So the answer is, yes, people were aware you could use titanium as the metal in the metal-***insulator***-semiconductor junction.

Appx28179 (65:16-24) (cited at Appx23754); *see also* Appx26828 (Taubenblatt). Consistent with that concession, Kim can only reasonably be read to suggest that titanium should not be used as a "***direct*** contact between titanium and silicon"—not

to suggest that titanium should never be used at all. The Board never considered that admission in its teaching-away analysis.

Accordingly, substantial evidence does not support the Board's finding that Kim teaches away from the claimed invention, so this Court should remand for this additional reason (independent of the legal error discussed above in Section IV.A.1).

B. The Board's Analysis Of The Combination's Electrical Properties Was Erroneous Because It Ignored Qualitative Evidence And The Background Knowledge Of A POSITA

The Board's analysis of the combination's electrical properties, relative to the electrical properties of Goodnick alone, was tainted by legal error. The Board failed to consider the background knowledge of a POSITA and the evidence presented during trial that a POSITA would have expected a net reduction in SCR. Instead, the Board cut the inquiry short when it saw no numerical calculations of the combination's SCR. Because the Board failed to apply the correct legal standard, this Court should remand.

Obviousness is an "expansive and flexible" inquiry that must account for the "background knowledge" of a POSITA and the "creative steps" that a POSITA would employ. *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 415, 418 (2007). Motivation to combine may arise from many sources, including "'any need or problem known in the field of endeavor at the time of invention and addressed by the patent'; and the background knowledge, creativity, and common sense of the

person of ordinary skill." *Perfect Web Techs., Inc. v. InfoUSA, Inc.*, 587 F.3d 1324, 1329 (Fed. Cir. 2009) (quoting *KSR*, 550 U.S. at 420). The analysis "not only permits, but ***requires***, consideration of common knowledge and common sense." *DyStar Textilfarben GmbH & Co. v. C.H. Patrick Co.*, 464 F.3d 1356, 1367 (Fed. Cir. 2006) (emphasis in original). Failure to consider the background knowledge of a POSITA as part of the motivation analysis constitutes legal error. *Randall Mfg. v. Rea*, 733 F.3d 1355, 1362-63 (Fed. Cir. 2013) (remanding for Board to reconsider obviousness); *see also Ball Aerosol & Specialty Container, Inc. v. Limited Brands, Inc.*, 555 F.3d 984, 993 (Fed. Cir. 2009).

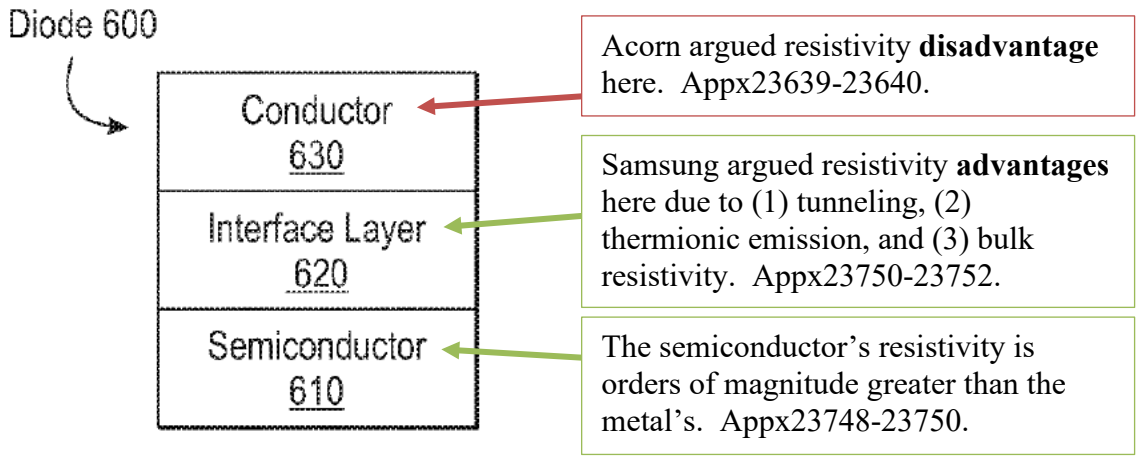
Here, the Board found that Samsung had not met its burden to show motivation because Samsung did not provide numerical "calculations or estimates" of the interface layer's resistivity to definitively prove that the combination reduces the structure's overall SCR. Appx0214-0216. The Board stopped there. The Board did not even attempt to analyze the qualitative evidence showing that a POSITA would have expected the combination's Ti-TiO_x-SiO_2-Si structure to reduce SCR compared to Goodnick's Al-Al_2O_3-SiO_2-Si. Nor did the Board evaluate the background knowledge showing that Acorn's asserted disadvantage (a 16-fold increase in the metal layer's bulk resistivity) was a red herring. The Board simply halted its analysis because Samsung's identified advantages had not been converted

into precise numbers in resistance units.[17] Appx0214-0215. That unduly heightened standard improperly makes the lack of one type of evidence (a numerical calculation in units of Ω) dispositive—just like the formalistic teaching-suggestion-motivation test that *KSR* rejected for being an unduly "rigid" rule. 550 U.S. at 421.

Neither the case law nor logic requires a mathematical calculation or conversion into common units of "ohms" to show motivation. *Cf. Hoffmann-La Roche Inc. v. Apotex Inc.*, 748 F.3d 1326, 1331 (Fed. Cir. 2014) ("Conclusive proof of efficacy is not necessary to show obviousness."). A POSITA "need only be able to recognize, based on her background knowledge, [the modification's] ***potential*** to improve the device" to have motivation. *Unwired Planet, LLC v. Google Inc.*, 841 F.3d 995, 1003 (Fed. Cir. 2016). Here, a POSITA would have weighed the advantages Samsung identified (*e.g.*, better tunneling probability and thermionic emission across the ***interface***) and the disadvantage Acorn asserted (*i.e.*, increase in the ***metal*** layer's bulk resistivity) using her knowledge about the ***relative importance*** of the ***layers***.

[17] Acorn urged the Board to find against Samsung because there was no quantification, but cited no legal authority for why motivation requires quantitative proof. Appx23816-23817 ("Third, the reply fails to show how 'tunneling probability' translates to resistance. Fourth, the reply fails to establish the significance of even a 30X increase [in] tunneling probability . . . . This is a failure of proof by the petitioner."); Appx24140-24141 (Hr'g Tr.) 71:12-72:10 ("How does that translate into actual resistance? . . . [T]here is ***no quantification*** how significant this would be.").

The record is replete with specific evidence of that background knowledge—evidence the Board chose not to analyze. Recall that the claimed MIS junction comprises: (1) a metal; (2) an interface layer containing (a) metal oxide and (b) semiconductor oxide; and (3) a semiconductor:



Appx0265 fig.6; Appx0276 ('395 claim 1). Of those layers, it was well known that the ***metal*** ("Conductor 630") contributes negligible resistance to the overall junction precisely because it is a conductor. Appx23748; Appx28989 ¶107 ("[I]t is fundamentally true that ***semi***conductors . . . are much more resistive than ***conductors*** (metals)."). Indeed, even using Acorn's calculations, the metal layer is a rounding error in the overall structure because the semiconductor is at least 100-fold more resistive. Appx23814.[18] And physics explains why the interface layer is far more important than the metal layer to the overall SCR: unlike a metal that simply

[18] In the worst case, the silicon semiconductor may be up to 10 billion times more resistive than the metal layer. Appx23748; Appx28989 ¶107.

conducts current (the classical way that wires carry electricity), for electricity to pass between the interface layer and the metal, electrons must traverse an energy barrier by tunneling (a "quantum-mechanical process" through the barrier, Appx29524) or by thermionic emission (requiring excess energy to drive the electrons over the barrier). *See* Statement of the Case, *supra* pp. 10-12; Appx28989-28993 ¶¶108-112. Both effects depend on the barrier height. *Id.* Indeed, in a MS junction, it is the "barrier height . . . that . . . determines the electrical properties of the junction." Appx0248 (3:4-6) ('395 patent background section).

Acorn chose to focus its attack on the metal layer, arguing that a POSITA would have been discouraged from making the Goodnick-Taubenblatt combination because titanium is a poor conductor. Appx23639-23640. But because the metal layer is relatively insignificant to the junction's overall SCR, the increased "bulk resistivity" that results from replacing Goodnick's aluminum with Taubenblatt's titanium does not matter to a POSITA. Appx28989 ¶107. Indeed, common sense refutes Acorn's argument that a POSITA would have avoided using titanium due to its unfavorable bulk resistivity. Acorn's expert admitted that, before 2002, "[t]itanium has ***commonly been used*** as the metal . . . even pure Ti . . . ***in the metal-insulator-semiconductor junction***." Appx28179 (65:16-24) (cited at Appx23754). Had POSITAs been so concerned with bulk resistivity of the metal, they would not have "commonly" used titanium as the metal in MIS junctions.

Unlike Acorn, Samsung focused on the layer that really matters to the overall SCR: ***the interface layer***. Appx23749-23750, Appx23752. That is where a POSITA would have focused her efforts, because "the prior art taught that an ***interface layer*** could reduce the specific contact resistance of a metal-semiconductor junction . . . ." Appx23282 (citing, *inter alia*, Appx27103 (Schroen)). Samsung demonstrated that the combination's TiO_x has a lower barrier height than Goodnick's Al_2O_3, which advantageously lowers resistance via two mechanisms. Appx28994-28996 ¶¶114-121. Most importantly, the lower barrier height lowers resistance to tunneling,[19] and the lower barrier height also permits current to pass via thermionic emission. Appx23752; Appx28994-28996 ¶¶114-121. Although Acorn quibbled with the precise numbers, Acorn could not dispute the ***direction*** of those effects: the combination has a lower (better) barrier height and higher (better) tunneling probability than Goodnick, and those effects directionally lower SCR. *See* Appx23813-23814; Appx0211.

Because the Board stopped its analysis when it could not numerically compare the combination's SCR to Goodnick's, the Board never addressed the significant record evidence showing that a POSITA's knowledge and common sense would

[19] This is the same mechanism by which the '395 patent reduces SCR, as Acorn's expert admits. Appx29527 ¶117 ("The Acorn Patents describe the use of a passivation layer (and potentially a MIGS separation layer) [collectively, an interface layer] to ***reduce the interface resistance by tunneling*** . . . .").

have led to the reasonable expectation of a net reduction in SCR. *See* Appx0214-0216. The Board dodged the key factual dispute regarding the relative importance of the interface layer, on the one hand, versus the metal layer, on the other hand, to the overall SCR. And the Board dodged all of the evidence showing that the combination results in lower SCR than the base reference alone. *KSR* does not permit the Board to avoid analyzing the qualitative factual disputes simply because it did not have resistivity "calculations or estimates."

For those reasons, the Board's determinations regarding the electrical properties should be vacated and the case remanded for the Board to evaluate all of the parties' evidence, including the reasons that a POSITA would have been motivated by an expected reduction in SCR in light of her background knowledge and common sense.

C. The Board's Determinations—Premised On Its Analysis Of Taubenblatt's *Titanium*—Must Be Vacated For Claims 20-21 And 26-27 Because The Combinations For Those Claims Use *Kim's Titanium/Tungsten Alloy*—Not Taubenblatt's Titanium

The Board's reasons for finding no motivation to combine Goodnick with Taubenblatt are wholly inapplicable to—and cannot support the Board's determination regarding—claims 20-21 and 26-27 of the '395 patent (Grounds 7-8) (the "Tungsten Claims"). As explained above, the Board determined that a POSITA would not have combined Goodnick with Taubenblatt based on the combination's use of titanium as the structure's metal layer. For the reasons explained above, those

determinations are wrong. Regardless, the combinations for the Tungsten Claims do not use pure titanium; instead, those combinations ***use Kim's titanium/tungsten alloy*** as the claimed metal layer.

The Tungsten Claims recite a metal layer that "includes tungsten." Appx0277.[20] The Petition included Kim in the proposed combinations for Grounds 7 (claims 26-27) and 8 (claims 20-21) and relied on Kim's titanium/tungsten alloy for the structure's metal layer. Appx23330-23333; *see also* Appx23762-23763. But the Board relied solely on its findings regarding the Goodnick-Taubenblatt combination's use of a pure ***titanium*** metal layer when it found the Tungsten Claims not obvious, rather than separately analyzing the Goodnick-Taubenblatt-Kim combination's use of a titanium/tungsten alloy. *See* Appx0220-0221. Therefore, the Board's determination is unsupported by substantial evidence.

1. The Board's Determination That Kim Teaches Away From Using Titanium Cannot Apply To The "Tungsten Claims" Because Samsung Used Kim's Titanium/Tungsten Alloy For The Metal Layer

As summarized in Section IV.A above, the Board determined that Kim teaches away from the Goodnick-Taubenblatt combination because Kim states that "pure titanium" is "not suitable" for use in a contact structure in view of a

[20] Claim 16 similarly "comprises tungsten," but that claim was found unpatentable in the -1207 IPR (Appx0102) and is therefore no longer at issue.

titanium/tungsten alloy's superior thermal properties. Appx0212-0214. That analysis cannot apply to the Tungsten Claims because the combinations for those claims use Kim's titanium/tungsten alloy—not Taubenblatt's titanium—as the claimed metal layer. Kim cannot teach away from using its own preferred alloy.

2. The Board's Analysis Of The Goodnick-Taubenblatt Combination's Electrical Properties Cannot Support Its Findings Regarding The "Tungsten Claims"

As summarized in Section IV.B above, the Board also found no motivation to combine Goodnick with Taubenblatt because it determined that Samsung had not sufficiently proven that other factors (like higher tunneling probability) outweigh that 16-fold increase in the metal layer's bulk resistivity from using pure titanium. Appx0214-0216. But that analysis cannot support the Board's finding of no unpatentability regarding the Tungsten Claims because those claims ***do not use pure titanium*** as the metal layer. Instead, Grounds 7-8 rely on Kim's titanium/tungsten alloy as the metal layer. Appx23331, Appx23333. Acorn did not submit ***any*** bulk resistivity values for a titanium/tungsten alloy, so there is nothing to rebut Samsung's showing that substituting TiO_x for Al_2O_3 in the interface layer reduces the structure's SCR.

Accordingly, the Board's determinations regarding the Tungsten Claims must be vacated and the Court should remand so that the Board can consider Samsung's actual combination.

CONCLUSION

For the foregoing reasons, Samsung respectfully requests that this Court (1) reverse the Board's determinations in IPR2020-01206 and IPR2020-01207 that claims 6, 8, 10-12, 15-19, and 26-29 of the '691 patent and claims 11-12, and 14 of the '395 patent are not anticipated; (2) vacate and remand in IPR2020-01279 and IPR2020-01282. In the alternative, Samsung respectfully requests that this Court vacate the Board's determinations and remand in all four IPRs.

Dated: June 24, 2022 /s/ *Cosmin Maier*

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ADDENDUM

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571-272-7822

Paper 49
Date: January 12, 2022

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD.,
Petitioner,

v.

ACORN SEMI, LLC,
Patent Owner.

IPR2020-01206
Patent 9,905,691 B2

Before BRIAN J. McNAMARA, JOHN R. KENNY, and AARON W. MOORE, *Administrative Patent Judges.*

McNAMARA, *Administrative Patent Judge*.

JUDGMENT
Final Written Decision
Determining Some Challenged Claims Unpatentable
Dismissing Patent Owner's Motion to Exclude
35 U.S.C. § 31]8(a)

I. BACKGROUND

On January 13, 2021, we instituted an *inter partes* review of claims 1–4, 6, 8, 10–13, 15–20, 22, and 25–30[1] of U. S. Patent No. 9,905,691 B2 ("the '691 Patent"). Paper 22 ("Dec. to Inst."). Patent Owner filed a Patent Owner Response (Paper 29, "PO Resp.") and a Notice of Jury Verdict in related district court litigation (Paper 31, "Notice"; Ex. 2121 "Jury Verdict"). Petitioner filed a Petitioner Reply (Paper 34, "Pet. Reply") and Patent Owner filed a Sur-reply (Paper 40, "PO Sur-reply"). Patent Owner also filed a Motion to Exclude some of the testimony its expert witness, Dr. Kelin J. Kuhn (Paper 41 "Mot."), Petitioner filed an Opposition to Patent Owner's Motion to Exclude (Paper 43, "Opp. to Mot."), and Patent Owner filed a Reply to Petitioner's Opposition to Patent Owner's Motion to Exclude (Paper 44, "Reply") a transcript of an oral hearing held on October 13, 2021 (Paper 48, "Hr'g. Tr.") has been entered into the record.

We have jurisdiction under 35 U.S.C. § 6. This Final Written Decision is issued pursuant to 35 U.S.C. §318(a). We base our decision on the preponderance of the evidence. 35 U.S.C. § 316(e); 37 C.F.R. § 42.1(d).

Having reviewed the arguments of the parties and the supporting evidence, we conclude that Petitioner has demonstrated by a preponderance of the evidence that challenged claims 1–4, 13, 20, 22, and 25 are unpatentable. Petitioner has not demonstrated that the remaining challenged claims (claims 6, 8, 10–12, 15–19 and 26–29) are unpatentable.

II. THE '691 PATENT

The '691 patent "relates to a process for depinning the Fermi level of a semiconductor at a metal-interface layer-semiconductor junction and to

[1] Claim 30 has been disclaimed and is not addressed in this Decision.

devices that employ such a junction." Ex. 1001, 1:27–29. The '691 patent explains that Schottky's theory concerning the ability of a junction to conduct current in one direction more favorably than in the other direction, i.e., the rectifying behavior of a metal/semiconductor junction (e.g., an contact between the metal and the semiconductor). *Id*. at 1:33–48. As the barrier height at the metal/semiconductor interface determines the electrical properties of the junction, controlling the barrier height is an important goal. Id. at 3:4–10.

The '691 patent further explains that Schottky's theory postulates the height of the barrier, as measured by the potential necessary for an electron to pass from the metal to the semiconductor, is the difference between the work function of the metal (i.e., the energy required to free an electron at the Fermi level (the highest occupied energy state of the metal at T=0)) and the electron affinity of the semiconductor (i.e., the difference between the energy of a free electron and the conduction band of the semiconductor); but experimental results indicate a weaker variation of barrier height with work function than implied by this model. *Id.* at 1:49–2:3.

To explain the discrepancy between the predicted and observed behavior, Bardeen introduced the concept of semiconductor surface states, i.e., energy states within the bandgap between the valence and conduction bands at the edge of the semiconductor crystal that arise from incomplete covalent bonds, impurities, and other effects of termination. *Id*. at 2:4–18, Fig. 1 (showing dangling bonds that may be responsible for surface states that trap electrical charges). Although Bardeen's model assumes that surface states are sufficient to pin the Fermi level in the semiconductor at a point between the valence and conduction bands, such that the barrier height

should be independent of the metal's work function, in experiments, this condition is observed rarely. *Id*. at 2:19–25.

Further, according to the '691 patent, Tersoff proposed that the Fermi level of a semiconductor is pinned near an effective "gap center" due to metal induced gap states (MIGS), which are energy states in the bandgap of aluminum/silicon junction), depends upon a barrier at the surface of the semiconductor that become populated with metal. *Id.* at 2:35–44. Thus, the wave functions of electrons in the metal do not terminate abruptly at the surface of the metal, but decay in proportion to the distance from the surface, extending inside the semiconductor. *Id.* at 2:44–48.

> To maintain the sum rule on the density of states in the semiconductor, electrons near the surface occupy energy states in the gap derived from the valence band such that the density of states in the valence band is reduced. To maintain charge neutrality, the highest occupied state (which defines the Fermi level of the semiconductor) will then lie at the crossover point from states derived from the valence band to those derived from the conduction band. This crossover occurs at the branch point of the band structure.

Id. at 2:48–56. The '691 patent also notes one further surface effect on diode characteristics is inhomogeneity, i.e., "if factors affecting the barrier height (e.g., density of surface states) vary across the plane of the junction, the resulting properties of the junction are found not to be a linear combination of the properties of the different regions." *Id.* at 2:63–67.

According to the '691 patent, "a classic metal-semiconductor junction is characterized by a Schottky barrier, the properties of which (e.g., barrier height) depend on surface states, MIGS and inhomogeneities." *Id.* at 2:67–3:3. "Before one can tune the barrier height, however, one must depin the Fermi level of the semiconductor." *Id.* at 3:10–12. The '691 patent seeks to

depin the Fermi level of the semiconductor while still permitting substantial current flow between the metal and the semiconductor. *Id.* at 3:12–15. The '691 patent describes depinning the Fermi level as follows:

> By depinning the Fermi level, the present inventors mean a condition wherein all, or substantially all, dangling bonds that may otherwise be present at the semiconductor surface have been terminated, and the effect of MIGS has been overcome, or at least reduced , by displacing the semiconductor a sufficient distance from the metal.

Id. at 3:30–35.

The '691 patent achieves this goal using thin interface layers disposed between a metal and a silicon based semiconductor to form a "metal-interface layer-semiconductor junction" whose thickness varies with a corresponding minimum specific contact resistance, which depends on the materials used and allows for depinning the Fermi level while permitting current to flow when the junction is appropriately biased. *Id.* at 3:19–30; *see also id.* at 12:59–14:17, 14:29–52, Figs. 6, 8. "Minimum specific contact resistances of less than or equal to approximately 10 Ω-μm^2 or even less than or equal to approximately 1Ω-μm^2 may be achieved for such junctions in accordance with the present invention." *Id.* at 3:36–39. Such low contact resistances are achieved by selecting a metal with a work function near the conduction band of the semiconductor for n-type semiconductors, or a work function near the valence band for p-type semiconductors. *Id.* at 5:19–23. Figure 8 of the '691 patent is reproduced below.

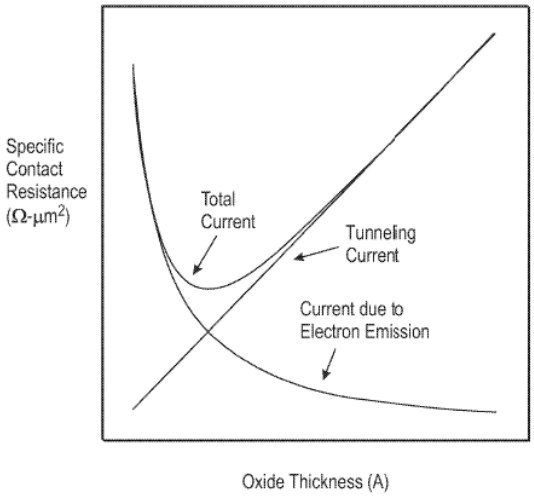


Figure 8 of the '691 patent

Figure 8 of the '691 patent is a graph of interface specific contact resistance versus interface thickness for a structure where the work function of the metal is the same as the electron affinity of the semiconductor, such that the Fermi level of the metal lines up with the conduction band of the semiconductor. *Id.* at 14:29–35. According to the '619 patent, Figure 8 shows that at large thicknesses, the interface layer poses significant resistance to current, but as interface layer thickness decreases, resistance falls due to increased tunneling current. *Id.* at 14:29–38. However, at some point, as the interface layer gets thinner, the effect of MIGS increasingly pulls the Fermi level of the metal down towards the mid-gap of the semiconductor, creating a Schottky barrier and increasing resistance. *Id.* at 14:38–42. Thus, there is an optimum thickness where the resistance is at a minimum and the effect of MIGS has been reduced to depin the metal and lower the Schottky barrier, but the layer is sufficiently thin to allow significant current across the interface layer, such that specific contact resistances of less than or equal to approximately 2500 Ω-m^2, 1000 Ω-m^2,

100 Ω-m^2, 50 Ω-m^2, 10 Ω-m^2, or less than 1 Ω-m^2 can be achieved. *Id.* at 14:45–52,

In one embodiment, the interface layer may be a monolayer or several monolayers of passivating material (e.g., a nitride, oxide, oxynitride, arsenide, hydride and/or fluoride) and may include a separation oxide layer, the specific contact resistance of the electrical device is less than 10 Ω-μm^2. *Id.* at 3:40–53; *see also* 10:43–54. In another embodiment, the interface layer is made up of a passivation layer fabricated by exposing the semiconductor to nitrogenous material (e.g., ammonia (NH_3), nitrogen (N_2) or unbound gaseous nitrogen (N) generated from a plasma process) and while heating the semiconductor in a vacuum chamber. *Id.* at 3:44–61. Another embodiment uses an interface layer of passivating material disposed between the surface of a semiconductor and a conductor in which the interface is of sufficient thickness to reduce the effect of MIGs in the semiconductor and passivates the semiconductor but, because the thickness of the interface layer is chosen to provide minimum, or near minimum, specific contact resistance for the junction, significant current may flow between the conductor and the semiconductor. *Id.* at 3:62–4:8. In other embodiments, the interface layer is configured to allow a Fermi level of the conductor to (i) align with a conduction band of the semiconductor, (ii) align with a valence band of the semiconductor, and (iii) to be independent of the Fermi level of the semiconductor, allowing current to flow between the conductor and the semiconductor when the junction is biased because the thickness of the interface layer corresponds to a minimum or near minimum contact resistance for the junction. *Id.* at 4:8–18. Specific contact resistances of less than or equal to approximately 2500 Ω-m^2, 1000 Ω-m^2,

100 Ω-m^2, 50 Ω-m^2, 10 Ω-m^2, or less than 1 Ω-m^2 reportedly can be achieved. *Id.* at 4:19–22, 14:45–52.

III. ILLUSTRATIVE CLAIM

Independent claim 1, reproduced below to include the subject matter of a certificate of correction issued on May 15, 2018 (Ex. 1001, 21), and including claim element designations (i) through (vii) used in the Petition, is representative of the subject matter of the '691 patent:

> 1. (i) A structure, comprising (ii) a semiconductor region in a substrate, (iii) a metal electrical contact to said semiconductor region, (iv) a metal oxide layer, (v) a passivating dielectric tunnel barrier layer between said semiconductor region and said metal electrical contact, (vi) said semiconductor region being electrically connected to said metal electrical contact through said passivating dielectric tunnel barrier layer and said metal oxide layer, (vii) wherein said passivating dielectric tunnel barrier layer comprises a semiconductor oxide.

IV. GROUNDS OF INSTITUTION

We instituted trial on the following ground:

Claim(s) Challenged	35 U.S.C. §	Reference(s)/Basis
1–4, 6, 8, 10–13, 15–20, 22, and 25–30[2]	102	Grupp '483[3]

V. CLAIM CONSTRUCTION

In the Decision to Institute, we noted that the term "specific contact resistivity" appears in challenged claims 18 and 25–29, but is not used in the '691 patent Specification. Dec. to Inst. 12. Recognizing that a person of

[2] Claim 30 was disclaimed on October 14, 2020 and is no longer before us. *See* Ex. 2004.
[3] U.S. Patent No. 7,176,483 B2, issued Feb. 13, 2007 (Ex. 1015).

ordinary skill would have understood "specific contact resistivity" in claim 18 and 25–29 to refer to "specific contact resistance," we construed the terms "specific contact resistivity" and "specific contact resistance" to be interchangeable.

VI. ANALYSIS OF PRIOR ART CHALLENGES

A. Priority Issue

Patent Owner characterizes the invention as recognizing "that satisfactorily depining the Fermi level in a metal-semiconductor junction involves both satisfying dangling bonds on the surface of the semiconductor (*i.e.*, passivation) and reducing the effects of metal-induced gap states (MIGS)." PO Resp. 4 (citing Ex. 1001, 3:30–35). According to Patent Owner "the Acorn inventors found that the thickness of an appropriate interface layer could be optimized to result in minimum total resistivity/resistance, as illustrated in Figure 8 of the Acorn patents." *Id.* (citing Ex. 1001, Fig. 8)

Petitioner contends that Grupp '483 discloses each of the limitations of claim 1. Pet. 26–32. Patent Owner does not dispute Petitioner's assertion that Grupp '483 discloses all of the limitations of claim 1, but Patent Owner asserts that Grupp '483 cannot be applied as a prior art reference because the '691 patent is entitled to priority over Grupp '483 based on U.S. Patent No. 7,084,423 ("the '423 patent") filed on August 12, 2002. PO Resp. 38.

1. The district court litigation

Patent Owner argues that Petitioner abandoned its inadequate written description of a generic metal oxide arguments as an invalidity defense in *Acorn Semi, LLC v. Samsung Electronics Co. Ltd.*, Civil Action No. 2:19-cv-347 (E.D. Tex.) ("the Acorn Litigation"). PO Resp. 2–3, 38 (citing Ex. 2067, 2). As this issue was not tried in the district court, there was no

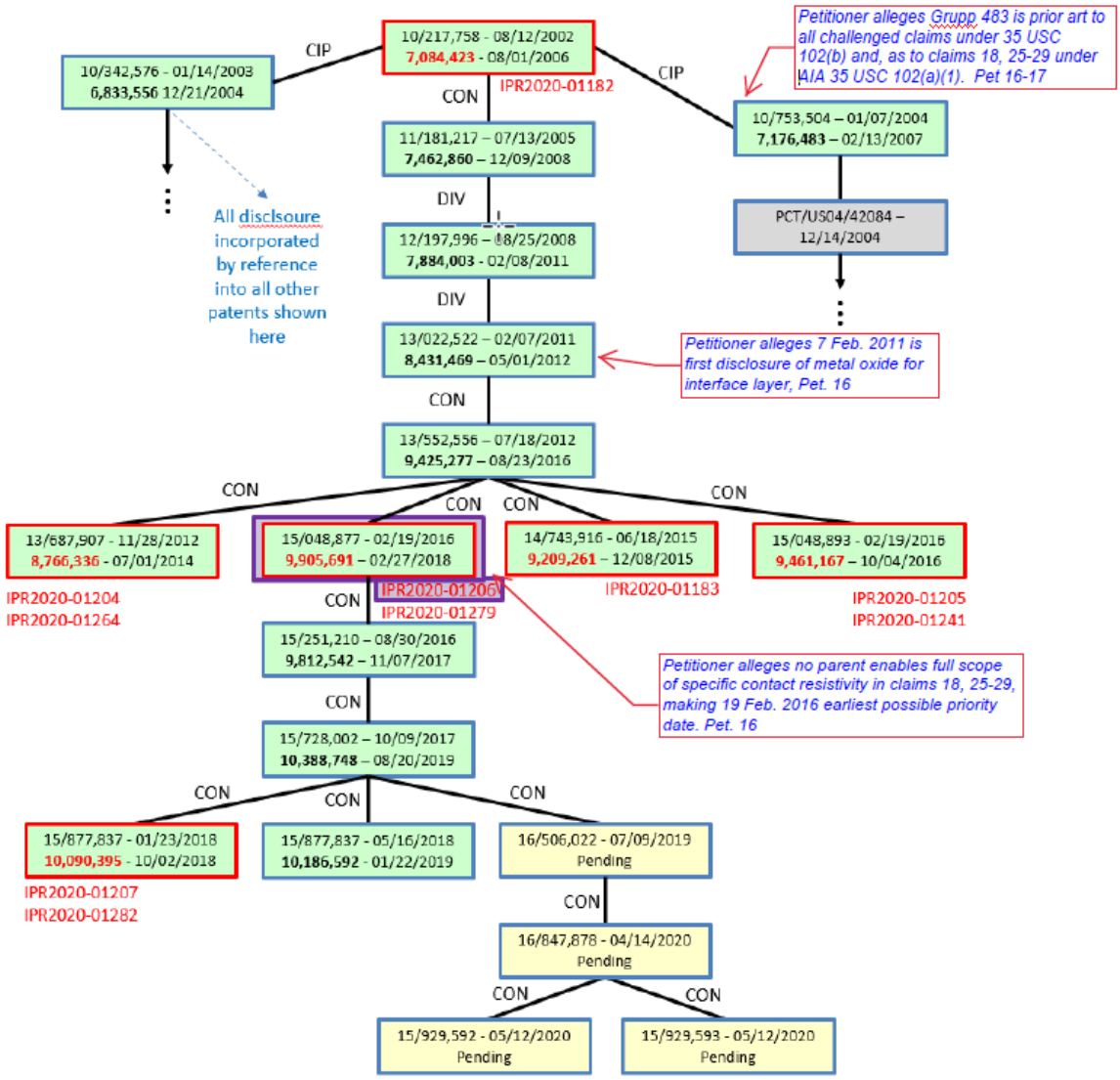
verdict or finding of invalidity. *See*, Ex. 2121. Petitioner has not withdrawn this challenge ground or abandoned the contest in this forum. We draw no inferences from how Petitioner conducted its district court litigation, recognizing that Petitioner may adopt strategies it considers appropriate in the context of procedural and substantive matters that may be different in each forum. Therefore, we accord no weight to Petitioner's withdrawal of its invalidity defense in the district court.

We further note that claims 6, 8, and 19 of the '691 patent were the subject of a verdict in the Acorn Litigation. *See* Notice; Jury Verdict. The jury found claims 6, 8, and 19 of the '691 patent were infringed. Jury Verdict, 4.

2. Priority claims and written description

Petitioner contends the challenged claims are not entitled to any priority date before February 7, 2011, rendering Grupp '483, which is a member of the family of patents that includes the '691 patent, prior art to the '691 patent. Pet. 15–17.

A chart showing a partial view of the family tree including the '691 patent and further annotated with italicized text boxes that identify some of Petitioner's contentions is provided below.



Partial Family of Patent Including '691 Patent

Dec. to Inst. 15. Petitioner contends that patentee did not describe the genus of the "metal oxide layer" as recited in the claims of the '691 patent until the patentee filed the claims of U.S. application 13/022,522 ("the '522 application") on February 7, 2011. Pet. 16 (citing Ex. 1010, 48; Ex. 1016, Schubert Decl. ¶¶ 89–90). Petitioner further contends that in no priority application did the patentee enable the full scope of the recitation in claims 18 and 25–29 of a specific contact resistivity less than $1\Omega\text{-m}^2$. Thus,

according to Petitioner, the priority date of the '691 patent is no earlier than its filing date, i.e., February 19, 2016. *Id.*

Patent Owner disputes Petitioner's contentions: (i) that the priority applications filed before 2011 (pre-2011 priority applications) do not support the recited metal-oxide layer and (ii) that none of the priority applications support the recited specific contact resistance range. According to Patent Owner, the priority date of the '691 patent is August 1, 2006 (the filing date of the '473 patent), and Grupp '483 is not prior art to the '691 patent. *Id.*

3. Metal Oxide Layer and Oxide of Titanium Claims

Patent Owner contends that Petitioner's initial challenge, based on a lack of written description of a metal oxide, did not address the claims individually and did not distinguish claims drawn to "a metal oxide" (challenged claims 1–4, 13, 20, 22, 25) from narrower claims drawn to a structure in which "the metal oxide comprises an oxide of titanium" (claims 6, 8, 10–12, 15–19) and "the metal oxide separation layer comprises an oxide of titanium" (claims 26–29). PO Resp. 2, 37–43; PO Sur-reply 5–7 (citing Pet. 17–20). Patent Owner states that its Patent Owner Response "simply pointed out the petition's failure to specifically address these 'oxide of titanium' dependent claims," but "did not open the door for the petitioner to present new theories directed at these dependent claims or to fill the identified gap in the petition." PO Sur-reply 6. According to Patent Owner "[i]t is unfair for the reply to belatedly make those arguments now that it is too late for Acorn to respond with rebuttal evidence, as due process and the APA require." *Id.* at 7 (citing 5 U.S.C. § 556(d)).

Patent Owner emphasizes that claims 1–4, 13, 20, 22, and 25 (the metal oxide claims) do not specifically recite "an oxide of titanium." PO Resp. 44. The Petition states that every claim of the '691 patent recites a

metal oxide interface layer. Pet. 18. As the language of all of the oxide of titanium claims begins with "the metal oxide comprises" or "the metal oxide separation layer comprises," the oxide of titanium claims recite a further limitation on the metal oxide feature. Patent Owner relies on the disclosure of TiO_2, itself an oxide of titanium, as support for its arguments that the priority applications provide an adequate written description of both the metal oxide claims (PO Resp. 44–48) and the oxide of titanium claims (*id.* at 33–43). The Petition states the "relevant question is whether the earlier parent applications' statement that

> [s]pacer layers may be used with lower barriers (e.g., TiO_2 has a barrier of less than 1 eV)" provides written description of the entire genus of metal oxide interface layers. ('691 Patent at 14:45-52.) And the answer is no: some metal oxides present considerably higher barriers than the 'barrier of less than 1 eV' ascribed to TiO_2.

Pet. 19.

We address the priority issues concerning metal oxide claims and the oxide of titanium claims separately below..

4. The Metal Oxide Claims (Claims 1–4, 13, 20, 22, 25)

According to Petitioner, the first time any of the applications "arguably disclosed a generic 'metal oxide' interface layer is in the originally filed claims of U.S. Patent App. No. 13/022,522 filed on February 7, 2011." *Id.* (citing Ex. 1010, 48 [*see* claims 15, 16]; Ex. 1016, Schubert Decl. ¶¶ 89–91). Petitioner acknowledges that earlier applications described a "possible example of a metal oxide interface layer" in the form of a TiO_2 spacer layer. *Id.* (citing Ex. 1001, 14:45–52; Ex. 1016, Schubert Decl. ¶ 90; *see, e.g.,* Ex. 1002 ¶¶ 82–85). According to Petitioner, however, the disclosed TiO_2 spacer layer fails to describe the genus of the recited metal

oxide interface layer even though that same description anticipates the challenged claims. *See In re Curtis*, 354 F.3d 1347, 1358 (Fed. Cir. 2004) ("A patentee will not be deemed to have invented species sufficient to constitute the genus by virtue of having disclosed a single species.").

Referring to limitation (iv) of claim 1 ("a metal oxide layer") Petitioner argues that Grupp '483 anticipates claim 1 because, among other things, it discloses a separation layer that can be an oxide (Pet. 29 (citing Ex. 1015, 11:35–38 ("in some cases [such] passivation layers are combined with separation layers (e.g., made of an oxide) to complete the interface layer")) and the separation can be a spacer layer of TiO_2 (*id.* (citing Ex. 1015, 18:65–67 ("[s]pacer layers may be used with lower barriers (e.g., TiO_2 has a barrier of less than 1eV))"). Thus, according to Petitioner, "Grupp '483 discloses an interface layer that includes a metal oxide layer; titanium dioxide." *Id.* (citing Ex. 1016, Schubert Decl. ¶¶ 116–117). At the same time, Petitioner argues that Grupp '483 can be applied as a reference because the exact same language in the pre-2011 priority applications fails to provide a written description of the genus of the recited "metal oxide layer." Pet. 18–19. *See, e.g., Yeda Research and Dev. V. Abbot GmbH & Co. KG*, 837 F.3d 1341, 1344–45 (Fed. Cir. 2016).

Patent Owner notes that independent claim 1 recites "a metal oxide layer" distinct from "a passivating dielectric tunnel layer" and that independent claim 25 recites "the interface layer comprising a metal oxide separation layer and a semiconductor oxide passivation layer." PO Resp. 44. According to Patent Owner, the '423 patent Specification filed in 2002 supports the subgenus "metal oxide" in two ways: (1) by its disclosure of titanium dioxide (TiO_2) as a species and (2) by its disclosure of oxide

spacer/separation layers in more general terms. *Id.* (citing Ex. 1003, 17:59–61).

Patent Owner argues that a person of ordinary skill would understand that the spacer layer is adjacent to the metal and would recognize that a desirable embodiment for the spacer layer (i.e., the MIGs separation layer) is an oxide of whatever metal is used as the metal in the metal-semiconductor junction. PO Resp. 44–45 (citing Ex. 2070, Declaration of Dr. Kelin Kuhn ("Kuhn Decl.") ¶ 98). As Patent Owner notes, claim 1 recites distinct passivation and metal oxide layers. PO Resp. 44, 46. According to Patent Owner, a person of ordinary skill would understand from the Specification that the oxide/separation layer, when present, is distinct from the passivation layer (citing Ex. 2070, Kuhn Decl. ¶¶ 107–109). According to Patent Owner, the placement of a metal adjacent to an oxide of that metal is very likely to be chemically more stable than having the metal adjacent to some other oxide that is not an oxide of the same metal. *Id.* (quoting Ex. 2070, Kuhn Decl. ¶ 98). Patent Owner asserts that (1) the metal-metal oxide relationship of Ti-TiO_2 and (2) the fact the metal and the space layer are adjacent are structural features common to the metal oxide genus such that a person of ordinary skill would visualize and recognize members of the genus. *Id.* at 45. Patent Owner also argues that a person of ordinary skill would understand from the Specification that the oxide spacer/separation layer should be a dielectric and that, from the list of metals in the patent, a person of ordinary skill would realize "appropriate dielectrics that do not passivate semiconductors and are oxides are metal oxides in the families such as aluminum oxides, titanium oxides, tantalum oxides, and zinc oxides." PO Resp. 46 (citing Ex. 2070, Kuhn Decl. ¶ 110).

Petitioner notes that the priority applications disclose only one species (TiO_2) of the titanium oxide genus, which includes at least the following species: TiO, Ti_2O, Ti_3O, TiO_2, Ti_2O_3, Ti_3O_5, and Ti_4O_7. Pet. Reply 3, 7–8 (citing Ex. 1042, Transcript of Deposition of Dr. Kelin Kuhn ("Kuhn Tr.") 114:10–18 (testifying that she did not know how many chemical compounds exist in the titanium oxide family)). Petitioner asserts that the single disclosed species TiO_2 is not representative of the entire genus of metal oxides and does not describe features common to all members of the claimed genus. *Id.* at 3. Petitioner further argues that its position is even more compelling when the number of metal oxides is compounded to include multiple metals. *Id.* at 3–4. Petitioner compares the characteristics of three metal oxides commonly used in semiconductor devices as illustrating disparate bandgap, melting point, and electron affinity properties, *id.* at 4–5 (citing Ex. 1047, Second Declaration of Dr. Fred Schubert ("Schubert Decl. 2") ¶ 51). Petitioner cites the testimony of Dr. Kuhn confirming that such characteristics are not discussed in the patent, as evidence that the patent fails to explain which properties one should consider when determining what would be encompassed by the claimed structures (*see, id.* at 4, citing Ex. 1042, Kuhn Tr., 108:5–19 (concerning conductivity), 109:9–11, 110:12–15 (concerning melting point), 110:17–20 (concerning bandgap energy), 112:16–113:7 (concerning electron affinity), 111:20–112:1 (concerning diffusivity); 112:2–9 (concerning hardness), 112:10–15 (concerning optical properties), 51:15–24 (concerning crystal structure).

Patent Owner argues that the patent's disclosure of TiO_2 supports claiming the metal oxide genus because "the metal oxide is the spacer layer in the claimed arrangement, and one important structural feature common to metal oxides in that role is that they are dielectrics, according to the

specification." PO Sur-reply 12 (citing Ex. 2070, Kuhn Decl. ¶¶ 107, 109 as "concluding that Acorn specification teaches POSITA to use a dielectric as the spacer layer"). Stating that Petitioner "does not dispute that fact," Patent Owner contends that Petitioner's arguments concerning the many possible metal oxides lacks "any analysis narrowing those metal oxides to relevant ones that are solid non-passivating dielectrics." *Id.* (citing *In re Smythe*, 480 F.2d 1376, 1385 (CCPA 1973); *In re Myers*, 410 F.2d 420, 426 (CCPA 1969)).

Patent Owner further cites four "blazemarks" in addition to the TiO_2 example in the Specification as "sufficient for a POSITA to recognize from the disclosure that the oxide spacer layer could be (most likely is) a metal oxide.)" According to Patent Owner:

> the patent teaches that the MIGS separation layer [1] is an optional layer added in addition to the passivation layer, [2] is sandwiched between the metal and the passivation layer, [3] is not itself a passivation layer, and [4] has the function of providing the proper thickness and band structure so that the MIGS states arising in the metal cannot pin the Fermi level of the junction. A POSITA would recognize that insulating metal oxides in families such as aluminum oxide, titanium oxide, tantalum oxide, and zinc oxide, which are generally considered to be non-passivating, would be appropriate choices for the MIGS separation layer that the inventors had contemplated as part of a two-layer (passivation layer + separation layer) interface.

PO Resp. 46–47 (quoting Ex. 2070, Kuhn Decl. ¶ 112). As Petitioner notes, however, these four purported blazemarks are not found in the Specification. Moreover, Petitioner points out that under cross-examination, Dr. Kuhn conceded that she has not opined on whether the metal oxide separation layer cannot have a passivation function. Pet. Reply 14–15 (citing Ex. 1042, Kuhn Tr. 47:15–22; Ex. 1047, Schubert Decl. ¶¶ 52–57).

Petitioner contends that allowing Patent Owner to claim priority back to 2002 based on the disclosure of TiO_2 "would result in the challenged claims impermissibly encompassing metal oxide interface layers in metal-semiconductor junctions that were only later invented" and "***to this day*** have not yet been invented and could not have been in the inventors' possession in 2002." *See* Pet. Reply 6–7 (citing Ex. 1042, Kuhn Tr. 99:6–23, 82:15–21 (asserting the claims would cover a newly invented species of titanium oxide or a gold oxide currently though to be unsuitable)).

"The goal [of] the written description doctrine [is to] giv[e] the incentive to actual invention and not 'attempt[s] to preempt the future before it has arrived." *Ariad Pharms., Inc. v. Eli Lilly & Co.*, 598 F.3d 1336, 1353 (Fed. Cir. 2010) (*en banc*). It is undisputed that the priority applications disclose only a single metal oxide species, i.e., TiO_2. As Petitioner points out, the first mention of a metal oxide was in U.S. Patent Application No. 13/022,522, filed on Feb. 7, 2011. Pet. 16; Ex. 1010, 48 (*see* claim 15, depending from independent claim 3). Patent Owner has identified no discussion of using a metal oxide in the entire Specification or the specification of any other priority application. As detailed above, Patent Owner relies solely on its assertions about what a person of ordinary skill would have understood in the relevant context.

A review of Dr. Kuhn's Declaration testimony that forms the basis for Patent Owner's responsive arguments concerning written description in the '423 patent (the patent issuing from the first application submitted in August 2002) is illustrative of the extent to which Patent Owner relies on the understanding of a person of ordinary skill, rather than actual written description in the '423 patent. Dr. Kuhn begins her analysis with the disclosure in the '423 patent that TiO_2 as an example of a "spacer layer" or

"separation layer" (the terms being used synonymously) with Ti as a possible metal for the metal-semiconductor junction. Ex. 2070, Kuhn Decl. ¶ 97. Referring to the spacer layer as the "MIGS separation layer," Dr. Kuhn asserts that a person of ordinary skill would recognize from the TiO_2 layer example that an oxide of whatever metal is used as the metal in the metal-semiconductor junction would be desirable. *Id.* ¶ 98. Dr. Kuhn cites no teaching in the '423 patent supporting this assertion, but states that a person of ordinary skill would recognize the value of a configuration in which the placement of a metal next to an oxide of that metal "is very likely to be more chemically stable than having the metal adjacent to some other oxide." *Id.*

According to Dr. Kuhn, the fact that the "'423 patent states that the separation layer may be an oxide in general, would have directed a person of ordinary skill to metal oxides in particular for reasons I will next explain." *Id.* ¶ 100. Nevertheless, after stating that metals other than titanium are disclosed in the patent, Dr. Kuhn acknowledges that "not all of these metals have oxides that would be acceptable as a spacer layer, many of them do have such oxides the details of which I describe in paragraphs 101-110." *Id.* ¶ 99. Noting that the interface layer may be a passivation layer or a single or compound layer including both a passivating material and an additional separation material, Dr. Kuhn states the layers should be well-behaved materials not displaying deleterious effects that would prevent their use in electrical devices. *Id.* ¶¶ 101–102. Dr. Kuhn next notes that patent states "the interface layers serve to (i) chemically passivate the semiconductor from the metal surface 540 and (ii) to displace the semiconductor sufficiently to eliminate or at least reduce the effect of MIGS." *Id.* (quoting Ex. 9:50–53). According to Dr. Kuhn, because the patent explains that the

passivation layer alone may not be sufficient to provide MIGS separation, an additional MIGS separation may be required. *Id.* ¶ 104. Dr. Kuhn states: "From this description, a POSITA would understand that the separation layer, when paired with a passivation layer, does not itself perform a passivation function, but is solely intended to provide the proper thickness and band structure so that the MIGS states arising in the metal cannot pin the Fermi level of the junction." *Id.*

Dr. Kuhn next notes that the '423 patent discloses passivation layers using N and/or O may not require distinct separation layers and asserts that "[f]rom this a POSITA would understand that a passivation material that is *also* an oxide (such as silicon dioxide or silicon oxy-nitride) would not be considered the distinct separation layers recited in the challenged claims, but rather a passivation layer." *Id.* ¶ 105 (citing Ex. 10:5–7). Based on the '423 patent's disclosure that "in some cases such passivation layers are combined with separation layers (e.g., made of an oxide) to complete the interface layer" (Ex. 10:48–50), Dr. Kuhn asserts that "a POSITA would understand that the separation layer is intended to be an oxide, but not one with the function of passivation." *Id*. ¶ 106.

Noting that "the patent provides extensive teachings on metals versus non-metals" and the relationship between metals, conductive materials, and conductors (*id*. ¶ 108), Dr. Kuhn posits that a person of ordinary skill would have understood or recognized the following:

> (i) that "using a metal for MIGS separation would ***not*** provide MIGS separation (the metal would simply make more MIGS states)";
>
> (ii) that "using metal-like materials for the MIGS separation layer (i.e., metals, semi-metals (metalloids), and semiconductors would carry a similar risk of not fully

> suppressing MIGS states due the band structure of the materials";
>
> (iii) that "the desired embodiments for the MIGS separation layer in a two-layer (passivation layer + separation layer) arrangement would be dielectrics and additionally would include (as per the patent's clarification that a passivation layer is distinct from a separation layer) dielectrics that do not passivate or only weakly passivate the semiconductor";
>
> (iv) that "the position of the MIGS separation layer (always between the metal and the passivation layer) suggests metal oxides of the parent metal to improve chemical stability";
>
> (v) that looking to "the complete list of metals provided in the patent (Al, In, Ti, Cr, Ta, Cs, Mg, Er, Yb, Mn, Pb, Ag, Y, Zn, Pt, Au, W, Ni, Mo, Cu, Co and Pd) . . . the most appropriate metal oxides would be conventional insulators with significant preexisting data due to the world-wide emphasis on high-k dielectrics at the time of the patent (families such as aluminum oxide, titanium oxide, and tantalum oxide)";
>
> (vi) that there was "the possibility of using insulators from materials well-established in the semiconductor industry, although perhaps not as well-researched as the high-k materials (families such indium oxide, magnesium oxide, zinc oxide, tungsten oxide, molybdenum oxide and yttrium oxide)";
>
> (vii) that "certain materials might have appropriate insulating properties but would not be appropriate for semiconductor fabrication due either to well-known mismatches between materials properties and typical semiconductor processing conditions (e.g. families such as silver oxide and gold oxide) or environmental issues (e.g. families such as lead oxide)"; and
>
> (viii) that "[t]he remaining oxides would be recognized as inappropriate choices as they are semiconductors or semimetals (metalloids)."

Ex. 2070, Kuhn Decl. ¶¶ 109–110.

Petitioner's expert, Dr. Schubert, identifies a large number of metal oxides and multiple metal oxides that is expanded by multiple equilibrium species and notes that the metal oxide genus would be even further expanded

to include non-equilibrium species. Ex. 1047, Schubert Decl. 2 ¶¶ 18–22. Dr. Schubert further emphasizes the significant variation in physical and chemical properties of such metal oxides. *Id.* at ¶¶ 27–51.

Much of Dr. Kuhn's analysis is premised on her assessment of the mental steps that an ordinarily skilled artisan theoretically might have taken after reviewing the minimal disclosure in the '423 patent. The '423 patent does not discuss any properties of metal oxides (other than the lower barrier of the metal oxide TiO_2) or design considerations concerning the selection of particular oxides to use in the claimed structure, particularly in the context of MIGS separation. Dr. Kuhn cites very little, if any, evidence to support her testimony regarding the knowledge of an ordinarily skilled artisan. Thus, we do not credit this analysis as showing that an ordinarily skilled artisan would have found that the inventors of the pre-2011 priority applications possessed the recited genus. *See Ariad*, 593 F.3d at 1352 (a description that merely renders the invention obvious does not satisfy the written description requirement); *Power Oasis Inc. v. T-Mobile USA*, 522 F.3d 1299, 1306 (Fed. Cir. 2008) ("Entitlement to a filing date does not extend to subject matter which is not disclosed, but would be obvious over what is expressly disclosed.") (quoting *In re Huston,* 308 F.3d 1267, 1277 (Fed. Cir. 2002), quoting *Lockwood v. Am. Airlines, Inc.,* 107 F.3d 1565, 1571–72 (Fed. Cir. 1997)); *Martin v. Mayer,* 823 F.2d 500, 505 (Fed. Cir. 1987) (holding that the written description requirement is "not a question of whether one skilled in the art *might* be able to construct the patentee's device from the teachings of the disclosure . . . . Rather, it is a question whether the application necessarily discloses that particular device") (emphasis in original).

Patent Owner also argues that policy "concerns about overclaiming – the policy concerns that animate the written description requirement" are

inapplicable here because the patentee purportedly had written description support for claiming even broader subject matter than the recited genus, i.e., the broader "oxide" genus. *See* PO Sur-reply 11–12. We disagree. First, the written description for priority is a statutory requirement that cannot be avoided based merely on policy arguments. 35 U.S.C. § 120. Second, even with respect to the concern of over-claiming, the mere fact that the patentee purportedly had written description support for subject matter broader than claim 1 would not alleviate that concern. The requirement for written description support is only one of a number of requirements for patentability, and it would still be over-claiming for a patentee to seek a claim that it did not describe to avoid a prior art rejection for a broader claim that it described.

Patent Owner further argues that because in a similar patent application Petitioner sought claims reciting that a "low resistance insulating layer comprises a metal oxide," while purportedly only disclosing TiO_2, Ta_2O_5, and ZnO, Petitioner's position in that case is inconsistent with its position here and that it takes "just a very few species to enable the full scope of 'metal oxide' in this particular arrangement." PO Resp. 48 (citing Ex. 2099, claim 2, ¶¶ 8, 33, 39, 86, 96, 99, 100, 111, 140, 156, 161); PO Sur-reply 13 (citing Ex. 2099, claims 2–3). On this record, we do not reach such a conclusion. Patent Owner cites to the publication of the involved application (Ex. 2099), which shows that Petitioner has filed such claims and that the involved application discloses TiO_2, Ta_2O_5, and ZnO, but Patent Owner provides no analysis of how the purported support for a genus based on the disclosure of three species would conflict with an alleged lack of a support for a genius based on one species. Patent Owner further does not set

forth any arguments that have been made in the prosecution of the involved application (Ex. 2099). *See* PO Resp. 47; PO Sur-reply 13.

As for Patent Owner's argument that Petitioner's decision not to challenge claims 17 and 23 of the '395 patent indicates that the pre-2011 priority applications support the recited genus, we disagree. PO Sur-reply 11. Petitioner filed petitions challenging the '395 patent in IPR2020-01207 and IPR2020-01282. Petitioner did not challenge claims 17 and 23 of the '395 patent in IPR2020-01207. *See* IPR2020-01207, Paper 2, 6. Petitioner, however challenged those claims in IPR2020–01282. *See* IPR2020-1282, Paper 2, 5. We cannot speculate as to why Petitioner chose not to challenge claims 17 and 23 of the '395 patent in IPR2020-01207. Whatever unexpressed reason Petitioner had for not challenging those claims in that proceeding is not in the record and is not evidence for consideration.

In sum, after considering all the arguments and evidence, we find that the pre-2011 priority applications do not describe the recited genus. Thus, Patent Owner is not entitled to the benefit of any pre-2011 priority applications for claims 1–4, 13, 20, 22, and 25, and Grupp '483 is prior art for those claims.

5. The Oxide of Titanium Claims (claims 6, 8, 10–12, 15–19, 26–29)

The Petition does not address whether the pre-2011 priority applications describe the breadth of the oxide-of-titanium limitation. *See* Pet. 18–26. Instead, the Petition argues that the pre-2011 priority applications do not describe the breadth of the broader genus of "the metal oxide of the interface layer." *Id.* The Patent Owner Response asserts that the mere fact that the pre-2011 priority applications may not describe the

broader class of metal oxides does not mean they fail to describe the breadth of the class of oxides of titanium. PO Resp. 39–43.

In its Reply, Petitioner does not dispute this argument by Patent Owner, but instead presents substantive arguments as to why the pre-2011 priority applications purportedly fail to describe the breadth of the recited oxides of titanium. Pet. Reply 7–12. According to Petitioner, the wide range of different characteristics, and the different crystalline structures that affect the electrical and other characteristics of each titanium oxide, is evidence that the disclosure of TiO_2 in the priority applications is insufficient to represent the full scope of even the claimed titanium oxide subgenus. Pet. Reply 9 (citing Ex. 1047, Schubert Decl. ¶ 68 (contrasting, e.g., TiO_2 as an oxide of titanium that behaves as a semiconductor and has a high electron affinity with TiO as an oxide of titanium that behaves as a conductor and has no electron affinity)). Noting the existence of superconducting and nonequilibrium compounds in the metal oxide genus, Petitioner further argues that the disclosure of TiO_2 in the priority applications is insufficient to represent the full scope of the claimed metal oxide genus. Pet. Reply 5–6.

In its Sur-reply, Patent Owner argues that Petitioner's reply arguments are belated and should not be considered. PO Sur-reply 5–7.

We agree with Patent Owner. A petitioner "may not submit new evidence or argument in reply that it could have presented earlier, e.g., to make out a prima facie case of unpatentability." Consolidated Trial Practice Guide 73[4]; *see also* 37 C.F.R. § 42.23(b). Here,

[4] Consolidated Office Trial Practice Guide (Nov. 2019), available at https://www.uspto.gov/about-us/news-updates/consolidated-trial-practice-guide-november-2019.

Petitioner's breadth challenge to the written description support for the genus of "the metal oxide of the interface layer comprises an oxide of titanium" recited in claims 6, 8, 10, 11, and 14–16 was part of Petitioner's *prima facie* case, which could have, and should have, been presented with the Petition. Thus, Petitioner could not properly wait until its Reply to specifically challenge the description support for the breadth of that class in the pre-2011 priority applications. *See Ariosa Diagnostics v. Verinata Heath, Inc.*, 805 F.3d 1359, 1368 (Fed. Cir. 2015); *Intelligent Bio-Sys., Inc. v. Illumina Cambridge Ltd.*, 821 F.3d 1359, 1369–70 (Fed. Cir. 2016); *Henny Penny Corp. v. Frymaster LLC*, 938 F.3d 1324, 1330–31 (Fed. Cir. 2019). Accordingly, we will not consider the breadth challenge to oxides of titanium that Petitioner presented for the first time in its Reply.

As for the breadth challenge presented in the Petition—that the pre-2011 priority applications do not describe the breadth of the class of metal oxides, that challenge is inapplicable to claims 6, 8, 10–12, 15–19, 26–29 because they narrow the recited class to an oxide of titanium, which is a far narrower class. Dr. Schubert provides examples of numerous metal oxides that do not comprise oxides of titanium. Ex. 1016, Schubert Decl. ¶ 94 (hafnium oxide and zirconium oxide); Ex. 1047, Schubert Decl. 2 ¶ 19 (*see* the compounds identified in that paragraph beyond titanium dioxide).

Petitioner does not dispute that the pre-2011 priority applications disclose a species within the scope of the recited genus. Pet. 20–25. To the contrary, Petitioner relies on one of the pre-2011 priority applications (Grupp '483) as disclosing a species (with TiO_2) as proof that claims 6, 8, 10–12, 15–19, and 26–29 are anticipated. *See* Pet. 38–45, 52–54.

Thus, we determine that Petitioner has not proven that the pre-2011 priority applications fail to describe the genus in which the metal oxide of

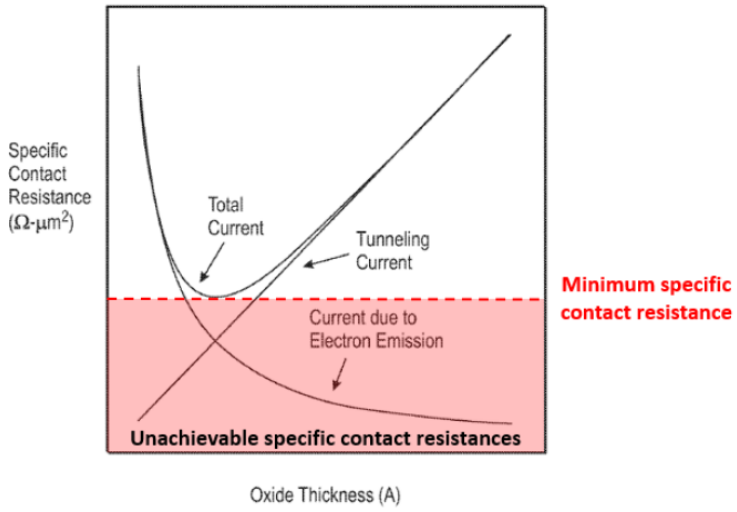
the interface layer comprises an oxide of titanium. Thus, Petitioner has not proven that Patent Owner is not entitled to the benefit of the pre-2011 priority applications for claims 6, 8, 10–12, 15–19, and 26–29 due to a lack of written description support.

6. Specific Contact Resistivity – Claims 18, 25–29

We now turn to Petitioner's argument that claims 18 and 25–29[5] are not entitled to the benefit of any of the priority applications for the '691 patent because none of those priority applications enable the full range of specific contact resistivity recited or included by dependence by those claims. Pet. 21–26. Petitioner argues the involved limitation—"a specific contact resistivity . . . less than 1Ω-μm2," has no lower bound. *Id.* at 22. Petitioner argues that this limitation encompasses specific contact resistivities down to and including approximately zero, which Petitioner argues that the challenged patent and priority applications teach cannot be achieved. *Id.* at 22–26.

To illustrate the point, Petitioner offers an annotated version of Figure 8 of the '691 patent, as shown:

[5] Petitioner also challenged claim 30, but claim 30 has been disclaimed and we do not consider it.



Petitioner's Annotated Version of Figure 8

Pet. 23. Petitioner argues that this figure shows how "the nadir of [the] 'total current' curve indicates a range of specific contact resistivities down to and including approximately zero that an ordinarily skilled artisan could not have attained by following the teachings of the '691 Patent and its parent applications." *Id.* at 23–24. Petitioner argues that the challenged claims encompass a range of specific contact resistivities down to and including approximately zero that cannot be achieved and thus cannot be enabled by the priority applications. *Id.* at 22.

Petitioner relies on *MagSil Corp. v. Hitachi Global Storage Techs., Inc.*, 687 F.3d 1377 (Fed. Cir. 2012). *See* Pet. 22, 24. In *MagSil*, the claims recited that "applying a small magnitude of electromagnetic energy to the junction . . . causes a change in the resistance by at least 10% at room temperature." *MagSil,* 687 F.3d at 1381. The patent owner offered testimony of an expert, who opined that "a person of ordinary skill in the art could work from the . . . patent and make tunneling junctions with a resistive change between 100% and 120% without undue experimentation." *Id.* at 1382. The Federal Circuit, however, found that the testimony suggesting a

resistive change up to 120% "only reaches a lower-end of the claimed scope," as "[t]he invention claims resistive changes from at least 10% up to infinity." *Id*. The Federal Circuit held that "the asserted claims are invalid for lack of enablement because their broad scope is not reasonably supported by the scope of enablement in the specification." *Id*. at 1384.

Patent Owner asserts that "[t]he vertical axis in Figure 8 has neither a scale nor numbers and therefore cannot be meaningfully compared to the numerical values recited in the claims," that Petitioner "failed to establish that the 'unachievable' region in Figure 8 is an appreciable portion of the claimed range," and that "[an ordinarily skilled artisan] would understand that the resistivity values achievable with the invention are quite low, perhaps even negligible or too low to measure." PO Resp. 15–16 (citing Ex. 2070, Kuhn Decl. ¶¶ 75, 77).

Next, Patent Owner argues that "Figure 8 should not be understood, and would not have been understood by [an ordinarily skilled artisan], to imply zero specific contact resistivity as the petition asserts" because "[an ordinarily skilled artisan] would understand from the shapes of the curves on Figure 8 that the vertical scale is logarithmic and therefore does not extend down to zero." PO Resp. 16 (citing Ex. 2070, Kuhn Decl. ¶¶ 76–77, 91).

Patent Owner also argues that "Figure 8 is a 'conceptual' diagram meant to illustrate the principles of the physics involved, not any absolute values," that "[t]he particular curves illustrated on Figure 8 are for one set of materials (semiconductor, interface, and metal)," and that "[i]f one or more of those materials is changed, then the curves would change." PO Resp. 17–19 (citing Ex. 2070, Kuhn Decl. ¶¶ 80–82). Patent Owner contends that "even if there is an unachievable region for one combination of materials,

another set of materials would almost certainly have a minimum that is less (i.e., in the so-called 'unachievable' region)." *Id*. at 19.

Patent Owner then argues that "[t]he fact that some values of specific contact resistance may not be possible would simply mean that there is an inherent lower limit, below which Acorn's specification need not teach how to achieve." PO Resp. 19 (emphasis omitted). According to Patent Owner, "[t]he issue of enablement of open-ended ranges is a well-developed area of the law, and the controlling rule is that the specification need not enable the entirety of an open-ended range when there is an 'inherent' limit on the open end of the range." *Id*. Patent Owner relies on *Andersen Corp. v. Fiber Composites, LLC*, 474 F.3d 1361 (Fed. Cir. 2007), *Rimfrost AS v. Aker Biomarine Antarctic AS*, PGR2018-00033, Paper 9 (Aug. 29, 2018), and *Ex parte Smith*, Appeal No. 2017-010042, 2019 WL 6173250 (PTAB Sept. 30, 2019). Patent Owner also asserts that its position is "is a corollary to the related principle that a patentee need not show that non-operable embodiments are enabled." PO Resp. 21–22.

Patent Owner contends that the Board and courts regularly decline to follow *MagSil* where, as here, there is an inherent limit on the open end of a range. PO Resp. 22 (citing *Snap-on Inc. v. Milwaukee Electric Tool Corp.*, IPR2015-01242, Paper 10 (Dec. 2, 2015); *Thermo Fisher Scientific Inc. v. Regents of University of California*, IPR2018-01347, Paper 10 (Jan. 22, 2019); *PerkinElmer Health Sciences, Inc. v. Agilent Technologies, Inc.*, 962 F. Supp. 2d 304 (D. Mass. 2013)). Patent Owner additionally claims that "[an ordinarily skilled artisan] would have understood there to be an inherent lower limit for specific contact resistivity for a given set of materials," and that "Figure 8 . . . clearly illustrates that lower limit," as "the minimum of the 'Total' curve." PO Resp. 24.

Patent Owner further cites testimony from Dr. Kuhn that

> Figure 8 conveys to [an ordinarily skilled artisan] a simple experiment to find a minimum or near-minimum specific contact resistivity for a given set of materials" and that "[an ordinarily skilled artisan] could have run simple experiments on 'test chip[s]' in a 'development fab' to vary the thickness of the interface layer, measure the specific contact resistance by well-known methods, and thereby determine the minimum or a near-minimum specific contact resistance and corresponding interface layer thickness.

PO Resp. 26–27 (citing Ex. 2070, Kuhn Decl. ¶¶ 83–87). Patent Owner argues that "[an ordinarily skilled artisan] could have repeated that experiment with different materials, aided by the teachings (materials and interface layer thickness ranges) in the . . . patents, until an acceptably low specific contact resistance was found" and that "[t]he amount of experimentation to do so would not have been undue." *Id*. at 27 (citing Ex. 2070, Kuhn Decl. ¶¶ 87–88).

Petitioner responds that Patent Owner "asks the Board to rewrite the claims to include some unspecified 'inherent lower limit'" and that if the Patent Owner "wanted the claims to include some lower limit," it "could have attempted to remedy the claims via Motion to Amend." Pet. Reply 18. Petitioner argues that the disclosures "fail to even hint at what that purported 'inherent lower limit' may be or how [to] achieve it" and that "[n]either figure 8 nor anything else in the specification discloses exemplary materials, thicknesses, or any other means for achieving the full range of claimed SCRs (e.g., lower than 1 Ω-μm^2 and approaching 0 Ω-μm^2)." *Id*. at 19–20.

We begin our analysis by noting that Petitioner has the burden of proving that Patent Owner is not entitled to the benefit of its priority applications. *Dynamic Drinkware,* 800 F.3d 1375, 1378 (Fed. Cir. 2015).

Neither party asks for a construction of the subject claim language, and we determine that the plain meaning of "a specific contact resistance of less than or equal to approximately X" would encompass all specific contact resistances below X and down to zero.

As noted above, the parties both focus on Figure 8. Petitioner argues that it shows a region below the minimum of the Total Current curve that is not enabled. *See* Pet. 21–23; Ex. 1016, Schubert Decl. ¶ 106 (explaining that the sum of the resistance to tunneling current with and resistance to current due to electron emission depicted in Fig. 8 "leaves a range of specific contact resistances that cannot be achieved using the techniques in the '336 Patent"); *see also id*. ¶ 107 ("[T]he claims encompass something that cannot be achieved according to the '336 Patent: specific contact resistances all the way down to and including approximately zero").

Patent Owner argues that the figure is not meaningful because it does not have scales on the axes, because it may be logarithmic, and because it may show resistivity values that are negligible or too low to measure. PO Resp. 16–19. We find these arguments somewhat off the mark, because the issue we need to resolve is whether the disclosure enables the specific numerical ranges recited in the claims. As Dr. Kuhn observes, Figure 8 merely illustrates how the tunneling resistivity increases as the thickness of the interface layer increases, the electron emission resistivity decreases as the thickness increases, and the how those behaviors affect the total current. *See* Ex. 2070, Kuhn Decl. ¶¶ 73–75. We agree that one cannot discern any "numerical values of specific contact resistance" from Figure 8. *See id*. ¶ 75.

As for the recited ranges, Patent Owner does not dispute, and the evidence shows, that the disclosure does not enable specific contact

resistance down to zero. Ex. 1016, Schubert Decl. ¶¶ 105–108. Instead, Patent Owner argues that one of skill in the art would have understood there to be an "inherent lower limit" and that the claims are enabled because one of skill in the art could achieve that lower limit through experimentation based on the disclosure of patent. We are not persuaded by Patent Owner's argument, for two main reasons.

First, we do not agree that the cases cited by Patent Owner establish that the enablement requirement is satisfied if one of skill in the art could experiment in accordance with the disclosure to find a practical end of an open ended range recited in a claim. Patent Owner principally relies on *Andersen Corp. v. Fiber Composites*, but the Federal Circuit in that case affirmed the jury verdict of enablement because "the upper limit of the Young's modulus of the structural member would lie somewhere between the Young's modulus of the wood fiber and that of the polymer used in the composition." 474 F.3d at 1377. In other words, there were two known quantities that provided a fixed range. That is not the case here, where Patent Owner does not point to any such predefined limits. Patent Owner also cites a District Court case, *PerkinElmer Health Scis., Inc. v. Agilent Techs., Inc.*, 962 F. Supp. 2d 304, 310 (D. Mass. 2013). That case is not directly on point, because it was considering claim construction and not enablement, but that court also found an existing practical upper limit to the claimed range of molecular weights, explaining that "the largest known proteins at the time of patenting had a high, but definite, mass." *Id*. at 310.[6]

[6] Patent Owner additionally cites several Board decisions in *inter partes* reviews and an *ex parte* appeal. They are not binding on us, and we find them unpersuasive because they are based on different facts. *See Scripps Clinic & Research Found. v. Genentech, Inc.*, 927 F.2d 1565, 1572 (Fed.

We also disagree with Patent Owner's suggestion that its position is supported by the principle that "a patentee need not show that non-operable embodiments are enabled." PO Resp. 21. It would be both circular and contrary to the important policy underlying the enablement requirement to allow it to be avoided by argument that subject matter within the scope of the claims that is not enabled may simply be disregarded as "inoperable." *See Alcon Research, Ltd. v. Apotex Inc.*, 687 F.3d 1362, 1368 (Fed. Cir. 2012) ("This is not how patent law works. When you claim a concentration range of 0.0001–5% w/v (as claim 2), you can't simply disavow the invalid portion and keep the valid portion of the claim. If everything up to 0.001% w/v is admittedly not enabled, then the entire claim is invalid."). *In re Cook*, 439 F.2d 730 (CCPA 1971), cited by Patent Owner, explains that the presence of inoperative embodiments within claim scope is permissible "so long as it would be obvious to [a skilled artisan] how to make the embodiment operative rather than inoperative." *Id*. at 734–35. -*In re Cook* is inapplicable here because neither party has argued or offered any evidence that it would have been obvious to skilled artisan how to make the lower part of the recited range operative or enabled.

Second, even if Patent Owner could rely on experiments based on the disclosure to find an "inherent lower limit," it has not alleged that the results would reveal a lower bound that would fall into the claimed ranges. Instead, Patent Owner and its expert assert that

> Figure 8 conveys to [an ordinarily skilled artisan] a simple experiment to find a minimum or near-minimum specific contact resistivity for a given set of materials" and that "[i]f desired, [an ordinarily skilled artisan] could have repeated that experiment

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Cir. 1991) (explaining the "appropriateness [of open-ended claims] depends on the particular facts of the invention, the disclosure, and the prior art").

> with different materials, aided by the teachings (materials and interface layer thickness ranges) in the . . . patents, until an acceptably low specific contact resistance was found" or, as described by Dr. Kuhn, until one reached "a suitable low SCR.

PO Resp. 26–27 (citing Ex. 2070 ¶ 88). But even if we accept those assertions as true, they show only that the disclosure enables experimentation to determine a resistance that was "suitable" or "acceptably low," and we fail to see how that identifies a specific contact resistance that would form an inherent lower end of the claimed ranges, which are less than or equal to approximately 1000 $\Omega \cdot \mu m^2$, less than or equal to approximately 10 $\Omega \cdot \mu m^2$, and less than or equal to approximately 1 $\Omega \cdot \mu m^2$.

We also find Dr. Kuhn's "inherent lower limit" analysis flawed. We agree that the minimum of the "Total Current" curve in Figure 8 represents an inherent lower limit of the contact resistance for a specific set of materials. *See* Ex. 2070, Kuhn Decl. ¶ 89. However, Dr. Kuhn asserts, with reference to the annotated version of Figure 8 below, that "'specific contact resistivity less than X' really means X > SCR ≥ Y, where *Y is an inherent lower limit*." *Id.* ¶ 90 (emphasis added).

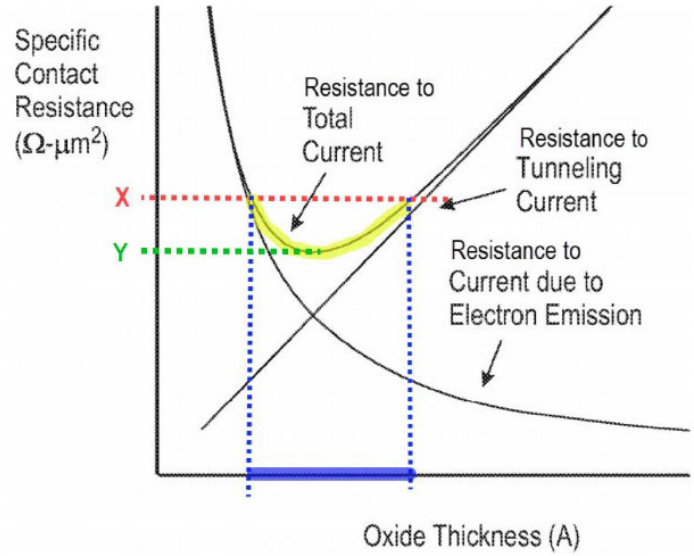


Figure 8 as Annotated by Dr. Kuhn (Ex. 2070 ¶ 90).

We find Dr. Kuhn's interpretation of the claim language to present a claim construction issue that was not raised in the Patent Owner Response and is now waived. (*See* Paper 22, 8 ("Patent Owner is cautioned that any arguments not raised in the response may be deemed waived."). But we also disagree with it, at least to the extent it is represented in the Figure, because it considers only one physical system, where the claims are not so limited. For example, we read the language in claim 25—"interface layer comprising a metal oxide separation layer and a semiconductor oxide passivation layer configured to provide a specific contact resistivity between the contact metal and the semiconductor of less than 1 $\Omega \cdot \mu m^2$"—to mean that the claims encompass systems with interface layers that are otherwise within their scope and in which the minimum of the "Total Current" curve falls between 1 $\Omega \cdot \mu m^2$ and zero. This means that any "inherent lower limit" would be the lowest resistance that could be achieved for any interface layer in *any physical device that meets the other limitations of the claims.* *See* Ex. 2070, Kuhn Decl. ¶¶ 81–82 (describing and illustrating different curves for different physical systems).

Petitioner provides evidence that "[e]ven two years after the earliest Priority Application was filed, [Patent Owner] had not achieved—and, accordingly, had not enabled—the full range of the claimed SCRs," as "the lowest reported SCR values that [Patent Owner] was able to achieve was approximately 300 Ω-μm^2," and that "those values were achieved with a silicon nitride interface layer (not the claimed metal oxide)." Pet. Reply 20–21 (citing Ex. 1046, Fig. 3; Ex. 1047, Schubert Decl. 2 ¶¶ 80–81). Petitioner provides further evidence that "after over a decade of additional research and innovation, researchers in 2013 finally reported achieving an SCR value of

about 0.1 Ω-μm^2 using an interface layer material—ZnO—not disclosed or contemplated by the Priority Applications." Pet. Reply 22 (citing Ex. 1041, 2). Patent Owner responds that it "was not required to demonstrate the full range of its invention's possibilities." PO Sur-Reply 19. We agree that Patent Owner had no obligation to practice the patented inventions, but this evidence does tend to suggest that achieving at least some of the claimed ranges was not a simple matter of trying various combinations of disclosed materials. *Cf. MagSil*, 687 F.3d at 1382 (relying on the patent owner's post-filing activities when assessing enablement).

Patent Owner also argues that "[r]eferring to a resistivity or resistance range with an unspecified lower end is 'common in this art.'" PO Resp. 27 (quoting Ex. 2070 ¶ 91 and citing, *e.g.*, Ex. 2034, 3:27–39; Ex. 2035, 3:23–24). We conclude that unrelated patents, with entirely different disclosures and claims, are not pertinent to our analysis, particularly given that it has not been established that they do not also have enablement problems.

Finally, Patent Owner argues that a Primary Patent Examiner "having deep familiarity with this technology in general and [Patent Owner's] patents in particular, recently allowed nine . . . claims reciting 'a specific contact resistivity of less than 1 [or 10] Ω·μ^2' after considering the arguments made in the petition." PO Resp. 31. The record does show that the Examiner initialed the IDS entries for ten IPR petitions in this family and ten copies of the Schubert Declaration. *See* Ex. 2062, 349–355. However, we are unable to discern the extent to which the Examiner considered the enablement issue and, as such, we will reach our own result from our substantially more developed record on this issue.

For the reasons given above, we conclude that (1) the plain language of the challenged claims encompasses specific contact resistances down to

zero, (2) Petitioner has proven with *undisputed* evidence that the disclosures of the priority applications do not enable resistances down to zero, (3) the record does not indicate there is an "inherent lower limit" for specific contact resistances that would satisfy the requirement that the full scope of the claims be enabled in the priority applications

"The standard for what constitutes proper enablement of a prior art reference for purposes of anticipation under section 102 . . . differs from the enablement standard under section 112." *Rasmusson v. SmithKline Beecham Corp.*, 413 F.3d 1318, 1325 (Fed. Cir. 2005). Enablement under section 112, which is required for priority under section 120, requires enablement of the full breadth of a claim. *Wyeth and Cordis Corp. v. Abbott Laboratories*, 720 F.3d 1380 (Fed. Cir. 2013); *MagSil,* 687 F.3d at 1384; 35 U.S.C. § 120. Enablement for anticipation does not; rather it requires only enablement of an embodiment or embodiments that fall within the scope of the claim. *Chester v. Miller*, 906 F.2d 1574, 1577 (Fed. Cir. 1990) ("a CIP's claim for a genus might not be enabled by a parent's disclosure, but that parent may enable a species that anticipates the CIP's claim for a genus . . . . the Court of Custom and Patent Appeals . . . made clear the differences between the requirements for claim-anticipating disclosures and for claim-supporting disclosures") (citing *In Re Lukach*, 442, F.2d 967, 969–970 (CCPA 1971)).

Here, the enablement challenge for priority is for a lack of enablement of the full breadth of the recited range, and in particular, a lack of enablement of the lower part of the recited range (that which is at or near zero). No party has argued that the upper part of the recited range (just below 1Ω-μm^2) is not enabled by either the priority applications or Grupp '483. *See, e.g.*, Pet. 21–26; PO Resp. 12–32; Pet. Reply 17–28; Sur-reply 14–19. Enablement by a prior art patent is presumed. *See In re Antor Media*

Corp., 689 F.3d 1282, 1287 (Fed. Cir. 2012); *Impax Labs., Inc. v. Aventis Pharm., Inc.*, 545 F.3d 1312, 1316 (Fed. Cir. 2008); *Amgen, Inc. v. Hoechst Marion Roussel, Inc.*, 314 F.3d 1313, 1355 (Fed. Cir. 2003). For this reason, the record does not reflect an inconsistency in holding the priority applications as not enabling the breadth of the recited range, while treating Grupp '483 as enabling the upper part of the range for purposes of anticipation. Thus, Grupp '483 is prior art for each of challenged claims 18, and 25–29.

B. Anticipation

1. Claim 1

As discussed above, claim 1 recites a structure that comprises a semiconductor region in a substrate, a metal electrical contact to that semiconductor region, a passive aiding dielectric tunnel barrier layer between the semiconductor region and the metal electrical contact. The semiconductor region is electrically connected to the metal electrical contact through the passive aiding dielectric tunnel barrier layer. Claim 1 further recites that the passive aiding dielectric tunnel layer comprises a metal oxide and a semiconductor oxide. Claim 1 is among the metal oxide claims discussed above. Having reviewed the arguments in the Petition and having determined that Grupp '483 is prior art to the metal oxide claims, we find the Petitioner has demonstrated that claim 1 is anticipated by Grupp '483.

2. Claim 2

Claim 2 depends from claim 1 and recites that "the semiconductor oxide comprises an oxide of the semiconductor region." Claim 2 is among the metal oxide claims discussed above. Having reviewed the arguments in the Petition and having determined that Grupp '483 is prior art to the metal

oxide claims, we find the Petitioner has demonstrated that claim 2 is anticipated by Grupp '483.

3. Claim 3

Claim 3 depends from claim one and recites that "the semiconductor oxide of the dielectric tunnel barrier layer has a thickness of approximately 0.1 nm to 5 nm." Claim 3 is among the metal oxide claims discussed above. Having reviewed the arguments in the Petition and having determined that Grupp '483 is prior art to the metal oxide claims, we find the Petitioner has demonstrated that claim 3 is anticipated by Grupp '483.

4. Claim 4

Claim 4 depends from claim 1 and recites that "the semiconductor region comprises an n-type doped source or drain of a transistor." Claim 4 is among the metal oxide claims discussed above. Having reviewed the arguments in the Petition and having determined that Grupp '483 is prior art to the metal oxide claims, we find the Petitioner has demonstrated that claim 4 is anticipated by Grupp '483.

5. Claim 6

Claim 6 depends from claim 3 and recites that "the metal oxide of the dielectric tunnel barrier layer comprises an oxide of titanium." Claim 6 is among the oxide of titanium claims discussed above. Having determined that Petitioner has failed to demonstrate that the oxide of titanium claims are not entitled to the priority date of Grupp '483, we find that Petitioner has not demonstrated claim 6 is anticipated by Grupp '483.

6. Claim 8

Claim 8 depends from claim 6 and recites that "the semiconductor region comprises an n-doped source or drain of a transistor." Claim 8 is among the oxide of titanium claims discussed above. Having determined

that Petitioner has failed to demonstrate that the oxide of titanium claims are not entitled to the priority date of Grupp '483, we find that Petitioner has not demonstrated claim 8 is anticipated by Grupp '483.

7. Claim 10

Claim 10 depends from claim 6 and recites that "the semiconductor oxide comprises an oxide of silicon." Claim 10 is among the oxide of titanium claims discussed above. Having determined that Petitioner has failed to demonstrate that the oxide of titanium claims are not entitled to the priority date of Grupp '483, we find that Petitioner has not demonstrated claim 10 is anticipated by Grupp '483.

8. Claim 11

Claim 11 depends from claim 6 and recites that "the semiconductor oxide of the dielectric tunnel barrier layer is adjacent the semiconductor region." Claim 11 is among the oxide of titanium claims discussed above. Having determined that Petitioner has failed to demonstrate that the oxide of titanium claims are not entitled to the priority date of Grupp '483, we find that Petitioner has not demonstrated claim 11 is anticipated by Grupp '483.

9. Claim 12

Claim 12 depends from claim 6 and recites that "the metal electrical contact comprises titanium." Claim 12 is among the oxide of titanium claims discussed above. Having determined that Petitioner has failed to demonstrate that the oxide of titanium claims are not entitled to the priority date of Grupp '483, we find that Petitioner has not demonstrated claim 12 is anticipated by Grupp '483.

10. Claim 13

Claim 13 depends from claim 3 and recites that "the semiconductor oxide comprises an oxide of silicon." Claim 13 is among the metal oxide

claims discussed above. Having reviewed the arguments in the Petition and having determined that Grupp '483 is prior art to the metal oxide claims, we find the Petitioner has demonstrated that claim 13 is anticipated by Grupp '483.

11. Claim 15

Claim 15 depends from claim 13 and recites that "the metal oxide of the dielectric tunnel barrier layer comprises an oxide of titanium." Claim 15 is among the oxide of titanium claims discussed above. Having determined that Petitioner has failed to demonstrate that the oxide of titanium claims are not entitled to the priority date of Grupp '483, we find that Petitioner has not demonstrated claim 15 is anticipated by Grupp '483.

12. Claim 16

Claim 16 depends from claim 15 and recites that "the metal electrical contact comprises titanium." Claim 16 is among the oxide of titanium claims discussed above. Having determined that Petitioner has failed to demonstrate that the oxide of titanium claims are not entitled to the priority date of Grupp '483, we find that Petitioner has not demonstrated claim 16 is anticipated by Grupp '483.

13. Claim 17

Claim 17 depends from claim 15 and recites that "the semiconductor comprises an n-type doped source or drain of a transistor." Claim 17 is among the oxide of titanium claims discussed above. Having determined that Petitioner has failed to demonstrate that the oxide of titanium claims are not entitled to the priority date of Grupp '483, we find that Petitioner has not demonstrated claim 17 is anticipated by Grupp '483.

14. Claim 18

Claim 18 depends from claim 17 and recites that "a specific contact resistivity between the n-type doped source or drain and the metal electrical contact is less than 1 $\Omega \cdot \mu m^2$." Claim 18 is among the oxide of titanium claims discussed above. Having determined that Petitioner has failed to demonstrate that the oxide of titanium claims are not entitled to the priority date of Grupp '483, we find that Petitioner has not demonstrated claim 18 is anticipated by Grupp '483.

15. Claim 19

Claim 19 depends from claim 1 and recites that "the semiconductor region comprises silicon, the semiconductor oxide comprises an oxide of silicon, the metal oxide of the dielectric tunnel barrier comprises an oxide of titanium, and the metal electrical contact comprises titanium." Claim 19 is among the oxide of titanium claims discussed above. Having determined that Petitioner has failed to demonstrate that the oxide of titanium claims are not entitled to the priority date of Grupp '483, we find that Petitioner has not demonstrated claim 19 is anticipated by Grupp '483.

16. Claim 20

Claim 20 depends from claim 1 and recites that "the dielectric tunnel barrier layer is configured to reduce a height of the Schottky barrier between the metal electrical contact and the semiconductor region from that which would exist at a contact junction between the metal electrical contact and the semiconductor region without the dielectric tunnel barrier layer disposed therebetween." Claim 20 is among the metal oxide claims discussed above. Having reviewed the arguments in the Petition and having determined that Grupp '483 is prior art to the metal oxide claims, we find the Petitioner has demonstrated that claim 20 is anticipated by Grupp '483.

17. Claim 22

Claim 22 depends from claim 1 and recites that "the dielectric tunnel barrier layer is configured to reduce contact resistivity between the metal electrical contact and the semiconductor region from that which would exist at a contact junction between the metal electrical contact and the semiconductor region without the dielectric tunnel barrier layer disposed therebetween." Claim 22 is among the metal oxide claims discussed above. Having reviewed the arguments in the Petition and having determined that Grupp '483 is prior art to the metal oxide claims, we find the Petitioner has demonstrated that claim 22 is anticipated by Grupp '483.

18. Claim 25

Claim 25 recites an electrical junction comprising an interface layer disposed between a contact metal and a semiconductor, the semiconductor comprising a source or drain of a transistor. The interface layer comprises a metal oxide separation layer and a semiconductor oxide passivation layer. The interface layer is configured to provide a specific contact resistivity between the contact metal and the semiconductor of less than 1 $\Omega \cdot \mu m^2$. Claim 25 is among the metal oxide claims and, as discussed above, we have determined that Grupp '483 is prior art to the metal oxide claim limitations. Claim 25 also recites the specific resistivity limitation. As discussed above, Petitioner has shown that that the challenged claims are not entitled to the benefit of the filing dates of the priority applications and Grupp '483 is prior art to the specific resistivity claim limitations. *See* Section VI.A.6. Therefore, Petitioner has demonstrated that all of the limitations of claim 25 are in the prior art, and we find that Petitioner has demonstrated claim 25 is anticipated.

19. Claim 26

Claim 26 depends from claim 25 and recites "the metal oxide separation layer comprises an oxide of titanium." Claim 26 is among the oxide of titanium claims discussed above. Having determined that Petitioner has failed to demonstrate that the oxide of titanium claims are not entitled to the priority date of Grupp '483, we find that Petitioner has not demonstrated claim 26 is anticipated by Grupp '483..

20. Claim 27

Claim 27 depends from claim 26 and recites "the semiconductor oxide passivation layer comprises an oxide of the semiconductor." Claim 27 is among the oxide of titanium claims discussed above. Having determined that Petitioner has failed to demonstrate that the oxide of titanium claims are not entitled to the priority date of Grupp '483, we find that Petitioner has not demonstrated claim 27 is anticipated by Grupp '483.

21. Claim 28

Claim 28 depends from claim 27 and recites "the semiconductor oxide passivation layer has a thickness of approximately 0.1 nm to 5 nm." Claim 28 is among the oxide of titanium claims discussed above. Having determined that Petitioner has failed to demonstrate that the oxide of titanium claims are not entitled to the priority date of Grupp '483, we find that Petitioner has not demonstrated claim 28 is anticipated by Grupp '483.

22. Claim 29

Claim 29 depends from claim 27 and recites that "the semiconductor oxide passivation layer is adjacent the semiconductor." Claim 29 is among the oxide of titanium claims discussed above. Having determined that Petitioner has failed to demonstrate that the oxide of titanium claims are not

entitled to the priority date of Grupp '483, we find that Petitioner has not demonstrated claim 29 is anticipated by Grupp '483.

VII. MOTION TO EXCLUDE

Patent Owner seeks to exclude the following portion of the cross-examination testimony of Dr. Kuhn: page 114, line 10 through page 123, line 14 of her deposition transcript (Exs. 1042, 1043). Mot. 1, 5. Patent Owner argues that the testimony at issue concerns the scope of claims that recite "an oxide of titanium." *Id.* at 1. According to Patent Owner, however, the oxide-of-titanium limitation was not substantively addressed in the Petition and Dr. Kuhn did not address it in her declaration. *Id.* Further, Patent Owner argues that it timely objected to the testimony at issue and thus the testimony should be excluded for exceeding the scope of Dr. Kuhn's direct testimony. *Id.* at 1–2.

Petitioner disagrees, arguing that Dr. Kuhn expressly opined on the "oxide of titanium" limitation. Opp. to Mot. 1. Petitioner asserts:

> First, Dr. Kuhn opined that "nothing in the petition or Dr. Schubert's declaration specifically address[ed] the written-description support of those dependent claims or an oxide of titanium." Ex. 2070, Kuhn Decl. at ¶114. Second, Dr. Kuhn opined that "the metal oxide comprises an oxide of titanium" claims are "clearly narrower than 'metal oxide.'" *Id.*

Id. at 1–2 (emphasis omitted). Petitioner argues that it was entitled to explore Dr. Kuhn's understanding of why she believes those claim limitations are "clearly narrower" and to challenge Dr. Kuhn's assertion that they were not addressed in the petition or in Dr. Shubert's declaration. *Id.* at 2.

Patent Owner responds that Dr. Kuhn merely observed that the class of oxides of titanium are clearly narrower than the class of metal oxides and

did not provide an opinion on that issue. Reply 1. Patent Owner further argues that statement did not open the door to Petitioner's questioning regarding the titanium oxide genus. *Id.* at 2.

Patent Owner's Motion to Exclude is moot in light of our determination regarding Petitioner's written description challenge to Patent Owner's benefit of its pre-2011 priority applications for claims 6, 8, 10–12, 15–19, 26–29. In particular, Petitioner relies on the testimony at issue to support its belated challenge to the breadth of written description support in the pre-2011 priority applications for the oxide of titanium class recited by those claims. Pet. Reply7–12. Because we decided not to consider that belated challenge (*see* Section III.E.1.b), the Motion to Exclude is moot.

VIII. OTHER ISSUES

A. 35 U.S,C, § 311(b)

Patent Owner argues that "[t]here are no disputes in this IPR regarding whether the 'prior art' reference ([Patent Owner]'s own Grupp '483 patent) teaches any of the claim limitations" and that "[f]or all intents and purposes, this IPR is a § 112 battle, just as if it were a PGR (for which the pre-AIA '336 Patent is not eligible)." PO Resp. 51.

Patent Owner further argues that "there is no priority dispute here regarding enablement" because "the petition does not assert that any subsequent developments after the filing of the earliest priority/benefit application (resulting in the '423 Patent) has changed the enablement issue" meaning that "either all of the specifications are enabling of the specific contact resistance ranges recited in the claims, or none of them are." Pet. 51–52. Patent Owner concludes that "[e]ntertaining the enablement challenge here would open the door for enablement challenges to a broad

class of continuation patents in IPRs that Congress never intended." *Id*. at 52.

We remain unpersuaded by Patent Owner's argument that an *inter partes* review may not address whether priority applications enable or have written description support for challenged claims. Although the issue of whether challenged claims are enabled by have written description support in the specification of the challenged patent is beyond the scope of an *inter partes* review (35 U.S.C. § 311), whether a patent is entitled to the benefit of earlier filed applications under 35 U.S.C. §§ 119 or 120 is properly an issue to be addressed in an *inter partes* review. *See Indivior UK Ltd. v. Dr. Reddy's Lab'ys S.A., 18 F.4th 1323, 1326–1330 (Fed. Cir. 2021).* And the benefit of an earlier filed application requires written description support for the challenged claims in the earlier filed application. *See id*. at 1381–1382.

B. Appointments Clause

Patent Owner argues that "[t]he AIA as written by Congress violates the Appointments Clause." PO Resp. 53.

The Supreme Court resolved this issue in *United States v. Arthrex, Inc.*, 141 S. Ct. 1970 (2021).

C. Alleged Structural Bias

Patent Owner argues that "[t]he Board's handling of this IPR is structurally biased in a way that has violated Acorn's due-process rights" because the Director's delegation of the authority determine whether to institute and try this case "results in an improper structural bias because the Board has a strong financial incentive to institute trials." PO Resp. 53–54.

This argument was rejected by the Federal Circuit in *Mobility Workx, LLC v. Unified Patents*, LLC, 15 F.4th 1146 (Fed. Cir. 2021).

D. Stipulation

Patent Owner argues that "[t]he Board's eleventh-hour invitation to the petitioner to revise its stipulation regarding parallel validity challenges in the district court . . . violated *SAS Institute Inc. v. Iancu*, 138 S. Ct. 1348 (2018), due-process, and fundamental notions of fairness." PO Resp. 56. Patent Owner contends that "Acorn invested its limited resources in these IPRs and the related litigation and chose which arguments to make based on the petition and the stipulation therein" but "after Acorn had made those significant investments, the Board allowed the petitioner to alter its case, indeed the Board invited and encouraged such revision." *Id*. at 57.

This argument is unpersuasive. The stipulation did not change the contours of, or "curate," the Petition; instead, in accordance with the precedential case of *Sotera Wireless, Inc. v. Masimo Corp.,* IPR2020-01019, Paper 12 (December 1, 2020), Petitioner simply stipulated not to bring the same arguments in the District Court.[7]

IX. CONCLUSION[8]

In consideration of the above, we conclude that Petitioner has demonstrated by a preponderance of the evidence that claims 1–4, 13, 18, 20

[7] *Sotera Wireless* issued and was designated precedential (on December 1, 2020 and December 17, 2020, respectively) after the Petition and Petitioner's Preliminary Reply were filed (on July 18, 2020 and October 16, 2020, respectively).

[8] Should Patent Owner wish to pursue amendment of the challenged claims in a reissue or reexamination proceeding subsequent to the issuance of this decision, we draw Patent Owner's attention to the April 2019 *Notice Regarding Options for Amendments by Patent Owner Through Reissue or Reexamination During a Pending AIA Trial Proceeding. See* 84 Fed. Reg. 16,654 (Apr. 22, 2019). If Patent Owner chooses to file a reissue application or a request for reexamination of the challenged patent, we remind Patent

and 22, and 25 are anticipated by Grupp '483. Petitioner has not demonstrated that claims 6, 8, 10–12, 15–19 and 26–29 are anticipated by Grupp '483.

In summary:

Claims	35 U.S.C. §	Basis	Claims Shown Unpatentable	Claims Not shown Unpatentable
1–4, 6, 8, 10–13, 15–20, 22, 25–29	102	Grupp '483	1–4, 13, 20, 22 25	6, 8, 10–12, 15–19, 26–29
Overall Outcome			1–4, 13, 20, 22, 25	6, 8, 10–12, 15–19, 26–29

Owner of its continuing obligation to notify the Board of any such related matters in updated mandatory notices. See 37 C.F.R. § 42.8(a)(3), (b)(2).

X. ORDER

In consideration of the above it is:

ORDERED that claims 1–4, 13, 20, 22 are unpatentable;

FURTHER ORDERED that Patent Owner's Motion to Exclude is dismissed as moot;

FURTHER ORDERED that that, because this is a Final Written Decision, parties to the proceeding seeking judicial review of the decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

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Paper 49
Date: February 9, 2022

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD.,
Petitioner,

v.

ACORN SEMI, LLC,
Patent Owner.

IPR2020-01207
Patent 10,090,395 B2

Before BRIAN J. McNAMARA, JOHN R. KENNY, and AARON W. MOORE, *Administrative Patent Judges.*

KENNY, *Administrative Patent Judge*.

DECISION
Final Written Decision
Determining Some Challenged Claims Unpatentable
Dismissing Patent Owner's Motion to Exclude
35 U.S.C. § 318(a)

I. INTRODUCTION

Samsung Electronics Co., Ltd. ("Petitioner") filed a Petition, Paper 2 ("Petition" or "Pet."), to institute an *inter partes* review of claims 1–6, 8–12, and 14–16 ("challenged claims") of U.S. Patent No. 10,090,395 B2 (Ex. 1001, "'395 patent"). Acorn Semi, LLC ("Patent Owner") filed a Preliminary Response, Paper 11 ("Prelim. Resp."), contending that the Petition should be denied as to all challenged claims.

On February 10, 2021, we instituted an *inter partes* review of all challenged claims. Paper 21 ("Institution Decision" or "Inst. Dec."). Patent Owner filed a Patent Owner Response (Paper 29, "PO Resp.") and an Updated Mandatory Notice reporting a jury verdict in a related district court litigation (Paper 31; Ex. 2121). Petitioner filed a Reply (Paper 34, "Pet. Reply"), and Patent Owner filed a Sur-reply (Paper 39, "PO Sur-reply"). Patent Owner also filed a Motion to Exclude certain cross-examination testimony of its expert witness, Dr. Kelin J. Kuhn (Paper 40 "Mot. Excl."). Petitioner filed an Opposition to Patent Owner's Motion to Exclude (Paper 42, "Opp. Mot. Excl."), and Patent Owner filed a Reply to Petitioner's Opposition to Patent Owner's Motion to Exclude (Paper 44, "Reply Mot. Excl."). A transcript of an oral hearing held on October 13, 2021 (Paper 48, "Tr.") has been entered into the record.

We have jurisdiction under 35 U.S.C. § 6. For the reasons discussed below, we determine that Petitioner has shown, by a preponderance of the evidence, that claims 1–6, 8–10, 15, and 16 are unpatentable. Petitioner, however, has not shown, by a preponderance of the evidence, that claims 11, 12, and 14 are unpatentable.

A. Related Matters

The Petition states that the '395 patent is asserted in *Acorn Semi, LLC v. Samsung Electronics Co. Ltd.*, Civil Action No. 2:19-cv-347 (E.D. Tex.) ("Related Litigation"), and that the complaint was served on October 24, 2019. Pet. 3 (citing Ex. 1039).

Patent Owner identifies IPR2020-01282 ("'1282 IPR") as also concerning the '395 patent. Paper 5, 2. Petitioner and Patent Owner identify other *inter partes* reviews concerning patents related to the '395 patent that may be affected by the outcome of this proceeding. *See* Pet. 3, Paper 5, 2. Petitioner also identifies patents and patent applications that are related to the '395 patent. *See* Pet. 4.

B. The '395 Patent

The '395 patent "relates to a process for depinning the Fermi level of a semiconductor at a metal-interface layer-semiconductor junction and to devices that employ such a junction." Ex. 1001, 1:32–35. The '395 patent explains that Schottky's theory concerning the ability of a junction to conduct current in one direction more favorably than in the other direction, i.e., the rectifying behavior of a metal/semiconductor junction (e.g., an aluminum/silicon junction) depends upon a barrier at the surface of the contact between the metal and the semiconductor. *Id.* at 1:52–64. Because the barrier height at the metal/semiconductor interface determines the electrical properties of the junction, controlling the barrier height is an important goal. *Id.* at 3:10–21.

The '395 patent further explains that Schottky's theory postulates the height of the barrier, as measured by the potential necessary for an electron to pass from the metal to the semiconductor, is the difference between the work function of the metal (i.e., the energy required to free an electron at the

Fermi level (the highest occupied energy state of the metal at T=0)) and the electron affinity of the semiconductor (i.e., the difference between the energy of a free electron and the conduction band of the semiconductor); but experimental results indicate a weaker variation of the barrier height with the work function than implied by this model. Ex. 1001, 1:55–2:9. To explain the discrepancy between the predicted and observed behavior, Bardeen introduced the concept of semiconductor surface states, i.e., energy states within the bandgap between the valence and conduction bands at the edge of the semiconductor crystal that arise from incomplete covalent bonds, impurities, and other effects of termination. *Id.* at 2:10–24, Fig. 1 (showing dangling bonds 120). Although Bardeen's model assumes that surface states are sufficient to pin the Fermi level in the semiconductor at a point between the valence and conduction bands, such that the barrier height should be independent of the metal's work function, in experiments, this condition is observed rarely. *Id.* at 2:25–31.

According to the '395 patent, Tersoff proposed that the Fermi level of a semiconductor is pinned near an effective "gap center" due to metal induced gap states (MIGS), which are energy states in the bandgap of the semiconductor that become populated with metal. Ex. 1001, 2:41–47. Thus, the wave functions of electrons in the metal do not terminate abruptly at the surface of the metal, but decay in proportion to the distance from the surface, extending inside the semiconductor. *Id.* at 2:50–54.

> To maintain the sum rule on the density of states in the semiconductor, electrons near the surface occupy energy states in the gap derived from the valence band such that the density of states in the valence band is reduced. To maintain charge neutrality, the highest occupied state (which defines the Fermi level of the semiconductor) will then lie at the crossover point from states derived from the valence band to those derived from

> the conduction band. This crossover occurs at the branch point of the band structure.

Id. at 2:54–63. The '395 patent also notes one further surface effect on diode characteristics is inhomogeneity, i.e., "if factors affecting the barrier height (e.g., density of surface states) vary across the plane of the junction, the resulting properties of the junction are found not to be a linear combination of the properties of the different regions." *Id.* at 3:2–6.

According to the '395 patent, "a classic metal-semiconductor junction is characterized by a Schottky barrier, the properties of which (e.g., barrier height) depend on surface states, MIGS and inhomogeneities." Ex. 1001, 3:6–9. "Before one can tune the barrier height, however, one must depin the Fermi level of the semiconductor." *Id.* at 3:16–18. The '395 patent seeks to depin the Fermi level of the semiconductor while still permitting substantial current flow between the metal and the semiconductor. *Id.* at 3:18–21. The '395 patent describes depinning the Fermi level as follows:

> By depinning the Fermi level, the present inventors mean a condition wherein all, or substantially all, dangling bonds that may otherwise be present at the semiconductor surface have been terminated, and the effect of MIGS has been overcome, or at least reduced, by displacing the semiconductor a sufficient distance from the metal.

Id. at 3:36–41. The '395 patent achieves this goal using thin interface layers disposed between a metal and a silicon-based semiconductor to form a "metal-interface layer-semiconductor junction" with minimum specific contact resistances. *Id.* at 3:25–29. "The interface layer thickness corresponding to this minimum specific contact resistance will vary depending on the materials used." *Id.* at 3:29–36. That corresponding thickness "allows for depinning the Fermi level while permitting current to flow when the junction is appropriately biased." *Id.* "Minimum specific

contact resistances of less than or equal to approximately 10 Ω-μm^2 or even less than or equal to approximately 1 Ω-μm^2 may be achieved for such junctions in accordance with the present invention." *Id.* at 3:42–45. Such low contact resistances are achieved by selecting a metal with a work function near the conduction band of the semiconductor for n-type semiconductors, or a work function near the valence band for p-type semiconductors. *Id.* at 5:30–34.

Figure 8 of the '395 patent is reproduced below:

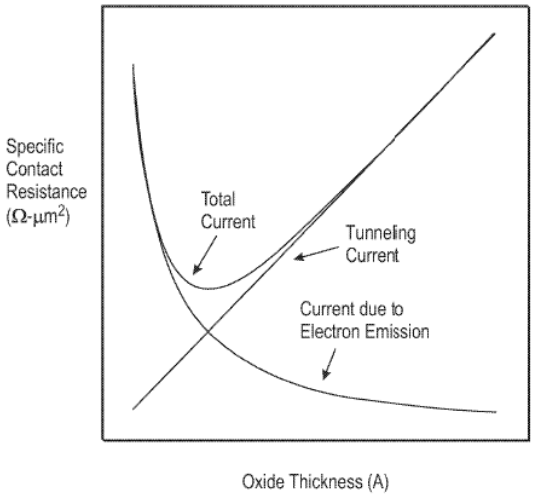


Figure 8 of the '395 patent

Figure 8 above is a graph of interface specific contact resistance versus interface thickness for a structure where the work function of the metal is the same as the electron affinity of the semiconductor, such that the Fermi level of the metal lines up with the conduction band of the semiconductor. Ex. 1001, 14:42–48. According to the '395 patent, Figure 8 shows that, at large thicknesses, the interface layer poses significant resistance to current, but as the interface layer thickness decreases, resistance falls due to increased tunneling current. *Id.* at 14:48–51. However, at some point, as the interface layer gets thinner, the effect of MIGS increasingly pulls the Fermi

level of the metal down towards the mid-gap of the semiconductor, creating a Schottky barrier and increasing resistance. *Id.* at 14:51–55. Thus, there is an optimum thickness where the resistance is at a minimum and the effect of MIGS has been reduced to depin the metal and lower the Schottky barrier, but the layer is sufficiently thin to allow significant current across the interface layer, such that specific contact resistances of less than or equal to approximately 2500 Ω-μm^2, 1000 Ω-μm^2, 100 Ω-μm^2, 50 Ω-μm^2, 10 Ω-μm^2, or less than 1 Ω-μm^2 reportedly can be achieved. *Id.* at 14:56–65.

In one embodiment, an electrical device has an interface layer that may be a monolayer or several monolayers of passivating material (e.g., a nitride, oxide, oxynitride, arsenide, hydride and/or fluoride) and may include a separation oxide layer. Ex. 1001, 3:46–59. The specific contact resistance for this electrical device is reported to be less than 10 Ω-μm^2. *Id.* at 3:52–53. In another embodiment, the interface layer consists of a passivation layer fabricated by exposing the semiconductor to nitrogenous material (e.g., ammonia (NH_3), nitrogen (N_2) or unbound gaseous nitrogen (N) generated from a plasma process). *Id.* at 3:60–64. Another embodiment uses an interface layer of passivating material disposed between the surface of a semiconductor and a conductor in which the interface layer is of a sufficient thickness to reduce the effect of MIGs in the semiconductor and passivates the semiconductor but, because the thickness of the interface layer is chosen to provide minimum, or near minimum, specific contact resistance for the junction, significant current may flow between the conductor and the semiconductor. *Id.* at 4:1–14.

In other embodiments, the interface layer is configured to allow a Fermi level of the conductor to (i) align with a conduction band of the semiconductor, (ii) align with a valence band of the semiconductor, and (iii)

to be independent of the Fermi level of the semiconductor, allowing current to flow between the conductor and the semiconductor when the junction is biased because the thickness of the interface layer corresponds to a minimum or near minimum contact resistance for the junction. Ex. 1001, 4:15–26. Specific contact resistances of less than or equal to approximately 2500 Ω-μm^2, 1000 Ω-μm^2, 100 Ω-μm^2, 50 Ω-μm^2, 10 Ω-μm^2, or less than 1 Ω-μm^2 reportedly can be achieved. *Id.* at 4:27–30.

C. Claims

As mentioned, Petitioner challenges claims 1–6, 8–12, and 14–16. Claim 1 is independent and reads:

> 1. An electrical junction, comprising a region in a semiconductor substrate, a metal electrical contact to said region, and an interface layer between said region and said metal electrical contact, said region being electrically connected to said metal electrical contact through said interface layer and said interface layer comprising a metal oxide and a semiconductor oxide, and being in contact with said region in the semiconductor substrate and said metal electrical contact.

Ex. 1001, 18:45–52.

D. Asserted Ground

Petitioner asserts that the challenged claims would have been unpatentable based on the following ground:

Claim(s) Challenged	35 U.S.C. §	Reference(s)/Basis
1–6, 8–12, and 14–16	102(b)	Grupp '483[1]

Pet. 6, 27.

E. Level of Ordinary Skill in the Art

Petitioner describes an ordinarily skilled artisan as having any of the following combinations of education and experience:

[1] U.S. Patent No. 7,176,483 B2, issued Feb. 13, 2007 (Ex. 1021).

> [i] a Ph.D. in electrical engineering, physics, materials science, or chemical engineering, with two years of practical experience with semiconductor research and design;
>
> [ii] a Master's degree in electrical engineering, physics, materials science, or chemical engineering, with four years of practical experience with semiconductor research and design; or
>
> [iii] a Bachelor's degree in electrical engineering, physics, materials science, or chemical engineering, with six to eight years of practical experience with semiconductor research and design.

Pet. 13–14 (citing Ex. 1022, Schubert Decl. ¶¶ 70–71).

The Patent Owner Preliminary Response did not comment on the level of ordinary skill in the art. In our Institution Decision, we were persuaded that Petitioner's description of the level of ordinary skill is appropriate for the subject matter of the '395 patent and applied it in that Institution Decision. Inst. Dec. 9–10. The Patent Owner Response does not comment on the level of ordinary skill in the art. *See generally* PO Resp. Thus, we apply the description of the level of ordinary skill set forth in the Petition in this Decision. Ex. 1022, Schubert Decl. ¶¶ 70–71.

II. CLAIM CONSTRUCTION

For petitions filed after November 13, 2018, we interpret claim terms using "the same claim construction standard that would be used to construe the claim in a civil action under 35 U.S.C. 282(b)." 37 C.F.R. § 42.100(b) (2019). In this context, claim terms "are generally given their ordinary and customary meaning" as understood by a person of ordinary skill in the art in question at the time of the invention. *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312–13 (Fed. Cir. 2005) (en banc). "In determining the meaning of the disputed claim limitation, we look principally to the intrinsic evidence of record, examining the claim language itself, the written description, and the

prosecution history, if in evidence." *DePuy Spine, Inc. v. Medtronic Sofamor Danek, Inc.*, 469 F.3d 1005, 1014 (Fed. Cir. 2006) (citing *Phillips*, 415 F.3d at 1312–17). Extrinsic evidence is "less significant than the intrinsic record in determining 'the legally operative meaning of claim language.'" *Phillips*, 415 F.3d at 1317.

Any special definition for a claim term must be set forth in the specification with reasonable clarity, deliberateness, and precision. *In re Paulsen*, 30 F.3d 1475, 1480 (Fed. Cir. 1994).

We construe only those claim terms that require analysis to determine whether to institute *inter partes* review. *See Vivid Techs., Inc. v. Am. Sci. & Eng'g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999) (holding that "only those terms need be construed that are in controversy, and only to the extent necessary to resolve the controversy").

A. Specific Contact Resistivity

Petitioner argues that the term "specific contact resistivity," recited in claim 6, should be construed to be interchangeable with the term "specific contact resistivity." Pet. 15. Petitioner asserts that the Specification of the '395 patent and claim 6 use those terms interchangeably. *Id.* (citing Ex. 1001, 3:25–29, 3:42–45, 3:52–53, 4:22–30). Petitioner further asserts that ordinarily skilled artisans commonly used those terms interchangeably. *Id.* (citing Ex. 1133, 2; Ex. 1022, Schubert Decl. ¶¶ 74–76). Patent Owner's Preliminary Response did not respond explicitly to Petitioner's proposed construction. *See generally* Prelim. Resp. Our Institution Decision construed the terms "specific contact resistivity" and "specific contact resistance" to be interchangeable. Inst. Dec. 11. The Patent Owner Response does not request that we alter this construction. *See generally* PO Resp.

Upon review of the record, we construe the terms "specific contact resistivity" and "specific contact resistance" to be interchangeable.

III. ANALYSIS

"In an [*inter partes* review], the petitioner has the burden from the onset to show with particularity why the patent it challenges is unpatentable." *Harmonic Inc. v. Avid Tech., Inc.*, 815 F.3d 1356, 1363 (Fed. Cir. 2016) (citing 35 U.S.C. § 312(a)(3) (requiring inter partes review petitions to identify "with particularity . . . the evidence that supports the grounds for the challenge to each claim")). This burden of persuasion never shifts to Patent Owner. *See Dynamic Drinkware, LLC v. Nat'l Graphics, Inc.*, 800 F.3d 1375, 1378 (Fed. Cir. 2015) (discussing the burden of proof in *inter partes* review).

Anticipation is a question of fact, as is the question of what a prior art reference teaches. *In re NTP, Inc.*, 654 F.3d 1279, 1297 (Fed. Cir. 2011). "A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros. Inc., v. Union Oil Co.*, 814 F.2d 628, 631 (Fed. Cir. 1987); *see also Finisar Corp. v. DirecTV Grp., Inc.*, 523 F.3d 1323, 1334 (Fed. Cir. 2008) (to anticipate a patent claim under 35 U.S.C. § 102, "a single prior art reference must expressly or inherently disclose each claim limitation"). Moreover, "[b]ecause the hallmark of anticipation is prior invention, the prior art reference—in order to anticipate under 35 U.S.C. § 102—must not only disclose all elements of the claim within the four corners of the document, but must also disclose those elements 'arranged as in the claim.'" *Net MoneyIN, Inc. v. VeriSign, Inc.*, 545 F.3d 1359, 1369 (Fed. Cir. 2008) (quoting *Connell v. Sears, Roebuck & Co.*, 722 F.2d 1542, 1548 (Fed. Cir. 1983)).

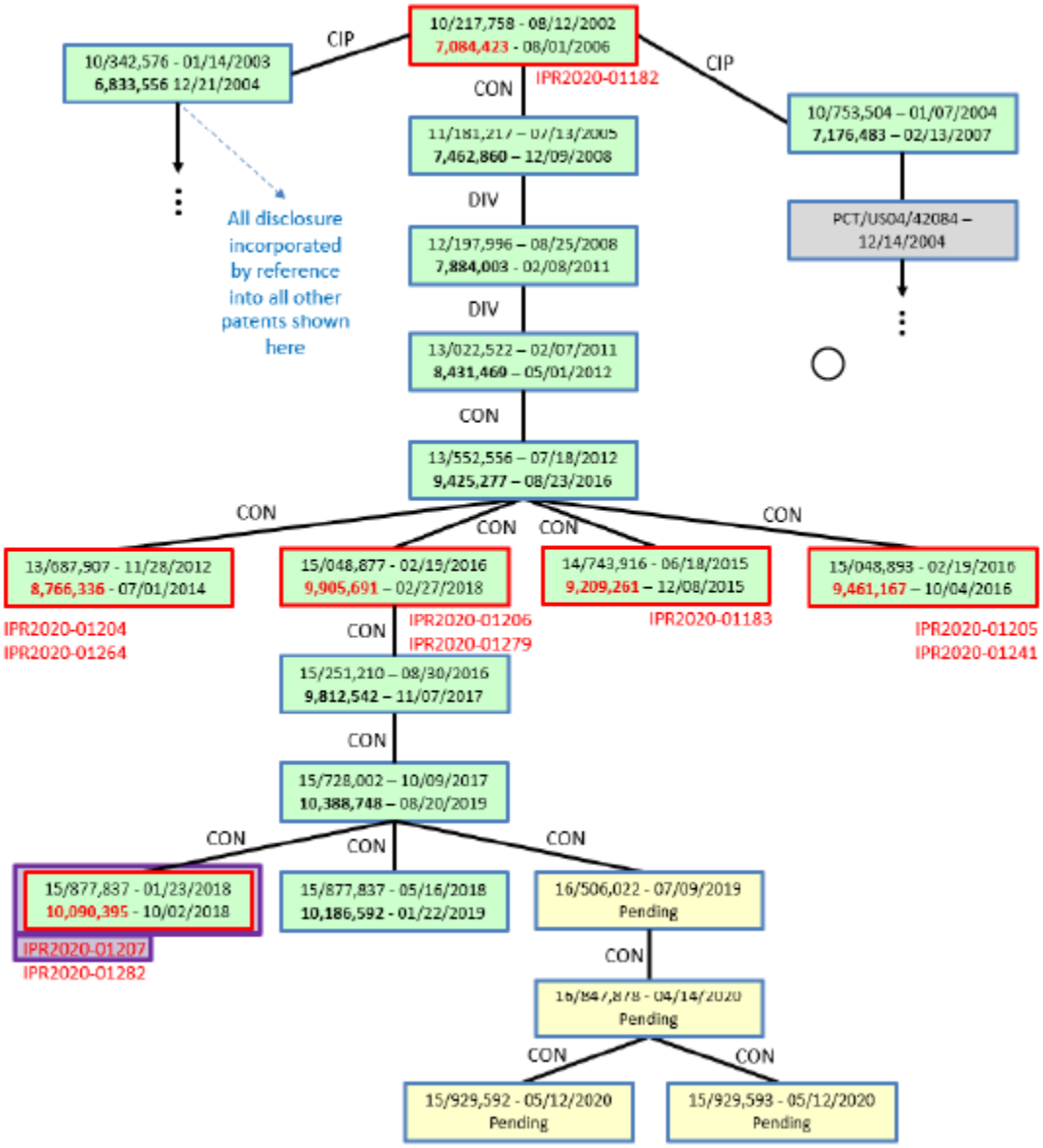
Whether a reference anticipates is assessed from the perspective of an ordinarily skilled artisan. *See Dayco Prods., Inc. v. Total Containment, Inc.*, 329 F.3d 1358, 1368 (Fed. Cir. 2003) ("'[T]he dispositive question regarding anticipation [i]s whether one skilled in the art would reasonably understand or infer from the [prior art reference's] teaching' that every claim element was disclosed in that single reference." (quoting *In re Baxter Travenol Labs.*, 952 F.2d 388, 390 (Fed. Cir. 1991))) (second two alterations in original).

Additionally, under the principles of inherency, if the prior art necessarily functions in accordance with, or includes, the claimed limitations, it anticipates. *MEHL/Biophile Int'l Corp. v. Milgraum*, 192 F.3d 1362, 1365 (Fed. Cir. 1999); *In re Cruciferous Sprout Litig.*, 301 F.3d 1343, 1349–50 (Fed. Cir. 2002).

A. Priority Issue

Petitioner contends the challenged claims are not entitled to any priority date before February 7, 2011, rendering Grupp '483, a member of the patent family that includes the '395 patent, prior art to the '395 patent. Pet. 16–22.

A chart provided in the Patent Owner Preliminary Response showing a partial patent family tree for the '395 patent, with annotations by Patent Owner, is provided below.



Partial Patent Family Tree

Prelim. Resp. 7. Petitioner contends that patentee did not describe the genus of the "metal oxide layer" recited in the challenged claims until the patentee filed the claims of U.S. application 13/022,522 ("the '522 application") on February 7, 2011. Pet. 17 (citing Ex. 1010, 48; Ex. 1022, Schubert Decl. ¶¶ 89–90). Petitioner further contends that no priority application enables the full scope of the recitation in claim 6 of a specific contact resistivity less

than 10 Ω-μm^2. *Id.* Thus, according to Petitioner, the priority date for claim 6 is no earlier than its filing date, i.e., January 23, 2018 and the filing date for the other challenged claims is no earlier than February 7, 2011. *Id.*

Patent Owner disputes Petitioner's contentions. PO Resp. 11–50. According to Patent Owner, the priority date of the '395 patent is the filing date of U.S. Patent No. 7,048,423 (Ex. 1002) ("'423 patent")) (August 12, 2002), and Grupp '483 is not prior art to the '395 patent. *Id.* at 1.

As mentioned above, Petitioner makes two sets of priority challenges: (i) challenges based on a purported lack of written description for the challenged claims in the pre-2011 priority applications and (ii) challenges based on a lack of enablement of claim 6 in all priority applications. We address these sets of challenges separately.

1. Written Description in the Priority Applications

We address Petitioner's priority challenges due to a purported lack of written description for two separate groups of challenged claims: (i) claims 1–6, 8–10, 15, and 16, which recite an "interface layer comprising a metal oxide," and (ii) claims 11, 12, and 14, which more narrowly recite "an oxide of titanium."

a. Claims 1–6, 8–10, 15, and 16

Claim 1 recites an "interface layer comprising a metal oxide." Ex. 1001, 18:45–52. Claim 2–6, 8–10, 15, and 16 each depend directly or indirectly from claim 1. *Id.* at 18:53–19:30.

1. Parties' Arguments

According to Petitioner, the first time any of the priority applications "arguably disclosed a generic 'metal oxide' interface layer is in the originally filed claims of U.S. Patent App. No. 13/022,522 filed on February 7, 2011." Pet. 19 (citing Ex. 1010, 48 [*see* claims 15, 16]; Ex. 1022,

Schubert Decl. ¶ 89). Petitioner acknowledges that the earlier-filed priority applications (those filed before 2011—"pre-2011 priority applications") describe a "possible example of a metal oxide interface layer" in the form of a TiO_2 [titanium dioxide] spacer layer. *Id.* (citing Ex. 1001, 18:6–8; Ex. 1022, Schubert Decl. ¶ 90). In fact, Petitioner relies on this description when arguing that Grupp '483 anticipates claim 1. *Id.* at 29–30 (citing Ex. 1022, Schubert Decl. ¶¶ 114–117). At the same time, Petitioner argues that Grupp '483 can be applied as a prior art reference because the same language in the pre-2011 priority applications fails to provide a written description of the genus of the recited "metal oxide layer." *Id.* at 18–22.

Petitioner asserts that the relevant question for this written description/priority issue is whether the pre-2011 priority applications' statement that "[s]pacer layers may be used with lower barriers (e.g., TiO_2 has a barrier of less than 1 eV)" provides a written description of the entire genus of metal oxide interface layers. Pet. 20 (citing Ex. 1001, 18:6–8) (alteration by Petitioner). Petitioner contends that the answer is no, arguing some metal oxides present considerably higher barriers than the "barrier of less than 1 eV" ascribed to TiO_2. *Id.* In particular, Petitioner argues "hafnium oxide and zirconium oxide are metal oxides with barriers to aluminum of 2 eV and 2.43 eV, respectively." *Id.* (citing Ex. 1035, 4; Ex. 1036, 1;[2] Ex. 1022, Schubert Decl. ¶ 94).

Patent Owner does not dispute that hafnium oxide and zirconium oxide have considerably higher barriers to metals than TiO_2. *See generally* PO Resp. Patent Owner, however, argues that the '423 patent (a pre-2011

[2] For Exhibits 1035 and 1036, we cite to the page numbers added by Petitioner.

priority application), as originally filed in 2002, nevertheless supports the genus of "metal oxide" in two ways. *Id.* at 43. First, Patent Owner argues that the specification discloses TiO_2 as a species. *Id.* (citing Ex. 1003, '423 patent, 17:59–61). Second, Patent Owner argues that the specification discloses oxide spacer/separation layers as a more general genus. *Id.* at 43–44 (citing Ex. 1003, '423 patent, 10:49–50). Patent Owner argues that these two disclosures demonstrate that the Acorn inventors possessed the "metal oxide" genus or subgenus. *Id.* at 44 (citing Ex. 2070, Kuhn Decl. ¶¶ 97–113). Patent Owner provides an analysis by Dr. Kuhn to support its argument that an ordinarily skilled artisan would have envisaged the metal oxide genus based on these disclosures. *Id.* at 43–46 (citing Ex. 2070, Kuhn Decl. ¶¶ 97–113).

Patent Owner also argues that the disclosure in the pre-2011 priority applications of the use of TiO_2 as material with a lower barrier does not teach away from the use of materials with higher barriers. PO Resp. 44–45 (citing Ex. 1003, '423 patent, 17:61–64; Ex. 2070, Kuhn Decl. ¶ 111). Further, Patent Owner argues that in an unrelated application Petitioner sought a claim to a metal oxide genus after disclosing only three species of metal oxides. *Id.* at 47 (citing Ex. 2099, claim 2, ¶¶ 8, 33, 39, 86, 96, 99, 100, 111, 140, 156, 161).

In its Reply, Petitioner argues that there are countless materials that contain metal oxides with just one metal. Pet. Reply 3. Further, Petitioner asserts that a metal oxide can include multiple metals. *Id.* (citing Ex. 1048, 211:8–212:3 (Kuhn deposition transcript); Ex. 1053, Schubert Reply Decl. ¶¶ 18–20). Petitioner also argues that metal oxides have varying properties. *Id.* at 4–5 (citing Ex. 1053, Schubert Reply Decl. ¶¶ 24–51). Further, Petitioner asserts that the claims of the '395 patent encompass metal oxides

that were invented after the priority applications were filed. *Id.* at 6–7 (citing Ex. 1048, 99:6–23).

In its Sur-reply, Patent Owner argues that the purpose of the written description requirement is to prevent over-claiming. PO Sur-reply 11–12. Patent Owner asserts that the pre-2011 priority applications describe the broader genus of oxides and, because the patentee could have claimed that genus, in this case, there is no concern of the patentee over-claiming metal oxides. *Id.*

Patent Owner also asserts that the disclosure of TiO_2 is sufficient to support the genus of metal oxides because it discloses structural features common to members of the genus so that an ordinarily skilled artisan can recognize the member of the genus. PO Sur-reply 12. Patent Owner asserts that, here, the metal oxide is in the spacer layer and a common structural feature of metal oxides used for such a purpose is that they are dielectrics. *Id.* Further, Patent Owner argues that Petitioner argued for its own patent application that the genus "metal oxide having a small conduction band offset with respect to the source/drain area" was supported by just TiO_2, Ta_2O_5, and ZnO. *Id.* at 13 (citing Ex. 2099, claims 2–3).

2. Analysis

We agree with Petitioner that the pre-2011 priority applications do not describe the recited genus.

To support a claim to a genus, a specification must disclose "either a representative number of species falling within the scope of the genus or structural features common to the members of the genus so that one of skill in the art can 'visualize or recognize' the members of the genus." *Ariad Pharms., Inc. v. Eli Lilly & Co.*, 598 F.3d 1336, 1350 (Fed. Cir. 2010) (en banc). Here, the recited genus is an interface layer comprising a metal

oxide. Ex. 1001, 18:45–52. It is undisputed that the only species the pre-2011 priority applications disclose is TiO_2, as set forth in the following passage:

> Two other properties of the dielectric deserve mention. First is the property of the height of the barrier compared to the semiconductor conduction band (for electrons). In making the barrier thinner than a silicide barrier, the tradeoff may be a higher tunnel barrier (e.g., 2 eV for nitride, compared with about half the gap of 0.6 eV for silicide). *Spacer layers may be used with lower barriers (e.g., TiO_2 has a barrier of less than 1 eV).* Nevertheless, even with the higher barrier to electrons, the present inventors have determined that the resistance can still be one hundred times lower than a contact to silicon with a silicide barrier.

Id. at 18:1–11 (emphasis added).

The pre-2011 priority applications incorporate by reference U.S. Patent No. 6,833,556 ("'556 patent"), which describes the use of metal oxides to isolate a transistor's gate from its channel. Ex. 1005, 7:60–8:22, 13:44–14:20; *see, e.g.*, Ex. 1001, 1:24–27, Ex. 1022, Schubert Decl. ¶¶ 91–93. It is undisputed, however, that this description in the '556 patent of metal oxides used to isolate a gate from its channel does not describe the recited genus. Ex. 1022, Schubert Decl. ¶¶ 91–93. The recited genus constitutes an interface layer that is conductive ("said region being *electrically connected* to the said metal interface layer *through said interface layer*"). Ex. 1001, 18:45–52 (emphasis added); Ex. 1022, Schubert Decl. ¶¶ 91–93.

The disclosure in the pre-2011 priority applications that "spacer layers may be used with lower barriers (e.g., TiO_2 has a barrier of less than 1 eV)" does not describe structural features common to the members of the genus so that one of skill in the art can visualize or recognize the members of the

genus. *See* Ex. 1022, Schubert Decl. ¶¶ 89–90, 93–97. The disclosure describes one property of TiO_2—it has a lower barrier of less than 1 eV, which is not a property of the recited genus as a whole. Hafnium oxide and zirconium oxide are metal oxides with barriers to the metal aluminum of 2 eV and 2.43 eV, respectively. *Id.* ¶ 94; Ex. 1035, 4; Ex. 1036, 1.

As mentioned, Patent Owner argues that the pre-2011 priority applications do not teach away from using materials with barriers of more than 1 eV, noting that the pre-2011 priority applications teach the disclosed techniques may be beneficial for such materials even if they are not as preferred as lower barrier materials. PO Resp. 44–45 (citing Ex. 1003, '423 patent, 17:61–64; Ex. 2070, Kuhn Decl. ¶ 111). That argument, however, misses the point. Although the pre-2011 priority applications may not teach away from higher barrier materials, the desirable property that those priority applications teach for TiO_2 is that it has a barrier of less than 1 eV, and that is not a property shared by metal oxides as a class.

As mentioned, Patent Owner also argues that the structural feature that is common to the members of the genus of metal oxides to be used for spacer layers is that they are dielectrics. PO Sur-reply 12 (citing Ex. 2070, Kuhn Decl. ¶¶ 107, 109). Even if we were to accept that argument, however, Patent Owner cites no evidence that an ordinarily skilled artisan would envision the recited genus merely from the fact that all metal oxides to be used as spacer layers are purportedly dielectrics. *See* Ex. 2070, Kuhn Decl. ¶¶ 107, 109. The cited testimony from Dr. Kuhn does not support such a contention, as Dr. Kuhn merely testifies that the '423 patent describes a MIGS separation layer as a dielectric and that dielectrics that do not passivate or only weakly passivate the semiconductor would be desirable. *Id.* Further, the '556 patent, which, as mentioned, is incorporated by

reference into the '395 patent and the pre-2011 priority applications, teaches that dielectrics are a broader class than metal oxides. Ex. 1005, 7:60–8:5. The '556 patent describes that dielectrics can be made from oxides of *semiconductors* as well as from metals: "the insulator 280 (which may be made of a dielectric such as an oxide of the metal gate or an oxide of a semiconductor)." *Id.* at 7:60–8:5. Thus, the disclosed use of a dielectric by itself is not the disclosure of a property that would lead an ordinarily skilled artisan to envision the recited genus of metal oxides.

In sum, the only disclosed property for the TiO_2 species—a lower barrier of less than 1 eV—would not cause an ordinarily skilled artisan to envision the recited genus.

TiO_2 is also not representative of the recited genus of metal oxides. The metal oxide genus encompasses many underlying species because there are many different metals that can form metal oxides, for example, alkali metals, alkaline earth metals, transition metals, ferrous metals, non-ferrous metals, noble metals, refractory metals, and common metals. Ex. 1053, Schubert Reply Decl. ¶ 18. Further, metal oxides can be formed from more than one metal species. *Id.* ¶¶ 19, 20. Significantly, important properties for the various metal oxides, such as conductivity,[3] vary significantly. *Id.* ¶¶ 19, 20, 27–51.[4]

[3] The electrical conductivity of a metal oxide is an important property for the recited genus because electrical conductivity directly affects the specific contact resistance of a junction, which is important property for the '395 patent's disclosure. *See* Ex. 1001, 3:25–4:30; Ex. 1053, Schubert Reply Decl. ¶ 30.

[4] Dr. Schubert characterizes TiO_2 as a semiconductor. Ex. 1053, Schubert Reply Decl. ¶ 51. Patent Owner argues that instead it is a dielectric. PO Sur-reply 7. Even if we were to find that TiO_2 is a dielectric, however, important properties of metal oxides would still vary significantly. *See*

As discussed above, Patent Owner nevertheless argues that the pre-2011 priority applications describe the recited genus due to the disclosure of oxide spacer/separation layers combined with the disclosure of an interface layer with TiO_2. PO Resp. 43. To support that argument, Patent Owner provides an analysis by Dr. Kuhn of how an ordinarily skilled artisan would purportedly envision the recited genus from these disclosures. *Id.* at 44–46 (citing Ex. 2070, Kuhn Decl. ¶¶ 97–113). We do not credit this analysis by Dr. Kuhn, however, because it relies on unsupported contentions regarding the knowledge of an ordinarily skilled artisan and on the premise that an ordinarily skilled artisan would take a series of mental steps that are not taught or suggested by the pre-2011 priority applications.

Dr. Kuhn begins her analysis with the disclosure in the '423 patent that TiO_2 is an example of a "spacer layer" or "separation layer" (the terms being used synonymously) with Ti as a possible metal for the metal-semiconductor junction. Ex. 2070, Kuhn Decl. ¶ 97. Referring to the spacer layer as the "MIGS separation layer," Dr. Kuhn asserts that an ordinarily skilled artisan would recognize from the TiO_2 layer example that an oxide of whatever metal is used as the metal in the metal-semiconductor junction would be desirable. *Id.* ¶ 98. Dr. Kuhn cites no teaching in the '423 patent or in any other reference, but further states that an ordinarily skilled artisan would recognize the value of a configuration in which the placement of a metal next to an oxide of that metal "is very likely to be more stable than having the metal adjacent to some other oxide." *Id.*

Ex. 1053, Schubert Reply Decl. ¶ 51; *see also id.* ¶¶ 27–50; Ex. 1022, Schubert Decl. ¶ 94. For example, HfO_2 is an insulator, whereas InSnO is a relatively good conductor. Ex. 1053, Schubert Reply Decl. ¶ 51.

According to Dr. Kuhn, the fact that the "'423 patent states the separation layer may be an oxide in general, would have directed [an ordinarily skilled artisan] to metal oxides in particular for reasons I will next explain." Ex. 2070, Kuhn Decl. ¶ 100. Nevertheless, after stating that metals other than titanium are disclosed in the patent, Dr. Kuhn acknowledges that "not all of these metals have oxides that would be acceptable as a spacer layer, many of them do have such oxides the details of which I describe in paragraphs 101-110." *Id.* ¶ 99. Noting that the interface layer may be a passivation layer or a single or compound layer including both a passivating material and an additional separation material, Dr. Kuhn states the layers should be well-behaved materials not displaying deleterious effects that would prevent their use in electrical devices. *Id.* ¶¶ 101–102.

Dr. Kuhn next notes that the '423 patent states "the interface layers serves to (i) chemically passivate the semiconductor surface . . . and (ii) to displace the semiconductor sufficiently to eliminate or at least reduce the effect of MIGS." Ex. 2070, Kuhn Decl. Ex. ¶ 103 (quoting Ex. 1003, '423 patent, 9:50–53). According to Dr. Kuhn, because the '423 patent explains that the passivation layer alone may not be sufficient to provide MIGS separation, an additional MIGS separation layer may be required. *Id.* ¶ 104. Dr. Kuhn states "[f]rom this description, [an ordinarily skilled artisan] would understand that the separation layer, when paired with a passivation layer, does not itself perform a passivation function, but is solely intended to provide the proper thickness and band structure so that the MIGS states arising in the metal cannot pin the Fermi level of the junction." *Id.* (emphasis omitted).

Dr. Kuhn next notes that the '423 patent discloses that passivation layers using N and/or O may not require distinct separation layers and

asserts that "[f]rom this [an ordinarily skilled artisan] would understand that a passivation material that is also an oxide (such as silicon dioxide or silicon oxy-nitride) would not be considered the distinct separation layers recited in the challenged claims, but rather a passivation layer." Ex. 2070, Kuhn Decl. ¶ 105 (citing Ex. 1003, '423 patent, 10:5–7) (emphasis omitted). Based on the '423 patent's disclosure that "in some cases such passivation layers are combined with separation layers (e.g., made of an oxide) to complete the interface layer" (Ex. 1003, 10:48–50), Dr. Kuhn asserts that "[an ordinarily skilled artisan] would understand that the separation layer is intended to be an oxide, but not one with the function of passivation" (Ex 2070, Kuhn Decl. ¶ 106).

Testifying that "the patent provides extensive teachings on metals versus non-metals" and the relationship between metals, conductive materials, and conductors, (Ex. 2070, Kuhn Decl. ¶ 108), Dr. Kuhn posits that an ordinarily skilled artisan would have understood or recognized that:

> (i) "using a metal for MIGS separation would *not* provide MIGS separation (the metal would simply make more MIGS states)";
>
> (ii) "using metal-like materials for the MIGS separation layer (i.e., metals, semi-metals (metalloids), and semiconductors would carry a similar risk of not fully suppressing MIGS states due the band structure of the materials";
>
> (iii) "the desired embodiments for the MIGS separation layer in a two-layer (passivation layer + separation layer) arrangement would be dielectrics and additionally would include (as per the patent's clarification that a passivation layer is distinct from a separation layer) dielectrics that do not passivate or only weakly passivate the semiconductor";
>
> (iv) "the position of the MIGS separation layer (always between the metal and the passivation layer) suggests metal oxides of the parent metal to improve chemical stability";

> (v) looking to "the complete list of metals provided in the patent (Al, In, Ti, Cr, Ta, Cs, Mg, Er, Yb, Mn, Pb, Ag, Y, Zn, Pt, Au, W, Ni, Mo, Cu, Co and Pd) . . . the most appropriate metal oxides would be conventional insulators with significant preexisting data due to the world-wide emphasis on high-k dielectrics at the time of the patent (families such as aluminum oxide, titanium oxide, and tantalum oxide)";
>
> (vi) there was "the possibility of using insulators from materials well-established in the semiconductor industry, although perhaps not as well researched as the high-k materials (families such indium oxide, magnesium oxide, zinc oxide, tungsten oxide, molybdenum oxide and yttrium oxide)";
>
> (vii) "certain materials might have appropriate insulating properties but would not be appropriate for semiconductor fabrication due either to well-known mismatches between materials properties and typical semiconductor processing conditions (e.g. families such as silver oxide and gold oxide) or environmental issues (e.g. families such as lead oxide)"; and
>
> (viii) "[t]he remaining oxides would be recognized as inappropriate choices as they are semiconductors or semimetals (metalloids)."

Ex. 2070, Kuhn Decl. ¶¶ 109–110.

Much of Dr. Kuhn's analysis is premised on her assessment of the mental steps that an ordinarily skilled artisan theoretically might have taken after reviewing the minimal disclosure in the '423 patent. The '423 patent does not discuss any properties of metal oxides (other than the lower barrier of the metal oxide TiO_2) or design considerations concerning the selection of particular oxides to use in the claimed structure, particularly in the context of MIGS separation. And Dr. Kuhn cites very little, if any, evidence to support her testimony regarding the knowledge of an ordinarily skilled artisan. Thus, we do not credit this analysis as showing that an ordinarily skilled artisan would have found that the inventors of the pre-2011 priority applications possessed the recited genus. *See Ariad*, 593 F.3d at 1352 (a

description that merely renders the invention obvious does not satisfy the written description requirement); *Power Oasis Inc. v. T-Mobile USA*, 522 F.3d 1299, 1306 (Fed. Cir. 2008) ("Entitlement to a filing date does not extend to subject matter which is not disclosed, but would be obvious over what is expressly disclosed.") (quoting *In re Huston*, 308 F.3d 1267, 1277 (Fed. Cir. 2002), quoting *Lockwood v. Am. Airlines, Inc.*, 107 F.3d 1565, 1571–72 (Fed. Cir. 1997)); *Martin v. Mayer*, 823 F.2d 500, 505 (Fed. Cir. 1987) (holding that the written description requirement is "not a question of whether one skilled in the art *might* be able to construct the patentee's device from the teachings of the disclosure . . . . Rather, it is a question whether the application necessarily discloses that particular device") (emphasis original).

As for Patent Owner's argument that the policy concern for the written description requirement does not apply here because the patentee purportedly had written description support for even broader subject matter than the recited genus, we disagree. PO Sur-reply 11. First, the written description for priority is a statutory requirement that cannot be avoided based merely on policy arguments. 35 U.S.C. § 120. Second, even with respect to the concern of over-claiming, the mere fact that the patentee purportedly had written description support for subject matter broader than claim 1 would not alleviate that concern. Written description support is only one of a number of requirements for patentability, and it would still be over-claiming for a patentee to obtain a claim that it did not describe to avoid a prior art rejection for a broader claim that it did describe.

As mentioned, Patent Owner argues that because Petitioner sought claims to a "metal oxide having a small conduction band offset with respect to the source/drain area" while purportedly only disclosing TiO_2, Ta_2O_5, and ZnO, Petitioner's position in that case is inconsistent with its position here.

PO Resp. 47 (citing Ex. 2099, claim 2, ¶¶ 8, 33, 39, 86, 96, 99, 100, 111, 140, 156, 161); PO Sur-reply 13 (citing Ex. 2099, claims 2–3). On this record, we do not reach such a conclusion. Patent Owner cites to the publication of the involved application (Ex. 2099), which shows that Petitioner has filed such claims and that the involved application discloses TiO_2, Ta_2O_5, and ZnO, but Patent Owner provides no analysis of how the purported support for a genus based on the disclosure of three species would conflict with an alleged lack of a support for a genius based on one species. PO Resp. 47; PO Sur-reply 13. Patent Owner further does not set forth any arguments that have been made in the prosecution of the involved application (Ex. 2099). PO Resp. 47; PO Sur-reply 13.

As for Patent Owner's argument that Petitioner's decision not to challenge claims 17 and 23 indicates that the pre-2011 priority applications support the recited genus, we disagree. PO Sur-reply 11. Petitioner challenged those claims in IPR2020-01282. *See* IPR2020-01282, Paper 2, 5. We cannot speculate as to why Petitioner chose not to challenge claims 17 and 23 of the '395 patent here. Whatever unexpressed reason Petitioner had for not challenging those claims in that proceeding is not in the record and is not evidence for consideration.

In sum, after considering all the arguments and evidence, we find that the pre-2011 priority applications do not describe the recited genus. Thus, Patent Owner is not entitled to the benefit of any pre-2011 priority applications for claims 1–6, 8–10, 15, and 16, and Grupp '483 is prior art for those claims.

b. Claims 11, 12, and 14

Claim 11 recites "wherein said metal oxide comprises an oxide of titanium." Ex. 1001, 19:20–21. Claim 12 depends from claim 11, and claim 14 depends from claim 12. *Id.* at 19:22–26.

The Petition does not address whether the pre-2011 priority applications describe the breadth of the oxide-of-titanium limitation. *See* Pet. 18–22. Instead, the Petition argues that the pre-2011 priority applications do not describe the breadth of the broader genus of metal oxides. *Id.* The Patent Owner Response asserts that the mere fact that the pre-2011 priority applications may not describe the broader class of metal oxides does not mean they fail to describe the breadth of the class of a metal oxide comprising an oxide of titanium. PO Resp. 38–42. In its Reply, Petitioner does not dispute this argument by Patent Owner, but instead presents substantive arguments as to why the pre-2011 priority applications purportedly fail to describe the breadth of the recited oxides of titanium. Pet. Reply 7–12. In its Sur-reply, Patent Owner argues that Petitioner's reply arguments are belated and should not be considered. PO Sur-reply 5–7.

We agree with Patent Owner. "[A p]etitioner may not submit new evidence or argument in reply that it could have presented earlier, e.g., to make out a prima facie case of unpatentability." Consolidated Trial Practice Guide[5] 73; *see also* 37 C.F.R. § 42.23(b). Here, Petitioner's breadth challenge to the written description support for the genus of "the metal oxide of the interface layer comprises an oxide of

[5] Consolidated Office Trial Practice Guide (Nov. 2019), available at https://www.uspto.gov/about-us/news-updates/consolidated-trial-practice-guide-november-2019.

titanium" recited in claims 6, 8, 10, 11, and 14–16, was part of Petitioner's prima facie case, which could have, and should have, been presented with the Petition. Thus, Petitioner could not properly wait until its Reply to specifically challenge the description support for the breadth of that class in the pre-2011 priority applications. *See Henny Penny Corp. v. Frymaster LLC*, 938 F.3d 1324, 1330–31 (Fed. Cir. 2019); *Intelligent Bio-Sys., Inc. v. Illumina Cambridge Ltd.*, 821 F.3d 1359, 1369–70 (Fed. Cir. 2016); *Ariosa Diagnostics v. Verinata Heath, Inc.*, 805 F.3d 1359, 1368 (Fed. Cir. 2015). Accordingly, we will not consider the breadth challenge to a metal oxide comprising an oxide of titanium that Petitioner presented for the first time in its Reply.

As for the breadth challenge presented in the Petition—that the pre-2011 priority applications do not describe the breadth of the class of metal oxides, that challenge is inapplicable here because claims 11, 12, and 14 narrow the recited class to comprising an oxide of titanium, which is a far narrower class. Dr. Schubert provides examples of numerous metal oxides that do not comprise oxides of titanium. Ex. 1022, Schubert Decl. ¶ 94 (hafnium oxide and zirconium oxide); Ex. 1053, Schubert Reply Decl. ¶¶ 18, 19 (*see* the compounds identified in that paragraph beyond titanium dioxide), 20.

Petitioner does not dispute that the pre-2011 priority applications disclose a species within the scope of the recited genus. Pet. 18–22. To the contrary, Petitioner relies on one of the pre-2011 priority applications (Grupp '483) as disclosing a species (with TiO_2) as proof that claims 11, 12, and 14 are anticipated. *See id.* at 40–44.

Thus, we determine that Petitioner has not proven that the pre-2011 priority applications fail to describe the genus of the metal oxide of the

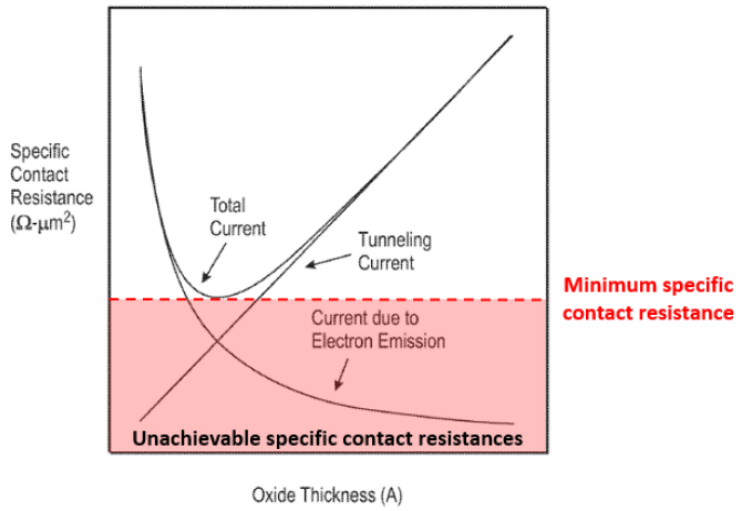
interface layer comprises an oxide of titanium. Therefore, Petitioner has not proven that Patent Owner is not entitled to the benefit of the pre-2011 priority applications for claims 11, 12, and 14 due to a lack of written description support. Accordingly, Petitioner has not proven that Grupp '483 is prior art for those claims.

2. Enablement of Claim 6 in the Priority Applications

Claim 6 recites "said interface layer is configured to provide a specific contact resistivity between the metal electrical contact and the region in the semiconductor of less than 10 Ω-μm^2." Ex. 1001, 19:4–7.

Petitioner argues that Patent Owner is not entitled to the filing dates of its priority applications for claim 6 because none of the priority applications enable the recited range of a specific contact resistivity in claim 6.

To illustrate the point, Petitioner offers an annotated version of Figure 8 of the '395 patent, as shown:



Petitioner's Annotated Version of Figure 8

Pet. 23. Petitioner argues that this figure shows how "the nadir of [the] 'total current' curve indicates a range of specific contact resistances down to and including approximately zero that an ordinarily skilled artisan could not

have attained by following the teachings of the '395 Patent and its parent applications." *Id.* at 24. Petitioner argues that claim 6 encompasses a range of specific contact resistivity down to and including approximately zero that cannot be achieved and thus cannot be enabled by the priority applications. *Id.*

Petitioner relies on *MagSil Corp. v. Hitachi Global Storage Techs., Inc.*, 687 F.3d 1377 (Fed. Cir. 2012). In that case, the claims recited that "applying a small magnitude of electromagnetic energy to the junction . . . causes a change in the resistance by at least 10% at room temperature." *Id.* at 1381 (alteration in original). The patent owner in *MagSil* offered testimony of an expert, who opined that "a person of ordinary skill in the art could work from the [] patent and make tunneling junctions with a resistive change between 100% and 120% without undue experimentation." *Id.* at 1382. The Federal Circuit, however, found that the testimony suggesting a resistive change up to 120% "only reaches a lower-end of the claimed scope," as "[t]he invention claims resistive changes from at least 10% up to infinity." *Id.* The Federal Circuit held that "the asserted claims are invalid for lack of enablement because their broad scope is not reasonably supported by the scope of enablement in the specification." *Id.* at 1384.

Patent Owner asserts that "[t]he vertical axis in Figure 8 has neither a scale nor numbers and therefore cannot be meaningfully compared to the numerical values recited in the claims"; that Petitioner "failed to establish that the '[u]nachievable' region in Figure 8 is an appreciable portion of the claimed range"; and that "[an ordinarily skilled artisan] would understand that the resistivity values achievable with the invention are quite low, perhaps even negligible or too low to measure." PO Resp. 14 (citing Ex. 2070, Kuhn Decl. ¶¶ 75, 77) (second alteration by Patent Owner).

Next, Patent Owner argues that "Figure 8 should not be understood, and would not have been understood by [an ordinarily skilled artisan], to imply zero specific contact resistivity as the petition asserts" because "[an ordinarily skilled artisan] would understand from the shapes of the curves on Figure 8 that the vertical scale is logarithmic and therefore does not extend down to zero." PO Resp. 15–16 (citing Ex. 2070, Kuhn Decl. ¶¶ 76–77, 91).

Patent Owner also argues that "Figure 8 is a 'conceptual' diagram meant to illustrate the principles of the physics involved, not any absolute values," that "[t]he particular curves illustrated on Figure 8 are for one set of materials (semiconductor, interface, and metal), and that "[i]f one or more of those materials is changed, then the curves would change." PO Resp. 16 (citing Ex. 2070, Kuhn Decl. ¶¶ 80–82). Patent Owner contends that "even if there is an unachievable region for one combination of materials, another set of materials would almost certainly have a minimum that is less (i.e., in the so-called 'unachievable' region)." *Id.* at 18.

Patent Owner then argues that "[t]he fact that some values of specific contact resistance may not be possible would simply mean that there is an inherent lower limit, below which Acorn's specification need not teach how to achieve." PO Resp. 18 (emphasis omitted). According to Patent Owner, "[t]he issue of enablement of open-ended ranges is a well-developed area of the law, and the controlling rule is that the specification need not enable the entirety of an open-ended range when there is an 'inherent' limit on the open end of the range." *Id.* at 18–19. Patent Owner relies on *Andersen Corp. v. Fiber Composites, LLC*, 474 F.3d 1361 (Fed. Cir. 2007), *Rimfrost AS v. Aker Biomarine Antarctic AS*, PGR2018-00033, Paper 9 (Aug. 29, 2018), and *Ex parte Smith*, Appeal No. 2017-010042, 2019 WL 6173250 (PTAB Sept. 30, 2019). Patent Owner also asserts that its position "is a corollary to the

related principle that a patentee need not show that non-operable embodiments are enabled." PO Resp. 21.

Patent Owner contends that the Board and courts regularly decline to follow *MagSil* where, as here, there is an inherent limit on the open end of a range. PO Resp. 21–22 (citing *Snap-on Inc. v. Milwaukee Electric Tool Corp.*, IPR2015-01242, Paper 10 (PTAB Dec. 2, 2015); *Thermo Fisher Scientific Inc. v. Regents of Univ. of California*, IPR2018-01347, Paper 10 (Jan. 22, 2019); *PerkinElmer Health Scis., Inc. v. Agilent Techs., Inc.*, 962 F. Supp. 2d 304 (D. Mass. 2013)). Patent Owner additionally argues that "[an ordinarily skilled artisan] would have understood there to be an inherent lower limit for specific contact resistivity for a given set of materials," and that "Figure 8 . . . clearly illustrates that lower limit," as "the minimum of the 'Total' curve." PO Resp. 24.

Patent Owner further cites testimony from Dr. Kuhn that "Figure 8 conveys to [an ordinarily skilled artisan] a simple experiment to find a minimum or near-minimum specific contact resistivity for a given set of materials" and that "[an ordinarily skilled artisan] could have run simple experiments on 'test chip[s]' in a 'development fab' to vary the thickness of the interface layer, measure the specific contact resistance by well-known methods, and thereby determine the minimum or a near-minimum specific contact resistance and corresponding interface layer thickness." PO Resp. 26 (citing Ex. 2070, Kuhn Decl. ¶¶ 83–87) (last alteration in original). Patent Owner argues that "[an ordinarily skilled artisan] could have repeated that experiment with different materials, aided by the teachings (materials and interface layer thickness ranges) in the . . . patents, until an acceptably low specific contact resistance was found" and that "[t]he amount of

experimentation to do so would not have been undue." *Id.* (citing Ex. 2070, Kuhn Decl. ¶¶ 87–88).

Petitioner responds that Patent Owner "asks the Board to rewrite the claims to include some unspecified 'inherent lower limit'" and that if the Patent Owner "wanted the claims to include some lower limit," it "could have attempted to remedy the claims via Motion to Amend." Pet. Reply 18. Petitioner argues that the disclosures "fail to even hint at what that purported 'inherent lower limit' may be or how achieve it" and that "[n]either Figure 8 nor anything else in the specification discloses exemplary materials, thicknesses, or any other means for achieving the full range of claimed SCRs [specific contact resistivities] (e.g., lower than 1 Ω-μm^2 and approaching 0 Ω-μm^2)." *Id.* at 19–20 (emphasis omitted).

We begin our analysis by noting that Petitioner has the burden of proving that Patent Owner is not entitled to the benefit of its priority applications. *Dynamic Drinkware*, 800 F.3d at 1378.

Neither party asks for a construction of the subject claim language, and we determine that the plain meaning of "a specific contact resistivity . . . of less than 10 Ω-μm^2" would encompass all specific contact resistances below 10 Ω-μm^2 and down to zero.

As noted above, the parties both focus on Figure 8. Petitioner argues that it shows a region below the minimum of the Total Current curve that is not enabled. *See* Pet. 22–26; Ex. 1022, Schubert Decl. ¶ 104 (explaining that the sum of the resistance to tunneling current with and resistance to current due to electron emission depicted in Fig. 8 "leaves a range of specific contact resistances that cannot be achieved using the techniques in the '395 Patent"); *see also id.* ¶ 105 ("[T]he claims encompass something

that cannot be achieved according to the '395 Patent: specific contact resistances all the way down to and including approximately zero").

Patent Owner argues that the figure is not meaningful because it does not have scales on the axes, because it may be logarithmic, and because it may show resistivity values that are negligible or too low to measure. PO Resp. 14–16. We find these arguments somewhat off the mark, because the issue we need to resolve is whether the disclosure enables the specific numerical range recited in the claims. As Dr. Kuhn observes, Figure 8 merely illustrates how the tunneling resistivity increases as the thickness of the interface layer increases, the electron emission resistivity decreases as the thickness increases, and the how those behaviors affect the total current. *See* Ex. 2070, Kuhn Decl. ¶¶ 73–75. We agree that one cannot discern any "numerical values of specific contact resistance" from Figure 8. *See id.* ¶ 75.

As for the recited range, Patent Owner does not dispute, and the evidence shows, that the disclosure does not enable specific contact resistance down to zero. Ex. 1022, Schubert Decl. ¶¶ 99–106. Instead, Patent Owner argues that an ordinarily skilled artisan would have understood there to be an "inherent lower limit" and that the claims are enabled because one of skill in the art could achieve that lower limit through experimentation based on the disclosure of patent. PO Resp. 18–25. We are not persuaded by Patent Owner's argument, for two main reasons.

First, we do not agree that the cases cited by Patent Owner establish that the enablement requirement is satisfied if an ordinarily skilled artisan could experiment in accordance with the disclosure to find a practical end of an open-ended range recited in a claim. Patent Owner principally relies on *Andersen Corp. v. Fiber Composites*, but the Federal Circuit in that case

affirmed the jury verdict of enablement because "the upper limit of the Young's modulus of the structural member would lie somewhere between the Young's modulus of the wood fiber and that of the polymer used in the composition." 474 F.3d at 1377. In other words, there were two known quantities that provided a fixed range. That is not the case here, where Patent Owner does not point to any such predefined limits. Patent Owner also cites a district court case, *PerkinElmer Health Sciences, Inc. v. Agilent Technologies., Inc.*, 962 F. Supp. 2d 304, 310 (D. Mass. 2013). That case is not directly on point, because it was considering claim construction and not enablement, but that court also found an existing practical upper limit to the claimed range of molecular weights, explaining that "the largest known proteins at the time of patenting had a high, but definite, mass."[6] *Id.*

We also disagree with Patent Owner's suggestion that its position is supported by the principle that "a patentee need not show that non-operable embodiments are enabled." PO Resp. 21. It would be both circular and contrary to the important policy underlying the enablement requirement to allow it to be avoided by argument that subject matter within the scope of the claims that is not enabled may simply be disregarded as "inoperable." *See Alcon Research, Ltd. v. Apotex Inc.*, 687 F.3d 1362, 1368 (Fed. Cir. 2012) ("This is not how patent law works. When you claim a concentration range of 0.0001–5% w/v (as claim 2), you can't simply disavow the invalid portion and keep the valid portion of the claim. If everything up to 0.001%

[6] Patent Owner additionally cites several Board decisions in *inter partes* reviews and an *ex parte* appeal. They are not binding on us, and we find them unpersuasive because they are based on different facts. *See Scripps Clinic & Research Found. v. Genentech, Inc.*, 927 F.2d 1565, 1572 (Fed. Cir. 1991) (explaining the "appropriateness [of open-ended claims] depends on the particular facts of the invention, the disclosure, and the prior art").

w/v is admittedly not enabled, then the entire claim is invalid."). *In re Cook*, 439 F.2d 730 (CCPA 1971), cited by Patent Owner, explains that the presence of inoperative embodiments within the claim scope is permissible "so long as it would be obvious to [a skilled artisan] how to make the embodiment operative rather than inoperative." *Id.* at 734–35. *In re Cook* is inapplicable here because neither party has argued or offered any evidence that it would have been obvious to a skilled artisan how to make the lower part of the recited range operative or enabled.

Second, even if Patent Owner could rely on experiments based on the disclosure to find an "inherent lower limit," it has not alleged that the results would reveal a lower bound that would fall into the claimed range. Instead, Patent Owner and its expert assert that "Figure 8 conveys to [an ordinarily skilled artisan] a simple experiment to find a minimum or near-minimum specific contact resistivity for a given set of materials" and that "[i]f desired, [an ordinarily skilled artisan] could have repeated that experiment with different materials, aided by the teachings (materials and interface layer thickness ranges) in the Acorn patents, until an acceptably low specific contact resistance was found" or, as described by Dr. Kuhn, until "an acceptably low specific contact resistance was found." PO Resp. 26; Ex. 2070, Kuhn Decl. ¶¶ 83, 88. But even if we accept those assertions as true, they show only that the disclosure enables experimentation to determine a resistance that was "suitable" or "acceptably low," and we fail to see how that identifies a specific contact resistance that would form an inherent lower end of the claimed range of less than 10 Ω-μm^2.

We also find Dr. Kuhn's "inherent lower limit" analysis flawed. We agree that the minimum of the "Total Current" curve in Figure 8 represents an inherent lower limit of the contact resistance for a specific set of

materials. *See* Ex. 2070, Kuhn Decl. ¶ 89. However, Dr. Kuhn asserts, with reference to the annotated version of Figure 8 below, that "'specific contact resistivity less than X' really means X > SCR ≥ Y, where *Y is an inherent lower limit*." *Id.* ¶ 90 (emphasis added).

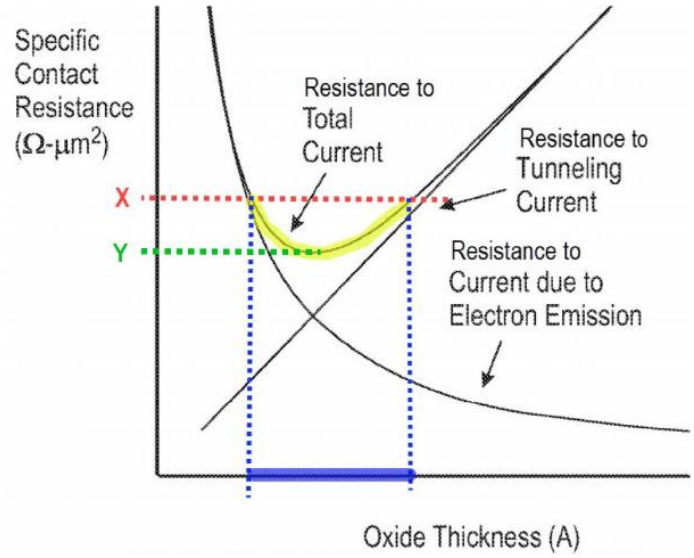


Figure 8 as Annotated by Dr. Kuhn (Ex. 2070 ¶ 90).

We find Dr. Kuhn's interpretation of the claim language to present a claim construction issue that was not raised in the Patent Owner Response and is now waived. (*See* Paper 25, 8 ("Patent Owner is cautioned that any arguments not raised in the response may be deemed waived.").) But we also disagree with Dr. Kuhn's interpretation, at least to the extent it is represented in annotated Figure 8, because that figure considers only one physical system, where the claims are not so limited. We read the claim language—"interface layer configured to provide a specific contact resistivity between the contact metal and the semiconductor of less than 1 Ω-μm²"—to mean that the claims encompass devices with interface layers that are otherwise within their scope and in which the minimum of the "Total Current" curve falls between 1 Ω-μm² and zero. This means that any

"inherent lower limit" would be the lowest resistance that could be achieved for an interface layer in *any physical device that meets the other limitations of the claims*. *See* Ex. 2070, Kuhn Decl. ¶¶ 81–82 (describing and illustrating different curves for different physical systems).

Petitioner provides evidence that "[e]ven two years after the earliest Priority Application was filed, [Patent Owner] had not achieved—and, accordingly, had not enabled—the full range of the claimed SCRs," as "the lowest reported SCR values that [Patent Owner] was able to achieve was approximately 300 Ω-μm^2," and that "those values were achieved with a silicon nitride interface layer (not the claimed metal oxide)." Pet. Reply 20–21 (citing Ex. 1057, Fig. 3; Ex. 1053, Schubert Reply Decl. ¶¶ 80–81) (emphasis omitted). Petitioner provides further evidence that "after over a decade of additional research and innovation, researchers in 2013 finally reported achieving an SCR value of about 0.1 Ω-μm^2 using an interface layer material—ZnO—not disclosed or contemplated by the Priority Applications." *Id.* at 22 (citing Ex. 1052, 2). Patent Owner responds that it "was not required to demonstrate the full range of its invention's possibilities" and "[t]hat [it] did not continue to optimize its invention is irrelevant." PO Sur-reply 19. We agree that Patent Owner had no obligation to optimize, or even practice, the patented inventions, but this evidence does tend to suggest that achieving at least some of the claimed range was not a simple matter of trying various combinations of disclosed materials. *Cf. MagSil*, 687 F.3d at 1382 (relying on the patent owner's post-filing activities when assessing enablement).

Patent Owner also argues that "[r]eferring to a resistivity or resistance range with an unspecified lower end is 'common in this art.'" PO Resp. 26 (quoting Ex. 2070, Kuhn Decl. ¶ 91 and citing, *e.g.*, Ex. 2034, 3:27–39;

Ex. 2035, 3:23–24). We conclude that unrelated patents, with entirely different disclosures and claims, are not pertinent to our analysis, particularly given that it has not been established that they do not also have enablement problems.

Finally, Patent Owner argues that a Primary Patent Examiner "having deep familiarity with this technology in general and [Patent Owner's] patents in particular, recently allowed nine Acorn claims reciting 'a specific contact resistivity of less than 1 [or 10] $\Omega \cdot \mu^2$' after considering the arguments made in the petition." PO Resp. 30 (emphasis omitted). The record does show that the Examiner initialed the IDS entries for ten IPR petitions in this family and ten copies of the Schubert Declaration. *See* Ex. 2062, 349–355. However, we are unable to discern the extent to which she considered the enablement issue and, as such, we will reach our own result from our substantially more developed record on this issue.

For the reasons given above, we conclude that (1) the plain language of the challenged claims encompasses specific contact resistances down to zero, (2) Petitioner has proven with *undisputed* evidence that the disclosures of the priority applications do not enable resistances down to zero, (3) the record does not indicate there is an "inherent lower limit" for specific contact resistances that would satisfy the requirement that the full scope of the claims be enabled in the priority applications, and (4) because Petitioner has shown that the subject matter of the challenged claims is not enabled in the priority applications, claim 6 is not entitled to the benefit of the filing dates of the priority applications due to a lack of the enablement of that claim in the priority applications. Thus, for this additional reason, Grupp '483 is prior art for claim 6.

B. Anticipation

1. Claims 1–6, 8–10, 15, and 16

Petitioner contends that Grupp '483 discloses every element of claims 1–6, 8–10, 15, and 16. Pet. 26–44. Patent Owner does not dispute this contention. PO Resp. 50 ("There are no disputes in this IPR regarding whether the 'prior art' reference (Acorn's own Grupp '483 patent) teaches any of the claim limitations.").

As set forth below, we find that Petitioner has proven that Grupp '483 anticipates claims 1–6, 8–10, 15, and 16.

a. Claim 1

Petitioner argues that Grupp '483 discloses an electrical junction, citing Grupp 483's disclosure that "the present invention provides an electrical junction." Pet. 27 (citing Ex. 1021, Grupp '483, 3:44–47). Petitioner further argues that Grupp '483 discloses a region in a semiconductor substrate by describing a source or drain of a transistor. *Id.* at 28 (citing Ex. 1022, Schubert Decl. ¶ 110). According to Petitioner, Grupp '483 discloses a metal electrical contact to said region by describing "an electrical device in which an interface layer is disposed between and in contact with a metal and a semiconductor." *Id.* (quoting Ex. 1021, Grupp '483, 4:21–23) (emphasis omitted). Petitioner asserts that Grupp '483 discloses "said region being electrically connected to said metal electrical contact through said interface layer" by describing "the present invention provides an electrical device in which an interface layer is disposed between and in contact with a metal and a semiconductor and is configured to depin the Fermi level of the semiconductor while still permitting current flow between the metal and the semiconductor . . . ." *Id.* at 29 (quoting Ex. 1021, Grupp '483, 4:21–26) (emphasis omitted).

Petitioner further argues that Grupp '483 discloses "said interface layer comprising a metal oxide and a semiconductor oxide" by describing an interface layer that includes (1) a passivation layer, which can be a semiconductor oxide; and (2) a separation layer, which can be titanium dioxide, a metal oxide. Pet. 29 (citing Ex. 1022, Schubert Decl. ¶ 114). Petitioner further asserts that Grupp '483 discloses "being in contact with said region in the semiconductor substrate and said metal electrical contact" by describing "an interface layer is disposed between and in contact with a metal and a semiconductor." *Id.* (quoting Ex. 1021, Grupp '483, 4:21–23) (emphasis omitted). After reviewing Petitioner's arguments and evidence, we find that Petitioner has proven that Grupp '483 anticipates claim 1.

b. Claim 2

Claim 2 recites the electrical junction of claim 1, "wherein the semiconductor oxide comprises an oxide of the region in the semiconductor substrate." Ex. 1001, 18:53–55. Petitioner argues that Grupp '483 discloses this wherein limitation by describing: the use of oxygen in a passivation layer, that oxygen that can form a compound of silicon, and the use of silicon dioxide as a passivating material. Pet. 31 (citing Ex. 1021, Grupp '483, 8:64–9:10, 10:60–63, 11:35–38; Ex. 1022, Schubert Decl. ¶ 125). After reviewing Petitioner's arguments and evidence, we find that Petitioner has proven that Grupp '483 anticipates claim 2.

c. Claim 3

Claim 3 recites the electrical junction of claim 2, "wherein the semiconductor oxide has a thickness of approximately 0.1 nm to 5 nm." Ex. 1001, 18:56–58. Petitioner argues that Grupp '483 discloses this wherein limitation by describing: "the interface layer 520 includes or is made up of a passivation layer with a thickness of between approximately

0.1 nm and about 5 nm." Pet. 32 (quoting Ex. 1021, Grupp '483, 10:66–11:1). After reviewing Petitioner's arguments and evidence, we find that Petitioner has proven that Grupp '483 anticipates claim 3.

d. Claim 4

Claim 4 recites the electrical junction of claim 1, "wherein said region in the semiconductor substrate comprises a source or drain of a transistor." Ex. 1001, 18:59–61. Petitioner argues Grupp '483 discloses this wherein limitation by describing source or drain semiconductor regions of a transistor. Pet. 33 (citing Ex. 1021, Grupp '483, 18:19–20, 19:11–15). After reviewing Petitioner's arguments and evidence, we find that Petitioner has proven that Grupp '483 anticipates claim 4.

e. Claim 5

Claim 5 recites the electrical junction of claim 1, "wherein said interface layer has a thickness sufficient to depin a Fermi level of the metal electrical contact in a vicinity of the junction." Ex. 1001, 18:62–64. Petitioner argues that Grupp '483 describes this wherein limitation by describing "[a]t this thickness the effect of MIGS has been sufficiently reduced to depin the metal and lower the Schottky barrier, and the layer is still sufficiently thin to allow significant current flow across the interface layer." Pet. 33 (quoting Ex. 1021, Grupp '483, 15:50–54).

Claim 5 further recites:

> yet thin enough to provide the junction with a specific contact resistivity that is generally dependent on: a workfunction of the metal electrical contact, a Fermi energy of the semiconductor in the region, or both the workfunction of the metal electrical contact and the Fermi energy of the semiconductor in the region.

Ex. 1001, 18:64–19:3. Petitioner argues that Grupp '483 describes this wherein limitation by describing an interface layer thin enough to provide

the junction with a specific contact resistivity that is generally dependent on a workfunction of the metal electrical contact. Pet. 34–36 (citing Ex. 1021, Grupp 483, 3:3–5, 17:28–45; Ex. 1022, Schubert Decl. ¶¶ 138–141). After reviewing Petitioner's arguments and evidence, we find that Petitioner has proven that Grupp '483 anticipates claim 5.

f. Claim 6

Claim 6 recites the electrical junction of claim 1, "wherein said interface layer is configured to provide a specific contact resistivity between the metal electrical contact and the region in the semiconductor of less than 10 Ω-μm^2." Ex. 1001, 19:4–7. Petitioner argues that Grupp '483 describes this wherein limitation by describing: "Indeed, minimum specific contact resistances of less than or equal to approximately 10 Ω-μm^2 or even less than or equal to approximately 1 Ω-μm^2 may be achieved for such junctions in accordance with the present invention." Pet. 37 (quoting Ex. 1021, Grupp '483, 6:1–5).

Patent Owner does not dispute that Grupp '483 discloses all of the limitations of claim 6 and is an enabling prior art reference. Patent Owner argues, however, that it would be inconsistent to use Grupp '483 as prior art to anticipate claim 6 while denying Patent Owner the benefit of priority applications due to a lack of enablement in the priority applications of the recited range of specific contact resistivity. PO Resp. 28–30. We disagree.

"The standard for what constitutes proper enablement of a prior art reference for purposes of anticipation under section 102 . . . differs from the enablement standard under section 112." *Rasmusson v. SmithKline Beecham Corp.*, 413 F.3d 1318, 1325 (Fed. Cir. 2005). Enablement under section 112, which is required for priority under section 120, requires enablement of the full breadth of a claim. *Wyeth & Cordis Corp. v. Abbott Labs.*, 720 F.3d

1380, 1384 (Fed. Cir. 2013); *MagSil*, 687 F.3d at 1384; 35 U.S.C. § 120. Enablement for anticipation does not; rather it requires only enablement of an embodiment or embodiments that fall within the scope of the claim. *Chester v. Miller*, 906 F.2d 1574, 1577 (Fed. Cir. 1990) ("a CIP's claim for a genus might not be enabled by a parent's disclosure, but that parent may enable a species that anticipates the CIP's claim for a genus . . . . the Court of Custom and Patent Appeals [] made clear the differences between the requirements for claim-anticipating disclosures and for claim-supporting disclosures") (citing *In re Lukach*, 442, F.2d 967, 969–970 (CCPA 1971)).

Here, the enablement challenge for priority is for a lack of enablement of the full breadth of the recited range, and, in particular, a lack of enablement of the lower part of the recited range (that which is at or near zero). No party has argued that the upper part of the recited range (just below 10 Ω-μm^2) is not enabled by either the priority applications or Grupp '483. *See, e.g.*, Pet. 22–26; PO Resp. 1–2; Pet. Reply 27–28; PO Sur-reply 17–18. And enablement by a prior art patent is presumed. *In re Antor Media Corp.*, 689 F.3d 1282, 1287 (Fed. Cir. 2012) *Impax Labs., Inc. v. Aventis Pharm., Inc.*, 545 F.3d 1312, 1316 (Fed. Cir. 2008); *Amgen, Inc. v. Hoechst Marion Roussel, Inc.*, 314 F.3d 1313, 1355 (Fed. Cir. 2003). Thus, the record does not reflect an inconsistency in holding the priority applications as not enabling the breadth of the recited range while treating Grupp '483 as enabling the upper part of the range for anticipation.

After reviewing Petitioner's arguments and evidence, we find that Petitioner has proven that Grupp '483 anticipates claim 6.

g. Claim 8

Claim 8 recites the electrical junction of claim 1, "wherein said metal oxide comprises an oxide of said metal electrical contact." Ex. 1001, 19:10–

11. Petitioner asserts that Grupp '483 discloses this wherein limitation by describing titanium as a metal electrical contact and titanium dioxide. Pet. 39 (citing Ex. 1021, Grupp '483, 4:13–20, 14:58–15:2, 18:65–67, claim 7; Ex. 1022, Schubert Decl. ¶ 148). After reviewing Petitioner's arguments and evidence, we find that Petitioner has proven that Grupp '483 anticipates claim 8.

h. Claims 9 and 10

Claims 9 and 10 are identical. Ex. 1001, 19:12–17. Both claims recite the electrical junction of claim 8, "wherein said semiconductor oxide comprises an oxide of the region in the semiconductor substrate." *Id.* Petitioner argues that Grupp '483 discloses this wherein limitation by describing: the use of oxygen in a passivation layer, that oxygen that can form a compound of silicon, and the use of silicon dioxide as a passivating material. Pet. 31, 40 (citing Ex. 1021, Grupp '483, 8:64–9:10, 10:60–63, 11:35–38; Ex. 1022, Schubert Decl. ¶¶ 125, 151). After reviewing Petitioner's arguments and evidence, we find that Petitioner has proven that Grupp '483 anticipates claims 9 and 10.

j. Claim 15

Claim 15 recites the electrical junction of claim 1, "wherein said metal electrical contact comprises titanium." Ex. 1001, 19:27–28. Petitioner argues that Grupp '483 discloses this wherein limitation by describing the use of titanium as a metal electrical contact. Pet. 44 (citing Ex. 1021, Grupp '483, 4:13-20, 14:58-15:2, claim 7). After reviewing Petitioner's arguments and evidence, we find that Petitioner has proven that Grupp '483 anticipates claim 15.

k. Claim 16

Claim 16 recites the electrical junction of claim 1, "wherein said metal electrical contact comprises tungsten." Ex. 1001, 19:29–30. Petitioner argues that Grupp '483 discloses this wherein limitation by describing the use of tungsten (W) as a metal electrical contact. Pet. 44 (citing Ex. 1021, Grupp '483, 4:13–20, 14:58–15:2, claim 8). After reviewing Petitioner's arguments and evidence, we find that Petitioner has proven that Grupp '483 anticipates claim 16.

2. Claims 11, 12, and 14

As set forth in Section III.A.1.b above, Petitioner has not proven that Patent Owner is not entitled to the benefit of its priority applications for claims 11, 12, and 14. Thus, Petitioner has not proven that Grupp '483 is prior art to these claims. Accordingly, Petitioner has not proven that Grupp '483 anticipates claims 11, 12, and 14.

C. Motion to Exclude

Patent Owner seeks to exclude the following portion of the cross-examination testimony of Dr. Kuhn: page 114, line 10 through page 123, line 14 of her deposition transcript (Exs. 1042, 1043). Mot. Excl. 1, 5. Patent Owner argues that the testimony at issue concerns the scope of claims that recite "an oxide of titanium." *Id.* at 1. According to Patent Owner, however, the oxide-of-titanium limitation was not substantively addressed in the Petition and Dr. Kuhn did not address it in her declaration. *Id.* Further, Patent Owner argues that it timely objected to the testimony at issue and thus the testimony should be excluded for exceeding the scope of Dr. Kuhn's direct testimony. *Id.* at 1–2.

Petitioner disagrees, arguing that Dr. Kuhn expressly opined on the "oxide of titanium" limitation. Opp. Mot. Excl. 1. Petitioner asserts:

> First, Dr. Kuhn opined that "nothing in the petition or Dr. Schubert's declaration specifically address[ed] the written-description support of those dependent claims or an oxide of titanium." Ex. 2070, Kuhn Decl. at ¶114. Second, Dr. Kuhn opined that "the metal oxide comprises an oxide of titanium" claims are "clearly narrower than 'metal oxide.'" *Id.*

Id. at 1–2 (emphasis omitted). Petitioner argues that it was entitled to explore Dr. Kuhn's understanding of why she believes those claim limitations are "clearly narrower" and to challenge Dr. Kuhn's assertion that they were not addressed in the petition or in Dr. Shubert's declaration. *Id.* at 2.

Patent Owner responds that Dr. Kuhn merely stated that the class of oxides of titanium is clearly narrower than the class of metal oxides and did not provide an opinion on that issue. Reply Mot. Excl. 1. Patent Owner further argues that statement did not open the door to Petitioner's questioning regarding the titanium oxide genus. *Id.* at 2.

We dismiss Patent Owner's Motion to Exclude as moot in light of our determination regarding Petitioner's written description challenge to Patent Owner's benefit of its pre-2011 priority applications for claims 11, 12, and 14. In particular, Petitioner relies on the testimony at issue to support its belated challenge to the breadth of written description support in the pre-2011 priority applications for the class of comprising an oxide of titanium that is recited by those claims. Reply Br. 7–12. Because we decided not to consider that belated challenge (*see* Section III.A.1.b above), the Motion to Exclude is moot.

D. Other Issues

1. 35 U.S.C. § 311(b)

Patent Owner argues that "[t]here are no disputes in this IPR regarding whether the 'prior art' reference ([Patent Owner]'s own Grupp

'483 patent) teaches any of the claim limitations" and that "[f]or all intents and purposes, this IPR is a § 112 battle, just as if it were a PGR (for which the pre-AIA '395 Patent is not eligible)." PO Resp. 50.

Patent Owner further argues that "there is no priority dispute here regarding enablement" because "the petition does not assert that any subsequent developments after the filing of the earliest priority/benefit application (resulting in the '423 Patent) has changed the enablement issue," meaning that "either all of the specifications are enabling of the specific contact resistance ranges recited in the claims, or none of them are." PO Resp. 50–51 (emphasis omitted). Patent Owner concludes that "[e]ntertaining the enablement challenge here would open the door for enablement challenges to a broad class of continuation patents in IPRs that Congress never intended." *Id.* at 51.

We remain unpersuaded by Patent Owner's argument that an *inter partes* review may not address whether priority applications enable or have written description support for challenged claims. Although the issue of whether challenged claims are enabled by or have written description support in the specification of the challenged patent is beyond the scope of an *inter partes* review (35 U.S.C. § 311), whether a patent is entitled to the benefit of earlier filed applications under 35 U.S.C. §§ 119 or 120 is properly an issue to be addressed in an *inter partes* review. *Indivior UK Ltd. v. Dr. Reddy's Lab'ys S.A.*, 18 F.4th 1323, 1326–1330 (Fed. Cir. 2021). And the benefit of an earlier filed application requires written description and enablement support for the challenged claims in the earlier filed application. 35 U.S.C. § 120.

2. Appointments Clause

Patent Owner argues that "[t]he AIA as written by Congress violates the Appointments Clause." PO Resp. 52–53.

The Supreme Court resolved this issue in *United States v. Arthrex, Inc.*, 141 S. Ct. 1970 (2021).

3. Alleged Structural Bias

Patent Owner argues that "[t]he Board's handling of this IPR is structurally biased in a way that has violated Acorn's due-process rights" because the Director's delegation of the authority to determine whether to institute and try this case "results in an improper structural bias because the Board has a strong financial incentive to institute trials." PO Resp. 53.

This argument was rejected by the Federal Circuit in *Mobility Workx, LLC v. Unified Patents, LLC*, 15 F.4th 1146 (Fed. Cir. 2021).

4. Stipulation

Patent Owner argues that "[t]he Board's eleventh-hour invitation to the petitioner to revise its stipulation regarding parallel validity challenges in the district court . . . violated *SAS Institute Inc. v. Iancu*, 138 S. Ct. 1348 (2018), due-process, and fundamental notions of fairness." PO Resp. 56. Patent Owner contends that "Acorn invested its limited resources in these IPRs and the related litigation and chose which arguments to make based on the petition and the stipulation therein" but "after Acorn had made those significant investments, the Board allowed the petitioner to alter its case, indeed the Board invited and encouraged such revision." *Id.* at 56 (emphasis omitted).

This argument is unpersuasive. The stipulation did not change the contours of, or "curate," the Petition; instead, in accordance with the precedential case of *Sotera Wireless, Inc. v. Masimo Corp.*, IPR2020-01019,

Paper 12 (December 1, 2020), Petitioner simply stipulated not to bring the same arguments in the District Court.[7]

IV. CONCLUSION

As set forth in the following table, Petitioner has proven that claims 1–6, 8–10, 15, 16 are unpatentable, but has not proven that claims 11, 12, and 14 are unpatentable:

Claims	35 U.S.C. §	Reference	Claims Shown Unpatentable	Claims Not Shown Unpatentable
1–6, 8–12, 14–16	102	Grupp '483	1–6, 8–10, 15, 16	11, 12, 14

V. ORDER

It is:

ORDERED that claims 1–6, 8–10, 15, and 16 of the '395 patent have been shown, by a preponderance of the evidence, to be unpatentable;[8]

[7] *Sotera Wireless* issued and was designated precedential (on December 1, 2020 and December 17, 2020, respectively) after the Petition and Petitioner's Preliminary Reply were filed (on June 29, 2020 and November 30, 2020, respectively). Papers 2, 14.

[8] Should Patent Owner wish to pursue amendment of the challenged claims in a reissue or reexamination proceeding subsequent to the issuance of this decision, we draw Patent Owner's attention to the April 2019 *Notice Regarding Options for Amendments by Patent Owner Through Reissue or Reexamination During a Pending AIA Trial Proceeding*. *See* 84 Fed. Reg. 16,654 (Apr. 22, 2019). If Patent Owner chooses to file a reissue application or a request for reexamination of the challenged patent, we remind Patent Owner of its continuing obligation to notify the Board of any such related matters in updated mandatory notices. *See* 37 C.F.R. § 42.8(a)(3), (b)(2).

FURTHER ORDERED that claims 11, 12, and 14 of the '395 patent have not been shown, by a preponderance of the evidence, to be unpatentable;

FURTHER ORDERED that Patent Owner's Motion to Exclude is dismissed as moot; and

FURTHER ORDERED that because this is a Final Written Decision, the parties to the proceeding seeking judicial review of the decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO. LTD.,
Petitioner,

v.

ACORN SEMI, LLC,
Patent Owner.

IPR2020-01207
Patent 10,090,395 B2

Before BRIAN J. McNAMARA, JOHN R. KENNY, and AARON W. MOORE, *Administrative Patent Judges.*

KENNY, *Administrative Patent Judge*.

ORDER
Granting Request for Rehearing
35 U.S.C. § 42.71

On February 9, 2022, we issued a Final Written Decision that addressed claims 1–6, 8–12, and 14–16 of U.S. Patent No. 10,090,395 B2. Paper 49 ("Decision"). Via email dated February 22, 2022, Patent Owner requested that we modify the Decision because claim 10 had been disclaimed by Patent Owner before we issued our institution decision. *See* Ex. 3001. Patent Owner identified the disclaimer at issue (Ex. 2056) in an updated mandatory notice (Paper 12), but did not identify it in its preliminary response (Paper 11) or pre-institution sur-reply (Paper 15). Our institution decision included claim 10 as part of the proceeding. Paper 21, 2 39. Patent Owner did not seek rehearing of our institution decision on this basis. Patent Owner, however, referred to its disclaimer in its Patent Owner Response. Paper 29, 9.

Patent Owner represents that Petitioner does not oppose correcting the Decision to remove the discussion of claim 10, and Patent Owner does not request the extension of any deadlines as a result of such a correction. Ex. 3001. Patent Owner has not otherwise sought rehearing of our Decision. Under the circumstances, we treat Patent Owner's email as a request for rehearing, which we grant. Thus, we remove the analysis of claim 10 from the Decision as set forth in the order below.

ORDER

It is:

ORDERED that textual changes are made to the Decision as indicated in Appendix A below;

FURTHER ORDERED that the following change is made to page 8 of the Decision, replacing the table of grounds with the following:

Claim(s) Challenged	35 U.S.C. §	Reference
1–6, 8, 9, 11, 12, 14–16	102(b)	Grupp '483[1]

and

FURTHER ORDERED that the following change is made to page 50 of the Decision, replacing the summary table with the following:

Claims	35 U.S.C. §	Reference	Claims Shown Unpatentable	Claims Not Shown Unpatentable
1–6, 8, 9,[2] 11, 12, 14–16	102	Grupp '483	1–6, 8, 9, 15, 16	11, 12, 14

[1] U.S. Patent No. 7,176,483 B2, issued Feb. 13, 2007 (Ex. 1021).
[2] Claim 10 was disclaimed. Ex. 2056.

APPENDIX A

Decision Page(s)	Original Text	Replacement Text
2	Samsung Electronics Co., Ltd. ("Petitioner") filed a Petition, Paper 2 ("Petition" or "Pet."), to institute an *inter partes* review of claims 1–6, 8–12, and 14–16 ("challenged claims") of U.S. Patent No. 10,090,395 B2 (Ex. 1001, "'395 patent"). Acorn Semi, LLC ("Patent Owner") filed a Preliminary Response, Paper 11 ("Prelim. Resp."), contending that the Petition should be denied as to all challenged claims.	Samsung Electronics Co., Ltd. ("Petitioner") filed a Petition, Paper 2 ("Petition" or "Pet."), to institute an *inter partes* review of claims 1–6, 8–12, and 14–16 of U.S. Patent No. 10,090,395 B2 (Ex. 1001, "'395 patent"). Acorn Semi, LLC ("Patent Owner") subsequently disclaimed claim 10 (*see* Ex. 2056, 1) and filed a Preliminary Response, Paper 11 ("Prelim. Resp."), contending that the Petition should be denied as to claims 1–6, 8, 9, 11, 12, and 14–16 ("challenged claims").
2	we determine that Petitioner has shown, by a preponderance of the evidence, that claims 1–6, 8–10, 15, and 16 are unpatentable	we determine that Petitioner has shown, by a preponderance of the evidence, that claims 1–6, 8, 9, 15, and 16 are unpatentable
8	claims 1–6, 8–12, and 14–16	claims 1–6, 8, 9, 11, 12, and 14–16
14, 26, 40	claims 1–6, 8–10, 15, and 16	claims 1–6, 8, 9, 15, and 16
14	Claim 2–6, 8–10, 15, and 16	Claim 2–6, 8, 9, 15, and 16
28	claims 6, 8, 10, 11, and 14–16	claims 6, 8, 11, and 14–16
45	*h. Claims 9 and 10*	*h. Claim 9*

Decision Page(s)	Original Text	Replacement Text
45	Claims 9 and 10 are identical. Ex. 1001, 19:12–17. Both claims recite the electrical junction of claim 8, "wherein said semiconductor oxide comprises an oxide of the region in the semiconductor substrate." *Id.*	Claim 9 recites the electrical junction of claim 8, "wherein said semiconductor oxide comprises an oxide of the region in the semiconductor substrate." Ex. 1001, 19:12–14."
45	Grupp '483 anticipates claims 9 and 10.	Grupp '483 anticipates claim 9.
50	As set forth in the following table, Petitioner has proven that claims 1–6, 8–10, 15, 16 are unpatentable, but has not proven that claims 11, 12, and 14 are unpatentable:	As set forth in the following table, Petitioner has proven that claims 1–6, 8, 9, 15, and 16 are unpatentable, but has not proven that claims 11, 12, and 14 are unpatentable:
50	claims 1–6, 8–10, 15, and 16 of the '395 patent have been shown, by a preponderance of the evidence, to be unpatentable	claims 1–6, 8, 9, 15, and 16 of the '395 patent have been shown, by a preponderance of the evidence, to be unpatentable

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Paper 55
Date: January 12, 2022

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD.,
Petitioner,

v.

ACORN SEMI, LLC,
Patent Owner.

IPR2020-01279
Patent 9,905,691 B2

Before BRIAN J. McNAMARA, JOHN R. KENNY, and AARON W. MOORE, *Administrative Patent Judges.*

McNAMARA, *Administrative Patent Judge*.

JUDGMENT
Final Written Decision
Determining Some Challenged Claims Unpatentable
Denying Patent Owner's Motion to Exclude Testimony of Dr. Goodnick
Dismissing Patent Owner's Motion to Exclude Testimony of Dr. Kuhn
Denying Petitioner's Motion to Exclude Testimony of Dr. Clifton
35 U.S.C. § 318(a)

I. BACKGROUND

On January 13, 2020, we instituted an *inter partes* review of claims 1–4, 6, 8, 10–13, 15–20, 22, and 25–30 of U. S. Patent No. 9,905,691 B2 (Ex. 1101, "the ' 691Patent"). Paper 20 ("Dec. to Inst."). Patent Owner filed a Patent Owner Response (Paper 28, "PO Resp."), Petitioner filed a Petitioner Reply (Paper 37, "Pet. Reply") and Patent Owner filed a Sur-reply (Paper 43, "PO Sur-reply). A transcript of an oral hearing held on October 13, 2001 (Paper 54, "Hr'g. Tr.") has been entered into the record.

We have jurisdiction under 35 U.S.C. § 6. This Final Written Decision is issued pursuant to 35 U.S.C. §318(a). We base our decision on the preponderance of the evidence. 35 U.S.C. § 316(e); 37 C.F.R. § 42.1(d).

Having reviewed the arguments of the parties and the supporting evidence, we conclude that Petitioner has demonstrated by a preponderance of the evidence that claims 1–4 and 13 are unpatentable.

II. THE '691 PATENT

The '691 patent "relates to a process for depinning the Fermi level of a semiconductor at a metal-interface layer-semiconductor junction and to devices that employ such a junction." Ex. 1101, 1:27–29. The '691 patent explains that Schottky's theory concerning the ability of a junction to conduct current in one direction more favorably than in the other direction, i.e., the rectifying behavior of a metal/semiconductor junction (e.g., an aluminum/silicon junction), depends upon a barrier at the surface of the contact between the metal and the semiconductor. *Id.* at 1:33–48. As the barrier height at the metal/semiconductor interface determines the electrical properties of the junction, controlling the barrier height is an important goal. *Id.* at 3:4–10.

The '691 patent further explains that Schottky's theory postulates the height of the barrier, as measured by the potential necessary for an electron to pass from the metal to the semiconductor, is the difference between the work function of the metal (i.e., the energy required to free an electron at the Fermi level (the highest occupied energy state of the metal at T=0)) and the electron affinity of the semiconductor (i.e., the difference between the energy of a free electron and the conduction band of the semiconductor); but experimental results indicate a weaker variation of barrier height with work function than implied by this model. *Id*. at 1:49–2:3.

To explain the discrepancy between the predicted and observed behavior, Bardeen introduced the concept of semiconductor surface states, i.e., energy states within the bandgap between the valence and conduction bands at the edge of the semiconductor crystal that arise from incomplete covalent bonds, impurities, and other effects of termination. *Id.* at 2:4–18, Fig. 1 (showing dangling bonds that may be responsible for surface states that trap electrical charges). Although Bardeen's model assumes that surface states are sufficient to pin the Fermi level in the semiconductor at a point between the valence and conduction bands, such that the barrier height should be independent of the metal's work function, in experiments this condition is observed rarely. *Id.* at 2:19–25.

Further, according to the '691 patent, Tersoff proposed that the Fermi level of a semiconductor is pinned near an effective "gap center" due to metal induced gap states (MIGS), which are energy states in the bandgap of the semiconductor that become populated with metal. *Id.* at 2:35–44. Thus, the wave functions of electrons in the metal do not terminate abruptly at the surface of the metal, but decay in proportion to the distance from the surface, extending inside the semiconductor. *Id.* at 2:44–48.

> To maintain the sum rule on the density of states in the semiconductor, electrons near the surface occupy energy states in the gap derived from the valence band such that the density of states in the valence band is reduced. To maintain charge neutrality, the highest occupied state (which defines the Fermi level of the semiconductor) will then lie at the crossover point from states derived from the valence band to those derived from the conduction band. This crossover occurs at the branch point of the band structure.

Id. at 2:48–56. The '691 patent also notes one further surface effect on diode characteristics is inhomogeneity, i.e., "if factors affecting the barrier height (e.g., density of surface states) vary across the plane of the junction, the resulting properties of the junction are found not to be a linear combination of the properties of the different regions." *Id.* at 2:63–67.

According to the '691 patent, "a classic metal-semiconductor junction is characterized by a Schottky barrier, the properties of which (e.g., barrier height) depend on surface states, MIGS and inhomogeneities." *Id.* at 2:67–3:3. "Before one can tune the barrier height, however, one must depin the Fermi level of the semiconductor." *Id.* at 3:10–12. The '691 patent seeks to depin the Fermi level of the semiconductor while still permitting substantial current flow between the metal and the semiconductor. *Id.* at 3:12–15. The '691 patent describes depinning the Fermi level as follows:

> By depinning the Fermi level, the present inventors mean a condition wherein all, or substantially all, dangling bonds that may otherwise be present at the semiconductor surface have been terminated, and the effect of MIGS has been overcome, or at least reduced, by displacing the semiconductor a sufficient distance from the metal.

Id. at 3:30–35.

The '691 patent achieves this goal using thin interface layers disposed between a metal and a silicon based semiconductor to form a "metal-

interface layer-semiconductor junction" whose thickness varies with a corresponding minimum specific contact resistance depending on the materials used and allows for depinning the Fermi level while permitting current to flow when the junction is appropriately biased. *Id.* at 3:19–30; *see also id.* at 12:59–14:17, 14:29–52, Figs. 6, 8. "Minimum specific contact resistances of less than or equal to approximately 10 Ω-μm^2 or even less than or equal to approximately 1Ω-μm^2 may be achieved for such junctions in accordance with the present invention." *Id.* at 3:36–39. Such low contact resistances are achieved by selecting a metal with a work function near the conduction band of the semiconductor for n-type semiconductors, or a work function near the valence band for p-type semiconductors. *Id.* at 5:19–23.

Figure 8 of the '691 patent is reproduced below.

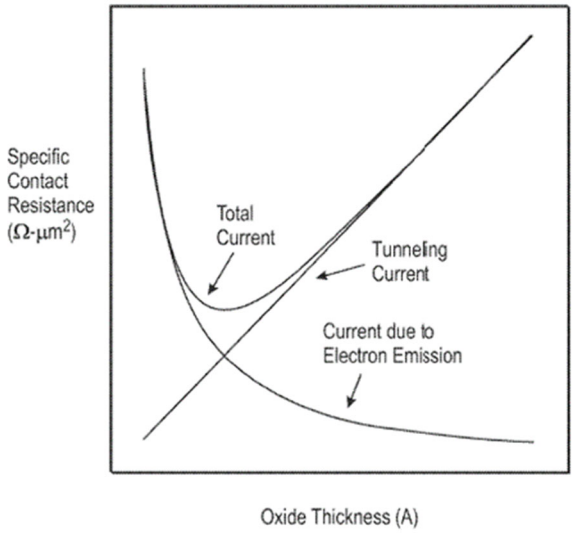


Figure 8 of the '691 patent

Figure 8 of the '691 patent is a graph of interface specific contact resistance versus interface thickness for a structure where the work function of the metal is the same as the electron affinity of the semiconductor, such that the Fermi level of the metal lines up with the conduction band of the

semiconductor. *Id.* at 14:29–35. According the '691 patent, Figure 8 shows that at large thicknesses, the interface layer poses significant resistance to current, but as interface layer thickness decreases, resistance falls due to increased tunneling current. *Id.* at 14:29–38. However, at some point, as the interface layer gets thinner, the effect of MIGS increasingly pulls the Fermi level of the metal down towards the mid-gap of the semiconductor, creating a Schottky barrier and increasing resistance. *Id.* at 14:38–42. Thus, there is an optimum thickness where the resistance is at a minimum and the effect of MIGS has been reduced to depin the metal and lower the Schottky barrier, but the layer is sufficiently thin to allow significant current across the interface layer, such that specific contact resistances of less than or equal to approximately 2500 Ω-m^2, 1000 Ω-m^2, 100 Ω-m^2, 50 Ω-m^2, 10 Ω-m^2, or less than 1 Ω-m^2 can be achieved. *Id.* at 14:45–52.

In one embodiment, the interface layer may be a monolayer or several monolayers of passivating material (e.g., a nitride, oxide, oxynitride, arsenide, hydride and/or fluoride) and may include a separation oxide layer, the specific contact resistance of the electrical device is less than 10 Ω-μm^2. *Id.* at 3:40–53; *see also* 10:43–54. In another embodiment, the interface layer is made up of a passivation layer fabricated by exposing the semiconductor to nitrogenous material (e.g., ammonia (NH3), nitrogen (N2) or unbound gaseous nitrogen (N) generated from a plasma process) and while heating the semiconductor in a vacuum chamber. *Id.* at 3:44–61. Another embodiment uses an interface layer of passivating material disposed between the surface of a semiconductor and a conductor in which the interface is of sufficient thickness to reduce the effect of MIGs in the semiconductor and passivates the semiconductor but, because the thickness of the interface layer is chosen to provide minimum, or near minimum,

specific contact resistance for the junction, significant current may flow between the conductor and the semiconductor. *Id.* at 3:62–4:8. In other embodiments the interface layer is configured to allow a Fermi level of the conductor to (i) align with a conduction band of the semiconductor, (ii) align with a valence band of the semiconductor, and (iii) be independent of the Fermi level of the semiconductor, allowing current to flow between the conductor and the semiconductor when the junction is biased because the thickness of the interface layer corresponds to a minimum or near minimum contact resistance for the junction. *Id.* at 4:8–18. Specific contact resistances of less than or equal to approximately 2500 Ω-m^2, 1000 Ω-m^2, 100 Ω-m^2, 50 Ω-m^2, 10 Ω-m^2, or less than 1 Ω-m^2 can be achieved. *Id.* at 4:19–22, 14:45–52.

III. ILLUSTRATIVE CLAIM(S)

Independent claim 1, reproduced below to include the subject matter of a certificate of correction issued on May 15, 2018 (Ex. 1101, 21), and including claim element designations (i) through (vii) used in the Petition, is representative of the subject matter of the ’691 patent:

> 1. (i) A structure, comprising
>
> (ii) a semiconductor region in a substrate,
>
> (iii) a metal electrical contact to said semiconductor region,
>
> (iv) a metal oxide layer,
>
> (v) a passivating dielectric tunnel barrier layer between said semiconductor region and said metal electrical contact,
>
> (vi) said semiconductor region being electrically connected to said metal electrical contact through said passivating dielectric tunnel barrier layer and said metal oxide layer,
>
> (vii) wherein said passivating dielectric tunnel barrier layer comprises a semiconductor oxide.

IV. GROUNDS OF INSTITUTION

Inter partes review was instituted on all the grounds asserted in the Petition as follows:

Claim(s) Challenged	35 U.S.C. §	Reference(s)/Basis
1–3, 13	102(b)	Goodnick[1]
4	103(a)	Goodnick, Jammy[2]
1, 3, 6, 10–13, 15, 16, 19, 20, 22	103(a)	Goodnick, Taubenblatt 1982[3]
8, 17	103(a)	Goodnick, Jammy, Taubenblatt 1982
18, 25–30[4]	103(a)	Goodnick, Jammy, Taubenblatt 1982, Chang[5]

V. CLAIM CONSTRUCTION

In the Decision to Institute, we construed the terms "specific contact resistivity" and "specific contact resistance" to be interchangeable. Dec. to Inst. 12. Neither party disagrees with this construction, and we apply the same construction for purposes of the Decision.

[1] S.M. Goodnick et al., *Effects of a thin SiO2 layer on the formation of metal-silicon contacts*, 18 J. VAC. SCI. & TECH. 949 (Apr. 1981). (Ex. 1116).
[2] U.S. Patent No. 6,724,088. (Ex. 1115)
[3] M.A. Taubenblatt and C.R. Helms, *Silicide and Schottky barrier formation in the Ti-Si and the Ti-SiOx-Si systems*, 58 J. APPLIED PHYS. 6308 (1982). (Ex. 1117).
[4] Claim 30 has been disclaimed and is no longer a subject of this proceeding.
[5] C.Y. Chang et al., *Specific contact resistance of metal-semiconductor barriers*, 15 SOLID STATE ELECS. 541 (1971)

VI. ANALYSIS OF PRIOR ART CHALLENGES

A. Introduction

"In an [inter partes review], the petitioner has the burden from the onset to show with particularity why the patent it challenges is unpatentable." *Harmonic Inc. v. Avid Tech., Inc*., 815 F.3d 1356, 1363 (Fed. Cir. 2016) (citing 35 U.S.C. § 312(a)(3) (requiring inter partes review petitions to identify "with particularity . . . the evidence that supports the grounds for the challenge to each claim")). This burden of persuasion never shifts to Patent Owner. *See Dynamic Drinkware, LLC v. Nat'l Graphics, Inc.*, 800 F.3d 1375, 1378 (Fed. Cir. 2015) (discussing the burden of proof in inter partes review).

Anticipation is a question of fact, as is the question of what a prior art reference teaches. *In re NTP, Inc*., 654 F.3d 1279, 1297 (Fed. Cir. 2011). "A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros. Inc., v. Union Oil Co*., 814 F.2d 628, 631 (Fed. Cir. 1987); *see also Finisar Corp. v. DirecTV Group, Inc*., 523 F.3d 1323, 1334 (Fed. Cir. 2008) (to anticipate a patent claim under 35 U.S.C. § 102, "a single prior art reference must expressly or inherently disclose each claim limitation"). Moreover, "[b]ecause the hallmark of anticipation is prior invention, the prior art reference—in order to anticipate under 35 U.S.C. § 102—must not only disclose all elements of the claim within the four corners of the document, but must also disclose those elements 'arranged as in the claim.'" *Net MoneyIN, Inc. v. VeriSign, Inc*., 545 F.3d 1359, 1369 (Fed. Cir. 2008) (quoting *Connell v. Sears, Roebuck & Co.*, 722 F.2d 1542, 1548 (Fed. Cir. 1983)).

Whether a reference anticipates is assessed from the perspective of an ordinarily skilled artisan. *See Dayco Prods., Inc. v. Total Containment, Inc.*, 329 F.3d 1358, 1368 (Fed. Cir. 2003) ("[T]he dispositive question regarding anticipation [i]s whether one skilled in the art would reasonably understand or infer from the [prior art reference's] teaching that every claim element was disclosed in that single reference." (quoting *In re Baxter Travenol Labs.*, 952 F.2d 388, 390 (Fed. Cir. 1991))).

Additionally, under the principles of inherency, if the prior art necessarily functions in accordance with, or includes, the claimed limitations, it anticipates. *MEHL/Biophile Int'l Corp. v. Milgraum*, 192 F.3d 1362, 1365 (Fed. Cir. 1999) (citation omitted); *In re Cruciferous Sprout Litig.*, 301 F.3d 1343, 1349–50 (Fed. Cir. 2002).

As set forth in 35 U.S.C. § 103(a),

> [a] patent may not be obtained . . . if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.

The question of obviousness is resolved on the basis of underlying factual determinations including: (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of ordinary skill in the art; and (4) objective evidence of nonobviousness. *Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966). Additionally, the obviousness inquiry typically requires an analysis of "whether there was an apparent reason to combine the known elements in the fashion claimed by the patent at issue." *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 418 (2007) (citing *In re Kahn*, 441 F.3d 977, 988 (Fed. Cir. 2006) (requiring "articulated reasoning with some rational underpinning to support the legal conclusion of

obviousness")); *see In re Warsaw Orthopedic, Inc.*, 832 F.3d 1327, 1333 (Fed. Cir. 2016) (citing *DyStar Textilfarben GmbH & Co. Deutschland KG v. C. H. Patrick Co.*, 464 F.3d 1356, 1360 (Fed. Cir. 2006)).

An obviousness analysis "need not seek out precise teachings directed to the specific subject matter of the challenged claim, for a court can take account of the inferences and creative steps that a person of ordinary skill in the art would employ." *KSR*, 550 U.S. at 418; *accord In re Translogic Tech., Inc.*, 504 F.3d 1249, 1259 (Fed. Cir. 2007). Petitioner cannot satisfy its burden of proving obviousness by employing "mere conclusory statements." *In re Magnum Oil Tools Int'l, Ltd.*, 829 F.3d 1364, 1380 (Fed. Cir. 2016). Instead, Petitioner must articulate a reason why a person of ordinary skill in the art would have combined the prior art references. *In re NuVasive*, 842 F.3d 1376, 1382 (Fed. Cir. 2016).

A reason to combine or modify the prior art may be found explicitly or implicitly in market forces; design incentives; the "interrelated teachings of multiple patents"; "any need or problem known in the field of endeavor at the time of invention and addressed by the patent"; and the background knowledge, creativity, and common sense of the person of ordinary skill. *Perfect Web Techs., Inc. v. InfoUSA, Inc*., 587 F.3d 1324, 1328–29 (Fed. Cir. 2009) (quoting *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 418–21 (2007)).

Before determining whether a claim is obvious in light of the prior art, we consider any relevant evidence of secondary considerations of non-obviousness. *See Graham*, 383 U.S. at 17. Notwithstanding what the teachings of the prior art would have suggested to one of ordinary skill in the art at the time of the invention, the totality of the evidence submitted, including objective evidence of non-obviousness, may lead to a conclusion

that the challenged claims would not have been obvious to one of ordinary skill. *In re Piasecki*, 745 F.2d 1468, 1471–72 (Fed. Cir. 1984).

We analyze the asserted grounds of unpatentability in accordance with these principles to determine whether Petitioner has met its burden to establish a reasonable likelihood of success at trial.

B. Claims 1–3 as anticipated by Goodnick (Petitioner's Ground 1)

Petitioner contends that Goodnick discloses each and every element of claims 1–3 and 13. Pet. 21–26.

1. Goodnick (Ex. 1116)

Goodnick concerns experiments in which "[t]he focus of the present investigation has been to observe the influence of thin SiO2 layers on the chemical formation of metal-silicon contacts." Ex. 1116, 1. According to Goodnick, a thick interfacial oxide at a metal-silicon interface suppresses current, thereby reducing rectifying characteristics, but a thin oxide layer sustains considerable current via tunneling and reduces the density of interface states by satisfying dangling bonds. *Id.* Goodnick discloses that:

> [a]s a result, the Fermi level at the surface may become unpinned and the barrier height is more directly determined by the metal work function. In addition, a thin interfacial layer may act as a barrier to the chemical reaction and interdiffusion that characterizes the intimate metal silicon contact. Thus, the presence of a thin oxide at the interface acts as a passivating influence, both from an electronic and a chemical standpoint.

Id.

Goodnick discloses experiments with aluminum, platinum, and gold in which thin SiO_2 oxide layers were grown in dry oxygen at 700 degrees Celcius in an open tube furnace to approximately 30Å. *Id.* at 1. The 30Å thermally grown SiO_2 appeared as a complete barrier to the formation of

platinum silicide and less of a barrier to the Au-Si reaction, where "widespread dissolution of the SiO_2 layer and reaction between the Au and Si appeared to occur." *Id.* at 5. "Al partially reduces the thin SiO2 layer to form Al_2O_3 and free Si. This reaction appeared to be self-limiting, with SiO_2 still present at the interface, even after heating at 400°C." *Id.* Goodnick concludes:

> a thermally grown SiO2 layer appears effective in preventing or retarding the widespread interdiffusion of elemental Si. However, chemically etched surfaces react readily with the metal overlayer even though a thin native oxide grows prior to deposition. The different chemical nature of room temperature air grown oxides of Si is suggested as an explanation of these results.

Id.

2. Claim 1

a) Preamble 1(i) and claim limitation 1 (ii)

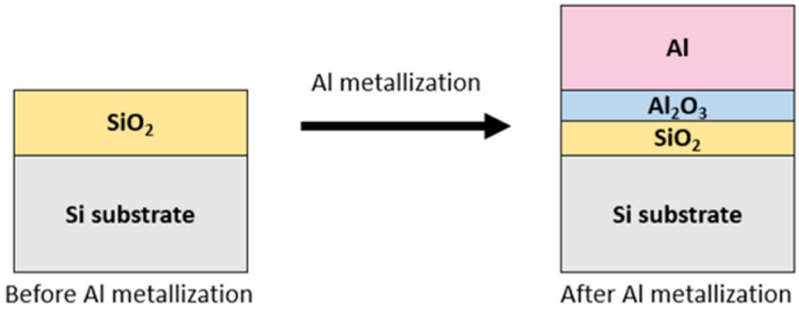
Petitioner asserts that the preamble is not limiting, but cites Goodnick as disclosing an Al-Al_2O3-SiO_2-Si contact structure. Pet. 22 (citing Ex. 1116 1–2, 5; Ex. 1119, Declaration of Dr. E. Fred Schubert ("Schubert Decl.") ¶ 105).

As to claim limitation 1(ii), "a semiconductor region in a substrate," Petitioner cites Goodnick's silicon substrate doped with phosphorous (an n-type dopant) is an example of a semiconductor. *Id.* (citing Ex. 1116, 1; Ex. 1119, Schubert Decl. ¶ 106). Patent Owner does not present any counterarguments to Petitioner's contentions concerning claim limitations 1(i) and 1(ii).

b) Claim limitations 1(iii), 1(iv), and 1(v)

Petitioner identifies claim limitation 1(iii) as reciting "a metal electrical contact to said semiconductor region." *Id.* Petitioner cites

Goodnick's disclosure of an aluminum metal electrical contact formed by evaporating aluminum onto a 30 Å layer of SiO_2 on a cleaned silicon substrate as disclosing this limitation. *Id.* (citing Ex. 1112, 1; Ex. 1119, Schubert Decl. ¶ 107). As to claim limitation 1(iv), "a metal oxide layer," Petitioner cites Goodnick's disclosure of an Al_2O_3 layer. *Id.* (citing Ex. 1116, 5; Ex. 1119, Schubert Decl. ¶ 108). Noting that Goodnick discloses an apparent self-limiting reaction that results in both SiO_2 and Al_2O_3 existing simultaneously at the interface, Petitioner proposes the schematic depiction of the metallization process and the resulting Al-Al_2O_3-SiO_2-Si contact shown below.



Petitioner's Depiction of Goodnick's Metallization Process

Id. at 18 (citing Ex. 1116, 1–2, 5; Ex. 1119 Schubert Decl. ¶¶ 79–85). As illustrated above, Petitioner contends that, after metallization, the contact has a distinct metal contact layer of Al and a metal oxide layer, Al_2O_3. Petitioner's depiction is illustrative and is not reproduced from Goodnick.

Petitioner identifies claim limitation 1(v), as reciting "a passivating dielectric tunnel barrier layer between said semiconductor region and said metal electrical contact." *Id.* at 23. Petitioner identifies the SiO_2 (silicon dioxide) layer as the claimed passivating dielectric tunnel barrier. *Id.* Petitioner notes Goodnick discloses that when thermally evaporating the aluminum metal contact onto the SiO_2 layer grown on the silicon substrate,

the aluminum partially reduces SiO_2 to produce Al_2O_3 and some of the SiO_2 layer grown on the silicon surface remained. *Id.* (citing Ex. 1116, 5; Ex. 1119, Schubert Decl. ¶109). According to Petitioner, Goodnick discloses that a layer of SiO_2 grown on the substrate lies between the silicon substrate and the aluminum and is a passivating layer from an electrical and chemical standpoint. *Id.* (citing Ex. 1116, 1; Ex. 1119, Schubert Decl. ¶ 110). Petitioner further asserts that the remaining thin SiO_2 layer grown on the surface of the substrate is a dielectric tunnel barrier. *Id.* at 23–24 (citing Ex. 1105, 7:60–61; Ex. 1101, 1:8–21; Ex. 1116, 1; Ex. 1119, Schubert Decl. ¶ 111).

Patent Owner states that "[a]ll challenges in the petition utilize Goodnick as the primary reference and are based on Goodnick disclosing distinct stratified layers of different material, including a layer of AL_2O_3, as shown in various petitioner-created diagrams in the petition." PO Resp. 52. (citing Pet. 18 and reproducing a portion of Petitioner's metallization diagram shown above).[6] *Id*. Patent Owner argues that, notwithstanding Petitioner's diagrams that purport to illustrate Goodnick teaching clean stratification of distinct layers, Goodnick includes no such diagrams, only uses the term "layer" twice, and does not support the Petition's assertions. *Id.* (citing Ex. 2043, Declaration of Dr. Stephen Goodnick ("Goodnick Decl."); Ex. 2080, Second Declaration of Dr. Stephen M. Goodnick ("2nd Goodnick Decl.")).

[6] Patent Owner also references its Preliminary Response, which notes that in district court litigation the parties agreed that claim limitation 1(iii) and 1(iv) "require two distinct layers: (1) a passivating dielectric tunnel barrier layer (comprising semiconductor oxide) and (2) a metal oxide layer." *Id.*, Prelim. Resp. 38–39.

Dr. Goodnick, who authored the Goodnick reference, states that Petitioner and Dr. Schubert have "misinterpreted key aspects of my paper." Ex. 2043, Goodnick Decl. ¶ 5. Noting the conventional understanding at the time of his paper was that imperfections in the surface layer, i.e. "dangling bonds," caused the Fermi level to be pinned, Dr. Goodnick states that his reference to the Fermi level becoming unpinned "refer[s] only to the fact that dangling bonds in the silicon are passivated by the oxide layer." *Id.* ¶ 43. Dr. Goodnick also states that, at the time of his paper, the phenomenon of MIGS was poorly understood and "the interaction of pinning due to MIGS and pinning due to dangling surface bonds had not been explored." *Id.* ¶ 44. According to Dr. Goodnick, the inventors "realized that those two pinning mechanisms can be jointly addressed leading to better results . . . they were able to discover that there is an optimum thickness at which the beneficial reduction of pinning by MIGS suppression is negated by the adverse increase in tunneling resistance as the interfacial layer is made thicker." *Id.* ¶ 45 (referring to Figure8 of the '691 patent).

The specific issue before us is what one of ordinary skill in the art would have understood from the Goodnick reference. Dr. Schubert contends that a person of ordinary skill would have understood Goodnick to disclose the claimed layered structure. *See* Ex. 1119, Schubert Decl. ¶¶ 79–85 (at ¶ 80 quoting Goodnick's description of Figure 8(b) that "[i]n contrast to the air exposed sample, an Al_2O_3 layer exists at the Al-SiO_2-Si interface"). Dr. Goodnick states that a person of ordinary skill at the time would not have understood his paper to mean there is a layer of Al_2O_3 on top of a layer of SiO2, but only that Al_2O_3 and SiO_2 were found together in the interface

region between the aluminum and the semiconductor. *See* Ex. 2043 ¶¶ 32–40; Ex. 2080, 2nd Goodnick Decl. ¶¶ 8–9.

Figure 8(a) of Goodnick shows "[p]eak to peak Auger sputter profile on room temperature oxidized Si, unheated" and Figure 8(b) of Goodnick shows "[p]eak to peak Auger profile of Al on 30 Å of SiO_2, unheated." Ex. 1116, 5. Responding to Petitioner's assertions concerning the case where 30Å of SiO_2 was first placed on the silicon before depositing the aluminum, Dr. Goodnick refers to Figure 8(b) of his paper, on which the X-axis is sputter time. Ex. 2043, Goodnick Decl. ¶¶ 32–34; Ex. 2080, 2nd Goodnick Decl. ¶ 8. Dr. Goodnick states that, in the period between 0 and 5 minutes, the high levels of Al_2O_3 represent its presence on the top surface of the aluminum, the high level of aluminum between 10 minutes and 30 minutes corresponds to the aluminum deposition, the high level of silicon after 50 minutes corresponds to the silicon substrate, and the high levels of aluminum and silicon between 30 and 50 minutes is the aluminum-silicon interface. Ex. 2043, Goodnick Decl. ¶ 33. According to Dr. Goodnick, Figure 8(b) shows that Al_2O_3 and SiO_2 were present at the aluminum silicon interface, but "it cannot be determined where Al_2O_3 is present with respect to SiO_2." *Id.* at 34. Dr. Goodnick asserts that the presence of a peak in the Al_2O_3 curve at about 40 minutes and the "O" curve (representing SiO_2) between 35 and 40 minutes and the fact that both curves have the same general shape "means that both compounds were found in the same relative quantities in the interface region." *Id.* According to Dr. Goodnick, "[a] POSITA understanding this data would not conclude that there is a layer of Al_2O_3 on top of a layer of SiO_2 as Samsung claims . . . only that both Al_2O_3 and SiO_2 were found together in the interface region between the aluminum and the silicon." *Id.*

Nevertheless, comparing Figures 8a and 8b, the Goodnick reference expressly states:

> Figure 8(a) shows the peak-to-peak profile of an unheated sample with an air grown oxide. It appears that Si has diffused into the Al and collected at the Al_2O_3-Al interface at the surface. No buildup of Al_2O_3 is seen at the Al-Si interface. Figure 8(b) is a profile of an unheated sample with 30Å SiO_2 at the interface. **In contrast to the air exposed sample, an Al_2O_3 layer exists at the Al-SiO_2-Si interface**. This is suggestive of the reduction reaction seen previously, with the presence of SiO_2 necessary for formation of Al_2O_3. Heat treatment of samples resulted in little change in the profiles with the exception of greater concentration of Si at the surface of the unoxidized samples.

Ex. 1116, 5 (emphasis added).

The Goodnick reference further states that, even at elevated temperatures, the reaction is self-limiting "probably [as] a result of the diffusion barrier formed by the Al2O3 layer to the transport of Al to the SiO_2 layer." Ex. 1116, 5 (emphasis added). Dr. Goodnick now states that "[t]his statement was a speculation based on the fact that both SiO_2 and Al_2O_3 were still present at the interface, whereas thermodynamically it was expected that Al would completely reduce SiO_2 to Al_2O_3 and free Si." Ex. 2043 ¶ 39.

Patent Owner emphasizes that Goodnick's two references to an Al_2O_3 layer do not state that the Al_2O_3 layer is distinct from SiO_2 and were not meant to suggest the type of stratified distinct layers in the IPR petitions. PO Resp. 53 (citing Ex. 2080, 2nd Goodnick Decl. ¶¶ 8–9).

Patent Owner contends that the Auger profile data in Figure 8(b) does not support Petitioner's stratified layer arguments. Patent Owner states that, in addition to the Al_2O_3 hump corresponding to 35–55 minutes sputter time indicating an Al_2O_3 layer, the data also shows oxygen of unknown origin

rising earlier and peaking to the left of the Al_2O_3 line, as well as aluminum and silicon in the same vicinity. Thus, Patent Owner argues that "according to the Auger profile data, the 'Al_2O_3 layer' is not a stratified distinct layer of Al_2O_3 as the petition asserts." PO Resp. 54 (citing Ex. 1116, 953).

Patent Owner does not explain sufficiently why the data it cites on the Auger profile does not support Petitioner's contentions. The Goodnick reference uses the term "layer" over 40 times and in no case does Goodnick ascribe a meaning to "layer" that is different from one layer being distinct from another.

Patent Owner next argues that XPS measurements reported in Goodnick indicate that both SiO_2 and Al_2O_3 exist simultaneously at the interface, but reveal nothing about the spatial distribution of the Al_2O_3 and SiO_2. PO Resp. 54–55 (citing Ex. 2080, 2nd Goodnick Decl. ¶ 10). Patent Owner also argues that the Goodnick reference speculated an Al_2O_3 diffusion barrier is the probable reason the $4\ Al + 3\ SiO_2 \rightarrow 2Al_2O_3 + 3Si$ reaction is self-limiting, but that speculation is an untested hypothesis insufficient to support Petitioner's contentions. *Id.* at 55 (citing Ex. 2080, 2nd Goodnick Decl ¶¶ 11–13).

Goodnick is entitled "Effects of a thin SiO_2 layer on the formation of metal-silicon contacts" and states "[t]"he reactions that occur between different metals and silicon wafers with a thin oxide layer have been investigated." Ex. 1116. Abstract. Goodnick further states "a thin interfacial layer may act as a barrier to the chemical reaction and interdiffusion that characterizes the intimate metal silicon contact. Thus, the presence of a thin oxide at the interface act as a passivating influence both from an electronic and a chemical standpoint." Ex. 1116, 949.

Taken in context, we agree that a person of ordinary skill would have understood Goodnick to refer to Al_2O_3 as a distinct layer. Referring to Fig. 8(a), Goodnick states that in an unheated sample with an air grown oxide "[i]t appears that Si has diffused into the Al and collected at the Al_2O_3-Al interface at the surface. No buildup of Al_2O_3 is seen at the Al-Si interface." Ex. 1116, 953. Noting that Fig. 8(b) is a profile of an unheated sample with 30Å of SiO_2 at the interface, Goodnick states "[i]n contrast to the air exposed sample, an Al_2O_3 layer exists at the Al-SiO_2-Si interface." *Id.*

Petitioner notes that, on cross examination, Dr. Goodnick acknowledged (i) that the Al metal layer would diffuse into the SiO_2 interface layer and reduce the portion of the SiO_2 layer nearest the Al layer to Al_2O_3, (ii) that once the Al_2O_3 layer forms, it would be difficult for aluminum atoms to diffuse through the Al_2O_3 layer to continue reaction with the SiO_2 layer, and (iii) because the reaction is self-limiting, a portion of the original SiO_2 layer would remain once the reaction forming the Al_2O_3 layer stopped. Pet. Reply 5–6 (citing Ex. 1168, Goodnick Tr. 55:5–25, 57:19–58:8, 59:24–60:7). In view of, *inter alia*, Dr. Goodnick's cross examination testimony, we are persuaded by Dr. Schubert's testimony that a person of ordinary skill would have understood that distinct layers of Al_2O_3 and SiO_2 are formed. Ex. 1173 ¶¶ 85–98.

As to Patent Owner's arguments concerning speculation (PO Sur-reply), we note that our inquiry is what Goodnick would have disclosed to a person of ordinary skill. Goodnick's comments, even if they are now deemed by Dr. Goodnick to be speculative, are consistent with the physical evidence and even Dr. Goodnick considers the process is to this day the best and only understanding of the structure formed. *See* Pet. Reply 7 (citing Ex.

1168, Goodnick Tr. 129:19–130:7; Ex. 1173, Schubert Decl. 2 ¶ 99). Moreover, no one has argued that it was beyond the skill of a person of ordinary skill in the art to create the described layer of Al_2O_3.

c) Claim limitations 1(vi) and 1 (vii)

Petitioner identifies claim limitation 1(vi) as reciting "said semiconductor region being electrically connected to said metal electrical contact through said passivating dielectric tunnel barrier layer and said metal oxide layer." Pet. 24. Petitioner cites Goodnick as investigating "the influence of thin SiO2 layers on the chemical formation of metal-silicon contacts." *Id.* (citing Ex. 1116, 1). Petitioner also cites Goodnick as describing its interfacial oxide layers as thin and stating "an oxide layer that is sufficiently thin may sustain considerable current via tunneling." *Id.* at 24–25 (citing Ex. 1116, 1; Ex. 1119, Schubert Decl. ¶ 112).

Petitioner identifies claim limitation 1(vii), as reciting "wherein said passivating dielectric tunnel barrier layer comprises a semiconductor oxide." *Id.* at 25. Referencing its earlier discussion of Goodnick, Petitioner cites that reference as describing a SiO_2 passivating dielectric tunnel barrier layer. *Id.* at 25 (citing Ex. 1116, 1–2, 5).

Other than asserting that Goodnick fails to disclose distinct layers, as discussed in detail above, Patent Owner does not respond to Petitioner's contentions concerning claim limitations 1(vi) and 1(vii).

In consideration of the above, we find that Petitioner has demonstrated by a preponderance of the evidence that Goodnick discloses all of the limitations of claim 1.

3. Claims 2–3 and 13

Claim 2 depends from claim 1 and recites the additional limitation that "the semiconductor oxide comprises an oxide of the semiconductor

region." Petitioner cites Goodnick as disclosing thermally growing a layer of SiO_2 on a silicon substrate, that some of the SiO_2 layer is reduced by aluminum to produce Al_2O_3, and that a layer of SiO_2 remaining on the silicon substrate is an oxide of the silicon substrate. Pet. 25.

Claim 3 depends from claim 1 and recites the additional limitation that "the semiconductor oxide of the dielectric tunnel barrier has a thickness of approximately 0.1 nm to 5 nm." Petitioner cites Goodnick as disclosing thermally growing a 30Å (3 nm) thick layer of SiO_2 on a silicon substrate that is reduced partially by aluminum to produce Al_2O_3 with a remaining layer of SiO_2, whose minimum thickness, i.e. the thickness of a monolayer (a layer one molecule thick), is 2 Å (0.2 nm). Pet. 26 (citing Ex. 1116, 1–2; Ex. 1119, Schubert Decl. ¶ 119).

Claim 13 depends from claim 3 and recites the additional limitation that "the semiconductor oxide comprises an oxide of silicon." Noting that SiO_2 is an oxide of silicon, Petitioner cites Goodnick as disclosing this feature. Pet. 27 (citing Ex. 1116, 5).

Patent Owner does not present any counterarguments concerning the additional limitations recited in claims 2–3 and 13. In consideration of the above, we find that Petitioner has demonstrated by a preponderance of the evidence that Goodnick discloses all of the limitations of claims 2–3 and 13.

C. Claim 4 as obvious over Goodnick in view of Jammy (Petitioner's Ground 2)

1. Jammy (Ex. 1115)

Jammy discloses "improved contact between conductive studs and shallow diffusion regions by incorporation of a quantum conductive barrier layer at the interface between the conductive stud and shallow diffusion

region." Ex. 1115, 3:18–21. An annotated version of Figure 1 of Jammy is shown below.

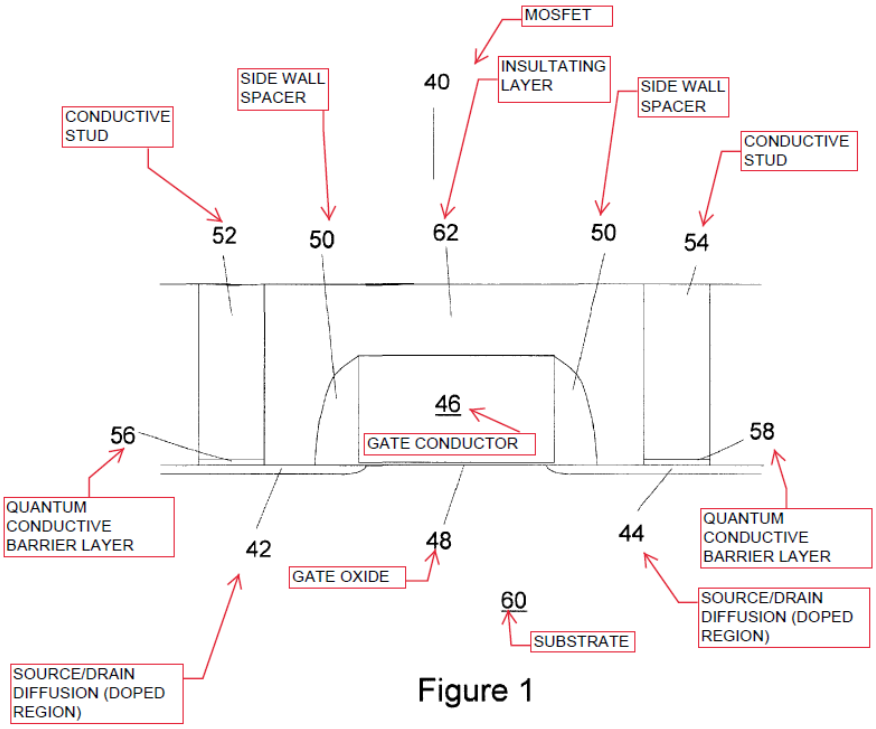


Figure 1

Ex. 1115, Fig. 1. Annotated Figure 1 shows MOSFET 40 in which shallow source/drain diffusions, i.e., doped regions 42, 44, formed in substrate 60 contact conductive studs 52, 54 through quantum conductive barriers 56, 58. *Id*. at 4:9–18. Jammy's quantum conductive layers are thin films of less than 50Å (more preferably about 5–30 Å, most preferably about 5–15 Å) of materials that in their bulk properties would be considered dielectrics, but in thin layers become electrically conductive, such that resulting layers preferably have a film resistance of less than about 1 K-ohm-μm^2, more preferably less than about 100 ohm-μm^2. *Id.* at 3:23–40. Jammy's thin layers also prevent or slow diffusion of chemical species from one side of the layer to the other.

1. Claim 4

Claim 4 depends from claim 3 and recites the additional limitation that "the semiconductor region comprises an n-typed doped source or drain of a transistor." Acknowledging that Goodnick "does not expressly disclose that its n-doped silicon semiconductor region 'comprises an n-type source or drain of a transistor,'" Petitioner cites Jammy as disclosing this feature. Pet. 27. According to Petitioner, a person of ordinary skill would have combined the teachings of Goodnick and Jammy because Goodnick describes contact metallization processes for semiconductor devices and Jammy describes a semiconductor device. *Id.* at 28.

Patent Owner asserts that Petitioner's challenge to claim 4 based on the combined teachings of Goodnick and Jammy fails because it is premised on Goodnick teaching a stratified layer of Al_2O_3 distinct from SiO_2. PO Resp. 60. As discussed above, we find that a person of ordinary skill would have understood Goodnick to disclose this feature. *See* Section VI.B. In consideration of the above, we find that Petitioner has demonstrated by a preponderance of the evidence that a person of ordinary skill would have had reason to combine the teachings of Goodnick and Jammy and that the combined teachings of Goodnick and Jammy would have suggested the limitations of claim 4 to a person of ordinary skill in the art.

As Patent Owner's contentions concerning objective considerations of non-obviousness apply to all the claims challenged on that basis, we address objective considerations further in Section VI.G.

D. Claims 1, 3, 6, 10–13, 15, 16, 19, 20, 22 as obvious over Goodnick and Taubenblatt (Petitioner's Ground 3)

1. Taubenblatt

Noting the importance of silicides as Schottky barriers, ohmic contacts, and low resistivity interconnects in integrated circuits, Taubenblatt states that "[m]any silicides are commonly formed by the deposition of a metal layer on silicon via e-beam evaporation, chemical vapor deposition, or sputtering, and the reaction of the metal layer with the underlying silicon at 400-600 °C." Ex. 1115, 1. Taubenblatt concerns experiments "to characterize silicide formation for the Ti-Si system under ultrahigh vacuum (UHV) conditions with the controlled addition of surface oxides." *Id.* Taubenblatt's "results show that the presence of SiO_2 at the Si surface, prior to Ti deposition, has a significant effect on the reaction of Ti and Si and that the thickness of the SiO_2 layer is especially important in determining the reaction end products." Ex. 1117, 8. According to Taubenblatt:

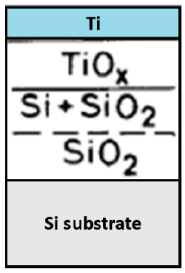
> in the manufacture of circuit elements employing titanium disilicide, Ti will react through a thin silicon dioxide layer with the SiO2 remaining at the surface. But in the reaction of Ti with a thicker SiO2 layer, Ti oxide forms, which can act as a diffusion barrier to prevent further reduction of the oxide by unreacted Ti metal or in the formation of silicide.

Id.

2. Motivation to combine the teachings of Goodnick and Taubenblatt

Petitioner argues that Goodnick discloses an interface layer that includes a metal oxide layer (aluminum oxide (Al_2O_3)), but acknowledges that Goodnick does not expressly describe a metal oxide layer that comprises an oxide of titanium, as recited explicitly in claims 6, 10–12, and 15–16. Pet. 29. Petitioner states that, because Taubenblatt teaches that

(i) depositing titanium on a layer of SiO_2 thicker than 20 Å (2nm) and (ii) annealing at temperatures between 700ºC–900ºC forms a TiO_x–SiO_2 interface layer, a person of ordinary skill would have understood that by depositing titanium on Goodnick's 30 Å (3 nm) thick layer of thermally grown SiO_2, "all it would have taken to form a TiO_x–SiO_2 interface layer is annealing at 700ºC–900ºC, as described in Taubenblatt 1982." *Id.* at 31 (citing Ex. 1117, 7–8; Ex. 1119, Schubert Decl. ¶ 137). Petitioner contends that the combined teachings of Goodnick and Taubenblatt would have resulted in the structure shown below.



Pet. 31–32 (citing Ex. 1115, 1–2; Ex. 11117, 7–8; Ex. 1119, Schubert Decl. ¶ 138). The structure Petitioner postulates a person of ordinary skill would have known includes a SiO_2 layer on top of a silicon substrate, a Si+SiO_2 layer over the SiO_2 layer, a TiO_x layer on top of the Si+SiO_2 layer and a Ti layer over the TiO_x layer. *Id.* at 32; *see also* Ex. 1117, Fig. 11, 8 (discussing Fig. 11, row 3, concerning the behavior of thin layers of SiO_2).

According to Petitioner, an ordinarily skilled artisan would have had reason to provide Goodnick with an interface layer that includes both titanium oxide and silicon dioxide "because that interface layer would have been expected to reduce the specific contact resistivity of that junction." *Id.* at 32 (citing, e.g., Ex. 1119, Schubert Decl. ¶ 39). Petitioner argues it was known that a SiO_2 interface layer grown on silicon would passivate the surface of the silicon and "[t]hat passivation would have reduced the barrier

height of a titanium to n-type silicon junction, such as the junction between Taubenblatt's titanium and Goodnick's n-type source drain/drain silicon substrate." *Id.* at 33 (citing Ex. 1115, 31; Ex. 1116, 1–2; Ex. 1119, Schubert Decl. ¶ 141). Petitioner further states that, for a junction between titanium and n-type silicon with a SiO_2 interface layer, the SiO_2 interface layer reduces the barrier height more than 0.1 eV" and that "reducing the barrier height of a junction reduces its specific contact resistivity." *Id.* (citing Ex. 1119, Schubert Decl. ¶ 141; Ex. 1118 (Chang)[7], 5–6).

In summarizing what would have been known to one of ordinary skill at the relevant time, Petitioner's expert, Dr. Schubert, cites another Taubenblatt reference, i.e., Taubenblatt 1984[8]. Petitioner notes that Taubenblatt 1984 references teachings in Turner and Rhoderick[9] as disclosing that an interfacial oxide reduces the pinning ability of the interface states in silicon, so that the barrier behaves more like an ideal Schottky barrier. Ex. 1119, Schubert Decl. ¶ 54 (citing Ex. 1123, 3). Dr. Schubert also states "it was well known before 2002 that interposing an interface layer between a metal and a semiconductor at a metal-semiconductor junction could reduce specific contact resistance." *Id.* ¶ 55; *see also id*. ¶ 56 (citing Schroen[10], issued in 1976 (Ex. 1124, Abstract) as disclosing the specific contact resistance obtained by using a thin insulating

[7] Chang is not a reference cited in this ground. Chang is cited in another ground.
[8] M.A. Taubenblatt et al., *Interface effects in titanium and hafnium Schottky barriers on silicon*, 44 APPLIED PHYS. LETTERS 895 (Ex. 1123, "Taubenblatt 1984").
[9] Ex. 1123, fn 18 (citing M. J. Turner and E. H. Rhoderick, Solid State Electron. II, 291, (1968)); *see also* Ex. 1117, fn 1.
[10] U.S. Patent No. 3,983,264 (Ex. 1124, "Schroen").

interfacial layer between a metal and a semiconductor is far smaller than the resistance observed in a structure of only a semiconductor and a metallization layer), *id.* ¶ 59 (quoting Iwaguro[11] (Ex. 1127) ¶ 6, which states "[b]y bringing a metal film into contact with this sub-silicon oxide film, an ohmic junction exhibiting favorable low contact resistance can be obtained.").

As to the use of titanium, Dr. Schubert cites a 1989 patent by Kim[12] (Ex. 1125) as describing an interface layer formed by titanium reducing silicon dioxide to achieve a specific contact resistance as low as 8Ω-μm^2. Ex. 1119, Schubert Decl. ¶¶ 57–58 (citing Ex. 1125, 5:27–30). In its discussion of Ground 5, Petitioner also cites Kim as evidence that ordinarily skilled artisans had achieved contact resistivity below 10 Ω-μm^2 using an interface layer, stating Kim "describes obtaining a specific contact resistance (resistivity) as low as 8 Ω-μm^2 for a junction between a Ti-W (titanium-tungsten) alloy and n-type silicon with an interfacial oxide layers that includes titanium dioxide therebetween. Pet. 54–55 (citing Ex. 1125, 4:63–5:1, 5:27–30).

In the Decision to Institute, we noted that Kim discloses the use of an alloy of tungsten and titanium, and specifically identifies disadvantages to the use of aluminum and titanium alone. Dec to Inst. 44–45 (citing Ex. 1025, 1:12–30. We found that Petitioner had not demonstrated a person of ordinary skill would have had reason to combine the teachings in Goodnick and Taubenblatt concerning experiments about the behavior of aluminum and titanium on silicon, as proposed by Dr. Schubert. *See* Dec. to

[11] Certified Translation of Japanese Laid-Open App. No. JPH11162874A (June 18, 1999) (Ex. 1127, "Iwaguro").
[12] U.S. Patent No. 4,845,050 (Ex. 1125, "Kim").

Inst. 44–45. We agreed with Patent Owner that Dr. Schubert's assertions that a person of ordinary skill would replace Goodnick's aluminum with Taubenblatt's titanium is inconsistent with Kim's disclosures concerning the use of a tungsten-titanium alloy consisting mostly of tungsten by weight. *Id.* at 45; *see also* PO Resp. 14–16. Although that issue remains before us, as discussed below, based on the evidence developed at trial, we further consider the presence of a titanium oxide and its effect on resistance.

Noting that Goodnick does not mention resistivity and Taubenblatt mentions resistivity only once, the Patent Owner Response contends that a person of ordinary skill would not have been motivated to combine the teachings of Goodnick and Taubenblatt in the manner proposed by Petitioner. PO Resp. 8–9 (citing Dec. to Inst. 42). Patent Owner emphasizes that Goodnick "presents experimental results of research into the effects of a layer of silicon dioxide between silicon and three metals (gold, platinum, and aluminum), none of which is titanium," that Taubenblatt "reports the results of several experiments depositing titanium on silicon under various conditions," and that neither reference is concerned with building a low resistance junction. *Id.* at 9. Patent Owner further argues that "[n]othing in Goodnick suggests any reason to study titanium" and "[n]othing in Taubenblatt suggests studying aluminum." *Id.*

According to Patent Owner, Petitioner's reference to the teachings in other documents, such as Kim, is unavailing because the Petition fails to establish a link between the subject matter cited by Dr. Schubert and his assertion that a person of ordinary skill would have substituted Taubenblatt's titanium for Goodnick's aluminum. *Id.* at 10.

Patent Owner further argues that the bulk resistivity of titanium is about 16 times that of aluminum, suggesting that a person of ordinary skill

would not have looked to replace aluminum with titanium. *Id.* at 11. Patent Owner notes Dr. Schubert's testimony that the resistivity of the metal in the metal-insulator-semiconductor stack is insignificant when compared to the much larger resistivity of insulators (PO Resp. 12 (citing Ex. 2076, Transcript of Deposition of Dr. Schubert ("Schubert Tr."), 65:21–67:9)). Patent Owner also cites its own expert, Dr. Kuhn, who testified that bulk resistivity of an insulator is irrelevant when it is used as a tunneling interface layer, i.e., because tunneling is a property of the barrier height at the junction and the physical thickness, not the material's bulk resistivity. *Id.* (citing Ex. 2070, Declaration of Dr. Kelin Kuhn ("Kuhn Decl.") ¶ 117). According to Dr. Kuhn,

> [I]t is not correct to say that a POSITA would ignore the bulk resistivity of the metal in a metal - insulator semiconductor stack of the type of interest here. That is especially true if the choice is between aluminum and titanium because, as I mentioned, aluminum is a significantly better electrical conductor than titanium (by a factor of about 16X).

Ex. 2070, Kuhn Decl. ¶ 120. In addition, "considerable research in the semiconductor industry has been (and currently is) conducted to try to find conductors that have marginally lower resistivity." *Id.* ¶ 119.

Petitioner's Reply counters that Patent Owner fails to consider the resistivity of the entire structure, not just the metal layer. *See* Pet. Reply 9. Petitioner notes that "[t]he proposed combination substitutes the Al-Al_2O_3 (in Goodnick) for Ti-TiO_x (in the proposed combination) (with the SiO_2 and Si layers the same in both structures)." *Id.* Petitioner acknowledges that the semiconductor's bulk resistivity far outweighs the bulk resistivity of the metal layer, regardless of whether aluminum or titanium is used in the metal layer, and notes that, because the bulk resistivity of the semiconductor is

largely fixed based on the doping concentration, the contributions from the SiO_2-Si would be similar in both structures. *Id.* According to Petitioner "that is precisely why a POSITA would have sought other means for reducing the junction's ***overall*** resistivity, such as by reducing the resistivity of the interface layer by substituting TiO_2 for Goodnick's higher-resistivity Al_2O_3 layer." Pet. Reply 10 (citing Ex. 1173, Schubert Decl. 2 ¶¶ 107-108). According to Petitioner "an ordinarily skilled artisan would have sought to provide an interface layer that reduces specific contact resistivity to reduce the power consumption of a device incorporating a contact with that interface layer." Pet. 35 (citing Takeshiu, 4:57–58; Ex. Schubert Decl. ¶ 149).

Responding to Dr. Kuhn's assertion that the bulk resistance of the material is irrelevant because the interface layer is used as a tunneling interface layer, Dr. Schubert states that Dr. Kuhn fails to consider tunneling barrier differences. *See* Pet. Reply 10 (citing PO Resp. 12; Ex. 2070, Kuhn Decl. ¶ 117). Dr. Schubert asserts that by substituting TiO_x for Al_2O_3 the tunneling probability in the proposed combination is nearly 30 times higher than the tunneling probability between Al and Al_2O_3, thereby reducing the structure's resistivity more than the 16 fold increase in resistivity attributable to the Ti in the Al metal layer. Ex. 1173, Schubert Decl. 2 ¶¶ 108, 114–121. According to Petitioner, TiO_x is substantially more conductive than Al_2O_3 because current can flow through TiO_x via electron tunneling and via conduction bands, but in the case of Al_2O_3, the tunneling barrier is higher, and current does not flow through Al_2O_3's conduction bands. Pet. Reply 11–12 (citing Ex. 1173, Schubert Decl. 2 ¶¶ 109–111).

Patent Owner contends that Dr. Schubert's tunneling analysis cited in the Petitioner Reply is a new theory not discussed in the Petition. PO Sur-

reply 11, 14–15. We consider the arguments in the Petitioner Reply to the extent Petitioner and Dr. Schubert offer an analytical reply to arguments in the Patent Owner Response, i.e., Dr. Kuhn's testimony that bulk resistivity of the metal is irrelevant because tunneling is a property of barrier height. PO Resp. 12 (citing Ex. 2070, Kuhn Decl. ¶ 117).

As discussed above, Petitioner cites Goodnick as recognizing a thick interfacial oxide at a metal-silicon interface suppresses current, thereby reducing rectifying characteristics, but a thin oxide layer sustains considerable current via tunneling and reduces the density of interface states by satisfying dangling bonds. *See* Section VI.B. The Petition also states that "reducing the barrier height of a junction reduces its specific contact resistivity" and that "for a junction between titanium and n-type silicon with an SiO_2 interface layer, the SiO_2 interface layer produces a net reduction of barrier height of more than 0.1 eV owing to the passivation that the SiO_2 interface layer provides." Pet. 33 (citing Ex. 1118, 5–6; Ex. 1119, Schubert Decl. ¶ 141; Ex. 1123, 3).

The issue presented in this challenge is whether a person of ordinary skill would have had reason to replace Goodnick's aluminum with titanium. Patent Owner disputes Dr. Schubert's tunneling analysis concerning the use of titanium. PO Sur-reply 10–11. Patent Owner argues that Dr. Schubert's 30 times improvement factor is wrong because Dr. Schubert uses a calculated electron affinity of 3.28 eV for Al_2O_3, rather than a measured value of 3.71 eV to determine the improvement. *Id.* at 10–11. According to Patent Owner, using the formulas in paragraph 116–121 of Dr. Schubert's 2nd Declaration and applying an electron affinity of 3.71eV, "[t]his tunneling probability for Al_2O_3 based on the measured electron affinity is only a factor of 1.66 greater than that of TiO_2." *Id.* at 11. Patent Owner further argues

that Dr. Schubert's analysis is based on documents and data dated after the 2002 effective filing date of the application of the subject patent, that Petitioner's reply fails to show "tunneling probability" translates to resistance, that Petitioner's reply fails to establish a baseline from which the significance of a factor of 30 increase in tunneling probability can be determined, and that Petitioner's tunneling argument in its reply is an improper new theory. *Id.*

In this context the arguments in the Petitioner Reply are responsive to issues raised by Dr. Kuhn. The Petition cites Kim's disclosure that an alloy of 10% titanium and the remainder of tungsten by weight forms a stable low resistance ohmic contact to silicon conduction members and a strong bond to a thick layer of silicon. Pet. 33.

Petitioner cites Kim (Ex. 1125) as evidence that a person of ordinary skill would have had reason to substitute Goodnick's aluminum with Taubenblatt's titanium and Dr. Schubert cites Kim as describing an interface layer formed by titanium reducing silicon dioxide to achieve a specific contact resistance as low as 8 Ω-μm^2. Ex. 1119, Schubert Decl. ¶¶ 57–58 (citing Ex. 1125, 5:27–30). According to Kim

> It is believed that during the sintering step titanium in the conductor 27 at the interface between the conductor 27 and the silicon conductive members 15, 17 and 16 reacts with native silicon dioxide present on the exposed portions of these conductors to form silicon and titanium dioxide, a semi-conductor, thereby reducing the interface resistance.

Ex. 1025, 4:63–5:1. Kim further states that "Alloys in the range of about 10% to 40% by weight of titanium and the remainder tungsten are particularly suitable for providing low resistance contacts to silicon." *Id.* at 5:2–4. Although Kim concerns alloys of tungsten and titanium, it is the

formation of the titanium dioxide documented in Kim that we understand to be the basis of Dr. Schubert's assertions concerning reduced ohmic resistance. The Petition points out that a person of ordinary skill would have recognized the existence of a relationship between barrier height and resistance for the device as a whole, stating

> [w]hile titanium oxides modestly passivate silicon surfaces—and therefore modestly reduce the junction's barrier height—they present less resistance to current than SiO_2 does. Thus, converting some of the interface layer's SiO_2 to a titanium oxide would have decreased specific contact resistivity further. But an ordinarily skilled artisan would have found it beneficial to leave *some* SiO_2 remaining in the interface layer to obtain the barrier-height reducing benefits of a passivating layer of SiO_2.

Pet. 33 (citing Ex. 1125, 4:63–5:1; Ex. 1119, Schubert Decl. ¶¶ 142–143; Ex. 1123, 3; Ex. 1130, 2–3). According to Petitioner, a TiO_x-SiO_2 interface layer combines the barrier-height-lowering of a passivating layer of SiO_2 with the lower resistance of a layer of titanium oxide." Pet. 35 (citing Ex. 1117, 7-8; Ex. 1125, 4:63-5:1; Ex. 1119, Schubert Decl. ¶ 145). As discussed above, even Patent Owner's electron affinity analysis recognizes at least some improvement in tunneling probability when using titanium instead of aluminum. PO Sur-reply 14. Goodnick demonstrates the effect of tunneling on specific resistance. *See* Section VI.B. Petitioner concludes that "an ordinarily skilled artisan would have expected that TiOx – SiO2 interface layer to present less electrical resistance than that presented by Goodnick's Al_2O_3 – SiO_2 interface layer. *Id* (citing Ex. 1119, Schubert Decl. ¶¶ 147–148.)

Petitioner does not cite Kim as part of this challenge, but as background art that reflects the knowledge of a person of ordinary skill. We addressed the disclosures of Kim in IPR2020-01264. There we determined

that Petitioner had not shown that Kim teaches a metal oxide layer or a layer of titanium dioxide. *See Samsung v. Acorn*, IPR2020-01264, Paper 18–20 at 17–19 PTAB (Jan. 13, 2021) (Decision Denying Institution). There we noted that "[t]he reference [Kim] simply says 'to form silicon and titanium dioxide, a semiconductor, thereby reducing the interface resistance,' with nothing to indicate that formation takes place as a layer."). *Id*. at 18. Consistent with this finding, we are not persuaded that Kim would have suggested to a person of ordinary skill replacing Goodnick's aluminum with Taubenblatt's titanium in a layered structure. Notwithstanding the bulk resistivity and tunneling effect evidence discussed above, there is insufficient evidence to conclude that a person or ordinary skill would have combined the teachings of Goodnick and Taubenblatt as proposed by Petitioner.

In consideration of the above, we find that Petitioner has not demonstrated by a preponderance of the evidence that a person of ordinary skull would have combined the teachings of Goodnick and Taubenblattt as proposed by Petitioner.

3. Claims 1, 3, 6, 10–12, 13, 15, 16, 19, 20, and 22

Citing its discussion of Goodnick, Petitioner contends that, if one of ordinary skill had reason to combine their teachings, Goodnick and Taubenblatt teach a Ti-TiO_x-SiO_2-Si contact, as recited in claim 1 (Pet. 36–41) with a tunnel barrier thickness of 0.1 nm to 5nm, as recited in claim 3 (*id.* at 42–43), wherein the metal oxide comprises an oxide of titanium, as recited in claim 6, the semiconductor oxide comprises an oxide of silicon, as recited in claim10, and the semiconductor oxide of the dielectric tunnel barrier is adjacent the semiconductor region, as recited in claim 11 (*id.* at 43–44). Noting that claim 13 depends from claim 3, which depends from

claim 1, Petitioner contends that the combined teachings of Goodnick and Taubenblatt teach a structure with the semiconductor oxide comprises an oxide of silicon, as recited in claim 13, that the metal oxide layer comprises an oxide of titanium, as recited in claim 15, and the metal electrical contact comprises titanium, as recited in claim 16. Pet. 44–45.

Claim 19 depends from claim 1 and recites the added limitations that "the semiconductor region comprises silicon, the semiconductor oxide comprises an oxide of silicon, the metal oxide of the dielectric tunnel barrier layer comprises an oxide of titanium, and the metal electrical contact comprises titanium." In support of its argument that Goodnick and Taubenblatt disclose this combination of features, Petitioner cites its earlier discussion of these individual features. Pet. 46–47.

Claim 20 depends from claim 1 and recites the added limitations that "the dielectric tunnel barrier layer is configured to reduce a height of a Schottky barrier between the metal electrical contact and the semiconductor region from that which would exist at a contact junction between the metal electrical contact and the semiconductor region without the dielectric tunnel barrier layer disposed therebetween." In support of its argument that Goodnick and Taubenblatt disclose this combination of features, Petitioner cites its earlier discussion of claim limitation 1(vii) and argues that the SiO_2 layer also reduces the Schottky barrier height between the titanium (the metal electrical contact) and the n-type silicon substrate (the semiconductor region) from the barrier height that would have existed without the SiO_2 layer disposed between them. Pet. 47–48.

Claim 22 recites "the dielectric tunnel barrier layer is configured to reduce contact resistivity between the metal electrical contact and the semiconductor region from that which would exist at a contact junction

between the metal electrical contact and the semiconductor region without the dielectric tunnel barrier layer disposed therebetween." In support of its argument that Goodnick and Taubenblatt disclose this combination of features, Petitioner cites its earlier discussion of claims 1 and 20, citing Carver (Ex. 1128, 2)[13], contends the terms "contact resistivity" and "specific contact resistivity" are interchangeable, and, citing Chang,[14] argues "[s]pecific contact resistivity depends on barrier height, so decreasing the barrier height between the metal electrical contact (titanium) and the semiconductor region (n-type silicon) would have decreased specific contact resistivity. Pet. 48–49 (citing Ex. 1119, Schubert Decl. ¶ 1119; Ex. 1118, 5–6).

Petitioner's challenges to each of these claims relies upon the combination of Goodnick and Taubenblatt in a layered structure with titanium as the metal oxide. Having determined that Petitioner has not demonstrated that a person of ordinary skill would have had reason to combine these teachings, we find that Petitioner has not demonstrated by a preponderance of the evidence that claims 1, 3, 6, 10–12, 13, 15, 16, 19, 20, and 22 are unpatentable.

E. Claims 8 and 17 as obvious over Goodnick in view of Jammy and Taubenblatt (Petitioner's Ground 4)

Claim 8 depends from claim 6, and claim 17 depends from claim 15; claim 6 and 15 recite that the metal oxide layer of the dielectric tunnel barrier layer comprises an oxide of titanium. Claim 8 and 17 recite that the semiconductor comprises an n-type doped source or drain of a transistor. Petitioner contends that a person of ordinary skill would have had reason to

[13] Carver is not cited as a reference in this ground.
[14] Chang is not cited as a reference in this ground.

grow Goodnick's 30 Å layer on Jammy's n-type doped source or drain of a transistor in a silicon substrate and then deposit aluminum. Pet. 49. Petitioner cites Taubenblatt as teaching depositing titanium instead of aluminum, arguing that swapping Goodnick's silicon substrate for Jammy's source or drain of a transistor and performing conventional processing steps, an ordinarily skilled artisan would have had a reasonable expectation of success in combining the teachings of the references. *Id.* at 49–50 (citing Ex. 1119, Schubert Decl. ¶¶ 203–204). Petitioner further argues that because Jammy discloses depositing conductive studs on its quantum conductive barrier and incorporates by reference Cote,[15] which teaches titanium conductive studs, depositing Jammy's conductive stud would have been equally suitable and would have yielded the same TiO_x-SiO_2 interface layer owing to the formation of the TiO_x diffusion barrier during Taubenblatt's annealing process. *Id.* at 50 n.3 (citing Ex. 1115, 4:5–8, Fig.1; Ex. 1129, 8:24–28; Ex. 1119, Schubert Decl. ¶ 202 n.13).

Petitioner's challenges to each of these claims relies upon the combination of Goodnick and Taubenblatt in a layered structure with titanium as the metal oxide. Having determined that Petitioner has not demonstrated that a person of ordinary skill would have had reason to combine these teachings, we find that Petitioner has not demonstrated by a preponderance of the evidence that claims 8 and 17 are unpatentable over Goodnick in View of Jammy and Taubenblatt.

[15] U.S. Patent No. 5,216,282 (Ex. 1129).

F. Claims 18 and 25–29 as obvious over Goodnick in view of Jammy, Taubenblatt, and Chang (Petitioner's Ground 5)

1. Chang (Ex. 1118)

Chang concerns the specific contact resistance of metal-semiconductor barriers. *See* Ex. 1118. Noting that the specific contact resistance at zero bias, R_c, is important as a measure of the ohmic or rectifying behavior of a metal-semiconductor barrier under operating conditions, Chang calculates R_c for metal-Si and metal-GaAs barriers on p-type and n-type samples. *Id.* at 1. According to Chang, R_c decreases exponentially with increasing temperatures and with decreasing barrier height. *Id.* Chang also states that for higher dopings where tunneling dominates, R_c decreases rapidly with increasing doping. *Id.*

2. Claims 18 and 25–29

Claim 18 depends from claim 17 and recites the additional limitation that "a specific contact resistivity between the n-type doped source or drain and the metal electric contact is less than 1 Ω-μm^2." Independent claim 25 recites an electrical junction having an interface layer, comprising a metal oxide separation layer and a semiconductor passivation layer, between a contact metal and a semiconductor comprising a transistor having a source and drain, in which the specific contact resistivity between the contact metal and the semiconductor is less than 1 Ω-μm^2. Claims 26–29 depend directly or indirectly from claim 25 and recite additional features. Claim 26 recites the metal oxide comprises an oxide of titanium; claim 27 recites the semiconductor oxide passivation layer comprises an oxide of the semiconductor; claim 28 recites the semiconductor oxide passivation layer is between 0.1μm and 5nm thick; claim 29 recites that the semiconductor oxide passivation layer is adjacent the semiconductor.

In support of its challenges to claims 25–29, Petitioner references its discussion of Goodnick, Jammy, Taubenblatt, and Chang concerning Grounds 1–4. Pet. 56–63. As discussed above, we are not persuaded that Petitioner has demonstrated a person of ordinary skill would have combined the references as proposed in Petitioner's challenges to each of these claims, i.e., the combination of Goodnick and Taubenblatt in a layered structure with titanium as the metal oxide. Having determined that Petitioner has not demonstrated that a person of ordinary skill would have had reason to combine these teachings, we find that Petitioner has not demonstrated by a preponderance of the evidence that claims 18 and 25–29 are unpatentable over Goodnick in View of Jammy Taubenblatt and Chang.

G. Objective indicia of non-obviousness of claim 4

1. Introduction

As discussed above, we find that Petitioner has demonstrated that a person of ordinary skill would have had reason to combine the teachings of Goodnick and Jammy and that their combined teachings would have suggested the limitations of claim 4 to a person of ordinary skill in the art. Before determining whether claim 4 is obvious in light of the prior art, we consider any relevant evidence of secondary or objective considerations of non-obviousness, as such evidence may lead to a conclusion that the challenged claim would not have been obvious to one of ordinary skill. *See Graham*, 383 U.S. at 17; *In re Piasecki*, 745 F.2d 1468, 1471–72 (Fed. Cir. 1984). Objective criteria constitute independent evidence of nonobviousness and may include any of the following: long-felt but unsolved needs, failure of others, unexpected results, commercial success, copying, licensing, and praise. *See Mintz v. Dietz & Watson, Inc.*, 679 F.3d 1372, 1378 (Fed. Cir. 2013).

Patent Owner contends that the invention reduces contact resistance, even for claims that do not specifically recite specific contact resistance values, and that the Petition acknowledges the tangible benefits of such reduced contact resistance. PO Sur-reply 20. According to Patent Owner, "[t]he objective evidence of non-obviousness overwhelmingly weighs in favor of the '691 Patent claims." PO Resp. 30 (citing Ex. 2090, Declaration of Dr. Paul Clifton ("Clifton Decl.") ¶¶ 8–102).

2. Presumption of Nexus

It is well established that to accord substantial weight to secondary considerations in an obviousness analysis, the evidence of secondary considerations must have a nexus to the challenged claim, i.e., there must be a legally and factually sufficient connection between the evidence and the patented invention. *Fox Factory, Inc. v. SRAM, LLC,* 944 F.3d 1366, 1373 (Fed. Cir. 2019). A patentee is entitled to a presumption of nexus when the patentee shows that the asserted objective evidence is tied to a specific product and that product embodies the claimed features and is coextensive with them. *Id.* Even where nexus cannot be presumed, "the patent owner is still afforded an opportunity to prove nexus by showing that the evidence of secondary considerations is the 'direct result of the unique characteristics of the claimed invention.'" *Id.* (quoting *In re Huang*, 100 F.3d 135, 140 (Fed. Cir. 1996)).

3. Commercial Success

Patent Owner argues that the products accused of infringement (and found to infringe) in the related litigation have been commercially successful. PO Resp. 41. Patent Owner argues that Petitioner has stipulated to commercial success (*id.*), and Petitioner, in fact, made the following stipulation in this proceeding:

> Samsung stipulates, solely for the purpose of, and for use in, this IPR proceeding, that the products accused of infringement in *Acorn Semi, LLC v. Samsung Electronics Co., Ltd. et al*., No. 2:19-cv-00347-JRG (E.D. Tex.) have been commercially successful. Samsung disputes, however, that any commercial success achieved by the accused products is attributable, in any way, to the challenged claims of the Acorn patents

Ex. 2116, 2.

In the Patent Owner Response, Patent Owner argued that infringement of the '691 patent was being tried in the Related Litigation and that the verdict that the jury would reach would likely establish infringement of the challenged claims, thus establishing that the accused products embody the claimed features and are coextensive with them. PO Resp. 38 (citing Ex. 1150 as evidence that the jury would address infringement of the '691 claims). After the Patent Owner Response was filed, the jury issued verdict. Ex. 2121. That verdict did not, however, address alleged infringement of claim 4. *Id.* at 4. Thus, the verdict did not establish any presumption of nexus between any commercial success of accused products and claim 4. Patent Owner has not presented evidence in this proceeding that the accused products in the litigation embodies the features of claim 4—district court infringement contentions are not evidence. Thus, Patent Owner has not established a presumption of nexus between claim 4 and the accused products in the Related Litigation. Nor has nexus been established by any other means.

4. Long felt need

According to Patent Owner, although Goodnick and Taubenblatt were available in prominent journals for over 20 years, the inability of others to produce the claimed invention during that time "is consistent with the fact that those references do not, in fact, actually suggest the claimed invention."

PO Resp. 31. Petitioner cites *Iron Grip Barbell Co. v. USA Sports, Inc.*, 392 F.3d 1317, 1325 (Fed. Cir. 2004), for the proposition that "[a]bsent a showing of long-felt need or the failure of others, the mere passage of time without the claimed invention is not evidence of nonobviousness." Pet. Reply 28.

Patent Owner cites multiple assertions from the International Technology Roadmap for Semiconductors (ITRS) concerning the incentive to reduce the contact resistance at metal-semiconductor junctions and notes that the 2001 ITRS stated achieving this goal via conventional approaches "May also require that the metal/semiconductor barrier height be reduced." *Id.* at 32 (quoting Ex. 2093, 28). We note that this quotation indicates a person of ordinary skill would have understood the relationship between ohmic resistance and barrier height.

Citing Dr. Clifton's testimony that ITRS Roadmap represents an opinion and that many of its statements may not turn out to be correct, Petitioner argues that we cannot rely upon such conjecture. Pet. Reply 23–24 (citing Ex. 1172, Transcript of Deposition of Dr. Paul Clifton ("Clifton Tr.") 274:24–275:6, 276:20–277:2). Citing testimony by Dr. Clifton that technology categories mentioned in the 2001 and 2003 ITRS do not anticipate that invention, Petitioner further notes that the 2001 and 2003 ITRS lays out a broad industry strategy out to 2019 to achieve lowered contact resistance using technologies that are different from those of the challenged patents. *Id.* at 24 (citing Ex. 1172, Clifton Tr., 272:14–21).

Petitioner asserts that the reference to other technologies indicates an absence of a specific long felt need or the absence of existing solutions to the problem of reducing specific resistance. *Id.* On this record Patent Owner has not provided sufficient evidence of a nexus between the long felt

and the specific limitations recited in claim 4, i.e., the structure recited in claim 1, in which the oxide of the tunnel barrier layer has a thickness between 0.1 nm and 5 nm (claim 3) and the semiconductor region is an n-type source or drain of a transistor (claim 4).

5. Unexpected results

Patent Owner contends that, prior to the invention claimed in the '691 patent, the conventional approach to achieving low ohmic resistivity contacts was to remove the oxide layer and use metals capable of reacting with the native oxide during the sintering or bonding step—thereby removing the native oxide from the metal-silicon interface. PO Resp. 32–33. Patent Owner contends that its introduction of an interface oxide layer, i.e., inserting a dielectric into a metal-semiconductor contact in order to reduce resistivity was hailed as counter-intuitive. *Id.* at 33–34 (citing Ex. 2095, 2928; Ex. 2096, 3; Ex. 2097, 5; Ex. 2070, Kuhn Decl. ¶49); *see* PO Sur-reply 23–24).

Petitioner notes that Patent Owner's expert, Dr. Kuhn, testified she had not studied whether the concepts in Patent Owner's inventions were unique or novel and had not considered background prior art references, such as Kim (Ex. 1125), Schroen (Ex. 1124), and Iwaguro (Ex. 1127), that Dr. Schubert asserts disclose inserting an insulating layer between a metal and semiconductor contact to achieve a low contact resistance. Pet. Reply 26–27 (citing Ex. 1169, Transcript of Deposition of Dr. Kelin Kuhn ("Kuhn Tr.") 237:19–24, 254:4–9; Ex. 1119, Schubert Decl. ¶¶ 55–59). According to Petitioner, in view of Dr. Schubert's unrebutted testimony that using an interface layer to achieve low contact resistance was known, there is no nexus between the claims and any purported unexpected results. *Id.*

Patent Owner notes that Petitioner was unsuccessful in relying on Kim in related IPR2020-01264 and has not tried to rely on Schroen and Iwagaro in this proceeding or the district court litigation. PO Sur-reply 21–22. Patent Owner characterizes Schroen and Iwagaro as marginally relevant references that fail to disclose a two layer interface layer with a metal oxide layer, and, even if they disclose limited aspects of the invention, they do not suggest the inventors' novel combination. PO Sur-reply 22 (citing *Henny Penny Corp. v. Frymaster LLC*, 938 F.3d 1324, 1333 (Fed. Cir. 2019); Ex. 1169, Kuhn Tr. 87:16–88:1). Patent Owner emphasizes that it "was the first to understand, explain, and control the unexpected reduced-resistance effect. [Patent Owner] had the insight; Kim, Schroen, and Iwaguro had none." *Id.* Patent Owner does not identify how the unexpected results relate specifically to claim 4. On this record, therefore, Patent Owner has not provided sufficient evidence of a nexus between any unexpected results and the limitations of claim 4.

6. Industry praise

Patent Owner notes that in 2004 and 2006, the inventors published two papers describing the invention (Exs. 2045, 2046 (collectively "the Connelly Papers")) that have been cited over 270 times in the professional literature. PO Resp. 34. On this record, Patent Owner has not demonstrated a sufficient nexus between any praise in these papers and specific limitations of claim 4. Patent Owner does not identify how the structures described in those papers relate to claim 4. Further, Petitioner provides evidence of the contrary. Claim 4, via its dependency from claim 1, recites a structure comprising a metal oxide layer. The Connolly papers disclose only a silicon nitride interface layer, which is not a metal oxide interface layer. Ex. 1171,

172:2–10, 175:19–25; Ex. 1173 ¶ 139. Thus, praise for the Connelly Papers does not constitute objective evidence of nonobviousness for claim 4.

7. Alleged suspicious behavior

Patent Owner alleges that, in an abstract in 2017, Petitioner's researchers cited the Connelly papers as a basis for their work, but removed the citation when the paper was published in full in 2018. *See* PO Resp. 47–51 (citing Ex. 2047, 1; Ex. 2048, 4879). According to Patent Owner, Petitioner's abstract focused on how contact resistance limits performance in scaling silicon MOSFETs and states that, instead of increased doping, the researchers studied an alternate option, i.e. a metal-interface-semiconductor (MIS) structure that mirrors the challenged independent claims. *Id.* at 48. Patent Owner states that the paper published by Petitioner's researchers in 2018 that did not cite the Connelly Papers "describes in positive terms reducing ρ_c, reducing the height of the Schottky barrier, depinning the Fermi level, and tuning the SBH (Schottky barrier height) between a low work-function metal and n-type silicon." *Id.* at 49. According to Patent Owner, there is a nexus between Petitioner's actions and claim 4, which recites a structure comprising a semiconductor oxide and metal oxide layers that together depin the Fermi level and recite an n-type semiconductor. *Id.* Patent Owner also alleges that Petitioner filed its own patent applications based on Patent Owner's technology. *Id.* at 49–51 (noting the similarity between a graph showing the thickness of the insulating mater and contact resistivity in Petitioner's patent a graph showing oxide thickness and specific contact resistance in Patent Owner's patents).

Noting that the sentence citing the Connelly Papers in the abstract is not present in the final published paper, Petitioner contends that "[o]mitting a citation when there is no longer relevant information in a paper is ***not***

evidence of any suspicious behavior—it is what authors routinely do" and "even Dr. Kuhn did not cite to the Connelly Papers in her related work," even though she was aware of the Connelly Papers. Pet. Reply 30 (citing Ex. 1169, Kuhn Tr., 34:4–23). Petitioner further points out that its "graph merely presents what was known in the literature long before [Patent Owner's] patents." *Id.* at 31.

The alleged suspicious behavior is not an objective criteria cited in Federal Circuit precedent. Patent Owner provides no testimony concerning the motivations of the authors of the abstract or the published paper and we make no inferences from the difference in the citations concerning the Connelly Papers.

8. Summary

In consideration of the above, we do not find that the objective evidence supports a conclusion of nonobviousness. Thus, we determine that claim 4 would have been obvious over Goodnick and Jammy.

VII. PATENT OWNER'S MOTIONS TO EXCLUDE

Patent Owner filed a Motion to Exclude. Paper 44 ("PO Mot. To Exclude"). Petitioner filed an Opposition to Patent Owner's Motion. Paper 48 (Pet. Opp."). Patent Owner filed a Reply. Paper 49 ("PO Reply)

A. Motion to exclude Goodnick cross examination testimony

Patent Owner moves to exclude portions of the deposition testimony of its own expert, Dr. Stephen Goodnick, as outside the scope of the challenged claims. PO Mot. To Exclude, 1. In particular, Patent Owner moves to exclude testimony elicited on cross examination concerning whether certain metal oxides fall within the scope of the challenged claims. *Id.* (citing Ex. 1168, Transcript of Deposition of Dr. Stephen Goodnick

("Goodnick Tr.") 65:20–66:17, 113:20–117:23, and 137:17–141:10 (collectively, the "Goodnick Metal-Oxide Testimony")). Patent Owner argues that "nothing in Dr. Goodnick's declaration even remotely addresses the interpretation of 'metal oxide' in the challenged claims, what is or is not a 'metal oxide,"' but that his "declaration instead concerns primarily the Goodnick paper, particularly whether a person of ordinary skill in the art (POSITA) would understand it as disclosing distinct stratified layers of Al_2O_3 and SiO." *Id.* at 2.

Petitioner argues that Dr. Goodnick's first declaration (Ex. 2043), which in its entirety is incorporated by reference in Dr. Goodnick's second declaration (Ex. 2080), includes statements directed to the composition of the various layers in a prior art structure, including a metal oxide layer. Pet. Opp. 2 (citing Ex. 2043, Goodnick Decl. ¶ 53). Noting Dr. Goodnick's testimony that the Goodnick Paper does not teach distinct layers, but instead that Al_2O_3 and SiO_2 form a "checkerboard" pattern, Petitioner asserts that questioning Dr. Goodnick on what constitutes a distinct metal oxide layer was proper. *Id.* at 2–3.

Although Patent Owner contends Dr. Goodnick's declaration did not open the door for general questioning about metal oxides (PO Opp. 2–3), we agree with Petitioner that the proper scope of cross examination includes Dr. Goodnick's understanding of what constitutes a distinct layer. A primary issue raised by Patent Owner against Petitioner's challenge that Goodnick anticipates is that, notwithstanding its use of the term layer, Goodnick does not teach distinct layers that are required by the claim. *See* Section VI.B. One of those layers is a metal oxide layer (Ex. 1101, claim 1), in particular a titanium oxide layer (claim 6). In view of Dr. Goodnick's checkerboard analogy in his declaration, it was proper for Petitioner to question Dr.

Goodnick about the extent of materials in the checkerboard. Both parties argue there may be implications of Dr. Goodnick's testimony for purposes of infringement litigation. *See* Pet. Opp. 4–6; PO Reply 3–4. We do not address those implications. The issue before us is whether Goodnick would have taught or suggested to a person of ordinary skill the limitations of the claims, which the parties agree include distinct layers of metal oxide and other semiconductor oxide. *See* Section VI.B. As Dr. Goodnick testified that his article did not teach such distinct layers, it was proper for Petitioner to explore Dr. Goodnick's views concerning the composition of a layer during cross examination.

In consideration of the above, Patent Owner's motion to exclude the Goodnick Metal Oxide testimony is denied.

B. Motion to exclude Kuhn cross examination testimony

Patent Owner also moves to exclude deposition testimony of its expert, Dr. Kuhn, about claim limitations that recite an "oxide of titanium." PO Mot. To Exclude 7. Patent Owner asserts that "the 'oxide of titanium' limitation was not substantively addressd in this or any other IPR petition, and Dr. Kuhn never addressed it in her declaration (Ex. 2070)." *Id*. Claim 6, which depends from claim 3, which depends from claim 1, recites that the metal oxide, which finds its antecedent in claim 1, is an oxide of titanium.

In combination with Goodnick's disclosure of an interface layer, Petitioner cited Taubenblatt as describing the formation of a titanium oxide layer. Pet. 30–31. As discussed extensively above, however, Petitioner was unable to demonstrate that a person of ordinary skill would have had reason to substitute Taubenblatt's titanium for Goodnick's aluminum. Therefore, we do not address specifically claims drawn to an oxide of titanium and do not consider the testimony Patent Owner seeks to exclude concerning the

titanium oxide genus and various species of titanium oxide. *See* PO Mot. To Exclude 8–11. For purposes of this proceeding, we determine that Patent Owner's Motion to Exclude the Kuhn oxide of titanium testimony is dismissed moot.

VIII. PETITIONER'S MOTION TO EXCLUDE

Petitioner filed a Motion to Exclude. Paper 45 ("Pet. Mot. To Exclude"). Patent Owner filed an Opposition. Paper 47 ("PO Opp."), and Petitioner filed a Reply. Paper 49 ("Pet. Reply").

Petitioner moves to exclude certain direct testimony of Dr. Paul Clifton, i.e., paragraphs 8–15, 19–25, 36–45, 47–50, 52–63, 67, 69–70, 72, 76–77, and 81–107 of the Clifton Declaration, becasue "during Dr. Clifton's deposition, it became clear that Acorn was offering Dr. Clifton only as a fact witness, not an expert witness and, accordingly, it became apparent that the expert opinions offered in Dr. Clifton's declaration are improper." Pet. Mot. To Exclude 3. Patent Owner offered Dr. Clifton's testimony in support of its objective considerations arguments. *See* Section VI.G.

Patent Owner contends that Petitioner misconstrues comments made by Patent Owner's counsel during Dr. Clifton's deposition indicating that Dr. Clifton was a fact witness, that Dr. Clifton testified as a hybrid fact-expert witness, that Petitioner failed to timely object to Dr. Clifton's testimony and that Petitioner's motion is mostly moot because the objective indicia that was the subject of Dr. Clifton's testimony is established independently from the documentation in evidence. *See generally* PO Opp.

Patent Owner asserts that, in *inter partes* reviews, the Board's rules do not specifically distinguish between experts and fact witnesses and that all witnesses (whether fact witnesses or expert witnesses) provide their direct testimony in the form of declarations. PO Opp. 2. This is in contrast to

procedures in district courts, where expert witnesses must be designated and special discovery procedures apply. *Id.* (citing Fed. R. Civ. P. 26(a)(2)). Although as a procedural matter, Patent Owner correctly characterizes the difference between district court proceedings and those before the Board, we do not endorse a standard that would allow a party to re-characterize a witness's testimony after the fact. In this case, however, we need not decide that issue.

At his deposition, Dr. Clifton stated that he understood himself to be testifying as a fact witness, not an expert (Pet. Reply 1, citing Ex. 1117, Clifton Tr. 100:2–12) and Dr. Clifton's declaration includes information that demonstrates sufficient knowledge of facts for admissibility (Ex. 2090 ¶¶ 3–6 (describing his education, his technical research in MIS junctions (although not specifically concerning contact resistance), his years of experience, his employment by Patent Owner since 2004, and his current role as Vice President of Semiconductor Technologies)). We do not agree with Petitioner that Dr. Clifton's occasional use of the expression "I believe" itself transforms his testimony from fact to opinion concerning the objective criteria. *See* Pet. Mot. To Exclude 6. Much of the testimony in Dr. Clifton's declaration concerning the long felt need in the industry, what the patents describe, the Connelly papers, the work that led up to the structures Patent Owner developed, the reactions of other researchers in the field, and the unexpected nature of the results, is based on events that occurred shortly before or while Dr. Clifton was employed by Patent Owner and derive from Dr. Clifton's personal knowledge. In light of his background and the largely factual nature of his testimony, Petitioner's arguments for excluding Dr. Clifton's testimony concern the weight that we should accord his testimony, rather than its admissibility.

Petitioner's Motion to Exclude is therefore denied.

IX. CONCLUSION[16]

In consideration of the above we find that Petitioner has demonstrated by a preponderance that claims 1–3 and 13 are unpatentable as anticipated by Goodnick and that claim 4 is unpatentable as obvious over the combined teachings of Goodnick and Jammy.

In summary:

Claims	35 U.S.C. §	Basis	Claims Shown Unpatentable	Claims Not shown Unpatentable
1–3, 13	102	Goodnick	1–3, 13	
4	103	Goodnick, Jammy	4	
1, 3, 6, 10–13, 15, 16, 19, 20, 22	103	Goodnick, Taubenblatt		1, 3, 6, 10–13, 15, 16, 19, 20, 22
8, 17	103	Goodnick, Jammy, Taubenblatt		8, 17
18, 25–29	103	Goodnick, Jammy, Taubenblatt, Chang		18, 25–29
Overall Outcome			1–4, 13	6, 8, 10–12, 15–20, 22, 25–29

[16] Should Patent Owner wish to pursue amendment of the challenged claims in a reissue or reexamination proceeding subsequent to the issuance of this decision, we draw Patent Owner's attention to the April 2019 *Notice Regarding Options for Amendments by Patent Owner Through Reissue or Reexamination During a Pending AIA Trial Proceeding. See* 84 Fed. Reg. 16,654 (Apr. 22, 2019). If Patent Owner chooses to file a reissue application or a request for reexamination of the challenged patent, we remind Patent Owner of its continuing obligation to notify the Board of any such related matters in updated mandatory notices. *See* 37 C.F.R. § 42.8(a)(3), (b)(2).

X. ORDER

In consideration of the above it is:

ORDERED that claims 1–4 and 13 are unpatentable;

FURTHER ORDERED that Petitioner's Motion to Exclude certain declaration testimony of Dr. Clifton is DENIED;

FURTHER ORDERED that Patent Owner's Motion to Exclude certain portions of the Goodnick deposition testimony is DENIED;

FURTHER ORDERED that Patent Owner's Motion to Exclude certain portions of the Kuhn deposition testimony is DIMISSED as moot; and

FURTHER ORDERED that, because this is a Final Written Decision, parties to the proceeding seeking judicial review of the decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

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Paper 56
Date: February 9, 2022

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD.,
Petitioner,

v.

ACORN SEMI, LLC,
Patent Owner.

IPR2020-01282
Patent 10,090,395 B2

Before BRIAN J. McNAMARA, JOHN R. KENNY, and AARON W. MOORE, *Administrative Patent Judges.*

KENNY, *Administrative Patent Judge*.

DECISION
Final Written Decision
Determining Some Challenged Claims Unpatentable
Dismissing Patent Owner's Motion to Exclude
Denying Petitioner's Motion to Exclude
35 U.S.C. § 318(a)

I. INTRODUCTION

Samsung Electronics Co., Ltd. ("Petitioner") filed a Petition, Paper 2 ("Petition" or "Pet."), to institute an *inter partes* review of claims 1–6, 8–12, and 14–28 ("challenged claims") of U.S. Patent No. 10,090,395 B2 (Ex. 1101, "'395 patent"). Acorn Semi LLC ("Patent Owner") filed a Preliminary Response, Paper 10 ("Prelim. Resp."), contending that the Petition should be denied as to all challenged claims.

On February 10, 2021, we instituted an *inter partes* review of all challenged claims. Paper 20 ("Institution Decision" or "Inst. Dec."). Patent Owner filed a Patent Owner Response (Paper 28, "PO Resp.") and an Updated Mandatory Notice reporting a jury verdict in a related district court litigation (Paper 30; Ex. 2121). Petitioner filed a Reply (Paper 37, "Pet. Reply"), and Patent Owner filed a Sur-reply (Paper 42, "PO Sur-reply").

Petitioner filed a Motion to Exclude certain testimony by Dr. Paul Clifton. (Paper 44, "Pet. Mot. Excl."). Patent Owner filed an Opposition to Petitioner's Motion to Exclude (Paper 46, "Opp. to Pet. Mot. Excl."), and Petitioner filed a Reply to Patent Owner's Opposition to Petitioner's Motion to Exclude (Paper 50, "Reply Pet. Mot. Excl.").

Patent Owner filed a Motion to Exclude certain cross-examination testimony of its witnesses, Dr. Kelin J. Kuhn and Dr. Stephen Goodnick (Paper 43, "PO Mot. Excl."). Petitioner filed an Opposition to Patent Owner's Motion to Exclude (Paper 47, "Opp. to PO Mot. Excl."), and Patent Owner filed a Reply to Petitioner's Opposition to Patent Owner's Motion to Exclude (Paper 49, "Reply Pet. Mot. Excl.").

A transcript of an oral hearing held on October 13, 2021 (Paper 55, "Tr.") has been entered into the record.

We have jurisdiction under 35 U.S.C. § 6. For the reasons discussed below, we determine that Petitioner has shown, by a preponderance of the evidence, that claims 1–5 and 8–10 are unpatentable. Petitioner, however, has not shown, by a preponderance of the evidence, that claims 6, 11, 12, and 14–28 are unpatentable.

A. Related Matters

The Petition states that the '395 patent is asserted in *Acorn Semi, LLC v. Samsung Electronics Co. Ltd.*, Civil Action No. 2:19-cv-347 (E.D. Tex.) ("Related Litigation"), and that the complaint was served on October 24, 2019. Pet. 3 (citing Ex. 1158).

Petitioner and Patent Owner identify IPR2020-01207 ("'1207 IPR") as also concerning the '395 patent. Pet. 3; Paper 4, 2. Petitioner and Patent Owner also identify *inter partes* reviews concerning patents related to the '395 patent that may be affected by the outcome of this proceeding. *See* Pet. 3, Paper 4, 2. Petitioner and Patent Owner also identify patents and patent applications that are related to the '395 patent. *See* Pet. 3, Paper 4, 1.

B. The '395 Patent

The '395 patent "relates to a process for depinning the Fermi level of a semiconductor at a metal-interface layer-semiconductor junction and to devices that employ such a junction." Ex. 1101, 1:32–35. The '395 patent explains that Schottky's theory concerning the ability of a junction to conduct current in one direction more favorably than in the other direction, i.e., the rectifying behavior of a metal/semiconductor junction (e.g., an aluminum/silicon junction) depends upon a barrier at the surface of the contact between the metal and the semiconductor. *Id.* at 1:52–64. Because the barrier height at the metal/semiconductor interface determines the

electrical properties of the junction, controlling the barrier height is an important goal. *Id.* at 3:10–21.

The '395 patent further explains that Schottky's theory postulates the height of the barrier, as measured by the potential necessary for an electron to pass from the metal to the semiconductor, is the difference between the work function of the metal (i.e., the energy required to free an electron at the Fermi level (the highest occupied energy state of the metal at T=0)) and the electron affinity of the semiconductor (i.e., the difference between the energy of a free electron and the conduction band of the semiconductor); but experimental results indicate a weaker variation of the barrier height with the work function than implied by this model. Ex. 1101, 1:55–2:9. To explain the discrepancy between the predicted and observed behavior, Bardeen introduced the concept of semiconductor surface states, i.e., energy states within the bandgap between the valence and conduction bands at the edge of the semiconductor crystal that arise from incomplete covalent bonds, impurities, and other effects of termination. *Id.* at 2:10–24, Fig. 1 (showing dangling bonds 120). Although Bardeen's model assumes that surface states are sufficient to pin the Fermi level in the semiconductor at a point between the valence and conduction bands, such that the barrier height should be independent of the metal's work function, in experiments, this condition is observed rarely. *Id.* at 2:25–31.

According to the '395 patent, Tersoff proposed that the Fermi level of a semiconductor is pinned near an effective "gap center" due to metal induced gap states (MIGS), which are energy states in the bandgap of the semiconductor that become populated with metal. Ex. 1101, 2:41–47. Thus, the wave functions of electrons in the metal do not terminate abruptly at the

surface of the metal, but decay in proportion to the distance from the surface, extending inside the semiconductor. *Id.* at 2:50–54.

> To maintain the sum rule on the density of states in the semiconductor, electrons near the surface occupy energy states in the gap derived from the valence band such that the density of states in the valence band is reduced. To maintain charge neutrality, the highest occupied state (which defines the Fermi level of the semiconductor) will then lie at the crossover point from states derived from the valence band to those derived from the conduction band. This crossover occurs at the branch point of the band structure.

Id. at 2:54–63. The '395 patent also notes one further surface effect on diode characteristics is inhomogeneity, i.e., "if factors affecting the barrier height (e.g., density of surface states) vary across the plane of the junction, the resulting properties of the junction are found not to be a linear combination of the properties of the different regions." *Id.* at 3:2–6.

According to the '395 patent, "a classic metal-semiconductor junction is characterized by a Schottky barrier, the properties of which (e.g., barrier height) depend on surface states, MIGS and inhomogeneities." Ex. 1101, 3:6–9. "Before one can tune the barrier height, however, one must depin the Fermi level of the semiconductor." *Id.* at 3:16–18. The '395 patent seeks to depin the Fermi level of the semiconductor while still permitting substantial current flow between the metal and the semiconductor. *Id.* at 3:18–21. The '395 patent describes depinning the Fermi level as follows:

> By depinning the Fermi level, the present inventors mean a condition wherein all, or substantially all, dangling bonds that may otherwise be present at the semiconductor surface have been terminated, and the effect of MIGS has been overcome, or at least reduced, by displacing the semiconductor a sufficient distance from the metal.

Id. at 3:36–41. The '395 patent achieves this goal using thin interface layers disposed between a metal and a silicon-based semiconductor to form a "metal-interface layer-semiconductor junction" with minimum specific contact resistances. *Id.* at 3:25–29. "The interface layer thickness corresponding to this minimum specific contact resistance will vary depending upon the materials used." *Id.* at 3:29–36. That thickness, however, "allows for depinning the Fermi level of the semiconductor while still permitting current to flow between the metal and semiconductor when the junction is biased." *Id.* "Minimum specific contact resistances of less than or equal to approximately 10 Ω-μm^2 or even less than or equal to approximately 1Ω-μm^2 may be achieved for such junctions in accordance with the present invention." *Id.* at 3:42–45. Such low contact resistances are achieved by selecting a metal with a work function near the conduction band of the semiconductor for n-type semiconductors, or a work function near the valence band for p-type semiconductors. *Id.* at 5:30–34.

Figure 8 of the '395 patent is reproduced below:

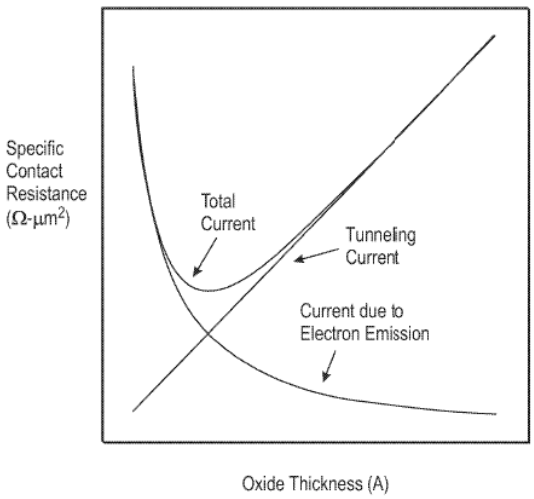


Figure 8 of the '395 patent

Figure 8 above is a graph of interface specific contact resistance versus interface thickness for a structure where the work function of the metal is the same as the electron affinity of the semiconductor, such that the Fermi level of the metal lines up with the conduction band of the semiconductor. Ex. 1101, 14:42–48. According to the '395 patent, Figure 8 shows that, at large thicknesses, the interface layer poses significant resistance to current, but as the interface layer thickness decreases, resistance falls due to increased tunneling current. *Id.* at 14:48–51. However, at some point, as the interface layer gets thinner, the effect of MIGS increasingly pulls the Fermi level of the metal down towards the mid-gap of the semiconductor, creating a Schottky barrier and increasing resistance. *Id.* at 14:51–55. Thus, there is an optimum thickness where the resistance is at a minimum and the effect of MIGS has been reduced to depin the metal and lower the Schottky barrier, but the layer is sufficiently thin to allow significant current across the interface layer, such that specific contact resistances of less than or equal to approximately 2500 Ω-μm^2, 1000 Ω-μm^2, 100 Ω-μm^2, 50 Ω-μm^2, 10 Ω-μm^2, or less than 1 Ω-μm^2 reportedly can be achieved. *Id.* at 14:56–65.

In one embodiment, an electrical device has an interface layer that may be a monolayer or several monolayers of passivating material (e.g., a nitride, oxide, oxynitride, arsenide, hydride and/or fluoride) and may include a separation oxide layer. Ex. 1101, 3:46–59. The specific contact resistance for this electrical device is reported to be less than 10 Ω-μm^2. *Id.* at 3:52–53. In another embodiment, the interface layer consists of a passivation layer fabricated by exposing the semiconductor to nitrogenous material (e.g., ammonia (NH_3), nitrogen (N_2) or unbound gaseous nitrogen (N) generated from a plasma process). *Id.* at 3:60–64. Another embodiment uses an interface layer of passivating material disposed between the surface of a

semiconductor and a conductor, in which the interface layer is of a sufficient thickness to reduce the effect of MIGs in the semiconductor and passivates the semiconductor but, because the thickness of the interface layer is chosen to provide minimum, or near minimum, specific contact resistance for the junction, significant current may flow between the conductor and the semiconductor. *Id.* at 4:1–14.

In other embodiments, the interface layer is configured to allow a Fermi level of the conductor to (i) align with a conduction band of the semiconductor, (ii) align with a valence band of the semiconductor, and (iii) to be independent of the Fermi level of the semiconductor, allowing current to flow between the conductor and the semiconductor when the junction is biased because the thickness of the interface layer corresponds to a minimum or near minimum contact resistance for the junction. Ex. 1101, 4:15–26. Specific contact resistances of less than or equal to approximately 2500 Ω-μm^2, 1000 Ω-μm^2, 100 Ω-μm^2, 50 Ω-μm^2, 10 Ω-μm^2, or less than 1 Ω-μm^2 reportedly can be achieved. *Id.* at 4:27–30.

C. Claims

As mentioned, Petitioner challenges claims 1–6, 8–12, and 14–28, of which claims 1, 17, and 23 are independent. Claim 1 reads:

> 1. An electrical junction, comprising a region in a semiconductor substrate, a metal electrical contact to said region, and an interface layer between said region and said metal electrical contact, said region being electrically connected to said metal electrical contact through said interface layer and said interface layer comprising a metal oxide and a semiconductor oxide, and being in contact with said region in the semiconductor substrate and said metal electrical contact.

Ex. 1101, 18:45–52.

D. Asserted Grounds

Petitioner asserts that the challenged claims would have been unpatentable based on the following grounds (Pet. 9–10):

Ground	Claim(s) Challenged	35 U.S.C. §	Reference(s)/Basis
1	1–3, 8–10	102(b)	Goodnick[1]
2	4	103(a)	Goodnick, Jammy[2]
3	5	103(a)	Goodnick
4	1, 11, 12, 15, 23–25, 28	103(a)	Goodnick, Taubenblatt 1982[3]
5	14, 17–19, 22	103(a)	Goodnick, Jammy, Taubenblatt 1982
6	6	103(a)	Goodnick, Jammy, Taubenblatt 1982, Chang[4]
7	16, 26, 27	103(a)	Goodnick, Taubenblatt 1982, Kim[5]
8	20, 21	103(a)	Goodnick, Jammy, Taubenblatt 1982, Kim

E. Level of Ordinary Skill in the Art

Petitioner describes an ordinarily skilled artisan as having any of the following combinations of education and experience:

[1] S.M. Goodnick et al., *Effects of a thin SiO_2 layer on the formation of metal-silicon contacts*, 18 J. VAC. SCI. & TECH. 949 (Apr. 1981) (Ex. 1121).
[2] U.S. Patent No. 6,724,088 B1 (Ex. 1122).
[3] M.A. Taubenblatt and C.R. Helms, *Silicide and Schottky barrier formation in the Ti-Si and the Ti-SiO_x-Si systems*, 58 J. APPLIED PHYS. 6308 (1982) (Ex. 1123).
[4] C.Y. Chang et al., *Specific contact resistance of metal-semiconductor barriers*, 15 SOLID STATE ELECS. 541 (1971) (Ex. 1124)
[5] U.S. Patent No. 4,845,050 (Ex. 1125).

> [i] a Ph.D. in electrical engineering, physics, materials science, or chemical engineering, with two years of practical experience with semiconductor research and design;
>
> [ii] a Master's degree in electrical engineering, physics, materials science, or chemical engineering, with four years of practical experience with semiconductor research and design; or
>
> [iii] a Bachelor's degree in electrical engineering, physics, materials science, or chemical engineering, with six to eight years of practical experience with semiconductor research and design.

Pet. 14 (citing Ex. 1126, Schubert Decl. ¶¶ 70–71).

The Patent Owner Preliminary Response did not comment on the level of ordinary skill in the art. In our Institution Decision, we were persuaded that Petitioner's description of the level of ordinary skill is appropriate for the subject matter of the '395 patent and applied it in that Decision. Inst. Dec. 9–10. The Patent Owner Response does not comment on the level of ordinary skill in the art. *See generally* PO Resp. Thus, we apply the description of the level of ordinary skill set forth in the Petition in this Decision. Ex. 1126, Schubert Decl. ¶ 66.

II. CLAIM CONSTRUCTION

For petitions filed after November 13, 2018, we interpret claim terms using "the same claim construction standard that would be used to construe the claim in a civil action under 35 U.S.C. 282(b)." 37 C.F.R. § 42.100(b) (2019). In this context, claim terms "are generally given their ordinary and customary meaning" as understood by a person of ordinary skill in the art in question at the time of the invention. *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312–13 (Fed. Cir. 2005) (citations omitted) (en banc). "In determining the meaning of the disputed claim limitation, we look principally to the intrinsic evidence of record, examining the claim language itself, the written

description, and the prosecution history, if in evidence." *DePuy Spine, Inc. v. Medtronic Sofamor Danek, Inc.*, 469 F.3d 1005, 1014 (Fed. Cir. 2006) (citing *Phillips*, 415 F.3d at 1312–17). Extrinsic evidence is "less significant than the intrinsic record in determining 'the legally operative meaning of claim language.'" *Phillips*, 415 F.3d at 1317 (citations omitted).

Any special definition for a claim term must be set forth in the specification with reasonable clarity, deliberateness, and precision. *In re Paulsen*, 30 F.3d 1475, 1480 (Fed. Cir. 1994).

We construe only those claim terms that require analysis to determine whether to institute *inter partes* review. *See Vivid Techs., Inc. v. Am. Sci. & Eng'g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999) (holding that "only those terms need be construed that are in controversy, and only to the extent necessary to resolve the controversy").

A. Depin a Fermi Level of the Metal Electrical Contact in the Vicinity of the Junction

Petitioner proposes that the phrase "depin a Fermi level of the metal electrical contact in the vicinity of the junction," recited in claim 5, should be construed as "passivate the semiconductor surface and reduce the effects of metal-induced gap states in the semiconductor." Pet. 15. According to Petitioner, "[t]he specification consistently describes that depinning a Fermi level involves passivating the semiconductor surface and reducing the effects of metal-induced gap states in the semiconductor." *Id.* In the Preliminary Response, Patent Owner supported this construction. Prelim. Resp. 44 ("In the Acorn patents, depinning the Fermi level requires two things: (1) passivating the semiconductor surface by satisfying dangling bonds and (2) reducing the effects of MIGs."). The Specification supports

Petitioner's proposed construction by providing the following definition for the phrase "depinning the Fermi level":

> By depinning the Fermi level, the present inventors mean a condition wherein all, or substantially all, dangling bonds that may otherwise be present at the semiconductor surface have been terminated, and the effect of MIGS has been overcome, or at least reduced, by displacing the semiconductor a sufficient distance from the metal.

Ex. 1101, 3:36–41.

In view of this definition in the Specification and the parties' agreement in pre-institution briefing, we construed the phrase "depin a Fermi level of the metal electrical contact in the vicinity of the junction" as "passivate the semiconductor surface and reduce the effects of metal-induced gap states in the semiconductor" in our Institution Decision. Patent Owner has not requested that we modify that construction. *See generally* PO Resp. Thus, we maintain it.

B. Specific Contact Resistivity

Petitioner argues that the term "specific contact resistivity," recited in claims 5 and 6, should be construed as interchangeable with the term "specific contact resistance." Pet. 16–17. Petitioner asserts that the Specification of the '395 patent and the claims of the '395 patent use those terms interchangeably. *Id.* at 16 (citing Ex. 1101, 3:25–29, 3:42–45, 3:52–53, 4:22–30). Petitioner further asserts that those working in the art commonly used those terms interchangeably. *Id.* at 16–17 (citing Ex. 1134, 2; Ex. 1126, Schubert Decl. ¶¶ 74–76). In the Preliminary Response, Patent Owner did not respond to this proposed construction.

In our Institution Decision, we construed the terms "specific contact resistivity" and "specific contact resistance" to be interchangeable. Patent

Owner has not requested that we modify this construction. *See generally* PO Resp. Thus, we maintain it.

C. An Interface Layer Comprising a Metal Oxide and a Semiconductor Oxide

In its Preliminary Response, Patent Owner argued that, in the related litigation, Petitioner and Patent Owner agreed to construe the phrase an "interface layer comprising a metal oxide and a semiconductor oxide" as "said interface layer comprising a layer of a metal oxide and a *distinct* layer of a semiconductor oxide." Prelim. Resp. 35 (citing Ex. 2009). Patent Owner asserted that the district court adopted that construction. *Id.* (citing Ex. 2053, 27). In our Institution Decision, we found that the record supported Patent Owner's arguments. Inst. Dec. 13 (citing Ex. 2009; Ex. 2053, 27). Further, in our Institution Decision, we noted that no party argued that we should construe the phrase differently than the district court. *Id.* Thus, we construed "an interface layer comprising a metal oxide and a semiconductor oxide" as "said interface layer comprising a layer of a metal oxide and a distinct layer of a semiconductor oxide." *Id.* No party has requested that we modify this construction. *See generally* PO Resp., Pet. Reply. Thus, we maintain it.

III. ANALYSIS OF ASSERTED GROUNDS

"In an [*inter partes* review], the petitioner has the burden from the onset to show with particularity why the patent it challenges is unpatentable." *Harmonic Inc. v. Avid Tech., Inc.*, 815 F.3d 1356, 1363 (Fed. Cir. 2016) (citing 35 U.S.C. § 312(a)(3) (requiring *inter partes review* petitions to identify "with particularity . . . the evidence that supports the grounds for the challenge to each claim")). This burden of persuasion never shifts to Patent Owner. *See Dynamic Drinkware, LLC v. Nat'l Graphics,*

Inc., 800 F.3d 1375, 1378 (Fed. Cir. 2015) (discussing the burden of proof in *inter partes* review).

Anticipation is a question of fact, as is the question of what a prior art reference teaches. *In re NTP, Inc.*, 654 F.3d 1279, 1297 (Fed. Cir. 2011). "A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros. Inc., v. Union Oil Co.*, 814 F.2d 628, 631 (Fed. Cir. 1987); *see also Finisar Corp. v. DirecTV Group, Inc.*, 523 F.3d 1323, 1334 (Fed. Cir. 2008) (to anticipate a patent claim under 35 U.S.C. § 102, "a single prior art reference must expressly or inherently disclose each claim limitation"). Moreover, "[b]ecause the hallmark of anticipation is prior invention, the prior art reference—in order to anticipate under 35 U.S.C. § 102—must not only disclose all elements of the claim within the four corners of the document, but must also disclose those elements 'arranged as in the claim.'" *Net MoneyIN, Inc. v. VeriSign, Inc.*, 545 F.3d 1359, 1369 (Fed. Cir. 2008) (quoting *Connell v. Sears, Roebuck & Co.*, 722 F.2d 1542, 1548 (Fed. Cir. 1983)).

Whether a reference anticipates is assessed from the perspective of an ordinarily skilled artisan. *See Dayco Prods., Inc. v. Total Containment, Inc.*, 329 F.3d 1358, 1368 (Fed. Cir. 2003) ("'[T]he dispositive question regarding anticipation [i]s whether one skilled in the art would reasonably understand or infer from the [prior art reference's] teaching' that every claim element was disclosed in that single reference." (quoting *In re Baxter Travenol Labs.*, 952 F.2d 388, 390 (Fed. Cir. 1991))).

Additionally, under the principles of inherency, if the prior art necessarily functions in accordance with, or includes, the claimed limitations, it anticipates. *MEHL/Biophile Int'l Corp. v. Milgraum*, 192 F.3d

1362, 1365 (Fed. Cir. 1999) (citation omitted); *In re Cruciferous Sprout Litig.*, 301 F.3d 1343, 1349–50 (Fed. Cir. 2002).

As set forth in 35 U.S.C. § 103(a),

> [a] patent may not be obtained . . . if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.

The question of obviousness is resolved on the basis of underlying factual determinations including: (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of ordinary skill in the art; and (4) objective evidence of nonobviousness. *Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966). Additionally, the obviousness inquiry typically requires an analysis of "whether there was an apparent reason to combine the known elements in the fashion claimed by the patent at issue." *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 418 (2007) (citing *In re Kahn*, 441 F.3d 977, 988 (Fed. Cir. 2006) (requiring "articulated reasoning with some rational underpinning to support the legal conclusion of obviousness")); *see In re Warsaw Orthopedic, Inc.*, 832 F.3d 1327, 1333 (Fed. Cir. 2016) (citing *DyStar Textilfarben GmbH & Co. Deutschland KG v. C. H. Patrick Co.*, 464 F.3d 1356, 1360 (Fed. Cir. 2006)).

An obviousness analysis "need not seek out precise teachings directed to the specific subject matter of the challenged claim, for a court can take account of the inferences and creative steps that a person of ordinary skill in the art would employ." *KSR*, 550 U.S. at 418; *accord In re Translogic Tech., Inc.*, 504 F.3d 1249, 1259 (Fed. Cir. 2007). Petitioner, however, cannot satisfy its burden of proving obviousness by employing "mere conclusory statements." *In re Magnum Oil Tools Int'l, Ltd.*, 829 F.3d 1364,

1380 (Fed. Cir. 2016). Instead, Petitioner must articulate a reason why an ordinarily skilled artisan would have combined the prior art references. *In re NuVasive*, 842 F.3d 1376, 1382 (Fed. Cir. 2016).

A reason to combine or modify the prior art may be found explicitly or implicitly in market forces; design incentives; the "interrelated teachings of multiple patents"; "any need or problem known in the field of endeavor at the time of invention and addressed by the patent"; and the background knowledge, creativity, and common sense of an ordinarily skilled artisan. *Perfect Web Techs., Inc. v. InfoUSA, Inc.*, 587 F.3d 1324, 1328–29 (Fed. Cir. 2009) (quoting *KSR*, 550 U.S. at 418–21).

Before determining whether a claim would have been obvious in light of the prior art, we consider any relevant evidence of secondary considerations of non-obviousness. *See Graham*, 383 U.S. at 17. Notwithstanding what the teachings of the prior art would have suggested to one of ordinary skill in the art at the time of the invention, the totality of the evidence submitted, including objective evidence of non-obviousness, may lead to a conclusion that the challenged claims would not have been obvious to one of ordinary skill. *In re Piasecki*, 745 F.2d 1468, 1471–72 (Fed. Cir. 1984).

A. Ground 1: Asserted Anticipation by Goodnick

Petitioner asserts that Goodnick anticipates claims 1–3 and 8–10. Pet. 9.

1. Goodnick

Goodnick concerns experiments "to observe the influence of thin SiO_2 layers on the chemical formation of metal-silicon contacts." Ex. 1121, 1.[6]

[6] For this exhibit, we cite the page numbers added by Petitioner.

According to Goodnick, a thick interfacial oxide at a metal-silicon interface suppresses current, thereby reducing rectifying characteristics. *Id.* A sufficiently thin oxide, however, may sustain considerable current via tunneling and may reduce the density of interface states by satisfying dangling bonds. *Id.* Goodnick discloses that, as a result, with a sufficiently thin oxide:

> the Fermi level at the surface may become unpinned and the barrier height is more directly determined by the metal work function. In addition, a thin interfacial layer may act as a barrier to the chemical reaction and interdiffusion that characterizes the intimate metal silicon contact. Thus, the presence of a thin oxide at the interface acts as a passivating influence, both from an electronic and a chemical standpoint.

Id.

Goodnick investigates three metals (aluminum, platinum, and gold) and grew SiO_2 at 700 degrees Celsius to approximately 30Å. Ex. 1121, 1. Goodnick reports that the 30Å thermally grown SiO_2 appeared as a complete barrier to the formation of platinum silicide and less of a barrier to the Au-Si reaction, where "widespread dissolution of the SiO_2 layer and reaction between the Au and Si appeared to occur." *Id.* at 5. "Al partially reduces the thin SiO_2 layer to form Al_2O_3 and free Si. This reaction appeared to be self-limiting, with SiO_2 still present at the interface, even after heating at 400°C." *Id.* Goodnick concludes:

> a thermally grown SiO_2 layer appears effective in preventing or retarding the widespread interdiffusion of elemental Si. However, chemically etched surfaces react readily with the metal overlayer even though a thin native oxide grows prior to deposition. The different chemical nature of room temperature air grown oxides of Si is suggested as an explanation of these results.

Id.

2. Claim 1

a. An electrical junction

Petitioner asserts that, if the preamble of claim 1 is limiting, Goodnick discloses it by describing an Al–Al_2O_3–SiO_2–Si contact structure. Pet. 21 (citing Ex. 1121, Goodnick, 1–2, 5; Ex. 1126, Schubert Decl. ¶ 118). Petitioner further asserts that the Specification of the '395 patent uses the terms "contact" and "junction" interchangeably. *Id.* Patent Owner presents no counterargument regarding the preamble of claim 1. PO Resp. 60. After reviewing the record, we determine that Petitioner has proven that Goodnick discloses the preamble of claim 1.[7]

b. a region in a semiconductor substrate

Petitioner argues that Goodnick discloses "a region in a semiconductor substrate" by describing a silicon substrate. Pet. 22 (citing Ex. 1121, Goodnick, 1; Ex. 1126, Schubert Decl. ¶ 122). Patent Owner presents no counterargument regarding this limitation. PO Resp. 60. After reviewing the record, we determine that Petitioner has proven that Goodnick discloses this limitation.

c. a metal electrical contact to said region

Petitioner asserts that Goodnick discloses "a metal electrical contact to said region" by describing the "chemical formulation of metal-silicon contacts" and by describing aluminum as an example of a metal electrical contact. Pet. 22 (citing Ex. 1121, Goodnick, 1; Ex. 1126, Schubert Decl. ¶ 123). Patent Owner presents no counterarguments regarding this limitation. After reviewing the record, we determine that Petitioner has proven that Goodnick discloses this limitation.

[7] For this reason, we do not need to determine whether the preamble of claim 1 is limiting.

d. an interface layer between said region and said metal electrical contact

Petitioner asserts that Goodnick discloses "an interface layer between said region and said metal electrical contact" by describing a process that produces an Al_2O_3–SiO_2 interface layer between the silicon substrate and the aluminum. Pet. 22 (citing Ex. 1121, Goodnick, 1–2, 5; Ex. 1126, Schubert Decl. ¶ 124). Patent Owner presents no counterargument regarding this limitation. PO Resp. 60. After reviewing the record, we determine that Petitioner has proven that Goodnick discloses this limitation.

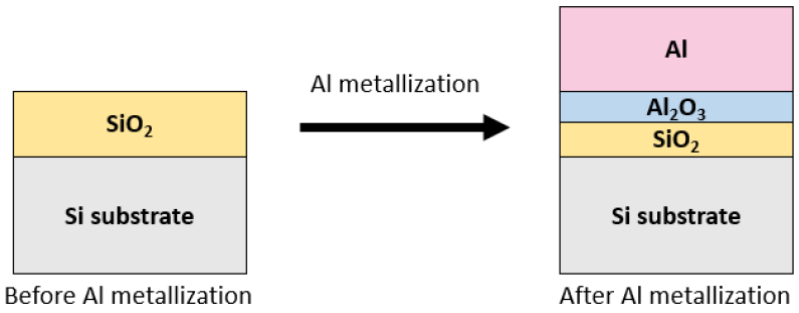
e. said region being electrically connected to said metal electrical contact through said interface layer

Petitioner asserts that Goodnick discloses "said region being electrically connected to said metal electrical contact through said interface layer" by characterizing its Al–Al_2O_3–SiO_2–Si contact as a "metal-silicon contact" and by describing that its interfacial oxide layers are thin while indicating that "an oxide layer that is sufficiently thin may sustain considerable current via tunneling." Pet. 23 (citing Ex. 1121, Goodnick, 1, 5; Ex. 1126, Schubert Decl. ¶ 126). Patent Owner presents no counterargument regarding this limitation. PO Resp. 60. After reviewing the record, we determine that Petitioner has proven that Goodnick discloses this limitation.

f. said interface layer comprising a metal oxide and a semiconductor oxide

Petitioner asserts that Goodnick discloses this limitation by describing that the results from experiments indicated that SiO_2 and Al_2O_3 existed simultaneously at the interface, probably resulting from diffusion barrier formed by the Al_2O_3 layer to the transport of Al to the SiO_2 layer. Pet. 23 (citing Ex. 1121, Goodnick, 1, 5; Ex. 1126, Schubert Decl. ¶ 125–126).

Petitioner proposes the schematic depiction of the involved metallization process and the resulting contact shown below:



Petitioner's Depiction of Goodnick's Metallization Process

Id. at 18 (citing Ex. 1121, Goodnick, 1–2, 5; Ex. 1126, Schubert Decl. ¶¶ 80–86). As illustrated above, Petitioner contends that, after metallization, the contact has a distinct metal contact layer of Al and a metal oxide layer, Al_2O_3. Petitioner's depiction is illustrative and is not reproduced from Goodnick.

Patent Owner argues that Goodnick does not disclose a stratified layer of Al_2O_3 distinct from SiO_2, as depicted in the Petition. PO Resp. 60.

Patent Owner states that "[a]ll challenges in the petition utilize Goodnick as the primary reference and are based on Goodnick disclosing distinct stratified layers of different material, including a layer of Al_2O_3, as shown in various petitioner-created diagrams in the petition." PO Resp. 52. (citing Pet. 18, 21 and reproducing a portion of Petitioner's metallization diagram shown above).[8] *Id.* Patent Owner argues that, notwithstanding Petitioner's diagrams that purport to illustrate Goodnick teaching clean

[8] Patent Owner also references its Preliminary Response, which notes that in district court litigation the parties agreed that claim limitation 1(iii) and 1(iv) "require two distinct layers: (1) a passivating dielectric tunnel barrier layer (comprising semiconductor oxide) and (2) a metal oxide layer." *Id.*, Prelim. Resp. 38–39.

stratification of distinct layers, Goodnick includes no such diagrams, only uses the term "layer" twice, and does not support the Petition's assertions. *Id.* at 18 (citing Ex. 2043, Declaration of Dr. Stephen Goodnick ("Goodnick Decl."); Ex. 2080, Second Declaration of Dr. Stephen M. Goodnick ("2nd Goodnick Decl.")).

Dr. Goodnick, who authored the Goodnick reference, states that Petitioner and Dr. Schubert have "misinterpreted key aspects of my paper." Ex. 2043, Goodnick Decl. ¶ 5. Noting the conventional understanding at the time of his paper was that imperfections in the surface layer, i.e. "dangling bonds," caused the Fermi level to be pinned, Dr. Goodnick states that his reference to the Fermi level becoming unpinned "refer[s] only to the fact that dangling bonds in the silicon are passivated by the oxide layer." *Id.* ¶ 43. Dr. Goodnick also states that, at the time of his paper, the phenomenon of MIGS was poorly understood and "the interaction of pinning due to MIGS and pinning due to dangling surface bonds had not been explored." *Id.* ¶ 44. According to Dr. Goodnick, the inventors

> realized that those two pinning mechanisms can be jointly addressed leading to better results . . . they were able to discover that there is an optimum thickness at which the beneficial reduction of pinning by MIGS suppression is negated by the adverse increase in tunneling resistance as the interfacial layer is made thicker.

Id. ¶ 45 (referring to Figure 8 of the '395 patent).

The specific issue before us is what an ordinarily skilled artisan would have understood from the Goodnick reference. Dr. Schubert contends that such an artisan would have understood Goodnick to disclose the claimed layered structure. *See* Ex. 1126, Schubert Decl. ¶¶ 79–87 (at ¶ 82 quoting Goodnick's description of Figure 8(b) that "[i]n contrast to the air exposed

sample, an Al_2O_3 layer exists at the Al-SiO_2-Si interface"). Dr. Goodnick indicates that an ordinarily skilled artisan at the time would not have understood his paper to mean there is a layer of Al_2O_3 on top of a layer of SiO_2, but only that Al_2O_3 and SiO_2 were found together in the interface region between the aluminum and the semiconductor. *See* Ex. 2043 ¶¶ 32–40; Ex. 2080, 2nd Goodnick Decl. ¶¶ 8–9.

Figure 8(a) of Goodnick shows "[p]eak to peak Auger sputter profile Al on room temperature oxidized Si, unheated" and Figure 8(b) of Goodnick shows "[p]eak to peak Auger profile of Al on 30 Å SiO_2, unheated." Ex. 1121, 5. Responding to Petitioner's assertions concerning the case where 30Å of SiO_2 was first placed on the silicon before depositing the aluminum, Dr. Goodnick refers to Figure 8(b) of his paper, on which the X-axis is sputter time. Ex. 2043, Goodnick Decl. ¶¶ 32–34; Ex. 2080, 2nd Goodnick Decl. ¶ 8. Referring to Figures 8(a) and 8(b) of his paper, Dr. Goodnick testifies that the high levels of Al_2O_3 shown between 0 and 5 minutes represent Al_2O_3's presence on the top surface of the aluminum, and the high level of aluminum between 10 minutes and 30 minutes corresponds to the aluminum deposition. Ex. 2043, Goodnick Decl. ¶ 33. According to Dr. Goodnick, the high level of silicon after 50 minutes corresponds to the silicon substrate, and the high levels of aluminum and silicon between 30 and 50 minutes is the aluminum-silicon interface. *Id.* Dr. Goodnick further testifies that Figure 8(b) shows that Al_2O_3 and SiO_2 were present at the aluminum silicon interface, but "it cannot be determined where Al_2O_3 is present with respect to SiO_2." *Id.* ¶ 34. Dr. Goodnick asserts that the presence of a peak in the Al_2O_3 curve at about 40 minutes and the "O" curve (representing SiO_2) between 35 and 40 minutes and the fact that both curves have the same general shape "means that both compounds were found in the

same relative quantities in the interface region." *Id.* According to Dr. Goodnick, "[an ordinarily skilled artisan] understanding this data would not conclude that there is a layer of Al_2O_3 on top of a layer of SiO_2 as Samsung claims . . . only that both Al_2O_3 and SiO_2 were found together in the interface region between the aluminum and the silicon." *Id.*

Nevertheless, comparing Figures 8a and 8b, the Goodnick reference expressly states:

> Figure 8(a) shows the peak-to-peak profile of an unheated sample with an air grown oxide. It appears that Si has diffused into the Al and collected at the Al_2O_3-Al interface at the surface. No buildup of Al_2O_3 is seen at the Al-Si interface. Figure 8(b) is a profile of an unheated sample with 30Å SiO_2 at the interface. *In contrast to the air exposed sample, an Al_2O_3 layer exists at the Al-SiO_2-Si interface.* This is suggestive of the reduction reaction seen previously, with the presence of SiO_2 necessary for formation of Al_2O_3. Heat treatment of samples resulted in little change in the profiles with the exception of greater concentration of Si at the surface of the unoxidized samples.

Ex. 1121, 5 (emphasis added).

The Goodnick reference further states that, even at elevated temperatures, the results imply that the reaction is self-limiting "probably [as] a result of the diffusion barrier formed by the Al_2O_3 layer to the transport of Al to the SiO_2 layer." Ex. 1121, 5. Dr. Goodnick now states that "[t]his statement was a speculation based on the fact that both SiO_2 and Al_2O_3 were still present at the interface, whereas thermodynamically it was expected that Al would completely reduce SiO_2 to form Al_2O_3 and free Si." Ex. 2043, Goodnick Decl. ¶ 39.

Patent Owner argues that Goodnick's two references to an Al_2O_3 layer do not state that the Al_2O_3 layer is distinct from SiO_2 and were not meant to

suggest the type of stratified distinct layers in the Petition. PO Resp. 52–53 (citing Ex. 2080, 2nd Goodnick Decl. ¶¶ 8–9).

Patent Owner further contends that the Auger profile data in Figure 8(b) does not support Petitioner's stratified layer arguments. PO Resp. 53. Patent Owner states that, in addition to the Al_2O_3 hump corresponding to 35–55 minutes sputter time indicating an Al_2O_3 layer, the data also shows oxygen of unknown origin rising earlier and peaking to the left of the Al_2O_3 line, as well as aluminum and silicon in the same vicinity. *Id.* Thus, Patent Owner argues that "according to the Auger profile data, the 'Al_2O_3 layer' is not a stratified distinct layer of Al_2O_3 as the petition asserts." *Id.* at 54 (citing Ex. 1121, 953).

Patent Owner does not explain sufficiently, however, why the data it cites on the Auger profile does not support Petitioner's contentions. PO Resp. 53–54. The Goodnick reference uses the term "layer" at least 40 times, and in no case does Goodnick ascribe a meaning to "layer" that is different from one layer being distinct from another. *See generally* Ex. 1121.

Patent Owner next argues that XPS measurements reported in Goodnick indicate that both SiO_2 and Al_2O_3 exist simultaneously at the interface, but reveal nothing about the spatial distribution of the Al_2O_3 and SiO_2. PO Resp. 54–55 (citing Ex. 2080, 2nd Goodnick Decl. ¶ 10). Patent Owner also argues that the Goodnick reference speculated an Al_2O_3 diffusion barrier is the probable reason the $4\ Al + 3\ SiO_2 \rightarrow 2Al_2O_3 + 3Si$ reaction is self-limiting, but that speculation is an untested hypothesis insufficient to support Petitioner's contentions. *Id.* at 55 (citing Ex. 2080, 2nd Goodnick Decl. ¶¶ 11–13).

Goodnick is entitled "Effects of a thin SiO_2 layer on the formation of metal-silicon contacts" and states "[t]he reactions that occur between different metals and silicon wafers with a thin oxide layer have been investigated." Ex. 1121, cover page. Goodnick further states "a thin interfacial layer may act as a barrier to the chemical reaction and interdiffusion that characterizes the intimate metal silicon contact. Thus, the presence of a thin oxide at the interface act as a passivating influence, both from an electronic and a chemical standpoint." Ex. 1121, 1.

Taken in context, we agree with Dr. Schubert that an ordinarily skilled artisan would have understood Goodnick to refer to Al_2O_3 as a distinct layer. Ex. 1126, Schubert Decl. ¶ 85; Ex. 1173, Schubert Reply Decl. ¶ 86. Referring to Fig. 8(a), Goodnick states that in an unheated sample with an air grown oxide "[i]t appears that Si has diffused into the Al and collected at the Al_2O_3-Al interface at the surface. No buildup of Al_2O_3 is seen at the Al-Si interface." Ex. 1121, 5. Noting that Fig. 8(b) is a profile of an unheated sample with 30Å of SiO_2 at the interface, Goodnick states "[i]n contrast to the air exposed sample, an Al_2O_3 layer exists at the Al-SiO_2-Si interface." *Id.*

Petitioner notes that, on cross-examination, Dr. Goodnick acknowledged (i) that the Al metal layer would diffuse into the SiO_2 interface layer and reduce the portion of the SiO_2 layer nearest the Al layer to Al_2O_3, (ii) that once the Al_2O_3 layer forms, it would be difficult for aluminum atoms to diffuse through the Al_2O_3 layer to continue reaction with the SiO_2 layer, and (iii) because the reaction is self-limiting, a portion of the original SiO_2 layer would remain once the reaction forming the Al_2O_3 layer stopped. Pet. Reply 6–7 (citing Ex. 1168, Goodnick Tr. 55:5–25, 57:19–58:8, 59:24–60:7, 81:4–8). In view of, *inter alia*, Dr. Goodnick's cross-

examination testimony, we are persuaded by Dr. Schubert's testimony that an ordinarily skilled artisan would have understood that distinct layers of Al_2O_3 and SiO_2 are formed. Ex. 1173, Schubert Reply Decl. ¶¶ 85–98.

As to Patent Owner's arguments concerning speculation (PO Sur-reply), we note that our inquiry is what Goodnick would have disclosed to an ordinarily skilled artisan. The Goodnick reference's comments, even if Dr. Goodnick now deems them to be speculative, are consistent with the physical evidence. Ex. 1173, Schubert Reply Decl. ¶ 88–92. Further, Dr. Goodnick testified that the only hypothesis presented as of today for why some of the original silicon dioxide remained in his structure is that aluminum oxide formed a diffusion barrier that prevented aluminum from further diffusing into the silicon dioxide layer underlying the aluminum oxide. Ex. 1168, Goodnick Tr. 129:19–130:7. Moreover, no one has argued that it was beyond the skill of an ordinarily skilled artisan to create the described layer of Al_2O_3. PO Resp. 52–60; Pet. Reply 6–8; PO Sur-reply 2–4.

In sum, we find that Petitioner has proven that Goodnick discloses the limitation of "said interface layer comprising a metal oxide and a semiconductor oxide."

g. being in contact with said region in the semiconductor substrate and said metal electrical contact

Petitioner asserts that Goodnick discloses this limitation by describing evaporating aluminum onto a SiO_2 layer grown on a silicon substrate. Pet. 24. Patent Owner presents no counterarguments regarding this limitation. PO Resp. 60. After reviewing the record, we determine that Petitioner has proven that Goodnick discloses this limitation.

h. Summary

Petitioner has proven that Goodnick discloses all limitations of claim 1, and, thus, Petitioner has proven that Goodnick anticipates claim 1.

3. Claims 2, 3, and 8–10

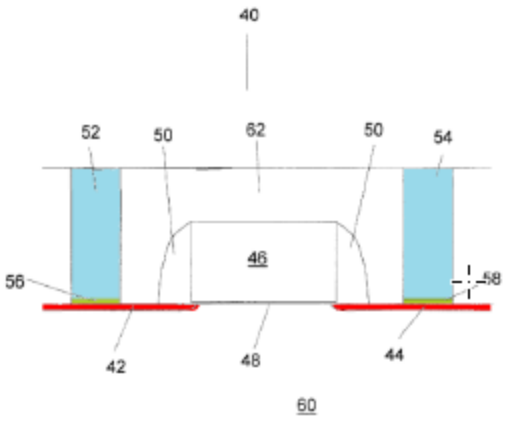
Petitioner sets forth how it contends Goodnick discloses all limitations that claims 2, 3, and 8–10 add to claim 1. Pet. 24–26 (and the exhibits cited therein). Patent Owner presents no counterarguments regarding those additional limitations. PO Resp. 60. After reviewing the record, we determine that Petitioner has proven that Goodnick discloses the limitations that claims 2, 3, and 8–10 add to claim 1. Thus, Petitioner has proven that Goodnick anticipates claims 2, 3, and 8–10.

B. Ground 2: Asserted Obviousness over Goodnick and Jammy

Petitioner asserts that claim 4 would have been obvious over Goodnick and Jammy. Pet. 9.

1. Jammy

Jammy generally describes a MOSFET (metal oxide semiconductor field effect transistor) that incorporates a quantum conductive barrier between a conductive stud and a semiconductor substrate. Ex. 1122, 2:42–53; 3:16–22. Figure 1 of Jammy, with color annotations added by Petitioner, is reproduced below:



Pet. 18. Figure 1 above shows MOSFET 40 in substrate 60. Ex. 1122, 3:9–11, 4:9–11. In Figure 1 above, conductive studs 52 and 54, quantum barrier layers 56 and 58, and shallow source/drain diffusions 42 and 44 are highlighted. Pet. 18; Ex. 1122, 3:11–18. Jammy discloses that "[p]referred quantum conductive materials are inorganic oxides or nitrides, more preferably silicon nitride compounds selected from the group consisting of silicon nitride or silicon oxynitride." Ex. 1122, 3:51–54. Jammy also discloses that "studs 52 and 54 would typically be made of tungsten or a doped polycrystalline silicon." *Id.* at 4:32–33.

Jammy states that its "invention is not limited to any specific device configuration . . . , however, the structures of the invention are preferably incorporated into a MOSFET or other transistor devices." Ex. 1122, 4:1–4. Jammy identifies Cote (Ex. 1135) as disclosing relevant transistor structures and incorporates Cote by reference. *Id.* at 4:5–8. Cote discloses that "titanium, titanium nitride, tungsten, or other appropriate metallurgy" can be used to form a diffusion contact stud. Ex. 1135, 8:24–28.

2. Claim 4

a. Arguments

Petitioner sets forth its evidence and arguments that the combination of Goodnick and Jammy teach or suggest every element of claim 4 and provides reasons why an ordinarily skilled artisan would combine the teachings of those references. Pet. 27–29. In response, Patent Owner relies on the argument it presented for claim 1, that Goodnick does not disclose distinct metal oxide and semiconductor oxide layers. PO Resp. 60. As set forth in Section III.A.2.f above, we found that Petitioner has proven that Goodnick discloses distinct metal oxide and semiconductor oxide layers.

For Ground 2 and for all other obviousness grounds, Patent Owner further argues "[t]he objective evidence of nonobviousness overwhelmingly weighs in favor of the nonobviousness of the '395 Patent claims." PO Resp. 30 (citing Ex. 2090, Declaration of Dr. Paul Clifton ("Clifton Decl.") ¶¶ 8–102). Petitioner disagrees. Pet. Reply 25–36.

We address the parties' arguments about objective evidence of nonobviousness below.

b. Objective Indicia of Nonobviousness

Objective criteria constitute independent evidence of non-obviousness. *Mintz v. Dietz & Watson, Inc.*, 679 F.3d 1372, 1378 (Fed. Cir. 2012). The totality of the evidence submitted, including objective evidence of nonobviousness, may lead to a conclusion that the challenged claims would not have been obvious to an ordinarily skilled artisan. *See Piasecki*, 745 F.2d at 1471–1472. Secondary considerations may include any of the following: long-felt but unsolved needs, failure of others, unexpected results, commercial success, copying, licensing, and praise.

It is well established that to accord substantial weight to secondary considerations in an obviousness analysis, the evidence of secondary considerations must have a nexus to the challenged claim, i.e., there must be a legally and factually sufficient connection between the evidence and the patented invention. *Fox Factory, Inc. v. SRAM, LLC*, 944 F.3d 1366, 1373 (Fed. Cir. 2019). A patentee is entitled to a presumption of nexus when the patentee shows that the asserted objective evidence is tied to a specific product and that product embodies the claimed features and is coextensive with them. *Id.* Even where nexus cannot be presumed, "the patent owner is still afforded an opportunity to prove nexus by showing that the evidence of secondary considerations is the 'direct result of the unique characteristics of

the claimed invention.'" *Id.* (quoting *In re Huang*, 100 F.3d 135, 140 (Fed. Cir. 1996)).

1. Commercial Success

Patent Owner argues that the products accused of infringement (and found to infringe) in the related litigation have been commercially successful. PO Resp. 37–47. Patent Owner argues that Petitioner has stipulated to the commercial success of its accused products. *Id.* at 41. Petitioner, in fact, made the following stipulation in this proceeding:

> Samsung stipulates, solely for the purpose of, and for use in, this IPR proceeding, that the products accused of infringement in *Acorn Semi, LLC v. Samsung Electronics Co., Ltd. et al.*, No. 2:19-cv-00347-JRG (E.D. Tex.) have been commercially successful. Samsung disputes, however, that any commercial success achieved by the accused products is attributable, in any way, to the challenged claims of the Acorn patents

Ex. 2116, 2.

Further, the Patent Owner Response argues that infringement of the '395 patent is being tried in the Related Litigation and that the verdict that the jury would reach would likely establish infringement of the challenged claims, thus establishing that the accused products embody the claimed features and are coextensive with them. PO Resp. 38–41 (citing Ex. 1150 as evidence that the jury would address infringement of the '395[9] claims). Patent Owner argues that the nexus is also established by the purported facts that: (i) the primary advantage of the Acorn inventions is reduced contact

[9] Patent Owner expressly states that "the question of whether the accused products practice the Acorn patents, including this '691 Patent, will be conclusively answered." PO Resp. 40. This reference to the '691 patent was presumably a clerical error because the Petition challenges the '395 patent.

resistivity; (ii) there are billions of junctions in each accused product; (iii) reducing specific contact resistance provides significant technical benefits, and (iv) these benefits give chips that utilize Acorn's inventions a tangible market benefit. PO Resp. 42–43. Patent Owner argues the above features establish a nexus even for claims that do not recite reduced contact resistivity. *Id.* at 45.

After the Patent Owner Response was filed, the jury in the Related Litigation issued a verdict. Ex. 2121. The verdict, however, did not address alleged infringement of claim 4 and thus did not establish any presumption of nexus between any commercial success of accused products and claim 4. *Id.* at 4. As for Patent Owner's additional arguments regarding a nexus, claim 4 does not recite any specific contact resistance, and Patent Owner has not shown that lower specific contact resistivity is the "direct result of the unique characteristics of the claimed invention" of claim 4. Ex. 1101, 1:45–61; PO Resp. 45–46. Patent Owner does not specifically address claim 4. PO Resp. 45–46, 60. Instead, Patent Owner merely cites Figure 8 of the '395 patent and quotes Dr. Kuhn's testimony that:

> [T]he key enabling disclosure of the Acorn Patents is Figure 8 . . . This figure sets forth the key idea that was not in the prior art, and upon which the asserted claims of the Acorn Patents are based. This counter-intuitive idea is clearly expressed in the abstract as []The interface layer thickness corresponding to this minimum specific contact resistance . . .

Id. at 45 (quoting Ex. 2070, Kuhn Decl. ¶¶ 50–51) (alterations original). This testimony, however, does not address the accused products or claim 4. It merely addresses Figure 8 of the '395 patent, which itself is merely an illustrative drawing and not one that provides any experimental data. Ex. 2070, Kuhn Decl. ¶ 75 ("Figure 8 is clearly intended to be illustrative of

the overall physics, *not* to be predictive of any exact values of resistivity." (emphasis original)). Also, for the additional reasons discussed in Section III.B.2.b.3 below, Patent Owner does not establish a nexus for objective indicia of nonobviousness with respect to a reduction in contact resistance. Thus, Patent Owner has not established a nexus between the accused products and claim 4. Accordingly, we accord little weight to Patent Owner's evidence of the commercial success of the accused products.

2. Time Lag

According to Patent Owner, although Goodnick and Taubenblatt 1982 were available in prominent journals for over 20 years, the inability of others to produce the claimed invention during that time "is consistent with the fact that those references do not, in fact, actually suggest the claimed invention." PO Resp. 31. Patent Owner cites *Leo Pharmaceutical Products, Ltd. v. Rea*, 726 F.3d 1346, 1356–57, 1359 (Fed. Cir. 2013) for the proposition that the length of intervening time between the cited references and patent at issue "speaks volumes to the nonobviousness" of the invention. *Id.* Petitioner disagrees, citing *Iron Grip Barbell Co. v. USA Sports, Inc.*, 392 F.3d 1317, 1325 (Fed. Cir. 2004), for the proposition that "[a]bsent a showing of long-felt need or the failure of others, the mere passage of time without the claimed invention is not evidence of nonobviousness." Pet. Reply 30.

The holdings of *Leo Pharmaceutical* and *Iron Grip Barbell* are consistent. In *Leo Pharmaceutical*, "[t]he record [] showed evidence of *long* felt but unsolved need." 726 F.3d at 1359 (emphasis original). Thus, "the intervening time between the prior art's teaching of the components and the eventual preparation of a successful composition" constituted objective evidence of non-obviousness. *Id.* Absent a showing of long-felt need or the failure of others, however, the mere passage of time without the claimed

invention is not evidence of nonobviousness. *Iron Grip Barbell Co.*, 392 F.3d at 1325; *see also Nike v. Adidas AG*, 812 F.3d 1326, 1338 (Fed. Cir. 2016) ("[O]ur decision in *Leo Pharmaceutical* is entirely consistent with established precedent that '[t]he mere age of the references is not persuasive of the unobviousness of the combination of their teachings, absent evidence that, notwithstanding knowledge of the references, the art tried and failed to solve the problem.'"), *overruled on other grounds by Aqua Prods., Inc. v. Matal*, 872 F.3d 1290, 1296 n.1 (Fed. Cir. 2017) (en banc); *In re Wright*, 569 F.2d 1124, 1127 (CCPA 1977). Thus, whether the passage of time between Goodnick's and Taubenblatt 1982's publications and the effective filing date of the '395 patent constitutes objective evidence of nonobviousness depends on the evidence of a long-felt need or failure of others, which we address next.

3. Long Felt Need

Patent Owner argues that the claimed invention addressed a need long and prominently felt in the semiconductor industry of reducing contact resistance. PO Resp. 31–32. Patent Owner, however, does not demonstrate any nexus between the alleged satisfaction of that need and any limitation or combination of limitations that is novel in claim 4.

"Where the offered secondary consideration actually results from something other than what is both claimed and *novel* in the claim, there is no nexus to the merits of the claimed invention," meaning that "there must be a nexus to some aspect of the claim not already in the prior art." *In re Kao*, 639 F.3d 1057, 1068–69 (Fed. Cir. 2011). On the other hand, there is no requirement that "objective evidence must be tied exclusively to claim elements that are not disclosed in a particular prior art reference in order for that evidence to carry substantial weight." *WBIP, LLC v. Kohler Co.*, 829

F.3d 1317, 1331 (Fed. Cir. 2016). A novel combination of limitations would also suffice. *Id.*

As set forth in Section III.A.2. above, Goodnick discloses all limitations of claim 1. Claim 4 recites the electrical junction of claim 1, "wherein said region in the semiconductor substrate comprises a source or drain of a transistor." Ex. 1101, 18:59–61. Patent Owner has not argued or offered any evidence that this additional limitation of claim 4 by itself or in combination with the limitations recited in claim 1 lowers contact resistance. PO Resp. 32–34 (and the exhibits cited therein); PO Sur-reply 23–24. Thus, Patent Owner has not established any nexus between the purported satisfaction of long felt need and any novel aspect of claim 4.

Further, Patent Owner attributes the reduction of contact resistance to the allegedly counter-intuitive idea to add an insulating layer in a contact to reduce contact resistance. PO Resp. 33. Although Patent Owner offers evidence that certain individuals in the field indicated this concept was counter-intuitive and further offered the testimony of Dr. Kuhn that it was counter-intuitive, Dr. Schubert's testimony that Iwaguro discloses this concept stands unrebutted. Ex. 1126, Schubert Decl. ¶ 55–59. Further, Dr. Kuhn did not consider Iwaguro before providing her declaration testimony. Ex. 1170, Kuhn Dep. Tr. 235:9–16, 237:19–24, 254:4–9. And there is no evidence that any of the other individuals quoted by Patent Owner had considered Iwaguro's teachings before making their quoted statements. In the Sur-reply, Patent Owner contends via attorney argument that Iwaguro's teachings are only marginally relevant to the claimed invention. Sur-reply 22–23. Attorney argument, however, is not evidence. Patent Owner had the opportunity to have its expert address Dr. Schubert's contrary testimony, which was submitted with the Petition, but Patent Owner

did not. Pet. 12–13 (citing Ex. 1126, Schubert Decl. ¶¶ 50–63); Ex. 1170, Kuhn Dep. Tr. 235:9–16, 237:19–24, 254:4–9. We credit Dr. Schubert's testimony regarding Iwaguro. Ex. 1126, Schubert Decl. ¶ 55–59.

Further, Patent Owner argues Iwaguro is only marginally relevant because it does not disclose the claimed invention and was not used to challenge any claim. Sur-reply 22–23. A prior art disclosure does not, however, need to disclose every claim element or even most claim elements to be relevant to the issues of objective evidence of nonobviousness. A prior art reference can be relevant because, like Iwaguro, it can demonstrate that the alleged indicia of obviousness results solely from an aspect of the claim that is not novel. *Kao*, 639 F.3d at 1068–69.

Patent Owner also does not address the full scope of claim 1 or claim 4. *Id.* at 31–32, 45–46. Patent Owner merely cites Figure 8 of the '395 patent and quotes certain testimony by Dr. Kuhn and Dr. Clifton. *Id.* at 45 (citing Ex. 1101, Fig. 8; Ex. 2070, Kuhn Decl. ¶¶ 50–51, Ex. 2090, Clifton Decl. ¶¶ 9–14). That testimony, however, does not address claim 4. Ex. 2070, Kuhn Decl. ¶¶ 50–51; Ex. 2090, Clifton Decl. ¶¶ 9–14. Instead, the testimony by Dr. Kuhn merely addresses an illustrative drawing provided in the patent (Figure 8) without providing any evidence that that illustrative drawing is indicative of a property comprising the full scope of claim 1 or claim 4. Ex. 2070, Kuhn Decl. ¶¶ 50–51. Further, the testimony by Dr. Clifton does not address specific contact resistivity and claim 1 or claim 4. Ex. 2090, Clifton Decl. ¶¶ 9–14.

In sum, we determine that Patent Owner has not shown a requisite nexus between the purported long felt need and claim 4. Thus, we accord little weight to its evidence of long felt need and thus little weight to the

passage of time between Goodnick's and Taubenblatt 1982's publications and the effective filing date of the '395 patent.[10]

4. Unexpected results

As mentioned, Patent Owner argues that the "inventors had the counter-intuitive idea to intentionally introduce . . . . an insulating layer in [a] contact in order to reduce the contact resistance." PO Resp. 33–34 (citing Ex. 2095, 2928; Ex. 2096, 3; Ex. 2097, 5, Ex. 2070, Kuhn Decl. ¶ 49). As discussed in Section III.B.2.b.3 above, Patent Owner has not demonstrated any nexus between this alleged reduction in contact resistance and any limitation or combination of limitations that is novel in claim 4. Further, as discussed above, Dr. Schubert's testimony regarding Iwaguro stands unrebutted. Ex. 1126 ¶ 55–59. As discussed above, Patent Owner also does not address the full scope of claim 1 or claim 4 with respect to contact resistance. Thus, we accord little weight to Patent Owner's evidence of unexpected results.

5. Industry praise

Patent Owner notes that in 2004 and 2006, the inventors published two papers (Exs. 2045, 2046 (collectively, "the Connelly Papers")) that have been cited over 270 times in the professional literature. PO Resp. 34. On this record, however, Patent Owner has not demonstrated a sufficient nexus between any praise for these papers and specific limitations of claim 4. *Id.* Patent Owner does not identify how the structures described in those papers relate to claim 4. *Id.* Further, Petitioner provides evidence of the contrary. Pet. Reply 30. Claim 4, via its dependency from claim 1, recites a structure comprising a metal oxide layer. Ex. 1101, 1:45–61. The Connolly papers

[10] Patent Owner does not separately argue that there was any failure by others. PO Resp. 30–51.

disclose only a silicon nitride interface layer, which is not a metal oxide interface layer. Ex. 1171, 172:2–10, 175:19–25; Ex. 1173, Schubert Reply Decl. ¶ 139. Thus, we accord little weight to Patent Owner's evidence of industry praise.

6. Alleged suspicious behavior

Patent Owner alleges that, in an abstract in 2017, Petitioner's researchers cited the Connelly papers as a basis for their work, but removed the citation when the paper was published in full in 2018. *See* PO Resp. 47–51 (citing Ex. 2047, 1; Ex. 2048, 4879). According to Patent Owner, Petitioner's abstract focused on how contact resistance limits performance in scaling silicon MOSFETs and states that, instead of increased doping, the researchers studied an alternate option, i.e. a metal-interface-semiconductor (MIS) structure that mirrors the challenged independent claims. *Id.* at 48. Patent Owner states that the paper published by Petitioner's researchers in 2018 that did not cite the Connelly Papers "describes in positive terms reducing ρ_c, reducing the height of the Schottky barrier, depinning the Fermi level, and tuning the SBH (Schottky barrier height) between a low work-function metal and n-type silicon." *Id.* at 49.

Patent Owner also alleges that Petitioner filed its own patent applications based on Patent Owner's technology. PO Resp. 49–51 (arguing that a graph showing the thickness of the insulating mater and contact resistivity in Petitioner's patent is similar to a graph showing oxide thickness and specific contact resistance in Patent Owner's patents). Patent Owner further argues that U.S. Patent Publication No. 2014/0183434 A1 (Ex. 2100) ("Petitioner's '434 publication") was filed by Petitioner and claim 6 of that application is similar to claims 1 and 20 of Patent Owner's U.S. Patent 9,905,691 ("'691 patent"). PO Resp. 50–51. Patent Owner also argues that

various descriptions in Petitioner's applications are similar to the descriptions in the '691 patent. *Id.*

Regarding its researchers' papers, Petitioner contends that "[o]mitting a citation when there is no longer relevant information in a paper is *not* evidence of any suspicious behavior—it is what authors routinely do" and "even Dr. Kuhn did not cite to the Connelly Papers in her related work," even though she was aware of the Connelly Papers. Pet. Reply 30 (citing Ex. 1169, Kuhn Tr., 34:4–23). Petitioner further argues that the graph at issue in its researchers' papers "merely presents what was known in the literature long before [Patent Owner's] patents." *Id.* at 31.

The parties cite no Federal Circuit precedent where alleged suspicious behavior is objective criteria of nonobviousness. PO Resp. 47–51; Pet. Reply 31–34. Patent Owner further provides no testimony concerning the motivations of the authors of the abstract or the published paper, and we make no inferences from the difference in the citations concerning the Connelly Papers. PO Resp. 47–51.

Further, Patent Owner has not shown that any of the claims of the applications filed by Petitioner are similar to claim 4. PO Resp. 49–51. Patent Owner compares claim 6 of Petitioner's '434 publication to claims 1 and 20 of '691 patent, but no makes no comparison to claim 4 or any other challenged claim in the '395 patent. *Id.* at 50–51. Thus, no nexus has been established between the filing of claim 6 of the '434 publication and any issues of patentability concerning challenged claim 4. Further, the fact that there may be an overlap in certain descriptions in the specifications of the cited applications by Petitioner and the '691 patent is of no significance unless that overlap is tied to the invention of claim 4, and there is no evidence of such a tie. *Id.* at 49–51.

7. Summary

In consideration of the above, we accord little weight to Patent Owner's evidence of objective indicia of nonobviousness.

c. Conclusion Regarding Claim 4

After reviewing the record, including the evidence presented regarding objective indicia of nonobviousness, we determine that Petitioner has proven the claim 4 would have been obvious over Goodnick and Jammy.

C. Ground 3: Asserted Obviousness over Goodnick

Petitioner asserts that claim 5 would have been obvious over Goodnick. Pet. 9. Petitioner sets forth its evidence and arguments that the combination of Goodnick teaches or suggests every element of claim 5. Pet. 29–34. In response, Patent Owner relies on the argument it presented for claim 1, that Goodnick does not disclose distinct metal oxide and semiconductor oxide layers. PO Resp. 60. As set forth in Section III.A.2.f above, we found that Petitioner has proven that Goodnick discloses distinct metal oxide and semiconductor oxide layers.

Patent Owner further argues that objective indicia of nonobviousness support a determination of nonobviousness of claim 5. PO Resp. 30–51. For claim 5, the parties present the same arguments and evidence regarding objective evidence of nonobviousness as for claim 4. *Id.*; Pet. Reply 25–34.

Our analysis of objective evidence of nonobviousness for claim 5 is essentially the same as for claim 4. As with claim 4, the jury verdict in the Related Litigation does not give rise to a presumption of nexus between the commercial success of the products found to infringe in the Related Litigation and claim 5 because the jury verdict does not address whether claim 5 is infringed. Ex. 2121, 2. For essentially the same reasons discussed for claim 4, Patent Owner does not establish a nexus between the

commercial success, alleged long felt need, alleged unexpected results, and alleged industry praise and claim 5 (i.e., none of its evidence and arguments are tied to claim 5). PO Resp. 30–51.

One difference regarding the analysis of objective evidence of nonobviousness between claims 4 and 5 is that the limitation of claim 5 adds to claim 1 and that Goodnick does not teach is different than for claim 4. In particular, Goodnick suggests, but does not teach, the following limitation in claim 5: "yet thin enough to provide the junction with a specific contact resistivity that is generally dependent on: a workfunction of the metal electrical contact, a Fermi energy of the semiconductor in the region, or both the workfunction of the metal electrical contact and the Fermi energy of the semiconductor in the region." Ex. 1126, Schubert Decl. ¶ 184. Patent Owner, however, does not tie this limitation in isolation or in combination with other limitations to the reduction in specific contact resistance that purportedly gives rise to the purported unexpected results, satisfaction of long felt need, or commercial success. PO Resp. 31–34 (and the exhibits cited therein). Further, for the other reasons discussed for claim 4, Patent Owner does not establish a nexus between the commercial success of the accused products, alleged long felt need, alleged unexpected results, and alleged industry praise and claim 5 (i.e., none of its evidence and arguments are tied to claim 5). PO Resp. 30–51; PO Sur-reply 23–25.

Similarly, Patent Owner does not establish a nexus between any claim of Petitioner's '434 publication and claim 5. *Id.* Nor has Patent Owner tied any of the alleged common disclosures between Petitioner's '434 publication and other cited applications by Petitioner and claim 5. *Id.* Thus, for the reasons explained in Section III.B.2.b above, we accord little weight to that evidence of objective indicia of nonobviousness for claim 5.

After reviewing the evidence of record, we determine that Petitioner has proven that claim 5 would have been obvious over Goodnick.

D. Ground 4: Asserted Obviousness over Goodnick and Taubenblatt 1982

Petitioner asserts that claims 1, 11, 12, 15, 23–25, and 28 would have been obvious over Goodnick and Taubenblatt 1982. Pet. 10.

1. Taubenblatt 1982

Noting the importance of silicides as Schottky barriers, ohmic contacts, and low resistivity interconnects in integrated circuits, Taubenblatt 1982 states that "[m]any silicides are commonly formed by the deposition of a metal layer on silicon via e-beam evaporation, chemical vapor deposition, or sputtering, and the reaction of the metal layer with the underlying silicon at 400-600 °C." Ex. 1123, 1.[11] The purpose of Taubenblatt 1982 was "to characterize silicide formation for the Ti-Si system under ultrahigh vacuum (UHV) conditions with the controlled addition of surface oxides." *Id.* Taubenblatt 1982's "results show that the presence of SiO_2 at the Si surface, prior to Ti deposition, has a significant effect on the reaction of Ti and Si and that the thickness of the SiO_2 layer is especially important in determining the reaction end products." *Id.* at 8. According to Taubenblatt 1982:

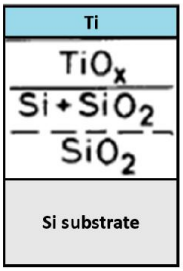
> in the manufacture of circuit elements employing titanium disilicide, Ti will react through a thin silicon dioxide layer with the SiO_2 remaining at the surface. But in the reaction of Ti with a thicker SiO_2 layer, Ti oxide forms, which can act as a diffusion barrier to prevent further reduction of the oxide by unreacted Ti metal or in the formation of silicide.

Id.

[11] We cite to the pages added by Petitioner for this exhibit.

2. Proposed Combination of Goodnick and Taubenblatt 1982

Petitioner argues that Goodnick discloses an interface layer that includes a metal oxide layer (aluminum oxide (Al_2O_3)), but acknowledges that Goodnick does not expressly describe an interface layer that includes titanium dioxide, as recited in claims 11 and 23, or a metal electrical contact that includes titanium, as recited in claims 15 and 24. Pet. 34. Petitioner asserts, however, that, because Taubenblatt 1982 teaches (i) depositing titanium on a layer of SiO_2 thicker than 20 Å (2 nm) and (ii) that annealing at temperatures between 700ºC–900ºC forms a TiO_x–SiO_2 interface layer, an ordinarily skilled artisan would have understood that by depositing titanium on Goodnick's 30 Å (3 nm) thick layer of thermally grown SiO_2, "all that it would have taken to form a TiO_x–SiO_2 interface layer is annealing at 700C–900C as described in Taubenblatt 1982." *Id.* at 36 (citing Ex. 1123, 7–8, Ex. 1126, Schubert Decl. ¶ 203). Petitioner contends that the combined teachings of Goodnick and Taubenblatt 1982 would have resulted in the structure shown below.



Pet. 36–37 (citing Ex. 1121, Goodnick, 1–2; Ex. 1123, 7–8; Ex. 1126, Schubert Decl. ¶ 204). The structure postulated by Petitioner includes a SiO_2 layer on top of a silicon substrate, a Si+SiO_2 layer over the SiO_2 layer, a TiO_x layer on top of the Si+SiO_2 layer, and a Ti layer over the TiO_x layer. *Id.* at 37.

3. Motivation to Combine Goodnick and Taubenblatt 1982

a. Parties' Arguments

According to Petitioner, an ordinarily skilled artisan would have had reason to provide Goodnick with an interface layer that includes both titanium oxide and silicon dioxide "because that interface layer would have been expected to reduce the specific contact resistivity of that junction." Pet. 37 (citing, e.g., Ex. 1126, Schubert Decl. ¶¶ 205–206). Petitioner argues that it was known that a SiO_2 interface layer grown on silicon would passivate the surface of the silicon and "[t]hat passivation would have reduced the barrier height of a titanium to n-type silicon junction, such as the junction between Taubenblatt 1982's titanium and Goodnick's n-type source drain/drain silicon substrate." *Id.* at 37–38 (citing Ex. 1121, Goodnick, 31; Ex. 1123, Taubenblatt 1982, 1–2; Ex. 1126, Schubert Decl. ¶ 207). Petitioner further states that, "[f]or a junction between titanium and n-type silicon with a SiO_2 interface layer, the SiO_2 interface layer reduces the barrier height more than 0.1 eV" and that "reducing the barrier height of a junction reduces its specific contact resistivity." *Id.* at 38 (citing Ex. 1126, Schubert Decl. ¶ 207; Ex. 1124, Chang,[12] 5–6).

In summarizing what would have been known to an ordinarily skilled artisan at the relevant time, Petitioner's expert, Dr. Schubert, cites another Taubenblatt reference, i.e., Taubenblatt 1984[13]. Ex. 1126, Schubert Decl. ¶ 54 (citing Ex. 1130, 3). Dr. Schubert cites a passage in Taubenblatt 1984

[12] Chang is not an asserted reference for this ground, but is an asserted reference for Ground 6.

[13] M.A. Taubenblatt et al., *Interface effects in titanium and hafnium Schottky barriers on silicon*, 44 APPLIED PHYS. LETTERS 895 (Ex. 1130, "Taubenblatt 1984").

that references teachings in Turner and Rhoderick[14] as disclosing that an interfacial oxide reduces the pinning ability of the interface states in silicon, so that the barrier behaves more like an ideal Schottky barrier. Ex. 1126, Schubert Decl. ¶ 54 (citing Ex. 1130, 3). Dr. Schubert also testifies, "it was well known before 2002 that interposing an interface layer between a metal and a semiconductor at a metal-semiconductor junction could reduce specific contact resistance." *Id.* ¶ 55; *see also id.* ¶ 56 (asserting Schroen[15] (abstract), discloses the specific contact resistance obtained by using a thin insulating interfacial layer between a metal and a semiconductor is far smaller than the resistance observed in a structure of only a semiconductor and a metallization layer), *id.* ¶ 59 (quoting Iwaguro[16] ¶ 6, which states "[b]y bringing a metal film into contact with this sub-silicon oxide film, an ohmic junction exhibiting favorable low contact resistance can be obtained").

As to the use of titanium, Dr. Schubert cites a 1989 patent by Kim[17] (Ex. 1125) as describing an interface layer formed by titanium reducing silicon dioxide to achieve a specific contact resistance as low as 8 Ω-μm^2. Ex. 1126, Schubert Decl. ¶¶ 57–58 (citing Ex. 1125, 5:27–30). In the Decision to Institute, we noted that Kim discloses the use of an alloy of tungsten and titanium, and specifically identifies disadvantages to the use of titanium alone. Dec to Inst. 32 (citing Ex. 1125, 1:24–30).

Noting that Goodnick does not mention resistivity and Taubenblatt 1982 mentions resistivity only once, the Patent Owner Response contends

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[14] Ex. 1123, n.18 (citing M. J. Turner and E. H. Rhoderick, Solid State Electron. II, 291, (1968)); *see also* Ex. 1117, n.1.
[15] U.S. Patent No. 3,983,264 (Ex. 1124, "Schroen").
[16] Certified Translation of Japanese Laid-Open App. No. JPH11162874A (June 18, 1999) (Ex. 1133, "Iwaguro").
[17] U.S. Patent No. 4,845,050 (Ex. 1125, "Kim").

that an ordinarily skilled artisan would not have been motivated to combine the teachings of Goodnick and Taubenblatt 1982 in the manner proposed by Petitioner. PO Resp. 8–9. Patent Owner emphasizes that Goodnick "presents experimental results of research into the effects of a layer of silicon dioxide between silicon and three metals (gold, platinum, and aluminum), none of which is titanium," that Taubenblatt 1982 "reports the results of several experiments depositing titanium on silicon under various conditions," and that neither reference is concerned with building a low resistance junction. *Id.* at 9. Patent Owner further argues that "[n]othing in Goodnick suggests any reason to study titanium" and "[n]othing in Taubenblatt suggests studying aluminum." *Id.*

According to Patent Owner, Petitioner's reference to the teachings in other documents, such as Kim, is unavailing because the Petition fails to establish a link between the subject matter cited by Dr. Schubert and his assertion that an ordinarily skilled artisan would have substituted Taubenblatt 1982's titanium for Goodnick's aluminum. PO Resp. 10.

Patent Owner argues that the bulk resistivity of titanium is about sixteen times that of aluminum, suggesting that a person of ordinary skill would not have looked to replace aluminum with titanium. PO Resp. 11 (citing Ex. 2052, 4, 6; Ex. 2081, 1–2, 12; Ex. 2082, 1–2; Ex. 2083). Patent Owner asserts that Dr. Schubert tried to downplay this difference by testifying that the resistivity of the metal in the metal-insulator-semiconductor stack is insignificant when compared to the much larger resistivity of insulators and semiconductors. *Id.* at 12 (citing Ex. 2076, Transcript of Deposition of Dr. Schubert ("Schubert Tr."), 65:21–67:9)). Patent Owner, however, argues that the bulk resistivity of an insulator is irrelevant when it is used as a tunneling interface layer, i.e., because

tunneling is a property of the barrier height at the junction and the physical thickness, not the material's bulk resistivity. *Id.* (citing Ex. 2070, Declaration of Dr. Kelin Kuhn ("Kuhn Decl.") ¶ 117). According to Dr. Kuhn,

> [I]t is not correct to say that a POSITA would ignore the bulk resistivity of the metal in a metal - insulator semiconductor stack of the type of interest here. That is especially true if the choice is between aluminum and titanium because, as I mentioned, aluminum is a significantly better electrical conductor than titanium (by a factor of about 16X).

Ex. 2070, Kuhn Decl. ¶ 120. In addition, Dr. Kuhn testifies that "considerable research in the semiconductor industry has been (and currently is) conducted to try to find conductors that have marginally lower resistivity." *Id.* ¶ 119. As a result, Patent Owner argues that the bulk resistivity of the metal is a factor an ordinarily skilled artisan would consider when trying to reduce resistance in the pertinent structure. PO Resp. 13.

Petitioner's Reply counters that reducing specific contact resistance in a junction had well known benefits including reducing power consumption. Pet. Reply 9 (citing Ex. 1126, Schubert Decl. ¶ 215). Petitioner also argues that Patent Owner fails to consider the resistivity of the entire structure, not just the metal layer. *Id.* at 10 (citing Ex. 1173, Schubert Reply Decl. ¶ 112). Petitioner notes that "[t]he proposed combination substitutes the Al-Al_2O_3 (in Goodnick) for Ti-TiO_x (in the proposed combination) (with the SiO_2 and Si layers the same in both structures)." *Id.* Petitioner argues that the semiconductor's bulk resistivity far outweighs the bulk resistivity of the metal layer, regardless of whether aluminum or titanium is used in the metal layer, and notes that, because the bulk resistivity of the semiconductor is largely fixed based on the doping concentration, the contributions from the

SiO_2-Si would be similar in both structures. *Id.* at 10–11. According to Petitioner, "that is precisely why a POSITA would have sought other means for reducing the junction's *overall* resistivity, such as by reducing the resistivity of the interface layer by substituting TiO_2 for Goodnick's higher-resistivity Al_2O_3 layer." *Id.* at 11 (citing Ex. 1173, Schubert Reply Decl. ¶¶ 107–108 (emphasis original)).

According to Petitioner, TiO_x is substantially more conductive than Al_2O_3 because current can flow through TiO_x via electron tunneling and via conduction bands, but in the case of Al_2O_3, the tunneling barrier is higher, and current does not flow through Al_2O_3's conduction bands. Pet. Reply 11–12 (citing Ex. 1173, Schubert Reply Decl. ¶¶ 109–111).

Patent Owner's Sur-reply argues that Petitioner has not proven that its proposed Ti-TiO_x-SiO_2-Si structure has lower resistance than Goodnick's Al-Al_2O_3-SiO_2-Si structure. PO Sur-reply 8–15. Patent Owner argues that the doped silicon used in the semiconductor industry does not have a bulk resistivity that is ten billion times greater than a metal. *Id.* at 8–9. Patent Owner also argues that Petitioner fails to account for the geometry of the materials used. *Id.* at 9–10. Further, Patent Owner asserts that the tunneling probability through TiO_x is not thirty times greater than that of Al_2O_3. *Id.* at 10–11. Patent Owner further argues that Petitioner does not quantify the conduction-band and thermionic current compared to the tunneling current. *Id.* at 12. Patent Owner also argues that Petitioner fails to account for the height of a metal layer. *Id.* at 13. Further, Patent Owner asserts that titanium is 16x more resistive to aluminum, whereas the tunneling probability of TiO2 is only 1.66 times more. *Id.* at 14–15. Patent Owner asserts that thus an ordinarily skilled artisan would not have been motivated

to substitute titanium for aluminum. *Id.* at 15. Patent Owner also argues that Petitioner's reply arguments were belated. *Id.*

Patent Owner also argues that thermal expansion concerns teach away from both aluminum and titanium. PO Sur-reply 16–17.

b. Analysis

We determine that Petitioner has not proven that an ordinarily skilled artisan would have been motivated to make the proposed combination. Petitioner argues that an ordinarily skilled artisan would have been motivated to substitute Al-Al_2O_3 (in Goodnick) for Ti-TiO_x (in the proposed combination) (with the SiO_2 and Si layers the same in both structures) to reduce specific contact resistance. Pet. 37. Petitioner cites nothing from Goodnick that suggests using titanium and cites nothing from Taubenblatt 1982 that suggests substituting titanium for aluminum. *Id.* at 37–40; Pet. Reply 9–17. Petitioner also cites nothing from either reference suggesting that Ti-TiO_x would have produced a better specific contact resistance than Al-Al_2O_3. Pet. 37–40; Pet. Reply 9–17. Petitioner cites Kim as supporting its proposed combination (Pet. 37–39, citing Kim 4:63–5:1), but Kim discloses that pure titanium is not suitable for contacts, which teaches away from the proposed combination:

> Pure titanium, however, is not suitable for contacts as direct contact between titanium and silicon has shown poor reproducibility due to the large difference in the linear thermal coefficient of expansions of titanium and silicon (the linear coefficient of expansion of titanium being three times the linear coefficient of expansion of silicon).

Ex. 1125, 1:24–30.

Addressing Patent Owner's arguments regarding this passage in Kim, Petitioner argues that thermal coefficients support its proposed substitution

because titanium has a better thermal coefficient match with silicon than aluminum. Pet. Reply 15–16 (citing PO Resp. 14–15). In making this contention, Petitioner does not specifically address Kim's disclosure. *Id.* The above passage from Kim directly follows a discussion of the use of aluminum as a contact metal. Ex. 1125, 1:14–23. Kim then notes an advantage of titanium: it is a good agent for reducing silicon dioxide. *Id.* at 1:23–24. But then Kim teaches that pure titanium is not suitable for contacts due to the large difference in the linear thermal coefficient of expansions of titanium and silicon. *Id.* at 1:24–30. In light of these teachings, an ordinarily skilled artisan would not read Kim as supporting the use of pure titanium in place of aluminum due to titanium's thermal coefficients. Rather, an ordinarily skilled artisan would recognize that Kim teaches that, instead of pure titanium or aluminum, an ordinarily skilled artisan should use an alloy of titanium and tungsten with a metal selected from the group of molybdenum and tungsten. *Id.* at 1:31–41, 2:32–35, 5:2–5 ("Alloys in the range of about 10% to 40% by weight of titanium and the remainder tungsten are particularly suitable for providing low resistance contacts to silicon."). Such an alloy, however, is not part of Petitioner's proposed combination for Ground 4. Pet. 36–37.

Petitioner argues that Kim addresses a direct contact between titanium and silicon, whereas Petitioner's proposed combination has an intervening layer of TiO_x and thus Kim teaches away from pure titanium and is inapplicable to Petitioner's proposed combination. Pet. Reply 16 n.1. Petitioner cites no expert testimony to support its contention that Kim only teaches away from direct contact between titanium and silicon. *Id.* We read Kim's teachings more broadly. Kim states that "[p]ure titanium [] is not suitable for contacts." Ex. 1125, 1:24–30. Although Kim mentions that

direct contact between titanium and silicon shows poor reproducibility, Kim does not limit its teaching away from pure titanium to structures with direct contact and does not suggest that an intervening layer would make pure titanium suitable for contacts. *Id.* Instead, Kim teaches that certain alloys should be used in place of pure titanium. *Id.* at 1:31–41, 2:32–35, 5:2–5. Further, Petitioner's contention that the intervening layer would make pure titanium suitable for contacts, based on Kim's teachings, rests solely on attorney argument, which is not persuasive. Pet. Reply 16 n.1.

Petitioner presents testimony by Dr. Schubert to demonstrate that TiO_x in the proposed combination would be less resistive than Al_2O_3. Pet. Reply 11. Dr. Schubert does not dispute that the bulk resistivity of titanium is about sixteen times greater than the bulk resistivity of aluminum. Ex. 1173, Schubert Reply Decl. ¶ 107. But Dr. Schubert testifies that:

> even if the bulk resistivity of titanium is 16 times greater than the bulk resistivity of aluminum, Goodnick and Taubenblatt 1982's Ti–TiO_x–SiO_2–Si contact as a whole provides reduced resistivity based on at least: (1) the thirty-fold increase in tunneling probability at the Ti–TiO_2 interface as compared to the Al–Al_2O_3 interface; and (2) the lower barrier height of the Ti–TiO_2 interface allowing for current transport by means of thermionic emission.

Id. ¶ 112 (emphasis omitted). Dr. Schubert, however, has not provided any calculations or estimates for the resistivity or resistance differences that result from the increase in tunneling probability or lower barrier height. *Id.* ¶¶ 103–113. Dr. Schubert merely concludes that the Ti–TiO_x–SiO_2–Si contact has reduced resistivity because the tunneling probability and lower barrier height for Ti–TiO_x would outweigh titanium's increased resistivity without providing any evidence or calculations to support that assertion. *Id.* The absence of supporting calculations or other evidence to support his

testimony that the tunneling probability and lower barrier height would outweigh the increase bulk resistivity of titanium undermines that testimony.

Dr. Kuhn provides an illustrative example demonstrating how the resistance of a contact would differ for Ti and Al. Ex. 2070, Kuhn Decl. ¶ 119. In Dr. Kuhn's example, the resistance due to the metal for the contact was calculated to be 12.5 Ω for aluminum and 201.6 Ω for titanium. *Id.* Dr. Schubert has not disputed these calculations. Ex. 1173, Schubert Reply Decl. ¶¶ 103–113. Further, Dr. Schubert presents no calculations or estimates showing how in that example or in any other example the differences due to the change in tunneling probability or lower barrier height at the interface would outweigh the difference in resistance in the contact metal. *Id.* For instance, for Dr. Kuhn's example, Dr. Schubert does not set forth how the difference in resistance due to the increase in tunneling probability and the lowering of the barrier height with the Ti–TiO_x interface would outweigh the 189.1 Ω (201.6 Ω – 12.5 Ω) increase in resistance due to the metal in the contact. *Id.* Dr. Schubert provides no estimate for how the resistance of the junction would change due to the increase in tunneling probability and the lowering of the barrier height. *Id.*

Even if we were to assume that the thirty-fold increase in tunneling probability at the Ti–TiO_2 interface were to result in a thirty-fold decrease in the contribution of resistance from the interface and the lower barrier height would also result in a significant difference (e.g., factor of ten), that would not necessarily mean that the differences in these contributions would outweigh the difference due to the contact metal. For example, if the Al–Al_2O_3 interface were to contribute 30 Ω resistance to the overall resistance of the junction and the increased tunneling probability for Ti–TiO_x would decrease that resistance by a factor of 30 and the lower barrier height would

decrease it by another factor of 10, the resistance contribution from the Ti–TiO_x junction would be 0.1 Ω (30 Ω x 1/30 x 1/10) versus 30 Ω with the aluminum structure. The decrease in resistance due to the Ti–TiO_x interface would be 29.9 Ω, but that would not outweigh the 189.1 Ω increase due to the increased resistance of Ti. Using this simple example with the same assumptions, however, one could arbitrarily pick numbers for the contributions for resistance from the interface where a decrease in the resistance at the interface would outweigh the increase in resistance due to the metal contact.[18] Without being provided any evidence of what the resistance difference between Ti–TiO_2 interface is as compared to the Al–Al_2O_3 interface, we cannot determine whether that decrease in resistivity at the interface would outweigh the increase in resistance at the metal contact nor can we determine whether an ordinarily skilled artisan would so recognize it. And Dr. Schubert's conclusory testimony that the resistance difference at the interface would outweigh the increase in resistance due to the metal contact is not persuasive, particularly when Dr. Schubert failed to account for metal contact resistance in his original analysis.[19] In sum, we

[18] This example is merely illustrative. For instance, it is based on mere assumptions as to how tunneling probabilities and decrease in barrier heights translate into changes in resistance. The example merely illustrates the fact that a thirty-times decrease in one effect (tunneling probability) and an unquantified difference in another effect (barrier height) does not necessarily mean such effect outweigh a sixteen-fold increase in resistance at the contact metal.

[19] Patent Owner disputes that the tunneling probability at the TiOx interface is 30 times greater than that of AlO_2. Sur-reply 10. Patent Owner argues that the electronic affinity for $Al0_2$ is 3.71 eV, rather than 3.28 eV that Dr. Schubert used in his calculations. *Id.* (citing Ex. 1143, 1190). Patent Owner further argues that, with a value of 3.71 eV, the tunneling probability

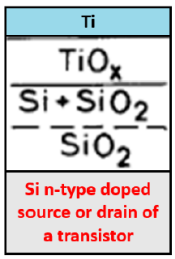
conclude that Petitioner has not proven that an ordinarily skilled artisan would have been motivated to make the proposed combination of Goodnick and Taubenblatt 1982. Thus, Petitioner has not proven that claim 1, 11, 12, 15, 23–25, and 28 would have been obvious over Goodnick and Taubenblatt 1982.[20] Pet. 10.

E. Ground 5: Asserted Obviousness over Goodnick, Jammy, and Taubenblatt 1982

Petitioner argues that claims 14, 17–19, and 22 would have been obvious over Goodnick, Jammy, and Taubenblatt 1982. Pet. 10.

1. Proposed Combination of Goodnick, Jammy, and Taubenblatt 1982

Petitioner proposes that an ordinarily skilled artisan would have (i) grown a 30 Å SiO_2 layer as taught in Goodnick on Jammy's n-type doped source or drain of a transistor in a silicon substrate, (ii) deposited Taubenblatt 1982's titanium on that 30 Å SiO_2 layer instead of Goodnick's aluminum; and (iii) annealed the resulting structure at 700ºC–900ºC as taught by Taubenblatt 1982. Pet. 49. According to Petitioner, this combination would have yielded the following structure:



for Al_2O_3 would be 1.66 times greater than TiO_2. *Id.* In light of our other findings, we do not need to resolve this dispute.

[20] As set forth in Section III.A.2, we determined that Goodnick anticipates claim 1.

Pet. 51. Petitioner describes the above structure as having a TiO_x – SiO_2 interface layer between a titanium metal electrical contact and exposed n-type source/drain diffusions in a silicon substrate. *Id.* at 50–51.

2. Motivation to Combine Goodnick, Jammy, Taubenblatt 1982

Petitioner asserts that an ordinarily skilled artisan would have combined Goodnick and Taubenblatt 1982 to make a Ti–TiO_x–Si+SO_2–SiO2–Si contact to reduce specific contact resistivity for the reasons expressed for Ground 4. Pet. 49. Petitioner further argues that, in addition, an ordinarily skilled artisan would have substituted Jammy's n-type silicon substrate for Goodnick's n-type silicon substrate because (i) that substitution would not have materially altered the Ti–TiO_x–Si+SO_2–SiO2–Si contact formed by combining Goodnick and Taubenblatt 1982 and (ii) it would be desirable for Jammy's structure to have a contact with low specific contact resistivity. *Id.* at 49–50.

As discussed in Section III.D.3.b above for Ground 4, we determined that Petitioner has not proven that an ordinarily skilled would have been motivated to combine Goodnick and Taubenblatt 1982 to reduce specific contact resistivity. Thus, Petitioner has not proven that an ordinarily skilled artisan would have been motivated to make the proposed combination of Goodnick, Jammy, and Taubenblatt 1982 for this ground. Accordingly, Petitioner has not proven that claims 14, 17–19, and 22 would have been obvious over Goodnick, Jammy, and Taubenblatt 1982.

F. Ground 6: Asserted Obviousness over Goodnick Jammy, Taubenblatt 1982, and Chang

Petitioner asserts that claim 6 would have been obvious over the combination of Goodnick, Jammy, Taubenblatt 1982, and Chang. Pet. 10.

1. Chang

Chang addresses the specific contact resistance of metal-semiconductor barriers. Ex. 1124, 1. Chang discloses that the specific contact resistance at zero bias, R_c, is important as a measure of the ohmic or rectifying behavior of a metal-semiconductor barrier under operating conditions, and Chang calculates R_c for metal-Si and metal-GaAs barriers on p-type and n-type samples. *Id.* According to Chang, R_c decreases exponentially with increasing temperatures and with decreasing barrier height. *Id.* Chang also states that, for higher dopings where tunneling dominates, R_c decreases rapidly with increased doping. *Id.*

2. Proposed Combination of Goodnick, Jammy, Taubenblatt 1982, and Chang and Motivation for the Combination

Petitioner relies on its arguments for Ground 5 that an ordinarily skilled artisan would have combined Goodnick, Jammy, and Taubenblatt 1982 to produce a Ti–TiO_x–Si+SO_2–SiO_2–Si structure. Pet. 57. Petitioner further argues that an ordinarily skilled artisan would have been motivated by Chang to provide a specific contact resistivity in that structure of less than 10 Ω-μm^2. *Id.*

As set forth in Section III.E.2 above, we determined that Petitioner has not proven that an ordinarily skilled artisan would have been motivated to combine Goodnick, Jammy, and Taubenblatt 1982 to produce a Ti–TiO_x–Si+SO_2–SiO_2–Si structure. Thus, Petitioner has not proven that an ordinarily skilled artisan would have been motivated to make the proposed combination of Goodnick, Jammy, Taubenblatt 1982, and Chang for this ground. Accordingly, Petitioner has not proven that claim 6 would have been obvious over the combination of Goodnick, Jammy, Taubenblatt 1982, and Chang.

G. Ground 7: Asserted Obviousness over Goodnick, Taubenblatt 1982, and Kim

Petitioner argues that claims 16, 26, and 27 would have been obvious over the combination of Goodnick, Taubenblatt 1982, and Kim. Pet. 10.

1. Kim

Kim is directed to a method of making molybdenum/titanium-tungsten or tungsten/titanium-tungsten ohmic contacts to silicon. Ex. 1125, 1:2–3. Kim generally describes a low resistance contact between a titanium-tungsten alloy and silicon. *Id.* at 4:59–5:4. Kim explains that the titanium in the tungsten-titanium alloy is believed to reduce native silicon dioxide present on the silicon to form silicon and titanium dioxide, which reduces the interface resistance. *Id.* at 4:63–5:4. Kim describes achieving a specific contact resistance from 8 to 15 Ω-μm^2 for a junction between that alloy and n-type doped silicon. *Id.* at 5:27–30.

2. Proposed Combination of Goodnick, Taubenblatt 1982, and Kim and Motivation to Combine

Petitioner relies on its arguments for Ground 4 that an ordinarily skilled artisan would have been motivated to combine Goodnick and Taubenblatt 1982 in the manner proposed for Ground 4. Pet. 61. Petitioner further argues that an ordinarily skilled artisan would have been motivated to substitute Kim's titanium tungsten alloy for Taubenblatt 1982's titanium. *Id.* at 62.

As set forth in Section III.D.3.b above, we determined that Petitioner has not proven that an ordinarily skilled artisan would have been motivated to combine Goodnick and Taubenblatt 1982 in the manner Petitioner proposes. Thus, Petitioner has not proven that an ordinarily skilled artisan would have been motivated to combine Goodnick, Taubenblatt 1982, and Kim for this ground. Accordingly, Petitioner has not proven that claims 16,

26, and 27 would have been obvious over Goodnick, Taubenblatt 1982, and Kim.

H. Ground 8: Asserted Obviousness over Goodnick, Jammy, Taubenblatt 1982, and Kim

Petitioner argues that claims 20 and 21 would have been obvious over Goodnick, Jammy, Taubenblatt 1982, and Kim. Pet. 10. For this ground, Petitioner relies on its argument for Ground 5 that an ordinarily skilled artisan would have been motivated to combine Goodnick, Jammy, and Taubenblatt 1982 in the manner proposed for Ground 5. Pet. 64. In addition, Petitioner argues that an ordinarily skilled artisan would have been motivated to substitute Kim's titanium tungsten alloy for Taubenblatt 1982's titanium. *Id.*

As set forth in Section III.E.2 above, we determined that Petitioner has not proven that an ordinarily skilled artisan would have been motivated to combine Goodnick, Jammy, and Taubenblatt 1982 in the manner Petitioner proposed for Ground 5. Thus, Petitioner has not proven that an ordinarily skilled artisan would have been motivated to combine Goodnick, Jammy, Taubenblatt 1982, and Kim for this ground. Therefore, Petitioner has not proven that claims 20 and 21 would have been obvious over Goodnick, Jammy, Taubenblatt 1982, and Kim.

IV. MOTIONS TO EXCLUDE

A. Patent Owner's Motion to Exclude

1. Goodnick Cross-Examination Testimony

Patent Owner moves to exclude testimony elicited on cross-examination of Dr. Goodnick concerning whether certain metal oxides fall within the scope of the challenged claims. PO Mot. to Excl. 1 (citing Ex. 1168, Transcript of Deposition of Dr. Stephen Goodnick ("Goodnick

Tr.") 65:20–66:17, 113:20–117:23, 137:17–141:10 (collectively, the "Goodnick metal-oxide testimony")). Patent Owner, however, acknowledges that Petitioner does not cite to any of the Goodnick-metal-oxide testimony in Petitioner's papers. *Id.* at 6. Patent Owner argues that, nevertheless, we should not deem the motion to exclude this testimony as moot because Petitioner should not be allowed to use this testimony in the Related Litigation. *Id.* Petitioner argues that we should not exclude the involved testimony. Opp. to PO Mot. Excl. 1.

The motion to exclude the Goodnick metal-oxide testimony is moot. Neither party cites that testimony in its papers, and we do not independently consider it. Regarding the Related Litigation, trial has already occurred, so no decision here would affect the admissibility at that trial. Further, it not within our purview to determine admissibility in the Related Litigation.

In consideration of the above, Patent Owner's motion to exclude the Goodnick-metal-oxide testimony is dismissed as moot.

2. Kuhn Cross-Examination Testimony

Patent Owner also moves to exclude testimony elicited on cross-examination of its expert, Dr. Kuhn, about claim limitations that recite an "oxide of titanium." PO Mot. To Excl. 7. Patent Owner asserts that "the 'oxide of titanium' limitation was not substantively addressed in this or any other IPR petition, and Dr. Kuhn never addressed it in her declaration (Ex. 2070)." *Id.* Petitioner argues that questions regarding the scope of that limitation were within the realm of proper cross-examination. Opp. To Pet. Mot. Excl. 7–8.

The motion to exclude the Kuhn testimony is also moot. Neither party has identified where either side has relied on the testimony at issue in this proceeding. Further, the dispositive issue for the grounds (4–8) that

address claims that recite an oxide of titanium (i.e., claims 11–14, 17–28) is Petitioner's failure to prove that an ordinarily skilled artisan would have been motivated to combine Goodnick and Taubenblatt 1982. *See* Section III.D–H above. The testimony at issue does not address Petitioner's proffered motivation for combining those references. Thus, the motion to exclude cross-examination testimony by Dr. Kuhn is also moot.

B. Petitioner's Motion to Exclude

Petitioner moves to exclude certain paragraphs of the direct testimony of Dr. Paul Clifton, i.e., paragraphs 8–15, 19–25, 36–45, 47–50, 52–63, 67, 69–70, 72, 76–77, and 81–107 of the Clifton Declaration, because "'during Dr. Clifton's deposition, it became clear that Acorn was offering Dr. Clifton only as a fact witness, not an expert witness' and, accordingly, it became apparent that the expert opinions offered in Dr. Clifton's declaration are improper." Pet. Mot. to Excl. 3. Patent Owner offered Dr. Clifton's testimony in support of its objective considerations arguments. *See* Section III.B.2.b.

Patent Owner contends that Petitioner misconstrues comments made by Patent Owner's counsel during Dr. Clifton's deposition indicating that Dr. Clifton was a fact witness, that Dr. Clifton testified as a hybrid fact-expert witness, that Petitioner failed to timely object to Dr. Clifton's testimony, and that Petitioner's motion is mostly moot because the objective indicia that was the subject of Dr. Clifton's testimony is established independently from the documentation in evidence. *See generally* Opp. to Pet. Mot. to Excl.

Patent Owner further asserts that, in *inter partes* reviews, the Board's rules do not specifically distinguish between experts and fact witnesses and that all witnesses (whether fact witnesses or expert witnesses) provide their

direct testimony in the form of declarations. Opp. to Pet. Mot. Excl. 2. Patent Owner argues that this is in contrast to procedures in district courts, where expert witnesses must be designated and special discovery procedures apply. *Id.* (citing Fed. R. Civ. P. 26(a)(2)). Although as a procedural matter, Patent Owner correctly characterizes the difference between district court proceedings and those before the Board, we do not endorse a standard that would allow a party to re-characterize a witness's testimony after the fact. In this case, however, we need not decide that issue.

At his deposition, Dr. Clifton stated that he understood himself to be testifying as a fact witness, not an expert (Pet. Reply 1, citing Ex. 1117, Clifton Tr. 100:2–12) and Dr. Clifton's declaration includes information that demonstrates sufficient knowledge of facts for admissibility (Ex. 2090 ¶¶ 3–6 (describing his education, his technical research in MIS junctions (although not specifically concerning contact resistance), his years of experience, his employment by Patent Owner since 2004, and his current role as Vice President of Semiconductor Technologies)). We do not agree with Petitioner that Dr. Clifton's occasional use of the expression "I believe" itself transforms his testimony from fact to opinion concerning the objective criteria. *See* Pet. Mot. To Excl. 6. Much of the testimony in Dr. Clifton's declaration concerning the long felt need in the industry, what the patents describe, the Connelly papers, the work that led up to the structures Patent Owner developed, the reactions of other researchers in the field, and the unexpected nature of the results, is based on events that occurred shortly before or while Dr. Clifton was employed by Patent Owner and derive from Dr. Clifton's personal knowledge. In light of his background and the largely factual nature of his testimony, Petitioner's arguments for excluding

Dr. Clifton's testimony concern the weight that we should accord his testimony, rather than its admissibility.

Petitioner's Motion to Exclude is, therefore, denied.

V. OTHER ISSUES

A. Appointments Clause

Patent Owner argues that "[t]he AIA as written by Congress violates the Appointments Clause." PO Resp. 60.

The Supreme Court resolved this issue in *United States v. Arthrex, Inc.*, 141 S. Ct. 1970 (2021).

B. Alleged Structural Bias

Patent Owner argues that "[t]he Board's handling of this IPR is structurally biased in a way that has violated Acorn's due-process rights" because the Director's delegation of the authority to determine whether to institute and try this case "results in an improper structural bias because the Board has a strong financial incentive to institute trials." PO Resp. 61.

This argument was rejected by the Federal Circuit in *Mobility Workx, LLC v. Unified Patents, LLC*, 15 F.4th 1146 (Fed. Cir. 2021).

C. Stipulation

Patent Owner argues that "[t]he Board's eleventh-hour invitation to the petitioner to revise its stipulation regarding parallel validity challenges in the district court . . . violated *SAS Institute Inc. v. Iancu*, 138 S. Ct. 1348 (2018), due-process, and fundamental notions of fairness." PO Resp. 64. Patent Owner contends that "Acorn invested its limited resources in these IPRs and the related litigation and chose which arguments to make based on the petition and the stipulation therein" but "after Acorn had made those significant investments, the Board allowed the petitioner to alter its case,

indeed the Board invited and encouraged such revision." *Id*. (emphasis omitted).

This argument is unpersuasive. The stipulation did not change the contours of, or "curate," the Petition; instead, in accordance with the precedential case of *Sotera Wireless, Inc. v. Masimo Corp.*, IPR2020-01019, Paper 12 (December 1, 2020), Petitioner simply stipulated not to bring the same arguments in the District Court.[21]

[21] *Sotera Wireless* issued and was designated precedential (on December 1, 2020 and December 17, 2020, respectively) after the Petition and Petitioner's Preliminary Reply were filed (on June 29, 2020 and November 23, 2020, respectively). Papers 2, 14.

VI. CONCLUSION

As set forth in the following table, Petitioner has shown, by a preponderance of the evidence, that claims 1–5 and 8–10 are unpatentable. Petitioner has not shown, by a preponderance of the evidence, that claims 6, 11, 12, and 14–28 are unpatentable.

Claims	35 U.S.C. §	References	Claims Shown Unpatentable	Claims Not Shown Unpatentable
1–3, 8–10	102(b)	Goodnick	1–3, 8–10	
4	103(a)	Goodnick, Jammy	4	
5	103(a)	Goodnick	5	
1, 11, 12, 15, 23–25, 28	103(a)	Goodnick, Taubenblatt 1982		1, 11, 12, 15, 23–25, 28
14, 17–19, 22	103(a)	Goodnick, Jammy, Taubenblatt 1982		14, 17–19, 22
6	103(a)	Goodnick, Jammy, Taubenblatt 1982, Chang		6
16, 26, 27	103(a)	Goodnick, Taubenblatt 1982, Kim		16, 26, 27
20, 21	103(a)	Goodnick, Jammy, Taubenblatt 1982, Kim		20, 21
Overall			1–5, 8–10	6, 11, 12, 14–28

VII. ORDER

It is:

ORDERED that claims 1–5 and 8–10 of the '395 patent have been shown, by a preponderance of the evidence, to be unpatentable;[22]

FURTHER ORDERED that claims 6, 11, 12, and 14–28 have not been shown, by a preponderance of the evidence, to be unpatentable;

FURTHER ORDERED, that Patent Owner's Motion to Exclude is dismissed; and

FURTHER ORDERED, that Petitioner's Motion to Exclude is denied; and

FURTHER ORDERED that because this is a Final Written Decision, the parties to the proceeding seeking judicial review of the decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

[22] Should Patent Owner wish to pursue amendment of the challenged claims in a reissue or reexamination proceeding subsequent to the issuance of this decision, we draw Patent Owner's attention to the April 2019 *Notice Regarding Options for Amendments by Patent Owner Through Reissue or Reexamination During a Pending AIA Trial Proceeding*. *See* 84 Fed. Reg. 16,654 (Apr. 22, 2019). If Patent Owner chooses to file a reissue application or a request for reexamination of the challenged patent, we remind Patent Owner of its continuing obligation to notify the Board of any such related matters in updated mandatory notices. *See* 37 C.F.R. § 42.8(a)(3), (b)(2).

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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO. LTD.,
Petitioner,

v.

ACORN SEMI, LLC,
Patent Owner.

IPR2020-01282
Patent 10,090,395 B2

Before BRIAN J. McNAMARA, JOHN R. KENNY, and AARON W. MOORE, *Administrative Patent Judges.*

KENNY, *Administrative Patent Judge*.

ORDER
Granting Request for Rehearing
35 U.S.C. § 42.71

On February 9, 2022, we issued a Final Written Decision that addressed claims 1–6, 8–12, and 14–28 of U.S. Patent No. 10,090,395 B2. Paper 56 ("Decision"). Via email dated February 22, 2022, Patent Owner requested that we modify the Decision because claim 10 had been disclaimed by Patent Owner before we issued our institution decision. *See* Ex. 3001. Patent Owner identified the disclaimer at issue (Ex. 2056) in an updated mandatory notice (Paper 11), but did not identify it in its preliminary response (Paper 10) or pre-institution sur-reply (Paper 14). Our institution decision included claim 10 as part of the proceeding. Paper 20, 2, 49. Patent Owner did not seek rehearing of our institution decision on this basis. Further, Patent Owner did not refer to its disclaimer in its Patent Owner Response. Paper 28.

Patent Owner represents that Petitioner does not oppose correcting the Decision to remove the discussion of claim 10, and Patent Owner does not request the extension of any deadlines as a result of such a correction. Ex. 3001. Patent Owner has not otherwise sought rehearing of our Decision. Under the circumstances, we treat Patent Owner's email as a request for rehearing, which we grant. 37 C.F.R. § 42.71. Thus, we remove the analysis of claim 10 from the Decision as set forth in the order below.

ORDER

It is:

ORDERED that textual changes are made to the Decision as indicated in Appendix A below;

FURTHER ORDERED that on the following change is made to page 9 of the Decision, replacing Ground 1 in the table of grounds with the following:

Ground	Claim(s) Challenged	35 U.S.C. §	Reference(s)/Basis
1	1–3, 8, 9	102(b)	Goodnick[1]

and

FURTHER ORDERED that the following change is made to page 63 of the Decision, replacing the summary table with the following:

Claims	35 U.S.C. §	References	Claims Shown Unpatentable	Claims Not Shown Unpatentable
1–3, 8, 9[2]	102(b)	Goodnick	1–3, 8, 9	
4	103(a)	Goodnick, Jammy	4	
5	103(a)	Goodnick	5	
1, 11, 12, 15, 23–25, 28	103(a)	Goodnick, Taubenblatt 1982		1, 11, 12, 15, 23–25, 28
14, 17–19, 22	103(a)	Goodnick, Jammy, Taubenblatt 1982		14, 17–19, 22
6	103(a)	Goodnick, Jammy, Taubenblatt 1982, Chang		6

[1] S.M. Goodnick et al., *Effects of a thin SiO_2 layer on the formation of metal-silicon contacts*, 18 J. VAC. SCI. & TECH. 949 (Apr. 1981) (Ex. 1121).
[2] Claim 10 was disclaimed.

Claims	35 U.S.C. §	References	Claims Shown Unpatentable	Claims Not Shown Unpatentable
16, 26, 27	103(a)	Goodnick, Taubenblatt 1982, Kim		16, 26, 27
20, 21	103(a)	Goodnick, Jammy, Taubenblatt 1982, Kim		20, 21
Overall			1–5, 8, 9	6, 11, 12, 14–28

APPENDIX A

Decision Page(s)	Original Text	Replacement Text
2	Samsung Electronics Co., Ltd. ("Petitioner") filed a Petition, Paper 2 ("Petition" or "Pet."), to institute an *inter partes* review of claims 1–6, 8–12, and 14–28 ("challenged claims") of U.S. Patent No. 10,090,395 B2 (Ex. 1101, "'395 patent"). Acorn Semi LLC ("Patent Owner") filed a Preliminary Response, Paper 10 ("Prelim. Resp."), contending that the Petition should be denied as to all challenged claims.	Samsung Electronics Co., Ltd. ("Petitioner") filed a Petition, Paper 2 ("Petition" or "Pet."), to institute an *inter partes* review of claims 1–6, 8–12, and 14–28 of U.S. Patent No. 10,090,395 B2 (Ex. 1101, "'395 patent"). Acorn Semi LLC ("Patent Owner") subsequently disclaimed claim 10 (*see* Ex. 2056, 1) and filed a Preliminary Response, Paper 10 ("Prelim. Resp."), contending that the Petition should be denied as to claims 1–6, 8, 9, 11, 12, and 14–28 ("challenged claims").
3	we determine that Petitioner has shown, by a preponderance of the evidence, that claims 1–5 and 8–10 are unpatentable	we determine that Petitioner has shown, by a preponderance of the evidence, that claims 1–5, 8, and 9 are unpatentable
8	claims 1–6, 8–12, and 14–28	claims 1–6, 8, 9, 11, 12, and 14–28
16	claims 1–3 and 8–10	claims 1–3, 8 and 9
27	claims 2, 3, and 8–10	claims 2, 3, 8, and 9
63	As set forth in the following table, Petitioner has shown, by a preponderance of the evidence, that claims 1–5 and 8–10 are unpatentable. Petitioner has not shown, by a preponderance of the evidence, that claims 6, 11, 12, and 14–28 are unpatentable.	As set forth in the following table, Petitioner has shown, by a preponderance of the evidence, that claims 1–5, 8, and 9 are unpatentable. Petitioner has not shown, by a preponderance of the evidence, that claims 6, 11, 12, and 14–28 are unpatentable.

64	claims 1–5 and 8–10 of the ’395 patent have been shown, by a preponderance of the evidence, to be unpatentable	claims 1–5, 8, and 9 of the ’395 patent have been shown, by a preponderance of the evidence, to be unpatentable

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US009905691B2

(12) **United States Patent**
Grupp et al.

(10) **Patent No.: US 9,905,691 B2**
(45) **Date of Patent: Feb. 27, 2018**

(54) **METHOD FOR DEPINNING THE FERMI LEVEL OF A SEMICONDUCTOR AT AN ELECTRICAL JUNCTION AND DEVICES INCORPORATING SUCH JUNCTIONS**

(71) Applicant: **Acorn Technologies, Inc.**, La Jolla, CA (US)

(72) Inventors: **Daniel E. Grupp**, Palo Alto, CA (US); **Daniel J. Connelly**, Redwood City, CA (US)

(73) Assignee: **Acorn Technologies, Inc.**, La Jolla, CA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 424 days.

(21) Appl. No.: **15/048,877**

(22) Filed: **Feb. 19, 2016**

(65) **Prior Publication Data**

US 2016/0172491 A1 Jun. 16, 2016

Related U.S. Application Data

(60) Continuation of application No. 13/552,556, filed on Jul. 18, 2012, which is a continuation of application No. 13/022,522, filed on Feb. 7, 2011, now Pat. No. 8,431,469, which is a division of application No. 12/197,996, filed on Aug. 25, 2008, now Pat. No. 7,884,003, which is a division of application No. 11/181,217, filed on Jul. 13, 2005, now Pat. No. 7,462,860, which is a continuation of application No.

(Continued)

(51) **Int. Cl.**

H01L 29/51	(2006.01)
H01L 21/31	(2006.01)
H01L 29/78	(2006.01)
H01L 29/872	(2006.01)
H01L 29/16	(2006.01)
H01L 29/161	(2006.01)

(52) **U.S. Cl.**

CPC ***H01L 29/7839*** (2013.01); ***H01L 29/16*** (2013.01); ***H01L 29/161*** (2013.01); ***H01L 29/1608*** (2013.01); ***H01L 29/872*** (2013.01)

(58) **Field of Classification Search**

CPC H01L 29/51; H01L 29/513; H01L 29/518; H01L 23/3171; H01L 21/31; H01L 21/3105; H01L 21/28; H01L 21/28202

USPC 257/629

See application file for complete search history.

(56) **References Cited**

U.S. PATENT DOCUMENTS

3,513,366 A	5/1970	Clark
3,590,471 A	7/1971	Lepselter et al.
3,708,360 A	1/1973	Wakefield, Jr. et al.

(Continued)

FOREIGN PATENT DOCUMENTS

EP	0295490 A1	12/1988
EP	0789388 A2	8/1997

(Continued)

OTHER PUBLICATIONS

Acorn Technologies, Inc., International Application No. PCT/US2012/060893 filed Oct. 18, 2012, ISA/US, International Search Report and Written Opinion, Dec. 11, 2012, 23 pages.

(Continued)

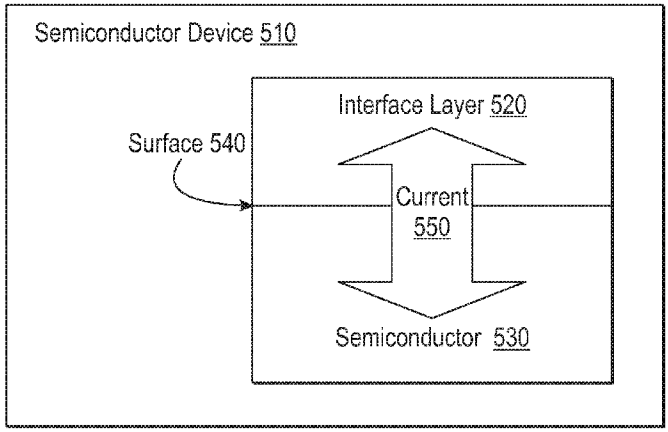
Primary Examiner — Monica D Harrison

(74) *Attorney, Agent, or Firm* — Ascenda Law Group, PC

(57) **ABSTRACT**

An electrical device in which an interface layer is disposed in between and in contact with a conductor and a semiconductor.

30 Claims, 6 Drawing Sheets



Related U.S. Application Data

10/217,758, filed on Aug. 12, 2002, now Pat. No. 7,084,423.

(56) **References Cited**

U.S. PATENT DOCUMENTS

3,983,264	A	9/1976	Schroen et al.	
4,019,113	A	4/1977	Hartman	
4,056,642	A	11/1977	Saxena et al.	
4,300,152	A	11/1981	Lepselter	
4,422,090	A	12/1983	Shepherd et al.	
4,485,550	A	12/1984	Koeneke et al.	
4,583,110	A	4/1986	Jackson et al.	
4,723,197	A	2/1988	Takiar et al.	
4,811,077	A	3/1989	Fowler et al.	
4,843,029	A	6/1989	Joyce et al.	
5,021,365	A	6/1991	Kirchner et al.	
5,027,166	A	6/1991	Ohtsuka et al.	
5,098,859	A	3/1992	Jackson et al.	
5,308,998	A	5/1994	Yamazaki et al.	
5,399,206	A	3/1995	De Lyon	
5,438,210	A	8/1995	Worley	
5,578,848	A	11/1996	Kwong et al.	
5,596,218	A	1/1997	Soleimani et al.	
5,608,266	A	3/1997	Agnello et al.	
5,612,567	A	3/1997	Baliga	
5,663,584	A	9/1997	Welch	
5,801,398	A	9/1998	Hebiguchi	
5,801,444	A	9/1998	Aboelfotoh et al.	
5,888,891	A	3/1999	Gould	
5,908,313	A	6/1999	Chau et al.	
5,939,763	A	8/1999	Hao et al.	
5,943,575	A	8/1999	Chung et al.	
6,011,271	A	1/2000	Sakkuma et al.	
6,037,605	A	3/2000	Yoshimura	
6,064,082	A	5/2000	Kawai et al.	
6,071,783	A	6/2000	Liang et al.	
6,091,076	A	7/2000	Deleonibus et al.	
6,096,590	A	8/2000	Chan et al.	
6,117,781	A	9/2000	Lukanc et al.	
6,150,286	A	11/2000	Sun et al.	
6,198,113	B1	3/2001	Grupp	
6,207,976	B1	3/2001	Takahashi et al.	
6,261,932	B1	7/2001	Hulfachor	
6,291,282	B1	9/2001	Wilk et al.	
6,291,866	B1	9/2001	Wallace et al.	
6,291,867	B1	9/2001	Wallace et al.	
6,293,137	B1	9/2001	Liu et al.	
6,303,479	B1	10/2001	Snyder	
6,326,294	B1	12/2001	Jang et al.	
6,339,232	B1	1/2002	Takagi	
6,344,673	B1	2/2002	Aussilhou	
6,380,021	B1	4/2002	Wang et al.	
6,452,244	B1	9/2002	Miura et al.	
6,462,931	B1	10/2002	Tang et al.	
6,548,875	B2	4/2003	Nishiyama	
6,608,352	B1	8/2003	Long et al.	
6,680,224	B2	1/2004	Shin et al.	
6,724,068	B2	4/2004	Matsuyama	
6,724,088	B1	4/2004	Jammy et al.	
7,084,423	B2	8/2006	Grupp et al.	
7,176,483	B2	2/2007	Grupp et al.	
8,110,877	B2	2/2012	Mukherjee et al.	
8,952,541	B2	2/2015	Mukherjee et al.	
2001/0028067	A1	10/2001	Awano	
2002/0061646	A1	5/2002	Kan et al.	
2002/0175386	A1*	11/2002	Kim	B82Y 10/00 257/423
2003/0009463	A1	1/2003	Gallant	
2003/0012146	A1	1/2003	Novaes	
2003/0121468	A1	7/2003	Boone et al.	
2003/0127700	A1	7/2003	Moddel et al.	
2003/0132466	A1	7/2003	Shin et al.	
2003/0235936	A1	12/2003	Snyder et al.	
2004/0026687	A1	2/2004	Grupp et al.	
2004/0142524	A1	7/2004	Grupp et al.	
2005/0009302	A1	1/2005	Wakui et al.	
2005/0037557	A1	2/2005	Doczy et al.	
2005/0093027	A1	5/2005	Grupp et al.	
2011/0092047	A1	4/2011	Gaines et al.	

FOREIGN PATENT DOCUMENTS

WO	WO 2004/015782 A1	2/2004
WO	WO 2004/030104 A1	4/2004

OTHER PUBLICATIONS

"Patents Act 1977: Examination Report under Section 18(3)", UK Intellectual Property Office dated Apr. 29, 2015, Application No. GB1409999.8 (filed Oct. 18, 2012), 5 pgs.

McKinley; et al., "Control of Ge homojunction band offsets via ultrathin Ga—As dipole layers", Applied Surface Science (1992), 56-58(Part 2):762-765.

McKinley; et al., "Controlled modification of heterojunction band lineups by diffusive intralayers", Journal of Vacuum Science & Technology A Vacuum Surfaces and Films (May/Jun. 1990), 8(3):1917-21.

"Research Achievements", Research Achievements at RCIQE, downloaded Apr. 12, 2002, from: http://www.rciqe.hokudai.ac.jp/RCIQEold/ResearchAchievements.html, 8 pgs.

Aberle, Armin G., et al., "Injection-Level Dependent Surface Recombination Velocities at the Silicon-Plasma Silicon Nitrite Interface", Institute fur Solarenergieforschung, ISFH, D-3 1860 Emmerthal, Germany, (Mar. 9, 1995), pp. 2828-2830.

"International Search Report and Written Opinion of the International Searching Authority", Patent Cooperation Treaty (Mar. 2, 2006), PCT/US2005/030209, 6 pgs.

"International Search Report", Patent Cooperation Treaty (Dec. 18, 2003), PCT/US03/25057, 4 pgs.

Adam; et al., "Experimental Identification of Nitrogen-Vacancy Complexes in Nitrogen Implanted Silicon", Applied Physics Letters (Jul. 2001), 79(5):623-625.

Alers; et al., "Effects of Thermal Stability and Roughness on Electrical Properties of Tantalus Oxide Gates", MRS Proceedings (1999), 567:391-395.

Almeida; et al., "Reaction-Diffusion Model for Thermal Growth of Silicon Nitrite Films on Si", Physical Review B (Dec. 2000), 62(24):R16255-R16258.

Aboelfotoh, "Influence of thin interfacial silicon oxide layers on the Schottky-barrier behavior of Ti on Si(100)", Phys Rev B Condens Matter (Mar. 1989), 39(8):5070-5078.

Bauernschmitt, et al., "Transition from MOS to Schottky-contract behaviour in Yb-SiO2-Si Tunneling Junctions with extremely thin SiO2 layer", Microelectronic Engineering (1993), 22:105-108.

Baumvol, "Atomic Transport During Growth of Ultrathin Dielectrics on Silicon", Surface Science Reports (Dec. 1999), 36(1-8):1-166.

Berger, "Contact Resistance and Contact Resistivity" J. Electrochem. Soc.: Solid-State Science and Technology (1972), 119(4):507-514.

Bannikov; et al., "Field-Effect Transistor With Metal-(Tunneling-Insulator)Semiconductor Contacts and a Gate Insulator Made of a Mangmuir-Blodgett Film", Soviet Technical Physics Letters (Mar. 1989), 15(3):211-212.

Bringans, "Arsenic Passivation of Si and Ge Surfaces", Critical Reviews in Solid State and Materials Sciences I(1992), 17(4):353-395.

Cai; et al., "Investigation of the Properties of Plasma-Enhanced Chemical Vapor Deposition Silicon Nitrite and its Effect on Silicon Surface Passivation", Journal of Applied Physics (May 1998), 83(11):5885-5889.

Blosse; et al., "A Novel Low Cost 65nm CMOS Process Architecture With Self Aligned Isolation and W Cladded Source/Drain", IEEE, Transactions of 2004 International Electron Device Meeting (Jan. 2005), pp. 669-672.

Chadi; et al., "Fermi-Level-Pinning Defects in Highly n-Doped Silicon", Physical Review Letters (Dec. 1997), 79(24):4834-4837.

(56) **References Cited**

OTHER PUBLICATIONS

Card; et al., "Studies of tunnel MOS diodes I. Interface effects in silicon Schottky diodes", Journal of Physics D: Applied Physics (1971), 4(10):1589-1601.

Chen; et al., "High Quality Native-Oxide-Free Ultrathin Oxide Grown by In-Situ HF-Vapor Treatment", Electronic Letters, (May 2000), 36(11):981-983.

Chaneliere; et al., "Tantalum Pentoxide (Ta2O5) Thin Films for Advanced Dielectric Applications"; Materials Science and Engineering, R: Reports (May 1998), 22(6):269-322.

Connelly; et al., "Optimizing Schottky S/D Offset for 25-nm Dual-Gate Cmos Performance", Electron Device Letters, IEEE (Jun. 2003), 24(6)411-413.

Gilmer; et al., "Process and Manufacturing Challenges for High-K Gate Stack Systems", MRS Proceedings, MRS Spring Meeting (1999), 567:323-341.

Edelstein; et al., "Full Copper Wiring in a Sub-0.25 mm CMOS ULSI Technology", Proceedings of the IEEE International Electron Device Meeting (1997), pp. 773-776.

Hara, et al., "Control of Schottky and Ohmic Interfaces by Unpinning Fermi Level", Applied Surface Science (1997), 117-118:394-399.

Hara; et al., "Pinning-Controlled Metal/Semiconductor Interfaces", Proc. SPIE 2779, 3rd International Conference on Intelligent Materials and 3rd European Conference on Smart Structures and Materials (Apr. 1996), 2779:802-807.

Hara; et al., "Pinning-Controlled Ohmic Contacts: Application to SiC(0001)", Applied Surface Science (Nov. 1996), 107:218-221.

Hasegawa; et al., "Unpinning of Fermi Level in Nanometer-Sized Schottky Contacts on GaAs and InP", Applied Surface Science (2000): 166:92-96.

Gopalakrishnan; et al., "Impact Ionization MOS (I-MOS)-Part I: Device and Circuit Simulations", IEEE Transactions Electron Devices (Jan. 2005), 52(1):69-76.

Heine, "Theory of Surface States", Physical Review (Jun. 1965), 138(6A):83-4.

Hilsenbeck; et al., "Aging Behavior of Algan HFETs With Advanced Ohmic and Schottky Contacts", Electronic letters (May 2000), 38(11):980-981.

Huang, "Metal-Oxide Semiconductor Field-Effect Transistors Using Schottky Barrier Drains", Electronics Letters (1797), 33(15):1341-1342.

Huang; et al., "Two-Dimensional Numerical Simulation of Schottky Barrier MOSFET with Channel Length to 10 nn", IEEE (Apr. 1998), pp. 842-848.

Hayafuji; et al., "Nitridation of Silicon and Oxidized-Silicon", J. Electrochem. Soc. (1982), 129(9):2102-2108.

International Search Report, PCT/US2004/042084, Mailing date Sep. 1, 2005, 4 pgs.

Izumi, "43 Hydrogen Termination: The Ideally Finished Silicon Surface", Ultraclean Surface Processing of Silicon Wafers (1998), pp. 559-565.

Kamins; et al., "Effect of Hydrogen on p-Type Epitaxial Silicon Sheet-Resistance Measurements", Electrochemical and Solid-State Letters (1998), 1(2):100-101.

Kamiyama; et al., "Ultrathin Tantalum Odise Capacitor Dielectric Layers Fabricated Using Rapid Thermal Nitridation Prior to Low Pressure Chemical Vapor Deposition", J. Electrochem Soc. (1993), 140(6)1617.

Kaxiras, "Efthimios. Semiconductor-surface restoration by valence-mending adsorbates: Application to Si (100): S and Si (100): Se", Phys Rev B Condens Matter (Mar. 1991), 43(18):6824-6827.

Kedzierski; et al., "Extension and Source/Drain Design for High-Performance FinFET Devices", IEEE Trans. Electron Devices (Apr. 2003), 50(4):952-958.

Keller; et al., "Calculations of the barrier height and charge distribution of a metal-dielectric interface", Journal of Vacuum Science & Technology A: Vacuum, Surfaces, and Films (Jul. 1992), 10(4):775-780.

Kim; et al., "Metal-Dependent Fermi-Level Movement in the Metal/Sulfer-Passivated InGaP Contact", Journal of Vacuum Science & Technology A: Vacuum, Surfaces, and Films (1997), 15(3):1124-1128.

Kimura; et al., "A New Type of Schottky Tunnel Transistor", IEEE Electron Device Letters (Oct. 1994), 15(10): 412-414.

Lee; et al., "Electronic Property of Metallic Nanoclusters on Semiconductor Surfaces: Implications for Nanoelectronic Device Applications", Journal of Nanoparticle Research (Dec. 2000), 2(4):345-362.

Louie; et al., "Ionicity and the Theory of Schottky Barriers", Physical Review B (Feb. 1977), 15(4):2154-2162.

Mandelis; et al., "Evidence of a Surface Acceptor State in Undoped Semi-Insulating GaAs by Photothermal Radiometric Deep Level Transient Spectroscopy", Sociedad Mexicana de Ciencias de Superficies y de Vacio, (1999), 8:13-17.

Martel; et al., "Ambipolar Single-Wall Carbon Nanotube Transistors and Inverters", AIP Conference Proceedings (Mar. 2001). 591:543-547.

McKee; et al., "Physical Structure and Inversion Charge at a Semiconductor Interface With a Crystalline Oxide", Science (Jul. 2001), 293(5529):468-471.

Miyawaki; et al., "Improvement of Aluminum-Si Contact Performance in Native-OxideFree Processing", IEEE Electron Device Letters (Oct. 1990), 11(10):448-450.

Nauka; et al., "Surface Photovoltage Measurement of Hydrogen-Treated Si Surfaces", Journal of Electrochemical Society (1999), 146(1):292-295.

Nishioka; et al., "Dielectric Characteristics of Fluorinated Ultradry SiO2", Appl. Phy. Letters (Mar. 1989), 54(12):1127-1129.

Okamoto; et al., "Near-Ohmic Contact of n-GaAs with GaS/GaAs Quaisi-Metal-Insulator-Semiconductor Structure", Jpn. J. Appl. Phys. (1998), 37:3248-3251.

Padovani, "Forward Voltage-Current Characteristics of Metal-Silicon Schottky Barriers", Journal of Applied Physics (1967), 38(2):891-892.

Park; et al., "Thermal stability of molybdenum-silicon nitride-silicon Schottky diodes", Journal of Applied Physics (Mar. 1991), 69(5):3149-3153.

Patel; et al., "Arsenic Atom Location on Passive Silicon (111) Surfaces", Physical Review B (Nov. 1987), 36(14):7715-17.

Porter; et al., "A Critical Review of Ohmic and Rectifying Contacts for Silicon Carbide", Material Science and Engineering: B (Nov. 1995), 34(2-3):83-105.

Ren; et al. "Metal I Silicon Schottky Barrier Lowering by RTCVD Interface Passivation" Electrochemical Society Proceedings (2000), 2000-9:161-166.

Ruzyllo; et al., "Semiconductor Glossary an Introduction to Semiconductor Terminology", Prosto Multimedia Publishing (2004), pp. 26.

Schmidt; et al., "Carrier Recombination at Silicon-Silicon Nitride Interfaces Fabricated by Plasma-Enhanced Chemical Vapor Deposition", Journal of Applied Physics (Apr. 1999), 85(7):3626-3633.

Shalish; et al., "Yellow Luminescence and Fermi Level Pinning in GaN Layers", Appl Phys Lett (Aug. 2000), 77(7):987-989.

Snyder; et al., "Experimental Investigation of a PtSi Source and Drain Field Emission Transister", Appl Phys Lett (1995), 67:1420-1422.

Sobolewski; et al., "Properties of Ultrathin Thermal Nitrides in Silicon Schottky Barrier Structures", Applied Physics Letters, American Institute of Physics (1989), 54(7):638-640.

Sobolewski; et al., "Studies of barrier height mechanisms in metal-silicon nitride-silicon Schottky barrier diodes", Journal of Vacuum Science & Technology B (1989), 7:971-979.

Spicer; et al., "Unified Mechanism for Schottky-Barrier Formation and III-V Oxide Interface States", Physical Review Letters (Feb. 1980), 44(6):420-423.

Sze, "Metal-Semiconductor Contacts", Physics of Semiconductor Devices, John Wiley & Sons, (1981), pp. 245-311.

Takahagi; et al., "The formation of hydrogen passivated silicon singlecrystal surfaces using ultraviolet cleaning and HF etching", J Appl Phys (1988), 64(7):3516-21.

(56) **References Cited**

OTHER PUBLICATIONS

Tao; et al., "Removal of dangling bonds and surface states on silicon (001) with a monolayer of selenium", Applied Physics Letters (Mar. 2003), 82(10)1559-1561.

Tao; et al., "Suppression of silicon (001) surface reactivity using a valence-mending technique", Solid State Communications (Oct. 2004), 132(2):89-92.

Taubenblatt; et al., "Interface effects in titanium and hafnium Schottky barriers on silicon", Appl Phys Lett (May 1984), 44:895-897.

Teraji; et al., "Ohmic Contacts to n-Type 6H-SiC Without Post-Annealing", Material Research Society, MRS Spring Meeting (1996), 423:149-154.

Tersoff, "Schottky Barrier Heightsand the Continuum of Gap States", Physical Review Letters (Feb. 1984), 52(6):465-468.

Thanailakis; et al., "Transition-metal contacts to atomically clean silicon, Department of Electrical Engineering and Electronics", Journal of Physics C: Solid State Physics (1976), 9:337-343.

Thompson; et al., "A Logic Nanotechnology Featuring Strained-Silicon", IEEE Electron Device Letters (Apr. 2004),25(4):191-193.

Tung, "Electron Transport of Inhomogeneous Schottky Barriers", Appl Phys Letter (1991), 58(24):2821-2823.

Udeshi; et al., "Thermal stability of ohmic contacts between Ti and Sepassivated n-type Si(001)", J Appl Phys (2004), 95(8):4219-4222.

Uemoto, "Reduction of Ohmic Contact Resistance on N-Type 6H-SiC by Heavy Doping", Japanese Journal of Applied Physics (Jan. 1995), 34(Parts 2, No. 1A).

Verhaverbeke; et al., "Surface Characterization of Si After HF Treatments and its Influence in the Dielectric Breakdown of Thermal Oxides", MRS Proceedings (1992), 259:391-399.

Wang; et al., "High Barrier GaN Schottky Diodes: Pt/GaN and Pd/GaN", Appl. Phys. Letters (Feb. 1996), 68(9):1267-1270.

Wei; et al., "The Use of Selective Electroless Metal Deposition for Micron Size Contact Fill", IEEE International Electron Device Meeting Technical Digest (1988), pp. 446-449.

Weinberger; et al., "Surface Chemistry of HF Passivation Silicon: X-Ray Photoelectron and Ion Scattering Spectroscopy Results", J. Appl. Phys (Nov. 1986), 60(9):3232-34.

Widjaja; et al., "Ab Initlo Study and Decomposition of NH3 on Si(100)-(2x1)", J. Phy. Chem B, (2000), 104:2527-2533.

Wittmer; et al., "Ideal Schottky diodes on passivated silicon", Phys Rev Lett (Nov. 1992), 69(18):2701-2704.

Wolf; et al., "Spintronics: A Spin-Based Vision for the Future", Science (Nov. 2001), 294(5546):1488-95.

Wright; et al., "Hot-Electron Immunity of SiO2 Dielectrics with Fluorine Incorporation", IEEE Electron Device Letters (1989), 10(8):347-348.

Yablonovitch; et al., "Unusually Low Surface-Recombination Velocity on Silicon and Germanium Surfaces", Physical Review Letters (Jul. 1986), 57(2):249-252.

Yagishita; et al., "High Performance Damascene Metal Gate Mosfet's for 0.1 mm Regime", IEEE Trans. Electron Devices (2000), 47(5):1028-1034.

Yang; et al., "The Effects of Interfacial Sub-Oxide Transition Regions and Monolayer Level Nitridation on Tunneling Currents in Silicon Devices", IEEE Electron Device Letters (2000), 21(2):76-78.

Zhang; et al., "Schottky diodes of NiÕAu on n-GaN grown on sapphire and SiC substrates", Applied Physics Letters (Oct. 2001), 79(16):2567-69.

Zhu; et al., "Low-Resistance Ti/n-Type Si(100) Contacts by Monolayer Se Passivation", ECS Trans (2006), 2(2):401-409.

Zhu; et al., "Stability of Se passivation layers on Si(001) surfaces characterized by time-of-flight positron annihilation induced Auger electron spectroscopy", Journal of Applied Physics (2005), 97(10):103510-1103510-4.

* cited by examiner

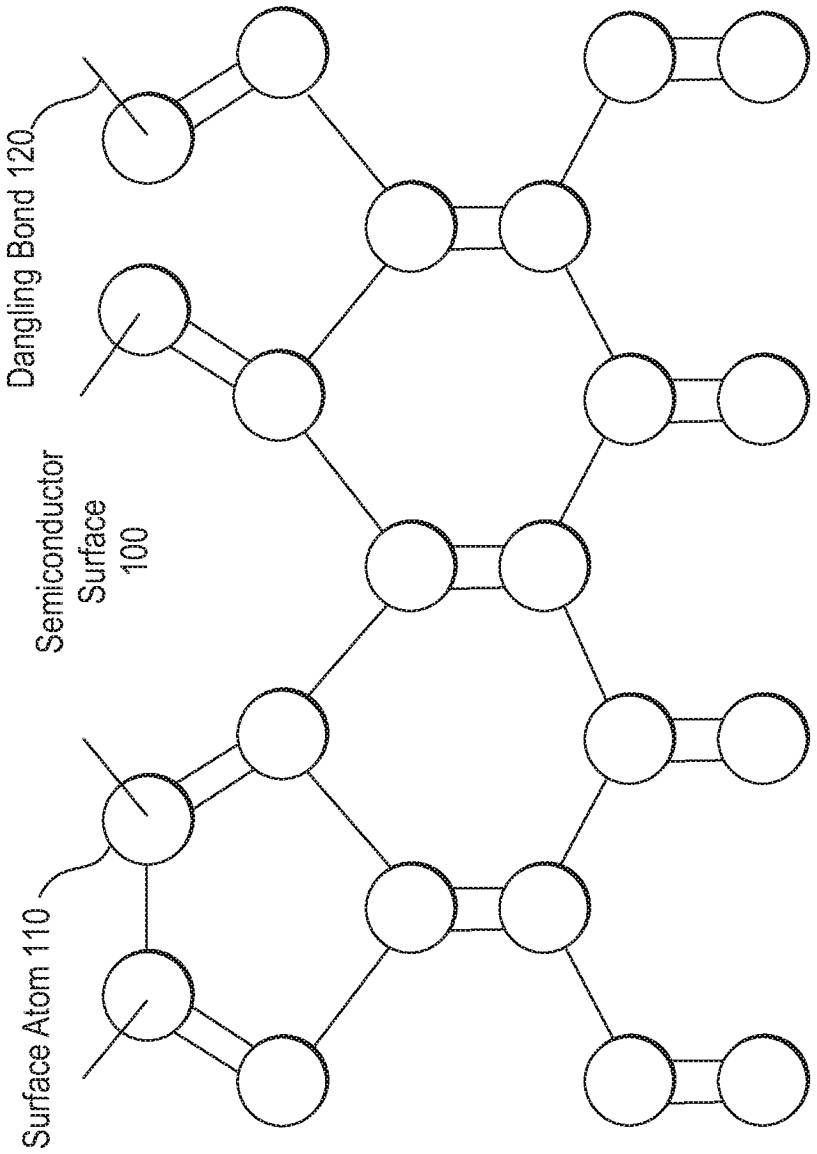

[100]
Dangling Bond 120
Semiconductor Surface 100
Surface Atom 110

Fig. 1

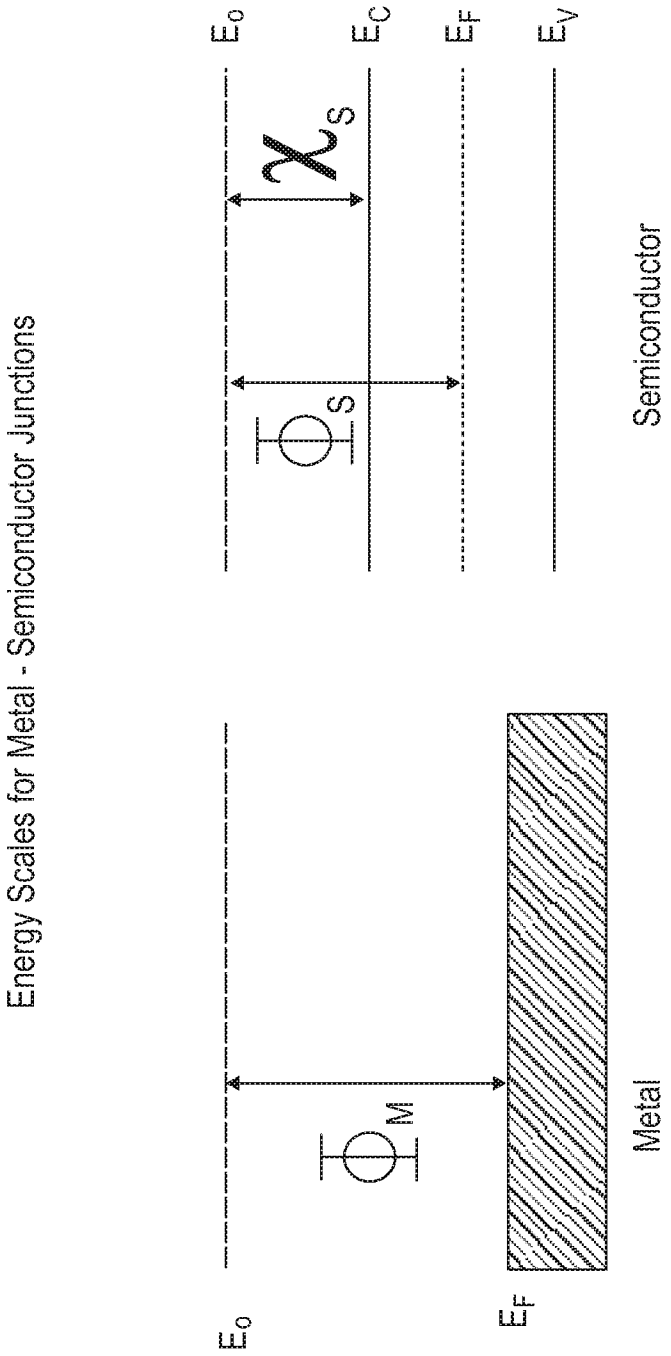

Energy Scales for Metal - Semiconductor Junctions
E_o
E_C
E_F
E_V
χ_S
Θ_S
Semiconductor
Θ_M
Metal
E_o
E_F

Fig. 2

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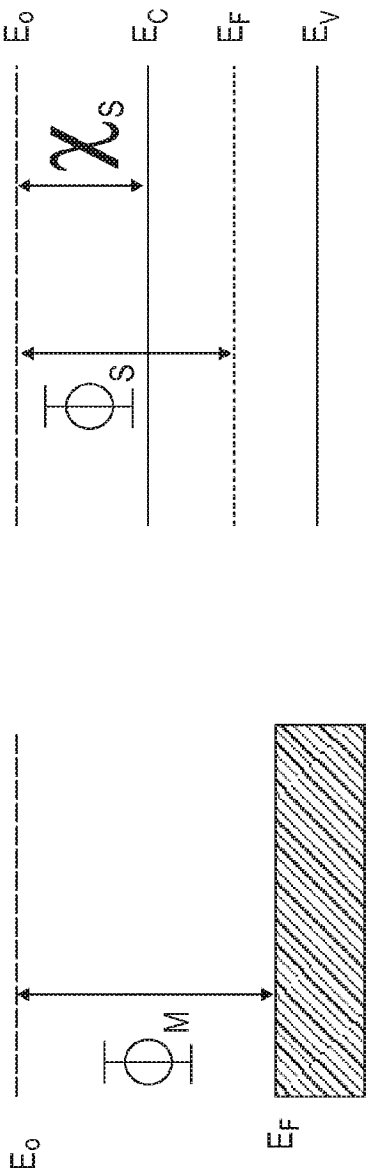


Fig. 3
(Prior Art)

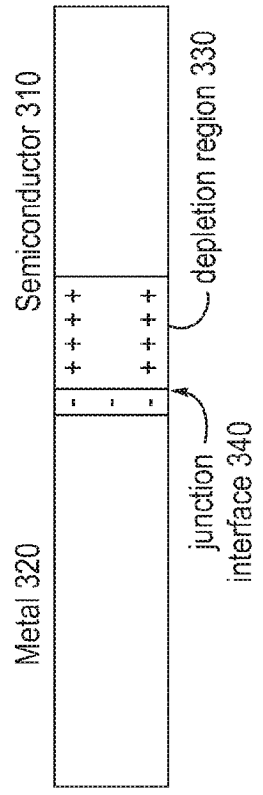
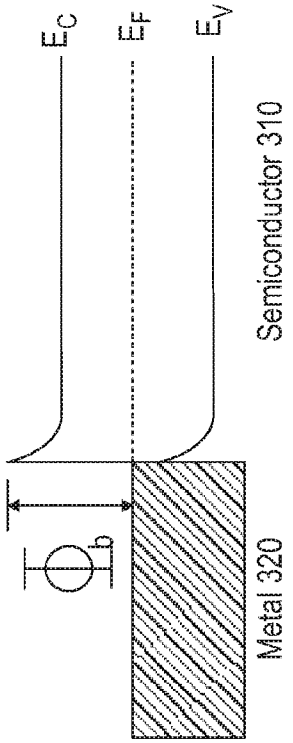


Fig. 4
(Prior Art)



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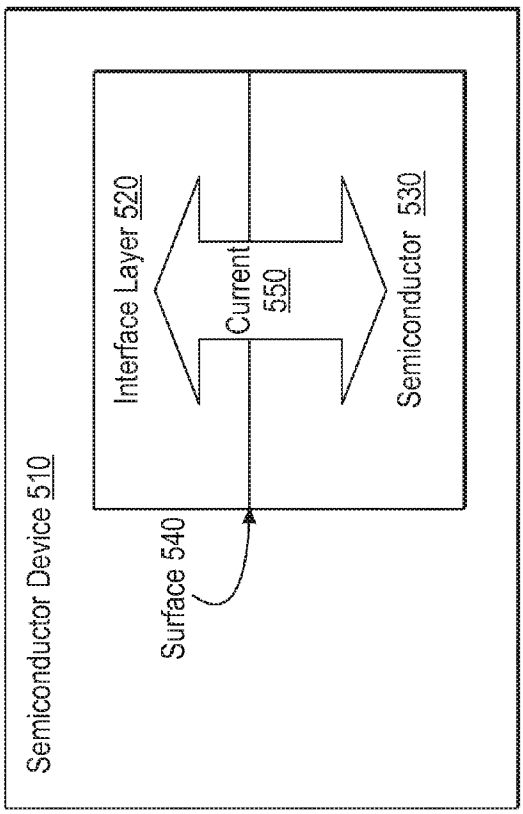


Fig. 5

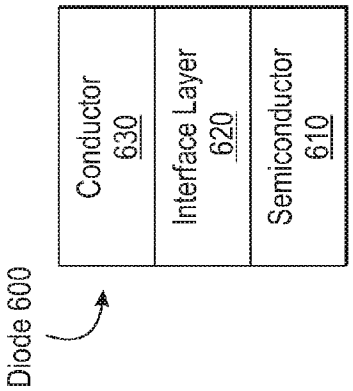


Fig.6

Case: 22-1539 Document: 19 Page: 329 Filed: 06/24/2022

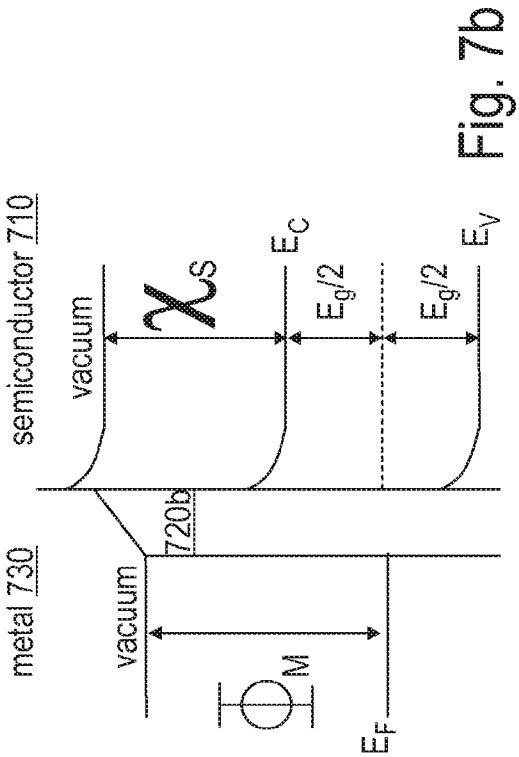


Fig. 7b

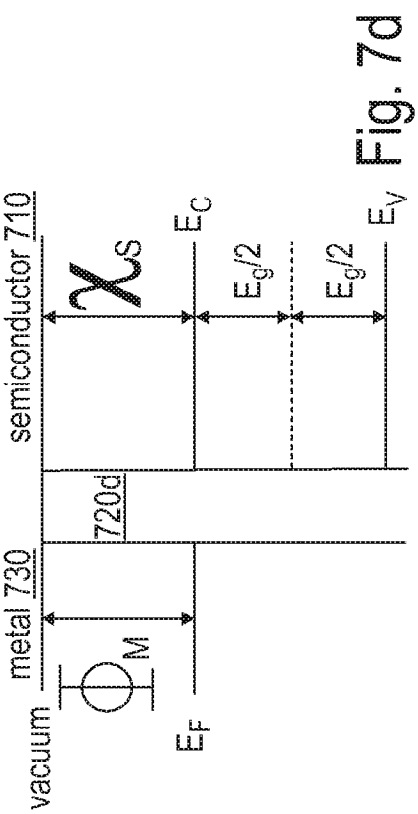


Fig. 7d

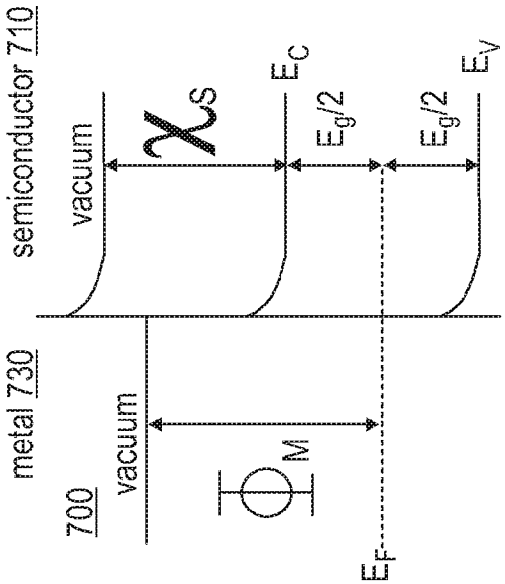


Fig. 7a

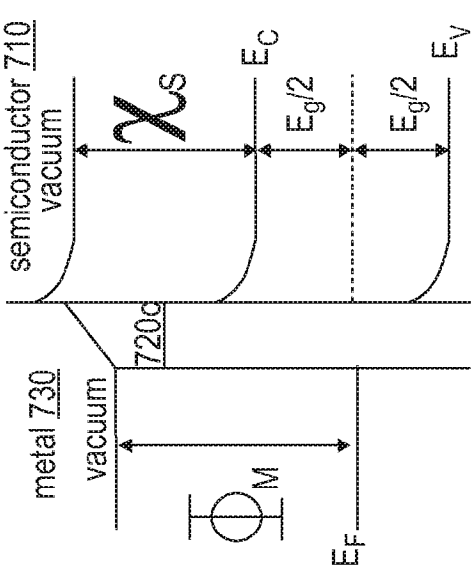
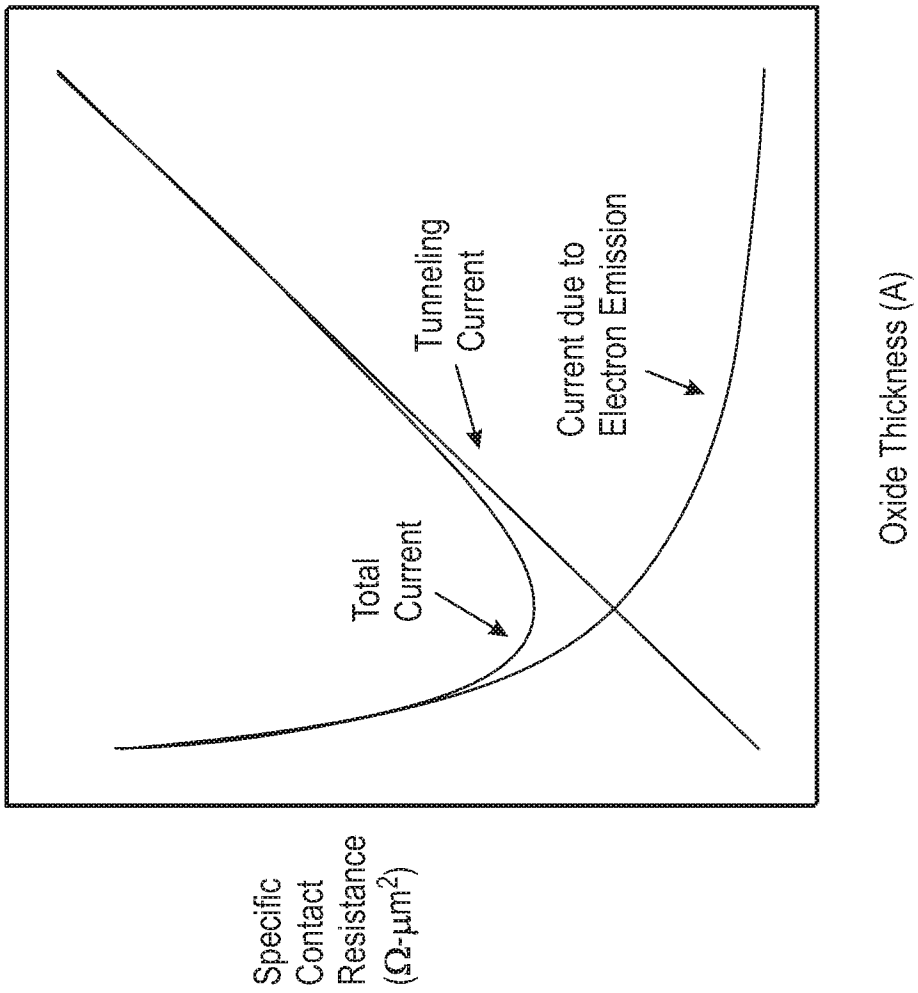


Fig. 7c

GF Exhibit 1122 - 329/363

Fig. 8


Specific Contact Resistance (Ω-μm^2)
Total Current
Tunneling Current
Current due to Electron Emission
Oxide Thickness (A)

METHOD FOR DEPINNING THE FERMI LEVEL OF A SEMICONDUCTOR AT AN ELECTRICAL JUNCTION AND DEVICES INCORPORATING SUCH JUNCTIONS

RELATED APPLICATIONS

The present application is a CONTINUATION of U.S. patent application Ser. No. 13/552,556, filed Jul. 18, 2012, which is a CONTINUATION of U.S. patent application Ser. No. 13/022,522, filed Feb. 7, 2011, now U.S. Pat. No. 8,431,469, which is a DIVISIONAL of U.S. patent application Ser. No. 12/197,996, filed Aug. 25, 2008, now U.S. Pat. No. 7,884,003, which is a DIVISIONAL of U.S. patent application Ser. No. 11/181,217, filed Jul. 13, 2005, now U.S. Pat. No. 7,462,860, which is a CONTINUATION of U.S. patent application Ser. No. 10/217,758, filed Aug. 12, 2002, now U.S. Pat. No. 7,084,423, which is related to U.S. patent application Ser. No. 10/342,576, filed Jan. 14, 2003, now U.S. Pat. No. 6,833,556, all of which are hereby incorporated by reference.

FIELD OF THE INVENTION

The invention relates generally to semiconductor processing and semiconductor devices. More particularly, the invention relates to a process for depinning the Fermi level of a semiconductor at a metal-interface layer-semiconductor junction and to devices that employ such a junction.

BACKGROUND

One of the most basic electrical junctions used in modern devices is the metal-semiconductor junction. In these junctions, a metal (such as aluminum) is brought in contact with a semiconductor (such as silicon). This forms a device (a diode) which can be inherently rectifying; that is, the junction will tend to conduct current in one direction more favorably than in the other direction. In other cases, depending on the materials used, the junction may be ohmic in nature (i.e., the contact may have negligible resistance regardless of the direction of current flow). Grondahl and Geiger first studied the rectifying form of these junctions in 1926, and by 1938 Schottky had developed a theoretical explanation for the rectification that was observed.

Schottky's theory explained the rectifying behavior of a metal-semiconductor contact as depending on a barrier at the surface of contact between the metal and the semiconductor. In this model, the height of the barrier (as measured by the potential necessary for an electron to pass from the metal to the semiconductor) was postulated as the difference between the work function of the metal (the work function is the energy required to free an electron at the Fermi level of the metal, the Fermi level being the highest occupied energy state of the metal at T=0) and the electron affinity of the semiconductor (the electron affinity is the difference between the energy of a free electron and the conduction band edge of the semiconductor). Expressed mathematically:

$$\Phi_B = \Phi_M - \chi_S \quad [1]$$

where Φ_B is the barrier height, Φ_M is the work function of the metal and χ_S is the electron affinity of the semiconductor.

Not surprisingly, many attempts were made to verify this theory experimentally. If the theory is correct, one should be able to observe direct variations in barrier heights for metals of different work functions when put in contact with a common semiconductor. What is observed, however, is not direct scaling, but instead only a much weaker variation of barrier height with work function than implied by the model.

Bardeen sought to explain this difference between theoretical prediction and experimental observation by introducing the concept that surface states of the semiconductor play a role in determining the barrier height. Surface states are energy states (within the bandgap between the valence and conduction bands) at the edge of the semiconductor crystal that arise from incomplete covalent bonds, impurities, and other effects of crystal termination. FIG. **1** shows a cross-section of an un-passivated silicon surface labeled **100**. The particular silicon surface shown is an Si(100) 2×1 surface. As shown, the silicon atoms at the surface, such as atom **110**, are not fully coordinated and contain un-satisfied dangling bonds, such as dangling bond **120**. These dangling bonds may be responsible for surface states that trap electrical charges.

Bardeen's model assumes that surface states are sufficient to pin the Fermi level in the semiconductor at a point between the valence and conduction bands. If true, the barrier height at a metal-semiconductor junction should be independent of the metal's work function. This condition is rarely observed experimentally, however, and so Bardeen's model (like Schottky's) is best considered as a limiting case.

For many years, the cause underlying the Fermi level pinning of the semiconductor at a metal-semiconductor junction remained unexplained. Indeed, to this day no one explanation satisfies all experimental observations regarding such junctions. Nevertheless, in 1984, Tersoff proposed a model that goes a long way towards explaining the physics of such junctions. See J. Tersoff, "Schottky Barrier Heights and the Continuum of Gap States," Phys. Rev. Lett. 52 (6), Feb. 6, 1984.

Tersoff's model (which is built on work by Heine and Flores & Tejedor, and see also Louie, Chelikowsky, and Cohen, "Ionicity and the theory of Schottky barriers," Phys. Rev. B 15, 2154 (1977)) proposes that the Fermi level of a semiconductor at a metal-semiconductor interface is pinned near an effective "gap center", which is related to the bulk semiconductor energy band structure. The pinning is due to so-called metal induced gap states (MIGS), which are energy states in the bandgap of the semiconductor that become populated due to the proximity of the metal. That is, the wave functions of the electrons in the metal do not terminate abruptly at the surface of the metal, but rather decay in proportion to the distance from that surface (i.e., extending inside the semiconductor). To maintain the sum rule on the density of states in the semiconductor, electrons near the surface occupy energy states in the gap derived from the valence band such that the density of states in the valence band is reduced. To maintain charge neutrality, the highest occupied state (which defines the Fermi level of the semiconductor) will then lie at the crossover point from states derived from the valence band to those derived from the conduction band. This crossover occurs at the branch point of the band structure. Although calculations of barrier heights based on Tersoff's model do not satisfy all experimentally observed barrier heights for all metal-semiconductor junctions, there is generally good agreement for a number of such junctions.

One final source of surface effects on diode characteristics is inhomogeneity. That is, if factors affecting the barrier height (e.g., density of surface states) vary across the plane of the junction, the resulting properties of the junction are found not to be a linear combination of the properties of the different regions. In summary then, a classic metal-semi-

conductor junction is characterized by a Schottky barrier, the properties of which (e.g., barrier height) depend on surface states, MIGS and inhomogeneities.

The importance of the barrier height at a metal-semiconductor interface is that it determines the electrical properties of the junction. Thus, if one were able to control or adjust the barrier height of a metal-semiconductor junction, one could produce electrical devices of desired characteristics. Such barrier height tuning may become even more important as device sizes shrink even further. Before one can tune the barrier height, however, one must depin the Fermi level of the semiconductor. As discussed in detail below, the present inventors have achieved this goal in a device that still permits substantial current flow between the metal and the semiconductor.

SUMMARY OF THE INVENTION

The present inventors have determined that for thin interface layers disposed between a metal and a silicon-based semiconductor (e.g., Si, SiC and SiGe), so as to form a metal-interface layer-semiconductor junction, there exist corresponding minimum specific contact resistances. The interface layer thickness corresponding to this minimum specific contact resistance will vary depending upon the materials used, however, it is a thickness that allows for depinning the Fermi level of the semiconductor while still permitting current to flow between the metal and the semiconductor when the junction is biased (e.g., forward or reverse biased). By depinning the Fermi level, the present inventors mean a condition wherein all, or substantially all, dangling bonds that may otherwise be present at the semiconductor surface have been terminated, and the effect of MIGS has been overcome, or at least reduced, by displacing the semiconductor a sufficient distance from the metal. Minimum specific contact resistances of less than or equal to approximately 10 Ω-μm^2 or even less than or equal to approximately 1 Ω-μm^2 may be achieved for such junctions in accordance with the present invention.

Thus, in one embodiment, the present invention provides an electrical device in which an interface layer is disposed between and in contact with a metal and a silicon-based semiconductor and is configured to depin the Fermi level of the semiconductor while still permitting current flow between the metal and the semiconductor when the electrical device is biased. The specific contact resistance of the electrical device is less than approximately 10 Ω-μm^2. The interface layer may include a passivating material (e.g., a nitride, oxide, oxynitride, arsenide, hydride and/or fluoride) and sometimes also includes a separation layer. In some cases, the interface layer may be essentially a monolayer (or several monolayers) of a semiconductor passivating material.

In another embodiment, the interface layer is made up of a passivation layer fabricated by heating the semiconductor in the presence of nitrogenous material, for example ammonia (NH3), nitrogen (N2) or unbound gaseous nitrogen (N) generated from a plasma process. In such cases, the interface layer may be fabricated by heating the semiconductor while in a vacuum chamber and exposing the semiconductor to the nitrogenous material.

A further embodiment of the present invention provides for depinning the Fermi level of a semiconductor in an electrical junction through the use of an interface layer disposed between a surface of the semiconductor and a conductor. The interface layer preferably (i) is of a thickness sufficient to reduce effects of MIGS in the semiconductor, and (ii) passivates the surface of the semiconductor. Despite the presence of the interface layer, significant current may flow between the conductor and the semiconductor because the thickness of the interface layer may be chosen to provide a minimum (or near minimum) specific contact resistance for the junction. As indicated above, the interface layer may include a passivating material such as a nitride, oxide, oxynitride, arsenide, hydride and/or fluoride.

Further embodiments of the present invention provide a junction between a semiconductor and a conductor separated from the semiconductor by an interface layer configured to allow a Fermi level of the conductor to (i) align with a conduction band of the semiconductor, (ii) align with a valence band of the semiconductor, or (iii) to be independent of the Fermi level of the semiconductor. In some or all of these cases, current may flow between the conductor and the semiconductor when the junction is biased because the interface layer has a thickness corresponding to a minimum or near minimum specific contact resistance for the junction. For example, specific contact resistances of less than or equal to approximately 2500 Ω-μm^2, 1000 Ω-μm^2, 100 Ω-μm^2, 50 Ω-μm^2, 10 Ω-μm^2 or even less than or equal to 1 Ω-μm^2 may be achieved.

BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWINGS

The present invention is illustrated by way of example, and not by way of limitation, in the figures of the accompanying drawings.

FIG. **1** shows a cross-section of an un-passivated silicon surface containing surface silicon atoms with dangling bonds.

FIG. **2** illustrates various energy levels for metals and semiconductors and is labeled to show the work function of a metal and the electron affinity of a semiconductor.

FIG. **3** shows an energy band diagram for a conventional metal-n-type semiconductor junction and also illustrates the concept of a depletion region formed in the semiconductor when the materials are brought into contact with one another.

FIG. **4** illustrates band bending at a conventional metal-n-type semiconductor junction.

FIG. **5** shows a semiconductor device containing a semiconductor material having a surface across which electrical current flows during operation of the semiconductor device, and containing an interface layer formed on the surface according to one embodiment of the present invention.

FIG. **6** shows an electrical junction containing an interface layer that is disposed between a semiconductor and a conductor in accordance with one embodiment of the present invention.

FIGS. **7***a*, **7***b*, **7***c* and **7***d* show relationships between Fermi energy, conduction-band energy, and valence-band energy for an unpassivated Schottky diode, a passivated Schottky diode in which MIGS are not removed, an unpassivated Schottky diode in which MIGS are removed and a passivated Schottky diode in which MIGS are removed according to one embodiment of the present invention, respectively.

FIG. **8** shows a curve of interface layer resistance versus interface layer thickness for an electrical junction containing an interface layer disposed between a semiconductor and a conductor in accordance with one embodiment of the present invention.

DETAILED DESCRIPTION

Described herein are processes for depinning the Fermi level of a silicon-based semiconductor (e.g., Si, SiC or SiGe)

at a metal-semiconductor junction as well as devices that use such a junction. As more fully discussed below, an interface layer is introduced between the semiconductor and the metal. The interface layer functions to passivate the semiconductor surface (that is, terminate dangling bonds that may otherwise be present at the semiconductor surface so as to assure chemical stability of the surface) and to displace the semiconductor from the metal so as to reduce the effect of MIGS.

As discussed more fully below, the present inventors have determined that for thin interface layers disposed between a metal and a silicon-based semiconductor (e.g., Si, SiC and SiGe), so as to form a metal-interface layer-semiconductor junction, there exist corresponding minimum specific contact resistances. Indeed, minimum specific contact resistances of less than or equal to approximately 10 Ω-μm^2 or even less than or equal to approximately 1 Ω-μm^2 may be achieved for such junctions in accordance with the present invention. To achieve such low contact resistances, a metal that has a work function near the conduction band of the semiconductor for n-type semiconductors, or a work function that is near the valence band for p-type semiconductors, is selected.

The Schottky barrier in such junctions is already minimized, meaning that it is much less than the Schottky barrier presented by a junction in which the Fermi level is pinned, generally near the middle of the semiconductor's bandgap. The current versus voltage (IV) characteristic of these junctions is non-linear, generally having a slope that increases as the voltage increases, such that the derivative of current with respect to voltage is increasing with voltage. This results in a decreasing differential resistance (dV/dI) and a decreasing resistance (V/I). Thus, a junction that has high resistance or high differential resistance near the origin of the IV characteristic (zero volts) may have significantly lower resistance or lower differential resistance at higher voltages.

The present invention achieves low resistance and low differential resistance near the origin of the current-voltage characteristic for a metal-interface layer-semiconductor junction. Generally, the voltage around the origin should be less than about 100 mV, or more preferably less than about 10 mV for purposes of measuring, determining, or utilizing such junctions of low resistance. At higher voltages, the junction resistance will be even lower. It is thus a feature of the present invention to set an upper bound on the resistance of a contact, where the upper bound occurs at low voltages.

It is further noted that in junctions where the Schottky barrier is minimized as described above, such that the Fermi level at the junction interface at zero volts lies at or near the conduction band edge or valence band edge (for n- and p-type semiconductors, respectively), the IV characteristic will be nearly symmetric, especially at low voltage. In this case, the term "forward bias" is not defined in the usual sense of a diode wherein forward bias corresponds to the direction of bias for which greater current flows. Thus, in determining or utilizing low resistance junctions of the present invention, the voltage may be either positive or negative.

It is also possible (in accordance with a further embodiment of the present invention) to make junctions where the Schottky barrier is higher than it would be if the Fermi level at the junction interface were pinned, usually around mid-gap of the semiconductor. Such junctions are formed in the present invention between a metal with a workfunction near or substantially equal to the conduction band edge of a p-type semiconductor, or between a metal with a workfunction near or substantially equal to the valence band edge of an n-type semiconductor. These junctions are diodes, in that little current will flow if the n-type (p-type) semiconductor is biased positive (negative) with respect to the metal, and large currents will flow if the voltage is reversed. The low-current flow state is referred to as reverse bias, and the high-current flow state is referred to as positive bias.

Low resistance in the case of a diode is only relevant in forward bias conditions. In junctions created in accordance with the present invention the resistance contribution of the interface layer is smaller than the resistance due to the Schottky barrier. That is, in forward bias conditions for junctions created in accordance with the present invention, the transport of charge is limited mainly by the thermal emission of carriers from the semiconductor over the barrier at the interface, and not by the tunneling through the interface dielectric. Thus, low resistance in the case of a diode refers to a resistance lower than the resistance presented by the Schottky barrier.

In certain applications of diodes, the ability to withstand high reverse biases may be more desirable than high current flow in forward bias. These applications would be considered high voltage/low power applications. In such cases, a low resistance is not essential, and junctions created in accordance with still another embodiment of the present invention provide high-voltage diodes capable of withstanding voltages higher than could otherwise be achieved if the Fermi level of the semiconductor in the junction were pinned.

The present invention is discussed below in terms of presently preferred embodiments thereof, however, this discussion is not meant to limit the scope of the invention. By studying the present disclosure, others of ordinary skill in the art may recognize equivalent procedures, materials or structures that can be substituted for those described herein to achieve the same effect. The reader is advised and reminded that the use of such equivalents is deemed to be within the scope of the present invention. For example, where the discussion refers to well-known structures and devices, block diagrams are used, in part to demonstrate the broad applicability of the present invention to a wide range of such structures and devices.

I. Introduction and Definitions

The present discussion makes use of terms that, although well known in the art, may not be familiar to all readers. Therefore, before beginning a detailed discussion of the present invention, it is helpful to define certain terms and concepts. To understand the properties of metal-semiconductor junctions and the impact of the present invention, one must refer to some important energy scales, which are shown graphically in FIG. **2**. The so-called vacuum level (E0) represents the minimum energy that an electron needs to possess in order to completely free itself from a metal or semiconductor. For a metal, the Fermi level (E_F) represents the highest occupied energy level for the material. That is, nearly all energy states below the Fermi level are filled, while nearly all states above the Fermi level are empty. The work function of the metal (ΦM) is then defined as the energy required to free an electron at the Fermi level and mathematically it is the difference between the vacuum level and the Fermi level. The work function is an invariant bulk property of the metal.

As illustrated in the diagram, semiconductors also have a Fermi level (E_F) and a work function (Φ_S), however, the work function is not an invariant property of the semicon-

ductor. Because the Fermi level varies depending on the doping level in the semiconductor (i.e., the relative amounts of impurities introduced into the semiconductor crystal which change the electron and hole carrier concentrations), a separate parameter, the electron affinity (χ_S), is defined. The electron affinity is an invariant property of the semiconductor and is the difference between the vacuum level and the conduction band edge of the semiconductor. In a semiconductor, almost all energy states are filled in the valence band (E_V) while the conduction band (E_C) is almost empty.

Now consider a conventional junction between a metal and an n-type semiconductor that has a work function smaller than the work function of the metal (i.e., $\Phi_S<\Phi_M$). An n-type semiconductor is one in which electrons are the majority charge carriers (in p-type semiconductors, holes are the majority charge carrier). As shown in FIG. **3**, because the Fermi level in the semiconductor is higher than the Fermi level in the metal, electrons transfer from the semiconductor **310** to the metal **320** when the materials are brought into contact. Thus, a depletion region (i.e., a region in which there are no free charge carriers) **330** forms near the junction interface **340**.

The formation of the depletion region gives rise to an electric field and so-called "band bending", as one approaches the junction interface from the semiconductor side (see FIG. **4**). The band bending creates an energy barrier (discussed above) that blocks further transfer of electrons into or out of the semiconductor. Similar barriers are formed for a junction between a metal and a p-type semiconductor when the work function of the metal is less than the work function of the semiconductor. However, in the case of a metal-n-type semiconductor junction in which the work function of the semiconductor is greater than that of the metal or a metal-p-type semiconductor junction in which the work function of the semiconductor is less than that of the metal, no such energy barriers are created and the contact is said to be ohmic in nature.

As discussed above, although Schottky first postulated that the height of the energy barrier (Φ_b) formed at a metal-semiconductor junction was simply the difference between the work function of the metal and the electron affinity of the semiconductor, experiments have not verified this relationship. Instead a more complex explanation that takes into account the effects of surface defect states, inhomogeneities and MIGS appears to provide more accurate estimates of barrier heights by explaining the pinning of the Fermi level in the semiconductor. The present inventors have created a technique which is believed to depin the Fermi level of a Si-based semiconductor at a junction with a metal (and thus allow for control or tuning of the barrier height) by both passivating the semiconductor surface (to eliminate or at least reduce the effects of surface states and possibly inhomogeneities) and displacing the metal from the semiconductor (to eliminate or at least reduce the effects of MIGS). This depinning is achieved by introducing an interface layer between the semiconductor and the metal to create a semiconductor-interface layer-metal junction, which still permits significant current to flow between the metal and the semiconductor when the junction is forward biased.

This latter point is important. As discussed further below, for contacts where the energy bands of the semiconductor and the conductor align (i.e., where the Fermi level of the conductor aligns with the conduction or valence band of the semiconductor depending on semiconductor type and/or contact application), if the interface layer is too thin, the specific contact resistance of the junction increases because of the presence of MIGS, resulting in an increased barrier height; thus, current flow is hampered. Conversely, if the interface layer is too thick, the specific contact resistance is again increased and one gets low current across the junction because of tunneling limitations. The present invention achieves an interface layer that is thick enough to reduce or eliminate the effect of MIGS, while still thin enough to permit significant current flow.

II. Passivation of Semiconductor Surfaces

A common processing operation performed during semiconductor device fabrication is silicon surface passivation. Surface passivation (whether by an oxide or another material) chemically neutralizes and physically protects the underlying silicon. For example, exposing a silicon surface to oxygen (under the appropriate conditions to grow a protective film of silicon dioxide) will allow the oxygen to react with the dangling bonds of the silicon surface to form covalent bonds that satisfy the surface silicon atoms' valency and render the surface fully coordinated. These covalent bonds provide chemical stability to the silicon surface. The covalent bonds also tie up unbound charges that exist on the silicon surface as a result of the discontinuation of the semiconductor crystal at the surface.

However, passivation with silicon dioxide has several significant disadvantages. For example, silicon dioxide is a dielectric insulator that poses a significant barrier to the flow of current. Accordingly, a layer of silicon dioxide deposited or grown on a silicon surface may significantly reduce the ability for electrical current to flow through that surface. As a result, the use of silicon dioxide has been limited in practicality to surfaces external to the active region of semiconductor devices through which current passes during device operation (e.g., as a gate oxide layer). This disadvantage is compounded by the fact that the silicon dioxide grows very rapidly and readily on the silicon surface so that it is difficult to limit the growth to a thin layer. Silicon dioxide is also a poor diffusion barrier to semiconductor dopants such as boron.

Instead of making use of silicon dioxide then, in one embodiment the present inventors utilize a nitrided semiconductor surface to provide chemical passivation. That is, a nitride layer is introduced to passivate the semiconductor surface by eliminating or at least reducing the effects of surface states and possibly inhomogeneities. The nitride layer also displaces the metal from the semiconductor and eliminates or at least reduces the effects of MIGS. The result of introducing the nitride layer as an interface between the semiconductor and the metal is a depinning of the Fermi level of the semiconductor. When the Fermi level of the semiconductor is depinned, the Fermi level of the metal at the interface will be that of the bulk metal, and will not be dependent upon the interface. In addition to the above, the present inventors propose techniques for providing non-insulating, passivated semiconductor surfaces using materials other than nitrogen; for example, oxides, hydrides, arsenides and/or fluorides.

These developments have wide applicability in connection with the fabrication of Schottky diodes, Schottky-barrier transistors and other electrical components. For example, in Schottky diodes, the ability to control the energy barrier height at the diode junction is important if the device is to be tailored to specific applications. Use of the present techniques allows for tuning of the barrier height. Further, for other three-terminal devices with Schottky-barrier-isolated channels, control of device characteristics is made

possible through the present invention by allowing n- and p-type devices to be fabricated without dopants, relying instead on the use of metals with different work functions.

FIG. **5** shows a semiconductor device **510** that contains a semiconductor **530** and an interface layer **520** formed on a surface **540** of the semiconductor in accordance with the present invention. The terms semiconductor device, microelectronic device, monolithic device, chip, and integrated circuit are often used interchangeably in this field. Any or all such devices may each contain an interface layer formed on a semiconductor surface in accordance with the present invention.

The semiconductor **530** contains a semiconductor material. The term semiconductor material refers to a material having a bandgap that is greater than about 0.1 eV and less than about 4 eV. The term bandgap refers to an energy gap of forbidden energy levels separating the conduction band, which is an upper energy band that is mostly devoid of electrons and wherein electrons can conduct, and the valence band, which is an energy band that is mostly filled with electrons and wherein electrons cannot conduct. The semiconductor material may have a wide range of doping levels including no doping at all.

The semiconductor **530** has a surface **540** that is passivated by the interface layer **520**. In this context (and as used elsewhere herein) the term passivation means the elimination or at least the reduction of the effects of surface states due to defects or dangling bonds of the semiconductor surface **540**. Note that passivation does not, as a practical matter, require that all surface states be eliminated. Rather, it is the effect of surface states on the device properties that is limited or eliminated in passivation. Note further that the presence of MIGS may be regarded as a surface state, however, as used herein the term passivation is not meant to infer the elimination of MIGS (though in some cases, a passivation layer may have sufficient thickness to provide a separation layer between the semiconductor and the metal sufficient to reduce or eliminate MIGS). The semiconductor **530** is operable to be electrically coupled with a first voltage associated with the semiconductor device **510** and to conduct electrical current **550** across the passivated surface **540**.

The interface layer **520** is formed on the semiconductor **530** and may contain a passivation material that bonds to the semiconductor material by way of a covalent (or other) bond formed between the passivation material and the semiconductor material. For example, an atom of passivation material may covalently bond with a dangling bond of a surface silicon atom to fully coordinate the silicon atom and thereby help passivate the silicon atom. In some cases, the passivation material may be the sole component of the interface layer **520**, while in other cases the interface layer **520** may be a compound layer that includes both a passivation layer and a separation layer. That is, the interface layer serves to (i) chemically passivate the semiconductor surface **540**, and (ii) displace the semiconductor from the metal sufficiently to eliminate or at least reduce the effect of MIGS. As explained below, this may necessitate including a separation layer in addition to a passivation layer within the interface layer, depending on the passivation material selected. Of course, the combination of the passivation layer and the separation layer must be sufficiently thin to permit the low specific contact resistances described herein.

Different passivation materials are contemplated. According to one embodiment, the interface layer **520** is formed using a material that is preferably selected from the group consisting of hydrogen (H), oxygen (O), nitrogen (N), arsenic (As), and fluorine (F) (that is, the interface layer **520** may include a nitride, an oxide, a hydride, an arsenide and/or a fluoride). Other materials having chemical characteristics or valences similar to these materials may also be used. Note that distinct separation layers (i.e., in addition to the passivation layer(s)) may be needed where H, As, or F passivation layers are used, as these tend to form monolayer coverage, rather than a layer of a compound with Si of process-dependent thickness. In contrast, passivation layers made using N and/or O may not require distinct separation layers, as these elements may form a layer of a compound of Si with a thickness that can be varied depending on processing.

Different amounts of passivation material are contemplated to be useful for different embodiments of the present invention. Often, the interface layer **520** includes or is made up of a passivation layer with a thickness of between approximately 0.1 nm and about 5 nm. For example, depending upon the particular implementation, the thickness may be less than about 1 nm, less than about 0.5 nm, less than about 0.2 nm, may be the thickness corresponding to a single layer or monolayer of passivation material that is bonded to the semiconductor surface, or may even be the number of atoms of passivation material required to passivate substantially all the dangling bonds associated with the semiconductor surface **540**.

In some cases, passivation of the semiconductor surface **540** will include removing (or terminating) dangling bonds located proximate to the surface of the semiconductor material, including those at the surface as well as those within a few molecular dimensions from the surface. This process may stabilize the surface of the semiconductor material and may improve the controllability of subsequent fabrication operations. Passivation may also reduce the density of surface states that may exist at the semiconductor surface as a result of the discontinuation of the semiconductor crystal at the surface. This may improve consistency and performance of the semiconductor device, inasmuch as such states are known to interfere with proper device operation. For example, they may provide surface charge states that result in a pinning of the Fermi level.

III. Forming Interface Layers

Exemplary methods for forming interface layers to provide (i) passivation of semiconductor surfaces, and (ii) displacement of the semiconductor from the metal to eliminate or at least reduce of the effects of MIGS within the semiconductor when in the presence of the metal (collectively referred to herein as depinning the Fermi level of the semiconductor) with hydrogen, fluorine or nitrogen are presented below to further illustrate the concepts of the present invention. Other passivation materials may include arsenic, oxygen or an oxynitride, and in some cases such passivation layers are combined with separation layers (e.g., made of an oxide) to complete the interface layer.

A. Hydrogen and Fluorine

An interface layer may contain hydrogen, fluorine, or both hydrogen and fluorine (e.g., in the form of a hydride and/or a fluoride). One method for forming an interface layer on a semiconductor surface with hydrogen and fluorine includes cleaning the semiconductor substrate with a cleaning solution, immersing the cleaned substrate in a hydrogen fluoride solution (or other liquid containing hydrogen and fluorine ions) having an effective concentration typically between about 1%-50% by weight, waiting an effective period of time, typically between about several seconds and about 5 minutes, removing the substrate from the hydrogen fluoride solution, optionally rinsing the substrate in deionized water,

and blow-drying the substrate with nitrogen. Such a method may form an interface layer containing hydrogen and fluorine that are bonded (e.g., covalently) to the semiconductor surface.

It should be noted that long rinses in deionized water, generally longer than about 30 seconds, might remove the hydrogen passivation. Thus, deionized water rinses might advantageously be kept to less than about 30 seconds to maintain the hydrogen passivation of the surface. Also, the higher the concentration of the hydrogen fluoride during the immersion, the greater the concentration of fluorine passivation. Finally, methods are also contemplated where the ratio of hydrogen to fluorine passivation is altered by removing either the hydrogen or the fluorine.

An interface layer formed in this fashion may be best suited for applications where a subsequent metal layer is deposited over the interface layer in a generally non-invasive fashion, for example using a thermally evaporated source. Experiments by the present inventors to date suggest that using other approaches (e.g., plasma deposition) may cause damage to the thin (e.g., monolayer thick) interface layer contemplated as part of the present invention.

B. Nitrogen

In a further embodiment, an interface layer may contain nitrogen (e.g., in the form of silicon nitride). One method for forming an interface over a semiconductor surface with nitrogen includes heating a substrate containing the semiconductor surface in the presence of a nitrogenous material (that is, a gas or other material containing nitrogen). For example, a substrate containing an exposed silicon surface may be annealed at a temperature between about 300° C. and about 750° C., which is lower than temperatures conventionally used for Rapid Thermal Nitridation (RTN), under a gaseous ambient having, for example, ammonia (NH_3) at some effective partial pressure. By exposed, we mean a clean surface, free of everything except silicon. Such a method may form an interface layer containing nitrogen, often in the form of a nitride, bonded to the semiconductor surface. Note that the present inventors have observed indications suggesting that in these low temperature conditions interface layer growth is self-limiting, depending only on temperature.

According to another embodiment, an interface layer that includes nitrogen may be formed on an exposed surface of a semiconductor material by a method that includes heating a semiconductor material to a substantially high temperature under vacuum and exposing the semiconductor material to a substantially small amount of a nitrogenous material, such as ammonia. The method may include placing a semiconductor having an exposed semiconductor surface in a heating chamber, pulling a vacuum of less than about one millionth of a Torr, or more favorably an ultra high vacuum of less than 10-9 Torr, and then heating the semiconductor in the heating chamber to a substantially high temperature. The higher the vacuum, the longer the substrate may be heated without growth of an oxide from residual oxygen or water in the chamber. Thus, the process may include heating the semiconductor to a temperature that is between about 900° C. and about 1000° C., or higher, in an inert ambient. As desired, the semiconductor may be exposed to hydrogen gas, or an equivalent, to reduce any native oxide on the semiconductor. These high temperatures may provide for greater passivation of the semiconductor surface as compared with results that may be achieved at lower temperatures.

Then, the heated semiconductor may be exposed to a substantially small amount of a nitrogenous material, such as ammonia. This may include exposing the semiconductor surface to ammonia for a substantially short period of time. For example, the surface may be subjected to a burst or pulse of ammonia lasting for a time period between about 0.5 seconds and about 5 seconds. Alternatively, the surface may be exposed to a controlled, small amount of ammonia over an arbitrarily longer period of time. In this way, the substantially small amount of ammonia will react with the surface to form a nitrogenous interface layer, such as a nitride layer, thereon and then further growth of the interface layer will cease. Then the semiconductor may be cooled from the substantially high temperature to ambient temperature and removed from the heating chamber. Further annealing of the substrate and the grown nitride layer may also be performed in the vacuum chamber before removal, at a substantially elevated temperature between about 700° C. and 1000° C., or higher.

Advantageously, it has been unexpectedly observed that a process such as that described above and incorporating substantially high temperature exposure for substantially short periods may be used to controllably form thin yet effective interface layers. That is, the present inventors have observed that in the creation of thin interface layers that include nitrogenous materials, temperature appears to be a dominant factor in controlling thickness. For example, by such methods effective interface layers may be formed having a thickness that is less than about 1 nm, less than about 0.5 nm, less than about 0.2 nm, or having a thickness that corresponds to essentially a single monolayer sufficient to passivate essentially all dangling bonds proximate the semiconductor surface.

Further, thin interface layers may be advantageously grown on a semiconductor in the presence of nitrogen gas, or other inert nitrogen-containing gas. The reaction rate of a semiconductor such as silicon with nitrogen gas is significantly lower than that of a reactive nitrogen-containing gas such as ammonia. The slow growth rate may be desirable for better control of the growth of films of nitrogen on a semiconductor of a thickness of less than about 1 nm, less than about 0.5 nm, less than about 0.2 nm, or having a thickness that corresponds to essentially a single monolayer sufficient to passivate essentially all dangling bonds proximate the silicon surface.

IV. Diodes Containing Passivated Semiconductor Surfaces

Diodes made from Schottky barriers (i.e., asymmetric electrical potentials formed at a junction between a metal and a semiconductor) are widely used in rectifiers in power supply and control applications. As used herein, the terms Schottky diode, metal-semiconductor junction diode, diode, and rectifier are all related and appear in order from more specific at the left to more general at the right. Likewise, the terms Schottky barrier, metal-semiconductor barrier, conductor-semiconductor junction, and multi-material junction are all related and appear in order from more specific at the left to more general at the right. The term Schottky diode will be used to refer to a diode containing a Schottky barrier.

As mentioned above, the present inventors have devised a scheme to control or adjust a Schottky barrier height by forming an interface layer (which includes or sometimes consists of a passivation layer that includes an oxide, oxynitride, nitride, arsenide, hydride, fluoride, or an equivalent) between a metal and a semiconductor. This scheme differs from past attempts by others to control barrier height, which attempts generally involved either using a silicide as a contact metal (and thus limiting the choices of available

contact metals to those that can form silicides), or using esoteric substrates that exhibit wide bandgaps. Further, in previous devices the Fermi level of the semiconductor remains pinned, with the barrier height being virtually independent of the metal used. Finally, doping of substrates has also been attempted, however, it has not been shown to truly affect the barrier height of the substrate material. For example, PtSi contacts have reduced resistance due to high silicon doping such that the current across the junction is dominated by tunneling through the barrier. Doping may thus lead to cases where the top of the barrier may be so thin as to be essentially transparent to electrons, however, doping does not appear to allow actual tuning of the barrier height.

FIG. **6** shows an example of a diode **600** containing, according to one embodiment of the present invention, an interface layer **620** disposed between and attached to both a semiconductor **610** and a conductor **630**. The conductor and the semiconductor are operable to be electrically coupled with different voltages associated with the operation of the diode **600** and to pass electrical current through a passivated semiconductor surface formed at the junction between the semiconductor **610** and the interface layer **620**.

The conductor **630** contains a conductive material such as a metal or an alloy of a metal. The terms metal, conductive material, and conductor are all related and appear in order from specific at the left to general at the right. In general, the terms refer to a highly electrically conductive substance that has a Fermi energy level that sits in a partially filled band. Unless otherwise specified, conductors include metals (e.g., pure metals and alloys), and other conductors such as doped polysilicon (a nonporous silicon containing randomly oriented crystallites), doped single crystal silicon, and metal silicides. Note that alloys may have workfunctions different than their constituents and may be designed to have specific workfunctions though selective use of ratios of the constituent metals.

Often, the conductor is a metal since metals may offer advantages over conductive semiconductors including lower resistance, higher carrier mobilities that provide superior high frequency performance and switching, favorable low power characteristics, and ease of manufacturing control. Use of metals may also avoid the need to perform semiconductor doping, which may simplify manufacturing and improve quality control.

Metals that are contemplated include pure metals, alloys, refractory metals, metals that do not form silicides, metals physically deposited by substantially non-invasive processes such as by condensation of a thermally evaporated metal vapor, and metals having a predetermined work function. The use of non-invasively deposited metals may allow for forming the metal on a thin interface layer without disrupting the passivation properties of the layer.

A metal having a predetermined work function may be a metal having a work function smaller or greater than that of the semiconductor, depending on the desired application. Often, the semiconductor will be silicon. In this case by the work function of a semiconductor or silicon we mean the energy in the middle of the semiconductor bandgap. Exemplary metals that have a work function smaller than silicon include Group 3A elements, aluminum (Al), indium (In), titanium (Ti), chromium (Cr), tantalum (Ta), cesium (Cs), magnesium (Mg), erbium (Er), ytterbium (Yb), manganese (Mn), lead (Pb), silver (Ag), yttrium (Y), and zinc (Zn). Exemplary metals that have a work function greater than silicon include platinum (Pt), gold (Au), tungsten (W), nickel (Ni), molybdenum (Mo), copper (Cu), cobalt (Co), and palladium (Pd).

The semiconductor-interface layer-conductor configuration illustrated in FIG. **6** defines what the present inventors have chosen to call a "passivated Schottky barrier". The passivated Schottky barrier is a naturally formed electrical potential barrier to an electron or hole at the Fermi energy (the electrochemical potential) in the conductor due to a depletion region formed in the semiconductor adjacent the conductor. The passivated Schottky barrier may deviate in barrier height from a standard un-passivated Schottky barrier that would form naturally at a contact junction between the semiconductor and the conductor without the interface layer disposed therebetween. That is, the passivated Schottky barrier may have a barrier height that depends predominantly upon the bulk characteristics of the semiconductor and the conductor, rather than on surface properties, and may depend in part on the characteristics of the interface layer.

Indeed, the present inventors have determined that changes in barrier height are approximately monotonic and continuous for variations in surface passivation thickness by nitridation of the semiconductor substrate. More specifically, experiments by the present inventors in a regime where the nitride layer is sufficiently thick to remove MIGS show that temperature of interface layer formation has the strongest effect on barrier height. In other regimes, thickness may be critical. Ideally, if all surface states are removed, barrier height should be controllable simply by the choice of metal used.

To understand why thickness of the interface layer is important, refer briefly to FIG. **8** where a graph of interface-specific contact resistance versus interface thickness is shown. The graph is for a structure where the workfunction of the metal is the same as the electron affinity in the semiconductor, such that the Fermi level of the metal lines up with the conduction band of the semiconductor. At large thicknesses, the interface layer poses significant resistance to current. As thickness decreases, resistance falls due to increased tunneling current. However, there comes a point where even as the interface layer continues to get thinner, resistance increases. This is due to the effect of MIGS, which increasingly pull the Fermi level of the metal down towards mid-gap of the semiconductor, creating a Schottky barrier. The present inventors have discovered that this competition results in an optimum thickness, as shown in the illustration, where the resistance is a minimum. At this thickness the effect of MIGS has been sufficiently reduced to depin the metal and lower the Schottky barrier, and the layer is still sufficiently thin to allow significant current flow across the interface layer. Contact resistances of less than or equal to approximately 2500 Ω-μm^2, 1000 Ω-μm^2, 100 Ω-μm^2, 50 Ω-μm^2, 10 Ω-μm^2 or even less than or equal to 1 Ω-μm^2 may be achieved.

Characteristics that may be adjusted to provide a desired barrier height thus include the passivation material used (e.g., selection based on bandgap), the interface layer thickness (e.g., especially where the interface layer is a compound layer formed of a passivation layer and a separation layer), the method of forming the interface layer (e.g., control of parameters such as temperature), the interface layer thickness that is substantially similar to a penetration depth of MIGS formed at a metal interface, the metal used for the source and/or drain, and other characteristics.

One advantage of the ability to adjust the Schottky barrier height with the introduction of interface layer **620** is the ability to form a substantially high barrier height. For example, an interface layer may be used to create a Schottky barrier having a barrier height that is greater than can be

achieved through the use of metal silicides, greater than about 2.0 eV, or greater than about 2.5 eV (using a semiconductor with a bandgap at least this large), or nearly 1.0 V using silicon. Such high barrier heights imply the ability to withstand high voltages before breakdown occurs. Thus, Schottky barriers having such high barrier heights may be particularly useful in high-voltage Schottky diodes.

Another advantage achieved through the use of the interface layer **620** is greater flexibility afforded in selecting a conductor **630**. Typically, metals chosen for application in classic Schottky diodes are those that can form a silicide with a silicon semiconductor. The formation of the silicide helps to reduce surface states (resulting from dangling bonds), but not the effects of MIGS. Thus, the Fermi level at the semiconductor surface is still pinned. Using metals that form silicides upon contact with silicon may thus help to make the devices more reproducible in a manufacturing environment, but such devices still suffer from the drawback of having a barrier height that is fixed.

According to one embodiment of the present invention, however, one may select a conductor that is not able (or not readily able) to form a silicide with the semiconductor. The metal silicide is not needed because the interface layer provided in accordance with the present invention passivates the semiconductor surface and also reduces or eliminates the effect of MIGS. This may allow for selection of a metal that has properties such as a desirable work function or Fermi level energy, even though that metal may not form a metal silicide.

For example, to make large-barrier diodes, for an n-type doped silicon semiconductor, a metal may be selected that has a work function that is either substantially equal to the valence band energy of the semiconductor or that is within about 0.1 eV to about 0.3 eV of the valence band energy of the semiconductor. Similarly, for a p-type doped silicon semiconductor, a metal may be selected that has a work function substantially equal to the conduction band energy of the semiconductor. For Schottky diodes configured in accordance with the present invention, the Fermi level of the metal may lie anywhere in the bandgap of the semiconductor when an interface layer is disposed within the junction, resulting in diodes of various barrier heights. The Fermi level of the metal may also lie in the conduction or valence band of the semiconductor.

The use of interface layer **620** thus provides a way to tune, adjust, or control the height of the barrier between the conductor and the semiconductor. Without the interface layer **620**, the barrier height would be substantially untunable, un-adjustable, and fixed (as discussed above).

The role played by interface layer **620** in tuning, adjusting, or controlling the height of the barrier between the conductor **630** and the semiconductor **610** may be understood as a depinning of the Fermi level of the semiconductor. That is, the interface layer may reduce surface states by bonding to the semiconductor material to consume dangling bonds. Additionally, the interface layer may reduce the formation of MIGS in the semiconductor by providing a thickness and bandgap that prevent the electron wave function (of the metal) from penetrating into the semiconductor. The electron wave function may instead penetrate into the interface layer and form MIGS within the interface layer at an energy related to the states of the interface layer material. As desired, the density of the MIGS and the depth of MIGS penetration into the interface layer may be reduced by choosing an interface layer material or materials having a larger bandgap or higher effective mass than the semiconductor.

According to one embodiment of the present invention then, the interface layer **620** is incorporated into a device operable to pass current through the semiconductor surface and the interface layer during device operation. In such an embodiment, it may be desirable to use an interface layer having a thickness of a monolayer, or, for example between about 0.1 nm and about 0.3 nm, and also having a wide bandgap (as compared to that of the semiconductor) so that the interface layer both de-pins the Fermi level (so that the barrier height depends predominantly on bulk properties of the junction materials) and allows sufficient current transfer across it. Advantageously, such interface layers may be sufficiently thin to provide low impedance to current flow (due to the exponential dependence of direct tunneling on barrier thickness), which is desirable for many semiconductor devices, while also providing sufficient semiconductor surface passivation to allow an adjustable barrier height. That is, the interface layer may allow passivation of surface states and reduction (or elimination) of MIGS in the semiconductor to allow for an adjustable barrier height with a substantially thin layer that allows sufficient current to be transferred across the interface layer.

There are several methods by which the barrier height can be made adjustable. For example, adjustment may be made by tuning the degree of Fermi level pinning. In other words, some embodiments may allow for a sufficiently thin interface layer so that not all of the effects of MIGS in the Si are eliminated. Further, the pinning may be varied by combinations of thickness of the interface layer and the choice of interface material. The metal in contact with the interface layer may be pinned by MIGS at different levels in different materials. Conversely, or in addition, the passivation may be left incomplete to allow for an effective level of unpassivated states. Complete depinning of the Fermi level (that is removal of all surface states in Si including MIGS) is another option, in which case one could tune the barrier height simply by choosing a pure metal or an alloy that possesses the desired workfunction. In that case, the barrier height is determined by Equation (1), which until now has been an unrealizable idealization. Note that the type of tuning being discussed here is adjustment of the barrier height by altering the structure of the junction at the time of manufacture, not by varying an externally applied condition during junction operation.

FIG. **7***a*-**7***d* show relationships between Fermi energy, conduction band energy, and valence band energy for various Schottky barriers containing a metal in contact with (or in close proximity to) a semiconductor, where the bandgap (E_g) of the semiconductor exists between the conduction band (E_c) and the valence band (E_v). In this example, the work function of the metal Φ_M is chosen to be approximately equal to the electron affinity χ_S of the semiconductor. In FIG. **7***a*, an unpassivated Schottky barrier **700** is shown. In this example, the Fermi level (E_F) of the metal **730** is pinned in the bandgap of the semiconductor **710**. This results in a discontinuity in the vacuum level caused by a charged dipole at the interface.

In FIG. **7***b*, the interface layer **720***b* is thick enough to passivate dangling bonds at the surface of the semiconductor **710**, but not thick enough to eliminate or sufficiently reduce the effect of MIGS. As a result, the band structure is largely unaltered from that seen in the previous illustration. Similarly, in FIG. **7***c*, when the interface layer **720***c* is sufficiently thick to eliminate or reduce the effect of MIGS but not to passivate the semiconductor surface, little change in the energy band structure is observed. However, as shown in FIG. **7***d*, when the interface layer **720***d* is sufficient to both

eliminate or reduce the effect of MIGS and to passivate the semiconductor surface, we see the Fermi level of the metal aligning with the conduction band of the semiconductor (i.e., the Fermi level of the semiconductor has been depinned and no longer lines up with the Fermi level of the metal). The vacuum level is now continuous as there is no charged dipole at the interface. Thus, the band structure of a device constructed in this fashion is a result of only bulk material properties, not properties of the surface. By way of example, the materials in such cases may be Al and Si, with a work function for Al of approximately Φ_M=4.1 eV and the electron affinity for Si of approximately χ_S=4.05 eV.

V. Transistors Containing Passivated Semiconductor Surfaces

The interface layers described herein may be used in connection with a semiconductor surface of a channel in a field effect transistor. That is, an interface layer may be disposed between a source and a channel, a channel and a drain, or both of an insulated gate field effect transistor. Such use of an interface layer is described in detail in co-pending U.S. Pat. No. 6,833,556, issued Dec. 21, 2004, entitled "INSULATED GATE FIELD EFFECT TRANSISTOR HAVING PASSIVATED SCHOTTKY BARRIERS TO THE CHANNEL", filed Jan. 14, 2003 by the present inventors, and assigned to the assignee of the present invention.

The source and drain contacts at the channel of a field effect transistor are examples of a broader category of metal-interface layer-semiconductor contacts that make up the present invention. In the past, such contacts generally comprised a silicide-n+-Si junction, which formed a somewhat "leaky" Schottky diode, with a Fermi level of the semiconductor pinned at the midgap. In contrast, the present invention provides a contact wherein the Fermi level of the metal is aligned with the conduction band of the semiconductor (e.g., as shown in FIG. 7*d*). Note that in other cases, depending on the type of semiconductor material and conductors used, the Fermi level of the metal may align with the valence band of the semiconductor.

Although both types of junctions (i.e., the new passivated Schottky barrier junction and the conventional silicide-semiconductor junction) permit tunneling currents, the present junction can be fabricated with a much thinner interface layer as compared to the thickness of the silicide layer used previously. Indeed, thickness of an order of magnitude less than the silicide thickness can be expected. In a conventional silicide-semiconductor junction a Schottky barrier is formed which is comprised of a depletion layer. The tunnel barrier presented by such a depletion layer may be an order of magnitude thicker than the dielectric tunnel barrier in the present invention. The thinner interface layers provided by the present invention permit higher current across the junction (i.e., lower junction specific contact resistance).

Two other properties of the dielectric deserve mention. First is the property of the height of the barrier compared to the semiconductor conduction band (for electrons). In making the barrier thinner than a silicide barrier, the tradeoff may be a higher tunnel barrier (e.g., 2 eV for nitride, compared with about half the gap of 0.6 eV for silicide). Spacer layers may be used with lower barriers (e.g., TiO_2 has a barrier of less than 1 eV). Nevertheless, even with the higher barrier to electrons, the present inventors have determined that the resistance can still be one hundred times lower than a contact to silicon with a silicide barrier.

The second property is the effective mass of electrons in the dielectric. Larger mass electrons will not penetrate as far (i.e., because of their shorter wavelength) from the metal into the semiconductor. The less the electrons penetrate into the dielectric, the less the effect of MIGS in the dielectric. Thus, MIGS in the dielectric are reduced with larger bandgap and larger effective mass.

In addition the junction of the present invention can be used in making contacts to source or drain implanted wells and will have the advantage of reducing the need for high doping levels (which are now reaching their limits of solid solubility). The high doping profiles were required in the past in order to keep the junction depletion layer relatively thin, so as to increase the tunneling current, thus reducing the junction resistance. However, it is becoming increasingly difficult to increase doping profiles in order to provide low resistance junctions. It may be possible to reach the same level of resistance with a lower doping concentration using the present invention. It may further be possible to achieve much lower resistance even with lower doping concentration. When the present invention is used with high doping levels, the resistance will be further reduced.

Thus, methods and applications for semiconductor-interface layer-metal junctions have been described. Although described with reference to specific embodiments it should be remembered that various modifications and changes may be made to the techniques described herein without departing from the broader spirit and scope of the invention. The specification and drawings are accordingly to be regarded in an illustrative rather than a restrictive sense and the invention measured only in terms of the claims, which follow.

What is claimed is:

1. A structure, comprising a semiconductor region in a substrate, a metal electrical contact to said semiconductor region, and a passivating dielectric tunnel barrier layer between said semiconductor region and said metal electrical contact, said semiconductor region being electrically connected to said metal electrical contact through said passivating dielectric tunnel barrier layer, wherein said passivating dielectric tunnel barrier layer comprises a metal oxide and a semiconductor oxide.

2. The structure of claim **1**, wherein the semiconductor oxide comprises an oxide of the semiconductor region.

3. The structure of claim **1**, wherein the semiconductor oxide of the dielectric tunnel barrier layer has a thickness of approximately 0.1 nm to 5 nm.

4. The structure of claim **3**, wherein the semiconductor region comprises an n-type doped source or drain of a transistor.

5. The structure of claim **3**, wherein the metal electrical contact is a metal or a stack of metals deposited on the dielectric tunnel barrier layer.

6. The structure of claim **3**, wherein the metal oxide of the dielectric tunnel barrier layer comprises an oxide of titanium.

7. The structure of claim **6**, wherein the semiconductor oxide of the dielectric tunnel barrier layer has a thickness of approximately less than 1 nm.

8. The structure of claim **6**, wherein the semiconductor region comprises an n-type doped source or drain of a transistor.

9. The structure of claim **6**, wherein the metal electrical contact is a metal or a stack of metals deposited on the dielectric tunnel barrier layer.

10. The structure of claim **6**, wherein the semiconductor oxide comprises an oxide of silicon.

11. The structure of claim **6**, wherein the semiconductor oxide of the dielectric tunnel barrier layer is adjacent the semiconductor region.

12. The structure of claim **6**, wherein the metal electric contact comprises titanium.

13. The structure of claim **3**, wherein the semiconductor oxide comprises an oxide of silicon.

14. The structure of claim **13**, wherein the metal electrical contact is a metal or a stack of metals deposited on the dielectric tunnel barrier layer.

15. The structure of claim **13**, wherein the metal oxide of the dielectric tunnel barrier layer comprises an oxide of titanium.

16. The structure of claim **15**, wherein the metal electrical contact comprises titanium.

17. The structure of claim **15**, wherein the semiconductor comprises an n-type doped source or drain of a transistor.

18. The structure of claim **17**, wherein a specific contact resistivity between the n-type doped source or drain and the metal electric contact is less than 1 $\Omega \cdot \mu m^2$.

19. The structure of claim **1**, wherein the semiconductor region comprises silicon, the semiconductor oxide comprises an oxide of silicon, the metal oxide of the dielectric tunnel barrier layer comprises an oxide of titanium, and the metal electrical contact comprises titanium.

20. The structure of claim **1**, wherein the dielectric tunnel barrier layer is configured to reduce a height of a Schottky barrier between the metal electrical contact and the semiconductor region from that which would exist at a contact junction between the metal electrical contact and the semiconductor region without the dielectric tunnel barrier layer disposed therebetween.

21. The structure of claim **1**, wherein for a specified contact resistivity of the structure the dielectric tunnel barrier layer has a thickness less than that which would exist for a silicide layer at a contact junction between the metal electrical contact and the semiconductor region.

22. The structure of claim **1**, wherein the dielectric tunnel barrier layer is configured to reduce contact resistivity between the metal electrical contact and the semiconductor region from that which would exist at a contact junction between the metal electrical contact and the semiconductor region without the dielectric tunnel barrier layer disposed therebetween.

23. The structure of claim **1**, wherein the semiconductor oxide of the dielectric tunnel barrier layer comprises an oxide of silicon having a thickness of approximately 0.1 nm to 5 nm, the semiconductor region comprises an n-type doped source or drain of a transistor, and the metal electrical contact comprises an oxide of titanium.

24. The structure of claim **23**, wherein the semiconductor oxide of the dielectric tunnel barrier layer is adjacent the semiconductor region.

25. An electrical junction comprising an interface layer disposed between a contact metal and a semiconductor, the semiconductor comprising a source or drain of a transistor, the interface layer comprising a metal oxide separation layer and a semiconductor oxide passivation layer and configured to provide a specific contact resistivity between the contact metal and the semiconductor of less than 1 $\Omega \cdot \mu m^2$.

26. The electrical junction of claim **25**, wherein the metal oxide separation layer comprises an oxide of titanium.

27. The electrical junction of claim **26**, wherein the semiconductor oxide passivation layer comprises an oxide of the semiconductor.

28. The electrical junction of claim **27**, wherein the semiconductor oxide passivation layer has a thickness of approximately 0.1 nm to 5 nm.

29. The electrical junction of claim **27**, wherein the semiconductor oxide passivation layer is adjacent the semiconductor.

30. The electrical junction of claim **25**, wherein the contact metal is a metal or a stack of metals deposited on the interface layer.

* * * * *

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO.	: 9,905,691 B2
APPLICATION NO.	: 15/048877
DATED	: February 27, 2018
INVENTOR(S)	: Daniel E. Grupp and Daniel J. Connelly

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

In Column 18, at Line 33 (Claim 1, Line 3), replace "and" with --a metal oxide layer, and--; at Line 37 (Claim 1, Line 7), after "dielectric tunnel barrier layer" insert --and said metal oxide layer--; at Lines 38-39 (Claim 1, Lines 8-9), delete "metal oxide and a"; and at Lines 51-52 (Claim 6, Lines 1-2), delete "of the dielectric tunnel barrier".

In Column 19, at Lines 8-9 (Claim 15, Lines 1-2), delete "of the dielectric tunnel barrier"; and at Lines 20-21 (Claim 19, Lines 3-4), delete "of the dielectric tunnel barrier".

Signed and Sealed this
Fifteenth Day of May, 2018



Andrei Iancu
Director of the United States Patent and Trademark Office

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(12) **United States Patent**
Grupp et al.

(10) **Patent No.: US 10,090,395 B2**
(45) **Date of Patent: Oct. 2, 2018**

(54) **METHOD FOR DEPINNING THE FERMI LEVEL OF A SEMICONDUCTOR AT AN ELECTRICAL JUNCTION AND DEVICES INCORPORATING SUCH JUNCTIONS**

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(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

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(Continued)

(56) **References Cited**

U.S. PATENT DOCUMENTS

3,513,366 A 5/1970 Clark
3,590,471 A 7/1971 Lepselter et al.
(Continued)

FOREIGN PATENT DOCUMENTS

EP 0295490 A1 12/1988
EP 0789388 A2 8/1997
(Continued)

OTHER PUBLICATIONS

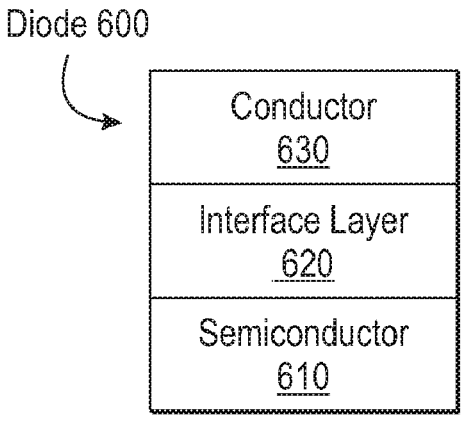
Acorn Technologies, Inc., International Application No. PCT/US2012/060893 filed Oct. 18, 2012, ISA/US, International Search Report and Written Opinion, dated Dec. 11, 2012, 23 pages.
(Continued)

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(57) **ABSTRACT**

An electrical device in which an interface layer is disposed in between and in contact with a conductor and a semiconductor.

30 Claims, 6 Drawing Sheets



Related U.S. Application Data

No. 15/251,210, filed on Aug. 30, 2016, now Pat. No. 9,812,542, which is a continuation of application No. 15/048,877, filed on Feb. 19, 2016, now Pat. No. 9,905,691, which is a continuation of application No. 13/552,556, filed on Jul. 18, 2012, now Pat. No. 9,425,277, which is a continuation of application No. 13/022,522, filed on Feb. 7, 2011, now Pat. No. 8,431,469, which is a division of application No. 12/197,996, filed on Aug. 25, 2008, now Pat. No. 7,884,003, which is a division of application No. 11/181,217, filed on Jul. 13, 2005, now Pat. No. 7,462,860, which is a continuation of application No. 10/217,758, filed on Aug. 12, 2002, now Pat. No. 7,084,423.

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See application file for complete search history.

(56) **References Cited**

U.S. PATENT DOCUMENTS

3,708,360	A	1/1973	Wakefield, Jr. et al.	
3,983,264	A	9/1976	Schroen et al.	
3,983,574	A	9/1976	Statz et al.	
4,019,113	A	4/1977	Hartman	
4,056,642	A	11/1977	Saxena et al.	
4,300,152	A	11/1981	Lepselter	
4,338,616	A	7/1982	Bol	
4,422,090	A	12/1983	Shepherd et al.	
4,485,550	A	12/1984	Koeneke et al.	
4,566,021	A	1/1986	Yokoyama	
4,583,110	A	4/1986	Jackson et al.	
4,723,197	A	2/1988	Takiar et al.	
4,811,077	A	3/1989	Fowler et al.	
4,843,029	A	6/1989	Joyce et al.	
4,999,685	A	3/1991	Waldrop et al.	
5,021,365	A	6/1991	Krichner et al.	
5,027,166	A	6/1991	Ohtsuka et al.	
5,098,859	A	3/1992	Jackson et al.	
5,243,213	A	9/1993	Miyazawa et al.	
5,308,998	A	5/1994	Yamazaki et al.	
5,399,206	A	3/1995	De Lyon	
5,438,210	A	8/1995	Worley	
5,578,848	A	11/1996	Kwong et al.	
5,596,218	A	1/1997	Soleimani et al.	
5,608,266	A	3/1997	Agnello et al.	
5,612,567	A	3/1997	Baliga	
5,663,584	A	9/1997	Welch	
5,801,398	A	9/1998	Hebiguchi	
5,801,444	A	9/1998	Aboelfotoh et al.	
5,888,891	A	3/1999	Gould	
5,908,313	A	6/1999	Chau et al.	
5,939,763	A	8/1999	Hao et al.	
5,943,575	A	8/1999	Chung et al.	
6,011,271	A	1/2000	Sakkuma et al.	
6,037,605	A	3/2000	Yoshimura	
6,064,082	A	5/2000	Kawai et al.	
6,071,783	A	6/2000	Liang et al.	
6,091,076	A	7/2000	Deleonibus et al.	
6,096,590	A	8/2000	Chan et al.	
6,117,781	A	9/2000	Lukanc et al.	
6,150,286	A	11/2000	Sun et al.	
6,198,113	B1	3/2001	Grupp	
6,207,976	B1	3/2001	Takahashi et al.	
6,261,932	B1	7/2001	Hulfachor	
6,291,282	B1	9/2001	Wilk et al.	
6,291,866	B1	9/2001	Wallace et al.	
6,291,867	B1	9/2001	Wallace et al.	
6,293,137	B1	9/2001	Liu et al.	
6,303,479	B1	10/2001	Snyder	
6,326,294	B1	12/2001	Jang Ha Soon et al.	
6,339,232	B1	1/2002	Takagi	
6,344,673	B1	2/2002	Aussilhou	
6,380,021	B1	4/2002	Wang et al.	
6,452,244	B1	9/2002	Miura et al.	
6,462,931	B1	10/2002	Tang et al.	
6,492,735	B1	12/2002	Matsubara	
6,548,875	B2	4/2003	Nishiyama	
6,608,352	B1	8/2003	Long et al.	
6,680,224	B2	1/2004	Shin et al.	
6,724,068	B2	4/2004	Matsuyama	
6,724,088	B1	4/2004	Jammy et al.	
7,057,333	B1	6/2006	Vu Thien et al.	
7,084,423	B2	8/2006	Grupp et al.	
7,176,483	B2	2/2007	Grupp et al.	
8,110,877	B2	2/2012	Mukherjee et al.	
8,952,541	B2	2/2015	Mukherjee et al.	
2001/0028067	A1	10/2001	Awano	
2002/0061646	A1	5/2002	Kan et al.	
2002/0158250	A1	10/2002	Fujisaki et al.	
2002/0175386	A1	11/2002	Kim et al.	
2003/0009463	A1	1/2003	Gallant	
2003/0012146	A1	1/2003	Novaes	
2003/0022474	A1	1/2003	Grover et al.	
2003/0121468	A1	7/2003	Boone et al.	
2003/0127700	A1	7/2003	Moddel et al.	
2003/0132466	A1	7/2003	Shin et al.	
2003/0219965	A1	11/2003	Cabral et al.	
2003/0235936	A1	12/2003	Snyder et al.	
2004/0026687	A1	2/2004	Grupp et al.	
2004/0142524	A1	7/2004	Grupp et al.	
2005/0009302	A1	1/2005	Wakui et al.	
2005/0037557	A1	2/2005	Doczy et al.	
2005/0093027	A1	5/2005	Grupp et al.	
2007/0141798	A1*	6/2007	Bohr	H01L 21/28079 438/301
2011/0092047	A1	4/2011	Gaines et al.	
2014/0117465	A1*	5/2014	Huang	H01L 29/78 257/411
2015/0001643	A1*	1/2015	Kim	H01L 21/28229 257/410

FOREIGN PATENT DOCUMENTS

WO	WO 2004/015782 A1	2/2004
WO	WO 2004/030104 A1	4/2004

OTHER PUBLICATIONS

"Patents Act 1977: Examination Report under Section 18(3)", UK Intellectual Property Office dated Apr. 29, 2015, Application No. GB1409999.8 (filed Oct. 18, 2012), 5 pgs.

(56) **References Cited**

OTHER PUBLICATIONS

"Research Achievements", Research Achievements at RCIQE, downloaded Apr. 12, 2002, from: http://www.rciqe.hokudai.ac.jp/RCIQEold/ResearchAchievements.html, 8 pgs.

Aberle, Armin G., et al., "Injection-Level Dependent Surface Recombination Velocities at The Silicon-Plasma Silicon Nitrite Interface", Institute fur Solarenergieforschung, ISFH, D-3 1860 Emmerthal, Germany, (Mar. 9, 1995), pp. 2828-2830.

"International Search Report and Written Opinion of the International Searching Authority", Patent Cooperation Treaty (dated Mar. 2, 2006), PCT/US2005/030209, 6 pgs.

"International Search Report", Patent Cooperation Treaty (dated Dec. 18, 2003), PCT/US03/25057, 4 pgs.

Adam; et al., "Experimental Identification of Nitrogen-Vacancy Complexes in Nitrogen Implanted Silicon", Applied Physics Letters (Jul. 2001), 79(5):623-625.

Alers; et al., "Effects of Thermal Stability and Roughness on Electrical Properties of Tantalus Oxide Gates", MRS Proceedings (1999), 567:391-395.

Almeida; et al., "Reaction-Diffusion Model For Thermal Growth of Silicon Nitrite Films on Si", Physical Review B (Dec. 2000), 62(24):R16255-R16258.

Aboelfotoh, "Influence of thin interfacial silicon oxide layers on the Schottky-barrier behavior of Ti on Si(100)", Phys Rev B Condens Matter (Mar. 1989), 39(8):5070-5078.

Bauernschmitt, et al., "Transition from MOS to Schottky-contract behaviour in Yb—SiO2—Si Tunneling Junctions with extremely thin SiO2 layer", Microelectronic Engineering (1993), 22:105-108.

Baumvol, "Atomic Transport During Growth of Ultrathin Dielectrics on Silicon", Surface Science Reports (Dec. 1999), 36(1-8):1-166.

Berger, "Contact Resistance and Contact Resistivity" J. Electrochem. Soc.: Solid-State Science and Technology (1972), 119(4):507-514.

Bannikov; et al., "Field-Effect Transistor With Metal-(Tunneling-Insulator)-Semiconductor Contacts and a Gate Insulator Made of A Mangmuir-Blodgett Film", Soviet Technical Physics Letters (Mar. 1989), 15(3):211-212.

Bringans, "Arsenic Passivation of Si and Ge Surfaces", Critical Reviews in Solid State and Materials Sciences I(1992), 17(4):353-395.

Cai; et al., "Investigation of The Properties of Plasma-Enhanced Chemical Vapor Deposition Silicon Nitrite And its Effect on Silicon Surface Passivation", Journal of Applied Physics (May 1998), 83(11):5885-5889.

Blosse; et al., "A Novel Low Cost 65nm CMOS Process Architecture With Self Aligned Isolation and W Cladded Source/Drain", IEEE, Transactions of 2004 International Electron Device Meeting (Jan. 2005), pp. 669-672.

Chadi; et al., "Fermi-Level-Pinning Defects in Highly n-Doped Silicon", Physical Review Letters (Dec. 1997), 79(24):4834-4837.

Card; et al., "Studies of tunnel MOS diodes I. Interface effects in silicon Schottky diodes", Journal of Physics D: Applied Physics (1971), 4(10):1589-1601.

Chen; et al., "High Quality Native-Oxide-Free Ultrathin Oxide Grown by In-Situ HF-Vapor Treatment", Electronic Letters, (May 2000), 36(11):981-983.

Chaneliere; et al., "Tantalum Pentoxide (Ta2O5) Thin Films for Advanced Dielectric Applications"; Materials Science and Engineering, R: Reports (May 1998), 22(6):269-322.

Connelly; et al., "Optimizing Schottky S/D Offset for 25-nm Dual-Gate CMOS Performance", Electron Device Letters, IEEE (Jun. 2003), 24(6)411-413.

Gilmer; et al., "Process and Manufacturing Challenges For High-K Gate Stack Systems", MRS Proceedings, MRS Spring Meeting (1999), 567:323-341.

Edelstein; et al., "Full Copper Wiring in a Sub-0.25 mm CMOS ULSI Technology", Proceedings of the IEEE International Electron Device Meeting (1997), pp. 773-776.

Hara, et al., "Control of Schottky And Ohmic Interfaces by Unpinning Fermi Level", Applied Surface Science (1997), 117-118:394-399.

Hara; et al., "Pinning-Controlled Metal/Semiconductor Interfaces", Proc. SPIE 2779, 3rd International Conference on Intelligent Materials and 3rd European Conference on Smart Structures and Materials (Apr. 1996), 2779:802-807.

Hara; et al., "Pinning-Controlled Ohmic Contacts: Application to SiC(0001)", Applied Surface Science (Nov. 1996), 107:218-221.

Hasegawa; et al., "Unpinning of Fermi Level in Nanometer-Sized Schottky Contacts on GaAs and InP", Applied Surface Science (2000): 166:92-96.

Gopalakrishnan; et al., "Impact Ionization MOS (I-MOS)—Part I: Device and Circuit Simulations", IEEE Transactions Electron Devices (Jan. 2005), 52(1):69-76.

Heine, "Theory of Surface States", Physical Review (Jun. 1965), 138(6A):83-4.

Hilsenbeck; et al., "Aging Behavior of Algan HFETs With Advanced Ohmic And Schottky Contacts", Electronic letters (May 2000), 38(11):980-981.

Huang, "Metal-Oxide Semiconductor Field-Effect Transistors Using Schottky Barrier Drains", Electronics Letters (1797), 33(15):1341-1342.

Huang; et al., "Two-Dimensional Numerical Simulation of Schottky Barrier MOSFET with Channel Length to 10 nn", IEEE (Apr. 1998), pp. 842-848.

Hayafuji; et al., "Nitridation of Silicon and Oxidized-Silicon", J. Electrochem. Soc. (1982), 129(9):2102-2108.

International Search Report, PCT/US2004/042084, dated Sep. 1, 2005, 4 pgs.

Izumi, "43 Hydrogen Termination: The Ideally Finished Silicon Surface", Ultraclean Surface Processing of Silicon Wafers (1998), pp. 559-565.

Kamins; et al., "Effect of Hydrogen on p-Type Epitaxial Silicon Sheet-Resistance Measurements", Electrochemical and Solid-State Letters (1998), 1(2):100-101.

Kamiyama; et al., "Ultrathin Tantalum Odise Capacitor DIELECTRIC Layers Fabricated Using Rapid Thermal Nitridation Prior to Low Pressure Chemical Vapor Deposition", J. Electrochem Soc. (1993), 140(6)1617.

Kaxiras, "Efthimios. Semiconductor-surface restoration by valence-mending adsorbates: Application to Si (100): S and Si (100): Se", Phys Rev B Condens Matter (Mar. 1991), 43(18):6824-6827.

Kedzierski; et al., "Extension and Source/Drain Design for High-Performance FinFET Devices", IEEE Trans. Electron Devices (Apr. 2003), 50(4):952-958.

Keller; et al., "Calculations of the barrier height and charge distribution of a metal-dielectric interface", Journal of Vacuum Science & Technology A: Vacuum, Surfaces, and Films (Jul. 1992), 10(4):775-780.

Kim; et al., "Metal-Dependent Fermi-Level Movement in The Metal/Sulfer-Passivated InGaP Contact", Journal of Vacuum Science & Technology A: Vacuum, Surfaces, and Films (1997), 15(3):1124-1128.

Kimura; et al., "A New Type of Schottky Tunnel Transistor", IEEE Electron Device Letters (Oct. 1994), 15(10): 412-414.

Lee; et al., "Electronic Property of Metallic Nanoclusters on Semiconductor Surfaces: Implications For Nanoelectronic Device Applications", Journal of Nanoparticle Research (Dec. 2000), 2(4):345-362.

Louie; et al., "Ionicity And The Theory of Schottky Barriers", Physical Review B (Feb. 1977), 15(4):2154-2162.

Mandelis; et al., "Evidence of a Surface Acceptor State in Undoped Semi-Insulating GaAs by Photothermal Radiometric Deep Level Transient Spectroscopy", Sociedad Mexicana de Ciencias de Superficies y de Vacio, (1999), 8:13-17.

Martel; et al., "Ambipolar Single-Wall Carbon Nanotube Transistors and Inverters", AIP Conference Proceedings (Mar. 2001). 591:543-547.

McKee; et al., "Physical Structure And Inversion Charge at a Semiconductor Interface With a Crystalline Oxide", Science (Jul. 2001), 293(5529):468-471.

(56) **References Cited**

OTHER PUBLICATIONS

McKinley; et al., "Control of Ge homojunction band offsets via ultrathin Ga—As dipole layers", Applied Surface Science (1992), 56-58(Part 2):762-765.

McKinley; et al., "Controlled modification of heterojunction band lineups by diffusive intralayers", Journal of Vacuum Science & Technology A Vacuum Surfaces and Films (May/Jun. 1990), 8(3):1917-21.

Miyawaki; et al., "Improvement of Aluminum-Si Contact Performance in Native-Oxide-Free Processing", IEEE Electron Device Letters (Oct. 1990), 11(10):448-450.

Nauka; et al., "Surface Photovoltage Measurement of Hydrogen-Treated Si Surfaces", Journal of Electrochemical Society (1999), 146(1):292-295.

Nishioka; et al., "Dielectric Characteristics of Fluorinated Ultradry SiO2", Appl. Phy. Letters (Mar. 1989), 54(12):1127-1129.

Okamoto; et al., "Near-Ohmic Contact of n-GaAs with GaS/GaAs Quaisi-Metal-Insulator-Semiconductor Structure", Jpn. J. Appl. Phys. (1998), 37:3248-3251.

Padovani, "Forward Voltage-Current Characteristics of Metal-Silicon Schottky Barriers", Journal of Applied Physics (1967), 38(2):891-892.

Park; et al., "Thermal stability of molybdenum-silicon nitride-silicon Schottky diodes", Journal of Applied Physics (Mar. 1991), 69(5):3149-3153.

Patel; et al., "Arsenic Atom Location on Passive Silicon (111) Surfaces", Physical Review B (Nov. 1987), 36(14):7715-17.

Porter; et al., "A Critical Review of Ohmic and Rectifying Contacts For Silicon Carbide", Material Science and Engineering: B (Nov. 1995), 34(2-3):83-105.

Ren; et al. "Metal I Silicon Schottky Barrier Lowering By RTCVD Interface Passivation" Electrochemical Society Proceedings (2000), 2000-9:161-166.

Ruzyllo; et al., "Semiconductor Glossary An Introduction to Semiconductor Terminology", Prosto Multimedia Publishing (2004), pp. 26.

Schmidt; et al., "Carrier Recombination at Silicon-Silicon Nitride Interfaces Fabricated by Plasma-Enhanced Chemical Vapor Deposition", Journal of Applied Physics (Apr. 1999), 85(7):3626-3633.

Shalish; et al., "Yellow Luminescence And Fermi Level Pinning in GaN Layers", Appl Phys Lett (Aug. 2000), 77(7):987-989.

Snyder; et al., "Experimental Investigation of a PtSi Source And Drain Field Emission Transister", Appl Phys Lett (1995), 67:1420-1422.

Sobolewski; et al., "Properties of Ultrathin Thermal Nitrides in Silicon Schottky Barrier Structures", Applied Physics Letters, American Institute of Physics (1989), 54(7):638-640.

Sobolewski; et al., "Studies of barrier height mechanisms in metal-silicon nitride-silicon Schottky barrier diodes", Journal of Vacuum Science & Technology B (1989), 7:971-979.

Spicer; et al., "Unified Mechanism For Schottky-Barrier Formation And III-V Oxide Interface States", Physical Review Letters (Feb. 1980), 44(6):420-423.

Sze, "Metal-Semiconductor Contacts", Physics of Semiconductor Devices, John Wiley & Sons, (1981), pp. 245-311.

Takahagi; et al., "The formation of hydrogen passivated silicon singlecrystal surfaces using ultraviolet cleaning and Hf etching", J Appl Phys (1988), 64(7):3516-21.

Tao; et al., "Removal of dangling bonds and surface states on silicon (001) with a monolayer of selenium", Applied Physics Letters (Mar. 2003), 82(10)1559-1561.

Tao; et al., "Suppression of silicon (001) surface reactivity using a valence-mending technique", Solid State Communications (Oct. 2004), 132(2):89-92.

Taubenblatt; et al., "Interface effects in titanium and hafnium Schottky barriers on silicon", Appl Phys Lett (May 1984), 44:895-897.

Teraji; et al., "Ohmic Contacts To n-Type 6H-SiC Without Post-Annealing", Material Research Society, MRS Spring Meeting (1996), 423:149-154.

Tersoff, "Schottky Barrier Heightsand The Continuum of Gap States", Physical Review Letters (Feb. 1984), 52(6):465-468.

Thanailakis; et al., "Transition-metal contacts to atomically clean silicon, Department of Electrical Engineering and Electronics", Journal of Physics C: Solid State Physics (1976), 9:337-343.

Thompson; et al., "A Logic Nanotechnology Featuring Strained-Silicon", IEEE Electron Device Letters (Apr. 2004),25(4):191-193.

Tung, "Electron Transport of Inhomogeneous Schottky Barriers", Appl Phys Letter (1991), 58(24):2821-2823.

Udeshi; et al., "Thermal stability of ohmic contacts between Ti and Sepassivated n-type Si(001)", J Appl Phys (2004), 95(8):4219-4222.

Uemoto, "Reduction of Ohmic Contact Resistance on N-Type 6H-SIC By Heavy Doping", Japanese Journal of Applied Physics (Jan. 1995), 34(Parts 2, No. 1A).

Verhaverbeke; et al., "Surface Characterization of Si After HF Treatments and its Influence in the Dielectric Breakdown of Thermal Oxides", MRS Proceedings (1992), 259:391-399.

Wang; et al., "High Barrier GaN Schottky Diodes: Pt/GaN and Pd/GaN", Appl. Phys. Letters (Feb. 1996), 68(9):1267-1270.

Wei; et al., "The Use of Selective Electroless Metal Deposition For Micron Size Contact Fill", IEEE International Electron Device Meeting Technical Digest (1988), pp. 446-449.

Weinberger; et al., "Surface Chemistry of HF Passivation Silicon: X-Ray Photoelectron And Ion Scattering Spectroscopy Results", J. Appl. Phys (Nov. 1986), 60(9):3232-34.

Widjaja; et al., "Ab Initlo Study and Decomposition of NH3 on Si(100)-(2x1)", J. Phy. Chem B, (2000), 104:2527-2533.

Wittmer; et al., "Ideal Schottky diodes on passivated silicon", Phys Rev Lett (Nov. 1992), 69(18):2701-2704.

Wolf; et al., "Spintronics: A Spin-Based Vision For The Future", Science (Nov. 2001), 294(5546):1488-95.

Wright; et al., "Hot-Electron Immunity of SiO2 Dielectrics with Fluorine Incorporation", IEEE Electron Device Letters (1989), 10(8):347-348.

Yablonovitch; et al., "Unusually Low Surface-Recombination Velocity on Silicon and Germanium Surfaces", Physical Review Letters (Jul. 1986), 57(2):249-252.

Yagishita; et al., "High Performance Damascene Metal Gate MOSFET's for 0.1 mm Regime", IEEE Trans. Electron Devices (2000), 47(5):1028-1034.

Yang; et al., "The Effects of Interfacial Sub-Oxide Transition Regions and Monolayer Level Nitridation on Tunneling Currents in Silicon Devices", IEEE Electron Device Letters (2000), 21(2):76-78.

Zhang; et al., "Schottky diodes of NiÕAu on n-GaN grown on sapphire and SiC substrates", Applied Physics Letters (Oct. 2001), 79(16):2567-69.

Zhu; et al., "Low-Resistance Ti/n-Type Si(100) Contacts by Monolayer Se Passivation", ECS Trans (2006), 2(2):401-409.

Zhu; et al., "Stability of Se passivation layers on Si(001) surfaces characterized by time-of-flight positron annihilation induced Auger electron spectroscopy", Journal of Applied Physics (2005), 97(10):103510-1103510-4.

* cited by examiner

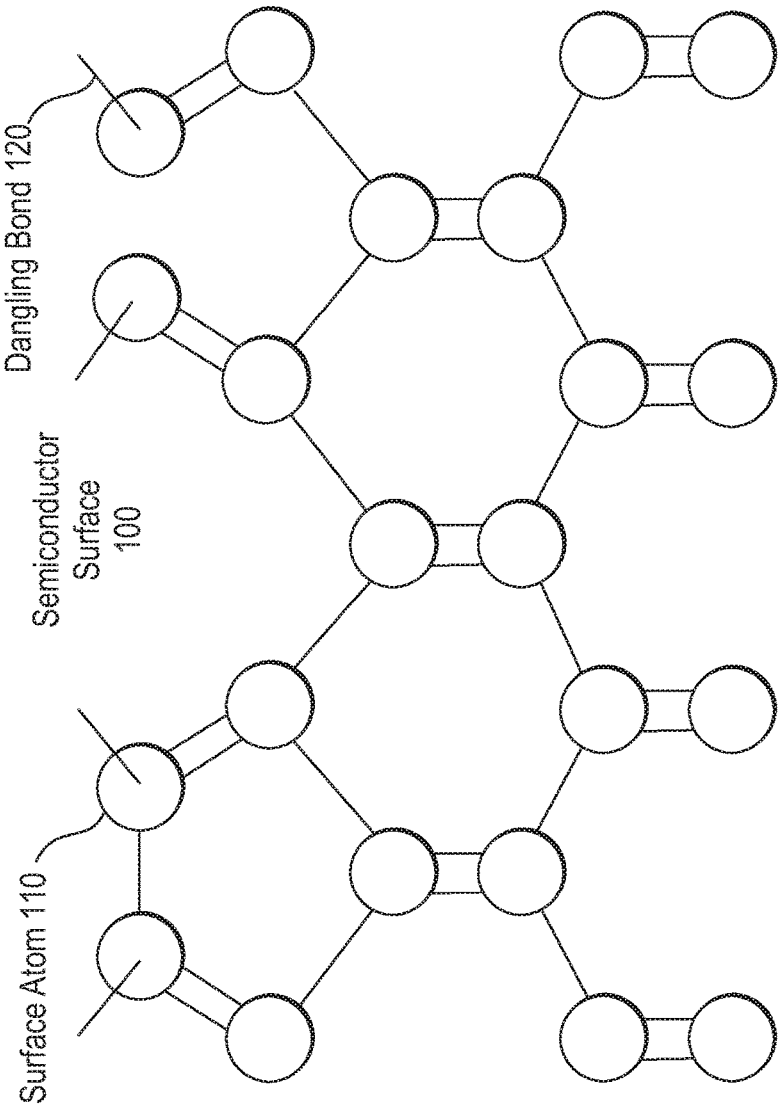

[100]
Dangling Bond 120
Semiconductor Surface 100
Surface Atom 110

Fig. 1

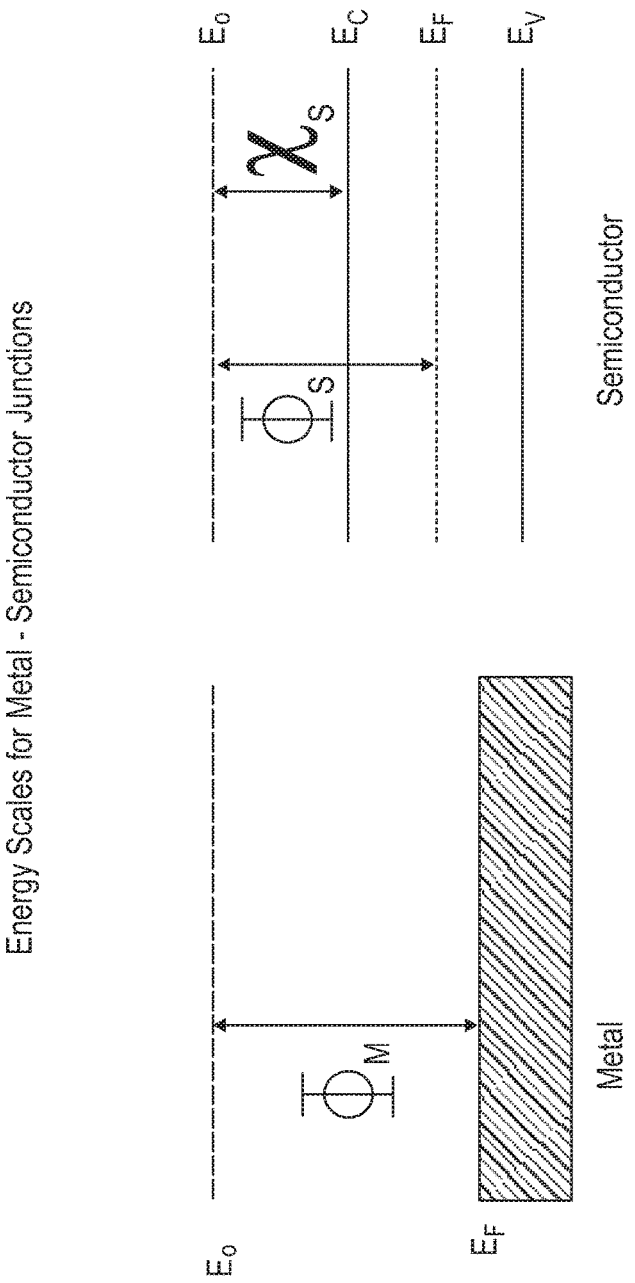

Energy Scales for Metal - Semiconductor Junctions
E_o
E_C
E_F
E_V
χ_S
Θ_S
Semiconductor
E_o
E_F
Θ_M
Metal

Fig. 2

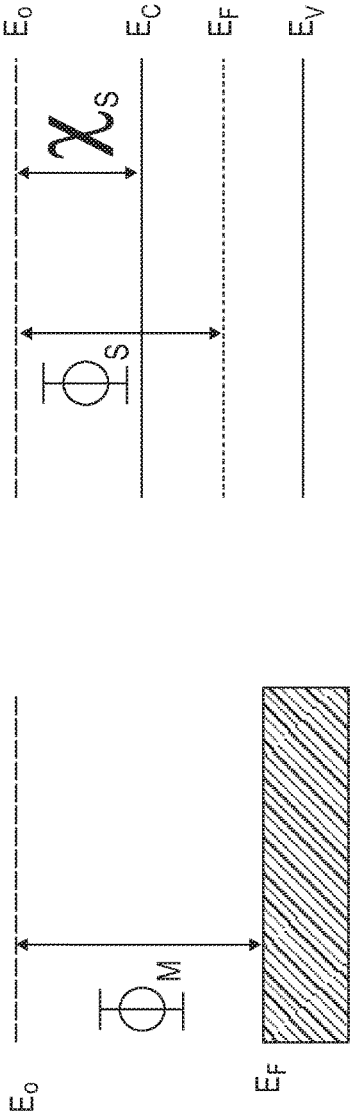


Fig. 3
(Prior Art)

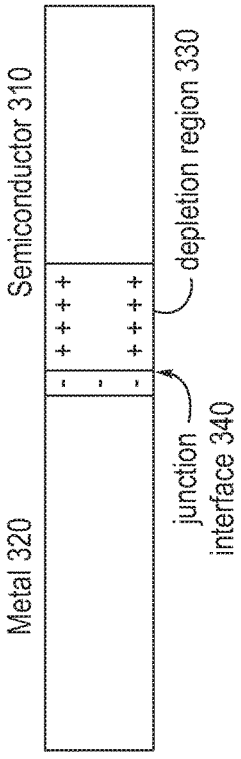
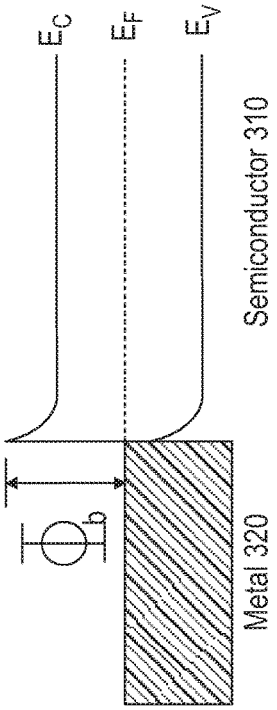


Fig. 4
(Prior Art)



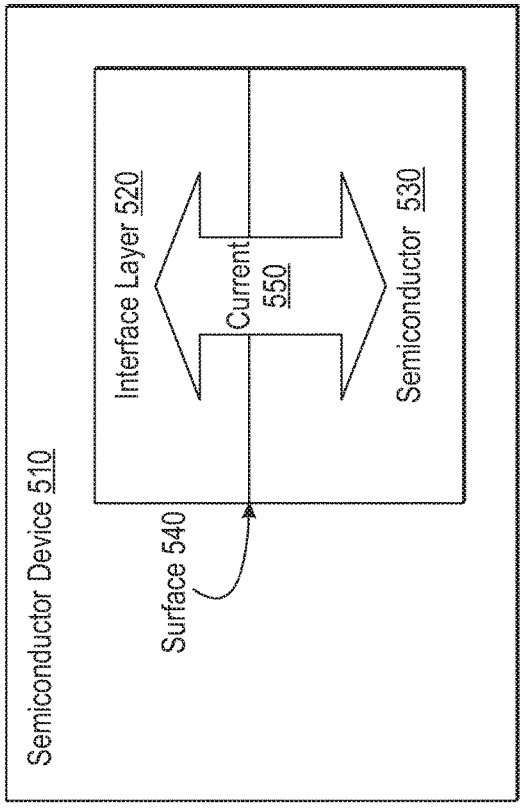

Semiconductor Device 510
Interface Layer 520
Current 550
Semiconductor 530
Surface 540

Fig. 5

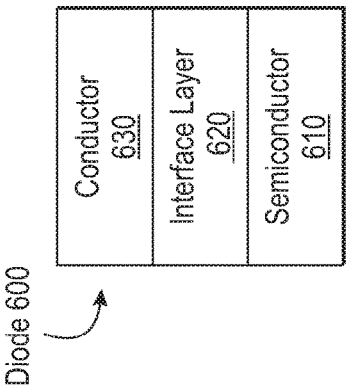

Diode 600
Conductor 630
Interface Layer 620
Semiconductor 610

Fig.6

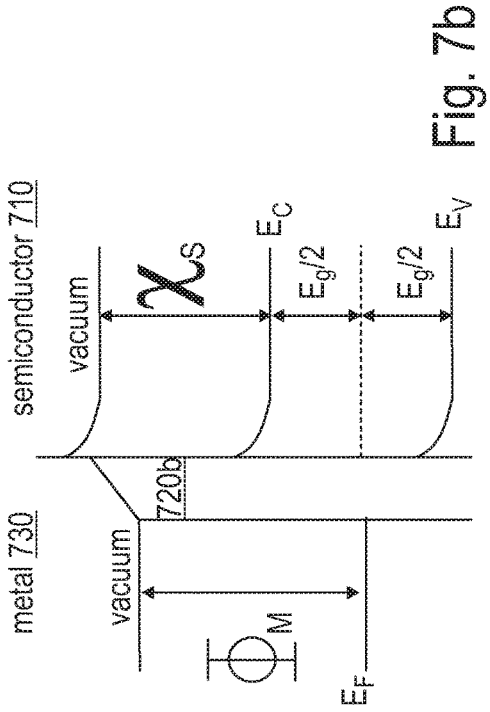


Fig. 7b

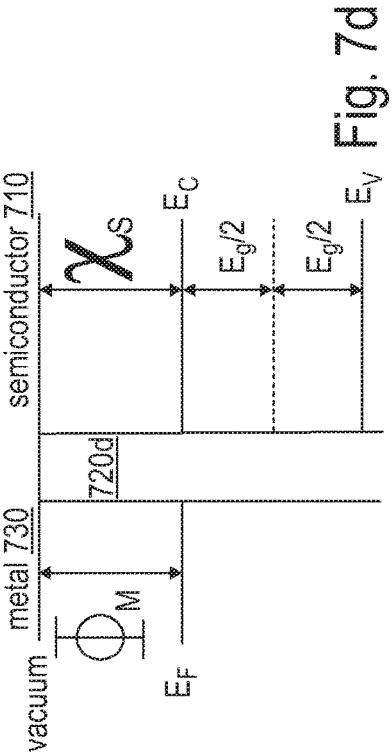


Fig. 7d

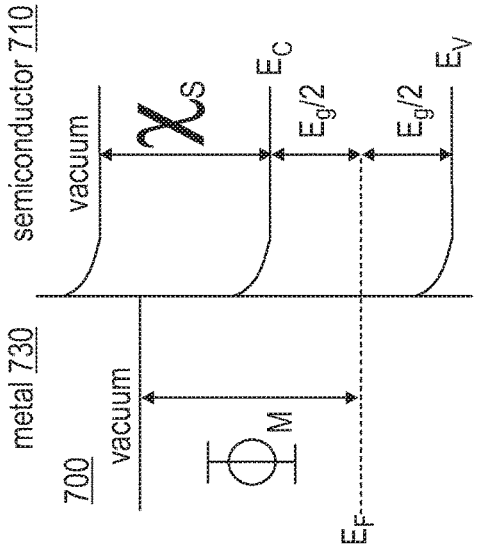


Fig. 7a

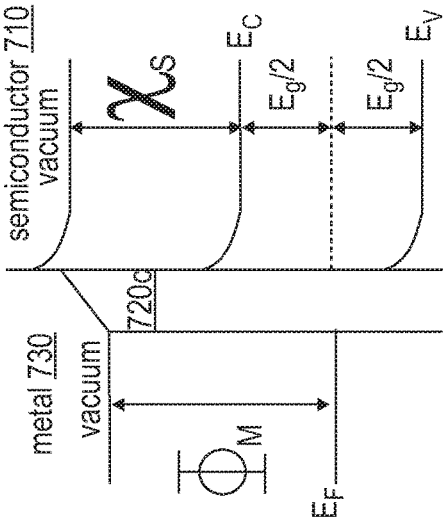
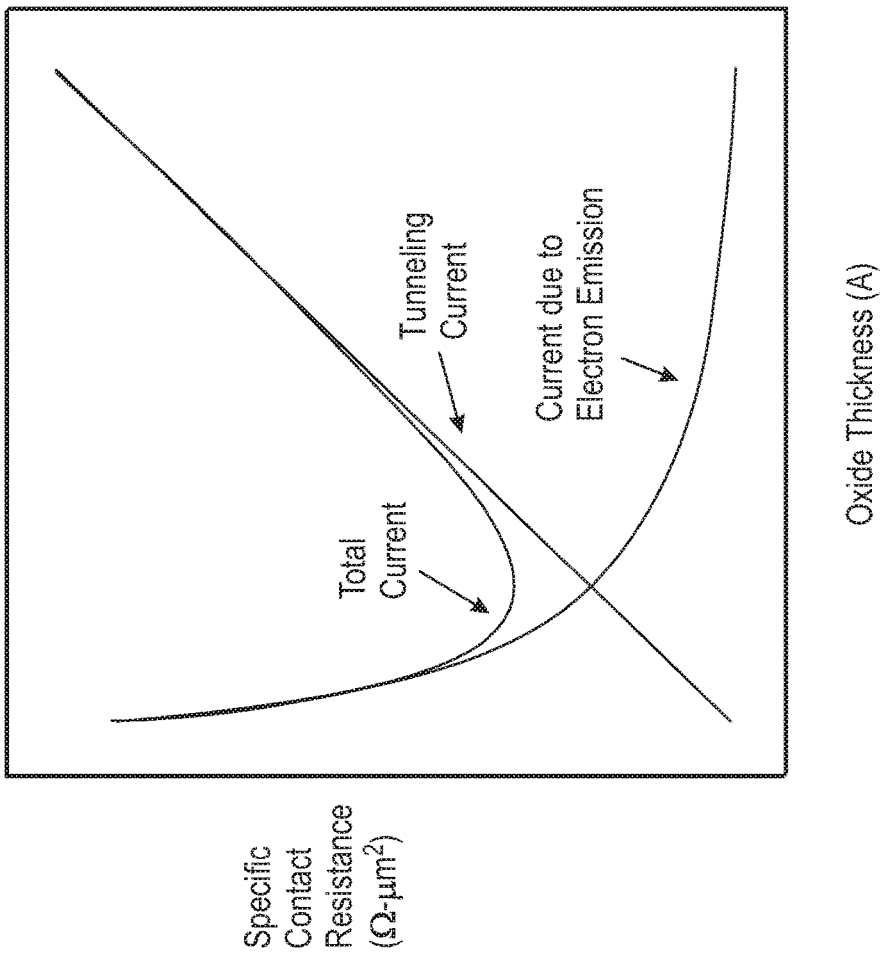


Fig. 7c

Fig. 8


Specific Contact Resistance (Ω-μm^2)
Total Current
Tunneling Current
Current due to Electron Emission
Oxide Thickness (A)

METHOD FOR DEPINNING THE FERMI LEVEL OF A SEMICONDUCTOR AT AN ELECTRICAL JUNCTION AND DEVICES INCORPORATING SUCH JUNCTIONS

RELATED APPLICATIONS

The present application is a CONTINUATION of U.S. patent application Ser. No. 15/728,002, filed Oct. 9, 2017, presently pending, which is a CONTINUATION of U.S. patent application Ser. No. 15/251,210, filed Aug. 30, 2016, now U.S. Pat. No. 9,812,542, which is a CONTINUATION of U.S. patent application Ser. No. 15/048,877, filed Feb. 19, 2016, which is a CONTINUATION of U.S. patent application Ser. No. 13/552,556, filed Jul. 18, 2012, now U.S. Pat. No. 9,425,277, which is a CONTINUATION of U.S. patent application Ser. No. 13/022,522, filed Feb. 7, 2011, now U.S. Pat. No. 8,431,469, which is a DIVISIONAL of U.S. patent application Ser. No. 12/197,996, filed Aug. 25, 2008, now U.S. Pat. No. 7,884,003, which is a DIVISIONAL of U.S. patent application Ser. No. 11/181,217, filed Jul. 13, 2005, now U.S. Pat. No. 7,462,860, which is a CONTINUATION of U.S. patent application Ser. No. 10/217,758, filed Aug. 12, 2002, now U.S. Pat. No. 7,084,423, which is related to U.S. patent application Ser. No. 10/342,576, filed Jan. 14, 2003, now U.S. Pat. No. 6,833,556, all of which are hereby incorporated by reference.

FIELD OF THE INVENTION

The invention elates generally to semiconductor processing and semiconductor devices. More particularly, the invention relates to a process for depinning the Fermi level of a semiconductor at a metal-interface layer-semiconductor junction and to devices that employ such a junction.

BACKGROUND

One of the most basic electrical junctions used in modern devices is the metal-semiconductor junction. In these junctions, a metal (such as aluminum) is brought in contact with a semiconductor (such as silicon). This forms a device (a diode) which can be inherently rectifying; that is, the junction will tend to conduct current in one direction more favorably than in the other direction. In other cases, depending on the materials used, the junction may be ohmic in nature (i.e., the contact may have negligible resistance regardless of the direction of current flow). Grondahl and Geiger first studied the rectifying form of these junctions in 1926, and by 1938 Schottky had developed a theoretical explanation for the rectification that was observed.

Schottky's theory explained the rectifying behavior of a metal-semiconductor contact as depending on a barrier at the surface of contact between the metal and the semiconductor. In this model, the height of the barrier (as measured by the potential necessary for an electron to pass from the metal to the semiconductor) was postulated as the difference between the work function of the metal (the work function is the energy required to free an electron at the Fermi level of the metal, the Fermi level being the highest occupied energy state of the metal at T=0) and the electron affinity of the semiconductor (the electron affinity is the difference between the energy of a free electron and the conduction band edge of the semiconductor). Expressed mathematically:

$$\varphi_B=\varphi_M-\chi_S \quad [1]$$

where Φ_B is the barrier height, Φ_M is the work function of the metal and χ_S is the electron affinity of the semiconductor.

Not surprisingly, many attempts were made to verify this theory experimentally. If the theory is correct, one should be able to observe direct variations in barrier heights for metals of different work functions when put in contact with a common semiconductor. What is observed, however, is not direct scaling, but instead only a much weaker variation of barrier height with work function than implied by the model.

Bardeen sought to explain this difference between theoretical prediction and experimental observation by introducing the concept that surface states of the semiconductor play a role in determining the barrier height. Surface states are energy states (within the bandgap between the valence and conduction bands) at the edge of the semiconductor crystal that arise from incomplete covalent bonds, impurities, and other effects of crystal termination. FIG. **1** shows a cross-section of an un-passivated silicon surface labeled **100**. The particular silicon surface shown is an Si(100) 2×1 surface. As shown, the silicon atoms at the surface, such as atom **110**, are not fully coordinated and contain un-satisfied dangling bonds, such as dangling bond **120**. These dangling bonds may be responsible for surface states that trap electrical charges.

Bardeen's model assumes that surface states are sufficient to pin the Fermi level in the semiconductor at a point between the valence and conduction bands. If true, the barrier height at a metal-semiconductor junction should be independent of the metal's work function. This condition is rarely observed experimentally, however, and so Bardeen's model (like Schottky's) is best considered as a limiting case.

For many years, the cause underlying the Fermi level pinning of the semiconductor at a metal-semiconductor junction remained unexplained. Indeed, to this day no one explanation satisfies all experimental observations regarding such junctions. Nevertheless, in 1984, Tersoff proposed a model that goes a long way towards explaining the physics of such junctions. See J. Tersoff, "Schottky Barrier Heights and the Continuum of Gap States," Phys. Rev. Lett. 52 (6), Feb. 6, 1984.

Tersoff's model (which is built on work by Heine and Flores & Tejedor, and see also Louie, Cheiikowsky, and Cohen, "Ionicity and the theory of Schottky barriers," Phys. Rev. B 15, 2154 (1977)) proposes that the Fermi level of a semiconductor at a metal-semiconductor interface is pinned near an effective "gap center", which is related to the bulk semiconductor energy band structure. The pinning is due to so-called metal induced gap states (MIGS), which are energy states in the bandgap of the semiconductor that become populated due to the proximity of the metal. That is, the wave functions of the electrons in the metal do not terminate abruptly at the surface of the metal, but rather decay in proportion to the distance from that surface (i.e., extending inside the semiconductor). To maintain the sum rule on the density of states in the semiconductor, electrons near the surface occupy energy states in the gap derived from the valence band such that the density of states in the valence band is reduced. To maintain charge neutrality, the highest occupied state (which defines the Fermi level of the semiconductor) will then lie at the crossover point from states derived from the valence band to those derived from the conduction band. This crossover occurs at the branch point of the band structure. Although calculations of barrier heights based on Tersoff's model do not satisfy all experimentally observed barrier heights for all metal-semiconductor junctions, there is generally good agreement for a number of such junctions.

One final source of surface effects on diode characteristics is inhomogeneity. That is, if factors affecting the barrier height (e.g., density of surface states) vary across the plane of the junction, the resulting properties of the junction are found not to be a linear combination of the properties of the different regions. In summary then, a classic metal-semiconductor junction is characterized by a Schottky barrier, the properties of which (e.g., barrier height) depend on surface states, MIGS and inhomogeneities.

The importance of the barrier height at a metal-semiconductor interface is that it determines the electrical properties of the junction. Thus, if one were able to control or adjust the barrier height of a metal-semiconductor junction, one could produce electrical devices of desired characteristics. Such barrier height tuning may become even more important as device sizes shrink even further. Before one can tune the barrier height, however, one must depin the Fermi level of the semiconductor. As discussed in detail below, the present inventors have achieved this goal in a device that still permits substantial current flow between the metal and the semiconductor.

SUMMARY OF THE INVENTION

The present inventors have determined that for thin interface layers disposed between a metal and a silicon-based semiconductor (e.g., Si, SiC and SiGe), so as to form a metal-interface layer-semiconductor junction, there exist corresponding minimum specific contact resistances. The interface layer thickness corresponding to this minimum specific contact resistance will vary depending upon the materials used, however, it is a thickness that allows for depinning the Fermi level of the semiconductor while still permitting current to flow between the metal and the semiconductor when the junction is biased (e.g., forward or reverse biased). By depinning the Fermi level, the present inventors mean a condition wherein all, or substantially all, dangling bonds that may otherwise be present at the semiconductor surface have been terminated, and the effect of MIGS has been overcome, or at least reduced, by displacing the semiconductor a sufficient distance from the metal. Minimum specific contact resistances of less than or equal to approximately 10 Ω-μm^2 or even less than or equal to approximately 1 Ω-μm^2 may be achieved for such junctions in accordance with the present invention.

Thus, in one embodiment, the present invention provides an electrical device in which an interface layer is disposed between and in contact with a metal and a silicon-based semiconductor and is configured to depin the Fermi level of the semiconductor while still permitting current flow between the metal and the semiconductor when the electrical device is biased. The specific contact resistance of the electrical device is less than approximately 10 Ω-μm^2. The interface layer may include a passivating material (e.g., a nitride, oxide, oxynitride, arsenide, hydride and/or fluoride) and sometimes also includes a separation layer. In some cases, the interface layer may be essentially a monolayer (or several monolayers) of a semiconductor passivating material.

In another embodiment, the interface layer is made up of a passivation layer fabricated by heating the semiconductor in the presence of nitrogenous material, for example ammonia (NH3), nitrogen (N2) or unbound gaseous nitrogen (N) generated from a plasma process. In such cases, the interface layer may be fabricated by heating the semiconductor while in a vacuum chamber and exposing the semiconductor to the nitrogenous material.

A further embodiment of the present invention provides for depinning the Fermi level of a semiconductor in an electrical junction through the use of an interface layer disposed between a surface of the semiconductor and a conductor. The interface layer preferably (i) is of a thickness sufficient to reduce effects of MIGS in the semiconductor, and (ii) passivates the surface of the semiconductor. Despite the presence of the interface layer, significant current may flow between the conductor and the semiconductor because the thickness of the interface layer may be chosen to provide a minimum (or near minimum) specific contact resistance for the junction. As indicated above, the interface layer may include a passivating material such as a nitride, oxide, oxynitride, arsenide, hydride and/or fluoride.

Further embodiments of the present invention provide a junction between a semiconductor and a conductor separated from the semiconductor by an interface layer configured to allow a Fermi level of the conductor to (i) align with a conduction band of the semiconductor, (ii) align with a valence band of the semiconductor, or (Hi) to be independent of the Fermi level of the semiconductor. In some or all of these cases, current may flow between the conductor and the semiconductor when the junction is biased because the interface layer has a thickness corresponding to a minimum or near minimum specific contact resistance for the junction. For example, specific contact resistances of less than or equal to approximately 2500 Ω-μm^2, 1000 Ω-μm^2, 100 Ω-μm^2, 50 Ω-μm^2, 10 Ω-μm^2 or even less than or equal to 1 Ω-μm^2 may be achieved.

BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWINGS

The present invention is illustrated by way of example, and not by way of limitation, in the figures of the accompanying drawings.

FIG. **1** shows a cross-section of an un-passivated silicon surface containing surface silicon atoms with dangling bonds.

FIG. **2** illustrates various energy levels for metals and semiconductors and is labeled to show the work function of a metal and the electron affinity of a semiconductor.

FIG. **3** shows an energy band diagram for a conventional metal-n-type semiconductor junction and also illustrates the concept of a depletion region formed in the semiconductor when the materials are brought into contact with one another.

FIG. **4** illustrates band bending at a conventional metal-n-type semiconductor junction.

FIG. **5** shows a semiconductor device containing a semiconductor material having a surface across which electrical current flows during operation of the semiconductor device, and containing an interface layer formed on the surface according to one embodiment of the present invention.

FIG. **6** shows an electrical junction containing an interface layer that is disposed between a semiconductor and a conductor in accordance with one embodiment of the present invention.

FIGS. **7***a*, **7***b*, **7***c* and **7***d* show relationships between Fermi energy, conduction-band energy, and valence-band energy for an unpassivated Schottky diode, a passivated Schottky diode in which MIGS are not removed, an unpassivated Schottky diode in which MIGS are removed and a passivated Schottky diode in which MIGS are removed according to one embodiment of the present invention, respectively.

FIG. **8** shows a curve of interface layer resistance versus interface layer thickness for an electrical junction containing an interface layer disposed between a semiconductor and a conductor in accordance with one embodiment of the present invention.

DETAILED DESCRIPTION

Described herein are processes for depinning the Fermi level of a silicon-based semiconductor (e.g., Si, SiC or SiGe) at a metal-semiconductor junction as well as devices that use such a junction. As more fully discussed below, an interface layer is introduced between the semiconductor and the metal. The interface layer functions to passivate the semiconductor surface (that is, terminate dangling bonds that may otherwise be present at the semiconductor surface so as to assure chemical stability of the surface) and to displace the semiconductor from the metal so as to reduce the effect of MIGS.

As discussed more fully below, the present inventors have determined that for thin interface layers disposed between a metal and a silicon-based semiconductor (e.g., Si, SiC and SiGe), so as to form a metal-interface layer-semiconductor junction, there exist corresponding minimum specific contact resistances. Indeed, minimum specific contact resistances of less than or equal to approximately 10 Ω-μm^2 or even less than or equal to approximately 1 Ω-μm^2 may be achieved for such junctions in accordance with the present invention. To achieve such low contact resistances, a metal that has a work function near the conduction band of the semiconductor for n-type semiconductors, or a work function that is near the valence band for p-type semiconductors, is selected.

The Schottky barrier in such junctions is already minimized, meaning that it is much less than the Schottky barrier presented by a junction in which the Fermi level is pinned, generally near the middle of the semiconductor's bandgap. The current versus voltage (IV) characteristic of these junctions is non-linear, generally having a slope that increases as the voltage increases, such that the derivative of current with respect to voltage is increasing with voltage. This results in a decreasing differential resistance (dV/dI) and a decreasing resistance (V/I). Thus, a junction that has high resistance or high differential resistance near the origin of the IV characteristic (zero volts) may have significantly lower resistance or lower differential resistance at higher voltages.

The present invention achieves low resistance and low differential resistance near the origin of the current-voltage characteristic for a metal-interface layer-semiconductor junction. Generally, the voltage around the origin should be less than about 100 mV, or more preferably less than about 10 mV for purposes of measuring, determining, or utilizing such junctions of low resistance. At higher voltages, the junction resistance will be even lower. It is thus a feature of the present invention to set an upper bound on the resistance of a contact, where the upper bound occurs at low voltages.

It is further noted that in junctions where the Schottky barrier is minimized as described above, such that the Fermi level at the junction interface at zero volts lies at or near the conduction band edge or valence band edge (for n- and p-type semiconductors, respectively), the IV characteristic will be nearly symmetric, especially at low voltage. In this case, the term "forward bias" is not defined in the usual sense of a diode wherein forward bias corresponds to the direction of bias for which greater current flows. Thus, in determining or utilizing low resistance junctions of the present invention, the voltage may be either positive or negative.

It is also possible (in accordance with a further embodiment of the present invention) to make junctions where the Schottky barrier is higher than it would be if the Fermi level at the junction interface were pinned, usually around mid-gap of the semiconductor. Such junctions are formed in the present invention between a metal with a workfunction near or substantially equal to the conduction band edge of a p-type semiconductor, or between a metal with a workfunction near or substantially equal to the valence band edge of an n-type semiconductor. These junctions are diodes, in that little current will flow if the n-type (p-type) semiconductor is biased positive (negative) with respect to the metal, and large currents will flow if the voltage is reversed. The low-current flow state is referred to as reverse bias, and the high-current flow state is referred to as positive bias.

Low resistance in the case of a diode is only relevant in forward bias conditions. In junctions created in accordance with the present invention the resistance contribution of the interface layer is smaller than the resistance due to the Schottky barrier. That is, in forward bias conditions for junctions created in accordance with the present invention, the transport of charge is limited mainly by the thermal emission of carriers from the semiconductor over the barrier at the interface, and not by the tunneling through the interface dielectric. Thus, low resistance in the case of a diode refers to a resistance lower than the resistance presented by the Schottky barrier.

In certain applications of diodes, the ability to withstand high reverse biases may be more desirable than high current flow in forward bias. These applications would be considered high voltage/low power applications. In such cases, a low resistance is not essential, and junctions created in accordance with still another embodiment of the present invention provide high-voltage diodes capable of withstanding voltages higher than could otherwise be achieved if the Fermi level of the semiconductor in the junction were pinned.

The present invention is discussed below in terms of presently preferred embodiments thereof, however, this discussion is not meant to limit the scope of the invention. By studying t present disclosure, others of ordinary skill in the art may recognize equivalent procedures, materials or structures that can be substituted for those described herein to achieve the same effect. The reader is advised and reminded that the use of such equivalents is deemed to be within the scope of the present invention. For example, where the discussion refers to well-known structures and devices, block diagrams are used, in part to demonstrate the broad applicability of the present invention to a wide range of such structures and devices.

I. Introduction and Definitions

The present discussion makes use of terms that, although well known in the art, may not be familiar to all readers. Therefore, before beginning a detailed discussion of the present invention, it is helpful to define certain terms and concepts. To understand the properties of metal-semiconductor junctions and the impact of the present invention, one must refer to some important energy scales, which are shown graphically in FIG. **2**. The so-called vacuum level (E0) represents the minimum energy that an electron needs to possess in order to completely free itself from a metal or semiconductor. For a metal, the Fermi level (E_F) represents

the highest occupied energy level for the material. That is, nearly all energy states below the Fermi level are filled, while nearly all states above the Fermi level are empty. The work function of the metal (ΦM) is then defined as the energy required to free an electron at the Fermi level and mathematically it is the difference between the vacuum level and the Fermi level. The work function is an invariant bulk property of the metal.

As illustrated in the diagram, semiconductors also have a Fermi level (E_F) and a work function (Φ_S), however, the work function is not an invariant property of the semiconductor. Because the Fermi level varies depending on the doping level in the semiconductor (i.e., the relative amounts of impurities introduced into the semiconductor crystal which change the electron and hole carrier concentrations), a separate parameter, the electron affinity (χ_S), is defined. The electron affinity is an invariant property of the semiconductor and is the difference between the vacuum level and the conduction band edge of the semiconductor. In a semiconductor, almost all energy states are filled in the valence band (E_V) while the conduction band (E_C) is almost empty.

Now consider a conventional junction between a metal and an n-type semiconductor that has a work function smaller than the work function of the metal (i.e., $\Phi_S<\Phi_M$). An n-type semiconductor is one in which electrons are the majority charge carriers (in p-type semiconductors, holes are the majority charge carrier). As shown in FIG. **3**, because the Fermi level in the semiconductor is higher than the Fermi level in the metal, electrons transfer from the semiconductor **310** to the metal **320** when the materials are brought into contact. Thus, a depletion region (i.e., a region in which there are no free charge carriers) **330** forms near the junction interface **340**.

The formation of the depletion region gives rise to an electric field and so-called "band bending", as one approaches the junction interface from the semiconductor side (see FIG. **4**). The band bending creates an energy barrier (discussed above) that blocks further transfer of electrons into or out of the semiconductor. Similar barriers are formed for a junction between a metal and a p-type semiconductor when the work function of the metal is less than the work function of the semiconductor. However, in the case of a metal-n-type semiconductor junction in which the work function of the semiconductor is greater than that of the metal or a metal-p-type semiconductor junction in which the work function of the semiconductor is less than that of the metal, no such energy barriers are created and the contact is said to be ohmic in nature.

As discussed above, although Schottky first postulated that the height of the energy barrier (Φ_b) formed at a metal-semiconductor junction was simply the difference between the work function of the metal and the electron affinity of the semiconductor, experiments have not verified this relationship. Instead a more complex explanation that takes into account the effects of surface defect states, inhomogeneities and MIGS appears to provide more accurate estimates of barrier heights by explaining the pinning of the Fermi level in the semiconductor. The present inventors have created a technique which is believed to depin the Fermi level of a Si-based semiconductor at a junction with a metal (and thus allow for control or tuning of the barrier height) by both passivating the semiconductor surface (to eliminate or at least reduce the effects of surface states and possibly inhomogeneities) and displacing the metal from the semiconductor (to eliminate or at least reduce the effects of MIGS). This depinning is achieved by introducing an interface layer between the semiconductor and the metal to create a semiconductor—interface layer—metal junction, which still permits significant current to flow between the metal and the semiconductor when the junction is forward biased.

This latter point is important. As discussed further below, for contacts where the energy bands of the semiconductor and the conductor align (i.e., where the Fermi level of the conductor aligns with the conduction or valence band of the semiconductor depending on semiconductor type and/or contact application), if the interface layer is too thin, the specific contact resistance of the junction increases because of the presence of MIGS, resulting in an increased barrier height; thus, current flow is hampered. Conversely, if the interface layer is too thick, the specific contact resistance is again increased and one gets low current across the junction because of tunneling limitations. The present invention achieves an interface layer that is thick enough to reduce or eliminate the effect of MIGS, while still thin enough to permit significant current flow.

II. Passivation of Semiconductor Surfaces

A common processing operation performed during semiconductor device fabrication is silicon surface passivation. Surface passivation (whether by an oxide or another material) chemically neutralizes and physically protects the underlying silicon. For example, exposing a silicon surface to oxygen (under the appropriate conditions to grow a protective film of silicon dioxide) will allow the oxygen to react with the dangling bonds of the silicon surface to form covalent bonds that satisfy the surface silicon atoms' valency and render the surface fully coordinated. These covalent bonds provide chemical stability to the silicon surface. The covalent bonds also tie up unbound charges that exist on the silicon surface as a result of the discontinuation of the semiconductor crystal at the surface.

However, passivation with silicon dioxide has several significant disadvantages. For example, silicon dioxide is a dielectric insulator that poses a significant barrier to the flow of current. Accordingly, a layer of silicon dioxide deposited or grown on a silicon surface may significantly reduce the ability for electrical current to flow through that surface. As a result, the use of silicon dioxide has been limited in practicality to surfaces external to the active region of semiconductor devices through which current passes during device operation (e.g., as a gate oxide layer). This disadvantage is compounded by the fact that the silicon dioxide grows very rapidly and readily on the silicon surface so that it is difficult to limit the growth to a thin layer. Silicon dioxide is also a poor diffusion barrier to semiconductor dopants such as boron.

Instead of making use of silicon dioxide then, in one embodiment the present inventors utilize a nitrided semiconductor surface to provide chemical passivation. That is, a nitride layer is introduced to passivate the semiconductor surface by eliminating or at least reducing the effects of surface states and possibly inhomogeneities. The nitride layer also displaces the metal from the semiconductor and eliminates or at least reduces the effects of MIGS. The result of introducing the nitride layer as an interface between the semiconductor and the metal is a depinning of the Fermi level of the semiconductor. When the Fermi level of the semiconductor is depinned, the Fermi level of the metal at the interface will be that of the bulk metal, and will not be dependent upon the interface. In addition to the above, the present inventors propose techniques for providing non-

insulating, passivated semiconductor surfaces using materials other than nitrogen; for example, oxides, hydrides, arsenides and/or fluorides.

These developments have wide applicability in connection with the fabrication of Schottky diodes, Schottky-barrier transistors and other electrical components. For example, in Schottky diodes, the ability to control the energy barrier height at the diode junction is important if the device is to be tailored to specific applications. Use of the present techniques allows for tuning of the barrier height. Further, for other three-terminal devices with Schottky-barrier-isolated channels, control of device characteristics is made possible through the present invention by allowing n- and p-type devices to be fabricated without dopants, relying instead on the use of metals with different work functions.

FIG. **5** shows a semiconductor device **510** that contains a semiconductor **530** and an interface layer **520** formed on a surface **540** of the semiconductor in accordance with the present invention. The terms semiconductor device, microelectronic device, monolithic device, chip, and integrated circuit are often used interchangeably in this field. Any or all such devices may each contain an interface layer formed on a semiconductor surface in accordance with the present invention.

The semiconductor **530** contains a semiconductor material. The term semiconductor material refers to a material having a bandgap that is greater than about 0.1 eV and less than about 4 eV. The term bandgap refers to an energy gap of forbidden energy levels separating the conduction band, which is an upper energy band that is mostly devoid of electrons and wherein electrons can conduct, and the valence band, which is an energy band that is mostly filled with electrons and wherein electrons cannot conduct. The semiconductor material may have a wide range of doping levels including no doping at all.

The semiconductor **530** has a surface **540** that is passivated by the interface layer **520**. In this context (and as used elsewhere herein) the term passivation means the elimination or at least the reduction of the effects of surface states due to defects or dangling bonds of the semiconductor surface **540**. Note that passivation does not, as a practical matter, require that all surface states be eliminated. Rather, it is the effect of surface states on the device properties that is limited or eliminated in passivation. Note further that the presence of MIGS may be regarded as a surface state, however, as used herein the term passivation is not meant to infer the elimination of MIGS (though in some cases, a passivation layer may have sufficient thickness to provide a separation layer between the semiconductor and the metal sufficient to reduce or eliminate MIGS). The semiconductor **530** is operable to be electrically coupled with a first voltage associated with the semiconductor device **510** and to conduct electrical current **550** across the passivated surface **540**.

The interface layer **520** is formed on the semiconductor **530** and may contain a passivation material that bonds to the semiconductor material by way of a covalent (or other) bond formed between the passivation material and the semiconductor material. For example, an atom of passivation material may covalently bond with a dangling bond of a surface silicon atom to fully coordinate the silicon atom and thereby help passivate the silicon atom. In some cases, the passivation material may be the sole component of the interface layer **520**, while in other cases the interface layer **520** may be a compound layer that includes both a passivation layer and a separation layer. That is, the interface layer serves to (i) chemically passivate the semiconductor surface **540**, and (ii) displace the semiconductor from the metal sufficiently to eliminate or at least reduce the effect of MIGS. As explained below, this may necessitate including a separation layer in addition to a passivation layer within the interface layer, depending on the passivation material selected. Of course, the combination of the passivation layer and the separation layer must be sufficiently thin to permit the low specific contact resistances described herein.

Different passivation materials are contemplated. According to one embodiment, the interface layer **520** is formed using a material that is preferably selected from the group consisting of hydrogen (H), oxygen (O), nitrogen (N), arsenic (As), and fluorine (F) (that is, the interface layer **520** may include a nitride, an oxide, a hydride, an arsenide and/or a fluoride). Other materials having chemical characteristics or valences similar to these materials may also be used. Note that distinct separation layers (i.e., in addition to the passivation layer(s)) may be needed where H, As, or F passivation layers are used, as these tend to form monolayer coverage, rather than a layer of a compound with Si of process-dependent thickness. In contrast, passivation layers made using N and/or O may not require distinct separation layers, as these elements may form a layer of a compound of Si with a thickness that can be varied depending on processing.

Different amounts of passivation material are contemplated to be useful for different embodiments of the present invention. Often, the interface layer **520** includes or is made up of a passivation layer with a thickness of between approximately 0.1 nm and about 5 nm. For example, depending upon the particular implementation, the thickness may be less than about 1 nm, less than about 0.5 nm, less than about 0.2 nm, may be the thickness corresponding to a single layer or monolayer of passivation material that is bonded to the semiconductor surface, or may even be the number of atoms of passivation material required to passivate substantially all the dangling bonds associated with the semiconductor surface **540**.

In some cases, passivation of the semiconductor surface **540** will include removing (or terminating) dangling bonds located proximate to the surface of the semiconductor material, including those at the surface as well as those within a few molecular dimensions from the surface. This process may stabilize the surface of the semiconductor material and may improve the controllability of subsequent fabrication operations. Passivation may also reduce the density of surface states that may exist at the semiconductor surface as a result of the discontinuation of the semiconductor crystal at the surface. This may improve consistency and performance of the semiconductor device, inasmuch as such states are known to interfere with proper device operation. For example, they may provide surface charge states that result in a pinning of the Fermi level.

III. Forming Interface Layers

Exemplary methods for forming interface layers to provide (i) passivation of semiconductor surfaces, and (ii) displacement of the semiconductor from the metal to eliminate or at least reduce of the effects of MIGS within the semiconductor when in the presence of the metal (collectively referred to herein as depinning the Fermi level of the semiconductor) with hydrogen, fluorine or nitrogen are presented below to further illustrate the concepts of the present invention. Other passivation materials may include arsenic, oxygen or an oxynitride, and in some cases such passivation layers are combined with separation layers (e.g., made of an oxide) to complete the interface layer.

A. Hydrogen and Fluorine

An interface layer may contain hydrogen, fluorine, or both hydrogen and fluorine (e.g., in the form of a hydride and/or a fluoride). One method for forming an interface layer on a semiconductor surface with hydrogen and fluorine includes cleaning the semiconductor substrate with a cleaning solution, immersing the cleaned substrate in a hydrogen fluoride solution (or other liquid containing hydrogen and fluorine ions) having an effective concentration typically between about 1%-50% by weight, waiting an effective period of time, typically between about several seconds and about 5 minutes, removing the substrate from the hydrogen fluoride solution, optionally rinsing the substrate in deionized water, and blow-drying the substrate with nitrogen. Such a method may form an interface layer containing hydrogen and fluorine that are bonded (e.g., covalently) to the semiconductor surface.

It should be noted that long rinses in deionized water, generally longer than about 30 seconds, might remove the hydrogen passivation. Thus, deionized water rinses might advantageously be kept to less than about 30 seconds to maintain the hydrogen passivation of the surface. Also, the higher the concentration of the hydrogen fluoride during the immersion, the greater the concentration of fluorine passivation. Finally, methods are also contemplated where the ratio of hydrogen to fluorine passivation is altered by removing either the hydrogen or the fluorine.

An interface layer formed in this fashion may be best suited for applications where a subsequent metal layer is deposited over the interface layer in a generally non-invasive fashion, for example using a thermally evaporated source. Experiments by the present inventors to date suggest that using other approaches (e.g., plasma deposition) may cause damage to the thin (e.g., monolayer thick) interface layer contemplated as part of the present invention.

B. Nitrogen

In a further embodiment, an interface layer may contain nitrogen (e.g., in the form of silicon nitride). One method for forming an interface over a semiconductor surface with nitrogen includes heating a substrate containing the semiconductor surface in the presence of a nitrogenous material (that is, a gas or other material containing nitrogen). For example, a substrate containing an exposed silicon surface may be annealed at a temperature between about 300° C. and about 750° C., which is lower than temperatures conventionally used for Rapid Thermal Nitridation (RTN), under a gaseous ambient having, for example, ammonia (NH_3) at some effective partial pressure. By exposed, we mean a clean surface, free of everything except silicon. Such a method may form an interface layer containing nitrogen, often in the form of a nitride, bonded to the semiconductor surface. Note that the present inventors have observed indications suggesting that in these low temperature conditions interface layer growth is self-limiting, depending only on temperature.

According to another embodiment, an interface layer that includes nitrogen may be formed on an exposed surface of a semiconductor material by a method that includes heating a semiconductor material to a substantially high temperature under vacuum and exposing the semiconductor material to a substantially small amount of a nitrogenous material, such as ammonia. The method may include placing a semiconductor having an exposed semiconductor surface in a heating chamber, pulling a vacuum of less than about one millionth of a Torr, or more favorably an ultra high vacuum of less than 10-9 Torr, and then heating the semiconductor in the heating chamber to a substantially high temperature. The higher the vacuum, the longer the substrate may be heated without growth of an oxide from residual oxygen or water in the chamber. Thus, the process may include heating the semiconductor to a temperature that is between about 900° C. and about 1000° C., or higher, in an inert ambient. As desired, the semiconductor may be exposed to hydrogen gas, or an equivalent, to reduce any native oxide on the semiconductor. These high temperatures may provide for greater passivation of the semiconductor surface as compared with results that may be achieved at lower temperatures.

Then, the heated semiconductor may be exposed to a substantially small amount of a nitrogenous material, such as ammonia. This may include exposing the semiconductor surface to ammonia for a substantially short period of time. For example, the surface may be subjected to a burst or pulse of ammonia lasting for a time period between about 0.5 seconds and about 5 seconds. Alternatively, the surface may be exposed to a controlled, small amount of ammonia over an arbitrarily longer period of time. In this way, the substantially small amount of ammonia will react with the surface to form a nitrogenous interface layer, such as a nitride layer, thereon and then further growth of the interface layer will cease. Then the semiconductor may be cooled from the substantially high temperature to ambient temperature and removed from the heating chamber. Further annealing of the substrate and the grown nitride layer may also be performed in the vacuum chamber before removal, at a substantially elevated temperature between about 700° C. and 1000° C., or higher.

Advantageously, it has been unexpectedly observed that a process such as that described above and incorporating substantially high temperature exposure for substantially short periods may be used to controllably form thin yet effective interface layers. That is, the present inventors have observed that in the creation of thin interface layers that include nitrogenous materials, temperature appears to be a dominant factor in controlling thickness. For example, by such methods effective interface layers may be formed having a thickness that is less than about 1 nm, less than about 0.5 nm, less than about 0.2 nm, or having a thickness that corresponds to essentially a single monolayer sufficient to passivate essentially all dangling bonds proximate the semiconductor surface.

Further, thin interface layers may be advantageously grown on a semiconductor in the presence of nitrogen gas, or other inert nitrogen-containing gas. The reaction rate of a semiconductor such as silicon with nitrogen gas is significantly lower than that of a reactive nitrogen-containing gas such as ammonia. The slow growth rate may be desirable for better control of the growth of films of nitrogen on a semiconductor of a thickness of less than about 1 nm, less than about 0.5 nm, less than about 0.2 nm, or having a thickness that corresponds to essentially a single monolayer sufficient to passivate essentially all dangling bonds proximate the silicon surface.

IV. Diodes Containing Passivated Semiconductor Surfaces

Diodes made from Schottky barriers (i.e., asymmetric electrical potentials formed at a junction between a metal and a semiconductor) are widely used in rectifiers in power supply and control applications. As used herein, the terms Schottky diode, metal-semiconductor junction diode, diode, and rectifier are all related and appear in order from more specific at the left to more general at the right. Likewise, the terms Schottky barrier, metal-semiconductor barrier, con-

ductor-semiconductor junction, and multi-material junction are all related and appear in order from more specific at the left to more general at the right. The term Schottky diode will be used to refer to a diode containing a Schottky barrier.

As mentioned above, the present inventors have devised a scheme to control or adjust a Schottky barrier height by forming an interface layer (which includes or sometimes consists of a passivation layer that includes an oxide, oxynitride, nitride, arsenide, hydride, fluoride, or an equivalent) between a metal and a semiconductor. This scheme differs from past attempts by others to control barrier height, which attempts generally involved either using a silicide as a contact metal (and thus limiting the choices of available contact metals to those that can form silicides), or using esoteric substrates that exhibit wide bandgaps. Further, in previous devices the Fermi level of the semiconductor remains pinned, with the barrier height being virtually independent of the metal used. Finally, doping of substrates has also been attempted, however, it has not been shown to truly affect the barrier height of the substrate material. For example, PtSi contacts have reduced resistance due to high silicon doping such that the current across the junction is dominated by tunneling through the barrier. Doping may thus lead to cases where the top of the barrier may be so thin as to be essentially transparent to electrons, however, doping does not appear to allow actual tuning of the barrier height.

FIG. **6** shows an example of a diode **600** containing, according to one embodiment of the present invention, an interface layer **620** disposed between and attached to both a semiconductor **610** and a conductor **630**. The conductor and the semiconductor are operable to be electrically coupled with different voltages associated with the operation of the diode **600** and to pass electrical current through a passivated semiconductor surface formed at the junction between the semiconductor **610** and the interface layer **620**.

The conductor **630** contains a conductive material such as a metal or an alloy of a metal. The terms metal, conductive material, and conductor are all related and appear in order from specific at the left to general at the right. In general, the terms refer to a highly electrically conductive substance that has a Fermi energy level that sits in a partially filled band. Unless otherwise specified, conductors include metals (e.g., pure metals and alloys), and other conductors such as doped polysilicon (a nonporous silicon containing randomly oriented crystallites), doped single crystal silicon, and metal silicides. Note that alloys may have workfunctions different than their constituents and may be designed to have specific workfunctions though selective use of ratios of the constituent metals.

Often, the conductor is a metal since metals may offer advantages over conductive semiconductors including lower resistance, higher carrier mobilities that provide superior high frequency performance and switching, favorable low power characteristics, and ease of manufacturing control. Use of metals may also avoid the need to perform semiconductor doping, which may simplify manufacturing and improve quality control.

Metals that are contemplated include pure metals, alloys, refractory metals, metals that do not form silicides, metals physically deposited by substantially non-invasive processes such as by condensation of a thermally evaporated metal vapor, and metals having a predetermined work function. The use of non-invasively deposited metals may allow for forming the metal on a thin interface layer without disrupting the passivation properties of the layer.

A metal having a predetermined work function may be a metal having a work function smaller or greater than that of the semiconductor, depending on the desired application. Often, the semiconductor will be silicon. In this case by the work function of a semiconductor or silicon we mean the energy in the middle of the semiconductor bandgap. Exemplary metals that have a work function smaller than silicon include Group 3A elements, aluminum (Al), indium (In), titanium (Ti), chromium (Cr), tantalum (Ta), cesium (Cs), magnesium (Mg), erbium (Er), ytterbium (Yb), manganese (Mn), lead (Pb), silver (Ag), yttrium (Y), and zinc (Zn). Exemplary metals that have a work function greater than silicon include platinum (Pt), gold (Au), tungsten (W), nickel (Ni), molybdenum (Mo), copper (Cu), cobalt (Co), and palladium (Pd).

The semiconductor-interface layer-conductor configuration illustrated in FIG. **6** defines what the present inventors have chosen to call a "passivated Schottky barrier". The passivated Schottky barrier is a naturally formed electrical potential barrier to an electron or hole at the Fermi energy (the electrochemical potential) in the conductor due to a depletion region formed in the semiconductor adjacent the conductor. The passivated Schottky barrier may deviate in barrier height from a standard un-passivated Schottky barrier that would form naturally at a contact junction between the semiconductor and the conductor without the interface layer disposed therebetween. That is, the passivated Schottky barrier may have a barrier height that depends predominantly upon the bulk characteristics of the semiconductor and the conductor, rather than on surface properties, and may depend in part on the characteristics of the interface layer.

Indeed, the present inventors have determined that changes in barrier height are approximately monotonic and continuous for variations in surface passivation thickness by nitridation of the semiconductor substrate. More specifically, experiments by the present inventors in a regime where the nitride layer is sufficiently thick to remove MIGS show that temperature of interface layer formation has the strongest effect on barrier height. In other regimes, thickness may be critical. Ideally, if all surface states are removed, barrier height should be controllable simply by the choice of metal used.

To understand why thickness of the interface layer is important, refer briefly to FIG. **8** where a graph of interface-specific contact resistance versus interface thickness is shown. The graph is for a structure where the workfunction of the metal is the same as the electron affinity in the semiconductor, such that the Fermi level of the metal lines up with the conduction band of the semiconductor. At large thicknesses, the interface layer poses significant resistance to current. As thickness decreases, resistance falls due to increased tunneling current. However, there comes a point where even as the interface layer continues to get thinner, resistance increases. This is due to the effect of MIGS, which increasingly pull the Fermi level of the metal down towards mid-gap of the semiconductor, creating a Schottky barrier. The present inventors have discovered that this competition results in an optimum thickness, as shown in the illustration, where the resistance is a minimum. At this thickness the effect of MIGS has been sufficiently reduced to depin the metal and lower the Schottky barrier, and the layer is still sufficiently thin to allow significant current flow across the interface layer. Contact resistances of less than or equal to approximately 2500 Ω-μm^2, 1000 $\Omega\mu m^2$, 100 $\Omega\mu m^2$, 50 Ω-μm^2, 10 $\Omega\mu m^2$ or even less than or equal to 1 Ω-μm^2 may be achieved.

Characteristics that may be adjusted to provide a desired barrier height thus include the passivation material used

(e.g., selection based on bandgap), the interface layer thickness (e.g., especially where the interface layer is a compound layer formed of a passivation layer and a separation layer), the method of forming the interface layer (e.g., control of parameters such as temperature), the interface layer thickness that is substantially similar to a penetration depth of MIGS formed at a metal interface, the metal used for the source and/or drain, and other characteristics.

One advantage of the ability to adjust the Schottky barrier height with the introduction of interface layer **620** is the ability to form a substantially high barrier height. For example, an interface layer may be used to create a Schottky barrier having a barrier height that is greater than can be achieved through the use of metal silicides, greater than about 2.0 eV, or greater than about 2.5 eV (using a semiconductor with a bandgap at least this large), or nearly 1.0 V using silicon. Such high barrier heights imply the ability to withstand high voltages before breakdown occurs. Thus, Schottky barriers having such high barrier heights may be particularly useful in high-voltage Schottky diodes.

Another advantage achieved through the use of the interface layer **620** is greater flexibility afforded in selecting a conductor **630**. Typically, metals chosen for application in classic Schottky diodes are those that can form a silicide with a silicon semiconductor. The formation of the silicide helps to reduce surface states (resulting from dangling bonds), but not the effects of MIGS. Thus, the Fermi level at the semiconductor surface is still pinned. Using metals that form silicides upon contact with silicon may thus help to make the devices more reproducible in a manufacturing environment, but such devices still suffer from the drawback of having a barrier height that is fixed.

According to one embodiment of the present invention, however, one may select a conductor that is not able (or not readily able) to form a silicide with the semiconductor. The metal silicide is not needed because the interface layer provided in accordance with the present invention passivates the semiconductor surface and also reduces or eliminates the effect of MIGS. This may allow for selection of a metal that has properties such as a desirable work function or Fermi level energy, even though that metal may not form a metal silicide.

For example, to make large-barrier diodes, for an n-type doped silicon semiconductor, a metal may be selected that has a work function that is either substantially equal to the valence band energy of the semiconductor or that is within about 0.1 eV to about 0.3 eV of the valence band energy of the semiconductor. Similarly, for a p-type doped silicon semiconductor, a metal may be selected that has a work function substantially equal to the conduction band energy of the semiconductor. For Schottky diodes configured in accordance with the present invention, the Fermi level of the metal may lie anywhere in the bandgap of the semiconductor when an interface layer is disposed within the junction, resulting in diodes of various barrier heights. The Fermi level of the metal may also lie in the conduction or valence band of the semiconductor.

The use of interface layer **620** thus provides a way to tune, adjust, or control the height of the barrier between the conductor and the semiconductor. Without the interface layer **620**, the barrier height would be substantially untunable, un-adjustable, and fixed (as discussed above).

The role played by interface layer **620** in tuning, adjusting, or controlling the height of the barrier between the conductor **630** and the semiconductor **610** may be understood as a depinning of the Fermi level of the semiconductor. That is, the interface layer may reduce surface states by bonding to the semiconductor material to consume dangling bonds. Additionally, the interface layer may reduce the formation of in the semiconductor by providing a thickness and bandgap that prevent the electron wave function (of the metal) from penetrating into the semiconductor. The electron wave function may instead penetrate into the interface layer and form MIGS within the interface layer at an energy related to the states of the interface layer material. As desired, the density of the MIGS and the depth of MIGS penetration into the interface layer may be reduced by choosing an interface layer material or materials having a larger bandgap or higher effective mass than the semiconductor.

According to one embodiment of the present invention then, the interface layer **620** is incorporated into a device operable to pass current through the semiconductor surface and the interface layer during device operation. In such an embodiment, it may be desirable to use an interface layer having a thickness of a monolayer, or, for example between about 0.1 nm and about 0.3 nm, and also having a wide bandgap (as compared to that of the semiconductor) so that the interface layer both de-pins the Fermi level (so that the harrier height depends predominantly on bulk properties of the junction materials) and allows sufficient current transfer across it. Advantageously, such interface layers may be sufficiently thin to provide low impedance to current flow (due to the exponential dependence of direct tunneling on barrier thickness), which is desirable for many semiconductor devices, while also providing sufficient semiconductor surface passivation to allow an adjustable barrier height. That is, the interface layer may allow passivation of surface states and reduction (or elimination) of MIGS in the semiconductor to allow for an adjustable harrier height with a substantially thin layer that allows sufficient current to be transferred across the interface layer.

There are several methods by which the barrier height can be made adjustable. For example, adjustment may be made by tuning the degree of Fermi level pinning. In other words, some embodiments may allow for a sufficiently thin interface layer so that not all of the effects of MIGS in the Si are eliminated. Further, the pinning may be varied by combinations of thickness of the interface layer and the choice of interface material. The metal in contact with the interface layer may be pinned by MIGS at different levels in different materials. Conversely, or in addition, the passivation may be left incomplete to allow for an effective level of unpassivated states. Complete depinning of the Fermi level (that is removal of all surface states in Si including MIGS) is another option, in which case one could tune the barrier height simply by choosing a pure metal or an alloy that possesses the desired workfunction. In that case, the harrier height is determined by Equation (1), which until now has been an unrealizable idealization. Note that the type of tuning being discussed here is adjustment of the barrier height by altering the structure of the junction at the time of manufacture, not by varying an externally applied condition during junction operation.

FIG. **7***a*-**7***d* show relationships between Fermi energy, conduction band energy, and valence band energy for various Schottky barriers containing a metal in contact with (or in close proximity to) a semiconductor, where the bandgap (E_g) of the semiconductor exists between the conduction band (E_c) and the valence band (E_v). In this example, the work function of the metal Φ_M is chosen to be approximately equal to the electron affinity χ_S of the semiconductor. In FIG. **7***a*, an unpassivated Schottky barrier **700** is shown. In this example, the Fermi level (E_F) of the metal **730** is pinned in

the bandgap of the semiconductor **710**. This results in a discontinuity in the vacuum level caused by a charged dipole at the interface.

In FIG. **7***b*, the interface layer **720***b* is thick enough to passivate dangling bonds at the surface of the semiconductor **710**, but not thick enough to eliminate or sufficiently reduce the effect of MIGS. As a result, the band structure is largely unaltered from that seen in the previous illustration. Similarly, in FIG. **7***c*, when the interface layer **720***c* is sufficiently thick to eliminate or reduce the effect of MIGS but not to passivate the semiconductor surface, little change in the energy band structure is observed. However, as shown in FIG. **7***d*, when the interface layer **720***d* is sufficient to both eliminate or reduce the effect of MIGS and to passivate the semiconductor surface, we see the Fermi level of the metal aligning with the conduction band of the semiconductor (i.e., the Fermi level of the semiconductor has been depinned and no longer lines up with the Fermi level of the metal). The vacuum level is now continuous as there is no charged dipole at the interface. Thus, the band structure of a device constructed in this fashion is a result of only bulk material properties, not properties of the surface. By way of example, the materials in such cases may be Al and Si, with a work function for Al of approximately Φ_M=4.1 eV and the electron affinity for Si of approximately χ_S=4.05 eV.

V. Transistors Containing Passivated Semiconductor Surfaces

The interface layers described herein may be used in connection with a semiconductor surface of a channel in a field effect transistor. That is, an interface layer may be disposed between a source and a channel, a channel and a drain, or both of an insulated gate field effect transistor. Such use of an interface layer is described in detail in co-pending U.S. Pat. No. 6,833,556, issued Dec. 21, 2004, entitled "INSULATED GATE FIELD EFFECT TRANSISTOR HAVING PASSIVATED SCHOTTKY BARRIERS TO THE CHANNEL", filed Jan. 14, 2003 by the present inventors, and assigned to the assignee of the present invention.

The source and drain contacts at the channel of a field effect transistor are examples of a broader category of metal-interface layer-semiconductor contacts that make up the present invention. In the past, such contacts generally comprised a silicide-n+-Si junction, which formed a somewhat "leaky" Schottky diode, with a Fermi level of the semiconductor pinned at the midgap. In contrast, the present invention provides a contact wherein the Fermi level of the metal is aligned with the conduction band of the semiconductor (e.g., as shown in FIG. **7***d*). Note that in other cases, depending on the type of semiconductor material and conductors used, the Fermi level of the metal may align with the valence band of the semiconductor.

Although both types of junctions (i.e., the new passivated Schottky barrier junction and the conventional silicide-semiconductor junction) permit tunneling currents, the present junction can be fabricated with a much thinner interface layer as compared to the thickness of the silicide layer used previously. Indeed, thickness of an order of magnitude less than the silicide thickness can be expected. In a conventional silicide—semiconductor junction a Schottky barrier is formed which is comprised of a depletion layer. The tunnel barrier presented by such a depletion layer may be an order of magnitude thicker than the dielectric tunnel barrier in the present invention. The thinner interface layers provided by the present invention permit higher current across the junction (i.e., lower junction specific contact resistance).

Two other properties of the dielectric deserve mention. First is the property of the height of the barrier compared to the semiconductor conduction band (for electrons). In making the barrier thinner than a silicide barrier, the tradeoff may be a higher tunnel barrier (e.g., 2 eV for nitride, compared with about half the gap of 0.6 eV for silicide). Spacer layers may be used with lower harriers (e.g., TiO_2 has a barrier of less than 1 eV). Nevertheless, even with the higher barrier to electrons, the present inventors have determined that the resistance can still be one hundred times lower than a contact to silicon with a silicide barrier.

The second property is the effective mass of electrons in the dielectric. Larger mass electrons will not penetrate as far (i.e., because of their shorter wavelength) from the metal into the semiconductor. The less the electrons penetrate into the dielectric, the less the effect of MIGS in the dielectric. Thus, MIGS in the dielectric are reduced with larger bandgap and larger effective mass.

In addition the junction of the present invention can be used in making contacts to source or drain implanted wells and will have the advantage of reducing the need for high doping levels (which are now reaching their limits of solid solubility). The high doping profiles were required in the past in order to keep the junction depletion layer relatively thin, so as to increase the tunneling current, thus reducing the junction resistance. However, it is becoming increasingly difficult to increase doping profiles in order to provide low resistance junctions. It may be possible to reach the same level of resistance with a lower doping concentration using the present invention. It may further be possible to achieve much lower resistance even with lower doping concentration. When the present invention is used with high doping levels, the resistance will be further reduced.

Thus, methods and applications for semiconductor-interface layer-metal junctions have been described. Although described with reference to specific embodiments it should be remembered that various modifications and changes may be made to the techniques described herein without departing from the broader spirit and scope of the invention. The specification and drawings are accordingly to be regarded in an illustrative rather than a restrictive sense and the invention measured only in terms of the claims, which follow.

What is claimed is:

1. An electrical junction, comprising a region in a semiconductor substrate, a metal electrical contact to said region, and an interface layer between said region and said metal electrical contact, said region being electrically connected to said metal electrical contact through said interface layer and said interface layer comprising a metal oxide and a semiconductor oxide, and being in contact with said region in the semiconductor substrate and said metal electrical contact.

2. The electrical junction of claim **1**, wherein the semiconductor oxide comprises an oxide of the region in the semiconductor substrate.

3. The electrical junction of claim **2**, wherein the semiconductor oxide has a thickness of approximately 0.1 nm to 5 nm.

4. The electrical junction of claim **1**, wherein said region in the semiconductor substrate comprises a source or drain of a transistor.

5. The electrical junction of claim **1**, wherein said interface layer has a thickness sufficient to depin a Fermi level of the metal electrical contact in a vicinity of the junction yet thin enough to provide the junction with a specific contact resistivity that is generally dependent on: a workfunction of the metal electrical contact, a Fermi energy of the semicon-

ductor in the region, or both the workfunction of the metal electrical contact and the Fermi energy of the semiconductor in the region.

6. The electrical junction of claim **1**, wherein said interface layer is configured to provide a specific contact resistivity between the metal electrical contact and the region in the semiconductor of less than 10 Ω-μm^2.

7. The electrical junction of claim **1**, wherein said metal electrical contact comprises an alloy of a metal.

8. The electrical junction of claim **1**, wherein said metal oxide comprises an oxide of said metal electrical contact.

9. The electrical junction of claim **8**, wherein said semiconductor oxide comprises an oxide of the region in the semiconductor substrate.

10. The electrical junction of claim **8**, wherein said semiconductor oxide comprises an oxide of the region in the semiconductor substrate.

11. The electrical junction of claim **1**, wherein said metal oxide comprises an oxide of titanium.

12. The electrical junction of claim **11**, wherein said semiconductor oxide comprises an oxide of silicon.

13. The electrical junction of claim **12**, wherein said semiconductor oxide comprises silicon dioxide.

14. The electrical junction of claim **12**, wherein said region in the semiconductor substrate comprises an n-type doped source or drain of a transistor.

15. The electrical junction of claim **1**, wherein said metal electrical contact comprises titanium.

16. The electrical junction of claim **1**, wherein said metal electrical contact comprises tungsten.

17. An electrical junction, comprising:

a source or drain of a transistor, said source or drain comprising a semiconductor,

a metal electrical contact to said source or drain, and

an interface layer disposed between and in contact with said source or drain and said metal electrical contact, said source or drain being electrically connected to said metal electrical contact through said interface layer and said interface layer comprising an oxide of titanium and an oxide of the semiconductor.

18. The electrical junction of claim **17**, wherein said metal electrical contact includes titanium.

19. The electrical junction of claim **18**, wherein said semiconductor comprises silicon.

20. The electrical junction of claim **17**, wherein said metal electrical contact includes tungsten.

21. The electrical junction of claim **20**, wherein said semiconductor comprises silicon.

22. The electrical junction of claim **17**, wherein said semiconductor comprises silicon.

23. A semiconductor device, comprising:

a semiconductor region,

a metal electrical contact to said semiconductor region, and

an interface layer disposed between and in contact with said semiconductor region and said metal electrical contact, said semiconductor region being electrically connected to said metal electrical contact through said interface layer and said interface layer comprising an oxide of titanium and an oxide of the semiconductor region.

24. The semiconductor device of claim **23**, wherein said metal electrical contact includes titanium.

25. The semiconductor device of claim **24**, wherein said semiconductor region comprises silicon.

26. The semiconductor device of claim **23**, wherein said metal electrical contact includes tungsten.

27. The semiconductor device of claim **26**, wherein said semiconductor region comprises silicon.

28. The semiconductor device of claim **23**, wherein said semiconductor region comprises silicon.

29. An electrical junction, comprising:

a source or drain of a transistor, said source or drain comprising a semiconductor,

a metal electrical contact to said source or drain, and

an interface layer disposed between and in contact with said source or drain and said metal electrical contact, said source or drain being electrically connected to said metal electrical contact through said interface layer and said interface layer being less than 1 nm thick and comprising an oxide of the semiconductor.

30. The electrical junction of claim **29**, wherein the metal electrical contact comprises titanium.

* * * * *

CERTIFICATE OF SERVICE

I hereby certify that on June 24, 2022, I served a complete copy of the foregoing on all counsel of record by filing it with the United States Court of Appeals for the Federal Circuit using the CM/ECF system.

Dated: June 24, 2022 /s/ *Cosmin Maier*

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UNITED STATES COURT OF APPEALS
FOR THE FEDERAL CIRCUIT

CERTIFICATE OF COMPLIANCE WITH TYPE-VOLUME LIMITATIONS

Case Number: 2022-1539

Short Case Caption: Samsung Electronics Co., Ltd. v. Acorn Semi, LLC

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