

EXHIBIT 779B

Invalidity of U.S. Patent No. 8,796,779 in View of Additional References

As detailed in the cover pleading, and in addition to the reasons set forth in Exhibits 779A1–A2, the claims of the ’779 Patent are invalid under 35 U.S.C. §§ 102 & 103 based on the prior art references identified in these invalidity contentions, alone or in combination with the references cited below.¹ As explained in the cover pleading, a person of ordinary skill in the art as of the claimed priority date of the ’779 Patent would have been motivated to combine the prior art identified in these invalidity contentions with the references cited below.

Defendant reserves the right to amend or supplement this claim chart at a later date as more fully set forth in the Invalidity Contentions.

Where the chart below states that the reference “discloses” or “describes” or “teaches” a limitation, such disclosure may be express, inherent, or implicit. Unless otherwise indicated, all citations to other claim charts in the discussion of claim elements below refer specifically to the corresponding claim element of the other claim chart.

Claim	Claim Language	Exemplary Disclosures in Additional References
1 [pre]	A semiconductor device comprising:	The following references disclose and/or render obvious a “A semiconductor device comprising:,” as further described below. <i>See, e.g.,</i> U.S. Pat. No. 6,787,421 to Gilmer et al. (“Gilmer”) at:

¹ The identification of exemplary portions of the cited references, in some instances, rely at least in part on AICP’ apparent positions regarding the scope of its claims for purposes of asserting infringement. Defendant’s assertion that a particular limitation is disclosed by a prior art reference, or Defendant’s assertion that a particular limitation is disclosed by a prior art reference in a particular manner, may be based in part on AICP’ apparent claim interpretations. In relying in part on AICP’ apparent claim interpretations, Defendant does not admit that AICP’ apparent claim interpretations are supportable or proper or that the claim limitations in question are definite or otherwise amenable to construction. Nor does Defendant admit that the claims are enabled, adequately described, or cover patentable subject matter, or that any of the Accused Instrumentalities infringe any claim of the Asserted Patents. Nor shall anything stated herein be construed as an admission or waiver of any particular construction of any claim term, or argument under 35 U.S.C. § 112. Nothing in these claim charts should be understood as an admission relating to infringement, either literally or under the doctrine of equivalents, or as an admission relating to the Defendant’s understanding of the proper interpretation or scope of the Asserted Claim. Moreover, Defendant reserves the right to rely on additional citations or sources of evidence that may also be applicable, or that may become applicable in light of any Court order on claim construction, changes in AICP’ Preliminary Infringement Contentions, or information obtained during discovery as the case proceeds.

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Claim	Claim Language	Exemplary Disclosures in Additional References
		<p>[1:7-10]: The present invention relates generally to Semiconductor devices, and more particularly to Semiconductor devices formed having dual gate dielectric thicknesses and utilizing high-k gate dielectric materials. Such as metal oxides.</p> <p>[2:13-38] The present invention integrates a high-k dielectric material, preferably a metal oxide, in a dual gate process Sequence using a Single metal oxide deposition to form multiple gate dielectric Stacks of differing thicknesses. With the present invention, the metal oxide is formed over prepared Surfaces of the Substrate that already provide a difference in equivalent oxide thickness (EOT) between two different regions of the Substrate (e.g. the core logic region and the I/O region). For example, a single metal oxide layer is deposited over two different thicknesses of silicon dioxide or Silicon oxynitride. Thus, the metal oxide need not be etched selective to the underlying Silicon Substrate (which can damage the Substrate Surface) where a gate quality Surface is required. Also with the invention, the Single metal oxide layer forms an interface with a high quality Silicon dioxide or Silicon Oxynitride layer, as opposed to an interface with a Silicon Surface which has been damaged or otherwise treated as a result of using conventional DGO processing methods with a metal oxide dielectric. Thus, devices formed in accordance with the invention do not Suffer from degraded performance, e.g. current leakage, due to interface irregularities as a result of contamination or damaged Surfaces. Referring now to FIGS. 1-4, a semiconductor device 10 is fabricated in accordance with one embodiment of the invention.</p> <p><i>See, e.g.,</i> Japanese Patent App. Pub. No. JP2006/060155 to Yasuhira et al. (“Yasuhira”) at: The present invention relates to a semiconductor device and a method of manufacturing the same, and more specifically, an insulated gate field effect transistor having a plurality of types of gate insulating films made of a high dielectric constant insulating film (High-k film) formed on the semiconductor device (MISFET) and a method for forming the same on a semiconductor substrate.</p> <p><i>See, e.g.,</i> Japanese Patent App. Pub. No. JP2003/100896 to Fujiwara et al. (“Fujiwara”) at: [0001] BACKGROUND OF THE INVENTION 1. Field of the Invention The present invention relates to a semiconductor device having a MIS field effect transistor (hereinafter,</p>

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Claim	Claim Language	Exemplary Disclosures in Additional References
		<p>simply referred to as a transistor) having a gate insulating film made of a high dielectric material.</p> <p>[0013] A semiconductor device according to the present invention comprises a semiconductor substrate and a first substrate divided into the semiconductor substrate.</p> <p><i>See, e.g., U.S. Pat. No. 8,349,695 to Scheiper et al. (“Scheiper”) at:</i></p> <p>[Abstract] In sophisticated manufacturing techniques, the work function and thus the threshold voltage of transistor elements may be adjusted in an early manufacturing stage by providing a work function adjusting species within the high-k dielectric material with substantially the same spatial distribution in the gate dielectric materials of different thickness. After the incorporation of the work function adjusting species, the final thickness of the gate dielectric materials may be adjusted by selectively forming an additional dielectric layer so that the further patterning of the gate electrode structures may be accomplished with a high degree of compatibility to conventional manufacturing techniques. Consequently, extremely complicated processes for re-adjusting the threshold voltages of transistors having a different thickness gate dielectric material may be avoided.</p> <p>3:42-45: FIG. 1a schematically illustrates a cross-sectional view of a semiconductor device 100 which comprises a substrate 101 and a semiconductor layer 102 formed above the substrate 101.</p> <p><i>See, e.g., U.S. Pat. No. 7,335,561 to Sakai (“Sakai ’561”) at:</i></p> <p>[2:31-53] The typical ones of the inventions disclosed in this application will be briefly described as follows. A semiconductor integrated circuit device of the present invention comprising: a semiconductor Substrate; a first MIS transistor including a pair of first semiconductor regions formed in the semiconductor substrate and a first conductive piece formed above the semiconductor Substrate through a first gate insulation film in a region between the pair of the first semiconductor regions; and a second MIS transistor including a pair of second semiconductor regions formed in the semiconductor Substrate and a second</p>

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		<p>conductive piece formed above the semiconductor Substrate through a second gate insulation film in a region between the pair of the second semiconductor regions, wherein the thickness of the first gate insulation film is larger than the thickness of the second gate insulation film and the first gate insulation film is comprised of the first insulation film located on the semiconductor Substrate and the second insulation film located on the first insulation film; and wherein the second gate insulation film is comprised of a third insulation film located on the semiconductor substrate and the dielectric constant of the second and third insulation films is larger than the dielectric constant of the first insulation film.</p> <p>[5:19-22] FIG. 35 is a major part sectional view of a semiconductor substrate showing an example of the manufacturing method of a semiconductor integrated circuit according to an embodiment of the present invention in the order of steps;</p> <p>[6:1-18] An example of the manufacturing method for the semiconductor integrated circuit device according to an embodiment of the present invention will be described using major part sectional views of the semiconductor Substrate shown in FIGS. 1-40. In the Figures, a region A indicates a region in which a gate insulation film having a larger effective thickness is formed and the region B indicates a region in which a gate insulation film having a smaller effective thickness is formed. In the regions A, B, n-channel MIS transistor (hereinafter referred to as low V_{th} NMOS) having a low threshold value voltage (hereinafter referred to as V_{th}), p-channel MIS transistor (hereinafter referred to as low V_{th} PMOS) having a low V_{th}, n-channel MIS transistor (hereinafter referred to as high V_{th} NMOS) having a high V_{th} and p-channel MIS transistor (hereinafter referred to as high V_{th} PMOS) having a high V_{th} are formed and that is, eight kinds of the MIS transistors are formed on the same substrate.</p> <p><i>See, e.g., U.S. Pat. App. No. 2009/0039445 to Wu ("Wu '445") at:</i></p> <p>[Abstract] MOSFET gate structures comprising multiple width offset spacers are provided. A first and a second gate structure are formed on a semiconductor substrate. A pair of first offset spacers are formed adjacent either side of the first gate structure. Each of the first offset spacers comprises a first silicon oxide layer with a first dielectric layer overlying. A pair of second offset spacers are formed adjacent either side of the second gate structure. Each of the</p>

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		<p>second offset spacers comprises a second silicon oxide layer with a second dielectric layer overlying. Ion implanted doped regions are formed in the semiconductor substrate adjacent the first and second offset spacers respectively to form a first and second MOSFET device. A maximum width of each of the first offset spacers is different from that of the second offset spacers. The first silicon oxide layer is thinner than the second silicon oxide layer.</p> <p>[0002] This invention generally relates to processes for forming semiconductor device integrated circuits including CMOS and MOSFET devices and more particularly to mixed signal devices (i.e., analog and digital) and a method for forming the same to simultaneously optimize offset spacer widths to improve performance of both analog and digital CMOS devices including system on chip (SOC) devices.</p> <p>[0012] In a first embodiment, the method includes providing a semiconductor substrate including at least two gate structures; growing a silicon oxide layer having a respective differential thickness over the at least two gate structures; forming a dielectric layer on the silicon oxide layer having an etching selectivity with respect to the silicon oxide layer; forming offset spacers having a differential thickness including the dielectric layer and the silicon oxide layer adjacent either side of the at least two respective gate structures; and, carrying out an ion implant process adjacent the offset spacers to form doped regions in the semiconductor substrate forming at least two MOSFET devices.</p>

Claim	Claim Language	Exemplary Disclosures in Additional References
1 [a]	a first MIS transistor and a second MIS transistor of an identical conductivity type provided on an identical semiconductor substrate,	<p>The following references disclose and/or render obvious a “a first MIS transistor and a second MIS transistor of an identical conductivity type provided on an identical semiconductor substrate,” as further described below.</p> <p><i>See, e.g., U.S. Pat. No. 6,787,421 to Gilmer et al. (“Gilmer”) at:</i></p> <p>[1:7-10]: The present invention relates generally to Semiconductor devices, and more particularly to Semiconductor devices formed having dual gate dielectric thicknesses and utilizing high-k gate dielectric materials. Such as metal oxides.</p>

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Claim	Claim Language	Exemplary Disclosures in Additional References
		<p>[2:13-35] The present invention integrates a high-k dielectric material, preferably a metal oxide, in a dual gate process Sequence using a Single metal oxide deposition to form multiple gate dielectric Stacks of differing thicknesses. With the present invention, the metal oxide is formed over prepared Surfaces of the Substrate that already provide a difference in equivalent oxide thickness (EOT) between two different regions of the Substrate (e.g. the core logic region and the I/O region). For example, a single metal oxide layer is deposited over two different thicknesses of silicon dioxide or Silicon oxynitride. Thus, the metal oxide need not be etched selective to the underlying Silicon Substrate (which can damage the Substrate Surface) where a gate quality Surface is required. Also with the invention, the Single metal oxide layer forms an interface with a high quality Silicon dioxide or Silicon Oxynitride layer, as opposed to an interface with a Silicon Surface which has been damaged or otherwise treated as a result of using conventional DGO processing methods with a metal oxide dielectric. Thus, devices formed in accordance with the invention do not Suffer from degraded performance, e.g. current leakage, due to interface irregularities as a result of contamination or damaged Surfaces.</p> <p>[2:36-55] Referring now to FIGS. 1-4, a semiconductor device 10 is fabricated in accordance with one embodiment of the invention. Referring now to FIGS. 1-4, a semiconductor device 10 is fabricated in accordance with one embodiment of the invention. As shown in FIG. 1, semiconductor device 10 includes a Semiconductor Substrate 12 which in a preferred embodiment is a single crystal Silicon Substrate (also sometimes referred to as a wafer), but which can instead be formed from other Semiconductor Substrate materials. Within substrate 12, trench isolation regions 14, preferably shallow trench isolation regions, are formed in a conventional manner for the purpose of electrically isolating different individual devices to be formed. After forming trench isolation regions 14, a first gate dielectric 16 is formed over substrate 12. First gate dielectric 16 is preferably silicon dioxide or silicon oxynitride, and is preferably formed by thermal oxidation in accordance with conventional practices. The thickness of gate dielectric 16 is determined by the particular device requirements for devices to be formed in I/O device region 24 as further explained below, but generally will be within a range of 30–50 Angstroms (3-5 nanometers).</p>

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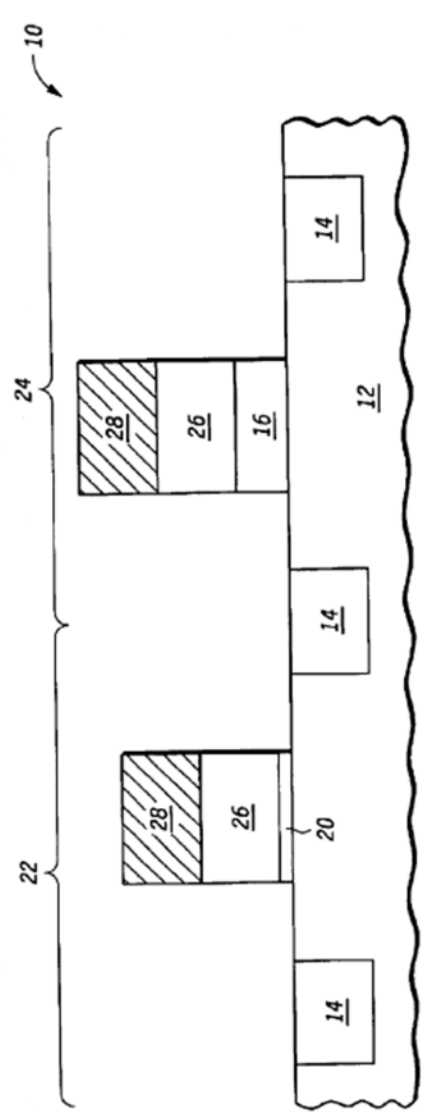
Claim	Claim Language	Exemplary Disclosures in Additional References
		 <p style="text-align: center;">FIG. 4</p> <p>See, e.g., Japanese Patent App. Pub. No. JP2006/060155 to Yasuhira et al. (“Yasuhira”) at:</p> <p>The present invention relates to a semiconductor device and a method of manufacturing the same, and more specifically, an insulated gate field effect transistor having a plurality of types of gate insulating films made of a high dielectric constant insulating film (High-k film) formed on the semiconductor device (MISFET) and a method for forming the same on a semiconductor substrate.</p> <p>In the following description, a p-channel type MISFET will be described, but an n-channel type MISFET is formed in the same manner. As shown in FIG. 1, for example, at least two types of MISFETs having gate insulating films having different equivalent film thicknesses in a region corresponding to a peripheral circuit portion on a p-conductivity type silicon substrate 1 and a</p>

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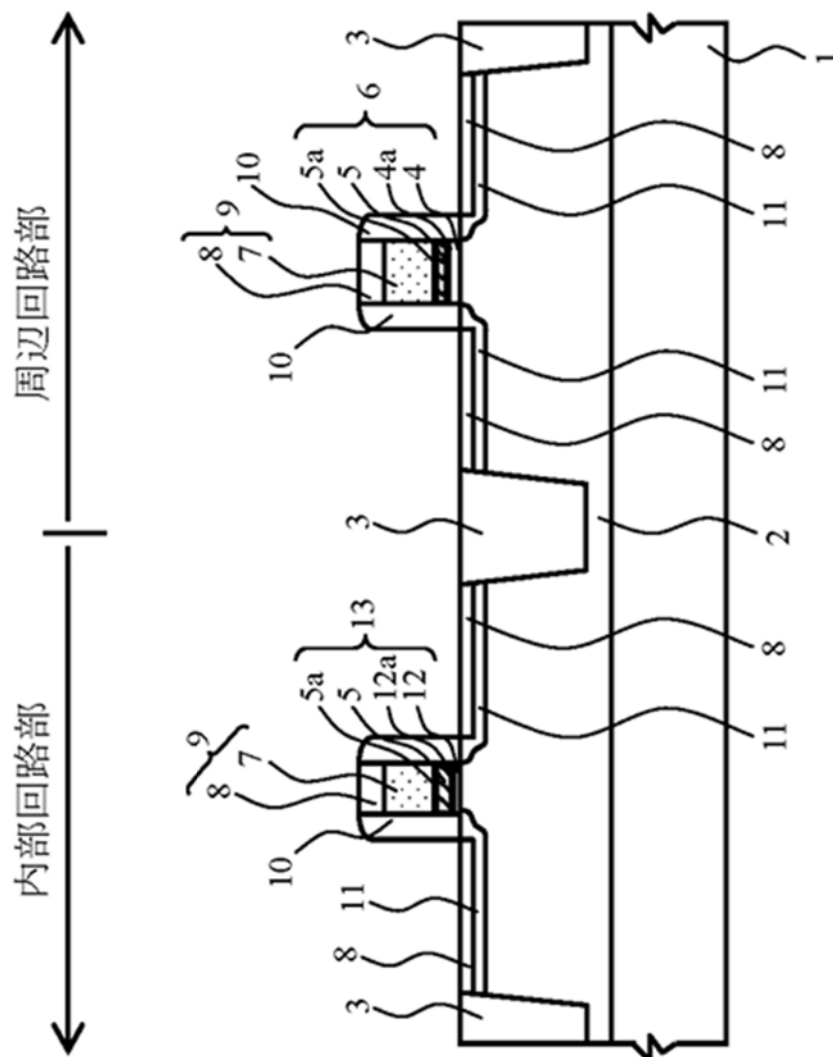
Claim	Claim Language	Exemplary Disclosures in Additional References
		<p>region corresponding to an internal circuit portion are provided. It is formed.</p> <p>【図 1】</p>  <p>The diagram is a cross-sectional view of a semiconductor device. It shows a substrate 1 with a central region 2 and side regions 3. A gate stack 4 is formed on the central region 2, and gate stacks 5 and 6 are formed on the side regions 3. The gate stack 4 includes a gate dielectric 4a and a gate electrode 4b. The gate stacks 5 and 6 include a gate dielectric 5a and gate electrodes 5b and 6b. A source/drain region 7 is formed in the central region 2, and source/drain regions 8 and 9 are formed in the side regions 3. A channel region 10 is formed in the central region 2, and channel regions 11 and 12 are formed in the side regions 3. A contact plug 13 is formed in the central region 2. A dashed line 14 indicates the boundary between the internal circuit portion and the peripheral circuit portion. A double-headed arrow at the bottom indicates the extent of the internal circuit portion.</p> <p>内部回路部</p> <p>周辺回路部</p> <p>See, e.g., Japanese Patent App. Pub. No. JP2003/100896 to Fujiwara et al. (“Fujiwara”) at:</p> <p>FIG. 11 is a cross-sectional view of the step of forming gate sidewalls and the step of implanting ions into the source and drain regions according to the first embodiment.</p>

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		<p><i>See, e.g.</i>, U.S. Pat. No. 8,349,695 to Scheiper et al. (“Scheiper”) at:</p> <p>4:1-4: Moreover, a basic dopant concentration may be established in the regions 102A, 102B corresponding to the conductivity type of the transistors to be formed in the respective active region.</p> <p>5:8-17: As previously explained, the layer 154 may be provided with different material characteristics for transistors of different conductivity type, such as P-channel transistors and N-channel transistors, in order to adjust an appropriate work function for each transistor type. For convenience, the material 154 in the active regions 102A, 102B may be provided for one type of transistor. Such as an N-channel transistor or a P-channel transistor, and may thus include any appropriate species, such as lanthanum for an N-channel transistor or aluminum for a P-channel transistor, and the like.</p> <p>6:26-36: Furthermore, drain and source regions 161 are formed in the active regions 102A, 102B. The drain and source regions 161 may be formed on the basis of well-established process techniques, such as ion implantation and the like, wherein the spacer structure 157 may be used as an implantation mask during some of the required implantation steps. As previously indicated, the transistors 160A, 160B may have a different threshold Voltage for a given configuration of the drain and Source regions 161 and the channel region 162, which may require additional process steps for re-adjusting the threshold voltage of at least one of the transistors 160A, 160B.</p>

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Claim Language		
Exemplary Disclosures in Additional References	<p>FIG. 1g (prior art)</p>	
	<p>See, e.g., U.S. Pat. No. 7,335,561 to Sakai ("Sakai '561") at:</p> <p>[2:31-53] The typical ones of the inventions disclosed in this application will be briefly described as follows. A semiconductor integrated circuit device of the present invention comprising: a semiconductor Substrate; a first MIS transistor including a pair of first semiconductor regions formed in the semiconductor substrate and a first conductive piece formed above the semiconductor Substrate through a first gate insulation film in a region between the pair of the first semiconductor regions; and a second MIS transistor including a pair of second semiconductor regions formed in the semiconductor Substrate and a second conductive piece formed above the semiconductor Substrate through a second gate insulation film in a region</p>	

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		<p>between the pair of the second semiconductor regions, wherein the thickness of the first gate insulation film is larger than the thickness of the second gate insulation film and the first gate insulation film is comprised of the first insulation film located on the semiconductor Substrate and the second insulation film located on the first insulation film; and wherein the second gate insulation film is comprised of a third insulation film located on the semiconductor substrate and the dielectric constant of the second and third insulation films is larger than the dielectric constant of the first insulation film.</p> <p>[5:19-22] FIG. 35 is a major part sectional view of a semiconductor substrate showing an example of the manufacturing method of a semiconductor integrated circuit according to an embodiment of the present invention in the order of steps;</p> <p>[6:1-18] An example of the manufacturing method for the semiconductor integrated circuit device according to an embodiment of the present invention will be described using major part sectional views of the semiconductor Substrate shown in FIGS. 1-40. In the Figures, a region A indicates a region in which a gate insulation film having a larger effective thickness is formed and the region B indicates a region in which a gate insulation film having a smaller effective thickness is formed. In the regions A, B, n-channel MIS transistor (hereinafter referred to as low V_{th} NMOS) having a low threshold value voltage (hereinafter referred to as V_{th}), p-channel MIS transistor (hereinafter referred to as low V_{th} PMOS) having a low V_{th}, n-channel MIS transistor (hereinafter referred to as high V_{th} NMOS) having a high V_{th} and p-channel MIS transistor (hereinafter referred to as high V_{th} PMOS) having a high V_{th} are formed and that is, eight kinds of the MIS transistors are formed on the same substrate.</p> <p>[6:19-24] First, as shown in FIG. 1, a semiconductor substrate comprised of for example, p-type silicon crystal is prepared. Next, thin silicon oxide film 2 about 0.01 μm is formed by oxidizing this semiconductor Substrate 1 thermally and a silicon nitride film 3 about 0.1 μm is deposited according to CVD (chemical vapor deposition) method.</p>

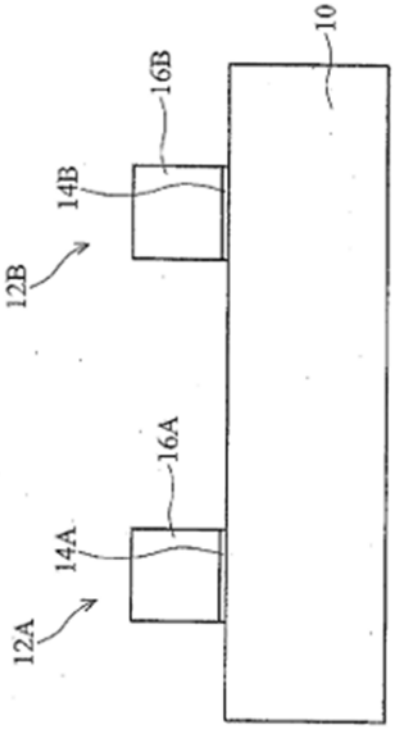
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Claim		
Claim Language		
Exemplary Disclosures in Additional References	<p>FIG. 35</p>	
	<p>See, e.g., U.S. Pat. App. Pub. No. 2009/0039445 to Wu ("Wu '445") at:</p> <p>[0016] Although the method of the present invention is explained by reference to exemplary CMOS transistors (i.e., MOSFET) devices, it will be appreciated that the present invention may be applied to various CMOS devices where MOSFET transistors having operationally distinguishable characteristics are formed on a single chip, e.g., in a system on chip (SOC) implementation to achieve individually optimized performance of transistors in a parallel manufacturing process.</p>	

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		<p>[0029] It will additionally be appreciated that the dual offset spacer widths may be used to form logic and SRAM devices, for example the relatively thicker offset spacer width forming a portion of SRAM transistors and the relatively thinner offset spacer widths forming a portion of logic transistors. In addition, dual spacer widths may be used to form an NMOS SRAM cell transistor (relatively thicker offset spacer width) and a PMOS SRAM cell transistor (relatively thinner offset spacer width).</p> <p>[0031] Thus, MOSFET devices having differentially wide offset spacers and associated ion implanted (doped) regions forming operationally distinguishable devices and a method for forming the same has been presented such that a cost effective way for forming respective ion implants to form doped regions adjacent gate structures can be accomplished with a minimal number of steps and be optimized for formation of different MOSFET devices in parallel. For example, analog/digital, logic/SRAM, and SRAM PMOS/NMOS MOSFET devices may be formed in parallel processes with a reduced number of processing steps on a single chip, including in a system on chip (SOC) implementation. Advantageously, analog devices having a thicker offset spacer width may be formed with doped regions optimized for Voltage threshold matching and Voltage gain while the thinner offset spacer width may be formed with doped regions being optimized for reducing SCE effects and increasing drive current.</p>

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Claim	Claim Language	Exemplary Disclosures in Additional References
		 <p>FIG. 1A</p>

Claim	Claim Language	Exemplary Disclosures in Additional References
1 [b]	wherein the first MIS transistor includes a first gate insulating film formed on a first active region in the semiconductor substrate and a first gate electrode formed on the first gate insulating film,	<p>The following references disclose and/or render obvious a “wherein the first MIS transistor includes a first gate insulating film formed on a first active region in the semiconductor substrate and a first gate electrode formed on the first gate insulating film,” as further described below.</p> <p><i>See, e.g., U.S. Pat. No. 6,787,421 to Gilmer et al. (“Gilmer”) at:</i></p> <p>[2:36-55] Referring now to FIGS. 1-4, a semiconductor device 10 is fabricated in accordance with one embodiment of the invention. Referring now to FIGS. 1-4, a semiconductor device 10 is fabricated in accordance with one embodiment of the invention. As shown in FIG. 1, semiconductor device 10 includes a Semiconductor Substrate 12 which in a preferred embodiment is a single crystal Silicon Substrate (also sometimes referred to as a wafer), but which can instead be formed from other Semiconductor Substrate materials. Within substrate</p>

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		<p>12, trench isolation regions 14, preferably shallow trench isolation regions, are formed in a conventional manner for the purpose of electrically isolating different individual devices to be formed. After forming trench isolation regions 14, a first gate dielectric 16 is formed over substrate 12. First gate dielectric 16 is preferably silicon dioxide or silicon oxynitride, and is preferably formed by thermal oxidation in accordance with conventional practices. The thickness of gate dielectric 16 is determined by the particular device requirements for devices to be formed in I/O device region 24 as further explained below, but generally will be within a range of 30–50 Angstroms (3-5 nanometers).</p> <p>[2:56-3:6] After forming first gate dielectric 16, a (photo)resist mask 18 is formed over the substrate to mask off a portion of the first gate dielectric layer. AS shown in FIG. 1, Semiconductor device 10 includes two different device regions, namely a core device region 22 and an I/O device region 24. In operation, devices to be formed in core device region 22 require thinner gate dielectrics that operate at lower Voltages than, e.g., I/O devices to be formed in I/O device region 24 that can withstand higher Voltages required for I/O functions. Accordingly, resist mask 18 is formed to protect the portion of first gate dielectric 16 which will Serve, in part, as a gate dielectric for the higher Voltage I/O devices. Other dielectric materials may instead be used for first gate dielectric 16. Silicon dioxide and silicon oxynitride are attractive choices because of the industry's understanding of these materials, the ability to form high gate quality films, and because they can be formed by Selective growth techniques rather than requiring blanket depositions and etch steps.</p> <p>[3:44-4:7] Now that gate dielectrics of two different thicknesses have been formed, a high-k dielectric (generally with $k > 4$, preferably with $k > 6$, and most preferably with $k > 7$) is deposited over semiconductor device 10. In a preferred embodiment, this high-k dielectric is a metal oxide, Such as metal oxide 26 shown in FIG. 3. Suitable materials for metal oxide 26 preferably include hafnium oxide (HfO₂), hafnium silicate (HfSiO₂), or lanthanum aluminate (LaAlO₃), but lanthanum oxide, hafnium aluminate, Zirconium oxide, and Zirconium Silicate, and other like materials, may also be Suitable high-k dielectrics. The thickness of the high-k dielectric layer will be dependent on the particular device requirements in each region of the Substrate (the core region and the I/O region), but generally it is believed the thickness of a metal oxide will be between about 15-50 angstroms (1.5-5.0 nanometers). The underlying thicknesses of first gate</p>

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		<p>dielectric 16 and Second gate dielectric 20 will also affect the choice of thickness of the high-k dielectric. The thickness of the high-k dielectric should be chosen So that its equivalent oxide thickness (EOT), when added to the EOT of the first gate dielectric 16 (I/O device dielectric) thickness or Second gate dielectric 20 (core device dielectric) thickness, provides a total EOT appropriate for the I/O and core device, respectively. Similarly, this calculation should be used to determine the initial deposited or grown thicknesses of the first and Second gate dielectrics. Because metal oxide 26 is deposited as a single blanket deposition, its thickness will not vary much across the Substrate Surface and thus one should use the thicknesses of the first and Second dielectrics as the “variables” to achieve the final EOTs for the core and I/O devices.</p> <p>FIG. 4</p>
		<p>See, e.g., Japanese Patent App. Pub. No. JP2006/060155 to Yasuhira et al. (“Yasuhira”) at:</p> <p>On the other hand, in the MISFET of the internal circuit portion, the base film 12 with a film thickness of about 1 nm and the nitride layer 12a whose surface is modified to a nitrogen-containing layer, the High-k film 5 and the nitride layer which is a modified layer on the surface thereof A second gate insulating film 13 is formed by the laminated film 5 a, and the above-described polycrystalline silicon layer 7 and silicide layer 8 are provided on the second gate</p>

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		<p>insulating film 13. Sidewall insulating films 10 are provided on the side walls of the second gate insulating film 13 and the gate electrode 9, and source / drain regions including the source / drain diffusion layers 11 and the silicide layers 8 are provided on the surface of the n-well layer 2. It has been. In the second gate insulating film 13 of the MISFET, the base film 12 has a silicon oxide film structure as a basic structure, and is interposed between the high-k film 5 and the silicon substrate 1 on the surface of the n-well layer 2. It has functions such as preventing boron penetration and improving the surface mobility of carrier charges (holes).</p> <p>Next, a method for manufacturing the semiconductor device according to the present invention will be described with reference to FIGS. Here, the same components as those in FIG. 1 are denoted by the same reference numerals.</p> <p>Then, without leaving time, thermal oxidation in a dilute oxygen atmosphere or plasma oxidation at a low temperature (for example, 300 ° C. temperature) is performed to form the base film 12 having a film thickness of about 1 nm. Here, the base film 12 is a silicon oxide film (FIG. 2C).</p> <p>Next, the surfaces of the base oxide film 4 and the base film 12 are nitrided by plasma nitriding, and the silicon oxide film surfaces are modified to form nitride layers 4a and 12a as nitrogen-containing layers (FIG. 2D). . In this plasma nitriding method, N₂ gas, N₂O, NO, N₂H₂ and NH₃ gas, which are raw material gases, are excited by plasma in ECR (Electron Cyclotron Resonance), ICP (Inductively Coupled Plasma), (magnetron type)) Active species of nitrogen are generated by excitation with RF plasma or helicon wave plasma, and the active species are exposed to the surface of the silicon oxide film. The active species include nitrogen atom ions, molecular ions, neutral radicals, and the like. Here, it is preferable that only the nitrogen neutral radicals are extracted from the active species to form the nitride layers 4a and 12a. For example, among the active species of nitrogen formed in the plasma excitation chamber, neutral radicals having a relatively long lifetime are extracted by the downflow method, and the neutral oxides are irradiated onto the surface of the base oxide film 4 and the base film 12. In this manner, the nitride layers 4a and 12a are preferably formed by the reaction between neutral radicals and the surface of the silicon oxide film.</p>

Claim	Claim Language	Exemplary Disclosures in Additional References
		<p>【図 1】</p> <p>内部回路部 周辺回路部</p> <p>The diagram is a cross-sectional view of a semiconductor device. It is divided into two main regions: the 'Internal Circuit Region' (内部回路部) on the left and the 'Peripheral Circuit Region' (周辺回路部) on the right, separated by a vertical line. Both regions feature a substrate (1) with a first substrate layer (11) and a second substrate layer (8). In the internal circuit region, there are two main structures: a first structure (3) with a gate stack (5, 5a) and a channel region (12, 12a), and a second structure (10) with a gate stack (7, 8) and a channel region (9). In the peripheral circuit region, there is a similar structure (3) with a gate stack (5, 5a) and a channel region (4, 4a). The peripheral circuit region also includes a first substrate layer (11) and a second substrate layer (8). The diagram is labeled with various reference numerals: 1, 2, 3, 4, 4a, 5, 5a, 6, 7, 8, 9, 10, 11, 12, 12a, 13.</p> <p>See, e.g., Japanese Patent App. Pub. No. JP2003/100896 to Fujiwara et al. (“Fujiwara”) at:</p> <p>A semiconductor device according to the present invention comprises a semiconductor substrate and a first substrate divided into the semiconductor substrate.</p>

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Claim	Claim Language	Exemplary Disclosures in Additional References
		<p>A first transistor having a first gate insulating film having a structure in which a first insulating film and a second insulating film are stacked in this order from the semiconductor substrate, and are divided into the semiconductor substrate. The third insulating film and the fourth insulating film formed in the second region are stacked in this order from the semiconductor substrate, and the silicon oxide film is formed as compared with the first gate insulating film. A second transistor having a second gate insulating film having a large converted film thickness, and the second and fourth transistors.</p> <p>The insulating film of is a high-dielectric film formed at the same time.</p> <p>And the third insulating film are interface layers having different compositions or film thicknesses from each other. Particularly preferably, the first and third insulating films are interface layers having different compositions from each other formed by the reaction between the second and third insulating films and the semiconductor substrate or the thin film formed on the surface thereof. I shall.</p> <p>The present invention is also a method of manufacturing a semiconductor device including transistors having different gate insulating film structures, which comprises selectively forming an oxygen barrier layer on the surface of the first region of the semiconductor substrate, A high dielectric insulating film is formed on the semiconductor substrate, the first region includes the oxygen barrier layer or an interface layer formed of a reaction layer between the oxygen barrier layer and the high dielectric film, and the second region includes the semiconductor. It is characterized by including a step of forming a gate insulating film including an interface layer by a reaction between a substrate and the high dielectric film, and a step of patterning a gate electrode on the gate insulating film.</p> <p>In the present invention, the high dielectric film (metal oxide or its silicate) as the gate insulating film is formed, or is formed on the substrate during the subsequent crystallization annealing. The interface layer formed between the thin film and the thin film has different characteristics and structure by controlling the electrical film thickness and film quality of the interface layer by introducing nitrogen into the substrate surface or inserting a thin film nitride film. A gate</p>

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		<p>insulating film is formed on the same substrate. In other words, by treating the interface layer that was previously integrated with the high-k dielectric film as a laminated structure with independent functions, by forming a high-k dielectric film with a sufficient thickness to suppress direct tunneling. By suppressing the gate leakage current and making the state of the substrate interface different depending on the transistor region, the gate insulating film can be selectively used for each transistor which requires different specifications.</p> <p>Next, a sacrificial oxide film 61 is formed by dilute hydrofluoric acid treatment. Was removed, after performing the hydrogen-terminated silicon substrate 51 surface, as shown in FIG. 8, TiO 2 is a high dielectric film</p> <p>The film 81 is formed. Specifically, the TiO 2 film 81 having a thickness of 5 nm is formed by the DC sputtering method using a TiO 2 sintered target under the sputtering conditions of power 300 W, pressure 1 Pa, Ar / O 2 flow rate 22 / 1.2 sccm. . At this time, the surface of the silicon substrate in the regions A and B is oxidized by the oxygen plasma atmosphere during the sputtering of the TiO 2 film, and the interface layers 82 and 83 are formed. The interface layer 82 in the region A has the result that the nitrogen introduction region 64 suppresses the diffusion of oxygen into the substrate.</p> <p>It becomes a thin silicon oxide film, and the interface layer 83 in the region B becomes a thicker silicon oxide film.</p> <p>A polycrystalline silicon film having a thickness of 175 n is formed on the upper surface by a CVD method.</p> <p>A gate electrode 91 is formed by forming a film and performing patterning. Along with the gate electrode 91, the TiO 2 film 81 and the interface layers 82 and 83 which will be the gate insulating film thereunder are also patterned. After that, in order to crystallize the TiO 2 film 81, RTA with a heat treatment temperature of 900 ° C. and a heat treatment time of 30 seconds is performed.</p> <p>Do. At this time, the surface of the silicon substrate in the region B is oxidized by the diffusion of oxygen from the TiO 2 film 81 to the silicon substrate 51 by RTA, and the interface layer 83 grows to finally become the interface layer 83a of about 2 nm. In the region A, the nitrogen introduction region 64 suppresses the diffusion of oxygen into the substrate, The growth of the</p>

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Claim	Claim Language	Exemplary Disclosures in Additional References
		<p>interface layer 82 is suppressed, and finally about 0.7 nm. The interface layer 82a has a thickness of nm.</p> <p>The TiO₂ film 81 becomes a microcrystalline state by the RTA treatment, and its dielectric constant is about 20. Therefore, the equivalent oxide film thickness of this portion is about 1 nm. Also, Ti.</p> <p>By the physical mixing of Ti into the substrate by sputtering of the O₂ film 81 and the activation annealing performed in a later step, the interface layers 82a and 83a become silicon oxide films containing a trace amount of Ti, and their dielectric constant is 5. It will be about.</p> <p>Therefore, the gate insulating film in the region A has a laminated structure of the interface layer 82a and the TiO₂ film 81, and the gate insulating film in the region B has a laminated structure of the interface layer 83a and the TiO₂ film 81. These gate insulating films have a physical film thickness of 5 nm or more, and can sufficiently suppress the direct tunneling current. On the other hand, due to the difference in the film thickness of the interface layers 82a and 83b, in the region A, the oxide film equivalent film thickness is 1.6n.</p> <p>In the region B, the gate insulating film of m has an oxide film equivalent thickness of 2.6. Thus, the gate insulating film having a thickness of nm is formed.</p> <p>Next, as shown in FIG. 10, N-type impurities are ion-implanted substantially perpendicularly to the silicon single crystal substrate 51 to form shallow source / drain n-type diffusion layers 101. Specifically, for example, arsenic is accelerated at an acceleration voltage of 5 keV to 10 keV, dose amount $5 \times 10^{14} / \text{cm}^2$ to $1 \times 10^{15} / \text{cm}^2$ Inject.</p> <p>As described above, according to this embodiment, the transistors Q1 and Q2 formed in the regions A and B are formed.</p> <p>Are formed of gate insulating films having different physical thicknesses of silicon oxide, while having a physical film thickness sufficient to suppress the direct tunneling current. Due to the difference in the gate insulating film structure, the transistor Q1 in the region A is relatively</p>

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Claim		
Claim Language	Exemplary Disclosures in Additional References	inferior in gate breakdown voltage and reliability to the transistor Q2 in the region B, but has a characteristic difference in high current driving capability.
		The gate insulating film has a laminated structure of a high dielectric film and an interface layer formed as a reaction layer between the high dielectric film and the substrate. By changing it, the interface layers of both are different. Moreover, the processing for changing the substrate surface state can be performed using the mask for channel ion implantation in the regions A and B as it is. Therefore, although the transistors Q1 and Q2 have different types of gate insulating film structures, the manufacturing process is simple, with only one additional ion implantation step.
		【図 1】
		<p>A cross-sectional view of two transistors, Q1 and Q2, on a common substrate. Both transistors feature a p-type substrate (P) with n+ regions (63, 64). They have a gate stack (91, 92) and a channel region (81, 82a). The diagram illustrates various layers (101, 111, 112, 54) and dimensions (A, B).</p>
		See, e.g., U.S. Pat. No. 8,349,695 to Scheiper et al. (“Scheiper”) at:

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Claim	Claim Language	Exemplary Disclosures in Additional References
		<p>3:42-63: FIG. 1a schematically illustrates a cross-sectional view of a semiconductor device 100 which comprises a substrate 101 and a semiconductor layer 102 formed above the substrate 101. The semiconductor layer 102 is typically provided in the 45 form of a silicon material, as explained above. Moreover, a first semiconductor region 102A and a second semiconductor region 102B are provided in the semiconductor layer 102. The active regions 102A, 102B are to be understood as semiconductor regions in and above 50 which transistor elements are to be formed on the basis of gate electrode structures including a high-k dielectric material. In the example shown, it may be assumed that a gate electrode structure of reduced gate dielectric thickness is to be formed on the semiconductor region 102A, while a gate electrode 55 structure having a gate dielectric material of increased thickness is to be formed on the semiconductor region 102B. Furthermore, in the manufacturing stage shown, a gate dielectric material 151 is selectively formed on the active region 102B and is comprised of silicon dioxide with a specific 60 thickness, for instance with a thickness of several nanometers, depending on the device requirements or any transistors to be formed in and above the semiconductor region 102B.</p> <p>4:37-56: FIG. 1c schematically illustrates the semiconductor device 100 when exposed to a deposition ambient 106 in which a high-k dielectric material. Such as hafnium oxide, is deposited above the active regions 102A, 102B, thereby forming a high-k dielectric layer 153. Thus, the layers 152 and 153 in combination may represent the gate dielectric material of a transistor to be formed in and above the semiconductor region 102A, thereby providing the required characteristics for high performance transistors, while the layer 153 in combination with the “thick” silicon dioxide material 151 represents the dielectric material for transistors and other circuit elements in which a Superior performance with respect to reduced leakage currents and the like is required. It should be appreciated that the deposition process 106 may be performed on the basis of any appropriate deposition recipe, for instance, by chemical vapor deposition (CVD), physical vapor deposition (PVD) and the like. For example, a thickness of the high-k dielectric layer 153 may be in the range of one to several nanometers, depending on the overall requirements in view of capacitive coupling, leakage currents and the like.</p>

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Claim	Claim Language	Exemplary Disclosures in Additional References
		<p>FIG. 1g (prior art)</p>
		<p>See, e.g., U.S. Pat. No. 7,335,561 to Sakai ("Sakai '561") at:</p> <p>[2:31-53] The typical ones of the inventions disclosed in this application will be briefly described as follows. A semiconductor integrated circuit device of the present invention comprising: a semiconductor Substrate; a first MIS transistor including a pair of first semiconductor regions formed in the semiconductor substrate and a first conductive piece formed above the semiconductor Substrate through a first gate insulation film in a region between the pair of the first semiconductor regions; and a second MIS transistor including a pair of second semiconductor regions formed in the semiconductor Substrate and a second conductive piece formed above the semiconductor Substrate through a second gate insulation film in a region</p>

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Claim	Claim Language	Exemplary Disclosures in Additional References
		<p>between the pair of the second semiconductor regions, wherein the thickness of the first gate insulation film is larger than the thickness of the second gate insulation film and the first gate insulation film is comprised of the first insulation film located on the semiconductor Substrate and the second insulation film located on the first insulation film; and wherein the second gate insulation film is comprised of a third insulation film located on the semiconductor substrate and the dielectric constant of the second and third insulation films is larger than the dielectric constant of the first insulation film.</p> <p>[5:19-22] FIG. 35 is a major part sectional view of a semiconductor substrate showing an example of the manufacturing method of a semiconductor integrated circuit according to an embodiment of the present invention in the order of steps;</p> <p>[6:1-18] An example of the manufacturing method for the semiconductor integrated circuit device according to an embodiment of the present invention will be described using major part sectional views of the semiconductor Substrate shown in FIGS. 1-40. In the Figures, a region A indicates a region in which a gate insulation film having a larger effective thickness is formed and the region B indicates a region in which a gate insulation film having a smaller effective thickness is formed. In the regions A, B, n-channel MIS transistor (hereinafter referred to as low V_{th} NMOS) having a low threshold value voltage (hereinafter referred to as V_{th}), p-channel MIS transistor (hereinafter referred to as low V_{th} PMOS) having a low V_{th}, n-channel MIS transistor (hereinafter referred to as high V_{th} NMOS) having a high V_{th} and p-channel MIS transistor (hereinafter referred to as high V_{th} PMOS) having a high V_{th} are formed and that is, eight kinds of the MIS transistors are formed on the same substrate.</p> <p>[7:60-8:4] Next, after the resist pattern RP10 is removed, as shown in FIG. 16, the protective film 5 is removed and the silicon oxide film 9 is formed on the surface of the semiconductor substrate 1, for example, in the thickness of 4 to 5 nm. The silicon oxide film 9 can be formed according to the thermal CVD method or thermal oxidation method. Meanwhile, the aforementioned silicon oxide film may be turned to silicon nitride film by nitriding the semiconductor substrate 1 thermally. The aforementioned thermal nitration is carried out with the semiconductor 1 heated at about 900° C. in a pressure reduced atmosphere containing nitrogen made radical by plasma discharge</p>

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Claim	Claim Language	Exemplary Disclosures in Additional References
		<p>[8:5-10] Next, as shown in FIG. 17, after the region A is covered with the resist pattern RP1, as shown in FIG. 18, the silicon oxide film 9 in the region B is removed using diluted HF with resist pattern RP11 as a mask. After that, as shown in FIG. 19, the resist pattern RP11 is removed.</p> <p>[8:11-26] Next, as shown in FIG. 20, high dielectric constant insulation film 10, for example, alumina film is formed on the semiconductor substrate 1. The high dielectric constant insulation film 10 can be deposited according to, for example, sputtering method. The thickness of the high dielectric constant insulation film 10 formed on the semiconductor substrate 1 is set so that its effective thickness is about 5 nm. For example, the alumina film is deposited in the thickness of about 10 nm considering dielectric constant. Consequently, gate insulation film 11 comprised of the high dielectric constant insulation film 10 about 5 nm in terms of its effective thickness is formed in the region B and gate insulation film 12 comprised of stacked film of the high dielectric constant film 10 and the silicon oxide film 9 about 9 to 10 nm in terms of its effective thickness is formed in the region A</p> <p>[8:27-31] Before forming the aforementioned high dielectric constant insulation film 10 on the semiconductor substrate 1, silicon oxide film or silicon nitride film, or silicon oxide nitride film less than 1 nm or less may be formed to stabilize an interface with the semiconductor substrate 1.</p> <p>[8:32-34] Next, as shown in FIG. 21, silicon film 13 about 200 nm. thick is deposited on the semiconductor Substrate 1 according to the CVD method.</p> <p>[8:35-39] Next, as shown in FIG.22, after resist pattern 12 is formed in the NMOS formation region in the regions A, B, p-type impurity, for example, boron is ion-implanted into the silicon film 13 in the PMOS formation region in the regions A, B with this resist pattern RP12 as a mask.</p> <p>[8:40-46] Next, the resist pattern 12 is removed and as shown in FIG. 23, resist pattern RP13 is formed in the PMOS formation region in the regions A, B. After that, n-type impurity, for example, phosphorus is ion-implanted into the NMOS formation region in the regions A, B with this resist pattern RP13 as a mask.</p>

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Claim	Claim Language	Exemplary Disclosures in Additional References
		<p>[8:47-55] Next, after the resist pattern RP13 is removed, by per forming heat treatment on the semiconductor Substrate 1, for example at 950° C. for about 60 seconds, the aforementioned n-type impurity and p-type impurity implanted into the silicon film 13 are activated. Further, the silicon film 13 in the NMOS formation region in the regions A, B is turned to n-type silicon polycrystal film and the silicon film 13 in the PMOS formation region in the regions A, B is changed to p-type silicon polycrystal film.</p> <p>[8:56-60] After as shown in FIG. 24, silicon oxide film 14 is deposited on the semiconductor Substrate 1 according to the CVD method, as shown in FIG. 25, resist pattern RP14 is formed to form gate electrodes of the n-channel and p-channel MIS transistor.</p> <p>[8:61-9:3] Next, after as shown in FIG. 26, the silicon oxide film 14 is etched with the resist pattern RP14 as a mask, the resist pattern RP14 is removed. Subsequently, as shown in FIG. 27, with the patterned silicon oxide film 14 as a mask, the silicon film 13 is etched so as to form a gate electrode (conductive piece) 15n comprised of n-type silicon poly crystal film in the NMOS formation region in the regions A, B and a gate electrode (conductive piece) comprised of p-type silicon polycrystal film in the PMOS formation region in the regions A, B</p>

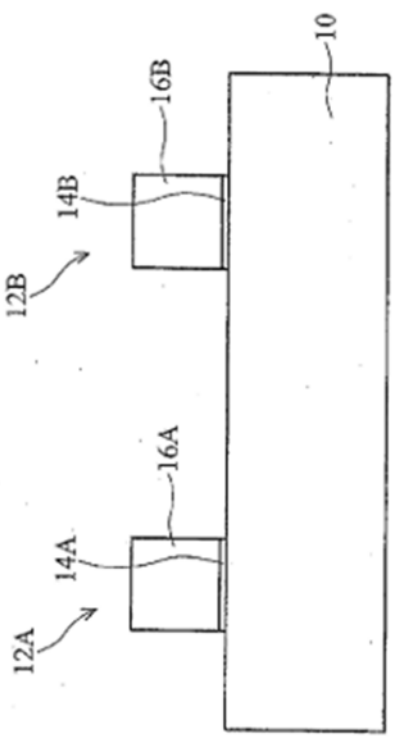
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Claim	Claim Language	Exemplary Disclosures in Additional References
		<p>combinations thereof. It will be appreciated that an electrical isolation structure such as a shallow trench isolation (STI) structure (not shown) may be provided between gate structures 12A and 12B to isolate the respective MOSFET devices.</p> <p>[0018] Still referring to FIG. 1A, the gate structures 12A and 12B may be formed by conventional CVD deposition, lithographic patterning, and plasma (dry) etching methods known in the art. The gate dielectric portions 14A and 14B may be formed by any process known in the art, e.g., thermal oxidation, nitridation, sputter deposition, chemical vapor deposition, or combinations thereof. The gate dielectric portions 14A and 14B may be formed of silicon oxide, silicon nitride, silicon oxynitride, and high-K dielectrics (e.g., K>8) including transition metal oxide and rare earth metal oxides. For example, high-K dielectrics may be formed of aluminum oxides (e.g., Al₂O₃), hafnium oxides (e.g., HfO₂), hafnium oxynitrides (HfON), hafnium silicates (e.g. HfSiO₄), hafnium silicon oxynitrides (e.g., HfSixOyNz), zirconium oxides (e.g., ZrO₂), zirconium oxynitrides (e.g., ZrON), zirconium silicon oxides (e.g., ZrSiO₂), yttrium oxides (Y₂O₃), lanthanum oxides (La₂O₃), cerium oxides (CeO₂), titanium oxides (TiO₂), tantalum oxides (Ta₂O₅), or combinations thereof. The high-k dielectric layer may be formed by known CVD methods such as atomic layer CVD (ALCVD) and metal-organic CVD (MOCVD). It will be appreciated that the high-K dielectric layer may include a lowermost interfacial layer formed on the semiconductor substrate such as an oxide or oxynitride (not shown).</p> <p>[0019] The gate electrode portions, 16A and 16B may be formed of poly gate such as polysilicon, amorphous polysilicon, doped polysilicon, polysilicon-germanium, or metal gate such as TaC, TaN, TiN, MoN or combinations thereof). For example, a gate dielectric layer is first formed by CVD, sputtering or thermal growth processes followed by deposition of an overlying gate electrode material and an optional hardmask layer (not shown). Conventional lithographic patterning and dry etching processes are then carried out to form the gate structures 12A and 12B.</p>

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Claim	Claim Language	Exemplary Disclosures in Additional References
		 <p style="text-align: center;">FIG. 1A</p>

Claim	Claim Language	Exemplary Disclosures in Additional References
1 [c]	the second MIS transistor includes a second gate insulating film formed on a second active region in the semiconductor substrate and a second gate electrode formed on the second gate insulating film,	<p>The following references disclose and/or render obvious a “the second MIS transistor includes a second gate insulating film formed on a second active region in the semiconductor substrate and a second gate electrode formed on the second gate insulating film,” as further described below.</p> <p><i>See, e.g., U.S. Pat. No. 6,787,421 to Gilmer et al. (“Gilmer”) at:</i></p> <p>[2:36-55] Referring now to FIGS. 1-4, a semiconductor device 10 is fabricated in accordance with one embodiment of the invention. Referring now to FIGS. 1-4, a semiconductor device 10 is fabricated in accordance with one embodiment of the invention. As shown in FIG. 1, semiconductor device 10 includes a Semiconductor Substrate 12 which in a preferred embodiment is a single crystal Silicon Substrate (also sometimes referred to as a wafer), but which can instead be formed from other Semiconductor Substrate materials. Within substrate 12, trench isolation regions 14, preferably shallow trench isolation regions, are formed in a</p>

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Claim	Claim Language	Exemplary Disclosures in Additional References
		<p>conventional manner for the purpose of electrically isolating different individual devices to be formed. After forming trench isolation regions 14, a first gate dielectric 16 is formed over substrate 12. First gate dielectric 16 is preferably silicon dioxide or silicon oxynitride, and is preferably formed by thermal oxidation in accordance with conventional practices. The thickness of gate dielectric 16 is determined by the particular device requirements for devices to be formed in I/O device region 24 as further explained below, but generally will be within a range of 30–50 Angstroms (3-5 nanometers).</p> <p>[2:56-3:6] After forming first gate dielectric 16, a (photo)resist mask 18 is formed over the substrate to mask off a portion of the first gate dielectric layer. AS shown in FIG. 1, Semiconductor device 10 includes two different device regions, namely a core device region 22 and an I/O device region 24. In operation, devices to be formed in core device region 22 require thinner gate dielectrics that operate at lower Voltages than, e.g., I/O devices to be formed in I/O device region 24 that can withstand higher Voltages required for I/O functions. Accordingly, resist mask 18 is formed to protect the portion of first gate dielectric 16 which will Serve, in part, as a gate dielectric for the higher Voltage I/O devices. Other dielectric materials may instead be used for first gate dielectric 16. Silicon dioxide and silicon oxynitride are attractive choices because of the industry's understanding of these materials, the ability to form high gate quality films, and because they can be formed by Selective growth techniques rather than requiring blanket depositions and etch steps.</p> <p>[3:7-33] Semiconductor device 10 is then etched to remove unprotected portions of first gate dielectric 16 in core device region 22, as shown in FIG. 2. The resist mask 18 is then removed and a Second gate dielectric 20 is formed on exposed portions of Substrate 12 within the core device region 22. In a preferred embodiment, second gate dielectric 20 is also silicon dioxide or silicon oxynitride, but like first gate dielectric 16 other materials could be used. This Second gate dielectric can be formed by thermal oxidation and/or chemical oxidation in accordance with conventional practices. The thickness of gate dielectric 20 is also determined by the particular device requirements for devices to be formed in core device region 22 as further explained below, but generally will be within a range of 4-12 Angstroms (0.4-1.2 nanometers). Because Second gate dielectric 20 is So thin, it may be difficult to adequately control the thickness or obtain an oxide of Sufficient quality using thermal oxidation</p>

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Claim	Claim Language	Exemplary Disclosures in Additional References
		<p>processes and therefore chemical oxidation may be useful. For instance, the thin dielectric may be formed by growing a thin oxide by rinsing the substrate in ozonated water. A combination of thermal and chemical treatment may also be used to form second dielectric 20. It may also be sufficient for second gate dielectric 20 to be a native oxide which is grown on Substrate 12 as a result of exposing the Substrate to ambient or other oxygen containing environment. In other embodiments, second gate dielectric 20 can be deposited, e.g., by atomic layer deposition.</p> <p>[3:34-43] In the course of forming Second gate dielectric 20, the thickness of first gate dielectric 16 may change, depending on the technique used to form the Second gate dielectric 20, and should be taken into account in choosing the initial deposited or grown thickness of first gate dielectric 16. Generally, however, it is not anticipated that the thickness of first gate dielectric 16 will change Significantly unless second gate dielectric 20 is deposited over first gate dielectric 16 rather than forming it through a thermal or chemical reaction of the Substrate Surface.</p> <p>[3:44-4:7] Now that gate dielectrics of two different thicknesses have been formed, a high-k dielectric (generally with $k > 4$, preferably with $k > 6$, and most preferably with $k > 7$) is deposited over semiconductor device 10. In a preferred embodiment, this high-k dielectric is a metal oxide, Such as metal oxide 26 shown in FIG. 3. Suitable materials for metal oxide 26 preferably include hafnium oxide (HfO_2), hafnium silicate (HfSiO_2), or lanthanum aluminate (LaAlO_3), but lanthanum oxide, hafnium aluminate, Zirconium oxide, and Zirconium Silicate, and other like materials, may also be Suitable high-k dielectrics. The thickness of the high-k dielectric layer will be dependent on the particular device requirements in each region of the Substrate (the core region and the I/O region), but generally it is believed the thickness of a metal oxide will be between about 15-50 angstroms (1.5-5.0 nanometers). The underlying thicknesses of first gate dielectric 16 and Second gate dielectric 20 will also affect the choice of thickness of the high-k dielectric. The thickness of the high-k dielectric should be chosen So that its equivalent oxide thickness (EOT), when added to the EOT of the first gate dielectric 16 (I/O device dielectric) thickness or Second gate dielectric 20 (core device dielectric) thickness, provides a total EOT appropriate for the I/O and core device, respectively. Similarly, this calculation should be used to determine the initial</p>

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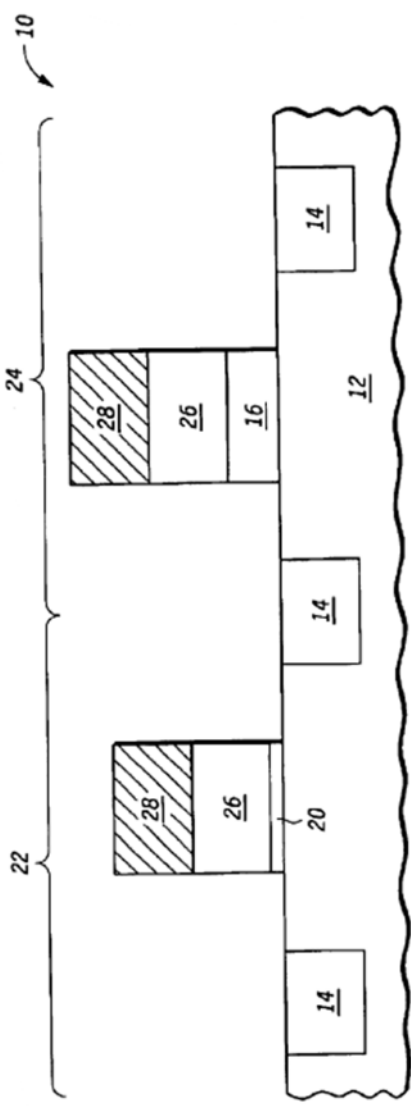
Claim	Claim Language	Exemplary Disclosures in Additional References
		<p>deposited or grown thicknesses of the first and Second gate dielectrics. Because metal oxide 26 is deposited as a single blanket deposition, its thickness will not vary much across the Substrate Surface and thus one should use the thicknesses of the first and Second dielectrics as the “variables” to achieve the final EOTs for the core and I/O devices.</p>  <p><i>FIG. 4</i></p>
		<p>See, e.g., Japanese Patent App. Pub. No. JP2006/060155 to Yasuhira et al. (“Yasuhira”) at:</p> <p>According to the present invention, gate insulating films having different electrical thicknesses using a High-k film for reducing gate leakage current of a MISFET constituting a semiconductor device can be formed on the same semiconductor substrate with high reproducibility. Accurate and simple formation.</p> <p>Hereinafter, some of the embodiments of the present invention will be described in detail with reference to the drawings.</p> <p>(Embodiment 1)</p> <p>FIG. 1 is a cross-sectional view of the main part of the semiconductor device according to the first embodiment of the present invention, and FIGS. Here, a technology generation in which</p>

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Claim	Claim Language	Exemplary Disclosures in Additional References
		<p>the design standard of the semiconductor element is 65 nm to 45 nm is shown. In this generation, a MISFET that operates at a voltage of 1 V or less is formed in the internal circuit of the semiconductor device, and the thickness of the gate insulating film is about 1.2 nm or less in terms of a silicon oxide film. A peripheral circuit of the semiconductor device, for example, an input / output circuit, is formed with a MISFET operating at a (power supply) voltage of 1.5 V to 3.3 V, and the thickness of the gate insulating film is 3 nm to 6 nm in terms of silicon oxide film. It will be about. Here, since the peripheral circuit differs greatly depending on the semiconductor device, there is a range in the usage range of the driving voltage and the film thickness of the gate insulating film.</p> <p>In the following description, a p-channel type MISFET will be described, but an n-channel type MISFET is formed in the same manner. As shown in FIG. 1, for example, at least two types of MISFETs having gate insulating films having different equivalent film thicknesses in a region corresponding to a peripheral circuit portion on a p-conductivity type silicon substrate 1 and a region corresponding to an internal circuit portion are provided. It is formed.</p> <p>That is, an n well layer 2 is formed on the surface portion of the silicon substrate 1, and the surface portion of the n well layer 2 is partitioned by an element isolation region 3 by STI. In the MISFET in the peripheral circuit portion, the base oxide film 4 having a thickness of 4 to 6 nm and the nitride layer 4a whose surface is modified to a nitrogen-containing layer, the High-k film 5 and the surface thereof are modified to a nitrogen-containing layer. A first gate insulating film 6 made of a laminated film of the nitrided layer 5a is formed. Then, a gate electrode 9 is constituted by the polycrystalline silicon layer 7 containing the p-conductivity type or n-conductivity type impurity formed on the first gate insulating film 6 and the silicide layer 8, and the first gate insulating film 6. A sidewall insulating film 10 is provided on the side wall of the gate electrode 9. Here, the base oxide film 4 is formed of a silicon oxide film, and the high-k film 5 is formed of hafnia (HfO₂), zirconia (ZrO₂), hafnium silicate (HfSiOx), zirconium silicate (ZrSiOx), hafnium aluminate (An insulating film having a thickness of 2 to 3 nm made of HfAlOx) or zirconium aluminate (ZrAlOx) is preferable. Alternatively, the High-k film 5 may be configured by an insulating film having a stacked structure in which two or more types of insulating films are selected from the high dielectric</p>

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Claim	Claim Language	Exemplary Disclosures in Additional References
		<p>constant insulating films and stacked. A source / drain region including a source / drain diffusion layer 11 and a silicide layer 8 is provided on the surface of the n well layer 2.</p> <p>Next, a method for manufacturing the semiconductor device according to the present invention will be described with reference to FIGS. Here, the same components as those in FIG. 1 are denoted by the same reference numerals.</p> <p>An n-well layer 2 is formed on the surface portion of the p-conductivity type silicon substrate 1, an STI element isolation region 3 is formed on the surface portion of the n-well layer 2, and a base oxide film 4 of about 5 nm is formed on the surface of the silicon substrate 1. It is formed by thermal oxidation. (FIG. 2 (a))</p>

Claim		<p>【図 1】</p>
Claim Language		
Exemplary Disclosures in Additional References		<p>See, e.g., Japanese Patent App. Pub. No. JP2003/100896 to Fujiwara et al. (“Fujiwara”) at:</p> <p>A semiconductor device according to the present invention comprises a semiconductor substrate and a first substrate divided into the semiconductor substrate</p>

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Claim	Claim Language	Exemplary Disclosures in Additional References
		<p>A first transistor having a first gate insulating film having a structure in which a first insulating film and a second insulating film are stacked in this order from the semiconductor substrate, and are divided into the semiconductor substrate. The third insulating film and the fourth insulating film formed in the second region are stacked in this order from the semiconductor substrate, and the silicon oxide film is formed as compared with the first gate insulating film. A second transistor having a second gate insulating film having a large converted film thickness, and the second and fourth transistors.</p> <p>The insulating film of is a high-dielectric film formed at the same time.</p> <p>And the third insulating film are interface layers having different compositions or film thicknesses from each other. Particularly preferably, the first and third insulating films are interface layers having different compositions from each other formed by the reaction between the second and third insulating films and the semiconductor substrate or the thin film formed on the surface thereof. I shall.</p> <p>The present invention is also a method of manufacturing a semiconductor device including transistors having different gate insulating film structures, which comprises selectively forming an oxygen barrier layer on the surface of the first region of the semiconductor substrate, A high dielectric insulating film is formed on the semiconductor substrate, the first region includes the oxygen barrier layer or an interface layer formed of a reaction layer between the oxygen barrier layer and the high dielectric film, and the second region includes the semiconductor. It is characterized by including a step of forming a gate insulating film including an interface layer by a reaction between a substrate and the high dielectric film, and a step of patterning a gate electrode on the gate insulating film.</p> <p>In the present invention, the high dielectric film (metal oxide or its silicate) as the gate insulating film is formed, or is formed on the substrate during the subsequent crystallization annealing. The interface layer formed between the thin film and the thin film has different characteristics and structure by controlling the electrical film thickness and film quality of the interface layer by introducing nitrogen into the substrate surface or inserting a thin film nitride</p>

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Claim	Claim Language	Exemplary Disclosures in Additional References
		<p>film. A gate insulating film is formed on the same substrate. In other words, by treating the interface layer that was previously integrated with the high-k dielectric film as a laminated structure with independent functions, by forming a high-k dielectric film with a sufficient thickness to suppress direct tunneling. By suppressing the gate leakage current and making the state of the substrate interface different depending on the transistor region, the gate insulating film can be selectively used for each transistor which requires different specifications.</p> <p>Next, a sacrificial oxide film 61 is formed by dilute hydrofluoric acid treatment. Was removed, after performing the hydrogen-terminated silicon substrate 51 surface, as shown in FIG. 8, TiO 2 is a high dielectric film</p> <p>The film 81 is formed. Specifically, the TiO 2 film 81 having a thickness of 5 nm is formed by the DC sputtering method using a TiO 2 sintered target under the sputtering conditions of power 300 W, pressure 1 Pa, Ar / O 2 flow rate 22 / 1.2 sccm. . At this time, the surface of the silicon substrate in the regions A and B is oxidized by the oxygen plasma atmosphere during the sputtering of the TiO 2 film, and the interface layers 82 and 83 are formed. The interface layer 82 in the region A has the result that the nitrogen introduction region 64 suppresses the diffusion of oxygen into the substrate.</p> <p>It becomes a thin silicon oxide film, and the interface layer 83 in the region B becomes a thicker silicon oxide film.</p> <p>A polycrystalline silicon film having a thickness of 175 n is formed on the upper surface by a CVD method.</p> <p>A gate electrode 91 is formed by forming a film and performing patterning. Along with the gate electrode 91, the TiO 2 film 81 and the interface layers 82 and 83 which will be the gate insulating film thereunder are also patterned. After that, in order to crystallize the TiO 2 film 81, RTA with a heat treatment temperature of 900 ° C. and a heat treatment time of 30 seconds is performed.</p> <p>Do. At this time, the surface of the silicon substrate in the region B is oxidized by the diffusion of oxygen from the TiO 2 film 81 to the silicon substrate 51 by RTA, and the interface layer 83 grows to finally become the interface layer 83a of about 2 nm. In the region A, the nitrogen</p>

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Claim	Claim Language	Exemplary Disclosures in Additional References
		<p>introduction region 64 suppresses the diffusion of oxygen into the substrate, The growth of the interface layer 82 is suppressed, and finally about 0.7 The interface layer 82a has a thickness of nm.</p> <p>The TiO 2 film 81 becomes a microcrystalline state by the RTA treatment, and its dielectric constant is about 20. Therefore, the equivalent oxide film thickness of this portion is about 1 nm. Also, Ti.</p> <p>By the physical mixing of Ti into the substrate by sputtering of the O 2 film 81 and the activation annealing performed in a later step, the interface layers 82a and 83a become silicon oxide films containing a trace amount of Ti, and their dielectric constant is 5 It will be about.</p> <p>Therefore, the gate insulating film in the region A has a laminated structure of the interface layer 82a and the TiO 2 film 81, and the gate insulating film in the region B has a laminated structure of the interface layer 83a and the TiO 2 film 81. These gate insulating films have a physical film thickness of 5 nm or more, and can sufficiently suppress the direct tunneling current. On the other hand, due to the difference in the film thickness of the interface layers 82a and 83b, in the region A, the oxide film equivalent film thickness is 1.6n.</p> <p>In the region B, the gate insulating film of m has an oxide film equivalent thickness of 2.6. Thus, the gate insulating film having a thickness of nm is formed.</p> <p>Next, as shown in FIG. 10, N-type impurities are ion-implanted substantially perpendicularly to the silicon single crystal substrate 51 to form shallow source / drain n-type diffusion layers 101. Specifically, for example, arsenic is accelerated at an acceleration voltage of 5 keV to 10 k. eV, dose amount $5 \times 10^{14} / \text{cm}^2$ to $1 \times 10^{15} / \text{cm}^2$ Inject.</p> <p>As described above, according to this embodiment, the transistors Q1 and Q2 formed in the regions A and B are formed.</p>

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Claim	Claim Language	Exemplary Disclosures in Additional References
		<p>Are formed of gate insulating films having different physical thicknesses of silicon oxide, while having a physical film thickness sufficient to suppress the direct tunneling current. Due to the difference in the gate insulating film structure, the transistor Q1 in the region A is relatively inferior in gate breakdown voltage and reliability to the transistor Q2 in the region B, but has a characteristic difference in high current driving capability.</p> <p>The gate insulating film has a laminated structure of a high dielectric film and an interface layer formed as a reaction layer between the high dielectric film and the substrate. By changing it, the interface layers of both are different. Moreover, the processing for changing the substrate surface state can be performed using the mask for channel ion implantation in the regions A and B as it is. Therefore, although the transistors Q1 and Q2 have different types of gate insulating film structures, the manufacturing process is simple, with only one additional ion implantation step.</p>

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Claim		Exemplary Disclosures in Additional References
Claim Language		<p style="text-align: center;">【 図 1 1 】</p> <p>See, e.g., U.S. Pat. No. 8,349,695 to Scheiper et al. (“Scheiper”) at: 4:27-36: FIG. 1b schematically illustrates the semiconductor device 100 in a further advanced manufacturing phase in which the etch mask 103 is removed and the device 100 is exposed to a cleaning ambient 105 in order to remove contaminants and also to re-grow a thin dielectric base layer 152 on the semiconductor region 102A. For this purpose, a plurality of well established process techniques are available in order to obtain a silicon dioxide material on the basis of a well-controllable growth process.</p>

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Claim	Claim Language	Exemplary Disclosures in Additional References
		<p>4:37-56: FIG.1c schematically illustrates the semiconductor device 100 when exposed to a deposition ambient 106 in which a high-k dielectric material. Such as hafnium oxide, is deposited above the active regions 102A, 102B, thereby forming a high-k dielectric layer 153. Thus, the layers 152 and 153 in combination may represent the gate dielectric material of a transistor formed in and above the semiconductor region 102A, thereby providing the required characteristics for high performance transistors, while the layer 153 in combination with the “thick” silicon dioxide material 151 represents the dielectric material for transistors and other circuit elements in which a Superior performance with respect to reduced leakage currents and the like is required. It should be appreciated that the deposition process 106 may be performed on the basis of any appropriate deposition recipe, for instance, by chemical vapor deposition (CVD), physical vapor deposition (PVD) and the like. For example, a thickness of the high-k dielectric layer 153 may be in the range of one to several nanometers, depending on the overall requirements in view of capacitive coupling, leakage currents and the like.</p>

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Claim	Claim Language	Exemplary Disclosures in Additional References
		<p>FIG. 1g (prior art)</p>
		<p>See, e.g., U.S. Pat. No. 7,335,561 to Sakai ("Sakai '561") at:</p> <p>[2:31-53] The typical ones of the inventions disclosed in this application will be briefly described as follows. A semiconductor integrated circuit device of the present invention comprising: a semiconductor Substrate; a first MIS transistor including a pair of first semiconductor regions formed in the semiconductor substrate and a first conductive piece formed above the semiconductor Substrate through a first gate insulation film in a region between the pair of the first semiconductor regions; and a second MIS transistor including a pair of second semiconductor regions formed in the semiconductor Substrate and a second conductive piece formed above the semiconductor Substrate through a second gate insulation film in a region between the pair of the second semiconductor regions, wherein the thickness of the second gate insulation film is greater than the thickness of the first gate insulation film.</p>

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Claim	Claim Language	Exemplary Disclosures in Additional References
		<p>of the first gate insulation film is larger than the thickness of the second gate insulation film and the first gate insulation film is comprised of the first insulation film located on the semiconductor Substrate and the second insulation film located on the first insulation film; and wherein the second gate insulation film is comprised of a third insulation film located on the semiconductor substrate and the dielectric constant of the second and third insulation films is larger than the dielectric constant of the first insulation film.</p> <p>[5:19-22] FIG. 35 is a major part sectional view of a semiconductor substrate showing an example of the manufacturing method of a semiconductor integrated circuit according to an embodiment of the present invention in the order of steps;</p> <p>[6:1-18] An example of the manufacturing method for the semiconductor integrated circuit device according to an embodiment of the present invention will be described using major part sectional views of the semiconductor Substrate shown in FIGS. 1-40. In the Figures, a region A indicates a region in which a gate insulation film having a larger effective thickness is formed and the region B indicates a region in which a gate insulation film having a smaller effective thickness is formed. In the regions A, B, n-channel MIS transistor (hereinafter referred to as low V_{th} NMOS) having a low threshold value voltage (hereinafter referred to as V_{th}), p-channel MIS transistor (hereinafter referred to as low V_{th} PMOS) having a low V_{th}, n-channel MIS transistor (hereinafter referred to as high V_{th} NMOS) having a high V_{th} and p-channel MIS transistor (hereinafter referred to as high V_{th} PMOS) having a high V_{th} are formed and that is, eight kinds of the MIS transistors are formed on the same substrate.</p> <p>[7:60-8:4] Next, after the resist pattern RP10 is removed, as shown in FIG. 16, the protective film 5 is removed and the silicon oxide film 9 is formed on the surface of the semiconductor substrate 1, for example, in the thickness of 4 to 5 nm. The silicon oxide film 9 can be formed according to the thermal CVD method or thermal oxidation method. Meanwhile, the aforementioned silicon oxide film may be turned to silicon nitride film by nitriding the semiconductor substrate 1 thermally. The aforementioned thermal nitration is carried out with the semiconductor 1 heated at about 900° C. in a pressure reduced atmosphere containing nitrogen made radical by plasma discharge</p>

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Claim	Claim Language	Exemplary Disclosures in Additional References
		<p>[8:5-10] Next, as shown in FIG. 17, after the region A is covered with the resist pattern RP1, as shown in FIG. 18, the silicon oxide film 9 in the region B is removed using diluted HF with resist pattern RP11 as a mask. After that, as shown in FIG. 19, the resist pattern RP11 is removed.</p> <p>[8:11-26] Next, as shown in FIG. 20, high dielectric constant insulation film 10, for example, alumina film is formed on the semiconductor substrate 1. The high dielectric constant insulation film 10 can be deposited according to, for example, sputtering method. The thickness of the high dielectric constant insulation film 10 formed on the semiconductor substrate 1 is set so that its effective thickness is about 5 nm. For example, the alumina film is deposited in the thickness of about 10 nm considering dielectric constant. Consequently, gate insulation film 11 comprised of the high dielectric constant insulation film 10 about 5 nm in terms of its effective thickness is formed in the region B and gate insulation film 12 comprised of stacked film of the high dielectric constant film 10 and the silicon oxide film 9 about 9 to 10 nm in terms of its effective thickness is formed in the region A</p> <p>[8:27-31] Before forming the aforementioned high dielectric constant insulation film 10 on the semiconductor substrate 1, silicon oxide film or silicon nitride film, or silicon oxide nitride film less than 1 nm or less may be formed to stabilize an interface with the semiconductor substrate 1.</p> <p>[8:32-34] Next, as shown in FIG. 21, silicon film 13 about 200 nm. thick is deposited on the semiconductor Substrate 1 according to the CVD method.</p> <p>[8:35-39] Next, as shown in FIG.22, after resist pattern 12 is formed in the NMOS formation region in the regions A, B, p-type impurity, for example, boron is ion-implanted into the silicon film 13 in the PMOS formation region in the regions A, B with this resist pattern RP12 as a mask.</p> <p>[8:40-46] Next, the resist pattern 12 is removed and as shown in FIG. 23, resist pattern RP13 is formed in the PMOS formation region in the regions A, B. After that, n-type impurity, for</p>

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Claim	Claim Language	Exemplary Disclosures in Additional References
		<p>example, phosphorus is ion-implanted into the NMOS formation region in the regions A, B with this resist pattern RP13 as a mask.</p> <p>[8:47-55] Next, after the resist pattern RP13 is removed, by per forming heat treatment on the semiconductor Substrate 1, for example at 950° C. for about 60 seconds, the aforementioned n-type impurity and p-type impurity implanted into the silicon film 13 are activated. Further, the silicon film 13 in the NMOS formation region in the regions A, B is turned to n-type silicon polycrystal film and the silicon film 13 in the PMOS formation region in the regions A, B is changed to p-type silicon polycrystal film.</p> <p>[8:56-60] After as shown in FIG. 24, silicon oxide film 14 is deposited on the semiconductor Substrate 1 according to the CVD method, as shown in FIG. 25, resist pattern RP14 is formed to form gate electrodes of the n-channel and p-channel MIS transistor.</p> <p>[8:61-9:3] Next, after as shown in FIG. 26, the silicon oxide film 14 is etched with the resist pattern RP14 as a mask, the resist pattern RP14 is removed. Subsequently, as shown in FIG. 27, with the patterned silicon oxide film 14 as a mask, the silicon film 13 is etched so as to form a gate electrode (conductive piece) 15n comprised of n-type silicon poly crystal film in the NMOS formation region in the regions A, B and a gate electrode (conductive piece) comprised of p-type silicon polycrystal film in the PMOS formation region in the regions A, B</p>

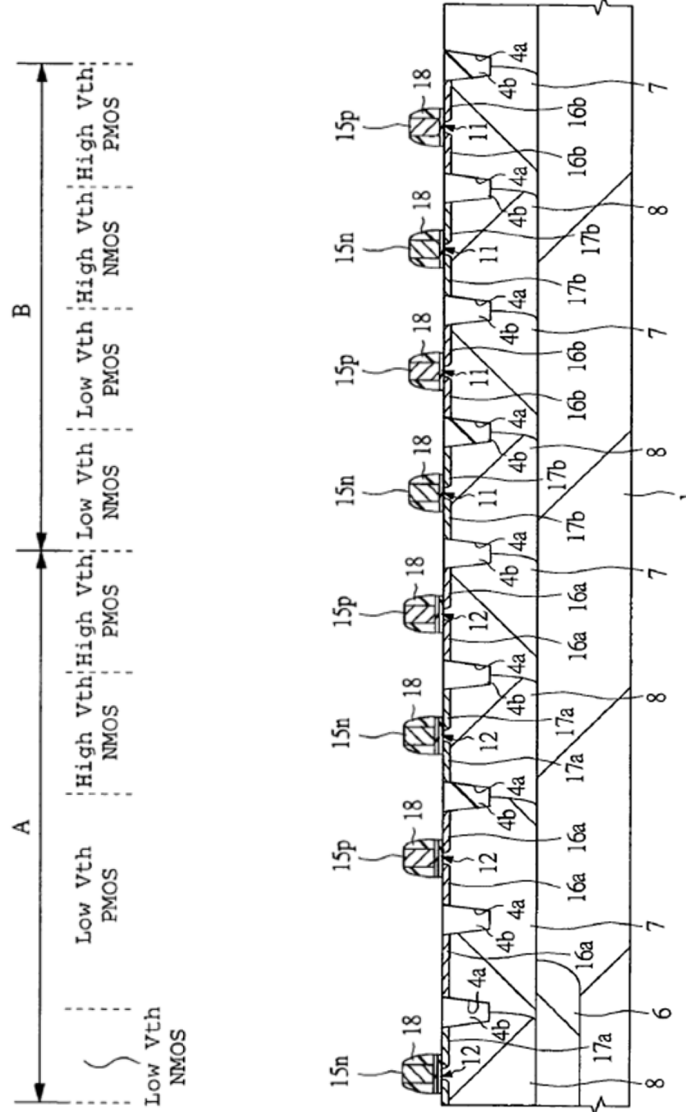
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Claim Language

Claim

FIG. 35



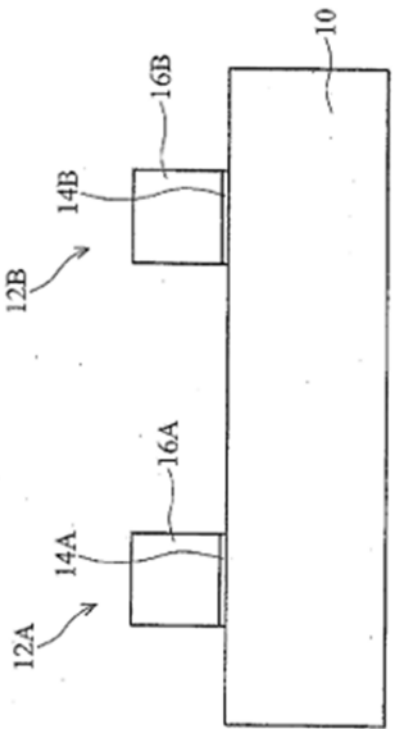
See, e.g., U.S. Pat. App. Pub. No. 2009/0039445 to Wu ("Wu '445") at:

[0017] Referring to FIG. 1A, in an exemplary implementation of the present invention, is shown a semiconductor substrate 10 having overlying gate structures 12A and 12B including respective gate dielectric portions 14A and 14B and respective overlying gate electrode portions 16A and 16B. Gate dielectric portions and overlying gate electrode portions of gate structures 12A and 12B may be formed by conventional deposition, lithographic and etching processes. The semiconductor substrate 10, may include, but is not limited to, silicon, silicon on insulator (SOI) stacked SOI (SSOI), stacked SiGe on insulator (S—SiGeOI), SiGeOI, and

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Claim	Claim Language	Exemplary Disclosures in Additional References
		<p>GeOI, or combinations thereof. It will be appreciated that an electrical isolation structure such as a shallow trench isolation (STI) structure (not shown) may be provided between gate structures 12A and 12B to isolate the respective MOSFET devices.</p> <p>[0018] Still referring to FIG. 1A, the gate structures 12A and 12B may be formed by conventional CVD deposition, lithographic patterning, and plasma (dry) etching methods known in the art. The gate dielectric portions 14A and 14B may be formed by any process known in the art, e.g., thermal oxidation, nitridation, sputter deposition, chemical vapor deposition, or combinations thereof. The gate dielectric portions 14A and 14B may be formed of silicon oxide, silicon nitride, silicon oxynitride, and high-K dielectrics (e.g., K>8) including transition metal oxide and rare earth metal oxides. For example, high-K dielectrics may be formed of aluminum oxides (e.g., Al₂O₃), hafnium oxides (e.g., HfO₂), hafnium oxynitrides (HfON), hafnium silicates (e.g. HfSiO₄), hafnium silicon oxynitrides (e.g., HfSi₆O₅N₂), zirconium oxides (e.g., ZrO₂), zirconium oxynitrides (e.g., ZrON), zirconium silicon oxides (e.g., ZrSiO₂), yttrium oxides (Y₂O₃), lanthanum oxides (La₂O₃), cerium oxides (CeO₂), titanium oxides (TiO₂), tantalum oxides (Ta₂O₅), or combinations thereof. The high-k dielectric layer may be formed by known CVD methods such as atomic layer CVD (ALCVD) and metal-organic CVD (MOCVD). It will be appreciated that the high-K dielectric layer may include a lowermost interfacial layer formed on the semiconductor substrate such as an oxide or oxynitride (not shown).</p> <p>[0019] The gate electrode portions, 16A and 16B may be formed of poly gate such as polysilicon, amorphous polysilicon, doped polysilicon, polysilicon-germanium, or metal gate such as TaC, TaN, TiN, MoN or combinations thereof). For example, a gate dielectric layer is first formed by CVD, sputtering or thermal growth processes followed by deposition of an overlying gate electrode material and an optional hardmask layer (not shown). Conventional lithographic patterning and dry etching processes are then carried out to form the gate structures 12A and 12B.</p>

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Claim	Claim Language	Exemplary Disclosures in Additional References
		 <p style="text-align: center;">FIG. 1A</p> <p style="text-align: right;">See 1 [b]</p>

Claim	Claim Language	Exemplary Disclosures in Additional References
1 [d]	the first gate insulating film includes a first interface layer being in contact with the semiconductor substrate and a first high dielectric constant insulating film formed on the first interface layer,	<p>The following references disclose and/or render obvious a “the first gate insulating film includes a first interface layer being in contact with the semiconductor substrate and a first high dielectric constant insulating film formed on the first interface layer,” as further described below.</p> <p><i>See, e.g., U.S. Pat. No. 6,787,421 to Gilmer et al. (“Gilmer”) at:</i></p> <p>[2:36-55] Referring now to FIGS. 1-4, a semiconductor device 10 is fabricated in accordance with one embodiment of the invention. Referring now to FIGS. 1-4, a semiconductor device 10 is fabricated in accordance with one embodiment of the invention. As shown in FIG. 1, semiconductor device 10 includes a Semiconductor Substrate 12 which in a preferred embodiment is a single crystal Silicon Substrate (also sometimes referred to as a wafer), but which can instead be formed from other Semiconductor Substrate materials. Within substrate 12, trench isolation regions 14, preferably shallow trench isolation regions, are formed in a conventional manner for the purpose of electrically isolating</p>

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Claim	Claim Language	Exemplary Disclosures in Additional References
		<p>different individual devices to be formed. After forming trench isolation regions 14, a first gate dielectric 16 is formed over substrate 12. First gate dielectric 16 is preferably silicon dioxide or silicon oxynitride, and is preferably formed by thermal oxidation in accordance with conventional practices. The thickness of gate dielectric 16 is determined by the particular device requirements for devices to be formed in I/O device region 24 as further explained below, but generally will be within a range of 30–50 Angstroms (3–5 nanometers).</p> <p>[2:56-3:6] After forming first gate dielectric 16, a (photo)resist mask 18 is formed over the substrate to mask off a portion of the first gate dielectric layer. AS shown in FIG. 1, Semiconductor device 10 includes two different device regions, namely a core device region 22 and an I/O device region 24. In operation, devices to be formed in core device region 22 require thinner gate dielectrics that operate at lower Voltages than, e.g., I/O devices to be formed in I/O device region 24 that can withstand higher Voltages required for I/O functions. Accordingly, resist mask 18 is formed to protect the portion of first gate dielectric 16 which will Serve, in part, as a gate dielectric for the higher Voltage I/O devices. Other dielectric materials may instead be used for first gate dielectric 16. Silicon dioxide and silicon oxynitride are attractive choices because of the industry's understanding of these materials, the ability to form high gate quality films, and because they can be formed by Selective growth techniques rather than requiring blanket depositions and etch steps.</p> <p>[3:44-4:7] Now that gate dielectrics of two different thicknesses have been formed, a high-k dielectric (generally with $k > 4$, preferably with $k > 6$, and most preferably with $k > 7$) is deposited over semiconductor device 10. In a preferred embodiment, this high-k dielectric is a metal oxide. Such as metal oxide 26 shown in FIG. 3. Suitable materials for metal oxide 26 preferably include hafnium oxide (HfO₂), hafnium silicate (HfSiO₂), or lanthanum aluminate (LaAlO₃), but lanthanum oxide, hafnium aluminate, Zirconium oxide, and Zirconium Silicate, and other like materials, may also be Suitable high-k dielectrics. The thickness of the high-k dielectric layer will be dependent on the particular device requirements in each region of the Substrate (the core region and the I/O region), but generally it is believed the thickness of a metal oxide will be between about 15–50 angstroms (1.5–5.0 nanometers). The underlying thicknesses of first gate dielectric 16 and Second gate dielectric 20 will also affect the choice of thickness of the high-k dielectric. The thickness of the high-k dielectric should be chosen So that its equivalent oxide thickness (EOT), when added to the EOT of the first gate dielectric 16 (I/O device dielectric) thickness or Second gate dielectric 20 (core device dielectric) thickness, provides a</p>

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Claim	Claim Language	Exemplary Disclosures in Additional References
		<p>total EOT appropriate for the I/O and core device, respectively. Similarly, this calculation should be used to determine the initial deposited or grown thicknesses of the first and Second gate dielectrics. Because metal oxide 26 is deposited as a single blanket deposition, its thickness will not vary much across the Substrate Surface and thus one should use the thicknesses of the first and Second dielectrics as the “variables” to achieve the final EOTs for the core and I/O devices.</p> <p style="text-align: center;">FIG. 4</p> <p>See, e.g., Japanese Patent App. Pub. No. JP2006/060155 to Yasuhira et al. (“Yasuhira”) at: Hereinafter, some of the embodiments of the present invention will be described in detail with reference to the drawings. (Embodiment 1)</p> <p>FIG. 1 is a cross-sectional view of the main part of the semiconductor device according to the first embodiment of the present invention, and FIGS. Here, a technology generation in which the design standard of the semiconductor element is 65 nm to 45 nm is shown. In this generation, a MISFET that operates at a voltage of 1 V or less is formed in the internal circuit of the semiconductor device, and the thickness of the gate insulating film is about 1.2 nm or less in terms of a silicon oxide film. A peripheral circuit of the semiconductor device, for example, an input / output circuit, is formed with a MISFET</p>

Claim	Claim Language	Exemplary Disclosures in Additional References
		<p>operating at a (power supply) voltage of 1.5 V to 3.3 V, and the thickness of the gate insulating film is 3 nm to 6 nm in terms of silicon oxide film. It will be about. Here, since the peripheral circuit differs greatly depending on the semiconductor device, there is a range in the usage range of the driving voltage and the film thickness of the gate insulating film.</p> <p>In the following description, a p-channel type MISFET will be described, but an n-channel type MISFET is formed in the same manner. As shown in FIG. 1, for example, at least two types of MISFETs having gate insulating films having different equivalent film thicknesses in a region corresponding to a peripheral circuit portion on a p-conductivity type silicon substrate 1 and a region corresponding to an internal circuit portion are provided. It is formed.</p> <p>That is, an n well layer 2 is formed on the surface portion of the silicon substrate 1, and the surface portion of the n well layer 2 is partitioned by an element isolation region 3 by STI. In the MISFET in the peripheral circuit portion, the base oxide film 4 having a thickness of 4 to 6 nm and the nitride layer 4a whose surface is modified to a nitrogen-containing layer, the High-k film 5 and the surface thereof are modified to a nitrogen-containing layer. A first gate insulating film 6 made of a laminated film of the nitrided layer 5a is formed. Then, a gate electrode 9 is constituted by the polycrystalline silicon layer 7 containing the p-conductivity type or n-conductivity type impurity formed on the first gate insulating film 6 and the silicide layer 8, and the first gate insulating film 6. A sidewall insulating film 10 is provided on the side wall of the gate electrode 9. Here, the base oxide film 4 is formed of a silicon oxide film, and the high-k film 5 is formed of hafnia (HfO₂), zirconia (ZrO₂), hafnium silicate (HfSiOx), zirconium silicate (ZrSiOx), hafnium aluminate (An insulating film having a thickness of 2 to 3 nm made of HfAlOx) or zirconium aluminate (ZrAlOx) is preferable. Alternatively, the High-k film 5 may be configured by an insulating film having a stacked structure in which two or more types of insulating films are selected from the high dielectric constant insulating films and stacked. A source / drain region including a source / drain diffusion layer 11 and a silicide layer 8 is provided on the surface of the n well layer 2.</p> <p>On the other hand, in the MISFET of the internal circuit portion, the base film 12 with a film thickness of about 1 nm and the nitride layer 12a whose surface is modified to a nitrogen-containing layer, the High-k film 5 and the nitride layer which is a modified layer on the surface thereof A second gate insulating film 13 is formed by the laminated film 5 a, and the above-described polycrystalline silicon</p>

Claim	Claim Language	Exemplary Disclosures in Additional References
		<p>layer 7 and silicide layer 8 are provided on the second gate insulating film 13. Sidewall insulating films 10 are provided on the side walls of the second gate insulating film 13 and the gate electrode 9, and source / drain regions including the source / drain diffusion layers 11 and the silicide layers 8 are provided on the surface of the n-well layer 2. It has been. In the second gate insulating film 13 of the MISFET, the base film 12 has a silicon oxide film structure as a basic structure, and is interposed between the high-k film 5 and the silicon substrate 1 on the surface of the n-well layer 2. It has functions such as preventing boron penetration and improving the surface mobility of carrier charges (holes).</p> <p>Next, a method for manufacturing the semiconductor device according to the present invention will be described with reference to FIGS. Here, the same components as those in FIG. 1 are denoted by the same reference numerals.</p> <p>Next, the surfaces of the base oxide film 4 and the base film 12 are nitrided by plasma nitriding, and the silicon oxide film surfaces are modified to form nitride layers 4a and 12a as nitrogen-containing layers (FIG. 2D). . In this plasma nitriding method, N₂ gas, N₂O, NO, N₂H₂ and NH₃ gas, which are raw material gases, are excited by plasma in ECR (Electron Cyclotron Resonance), ICP (Inductively Coupled Plasma), (magnetron type)) Active species of nitrogen are generated by excitation with RF plasma or helicon wave plasma, and the active species are exposed to the surface of the silicon oxide film. The active species include nitrogen atom ions, molecular ions, neutral radicals, and the like. Here, it is preferable that only the nitrogen neutral radicals are extracted from the active species to form the nitride layers 4a and 12a. For example, among the active species of nitrogen formed in the plasma excitation chamber, neutral radicals having a relatively long lifetime are extracted by the downflow method, and the neutral oxides are irradiated onto the surface of the base oxide film 4 and the base film 12. In this manner, the nitride layers 4a and 12a are preferably formed by the reaction between neutral radicals and the surface of the silicon oxide film.</p> <p>In the plasma nitriding method using nitrogen neutral radicals, the nitrogen active species and the depth of the nitride layer in the nitride layers 4a and 12a to be formed are limited because the active species of nitrogen are controlled to one kind. It becomes possible to control with high accuracy. Further, this method is a so-called remote plasma method, and since the ion irradiation or plasma emission irradiation can be prevented, irradiation damage in the base oxide film 4 and the base film 12 is greatly reduced, and a high-quality gate insulating film is obtained. Can be secured.</p>

Claim	Claim Language	Exemplary Disclosures in Additional References
		<p>Here, when the active species is generated by plasma excitation of a source gas containing hydrogen such as N₂ H₂ or NH₃ gas, a large amount of hydrogen is mixed into the nitride layer and the silicon oxide film to deteriorate the film quality. . Therefore, in this case, it is preferable to desorb hydrogen in the film by performing a heat treatment in an inert gas after the plasma nitridation.</p> <p>In the plasma nitriding method described above, the amount or depth of nitrogen introduced into the base oxide film 4 and the base film 12 can be easily controlled by the plasma processing conditions or processing time such as the power power of plasma excitation. FIG. 4 shows an example of nitrogen distribution in the nitride layer 12a. Here, the plasma nitridation was performed by irradiating the surface of the underlayer 12 with nitrogen neutral radicals in a downflow manner by exciting the N₂ gas with ECR. FIG. 4 is a nitrogen distribution diagram obtained by XPS (X-ray Photoelectron Spectroscopy) analysis of the nitride layer 12a. As can be seen from FIG. 4, the nitrogen concentration on the surface of the nitride layer 12a is 15 at. % To 20 at. The nitrogen concentration decreases as the depth from the surface decreases, and nitrogen does not exist in a region deeper than 1 nm. Therefore, there is almost no nitrogen at the interface between the base film 12 and the n-well layer 2.</p> <p>Next, a High-k film 5 is deposited on the entire surface so as to cover the base oxide film 4 and the base film 12. As the High-k film 5, for example, a thin film of HfAlOx, HfSiOx or HfO₂ having a relative dielectric constant of 10 to 20 is formed. It is preferable to use an ALD (Atomic Layer Deposition) method or an MOCVD (Metal Organic Chemical Vapor Deposition) method for the growth of such a High-k film. For example, when HfAlOx is formed as the high-k film by using the ALD method, the substrate temperature is 300 ° C., and hafnium tetrachloride (HfCl₄) and trimethylaluminum (TMA) are used as the film forming raw materials. A thin film of HfAlOx having a film thickness of 2 nm to 3 nm is formed using water vapor (H₂O) or ozone (O₃) as an oxidant (FIG. 3A). In the formation of the high-k film 5, the thin base film 12 prevents an interface reaction between the high-k film 5 and the silicon substrate 1 on the surface of the n-well layer 2.</p>

Claim	Claim Language	Exemplary Disclosures in Additional References
		<p>【図 1】</p> <p>内部回路部 周辺回路部</p> <p>The diagram is a cross-sectional view of a semiconductor device. It is divided into two main regions: the '内部回路部' (Internal Circuit Region) on the left and the '周辺回路部' (Peripheral Circuit Region) on the right, separated by a vertical dashed line. The internal circuit region contains two identical circuit blocks, each with a central core (12) surrounded by a ring (13). The peripheral circuit region contains a similar structure but with a different internal layout. Various layers and components are labeled with numbers: 1 (top layer), 2 (second layer), 3 (third layer), 4 (fourth layer), 5 (fifth layer), 6 (sixth layer), 7 (seventh layer), 8 (eighth layer), 9 (ninth layer), 10 (tenth layer), 11 (eleventh layer), 12 (twelfth layer), 13 (thirteenth layer), 14 (fourteenth layer), 15 (fifteenth layer), 16 (sixteenth layer), 17 (seventeenth layer), 18 (eighteenth layer), 19 (nineteenth layer), 20 (twentieth layer), 21 (twenty-first layer), 22 (twenty-second layer), 23 (twenty-third layer), 24 (twenty-fourth layer), 25 (twenty-fifth layer), 26 (twenty-sixth layer), 27 (twenty-seventh layer), 28 (twenty-eighth layer), 29 (twenty-ninth layer), 30 (thirtieth layer), 31 (thirty-first layer), 32 (thirty-second layer), 33 (thirty-third layer), 34 (thirty-fourth layer), 35 (thirty-fifth layer), 36 (thirty-sixth layer), 37 (thirty-seventh layer), 38 (thirty-eighth layer), 39 (thirty-ninth layer), 40 (fortieth layer), 41 (forty-first layer), 42 (forty-second layer), 43 (forty-third layer), 44 (forty-fourth layer), 45 (forty-fifth layer), 46 (forty-sixth layer), 47 (forty-seventh layer), 48 (forty-eighth layer), 49 (forty-ninth layer), 50 (fiftieth layer).</p> <p>See, e.g., Japanese Patent App. Pub. No. JP2003/100896 to Fujiwara et al. (“Fujiwara”) at:</p>

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Claim	Claim Language	Exemplary Disclosures in Additional References
		<p>A semiconductor device according to the present invention comprises a semiconductor substrate and a first substrate divided into the semiconductor substrate.</p> <p>A first transistor having a first gate insulating film having a structure in which a first insulating film and a second insulating film are stacked in this order from the semiconductor substrate, and are divided into the semiconductor substrate. The third insulating film and the fourth insulating film formed in the second region are stacked in this order from the semiconductor substrate, and the silicon oxide film is formed as compared with the first gate insulating film. A second transistor having a second gate insulating film having a large converted film thickness, and the second and fourth transistors.</p> <p>The insulating film of is a high-dielectric film formed at the same time.</p> <p>And the third insulating film are interface layers having different compositions or film thicknesses from each other. Particularly preferably, the first and third insulating films are interface layers having different compositions from each other formed by the reaction between the second and third insulating films and the semiconductor substrate or the thin film formed on the surface thereof. I shall.</p> <p>The present invention is also a method of manufacturing a semiconductor device including transistors having different gate insulating film structures, which comprises selectively forming an oxygen barrier layer on the surface of the first region of the semiconductor substrate, A high dielectric insulating film is formed on the semiconductor substrate, the first region includes the oxygen barrier layer or an interface layer formed of a reaction layer between the oxygen barrier layer and the high dielectric film, and the second region includes the semiconductor. It is characterized by including a step of forming a gate insulating film including an interface layer by a reaction between a substrate and the high dielectric film, and a step of patterning a gate electrode on the gate insulating film.</p> <p>In the present invention, the high dielectric film (metal oxide or its silicate) as the gate insulating film is formed, or is formed on the substrate during the subsequent crystallization annealing. The interface layer formed between the thin film and the thin film has different characteristics and structure by controlling the electrical film thickness and film quality of the interface layer by introducing nitrogen into the substrate surface or inserting a thin film nitride film. A gate insulating film is formed on the same substrate. In other words, by treating the interface layer that was previously integrated with the</p>

Claim	Claim Language	Exemplary Disclosures in Additional References
		<p>high-k dielectric film as a laminated structure with independent functions, by forming a high-k dielectric film with a sufficient thickness to suppress direct tunneling. By suppressing the gate leakage current and making the state of the substrate interface different depending on the transistor region, the gate insulating film can be selectively used for each transistor which requires different specifications.</p> <p>Next, a sacrificial oxide film 61 is formed by dilute hydrofluoric acid treatment.</p> <p>Was removed, after performing the hydrogen-terminated silicon substrate 51 surface, as shown in FIG. 8, TiO₂ is a high dielectric film</p> <p>The film 81 is formed. Specifically, the TiO₂ film 81 having a thickness of 5 nm is formed by the DC sputtering method using a TiO₂ sintered target under the sputtering conditions of power 300 W, pressure 1 Pa, Ar / O₂ flow rate 22 / 1.2 sccm. . At this time, the surface of the silicon substrate in the regions A and B is oxidized by the oxygen plasma atmosphere during the sputtering of the TiO₂ film, and the interface layers 82 and 83 are formed. The interface layer 82 in the region A has the result that the nitrogen introduction region 64 suppresses the diffusion of oxygen into the substrate.</p> <p>It becomes a thin silicon oxide film, and the interface layer 83 in the region B becomes a thicker silicon oxide film.</p> <p>A polycrystalline silicon film having a thickness of 175 nm is formed on the upper surface by a CVD method.</p> <p>A gate electrode 91 is formed by forming a film and performing patterning. Along with the gate electrode 91, the TiO₂ film 81 and the interface layers 82 and 83 which will be the gate insulating film thereunder are also patterned. After that, in order to crystallize the TiO₂ film 81, RTA with a heat treatment temperature of 900 ° C. and a heat treatment time of 30 seconds is performed.</p> <p>Do. At this time, the surface of the silicon substrate in the region B is oxidized by the diffusion of oxygen from the TiO₂ film 81 to the silicon substrate 51 by RTA, and the interface layer 83 grows to finally become the interface layer 83a of about 2 nm. In the region A, the nitrogen introduction region 64 suppresses the diffusion of oxygen into the substrate, The growth of the interface layer 82 is suppressed, and finally about 0.7 nm. The interface layer 82a has a thickness of nm.</p> <p>The TiO₂ film 81 becomes a microcrystalline state by the RTA treatment, and its dielectric constant is about 20. Therefore, the equivalent oxide film thickness of this portion is about 1 nm. Also, Ti.</p>

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Claim	Claim Language	Exemplary Disclosures in Additional References
		<p>By the physical mixing of Ti into the substrate by sputtering of the O 2 film 81 and the activation annealing performed in a later step, the interface layers 82a and 83a become silicon oxide films containing a trace amount of Ti, and their dielectric constant is 5 It will be about.</p> <p>Therefore, the gate insulating film in the region A has a laminated structure of the interface layer 82a and the TiO 2 film 81, and the gate insulating film in the region B has a laminated structure of the interface layer 83a and the TiO 2 film 81. These gate insulating films have a physical film thickness of 5 nm or more, and can sufficiently suppress the direct tunneling current. On the other hand, due to the difference in the film thickness of the interface layers 82a and 83b, in the region A, the oxide film equivalent film thickness is 1.6n.</p> <p>In the region B, the gate insulating film of m has an oxide film equivalent thickness of 2.6. Thus, the gate insulating film having a thickness of nm is formed.</p> <p>Next, as shown in FIG. 10, N-type impurities are ion-implanted substantially perpendicularly to the silicon single crystal substrate 51 to form shallow source / drain n-type diffusion layers 101. Specifically, for example, arsenic is accelerated at an acceleration voltage of 5 keV to 10 k. eV, dose amount $5 \times 10^{14} / \text{cm}^2$ to $1 \times 10^{15} / \text{cm}^2$ Inject.</p> <p>As described above, according to this embodiment, the transistors Q1 and Q2 formed in the regions A and B are formed.</p> <p>Are formed of gate insulating films having different physical thicknesses of silicon oxide, while having a physical film thickness sufficient to suppress the direct tunneling current. Due to the difference in the gate insulating film structure, the transistor Q1 in the region A is relatively inferior in gate breakdown voltage and reliability to the transistor Q2 in the region B, but has a characteristic difference in high current driving capability.</p> <p>The gate insulating film has a laminated structure of a high dielectric film and an interface layer formed as a reaction layer between the high dielectric film and the substrate. By changing it, the interface layers of both are different. Moreover, the processing for changing the substrate surface state can be performed</p>

Claim	Claim Language	Exemplary Disclosures in Additional References
		<p>using the mask for channel ion implantation in the regions A and B as it is. Therefore, although the transistors Q1 and Q2 have different types of gate insulating film structures, the manufacturing process is simple, with only one additional ion implantation step.</p> <p style="text-align: center;">【 図 1 1 】</p> <p>See, e.g., U.S. Pat. No. 8,349,695 to Scheiper et al. (“Scheiper”) at: 3:42-63: FIG. 1a schematically illustrates a cross-sectional view of a semiconductor device 100 which comprises a substrate 101 and a semiconductor layer 102 formed above the substrate 101. The semiconductor layer 102 is typically provided in the 45 form of a silicon material, as explained above. Moreover, a first semiconductor region 102A and a second semiconductor region or active region 102B are provided in the semiconductor layer 102. The active regions 102A, 102B are to be understood as semiconductor regions in and above 50 which transistor elements are to be formed on</p>

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Claim	Claim Language	Exemplary Disclosures in Additional References
		<p>the basis of gate electrode structures including a high-k dielectric material. In the example shown, it may be assumed that a gate electrode structure of reduced gate dielectric thickness is to be formed on the semiconductor region 102A, while a gate electrode 55 structure having a gate dielectric material of increased thickness is to be formed on the semiconductor region 102B. Furthermore, in the manufacturing stage shown, a gate dielectric material 151 is selectively formed on the active region 102B and is comprised of silicon dioxide with a specific 60 thickness, for instance with a thickness of several nanometers, depending on the device requirements or any transistors to be formed in and above the semiconductor region 102B.</p> <p>4:27-36: FIG.1b schematically illustrates the semiconductor device 100 in a further advanced manufacturing phase in which the etch mask 103 is removed and the device 100 is exposed to a cleaning ambient 105 in order to remove contaminants and also to re-grow a thin dielectric base layer 152 on the semiconductor region 102A. For this purpose, a plurality of well established process techniques are available in order to obtain a silicon dioxide material on the basis of a well-controllable growth process.</p> <p>4:37-56: FIG.1c schematically illustrates the semiconductor device 100 when exposed to a deposition ambient 106 in which a high-k dielectric material. Such as hafnium oxide, is deposited above the active regions 102A, 102B, thereby forming a high-k dielectric layer 153. Thus, the layers 152 and 153 in combination may represent the gate dielectric material of a transistor formed in and above the semiconductor region 102A, thereby providing the required characteristics for high performance transistors, while the layer 153 in combination with the “thick” silicon dioxide material 151 represents the dielectric material for transistors and other circuit elements in which a Superior performance with respect to reduced leakage currents and the like is required. It should be appreciated that the deposition process 106 may be performed on the basis of any appropriate deposition recipe, for instance, by chemical vapor deposition (CVD), physical vapor deposition (PVD) and the like. For example, a thickness of the high-k dielectric layer 153 may be in the range of one to several nanometers, depending on the overall requirements in view of capacitive coupling, leakage currents and the like.</p>

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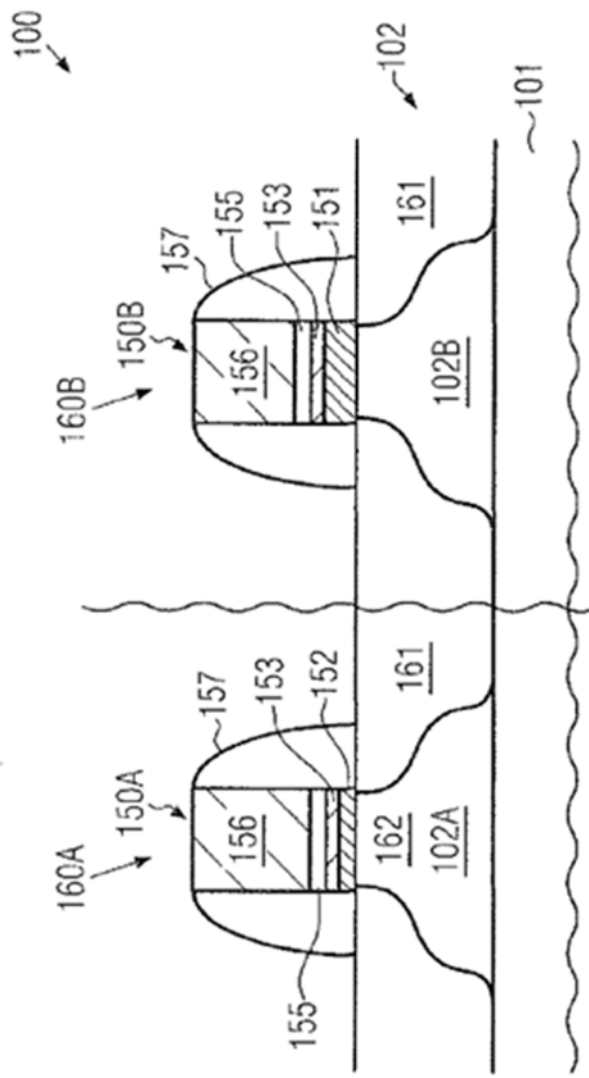
Claim	Claim Language	Exemplary Disclosures in Additional References
		 <p>FIG. 1g (prior art)</p> <p>See, e.g., U.S. Pat. No. 7,335,561 to Sakai ("Sakai '561") at: [2:31-53] The typical ones of the inventions disclosed in this application will be briefly described as follows. A semiconductor integrated circuit device of the present invention comprising: a semiconductor Substrate; a first MIS transistor including a pair of first semiconductor regions formed in the semiconductor substrate and a first conductive piece formed above the semiconductor Substrate through a first gate insulation film in a region between the pair of the first semiconductor regions; and a second MIS transistor including a pair of second semiconductor regions formed in the semiconductor Substrate and a second conductive piece formed above the semiconductor Substrate through a second gate</p>

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Claim	Claim Language	Exemplary Disclosures in Additional References
		<p>insulation film in a region between the pair of the second semiconductor regions, wherein the thickness of the first gate insulation film is larger than the thickness of the second gate insulation film and the first gate insulation film is comprised of the first insulation film located on the semiconductor Substrate and the second insulation film located on the first insulation film; and wherein the second gate insulation film is comprised of a third insulation film located on the semiconductor substrate and the dielectric constant of the second and third insulation films is larger than the dielectric constant of the first insulation film.</p> <p>[5:19-22] FIG. 35 is a major part sectional view of a semiconductor substrate showing an example of the manufacturing method of a semiconductor integrated circuit according to an embodiment of the present invention in the order of steps;</p> <p>[6:1-18] An example of the manufacturing method for the semiconductor integrated circuit device according to an embodiment of the present invention will be described using major part sectional views of the semiconductor Substrate shown in FIGS. 1-40. In the Figures, a region A indicates a region in which a gate insulation film having a larger effective thickness is formed and the region B indicates a region in which a gate insulation film having a smaller effective thickness is formed. In the regions A, B, n-channel MIS transistor (hereinafter referred to as low V_{th} NMOS) having a low threshold value voltage (hereinafter referred to as V_{th}), p-channel MIS transistor (hereinafter referred to as low V_{th} PMOS) having a low V_{th}, n-channel MIS transistor (hereinafter referred to as high V_{th} NMOS) having a high V_{th} and p-channel MIS transistor (hereinafter referred to as high V_{th} PMOS) having a high V_{th} are formed and that is, eight kinds of the MIS transistors are formed on the same substrate.</p> <p>[7:60-8:4] Next, after the resist pattern RP10 is removed, as shown in FIG. 16, the protective film 5 is removed and the silicon oxide film 9 is formed on the surface of the semiconductor substrate 1, for example, in the thickness of 4 to 5 nm. The silicon oxide film 9 can be formed according to the thermal CVD method or thermal oxidation method. Meanwhile, the aforementioned silicon oxide film may be turned to silicon nitride film by nitriding the semiconductor substrate 1 thermally. The aforementioned thermal nitration is carried out with the semiconductor 1 heated at about 900° C. in a pressure reduced atmosphere containing nitrogen made radical by plasma discharge</p>

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Claim	Claim Language	Exemplary Disclosures in Additional References
		<p>[8:5-10] Next, as shown in FIG. 17, after the region A is covered with the resist pattern RP1, as shown in FIG. 18, the silicon oxide film 9 in the region B is removed using diluted HF with resist pattern RP11 as a mask. After that, as shown in FIG. 19, the resist pattern RP11 is removed.</p> <p>[8:11-26] Next, as shown in FIG. 20, high dielectric constant insulation film 10, for example, alumina film is formed on the semiconductor substrate 1. The high dielectric constant insulation film 10 can be deposited according to, for example, sputtering method. The thickness of the high dielectric constant insulation film 10 formed on the semiconductor substrate 1 is set so that its effective thickness is about 5 nm. For example, the alumina film is deposited in the thickness of about 10 nm considering dielectric constant. Consequently, gate insulation film 11 comprised of the high dielectric constant insulation film 10 about 5 nm in terms of its effective thickness is formed in the region B and gate insulation film 12 comprised of stacked film of the high dielectric constant film 10 and the silicon oxide film 9 about 9 to 10 nm in terms of its effective thickness is formed in the region A</p> <p>[8:27-31] Before forming the aforementioned high dielectric constant insulation film 10 on the semiconductor substrate 1, silicon oxide film or silicon nitride film, or silicon oxide nitride film less than 1 nm or less may be formed to stabilize an interface with the semiconductor substrate 1.</p> <p>[8:32-34] Next, as shown in FIG. 21, silicon film 13 about 200 nm. thick is deposited on the semiconductor Substrate 1 according to the CVD method.</p> <p>[8:35-39] Next, as shown in FIG.22, after resist pattern 12 is formed in the NMOS formation region in the regions A, B, p-type impurity, for example, boron is ion-implanted into the silicon film 13 in the PMOS formation region in the regions A, B with this resist pattern RP12 as a mask.</p> <p>[8:40-46] Next, the resist pattern 12 is removed and as shown in FIG. 23, resist pattern RP13 is formed in the PMOS formation region in the regions A, B. After that, n-type impurity, for example, phosphorus is ion-implanted into the NMOS formation region in the regions A, B with this resist pattern RP13 as a mask.</p> <p>[8:47-55] Next, after the resist pattern RP13 is removed, by per forming heat treatment on the semiconductor Substrate 1, for example at 950° C. for about 60 seconds, the aforementioned n-type</p>

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Claim	Claim Language	Exemplary Disclosures in Additional References
		<p>impurity and p-type impurity implanted into the silicon film 13 are activated. Further, the silicon film 13 in the NMOS formation region in the regions A, B is turned to n-type silicon polycrystal film and the silicon film 13 in the PMOS formation region in the regions A, B is changed to p-type silicon polycrystal film.</p> <p>[8:56-60] After as shown in FIG. 24, silicon oxide film 14 is deposited on the semiconductor Substrate 1 according to the CVD method, as shown in FIG. 25, resist pattern RP14 is formed to form gate electrodes of the n-channel and p-channel MIS transistor.</p> <p>[8:61-9:3] Next, after as shown in FIG. 26, the silicon oxide film 14 is etched with the resist pattern RP14 as a mask, the resist pattern RP14 is removed. Subsequently, as shown in FIG. 27, with the patterned silicon oxide film 14 as a mask, the silicon film 13 is etched so as to form a gate electrode (conductive piece) 15n comprised of n-type silicon poly crystal film in the NMOS formation region in the regions A, B and a gate electrode (conductive piece) comprised of p-type silicon polycrystal film in the PMOS formation region in the regions A, B</p> <p>[11:5-18] As described above, according to this embodiment, after the silicon oxide film 9 is formed on the surface of the semiconductor substrate 1, the silicon oxide film 9 in the region B (region in which a gate insulation whose effective thickness is small is formed) is removed with diluted HF and after that, by forming high dielectric constant insulation film 10 on the semiconductor Substrate 1, a damage or pollution to the surface of the semiconductor substrate 1 is prevented So as to form two kinds of the gate insulation films, that is, the gate insulation film 12 comprised of stacked film of the high dielectric constant insulation film 10 and the silicon oxide film 9 and the gate insulation film 11 comprised of the high dielectric constant insulation film 10 on the same semiconductor Substrate 1.</p> <p>[11:19-24] Because the gate insulation film 12 in the region A is comprised of stacked film of the high dielectric constant insulation film 10 and the silicon oxide film 9, the difference in level between the region A and region B can be reduced compared to the stacked film comprised of two high dielectric constant insulation films.</p> <p>[11:25-30] Further because the thickness of the silicon oxide film 9 can be reduced as compared to a case where the gate insulation film 12 in the region A is comprised of only the silicon oxide film,</p>

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Claim	Claim Language	Exemplary Disclosures in Additional References
		<p>oxidation of the interior of the isolation groove 4a can be suppressed so that stress at an end portion of the isolation groove 4a can be reduced.</p> <p>FIG. 35</p> <p>See, e.g., U.S. Pat. App. Pub. No. 2009/0039445 to Wu ("Wu '445") at:</p> <p>[0018] Still referring to FIG. 1A, the gate structures 12A and 12B may be formed by conventional CVD deposition, lithographic patterning, and plasma (dry) etching methods known in the art. The gate</p>

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Claim	Claim Language	Exemplary Disclosures in Additional References
		dielectric portions 14A and 14B may be formed by any process known in the art, e.g., thermal oxidation, nitridation, sputter deposition, chemical vapor deposition, or combinations thereof. The gate dielectric portions 14A and 14B may be formed of silicon oxide, silicon nitride, silicon oxynitride, and high-K dielectrics (e.g., K>8) including transition metal oxide and rare earth metal oxides. For example, high-K dielectrics may be formed of aluminum oxides (e.g., Al ₂ O ₃), hafnium oxides (e.g., HfO ₂), hafnium oxynitrides (HfON), hafnium silicates (e.g. HfSiO ₄), hafnium silicon oxynitrides (e.g., HfSi _x O _y N _z), zirconium oxides (e.g., ZrO ₂), zirconium oxynitrides (e.g., ZrON), zirconium silicon oxides (e.g., ZrSiO ₂), yttrium oxides (Y ₂ O ₃), lanthanum oxides (La ₂ O ₃), cerium oxides (CeO ₂), titanium oxides (TiO ₂), tantalum oxides (Ta ₂ O ₅), or combinations thereof. The high-k dielectric layer may be formed by known CVD methods such as atomic layer CVD (ALCVD) and metal-organic CVD (MOCVD). It will be appreciated that the high-K dielectric layer may include a lowermost interfacial layer formed on the semiconductor substrate such as an oxide or oxynitride (not shown).
		See 1[b]

Claim	Claim Language	Exemplary Disclosures in Additional References
1 [e]	the second gate insulating film includes a second interface layer being in contact with the semiconductor substrate and a second high dielectric constant insulating film formed on the second interface layer,	<p>The following references disclose and/or render obvious a “the second gate insulating film includes a second interface layer being in contact with the semiconductor substrate and a second high dielectric constant insulating film formed on the second interface layer,” as further described below.</p> <p>See, e.g., U.S. Pat. No. 6,787,421 to Gilmer et al. (“Gilmer”) at:</p> <p>[2:36-55] Referring now to FIGS. 1-4, a semiconductor device 10 is fabricated in accordance with one embodiment of the invention. Referring now to FIGS. 1-4, a semiconductor device 10 is fabricated in accordance with one embodiment of the invention. As shown in FIG. 1, semiconductor device 10 includes a Semiconductor Substrate 12 which in a preferred embodiment is a single crystal Silicon Substrate (also sometimes referred to as a wafer), but which can instead be formed from other Semiconductor Substrate materials. Within substrate 12, trench isolation regions 14, preferably shallow trench isolation regions, are formed in a conventional manner for the purpose of electrically isolating different individual devices to be</p>

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Claim	Claim Language	Exemplary Disclosures in Additional References
		<p>formed. After forming trench isolation regions 14, a first gate dielectric 16 is formed over substrate 12. First gate dielectric 16 is preferably silicon dioxide or silicon oxynitride, and is preferably formed by thermal oxidation in accordance with conventional practices. The thickness of gate dielectric 16 is determined by the particular device requirements for devices to be formed in I/O device region 24 as further explained below, but generally will be within a range of 30–50 Angstroms (3–5 nanometers).</p> <p>[2:56-3:6] After forming first gate dielectric 16, a (photo)resist mask 18 is formed over the substrate to mask off a portion of the first gate dielectric layer. AS shown in FIG. 1, Semiconductor device 10 includes two different device regions, namely a core device region 22 and an I/O device region 24. In operation, devices to be formed in core device region 22 require thinner gate dielectrics that operate at lower Voltages than, e.g., I/O devices to be formed in I/O device region 24 that can withstand higher Voltages required for I/O functions. Accordingly, resist mask 18 is formed to protect the portion of first gate dielectric 16 which will Serve, in part, as a gate dielectric for the higher Voltage I/O devices. Other dielectric materials may instead be used for first gate dielectric 16. Silicon dioxide and silicon oxynitride are attractive choices because of the industry's understanding of these materials, the ability to form high gate quality films, and because they can be formed by Selective growth techniques rather than requiring blanket depositions and etch steps.</p> <p>[3:7-33] Semiconductor device 10 is then etched to remove unprotected portions of first gate dielectric 16 in core device region 22, as shown in FIG. 2. The resist mask 18 is then removed and a Second gate dielectric 20 is formed on exposed portions of Substrate 12 within the core device region 22. In a preferred embodiment, second gate dielectric 20 is also silicon dioxide or silicon oxynitride, but like first gate dielectric 16 other materials could be used. This Second gate dielectric can be formed by thermal oxidation and/or chemical oxidation in accordance with conventional practices. The thickness of gate dielectric 20 is also determined by the particular device requirements for devices to be formed in core device region 22 as further explained below, but generally will be within a range of 4-12 Angstroms (0.4-1.2 nanometers). Because Second gate dielectric 20 is So thin, it may be difficult to adequately control the thickness or obtain an oxide of Sufficient quality using thermal oxidation processes and therefore chemical oxidation may be useful. For instance, the thin dielectric may be formed by</p>

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Claim	Claim Language	Exemplary Disclosures in Additional References
		<p>growing a thin oxide by rinsing the substrate in ozonated water. A combination of thermal and chemical treatment may also be used to form second dielectric 20. It may also be sufficient for second gate dielectric 20 to be a native oxide which is grown on Substrate 12 as a result of exposing the Substrate to ambient or other oxygen containing environment. In other embodiments, second gate dielectric 20 can be deposited, e.g., by atomic layer deposition.</p> <p>[3:34-43] In the course of forming Second gate dielectric 20, the thickness of first gate dielectric 16 may change, depending on the technique used to form the Second gate dielectric 20, and should be taken into account in choosing the initial deposited or grown thickness of first gate dielectric 16. Generally, however, it is not anticipated that the thickness of first gate dielectric 16 will change Significantly unless second gate dielectric 20 is deposited over first gate dielectric 16 rather than forming it through a thermal or chemical reaction of the Substrate Surface.</p> <p>[3:44-4:7] Now that gate dielectrics of two different thicknesses have been formed, a high-k dielectric (generally with $k > 4$, preferably with $k > 6$, and most preferably with $k > 7$) is deposited over semiconductor device 10. In a preferred embodiment, this high-k dielectric is a metal oxide, Such as metal oxide 26 shown in FIG. 3. Suitable materials for metal oxide 26 preferably include hafnium oxide (HfO_2), hafnium silicate (HfSiO_2), or lanthanum aluminate (LaAlO_3), but lanthanum oxide, hafnium aluminate, Zirconium oxide, and Zirconium Silicate, and other like materials, may also be Suitable high-k dielectrics. The thickness of the high-k dielectric layer will be dependent on the particular device requirements in each region of the Substrate (the core region and the I/O region), but generally it is believed the thickness of a metal oxide will be between about 15-50 angstroms (1.5-5.0 nanometers). The underlying thicknesses of first gate dielectric 16 and Second gate dielectric 20 will also affect the choice of thickness of the high-k dielectric. The thickness of the high-k dielectric should be chosen So that its equivalent oxide thickness (EOT), when added to the EOT of the first gate dielectric 16 (I/O device dielectric) thickness or Second gate dielectric 20 (core device dielectric) thickness, provides a total EOT appropriate for the I/O and core device, respectively. Similarly, this calculation should be used to determine the initial deposited or grown thicknesses of the first and Second gate dielectrics. Because metal oxide 26 is deposited as a single blanket deposition, its thickness will not vary much across the Substrate Surface and thus one should</p>

Claim	Claim Language	Exemplary Disclosures in Additional References
		<p>use the thicknesses of the first and Second dielectrics as the “variables” to achieve the final EOTs for the core and I/O devices.</p> <p>FIG. 4</p> <p><i>See, e.g., Japanese Patent App. Pub. No. JP2006/060155 to Yasuhira et al. (“Yasuhira”) at: Hereinafter, some of the embodiments of the present invention will be described in detail with reference to the drawings.</i></p> <p><i>(Embodiment 1)</i></p> <p>FIG. 1 is a cross-sectional view of the main part of the semiconductor device according to the first embodiment of the present invention, and FIGS. Here, a technology generation in which the design standard of the semiconductor element is 65 nm to 45 nm is shown. In this generation, a MISFET that operates at a voltage of 1 V or less is formed in the internal circuit of the semiconductor device, and the thickness of the gate insulating film is about 1.2 nm or less in terms of a silicon oxide film. A peripheral circuit of the semiconductor device, for example, an input / output circuit, is formed with a MISFET operating at a (power supply) voltage of 1.5 V to 3.3 V, and the thickness of the gate insulating film is 3 nm to 6 nm in terms of silicon oxide film. It will be about. Here, since the peripheral circuit differs greatly</p>

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Claim	Claim Language	Exemplary Disclosures in Additional References
		<p>depending on the semiconductor device, there is a range in the usage range of the driving voltage and the film thickness of the gate insulating film.</p> <p>In the following description, a p-channel type MISFET will be described, but an n-channel type MISFET is formed in the same manner. As shown in FIG. 1, for example, at least two types of MISFETs having gate insulating films having different equivalent film thicknesses in a region corresponding to a peripheral circuit portion on a p-conductivity type silicon substrate 1 and a region corresponding to an internal circuit portion are provided. It is formed.</p> <p>That is, an n well layer 2 is formed on the surface portion of the silicon substrate 1, and the surface portion of the n well layer 2 is partitioned by an element isolation region 3 by STI. In the MISFET in the peripheral circuit portion, the base oxide film 4 having a thickness of 4 to 6 nm and the nitride layer 4a whose surface is modified to a nitrogen-containing layer, the High-k film 5 and the surface thereof are modified to a nitrogen-containing layer. A first gate insulating film 6 made of a laminated film of the nitrided layer 5a is formed. Then, a gate electrode 9 is constituted by the polycrystalline silicon layer 7 containing the p-conductivity type or n-conductivity type impurity formed on the first gate insulating film 6 and the silicide layer 8, and the first gate insulating film 6. A sidewall insulating film 10 is provided on the side wall of the gate electrode 9. Here, the base oxide film 4 is formed of a silicon oxide film, and the high-k film 5 is formed of hafnia (HfO₂), zirconia (ZrO₂), hafnium silicate (HfSiOx), zirconium silicate (ZrSiOx), hafnium aluminate (An insulating film having a thickness of 2 to 3 nm made of HfAlOx) or zirconium aluminate (ZrAlOx) is preferable. Alternatively, the High-k film 5 may be configured by an insulating film having a stacked structure in which two or more types of insulating films are selected from the high dielectric constant insulating films and stacked. A source / drain region including a source / drain diffusion layer 11 and a silicide layer 8 is provided on the surface of the n well layer 2.</p> <p>On the other hand, in the MISFET of the internal circuit portion, the base film 12 with a film thickness of about 1 nm and the nitride layer 12a whose surface is modified to a nitrogen-containing layer, the High-k film 5 and the nitride layer which is a modified layer on the surface thereof A second gate insulating film 13 is formed by the laminated film 5 a, and the above-described polycrystalline silicon layer 7 and silicide layer 8 are provided on the second gate</p>

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Claim	Claim Language	Exemplary Disclosures in Additional References
		<p>insulating film 13. Sidewall insulating films 10 are provided on the side walls of the second gate insulating film 13 and the gate electrode 9, and source / drain regions including the source / drain diffusion layers 11 and the silicide layers 8 are provided on the surface of the n-well layer 2. It has been. In the second gate insulating film 13 of the MISFET, the base film 12 has a silicon oxide film structure as a basic structure, and is interposed between the high-k film 5 and the silicon substrate 1 on the surface of the n-well layer 2. It has functions such as preventing boron penetration and improving the surface mobility of carrier charges (holes).</p> <p>Next, a method for manufacturing the semiconductor device according to the present invention will be described with reference to FIGS. Here, the same components as those in FIG. 1 are denoted by the same reference numerals.</p> <p>Next, the surfaces of the base oxide film 4 and the base film 12 are nitrided by plasma nitriding, and the silicon oxide film surfaces are modified to form nitride layers 4a and 12a as nitrogen-containing layers (FIG. 2D). . In this plasma nitriding method, N₂ gas, N₂O, NO, N₂H₂ and NH₃ gas, which are raw material gases, are excited by plasma in ECR (Electron Cyclotron Resonance), ICP (Inductively Coupled Plasma), (magnetron type)) Active species of nitrogen are generated by excitation with RF plasma or helicon wave plasma, and the active species are exposed to the surface of the silicon oxide film. The active species include nitrogen atom ions, molecular ions, neutral radicals, and the like. Here, it is preferable that only the nitrogen neutral radicals are extracted from the active species to form the nitride layers 4a and 12a. For example, among the active species of nitrogen formed in the plasma excitation chamber, neutral radicals having a relatively long lifetime are extracted by the downflow method, and the neutral oxides are irradiated onto the surface of the base oxide film 4 and the base film 12. In this manner, the nitride layers 4a and 12a are preferably formed by the reaction between neutral radicals and the surface of the silicon oxide film.</p> <p>In the plasma nitriding method using nitrogen neutral radicals, the nitrogen active species and the depth of the nitride layer in the nitride layers 4a and 12a to be formed are limited because the active species of nitrogen are controlled to one kind. It becomes possible to control with high accuracy. Further, this method is a so-called remote plasma method, and since the ion irradiation or plasma emission irradiation can be prevented, irradiation damage in the base</p>

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		<p>oxide film 4 and the base film 12 is greatly reduced, and a high-quality gate insulating film is obtained. Can be secured.</p> <p>Here, when the active species is generated by plasma excitation of a source gas containing hydrogen such as N₂ H₂ or NH₃ gas, a large amount of hydrogen is mixed into the nitride layer and the silicon oxide film to deteriorate the film quality. . Therefore, in this case, it is preferable to desorb hydrogen in the film by performing a heat treatment in an inert gas after the plasma nitridation.</p> <p>In the plasma nitriding method described above, the amount or depth of nitrogen introduced into the base oxide film 4 and the base film 12 can be easily controlled by the plasma processing conditions or processing time such as the power power of plasma excitation. FIG. 4 shows an example of nitrogen distribution in the nitride layer 12a. Here, the plasma nitridation was performed by irradiating the surface of the underlayer 12 with nitrogen neutral radicals in a downflow manner by exciting the N₂ gas with ECR. FIG. 4 is a nitrogen distribution diagram obtained by XPS (X-ray Photoelectron Spectroscopy) analysis of the nitride layer 12a. As can be seen from FIG. 4, the nitrogen concentration on the surface of the nitride layer 12a is 15 at. % To 20 at. The nitrogen concentration decreases as the depth from the surface decreases, and nitrogen does not exist in a region deeper than 1 nm. Therefore, there is almost no nitrogen at the interface between the base film 12 and the n-well layer 2.</p> <p>Next, a High-k film 5 is deposited on the entire surface so as to cover the base oxide film 4 and the base film 12. As the High-k film 5, for example, a thin film of HfAlOx, HfSiOx or HfO₂ having a relative dielectric constant of 10 to 20 is formed. It is preferable to use an ALD (Atomic Layer Deposition) method or an MOCVD (Metal Organic Chemical Vapor Deposition) method for the growth of such a High-k film. For example, when HfAlOx is formed as the high-k film by using the ALD method, the substrate temperature is 300 ° C., and hafnium tetrachloride (HfCl₄) and trimethylaluminum (TMA) are used as the film forming raw materials. A thin film of HfAlOx having a film thickness of 2 nm to 3 nm is formed using water vapor (H₂O) or ozone (O₃) as an oxidant (FIG. 3A). In the formation of the high-k film 5, the thin base film 12 prevents an interface reaction between the high-k film 5 and the</p>

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		<p>silicon substrate 1 on the surface of the n-well layer 2.</p> <p>【図 1】</p> <p>内部回路部 周辺回路部</p> <p>See, e.g., Japanese Patent App. Pub. No. JP2003/100896 to Fujiwara et al. (“Fujiwara”) at:</p> <p>A semiconductor device according to the present invention comprises a semiconductor substrate and a first substrate divided into the semiconductor substrate.</p> <p>A first transistor having a first gate insulating film having a structure in which a first insulating film and a second insulating film are stacked in this order from the semiconductor substrate, and are divided into the semiconductor substrate. The third insulating film and the fourth insulating film formed in the second region are stacked in this order from the semiconductor</p>

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Claim	Claim Language	Exemplary Disclosures in Additional References
		<p>substrate, and the silicon oxide film is formed as compared with the first gate insulating film. A second transistor having a second gate insulating film having a large converted film thickness, and the second and fourth transistors.</p> <p>The insulating film of is a high-dielectric film formed at the same time.</p> <p>And the third insulating film are interface layers having different compositions or film thicknesses from each other. Particularly preferably, the first and third insulating films are interface layers having different compositions from each other formed by the reaction between the second and third insulating films and the semiconductor substrate or the thin film formed on the surface thereof. I shall.</p> <p>The present invention is also a method of manufacturing a semiconductor device including transistors having different gate insulating film structures, which comprises selectively forming an oxygen barrier layer on the surface of the first region of the semiconductor substrate, A high dielectric insulating film is formed on the semiconductor substrate, the first region includes the oxygen barrier layer or an interface layer formed of a reaction layer between the oxygen barrier layer and the high dielectric film, and the second region includes the semiconductor. It is characterized by including a step of forming a gate insulating film including an interface layer by a reaction between a substrate and the high dielectric film, and a step of patterning a gate electrode on the gate insulating film.</p> <p>In the present invention, the high dielectric film (metal oxide or its silicate) as the gate insulating film is formed, or is formed on the substrate during the subsequent crystallization annealing. The interface layer formed between the thin film and the thin film has different characteristics and structure by controlling the electrical film thickness and film quality of the interface layer by introducing nitrogen into the substrate surface or inserting a thin film nitride film. A gate insulating film is formed on the same substrate. In other words, by treating the interface layer that was previously integrated with the high-k dielectric film as a laminated structure with independent functions, by forming a high-k dielectric film with a sufficient thickness to suppress direct tunneling. By suppressing the gate leakage current and making the</p>

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		<p>state of the substrate interface different depending on the transistor region, the gate insulating film can be selectively used for each transistor which requires different specifications.</p> <p>Next, a sacrificial oxide film 61 is formed by dilute hydrofluoric acid treatment. Was removed, after performing the hydrogen-terminated silicon substrate 51 surface, as shown in FIG. 8, TiO₂ is a high dielectric film</p> <p>The film 81 is formed. Specifically, the TiO₂ film 81 having a thickness of 5 nm is formed by the DC sputtering method using a TiO₂ sintered target under the sputtering conditions of power 300 W, pressure 1 Pa, Ar / O₂ flow rate 22 / 1.2 sccm. . At this time, the surface of the silicon substrate in the regions A and B is oxidized by the oxygen plasma atmosphere during the sputtering of the TiO₂ film, and the interface layers 82 and 83 are formed. The interface layer 82 in the region A has the result that the nitrogen introduction region 64 suppresses the diffusion of oxygen into the substrate.</p> <p>It becomes a thin silicon oxide film, and the interface layer 83 in the region B becomes a thicker silicon oxide film.</p> <p>A polycrystalline silicon film having a thickness of 175 nm is formed on the upper surface by a CVD method.</p> <p>A gate electrode 91 is formed by forming a film and performing patterning. Along with the gate electrode 91, the TiO₂ film 81 and the interface layers 82 and 83 which will be the gate insulating film thereunder are also patterned. After that, in order to crystallize the TiO₂ film 81, RTA with a heat treatment temperature of 900 ° C. and a heat treatment time of 30 seconds is performed.</p> <p>Do. At this time, the surface of the silicon substrate in the region B is oxidized by the diffusion of oxygen from the TiO₂ film 81 to the silicon substrate 51 by RTA, and the interface layer 83 grows to finally become the interface layer 83a of about 2 nm. In the region A, the nitrogen introduction region 64 suppresses the diffusion of oxygen into the substrate. The growth of the interface layer 82 is suppressed, and finally about 0.7 nm. The interface layer 82a has a thickness of nm.</p>

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		<p>The TiO 2 film 81 becomes a microcrystalline state by the RTA treatment, and its dielectric constant is about 20. Therefore, the equivalent oxide film thickness of this portion is about 1 nm. Also, Ti.</p> <p>By the physical mixing of Ti into the substrate by sputtering of the O 2 film 81 and the activation annealing performed in a later step, the interface layers 82a and 83a become silicon oxide films containing a trace amount of Ti, and their dielectric constant is 5 It will be about.</p> <p>Therefore, the gate insulating film in the region A has a laminated structure of the interface layer 82a and the TiO 2 film 81, and the gate insulating film in the region B has a laminated structure of the interface layer 83a and the TiO 2 film 81. These gate insulating films have a physical film thickness of 5 nm or more, and can sufficiently suppress the direct tunneling current. On the other hand, due to the difference in the film thickness of the interface layers 82a and 83b, in the region A, the oxide film equivalent film thickness is 1.6n.</p> <p>In the region B, the gate insulating film of m has an oxide film equivalent thickness of 2.6. Thus, the gate insulating film having a thickness of nm is formed.</p> <p>Next, as shown in FIG. 10, N-type impurities are ion-implanted substantially perpendicularly to the silicon single crystal substrate 51 to form shallow source / drain n-type diffusion layers 101. Specifically, for example, arsenic is accelerated at an acceleration voltage of 5 keV to 10 k.eV, dose amount 5×10^{14} / cm² to 1×10^{15} / cm² Inject.</p> <p>As described above, according to this embodiment, the transistors Q1 and Q2 formed in the regions A and B are formed.</p> <p>Are formed of gate insulating films having different physical thicknesses of silicon oxide, while having a physical film thickness sufficient to suppress the direct tunneling current. Due to the difference in the gate insulating film structure, the transistor Q1 in the region A is relatively inferior in gate breakdown voltage and reliability to the transistor Q2 in the region B, but has a characteristic difference in high current driving capability.</p>

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		<p>The gate insulating film has a laminated structure of a high dielectric film and an interface layer formed as a reaction layer between the high dielectric film and the substrate. By changing it, the interface layers of both are different. Moreover, the processing for changing the substrate surface state can be performed using the mask for channel ion implantation in the regions A and B as it is. Therefore, although the transistors Q1 and Q2 have different types of gate insulating film structures, the manufacturing process is simple, with only one additional ion implantation step.</p> <p style="text-align: center;">【図 11】</p> <p>See, e.g., U.S. Pat. No. 8,349,695 to Scheiper et al. (“Scheiper”) at:</p>

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Claim	Claim Language	Exemplary Disclosures in Additional References
		<p>3:42-63: FIG. 1a schematically illustrates a cross-sectional view of a semiconductor device 100 which comprises a substrate 101 and a semiconductor layer 102 formed above the substrate 101. The semiconductor layer 102 is typically provided in the 45 form of a silicon material, as explained above. Moreover, a first semiconductor region 102A and a second semiconductor region or active region 102B are provided in the semiconductor layer 102. The active regions 102A, 102B are to be understood as semiconductor regions in and above 50 which transistor elements are to be formed on the basis of gate electrode structures including a high-k dielectric material. In the example shown, it may be assumed that a gate electrode structure of reduced gate dielectric thickness is to be formed on the semiconductor region 102A, while a gate electrode 55 structure having a gate dielectric material of increased thickness is to be formed on the semiconductor region 102B. Furthermore, in the manufacturing stage shown, a gate dielectric material 151 is selectively formed on the active region 102B and is comprised of silicon dioxide with a specific 60 thickness, for instance with a thickness of several nanometers, depending on the device requirements or any transistors to be formed in and above the semiconductor region 102B.</p> <p>4:27-36: FIG. 1b schematically illustrates the semiconductor device 100 in a further advanced manufacturing phase in which the etch mask 103 is removed and the device 100 is exposed to a cleaning ambient 105 in order to remove contaminants and also to re-grow a thin dielectric base layer 152 on the semiconductor region 102A. For this purpose, a plurality of well established process techniques are available in order to obtain a silicon dioxide material on the basis of a well-controllable growth process.</p> <p>4:37-56: FIG. 1c schematically illustrates the semiconductor device 100 when exposed to a deposition ambient 106 in which a high-k dielectric material. Such as hafnium oxide, is deposited above the active regions 102A, 102B, thereby forming a high-k dielectric layer 153. Thus, the layers 152 and 153 in combination may represent the gate dielectric material of a transistor formed in and above the semiconductor region 102A, thereby providing the required characteristics for high performance transistors, while the layer 153 in combination with the “thick” silicon dioxide material 151 represents the dielectric material for transistors and other circuit elements in which a Superior performance with respect to reduced leakage currents and the like is required. It should be appreciated that the deposition process 106 may</p>

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		<p>be performed on the basis of any appropriate deposition recipe, for instance, by chemical vapor deposition (CVD), physical vapor deposition (PVD) and the like. For example, a thickness of the high-k dielectric layer 153 may be in the range of one to several nanometers, depending on the overall requirements in view of capacitive coupling, leakage currents and the like.</p> <p style="text-align: center;">FIG. 1g (prior art)</p> <p><i>See, e.g., U.S. Pat. No. 7,335,561 to Sakai ("Sakai '561") at:</i></p> <p>[2:31-53] The typical ones of the inventions disclosed in this application will be briefly described as follows. A semiconductor integrated circuit device of the present invention comprising: a semiconductor Substrate; a first MIS transistor including a pair of first semiconductor regions formed in the semiconductor substrate and a first conductive piece formed above the semiconductor Substrate through a first gate insulation film in a region</p>

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		<p>between the pair of the first semiconductor regions; and a second MIS transistor including a pair of second semiconductor regions formed in the semiconductor Substrate and a second conductive piece formed above the semiconductor Substrate through a second gate insulation film in a region between the pair of the second semiconductor regions, wherein the thickness of the first gate insulation film is larger than the thickness of the second gate insulation film and the first gate insulation film is comprised of the first insulation film located on the semiconductor Substrate and the second insulation film located on the first insulation film; and wherein the second gate insulation film is comprised of a third insulation film located on the semiconductor substrate and the dielectric constant of the second and third insulation films is larger than the dielectric constant of the first insulation film.</p> <p>[5:19-22] FIG. 35 is a major part sectional view of a semiconductor substrate showing an example of the manufacturing method of a semiconductor integrated circuit according to an embodiment of the present invention in the order of steps;</p> <p>[6:1-18] An example of the manufacturing method for the semiconductor integrated circuit device according to an embodiment of the present invention will be described using major part sectional views of the semiconductor Substrate shown in FIGS. 1-40. In the Figures, a region A indicates a region in which a gate insulation film having a larger effective thickness is formed and the region B indicates a region in which a gate insulation film having a smaller effective thickness is formed. In the regions A, B, n-channel MIS transistor (hereinafter referred to as low V_{th} NMOS) having a low threshold value voltage (hereinafter referred to as V_{th}), p-channel MIS transistor (hereinafter referred to as low V_{th} PMOS) having a low V_{th}, n-channel MIS transistor (hereinafter referred to as high V_{th} NMOS) having a high V_{th} and p-channel MIS transistor (hereinafter referred to as high V_{th} PMOS) having a high V_{th} are formed and that is, eight kinds of the MIS transistors are formed on the same substrate.</p> <p>[7:60-8:4] Next, after the resist pattern RP10 is removed, as shown in FIG. 16, the protective film 5 is removed and the silicon oxide film 9 is formed on the surface of the semiconductor substrate 1, for example, in the thickness of 4 to 5 nm. The silicon oxide film 9 can be formed according to the thermal CVD method or thermal oxidation method. Meanwhile, the aforementioned silicon oxide film may be turned to silicon nitride film by nitriding the</p>

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		<p>semiconductor substrate 1 thermally. The aforementioned thermal nitration is carried out with the semiconductor 1 heated at about 900° C. in a pressure reduced atmosphere containing nitrogen made radical by plasma discharge</p> <p>[8:5-10] Next, as shown in FIG. 17, after the region A is covered with the resist pattern RP1, as shown in FIG. 18, the silicon oxide film 9 in the region B is removed using diluted HF with resist pattern RP11 as a mask. After that, as shown in FIG. 19, the resist pattern RP11 is removed.</p> <p>[8:11-26] Next, as shown in FIG. 20, high dielectric constant insulation film 10, for example, alumina film is formed on the semiconductor substrate 1. The high dielectric constant insulation film 10 can be deposited according to, for example, spattering method. The thickness of the high dielectric constant insulation film 10 formed on the semiconductor substrate 1 is set so that its effective thickness is about 5 nm. For example, the alumina film is deposited in the thickness of about 10 nm considering dielectric constant. Consequently, gate insulation film 11 comprised of the high dielectric constant insulation film 10 about 5 nm in terms of its effective thickness is formed in the region B and gate insulation film 12 comprised of stacked film of the high dielectric constant film 10 and the silicon oxide film 9 about 9 to 10 nm in terms of its effective thickness is formed in the region A</p> <p>[8:27-31] Before forming the aforementioned high dielectric constant insulation film 10 on the semiconductor substrate 1, silicon oxide film or silicon nitride film, or silicon oxide nitride film less than 1 nm or less may be formed to stabilize an interface with the semiconductor substrate 1.</p> <p>[8:32-34] Next, as shown in FIG. 21, silicon film 13 about 200 nm. thick is deposited on the semiconductor Substrate 1 according to the CVD method.</p> <p>[8:35-39] Next, as shown in FIG.22, after resist pattern 12 is formed in the NMOS formation region in the regions A, B, p-type impurity, for example, boron is ion-implanted into the silicon film 13 in the PMOS formation region in the regions A, B with this resist pattern RP12 as a mask.</p>

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Claim	Claim Language	Exemplary Disclosures in Additional References
		<p>[8:40-46] Next, the resist pattern 12 is removed and as shown in FIG. 23, resist pattern RP13 is formed in the PMOS formation region in the regions A, B. After that, n-type impurity, for example, phosphorus is ion-implanted into the NMOS formation region in the regions A, B with this resist pattern RP13 as a mask.</p> <p>[8:47-55] Next, after the resist pattern RP13 is removed, by per forming heat treatment on the semiconductor Substrate 1, for example at 950° C. for about 60 seconds, the aforementioned n-type impurity and p-type impurity implanted into the silicon film 13 are activated. Further, the silicon film 13 in the NMOS formation region in the regions A, B is turned to n-type silicon polycrystal film and the silicon film 13 in the PMOS formation region in the regions A, B is changed to p-type silicon polycrystal film.</p> <p>[8:56-60] After as shown in FIG. 24, silicon oxide film 14 is deposited on the semiconductor Substrate 1 according to the CVD method, as shown in FIG. 25, resist pattern RP14 is formed to form gate electrodes of the n-channel and p-channel MIS transistor.</p> <p>[8:61-9:3] Next, after as shown in FIG. 26, the silicon oxide film 14 is etched with the resist pattern RP14 as a mask, the resist pattern RP14 is removed. Subsequently, as shown in FIG. 27, with the patterned silicon oxide film 14 as a mask, the silicon film 13 is etched so as to form a gate electrode (conductive piece) 15n comprised of n-type silicon poly crystal film in the NMOS formation region in the regions A, B and a gate electrode (conductive piece) comprised of p-type silicon polycrystal film in the PMOS formation region in the regions A, B</p> <p>[11:5-18] As described above, according to this embodiment, after the silicon oxide film 9 is formed on the surface of the semiconductor substrate 1, the silicon oxide film 9 in the region B (region in which a gate insulation whose effective thickness is small is formed) is removed with diluted HF and after that, by forming high dielectric constant insulation film 10 on the semiconductor Substrate 1, a damage or pollution to the surface of the semiconductor substrate 1 is prevented So as to form two kinds of the gate insulation films, that is, the gate insulation film 12 comprised of stacked film of the high dielectric constant insulation film 10 and the</p>

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Claim	Claim Language	Exemplary Disclosures in Additional References
		<p>silicon oxide film 9 and the gate insulation film 11 comprised of the high dielectric constant insulation film 10 on the same semiconductor Substrate 1.</p> <p>[11:19-24] Because the gate insulation film 12 in the region A is comprised of stacked film of the high dielectric constant insulation film 10 and the silicon oxide film 9, the difference in level between the region A and region B can be reduced compared to the stacked film comprised of two high dielectric constant insulation films.</p> <p>[11:25-30] Further because the thickness of the silicon oxide film 9 can be reduced as compared to a case where the gate insulation film 12 in the region A is comprised of only the silicon oxide film, oxidation of the interior of the isolation groove 4a can be suppressed so that stress at an end portion of the isolation groove 4a can be reduced.</p>

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		<p style="text-align: center;">FIG. 35</p> <p>See, e.g., U.S. Pat. App. Pub. No. 2009/0039445 to Wu ("Wu '445") at:</p> <p>[0018] Still referring to FIG. 1A, the gate structures 12A and 12B may be formed by conventional CVD deposition, lithographic patterning, and plasma (dry) etching methods known in the art. The gate dielectric portions 14A and 14B may be formed by any process known in the art, e.g., thermal oxidation, nitridation, sputter deposition, chemical vapor deposition, or combinations thereof. The gate dielectric portions 14A and 14B may be formed of silicon oxide, silicon nitride, silicon oxynitride, and high-K dielectrics (e.g., $K > 8$) including transition metal oxide and rare earth metal oxides. For example, high-K dielectrics may be</p>

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		<p>formed of aluminum oxides (e.g., Al₂O₃), hafnium oxides (e.g., HfO₂), hafnium oxynitrides (HfON), hafnium silicates (e.g. HfSiO₄), hafnium silicon oxynitrides (e.g., HfSi_xO_yN_z), zirconium oxides (e.g., ZrO₂), zirconium oxynitrides (e.g., ZrON), zirconium silicon oxides (e.g., ZrSiO₂), yttrium oxides (Y₂O₃), lanthanum oxides (La₂O₃), cerium oxides (CeO₂), titanium oxides (TiO₂), tantalum oxides (Ta₂O₅), or combinations thereof. The high-k dielectric layer may be formed by known CVD methods such as atomic layer CVD (ALCVD) and metal-organic CVD (MOCVD). It will be appreciated that the high-K dielectric layer may include a lowermost interfacial layer formed on the semiconductor substrate such as an oxide or oxynitride (not shown).</p> <p><i>See 1[c], [d]</i></p>

Claim	Claim Language	Exemplary Disclosures in Additional References
1 [f]	the first interface layer has a thickness larger than that of the second interface layer, and	<p>The following references disclose and/or render obvious a “the first interface layer has a thickness larger than that of the second interface layer, and” as further described below.</p> <p><i>See, e.g., U.S. Pat. No. 6,787,421 to Gilmer et al. (“Gilmer”) at:</i></p> <p>[Abstract] A semiconductor device (10) having two different gate dielectric thicknesses is formed using a single high-k dielectric layer, preferably a metal oxide. A thicker first gate dielectric (16) is formed in a region of the device for higher voltage requirements, e.g. an I/O region (24). A thinner Second gate dielectric (20) is formed in a region of the device for lower Voltage requirements, e.g. a core device region (22). First and Second dielectrics are preferably Silicon dioxide or oxynitride. A metal oxide (26) is deposited over both dielectrics, followed by deposition of a gate electrode material (28). By using a single metal oxide layer in forming the gate dielectric Stack for each transistor, together with high quality Silicon dioxide or oxynitride dielectric layers, problems associated with Selective etching of the metal oxide may be avoided, as may problems associated with various interfaces between the metal oxide and damaged or treated surfaces.</p>

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Claim	Claim Language	Exemplary Disclosures in Additional References
		<p>[1:56-61] FIGS. 1-4 illustrate partial cross-sectional views of a semiconductor device formed to have two gate dielectric thickness (e.g. one for core devices and one for I/O devices) as it undergoes processing in accordance with one embodiment of the present invention;</p> <p>[2:13-38] The present invention integrates a high-k dielectric material, preferably a metal oxide, in a dual gate process Sequence using a Single metal oxide deposition to form multiple gate dielectric Stacks of differing thicknesses. With the present invention, the metal oxide is formed over prepared Surfaces of the Substrate that already provide a difference in equivalent oxide thickness (EOT) between two different regions of the Substrate (e.g. the core logic region and the I/O region). For example, a single metal oxide layer is deposited over two different thicknesses of silicon dioxide or Silicon oxynitride. Thus, the metal oxide need not be etched selective to the underlying Silicon Substrate (which can damage the Substrate Surface) where a gate quality Surface is required. Also with the invention, the Single metal oxide layer forms an interface with a high quality Silicon dioxide or Silicon Oxynitride layer, as opposed to an interface with a Silicon Surface which has been damaged or otherwise treated as a result of using conventional DGO processing methods with a metal oxide dielectric. Thus, devices formed in accordance with the invention do not Suffer from degraded performance, e.g. current leakage, due to interface irregularities as a result of contamination or damaged Surfaces.</p> <p>[2:36-55] Referring now to FIGS. 1-4, a semiconductor device 10 is fabricated in accordance with one embodiment of the invention. Referring now to FIGS. 1-4, a semiconductor device 10 is fabricated in accordance with one embodiment of the invention. As shown in FIG. 1, semiconductor device 10 includes a Semiconductor Substrate 12 which in a preferred embodiment is a single crystal Silicon Substrate (also sometimes referred to as a wafer), but which can instead be formed from other Semiconductor Substrate materials. Within substrate 12, trench isolation regions 14, preferably shallow trench isolation regions, are formed in a conventional manner for the purpose of electrically isolating different individual devices to be formed. After forming trench isolation regions 14, a first gate dielectric 16 is formed over substrate 12. First gate dielectric 16 is preferably silicon dioxide or silicon oxynitride, and is preferably formed by thermal oxidation in accordance with conventional practices. The thickness of gate dielectric 16 is determined by the particular device requirements for devices to</p>

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		<p>be formed in I/O device region 24 as further explained below, but generally will be within a range of 30–50 Angstroms (3–5 nanometers).</p> <p>[3:7-33] Semiconductor device 10 is then etched to remove unprotected portions of first gate dielectric 16 in core device region 22, as shown in FIG. 2. The resist mask 18 is then removed and a Second gate dielectric 20 is formed on exposed portions of Substrate 12 within the core device region 22. In a preferred embodiment, second gate dielectric 20 is also silicon dioxide or silicon oxynitride, but like first gate dielectric 16 other materials could be used. This Second gate dielectric can be formed by thermal oxidation and/or chemical oxidation in accordance with conventional practices. The thickness of gate dielectric 20 is also determined by the particular device requirements for devices to be formed in core device region 22 as further explained below, but generally will be within a range of 4-12 Angstroms (0.4-1.2 nanometers). Because Second gate dielectric 20 is So thin, it may be difficult to adequately control the thickness or obtain an oxide of Sufficient quality using thermal oxidation processes and therefore chemical oxidation may be useful. For instance, the thin dielectric may be formed by growing a thin oxide by rinsing the substrate in ozonated water. A combination of thermal and chemical treatment may also be used to form second dielectric 20. It may also be sufficient for second gate dielectric 20 to be a native oxide which is grown on Substrate 12 as a result of exposing the Substrate to ambient or other oxygen containing environment. In other embodiments, second gate dielectric 20 can be deposited, e.g., by atomic layer deposition.</p> <p>[3:34-43] In the course of forming Second gate dielectric 20, the thickness of first gate dielectric 16 may change, depending on the technique used to form the Second gate dielectric 20, and should be taken into account in choosing the initial deposited or grown thickness of first gate dielectric 16. Generally, however, it is not anticipated that the thickness of first gate dielectric 16 will change Significantly unless second gate dielectric 20 is deposited over first gate dielectric 16 rather than forming it through a thermal or chemical reaction of the Substrate Surface.</p> <p>[3:44-4:7] Now that gate dielectrics of two different thicknesses have been formed, a high-k dielectric (generally with $k > 4$, preferably with $k > 6$, and most preferably with $k > 7$) is deposited over semiconductor device 10. In a preferred embodiment, this high-k dielectric is a metal oxide, Such as metal oxide 26 shown in FIG. 3. Suitable materials for metal oxide 26 preferably include</p>

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		<p>hafnium oxide (HfO₂), hafnium silicate (Hf_xSi_{1-x}O₂), or lanthanum aluminate (LaAlO₃), but lanthanum oxide, hafnium aluminate, Zirconium oxide, and Zirconium Silicate, and other like materials, may also be Suitable high-k dielectrics. The thickness of the high-k dielectric layer will be dependent on the particular device requirements in each region of the Substrate (the core region and the I/O region), but generally it is believed the thickness of a metal oxide will be between about 15-50 angstroms (1.5-5.0 nanometers). The underlying thicknesses of first gate dielectric 16 and Second gate dielectric 20 will also affect the choice of thickness of the high-k dielectric. The thickness of the high-k dielectric should be chosen So that its equivalent oxide thickness (EOT), when added to the EOT of the first gate dielectric 16 (I/O device dielectric) thickness or Second gate dielectric 20 (core device dielectric) thickness, provides a total EOT appropriate for the I/O and core device, respectively. Similarly, this calculation should be used to determine the initial deposited or grown thicknesses of the first and Second gate dielectrics. Because metal oxide 26 is deposited as a single blanket deposition, its thickness will not vary much across the Substrate Surface and thus one should use the thicknesses of the first and Second dielectrics as the “variables” to achieve the final EOTs for the core and I/O devices.</p> <p>[Claim 1] A method for forming a semiconductor device comprising: providing a semiconductor substrate; forming a first gate dielectric layer overlying the semiconductor substrate, the first gate dielectric layer having a first thickness in a range of 30–50 Angstroms, removing a portion of the first gate dielectric layer over lying a first region of the semiconductor substrate; forming a second gate dielectric layer overlying the first region of the semiconductor substrate, the second gate dielectric layer having a Second thickness less than the first thickness, and forming a metal oxide layer overlying the first gate dielectric layer and the Second gate dielectric layer.</p>

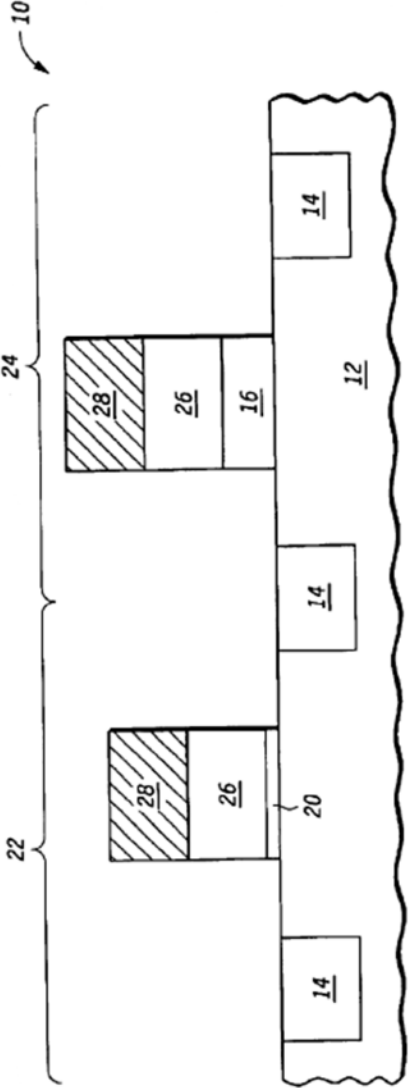
Claim	Claim Language	Exemplary Disclosures in Additional References
		<div></div> <p><i>FIG. 4</i></p> <p>See, e.g., Japanese Patent App. Pub. No. JP2006/060155 to Yasuhira et al. (“Yasuhira”) at:</p> <p>Hereinafter, some of the embodiments of the present invention will be described in detail with reference to the drawings. (Embodiment 1)</p> <p>An n-well layer 2 is formed on the surface portion of the p-conductivity type silicon substrate 1, an STI element isolation region 3 is formed on the surface portion of the n-well layer 2, and a base oxide film 4 of about 5 nm is formed on the surface of the silicon substrate 1. It is formed by thermal oxidation. (FIG. 2 (a)).</p> <p>On the other hand, in the MISFET of the internal circuit portion, the base film 12 with a film thickness of about 1 nm and the nitride layer 12a whose surface is modified to a nitrogen-containing layer, the High-k film 5 and the nitride layer which is a modified layer on the surface thereof A second gate insulating film 13 is formed by the laminated film 5 a, and the above-described polycrystalline silicon layer 7 and silicide layer 8 are provided on the second gate</p>

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		<p>insulating film 13. Sidewall insulating films 10 are provided on the side walls of the second gate insulating film 13 and the gate electrode 9, and source / drain regions including the source / drain diffusion layers 11 and the silicide layers 8 are provided on the surface of the n-well layer 2. It has been. In the second gate insulating film 13 of the MISFET, the base film 12 has a silicon oxide film structure as a basic structure, and is interposed between the high-k film 5 and the silicon substrate 1 on the surface of the n-well layer 2. It has functions such as preventing boron penetration and improving the surface mobility of carrier charges (holes).</p> <p>Next, a method for manufacturing the semiconductor device according to the present invention will be described with reference to FIGS. Here, the same components as those in FIG. 1 are denoted by the same reference numerals.</p> <p>In the MISFET constituting the input / output circuit of the semiconductor device manufactured as described above, the first gate insulating film 6 having a converted film thickness of about 5 nm is formed. In the MISFET forming the internal circuit of the semiconductor device, the converted film thickness is formed. A second gate insulating film 13 having a thickness of about 1 nm is formed. Then, MISFETs having gate insulating films having different electrical thicknesses are formed on the silicon substrate 1.</p> <p>Then, without leaving time, thermal oxidation in a dilute oxygen atmosphere or plasma oxidation at a low temperature (for example, 300 ° C. temperature) is performed to form the base film 12 having a film thickness of about 1 nm. Here, the base film 12 is a silicon oxide film (FIG. 2C).</p>

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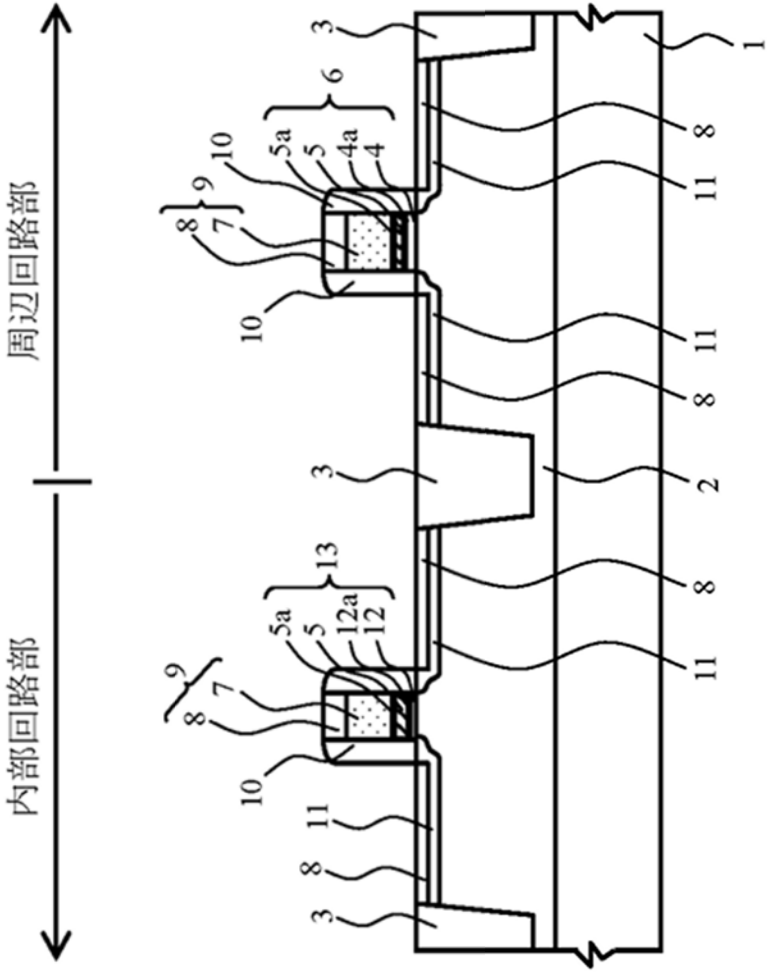
Claim	Claim Language	Exemplary Disclosures in Additional References
		<p>【図 1】</p>  <p>内部回路部</p> <p>周辺回路部</p> <p>See, e.g., Japanese Patent App. Pub. No. JP2003/100896 to Fujiwara et al. (“Fujiwara”) at:</p> <p>[0013] A semiconductor device according to the present invention comprises a semiconductor substrate and a first substrate divided into the semiconductor substrate.</p> <p>A first transistor having a first gate insulating film having a structure in which a first insulating film and a second insulating film are stacked in this order from the semiconductor substrate, and</p>

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		<p>are divided into the semiconductor substrate. The third insulating film and the fourth insulating film formed in the second region are stacked in this order from the semiconductor substrate, and the silicon oxide film is formed as compared with the first gate insulating film. A second transistor having a second gate insulating film having a large converted film thickness, and the second and fourth transistors.</p> <p>The insulating film of is a high-dielectric film formed at the same time.</p> <p>And the third insulating film are interface layers having different compositions or film thicknesses from each other. Particularly preferably, the first and third insulating films are interface layers having different compositions from each other formed by the reaction between the second and third insulating films and the semiconductor substrate or the thin film formed on the surface thereof. I shall.</p> <p>Next, a sacrificial oxide film 61 is formed by dilute hydrofluoric acid treatment.</p> <p>Was removed, after performing the hydrogen-terminated silicon substrate 51 surface, as shown in FIG. 8, TiO₂ is a high dielectric film</p> <p>The film 81 is formed. Specifically, the TiO₂ film 81 having a thickness of 5 nm is formed by the DC sputtering method using a TiO₂ sintered target under the sputtering conditions of power 300 W, pressure 1 Pa, Ar / O₂ flow rate 22 / 1.2 sccm. . At this time, the surface of the silicon substrate in the regions A and B is oxidized by the oxygen plasma atmosphere during the sputtering of the TiO₂ film, and the interface layers 82 and 83 are formed. The interface layer 82 in the region A has the result that the nitrogen introduction region 64 suppresses the diffusion of oxygen into the substrate.</p> <p>It becomes a thin silicon oxide film, and the interface layer 83 in the region B becomes a thicker silicon oxide film.</p> <p>A polycrystalline silicon film having a thickness of 175 n is formed on the upper surface by a CVD method.</p> <p>A gate electrode 91 is formed by forming a film and performing patterning. Along with the gate electrode 91, the TiO₂ film 81 and the interface layers 82 and 83 which will be the gate insulating film thereunder are also patterned. After that, in order to crystallize the TiO₂ film 81, RTA with a heat treatment temperature of 900 ° C. and a heat treatment time of 30 seconds is performed.</p>

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		<p>Do. At this time, the surface of the silicon substrate in the region B is oxidized by the diffusion of oxygen from the TiO 2 film 81 to the silicon substrate 51 by RTA, and the interface layer 83 grows to finally become the interface layer 83a of about 2 nm. In the region A, the nitrogen introduction region 64 suppresses the diffusion of oxygen into the substrate, The growth of the interface layer 82 is suppressed, and finally about 0.7 nm. The interface layer 82a has a thickness of nm.</p> <p style="text-align: center;">【 図 1 1 】</p> <p>The diagram illustrates a cross-sectional view of a semiconductor device. It shows a central barrier region (51) flanked by two main regions, A and B. Region A (left) consists of a p-type substrate (p) with an n+ layer (n+) and a TiO2 film (81) on top. Region B (right) consists of an n+ layer (n+) with a TiO2 film (81) on top. The interface layer (82) is shown in both regions, with 82a in region A and 83a in region B. The diagram includes labels for various layers (51, 52, 53, 54, 63, 64, 72, 101, 111, 112, 91, Q1, Q2) and dimensions (A, B).</p>

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		<p><i>See, e.g.</i>, U.S. Pat. No. 8,349,695 to Scheiper et al. (“Scheiper”) at:</p> <p>3:24-62: In addition to enhancing performance of gate electrode structures by incorporating a high-k dielectric material in 25 Sophisticated semiconductor devices, frequently, transistor elements of different characteristics, for instance of different leakage behavior, have to be provided, thereby requiring a gate dielectric material of different material composition and/or of different thickness. In some conventional approaches, 30 the high-k dielectric material in combination with any work function adjusting species are provided in an early manufacturing stage, wherein a different thickness of the gate dielectric material may also be provided in different device regions in order to provide different transistor types, or any other 35 circuit elements, such as polysilicon resistors and the like. It turns out, however, that the conventional process strategy for providing gate electrode structures with differently composed gate dielectrics may result in significant threshold Voltage variations, as will be described in more detail with reference to FIGS. 1a-1g.</p> <p>3:42-63: FIG. 1a schematically illustrates a cross-sectional view of a semiconductor device 100 which comprises a substrate 101 and a semiconductor layer 102 formed above the substrate 101. The semiconductor layer 102 is typically provided in the form of a silicon material, as explained above. Moreover, a first semiconductor region 102A and a second semiconductor region or active region 102B are provided in the semiconductor layer 102. The active regions 102A, 102B are to be understood as semiconductor regions in and above 50 which transistor elements are to be formed on the basis of gate electrode structures including a high-k dielectric material. In the example shown, it may be assumed that a gate electrode structure of reduced gate dielectric thickness is to be formed on the semiconductor region 102A, while a gate electrode 55 structure having a gate dielectric material of increased thickness is to be formed on the semiconductor region 102B. Furthermore, in the manufacturing stage shown, a gate dielectric material 151 is selectively formed on the active region 102B and is comprised of silicon dioxide with a specific 60 thickness, for instance with a thickness of several nanometers, depending on the device requirements or any transistors to be formed in and above the semiconductor region 102B.</p>

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		<p>4:27-36: FIG. 1b schematically illustrates the semiconductor device 100 in a further advanced manufacturing phase in which the etch mask 103 is removed and the device 100 is exposed to a cleaning ambient 105 in order to remove contaminants and also to re-grow a thin dielectric base layer 152 on the semiconductor region 102A. For this purpose, a plurality of well established process techniques are available in order to obtain a silicon dioxide material on the basis of a well-controllable growth process.</p> <p>4:37-56: FIG. 1c schematically illustrates the semiconductor device 100 when exposed to a deposition ambient 106 in which a high-k dielectric material. Such as hafnium oxide, is deposited above the active regions 102A, 102B, thereby forming a high-k dielectric layer 153. Thus, the layers 152 and 153 in combination may represent the gate dielectric material of a transistor formed in and above the semiconductor region 102A, thereby providing the required characteristics for high performance transistors, while the layer 153 in combination with the “thick” silicon dioxide material 151 represents the dielectric material for transistors and other circuit elements in which a Superior performance with respect to reduced leakage currents and the like is required. It should be appreciated that the deposition process 106 may be performed on the basis of any appropriate deposition recipe, for instance, by chemical vapor deposition (CVD), physical vapor deposition (PVD) and the like. For example, a thickness of the high-k dielectric layer 153 may be in the range of one to several nanometers, depending on the overall requirements in view of capacitive coupling, leakage currents and the like.</p>

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Claim Language		<p>FIG. 1g (prior art)</p>
Claim		<p>See, e.g., U.S. Pat. No. 7,335,561 to Sakai ("Sakai '561") at: [2:31-53] The typical ones of the inventions disclosed in this application will be briefly described as follows. A semiconductor integrated circuit device of the present invention comprising: a semiconductor Substrate; a first MIS transistor including a pair of first semiconductor regions formed in the semiconductor substrate and a first conductive piece formed above the semiconductor Substrate through a first gate insulation film in a region between the pair of the first semiconductor regions; and a second MIS transistor including a pair of second semiconductor regions formed in the semiconductor Substrate and a second conductive piece formed above the semiconductor Substrate through a second gate insulation film in a region</p>

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		<p>between the pair of the second semiconductor regions, wherein the thickness of the first gate insulation film is larger than the thickness of the second gate insulation film and the first gate insulation film is comprised of the first insulation film located on the semiconductor Substrate and the second insulation film located on the first insulation film; and wherein the second gate insulation film is comprised of a third insulation film located on the semiconductor substrate and the dielectric constant of the second and third insulation films is larger than the dielectric constant of the first insulation film.</p> <p>[5:19-22] FIG. 35 is a major part sectional view of a semiconductor substrate showing an example of the manufacturing method of a semiconductor integrated circuit according to an embodiment of the present invention in the order of steps;</p> <p>[6:1-18] An example of the manufacturing method for the semiconductor integrated circuit device according to an embodiment of the present invention will be described using major part sectional views of the semiconductor Substrate shown in FIGS. 1-40. In the Figures, a region A indicates a region in which a gate insulation film having a larger effective thickness is formed and the region B indicates a region in which a gate insulation film having a smaller effective thickness is formed. In the regions A, B, n-channel MIS transistor (hereinafter referred to as low V_{th} NMOS) having a low threshold value voltage (hereinafter referred to as V_{th}), p-channel MIS transistor (hereinafter referred to as low V_{th} PMOS) having a low V_{th}, n-channel MIS transistor (hereinafter referred to as high V_{th} NMOS) having a high V_{th} and p-channel MIS transistor (hereinafter referred to as high V_{th} PMOS) having a high V_{th} are formed and that is, eight kinds of the MIS transistors are formed on the same substrate.</p> <p>[7:60-8:4] Next, after the resist pattern RP10 is removed, as shown in FIG. 16, the protective film 5 is removed and the silicon oxide film 9 is formed on the surface of the semiconductor substrate 1, for example, in the thickness of 4 to 5 nm. The silicon oxide film 9 can be formed according to the thermal CVD method or thermal oxidation method. Meanwhile, the aforementioned silicon oxide film may be turned to silicon nitride film by nitriding the semiconductor substrate 1 thermally. The aforementioned thermal nitration is carried out with the semiconductor 1 heated at about 900° C. in a pressure reduced atmosphere containing nitrogen made radical by plasma discharge</p>

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		<p>[8:5-10] Next, as shown in FIG. 17, after the region A is covered with the resist pattern RP1, as shown in FIG. 18, the silicon oxide film 9 in the region B is removed using diluted HF with resist pattern RP11 as a mask. After that, as shown in FIG. 19, the resist pattern RP11 is removed.</p> <p>[8:11-26] Next, as shown in FIG. 20, high dielectric constant insulation film 10, for example, alumina film is formed on the semiconductor substrate 1. The high dielectric constant insulation film 10 can be deposited according to, for example, sputtering method. The thickness of the high dielectric constant insulation film 10 formed on the semiconductor substrate 1 is set so that its effective thickness is about 5 nm. For example, the alumina film is deposited in the thickness of about 10 nm considering dielectric constant. Consequently, gate insulation film 11 comprised of the high dielectric constant insulation film 10 about 5 nm in terms of its effective thickness is formed in the region B and gate insulation film 12 comprised of stacked film of the high dielectric constant film 10 and the silicon oxide film 9 about 9 to 10 nm in terms of its effective thickness is formed in the region A</p> <p>[8:27-31] Before forming the aforementioned high dielectric constant insulation film 10 on the semiconductor substrate 1, silicon oxide film or silicon nitride film, or silicon oxide nitride film less than 1 nm or less may be formed to stabilize an interface with the semiconductor substrate 1.</p> <p>[8:32-34] Next, as shown in FIG. 21, silicon film 13 about 200 nm. thick is deposited on the semiconductor Substrate 1 according to the CVD method.</p> <p>[8:35-39] Next, as shown in FIG.22, after resist pattern 12 is formed in the NMOS formation region in the regions A, B, p-type impurity, for example, boron is ion-implanted into the silicon film 13 in the PMOS formation region in the regions A, B with this resist pattern RP12 as a mask.</p> <p>[8:40-46] Next, the resist pattern 12 is removed and as shown in FIG. 23, resist pattern RP13 is formed in the PMOS formation region in the regions A, B. After that, n-type impurity, for</p>

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		<p>example, phosphorus is ion-implanted into the NMOS formation region in the regions A, B with this resist pattern RP13 as a mask.</p> <p>[8:47-55] Next, after the resist pattern RP13 is removed, by per forming heat treatment on the semiconductor Substrate 1, for example at 950° C. for about 60 seconds, the aforementioned n-type impurity and p-type impurity implanted into the silicon film 13 are activated. Further, the silicon film 13 in the NMOS formation region in the regions A, B is turned to n-type silicon polycrystal film and the silicon film 13 in the PMOS formation region in the regions A, B is changed to p-type silicon polycrystal film.</p> <p>[8:56-60] After as shown in FIG. 24, silicon oxide film 14 is deposited on the semiconductor Substrate 1 according to the CVD method, as shown in FIG. 25, resist pattern RP14 is formed to form gate electrodes of the n-channel and p-channel MIS transistor.</p> <p>[8:61-9:3] Next, after as shown in FIG. 26, the silicon oxide film 14 is etched with the resist pattern RP14 as a mask, the resist pattern RP14 is removed. Subsequently, as shown in FIG. 27, with the patterned silicon oxide film 14 as a mask, the silicon film 13 is etched so as to form a gate electrode (conductive piece) 15n comprised of n-type silicon poly crystal film in the NMOS formation region in the regions A, B and a gate electrode (conductive piece) comprised of p-type silicon polycrystal film in the PMOS formation region in the regions A, B</p> <p>[11:5-18] As described above, according to this embodiment, after the silicon oxide film 9 is formed on the surface of the semiconductor substrate 1, the silicon oxide film 9 in the region B (region in which a gate insulation whose effective thickness is small is formed) is removed with diluted HF and after that, by forming high dielectric constant insulation film 10 on the semiconductor Substrate 1, a damage or pollution to the surface of the semiconductor substrate 1 is prevented So as to form two kinds of the gate insulation films, that is, the gate insulation film 12 comprised of stacked film of the high dielectric constant insulation film 10 and the silicon oxide film 9 and the gate insulation film 11 comprised of the high dielectric constant insulation film 10 on the same semiconductor Substrate 1.</p>

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		<p>[11:19-24] Because the gate insulation film 12 in the region A is comprised of stacked film of the high dielectric constant insulation film 10 and the silicon oxide film 9, the difference in level between the region A and region B can be reduced compared to the stacked film comprised of two high dielectric constant insulation films.</p> <p>[11:25-30] Further because the thickness of the silicon oxide film 9 can be reduced as compared to a case where the gate insulation film 12 in the region A is comprised of only the silicon oxide film, oxidation of the interior of the isolation groove 4a can be suppressed so that stress at an end portion of the isolation groove 4a can be reduced.</p> <p>[11:31-32] Next, an example of an inverter circuit applying an embodiment of the present invention is shown in FIG. 41.</p> <p>[11:33-46] In the same Figure, a region Surrounded by dotted lines indicates a CMOS inverter and Tkp and Tnp denote p-channel MIS transistor while Tkn and Tnn denote n-channel MIS transistor. The gate insulation film of the MIS transistors Tnp, Tnn constituting the CMOS inverter is thinner than the gate insulation film of the MIS transistors Tkp, Tkn. For example, the gate insulation film of the MIS transistors Tnp, Tnn constituting the CMOS inverter is formed of high dielectric constant insulation film and its effective thickness is about 3.5 nm. The gate insulation film of the MIS transistors Tkp, Tkn is constituted of stacked film of high dielectric constant insulation film and silicon oxide film and its effective thickness is about 6 nm.</p> <p>[13:20-37] Because the gate insulation film comprised of stacked film of high dielectric constant insulation film and silicon oxide film and the gate insulation film comprised of the high dielectric constant insulation film can be formed on the same semiconductor Substrate so as to Suppress damage or pollution to the surface of the semiconductor substrate, plural gate insulation films each having a different thickness and a high reliability can be formed. Further, because the gate insulation film having a high effective thickness is constituted of stacked film of the high dielectric constant insulation film and silicon oxide film, a difference in step between a region in which the gate insulation film having a large effective thickness is formed and a region in which the gate insulation film having a small effective thickness is decreased as compared to a stacked</p>

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		<p>film in which two high dielectric constant insulation films are stacked, so that subsequent manufacturing of the MIS transistor is facilitated.</p> <p>[Claim 1] 1. A method of manufacturing a semiconductor integrated circuit device comprising the steps of (a) forming a first insulation film over a surface of a semiconductor Substrate in a first region and a second region different from said first region of said semiconductor substrate; (b) selectively removing said first insulation film in said second region, with said first insulation film being left in said first region; (c) forming a second insulation film over said semiconductor Substrate of said second region; (d) forming a third insulation film over said first insulation film in said first region and over said second insulation film in said second region; (e) forming a first conductive layer over said third insulation film; and (f) forming a first conductive piece in said first region and a second conductive piece in said second region by patterning said first conductive layer, wherein the thickness of said first insulation film is larger than the thickness of said second insulation film; said first insulation film includes silicon and at least one of oxygen and nitrogen; said second insulation film includes silicon and at least one of oxygen and nitrogen; said third insulation film has a greater dielectric constant than each of said first and second insulation films; and the thickness of said third insulation film is larger than the thickness of said first insulation film and said second insulation film</p>

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		<p>[Abstract] A semiconductor device (10) having two different gate dielectric thicknesses is formed using a single high-k dielectric layer, preferably a metal oxide. A thicker first gate dielectric (16) is formed in a region of the device for higher voltage requirements, e.g. an I/O region (24). A thinner Second gate dielectric (20) is formed in a region of the device for lower Voltage requirements, e.g. a core device region (22). First and Second dielectrics are preferably Silicon dioxide or oxynitride. A metal oxide (26) is deposited over both dielectrics, followed by deposition of a gate electrode material (28). By using a single metal oxide layer in forming the gate dielectric Stack for each transistor, together with high quality Silicon dioxide or oxynitride dielectric layers, problems associated with Selective etching of the metal oxide may be avoided, as may problems associated with various interfaces between the metal oxide and damaged or treated surfaces.</p> <p>[2:13-38] The present invention integrates a high-k dielectric material, preferably a metal oxide, in a dual gate process Sequence using a Single metal oxide deposition to form multiple gate dielectric Stacks of differing thicknesses. With the present invention, the metal oxide is formed over prepared Surfaces of the Substrate that already provide a difference in equivalent oxide thickness (EOT) between two different regions of the Substrate (e.g. the core logic region and the I/O region). For example, a single metal oxide layer is deposited over two different thicknesses of silicon dioxide or Silicon oxynitride. Thus, the metal oxide need not be etched selective to the underlying Silicon Substrate (which can damage the Substrate Surface) where a gate quality Surface is required. Also with the invention, the Single metal oxide layer forms an interface with a high quality Silicon dioxide or Silicon Oxynitride layer, as opposed to an interface with a Silicon Surface which has been damaged or otherwise treated as a result of using conventional DGO processing methods with a metal oxide dielectric. Thus, devices formed in accordance with the invention do not Suffer from degraded performance, e.g. current leakage, due to interface irregularities as a result of contamination or damaged Surfaces.</p> <p>[2:36-55] Referring now to FIGS. 1-4, a semiconductor device 10 is fabricated in accordance with one embodiment of the invention. Referring now to FIGS. 1-4, a semiconductor device 10 is fabricated in accordance with one embodiment of the invention. As shown in FIG. 1, semiconductor device 10 includes a Semiconductor Substrate 12 which in a preferred embodiment is a single crystal Silicon Substrate (also sometimes referred to as a wafer), but</p>

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		<p>which can instead be formed from other Semiconductor Substrate materials. Within substrate 12, trench isolation regions 14, preferably shallow trench isolation regions, are formed in a conventional manner for the purpose of electrically isolating different individual devices to be formed. After forming trench isolation regions 14, a first gate dielectric 16 is formed over substrate 12. First gate dielectric 16 is preferably silicon dioxide or silicon oxynitride, and is preferably formed by thermal oxidation in accordance with conventional practices. The thickness of gate dielectric 16 is determined by the particular device requirements for devices to be formed in I/O device region 24 as further explained below, but generally will be within a range of 30–50 Angstroms (3-5 nanometers).</p> <p>[2:56-3:6] After forming first gate dielectric 16, a (photo)resist mask 18 is formed over the substrate to mask off a portion of the first gate dielectric layer. AS shown in FIG. 1, Semiconductor device 10 includes two different device regions, namely a core device region 22 and an I/O device region 24. In operation, devices to be formed in core device region 22 require thinner gate dielectrics that operate at lower Voltages than, e.g., I/O devices to be formed in I/O device region 24 that can withstand higher Voltages required for I/O functions. Accordingly, resist mask 18 is formed to protect the portion of first gate dielectric 16 which will Serve, in part, as a gate dielectric for the higher Voltage I/O devices. Other dielectric materials may instead be used for first gate dielectric 16. Silicon dioxide and silicon oxynitride are attractive choices because of the industry's understanding of these materials, the ability to form high gate quality films, and because they can be formed by Selective growth techniques rather than requiring blanket depositions and etch steps.</p> <p>[3:7-33] Semiconductor device 10 is then etched to remove unprotected portions of first gate dielectric 16 in core device region 22, as shown in FIG. 2. The resist mask 18 is then removed and a Second gate dielectric 20 is formed on exposed portions of Substrate 12 within the core device region 22. In a preferred embodiment, second gate dielectric 20 is also silicon dioxide or silicon oxynitride, but like first gate dielectric 16 other materials could be used. This Second gate dielectric can be formed by thermal oxidation and/or chemical oxidation in accordance with conventional practices. The thickness of gate dielectric 20 is also determined by the particular device requirements for devices to be formed in core device region 22 as further explained below, but generally will be within a range of 4-12 Angstroms (0.4-1.2 nanometers). Because Second</p>

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		<p>base oxide film 4 of about 5 nm is formed on the surface of the silicon substrate 1. It is formed by thermal oxidation. (FIG. 2 (a)).</p> <p>On the other hand, in the MISFET of the internal circuit portion, the base film 12 with a film thickness of about 1 nm and the nitride layer 12a whose surface is modified to a nitrogen-containing layer, the High-k film 5 and the nitride layer which is a modified layer on the surface thereof A second gate insulating film 13 is formed by the laminated film 5 a, and the above-described polycrystalline silicon layer 7 and silicide layer 8 are provided on the second gate insulating film 13. Sidewall insulating films 10 are provided on the side walls of the second gate insulating film 13 and the gate electrode 9, and source / drain regions including the source / drain diffusion layers 11 and the silicide layers 8 are provided on the surface of the n-well layer 2. It has been. In the second gate insulating film 13 of the MISFET, the base film 12 has a silicon oxide film structure as a basic structure, and is interposed between the high-k film 5 and the silicon substrate 1 on the surface of the n-well layer 2. It has functions such as preventing boron penetration and improving the surface mobility of carrier charges (holes).</p> <p>Next, a method for manufacturing the semiconductor device according to the present invention will be described with reference to FIGS. Here, the same components as those in FIG. 1 are denoted by the same reference numerals.</p> <p>In the MISFET constituting the input / output circuit of the semiconductor device manufactured as described above, the first gate insulating film 6 having a converted film thickness of about 5 nm is formed. In the MISFET forming the internal circuit of the semiconductor device, the converted film thickness is formed. A second gate insulating film 13 having a thickness of about 1 nm is formed. Then, MISFETs having gate insulating films having different electrical thicknesses are formed on the silicon substrate 1.</p> <p>Then, without leaving time, thermal oxidation in a dilute oxygen atmosphere or plasma oxidation at a low temperature (for example, 300 ° C. temperature) is performed to form the base film 12 having a film thickness of about 1 nm. Here, the base film 12 is a silicon oxide film (FIG. 2C).</p>

Claim	Claim Language	Exemplary Disclosures in Additional References
		<p>【図 1】</p> <p>内部回路部</p> <p>周辺回路部</p> <p>See, e.g., Japanese Patent App. Pub. No. JP2003/100896 to Fujiwara et al. (“Fujiwara”) at:</p> <p>[0013] A semiconductor device according to the present invention comprises a semiconductor substrate and a first substrate divided into the semiconductor substrate.</p> <p>A first transistor having a first gate insulating film having a structure in which a first insulating film and a second insulating film are stacked in this order from the semiconductor substrate, and are divided into the semiconductor substrate. The third insulating film and the fourth insulating</p>

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Claim	Claim Language	Exemplary Disclosures in Additional References
		<p>film formed in the second region are stacked in this order from the semiconductor substrate, and the silicon oxide film is formed as compared with the first gate insulating film. A second transistor having a second gate insulating film having a large converted film thickness, and the second and fourth transistors.</p> <p>The insulating film of is a high-dielectric film formed at the same time.</p> <p>And the third insulating film are interface layers having different compositions or film thicknesses from each other. Particularly preferably, the first and third insulating films are interface layers having different compositions from each other formed by the reaction between the second and third insulating films and the semiconductor substrate or the thin film formed on the surface thereof. I shall.</p> <p>Next, a sacrificial oxide film 61 is formed by dilute hydrofluoric acid treatment.</p> <p>Was removed, after performing the hydrogen-terminated silicon substrate 51 surface, as shown in FIG. 8, TiO 2 is a high dielectric film</p> <p>The film 81 is formed. Specifically, the TiO 2 film 81 having a thickness of 5 nm is formed by the DC sputtering method using a TiO 2 sintered target under the sputtering conditions of power 300 W, pressure 1 Pa, Ar / O 2 flow rate 22 / 1.2 sccm. . At this time, the surface of the silicon substrate in the regions A and B is oxidized by the oxygen plasma atmosphere during the sputtering of the TiO 2 film, and the interface layers 82 and 83 are formed. The interface layer 82 in the region A has the result that the nitrogen introduction region 64 suppresses the diffusion of oxygen into the substrate.</p> <p>A polycrystalline silicon film having a thickness of 175 n is formed on the upper surface by a CVD method.</p> <p>A gate electrode 91 is formed by forming a film and performing patterning. Along with the gate electrode 91, the TiO 2 film 81 and the interface layers 82 and 83 which will be the gate insulating film thereunder are also patterned. After that, in order to crystallize the TiO 2 film 81, RTA with a heat treatment temperature of 900 ° C. and a heat treatment time of 30 seconds is performed.</p> <p>Do. At this time, the surface of the silicon substrate in the region B is oxidized by the diffusion of oxygen from the TiO 2 film 81 to the silicon substrate 51 by RTA, and the interface layer 83 grows to finally become the interface layer 83a of about 2 nm. In the region A, the nitrogen introduction region 64 suppresses the diffusion of oxygen into the substrate,</p>

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Claim	Claim Language	Exemplary Disclosures in Additional References
		<p>The growth of the interface layer 82 is suppressed, and finally about 0.7 nm. The interface layer 82a has a thickness of nm. It becomes a thin silicon oxide film, and the interface layer 83 in the region B becomes a thicker silicon oxide film.</p> <p style="text-align: center;">【 図 1 1 】</p> <p>See, e.g., U.S. Pat. No. 8,349,695 to Scheiper et al. (“Scheiper”) at:</p> <p>3:42-63: FIG. 1a schematically illustrates a cross-sectional view of a semiconductor device 100 which comprises a substrate 101 and a semiconductor layer 102 formed above the substrate 101. The semiconductor layer 102 is typically provided in the 45° form of a silicon material as</p>

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Claim	Claim Language	Exemplary Disclosures in Additional References
		<p>explained above. Moreover, a first semiconductor region or active region 102A and a second semiconductor region or active region 102B are provided in the semiconductor layer 102. The active regions 102A, 102B are to be understood as semiconductor regions in and above 50 which transistor elements are to be formed on the basis of gate electrode structures including a high-k dielectric material. In the example shown, it may be assumed that a gate electrode structure of reduced gate dielectric thickness is to be formed on the semiconductor region 102A, while a gate electrode 55 structure having a gate dielectric material of increased thickness is to be formed on the semiconductor region 102B. Furthermore, in the manufacturing stage shown, a gate dielectric material 151 is selectively formed on the active region 102B and is comprised of silicon dioxide with a specific 60 thickness, for instance with a thickness of several nanometers, depending on the device requirements or any transistors to be formed in and above the semiconductor region 102B.</p> <p>4:27-36: FIG.1b schematically illustrates the semiconductor device 100 in a further advanced manufacturing phase in which the etch mask 103 is removed and the device 100 is exposed to a cleaning ambient 105 in order to remove contaminants and also to re-grow a thin dielectric base layer 152 on the semiconductor region 102A. For this purpose, a plurality of well established process techniques are available in order to obtain a silicon dioxide material on the basis of a well-controllable growth process.</p>

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Claim	Claim Language	Exemplary Disclosures in Additional References
		<p>insulation film is larger than the thickness of the second gate insulation film and the first gate insulation film is comprised of the first insulation film located on the semiconductor Substrate and the second insulation film located on the first insulation film; and wherein the second gate insulation film is comprised of a third insulation film located on the semiconductor substrate and the dielectric constant of the second and third insulation films is larger than the dielectric constant of the first insulation film.</p> <p>[5:19-22] FIG. 35 is a major part sectional view of a semiconductor substrate showing an example of the manufacturing method of a semiconductor integrated circuit according to an embodiment of the present invention in the order of steps;</p> <p>[6:1-18] An example of the manufacturing method for the semiconductor integrated circuit device according to an embodiment of the present invention will be described using major part sectional views of the semiconductor Substrate shown in FIGS. 1-40. In the Figures, a region A indicates a region in which a gate insulation film having a larger effective thickness is formed and the region B indicates a region in which a gate insulation film having a smaller effective thickness is formed. In the regions A, B, n-channel MIS transistor (hereinafter referred to as low V_{th} NMOS) having a low threshold value voltage (hereinafter referred to as V_{th}), p-channel MIS transistor (hereinafter referred to as low V_{th} PMOS) having a low V_{th}, n-channel MIS transistor (hereinafter referred to as high V_{th} NMOS) having a high V_{th} and p-channel MIS transistor (hereinafter referred to as high V_{th} PMOS) having a high V_{th} are formed and that is, eight kinds of the MIS transistors are formed on the same substrate.</p> <p>[7:60-8:4] Next, after the resist pattern RP10 is removed, as shown in FIG. 16, the protective film 5 is removed and the silicon oxide film 9 is formed on the surface of the semiconductor substrate 1, for example, in the thickness of 4 to 5 nm. The silicon oxide film 9 can be formed according to the thermal CVD method or thermal oxidation method. Meanwhile, the aforementioned silicon oxide film may be turned to silicon nitride film by nitriding the semiconductor substrate 1 thermally. The aforementioned thermal nitration is carried out with the semiconductor 1 heated at about 900° C. in a pressure reduced atmosphere containing nitrogen made radical by plasma discharge</p>

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Claim	Claim Language	Exemplary Disclosures in Additional References
		<p>[8:5-10] Next, as shown in FIG. 17, after the region A is covered with the resist pattern RP1, as shown in FIG. 18, the silicon oxide film 9 in the region B is removed using diluted HF with resist pattern RP11 as a mask. After that, as shown in FIG. 19, the resist pattern RP11 is removed.</p> <p>[8:11-26] Next, as shown in FIG. 20, high dielectric constant insulation film 10, for example, alumina film is formed on the semiconductor substrate 1. The high dielectric constant insulation film 10 can be deposited according to, for example, sputtering method. The thickness of the high dielectric constant insulation film 10 formed on the semiconductor substrate 1 is set so that its effective thickness is about 5 nm. For example, the alumina film is deposited in the thickness of about 10 nm considering dielectric constant. Consequently, gate insulation film 11 comprised of the high dielectric constant insulation film 10 about 5 nm in terms of its effective thickness is formed in the region B and gate insulation film 12 comprised of stacked film of the high dielectric constant film 10 and the silicon oxide film 9 about 9 to 10 nm in terms of its effective thickness is formed in the region A</p> <p>[8:27-31] Before forming the aforementioned high dielectric constant insulation film 10 on the semiconductor substrate 1, silicon oxide film or silicon nitride film, or silicon oxide nitride film less than 1 nm or less may be formed to stabilize an interface with the semiconductor substrate 1.</p> <p>[8:32-34] Next, as shown in FIG. 21, silicon film 13 about 200 nm. thick is deposited on the semiconductor Substrate 1 according to the CVD method.</p> <p>[8:35-39] Next, as shown in FIG.22, after resist pattern 12 is formed in the NMOS formation region in the regions A, B, p-type impurity, for example, boron is ion-implanted into the silicon film 13 in the PMOS formation region in the regions A, B with this resist pattern RP12 as a mask.</p> <p>[8:40-46] Next, the resist pattern 12 is removed and as shown in FIG. 23, resist pattern RP13 is formed in the PMOS formation region in the regions A, B. After that, n-type impurity, for example, phosphorus is ion-implanted into the NMOS formation region in the regions A, B with this resist pattern RP13 as a mask.</p>

Claim	Claim Language	Exemplary Disclosures in Additional References
		<p>[8:47-55] Next, after the resist pattern RP13 is removed, by per forming heat treatment on the semiconductor Substrate 1, for example at 950° C. for about 60 seconds, the aforementioned n-type impurity and p-type impurity implanted into the silicon film 13 are activated. Further, the silicon film 13 in the NMOS formation region in the regions A, B is turned to n-type silicon polycrystal film and the silicon film 13 in the PMOS formation region in the regions A, B is changed to p-type silicon polycrystal film.</p> <p>[8:56-60] After as shown in FIG. 24, silicon oxide film 14 is deposited on the semiconductor Substrate 1 according to the CVD method, as shown in FIG. 25, resist pattern RP14 is formed to form gate electrodes of the n-channel and p-channel MIS transistor.</p> <p>[8:61-9:3] Next, after as shown in FIG. 26, the silicon oxide film 14 is etched with the resist pattern RP14 as a mask, the resist pattern RP14 is removed. Subsequently, as shown in FIG. 27, with the patterned silicon oxide film 14 as a mask, the silicon film 13 is etched so as to form a gate electrode (conductive piece) 15n comprised of n-type silicon poly crystal film in the NMOS formation region in the regions A, B and a gate electrode (conductive piece) comprised of p-type silicon polycrystal film in the PMOS formation region in the regions A, B</p> <p>[11:5-18] As described above, according to this embodiment, after the silicon oxide film 9 is formed on the surface of the semiconductor substrate 1, the silicon oxide film 9 in the region B (region in which a gate insulation whose effective thickness is small is formed) is removed with diluted HF and after that, by forming high dielectric constant insulation film 10 on the semiconductor Substrate 1, a damage or pollution to the surface of the semiconductor substrate 1 is prevented So as to form two kinds of the gate insulation films, that is, the gate insulation film 12 comprised of stacked film of the high dielectric constant insulation film 10 and the silicon oxide film 9 and the gate insulation film 11 comprised of the high dielectric constant insulation film 10 on the same semiconductor Substrate 1.</p> <p>[11:19-24] Because the gate insulation film 12 in the region A is comprised of stacked film of the high dielectric constant insulation film 10 and the silicon oxide film 9, the difference in level</p>

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Claim	Claim Language	Exemplary Disclosures in Additional References
		<p>between the region A and region B can be reduced compared to the stacked film comprised of two high dielectric constant insulation films.</p> <p>[11:25-30] Further because the thickness of the silicon oxide film 9 can be reduced as compared to a case where the gate insulation film 12 in the region A is comprised of only the silicon oxide film, oxidation of the interior of the isolation groove 4a can be suppressed so that stress at an end portion of the isolation groove 4a can be reduced.</p> <p>[11:31-32] Next, an example of an inverter circuit applying an embodiment of the present invention is shown in FIG. 41.</p> <p>[11:33-46] In the same Figure, a region Surrounded by dotted lines indicates a CMOS inverter and Tkp and Tnp denote p-channel MIS transistor while Tkn and Tnn denote n-channel MIS transistor. The gate insulation film of the MIS transistors Tnp, Tnn constituting the CMOS inverter is thinner than the gate insulation film of the MIS transistors Tkp, Tkn. For example, the gate insulation film of the MIS transistors Tnp, Tnn constituting the CMOS inverter is formed of high dielectric constant insulation film and its effective thickness is about 3.5 nm. The gate insulation film of the MIS transistors Tkp, Tkn is constituted of stacked film of high dielectric constant insulation film and silicon oxide film and its effective thickness is about 6 nm.</p> <p>[13:20-37] Because the gate insulation film comprised of stacked film of high dielectric constant insulation film and silicon oxide film and the gate insulation film comprised of the high dielectric constant insulation film can be formed on the same semiconductor substrate so as to Suppress damage or pollution to the surface of the semiconductor substrate, plural gate insulation films each having a different thickness and a high reliability can be formed. Further, because the gate insulation film having a high effective thickness is constituted of stacked film of the high dielectric constant insulation film and silicon oxide film, a difference in step between a region in which the gate insulation film having a large effective thickness is formed and a region in which the gate insulation film having a small effective thickness is decreased as compared to a stacked film in which two high dielectric constant insulation films are stacked, so that subsequent manufacturing of the MIS transistor is facilitated.</p>

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Claim	Claim Language	Exemplary Disclosures in Additional References
		<p>[Claim 1] 1. A method of manufacturing a semiconductor integrated circuit device comprising the steps of (a) forming a first insulation film over a surface of a semiconductor Substrate in a first region and a second region different from said first region of said semiconductor substrate; (b) selectively removing said first insulation film in said second region, with said first insulation film being left in said first region; (c) forming a second insulation film over said semiconductor Substrate of said second region; (d) forming a third insulation film over said first insulation film in said first region and over said second insulation film in said second region; (e) forming a first conductive layer over said third insulation film; and (f) forming a first conductive piece in said first region and a second conductive piece in said second region by patterning said first conductive layer, wherein the thickness of said first insulation film is larger than the thickness of said second insulation film; said first insulation film includes silicon and at least one of oxygen and nitrogen; said second insulation film includes silicon and at least one of oxygen and nitrogen; said third insulation film has a greater dielectric constant than each of said first and second insulation films; and the thickness of said third insulation film is larger than the thickness of said first insulation film and said second insulation film</p>

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Claim		Claim Language	Exemplary Disclosures in Additional References
			<p align="center">FIG. 35</p> <p>The diagram illustrates a cross-section of a semiconductor device divided into two main sections, A and B. Section A features a low threshold voltage (Low V_{th}) NMOS transistor and a PMOS transistor. Section B features high threshold voltage (High V_{th}) NMOS and PMOS transistors. The device structure includes multiple layers: a substrate (6), a gate dielectric layer (12), a channel layer (16a, 17a), and source/drain regions (18). Various other layers and structures are labeled, such as 15n, 15p, 4a, 4b, 16b, 17b, 7, and 8.</p> <p>See, e.g., U.S. Pat. App. Pub. No. 2009/0039445 to Wu ("Wu '445") at:</p> <p>[0018] Still referring to FIG. 1A, the gate structures 12A and 12B may be formed by conventional CVD deposition, lithographic patterning, and plasma (dry) etching methods known in the art. The gate dielectric portions 14A and 14B may be formed by any process known in the art, e.g., thermal oxidation, nitridation, sputter deposition, chemical vapor deposition, or combinations thereof. The gate dielectric portions 14A and 14B may be formed of silicon oxide, silicon nitride, silicon oxynitride, and high-K dielectrics (e.g., K>8) including transition metal oxide and rare</p>

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Claim	Claim Language	Exemplary Disclosures in Additional References
		<p>earth metal oxides. For example, high-K dielectrics may be formed of aluminum oxides (e.g., Al₂O₃), hafnium oxides (e.g., HfO₂), hafnium oxynitrides (HfON), hafnium silicates (e.g., HfSiO₄), hafnium silicon oxynitrides (e.g., HfSixOyNz), zirconium oxides (e.g., ZrO₂), zirconium oxynitrides (e.g., ZrON), zirconium silicon oxides (e.g., ZrSiO₂), yttrium oxides (Y₂O₃), lanthanum oxides (La₂O₃), cerium oxides (CeO₂), titanium oxides (TiO₂), tantalum oxides (Ta₂O₅), or combinations thereof. The high-k dielectric layer may be formed by known CVD methods such as atomic layer CVD (ALCVD) and metal-organic CVD (MOCVD). It will be appreciated that the high-K dielectric layer may include a lowermost interfacial layer formed on the semiconductor substrate such as an oxide or oxynitride (not shown).</p> <p>See 1[d]-[e]</p>

Claim	Claim Language	Exemplary Disclosures in Additional References
2 [a]	<p>The semiconductor device of claim 1, wherein the first gate electrode includes first sidewall spacers formed on side surfaces thereof and first insulating spacers interposed between the first gate electrode and the first sidewall spacers,</p>	<p>The following references disclose and/or render obvious a “The semiconductor device of claim 1, wherein the first gate electrode includes first sidewall spacers formed on side surfaces thereof and first insulating spacers interposed between the first gate electrode and the first sidewall spacers,” as further described below.</p> <p><i>See, e.g.,</i> U.S. Pat. App. Pub. No. 2004/0188769 to Tsuno (“Tsuno”) at:</p> <p>[0034] First, the structure of a semiconductor device according to a first embodiment of the present invention will be described. FIG. 9 is a cross-sectional view of the structure of the Semiconductor device in accordance with the first embodiment.</p> <p>[0037] A gate insulation film 19A is formed on the n-type well region 12 between the source/drain regions 16, and a gate electrode 20A is formed on the gate insulation film 19A. Offset spacers 21A are formed on either side of the gate electrode 20A. Gate sidewall films 22A are formed on the side of the offset spacers 21A.</p> <p>[0038] A gate insulation film 19B is formed on the p-type well region 13 between the Source/drain regions 18, and a gate electrode 20B is formed on the gate insulation film 19B.</p>

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Claim	Claim Language	Exemplary Disclosures in Additional References
		<p>Offset spacers 21B whose thickness differs from that of the offset spacer 21A are formed on either side of the gate electrode 20B. Gate sidewall films 22B whose thickness differs from that of the gate sidewall films 22A are formed on the side of the offset spacer 21B.</p> <p>[0039] The offset spacer 21B is thinner than the offset spacer 21A. For example, the bottom portion of the offset spacer 21B, which contacts the Semiconductor Substrate 11, is about 6 nm to 10 nm in thickness and the bottom portion of the offset spacer 21A, which contacts the semiconductor substrate 11, is about 12 nm in thickness. The gate sidewall film 22B is thinner than the gate sidewall film 22A. For example, the bottom portion of the gate Sidewall film 22A, which contacts the semiconductor Substrate 11, is about 70 nm in thickness and thicker than the bottom portion of the gate Sidewall film 22B which contacts the Semiconductor Substrate 11.</p> <p>[0040] The offset spacers 21A and 21B are each made of an insulation film Such as a TEOS (tetraethylorthosilicate) film and a silicon nitride film. The offset spacer 21B includes an element that is not contained in the offset spacer 21A and more specifically an element that enhances the etching rate. The element that enhances the etching rate is, for example, arsenic (AS), phosphorus (P), boron (B), indium (In), carbon (C) and germanium (Ge). The offset spacer 21B includes at least one of these elements.</p> <p>[0041] The gate sidewall films 22A and 22B are each made up of an insulation film such as a multilayer film including a TEOS film, a silicon nitride film and a BSG (borosilicate glass) film. The gate sidewall film 22B includes an element that is not contained in the gate sidewall film 22A and more specifically an element that enhances the etching rate. The element that enhances the etching rate is, for example, arsenic (AS), phosphorus (P), boron (B), indium (In), carbon (C) and germanium (Ge). The gate Sidewall film 22B includes at least one of these elements.</p> <p>[0043] A pMOSFET includes a n-type well region 12, extension regions is, Source/drain regions 16, a gate insulation film 19A, a gate electrode 20A, offset spacers 21A and gate sidewall films 22A. An nMOSFET includes a p-type well region 13, extension regions 17,</p>

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Claim	Claim Language	Exemplary Disclosures in Additional References
		<p>source/drain regions 18, a gate insulation film 19B, a gate electrode 20B, offset spacers 21B and gate sidewall films 22B.</p> <p>[0044] In the semiconductor device described above, the offset Spacers and/or the gate Sidewall films can be varied in thickness between the nMOSFET and pMOSFET. Thus each of the offset Spacers and the gate Sidewall films may be optimized in thickness without deteriorating from predetermined characteristics of nMOSFETs and pMOSFETs. In particular, the offset spacers can be adjusted in thickness between the nMOSFET and pMOSFET and thus the location of the extension regions, which is formed on the underside of the gate sidewall films formed outside of the offset spacers, can be controlled. Accordingly, the characteristics of the nMOSFET and pMOSFET can be optimized.</p> <p>[0045] Moreover, the offset spacer and the gate sidewall film, which were undesirably thick, can be thinned. Further miniaturization of a Semiconductor integrated circuit including the nMOSFETs and the pMOSFETs can be achieved.</p>

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Claim		
Claim Language		
Exemplary Disclosures in Additional References	<p>FIG. 9</p> <p>See, e.g., U.S. Pat. App. Pub. No. 2009/0039445 to Wu ("Wu '445"):</p> <p>[0012] In a first embodiment, the method includes providing a semiconductor substrate including at least two gate structures; growing a silicon oxide layer having a respective differential thickness over the at least two gate structures; forming a dielectric layer on the silicon oxide layer having an etching selectivity with respect to the silicon oxide layer; forming offset spacers having a differential thickness including the dielectric layer and the silicon oxide layer adjacent either side of the at least two respective gate structures; and, carrying out an ion implant process adjacent the offset spacers to form doped regions in the semiconductor substrate forming at least two MOSFET devices.</p>	

See, e.g., U.S. Pat. App. Pub. No. 2009/0039445 to Wu (“Wu ’445”):

[0012] In a first embodiment, the method includes providing a semiconductor substrate including at least two gate structures; growing a silicon oxide layer having a respective differential thickness over the at least two gate structures; forming a dielectric layer on the silicon oxide layer having an etching selectivity with respect to the silicon oxide layer; forming offset spacers having a differential thickness including the dielectric layer and the silicon oxide layer adjacent either side of the at least two respective gate structures; and, carrying out an ion implant process adjacent the offset spacers to form doped regions in the semiconductor substrate forming at least two MOSFET devices.

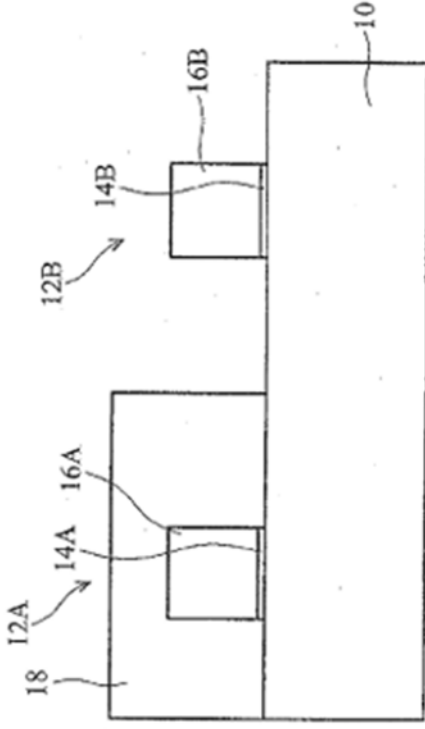
Claim	Claim Language	Exemplary Disclosures in Additional References
		<p>[0020] Referring to FIG. 1B, a patterned photoresist layer 18 is then formed to cover selected gate structures. For example, in the dual device gate structure formation process shown, gate structure 12A is covered while leaving gate structure 12B uncovered. Following formation of patterned photoresist layer 18, in an important aspect of the invention, an ion implantation process is carried out to ion implant uncovered gate structure 12B and adjacent substrate areas with one of a thermal oxidation rate enhancing or thermal oxidation rate suppressing ion implant. For example, in the embodiment as shown, fluorine ions (e.g., F-) are used in the ion implant process to enhance a subsequent thermal oxidation rate in growing a thermal oxide (SiO₂) over the gate structures 12A and 12B as well as adjacent substrate areas. Alternatively, a thermal oxidation rate suppressing ion implant such as a nitrogen (e.g., N-) implant may be used to suppress a subsequent thermal oxidation rate and thereby a subsequent SiO₂ thermal oxide thickness is reduced.</p>  <p>The diagram is a cross-sectional view of a semiconductor device. It shows a substrate 10 with two gate structures, 12A and 12B, on its surface. Gate structure 12A is on the left and gate structure 12B is on the right. A patterned photoresist layer 18 is formed over the device, covering gate structure 12A and the substrate area between the two gates. The photoresist layer 18 has two openings, 14A and 14B, which align with the top surfaces of gate structures 12A and 12B, respectively. Within these openings, there are layers 16A and 16B, which appear to be ion implantation regions. The photoresist layer 18 is thicker over the substrate area between the gates than it is over the gates themselves.</p> <p style="text-align: center;">FIG. 1B</p> <p>[0021] Referring to FIG. 1C, following the ion implant process and stripping of the patterned photoresist layer 18, a conventional thermal oxide growth process is carried out, for example, a wet or dry oxidation process at temperatures of about 900° C. to about 1050° C., to grow a silicon oxide (SiO₂) layer over gate structures 12A and 12B as well as adjacent substrate 10</p>

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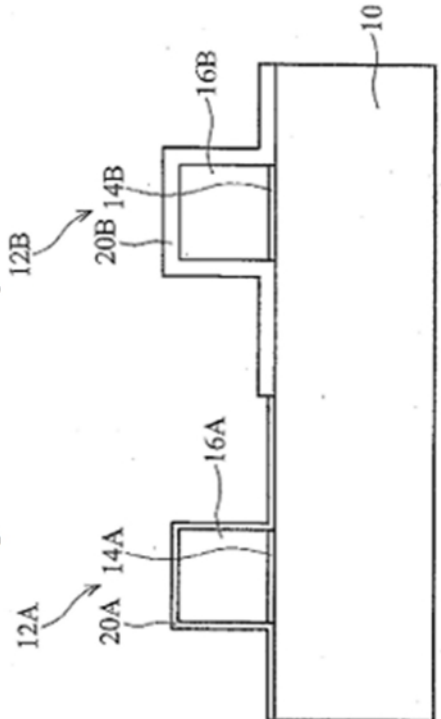
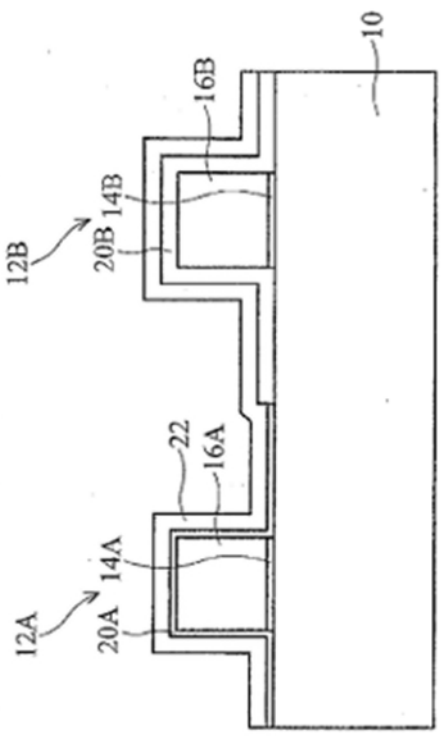
Claim	Claim Language	Exemplary Disclosures in Additional References
		<p>portions. In an important aspect of the invention, the SiO₂ layer formed over the gate structures are formed to have a differential thickness. For example, in the embodiment shown, SiO₂ layer portion 20B, grown over the area subjected to the fluorine ion implant including gate structure 12B, is formed have a relatively greater thickness compared to SiO₂ layer portion 20A grown over the photoresist covered area including gate structure 12A. The differential thickness is advantageously formed as a result of the oxide growth rate enhancing fluorine ion implantation over the gate structure 12B and adjacent substrate portions.</p>  <p style="text-align: center;">FIG. 1C</p> <p>[0022] It will be appreciated that an oxide growth suppressing ion implant may be used to form the differentially thick SiO₂ thermal oxide layer. For example, a nitrogen ion implant may be carried out over gate structure 12A while covering gate structure 12B with photoresist such that the similar differentially thick SiO₂ layer portions 20A and 20B will be formed. It will also be appreciated that a greater differential thickness between oxide layer portions e.g., 20A and 20B may be formed by carrying out both an oxide growth enhancing implant over one gate structure e.g., 12B as well as an oxide growth suppressing implant over another gate structure e.g., 12A. Preferably, the relatively thinner oxide layer portion e.g., 20A is formed at a thickness between about 10 Angstroms to about 50 Angstroms and the relatively thicker</p>

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Claim	Claim Language	Exemplary Disclosures in Additional References
		<p>oxide layer portion e.g., 20B is formed at a thickness between about 20 Angstroms to 80 Angstroms.</p> <p>[0023] Referring to FIG. 1D a dielectric layer 22 is blanket deposited, e.g., by CVD or PECVD over the oxide layers 20A and 20B. The dielectric layer 22 preferably has an etching selectivity with respect to the underlying thermal oxide layer portions e.g., 20A and 20B, for example, formed of a nitride material such as silicon nitride (e.g., SiN) and/or silicon oxynitride (e.g., SiON). The dielectric layer 22 is preferably deposited having a thickness range of about 20 Angstroms to about 80 Angstroms.</p>  <p>FIG. 1D</p> <p>[0024] Referring to FIG. 1E, conventional dry and/or wet etching processes, are then carried out to etch back the dielectric layer 22 and oxide layer portions, 20A and 20B, to form composite oxide/nitride offset spacers e.g., 24A and 24B, adjacent either side of the gate structures 12A and 12B.</p>

Claim		Claim Language	Exemplary Disclosures in Additional References
			<p style="text-align: center;">FIG. 1E</p> <p>[0030] Referring to FIG. 2, is shown a process flow diagram including several embodiments of the present invention. In process 201, gate structures are provided on a semiconductor substrate. In process 203, a thermally grown oxide layer is formed over the gate structures and adjacent substrate portions to form at least two different thermal oxide layer thicknesses over respective gate structures. In process 205, a dielectric layer with an etching selectivity with respect to the thermal oxide layer is formed on the thermal oxide layer. In process 207, etching processes are carried out to form at least two different pair of offset spacers and associated respective maximum widths adjacent respective gate structures. In process 209, ion implant processes are carried out to form doped regions adjacent the offset spacers to form at least two operationally different transistor devices.</p>

Claim	Claim Language	Exemplary Disclosures in Additional References
		<pre> graph TD 201[provide gate structures on a semiconductor substrate] --> 203[form at least two different thermal oxide layer thicknesses over respective gate structures] 203 --> 205[form a dielectric layer on the thermal oxide layer] 205 --> 207[form at least two different pair of offset spacer widths adjacent respective gate structures] 207 --> 209[carry out ion implant to form at least two operationally different transistor devices] </pre> <p style="text-align: center;">FIG. 2</p> <p><i>See, e.g., 6,946,709, Yang at:</i></p> <p>3:65-4:10: A second thin oxide layer 130, as shown in FIG. 5, (such as 50 Å thick LTO) is deposited after the photoresist 128 is removed from the wafer. This process adds thickness to the oxide 124. Therefore, the oxide 124 is thicker than the oxide 130 and the PFET devices 120 have a thicker total oxide layer 124 than the NFET devices 118. FIG. 6 shows a spacer</p>

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Claim	Claim Language	Exemplary Disclosures in Additional References
		<p>134 (such as Si₃N₄) that is formed to offset source and drain ion implants. In this embodiment, total Spacers size (thickness) is determined by the combined thicknesses of the spacer 134 along with the oxide 124, 130. Thus, the NFET devices 118 have a thinner total Spacer Size and hence a Shorter extension and lower extension resistance. The Source/drain extension implant is made at this point.</p> <div data-bbox="483 394 782 1312"> <p>FIG. 5 is a cross-sectional view of a semiconductor device. It shows a pFET on the left and an nFET on the right. Both have gate stacks 112. The pFET gate stack includes a thin oxide layer 130 and a spacer 124. The nFET gate stack includes a thin oxide layer 130 and a spacer 122. The source/drain regions are labeled 114 and 110.</p> </div> <div data-bbox="812 819 852 938"> <p>FIG. 5</p> </div> <div data-bbox="880 394 1214 1312"> <p>FIG. 6 is a cross-sectional view of a semiconductor device. It shows a pFET on the left and an nFET on the right. Both have gate stacks 112. The pFET gate stack includes a thin oxide layer 130 and a spacer 124. The nFET gate stack includes a thin oxide layer 130 and a spacer 122. The source/drain regions are labeled 114 and 110.</p> </div> <div data-bbox="1243 819 1284 938"> <p>FIG. 6</p> </div>

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Claim	Claim Language	Exemplary Disclosures in Additional References
2 [b]	the second gate electrode includes second sidewall spacers formed on side surfaces thereof and second insulating spacers interposed between the second gate electrode and the second sidewall spacers, and	<p>The following references disclose and/or render obvious a “the second gate electrode includes second sidewall spacers formed on side surfaces thereof and second insulating spacers interposed between the second gate electrode and the second sidewall spacers, and” as further described below.</p> <p><i>See, e.g., U.S. Pat. App. Pub. No. 2004/0188769 to Tsuno (“Tsuno”) at:</i></p> <p>[0034] First, the structure of a semiconductor device according to a first embodiment of the present invention will be described. FIG. 9 is a cross-sectional view of the structure of the Semiconductor device in accordance with the first embodiment.</p> <p>[0037] A gate insulation film 19A is formed on the n-type well region 12 between the source/drain regions 16, and a gate electrode 20A is formed on the gate insulation film 19A. Offset spacers 21A are formed on either side of the gate electrode 20A. Gate sidewall films 22A are formed on the side of the offset spacers 21A.</p> <p>[0038] A gate insulation film 19B is formed on the p-type well region 13 between the Source/drain regions 18, and a gate electrode 20B is formed on the gate insulation film 19B. Offset spacers 21B whose thickness differs from that of the offset spacer 21A are formed on either side of the gate electrode 20B. Gate sidewall films 22B whose thickness differs from that of the gate sidewall films 22A are formed on the side of the offset spacer 21B.</p> <p>[0039] The offset spacer 21B is thinner than the offset spacer 21A. For example, the bottom portion of the offset spacer 21B, which contacts the Semiconductor Substrate 11, is about 6 nm to 10 nm in thickness and the bottom portion of the offset spacer 21A, which contacts the semiconductor substrate 11, is about 12 nm in thickness. The gate sidewall film 22B is thinner than the gate sidewall film 22A. For example, the bottom portion of the gate Sidewall film 22A, which contacts the semiconductor Substrate 11, is about 70 nm in thickness and thicker than the bottom portion of the gate Sidewall film 22B which contacts the Semiconductor Substrate 11.</p>

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Claim	Claim Language	Exemplary Disclosures in Additional References
		<p>[0040] The offset spacers 21A and 21B are each made of an insulation film such as a TEOS (tetraethylorthosilicate) film and a silicon nitride film. The offset spacer 21B includes an element that is not contained in the offset spacer 21A and more specifically an element that enhances the etching rate. The element that enhances the etching rate is, for example, arsenic (As), phosphorus (P), boron (B), indium (In), carbon (C) and germanium (Ge). The offset spacer 21B includes at least one of these elements.</p> <p>[0041] The gate sidewall films 22A and 22B are each made up of an insulation film such as a multilayer film including a TEOS film, a silicon nitride film and a BSG (borosilicate glass) film. The gate sidewall film 22B includes an element that is not contained in the gate sidewall film 22A and more specifically an element that enhances the etching rate. The element that enhances the etching rate is, for example, arsenic (As), phosphorus (P), boron (B), indium (In), carbon (C) and germanium (Ge). The gate Sidewall film 22B includes at least one of these elements.</p> <p>[0043] A pMOSFET includes a n-type well region 12, extension regions is, Source/drain regions 16, a gate insulation film 19A, a gate electrode 20A, offset spacers 21A and gate sidewall films 22A. An nMOSFET includes a p-type well region 13, extension regions 17, source/drain regions 18, a gate insulation film 19B, a gate electrode 20B, offset spacers 21B and gate sidewall films 22B.</p> <p>[0044] In the semiconductor device described above, the offset Spacers and/or the gate Sidewall films can be varied in thickness between the nMOSFET and pMOSFET. Thus each of the offset Spacers and the gate Sidewall films may be optimized in thickness without deteriorating from predetermined characteristics of nMOSFETs and pMOSFETs. In particular, the offset spacers can be adjusted in thickness between the nMOSFET and pMOSFET and thus the location of the extension regions, which is formed on the underside of the gate sidewall films formed outside of the offset spacers, can be controlled. Accordingly, the characteristics of the nMOSFET and pMOSFET can be optimized.</p>

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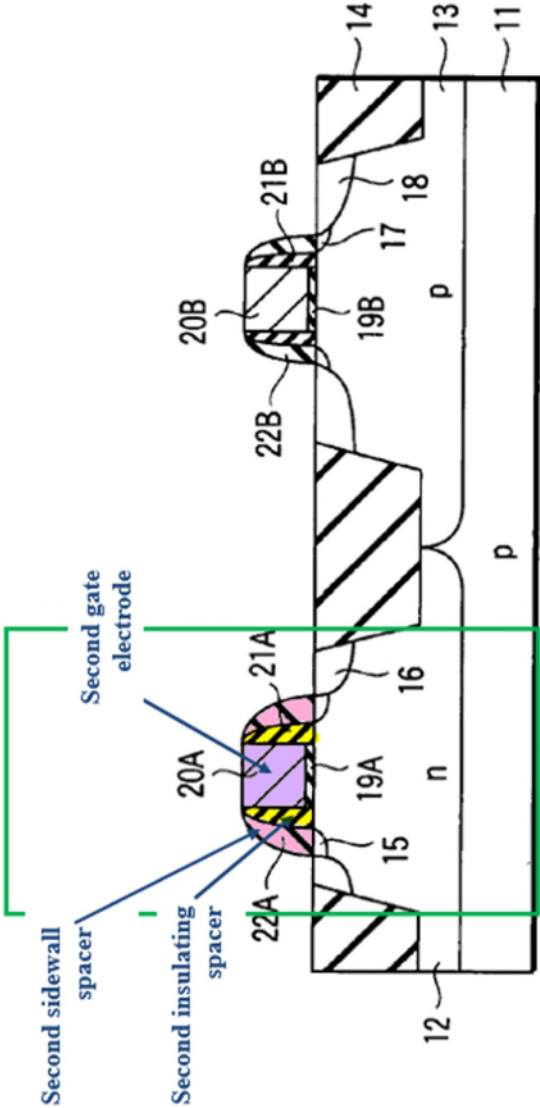
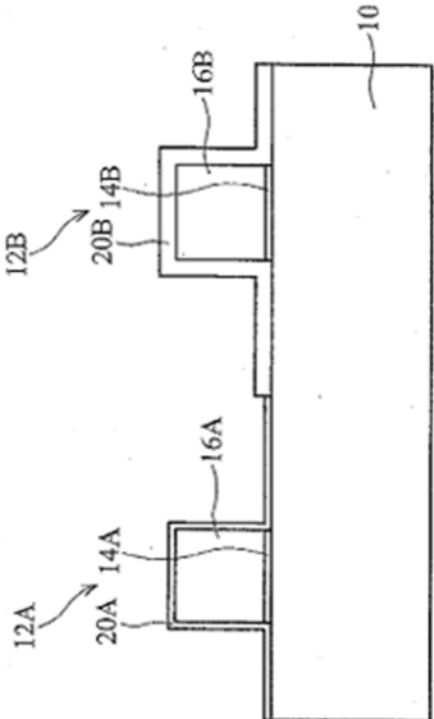
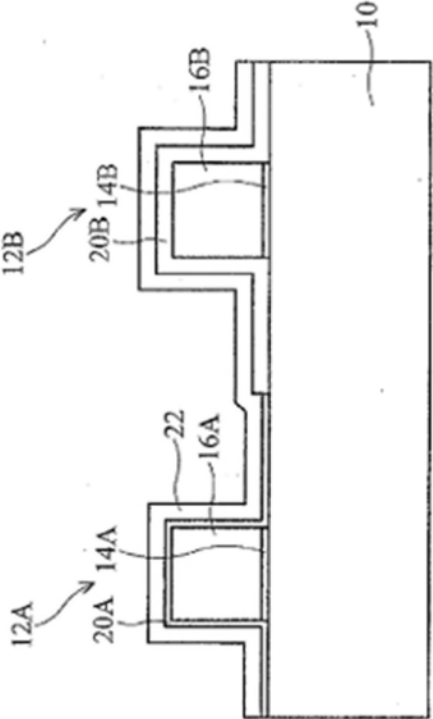
Claim	Claim Language	Exemplary Disclosures in Additional References
		<p>[0045] Moreover, the offset spacer and the gate sidewall film, which were undesirably thick, can be thinned. Further miniaturization of a Semiconductor integrated circuit including the nMOSFETs and the pMOSFETs can be achieved.</p>  <p style="text-align: center;">FIG. 9</p> <p>See, e.g., U.S. Pat. App. Pub. No. 2009/0039445 to Wu ("Wu '445") at:</p> <p>[0012] In a first embodiment, the method includes providing a semiconductor substrate including at least two gate structures; growing a silicon oxide layer having a respective differential thickness over the at least two gate structures; forming a dielectric layer on the silicon oxide layer having an etching selectivity with respect to the silicon oxide layer; forming offset spacers having a differential thickness including the dielectric layer and the silicon oxide layer adjacent either side of the at least two respective gate structures; and, carrying out an ion implant process adjacent the offset spacers to form doped regions in the semiconductor substrate forming at least two MOSFET devices.</p>

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Claim	Claim Language	Exemplary Disclosures in Additional References
		<p>[0020] Referring to FIG. 1B, a patterned photoresist layer 18 is then formed to cover selected gate structures. For example, in the dual device gate structure formation process shown, gate structure 12A is covered while leaving gate structure 12B uncovered. Following formation of patterned photoresist layer 18, in an important aspect of the invention, an ion implantation process is carried out to ion implant uncovered gate structure 12B and adjacent substrate areas with one of a thermal oxidation rate enhancing or thermal oxidation rate suppressing ion implant. For example, in the embodiment as shown, fluorine ions (e.g., F-) are used in the ion implant process to enhance a subsequent thermal oxidation rate in growing a thermal oxide (SiO₂) over the gate structures 12A and 12B as well as adjacent substrate areas. Alternatively, a thermal oxidation rate suppressing ion implant such as a nitrogen (e.g., N-) implant may be used to suppress a subsequent thermal oxidation rate and thereby a subsequent SiO₂ thermal oxide thickness is reduced.</p> <p style="text-align: center;">FIG. 1B</p> <p>[0021] Referring to FIG. 1C, following the ion implant process and stripping of the patterned photoresist layer 18, a conventional thermal oxide growth process is carried out, for example, a wet or dry oxidation process at temperatures of about 900° C. to about 1050° C., to grow a</p>

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Claim	Claim Language	Exemplary Disclosures in Additional References
		<p>silicon oxide (SiO₂) layer over gate structures 12A and 12B as well as adjacent substrate 10 portions. In an important aspect of the invention, the SiO₂ layer formed over the gate structures are formed to have a differential thickness. For example, in the embodiment shown, SiO₂ layer portion 20B, grown over the area subjected to the fluorine ion implant including gate structure 12B, is formed have a relatively greater thickness compared to SiO₂ layer portion 20A grown over the photoresist covered area including gate structure 12A. The differential thickness is advantageously formed as a result of the oxide growth rate enhancing fluorine ion implantation over the gate structure 12B and adjacent substrate portions.</p>  <p style="text-align: center;">FIG. 1C</p> <p>[0022] It will be appreciated that an oxide growth suppressing ion implant may be used to form the differentially thick SiO₂ thermal oxide layer. For example, a nitrogen ion implant may be carried out over gate structure 12A while covering gate structure 12B with photoresist such that the similar differentially thick SiO₂ layer portions 20A and 20B will be formed. It will also be appreciated that a greater differential thickness between oxide layer portions e.g., 20A and 20B may be formed by carrying out both an oxide growth enhancing implant over one gate structure e.g., 12B as well as an oxide growth suppressing implant over another gate structure e.g., 12A. Preferably, the relatively thinner oxide layer portion e.g., 20A is formed</p>

Claim	Claim Language	Exemplary Disclosures in Additional References
		<p>at a thickness between about 10 Angstroms to about 50 Angstroms and the relatively thicker oxide layer portion e.g., 20B is formed at a thickness between about 20 Angstroms to 80 Angstroms.</p> <p>[0023] Referring to FIG. 1D a dielectric layer 22 is blanket deposited, e.g., by CVD or PECVD over the oxide layers 20A and 20B. The dielectric layer 22 preferably has an etching selectivity with respect to the underlying thermal oxide layer portions e.g., 20A and 20B, for example, formed of a nitride material such as silicon nitride (e.g., SiN) and/or silicon oxynitride (e.g., SiON). The dielectric layer 22 is preferably deposited having a thickness range of about 20 Angstroms to about 80 Angstroms.</p>  <p style="text-align: center;">FIG. 1D</p> <p>[0024] Referring to FIG. 1E, conventional dry and/or wet etching processes, are then carried out to etch back the dielectric layer 22 and oxide layer portions, 20A and 20B, to form composite oxide/nitride offset spacers e.g., 24A and 24B, adjacent either side of the gate structures 12A and 12B.</p>

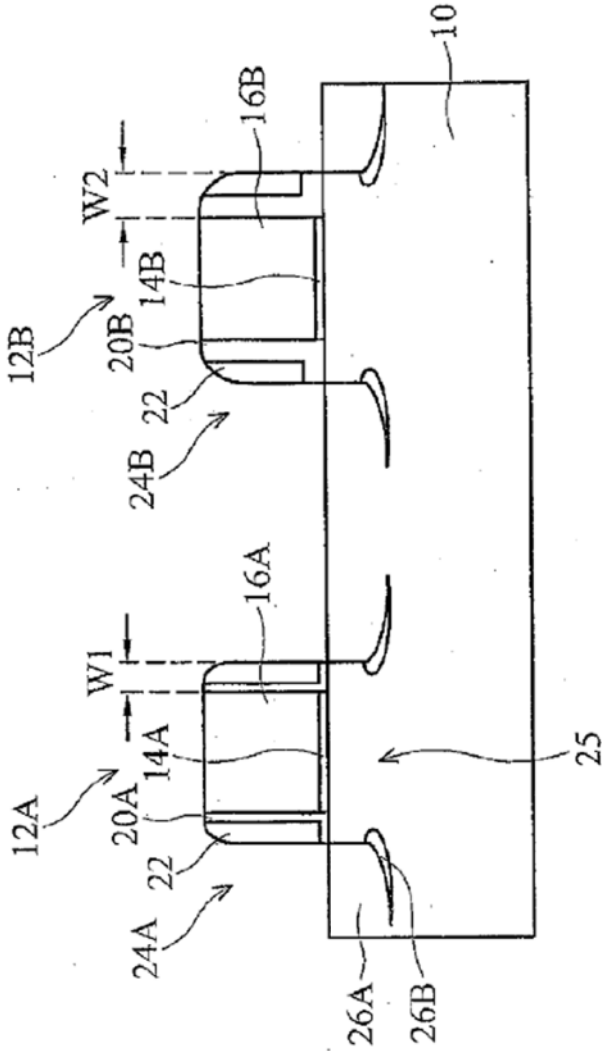
Claim	Claim Language	Exemplary Disclosures in Additional References
		 <p data-bbox="876 703 933 913">FIG. 1E</p> <p data-bbox="982 191 1356 1394">[0030] Referring to FIG. 2, is shown a process flow diagram including several embodiments of the present invention. In process 201, gate structures are provided on a semiconductor substrate. In process 203, a thermally grown oxide layer is formed over the gate structures and adjacent substrate portions to form at least two different thermal oxide layer thicknesses over respective gate structures. In process 205, a dielectric layer with an etching selectivity with respect to the thermal oxide layer is formed on the thermal oxide layer. In process 207, etching processes are carried out to form at least two different pair of offset spacers and associated respective maximum widths adjacent respective gate structures. In process 209, ion implant processes are carried out to form doped regions adjacent the offset spacers to form at least two operationally different transistor devices.</p>

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Claim	Claim Language	Exemplary Disclosures in Additional References
		<pre> graph TD 201[provide gate structures on a semiconductor substrate] --> 203[form at least two different thermal oxide layer thicknesses over respective gate structures] 203 --> 205[form a dielectric layer on the thermal oxide layer] 205 --> 207[form at least two different pair of offset spacer widths adjacent respective gate structures] 207 --> 209[carry out ion implant to form at least two operationally different transistor devices] </pre> <p style="text-align: center;">FIG. 2</p> <p><i>See, e.g., U.S. Pat. No. 6,946,709 to Yang ("Yang") at:</i></p> <p>3:51-62: A first embodiment of the invention is shown in FIGS. 1-9. FIG. 1 Shows the PFET 120 and NFET 118 devices separated by a shallow trench isolation (STI) region 122 in the Substrate 110. The gate conductor 112 is patterned and a thin Spacer 114 is formed to offset extension ion implants to the channel. FIG. 2 shows a thin oxide liner 124 (such as 100 Å</p>

Claim	Claim Language	Exemplary Disclosures in Additional References
		<p>thick LTO) that is deposited over the gate conductors 112 and the thin Spacers 114. A protective mask 128, Such as a photoresist, is applied and patterned to cover PFET devices 120 in FIG. 3. Then, the thin oxide 124 is removed to the expose NFET devices 118 by either reactive ion etching (RIE) or wet etching chemicals, as shown in FIG. 4. The mask 128 is then removed.</p> <p>The diagrams illustrate the process of removing thin oxide 124 to expose NFET devices 118. FIG. 2 shows a cross-section of the device with gate conductors 112, thin spacers 114, and a thin oxide layer 124. A protective mask 128 is applied over the PFET devices 120. FIG. 3 shows the mask 128 being patterned to cover the PFET devices 120. FIG. 4 shows the thin oxide 124 being removed to expose the NFET devices 118.</p>

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Claim	Claim Language	Exemplary Disclosures in Additional References
		<p>3:65-4:10: A second thin oxide layer 130, as shown in FIG. 5, (such as 50 Å thick LTO) is deposited after the photoresist 128 is removed from the wafer. This process adds thickness to the oxide 124. Therefore, the oxide 124 is thicker than the oxide 130 and the PFET devices 120 have a thicker total oxide layer 124 than the NFET devices 118. FIG. 6 shows a spacer 134 (such as Si₃N₄) that is formed to offset source and drain ion implants. In this embodiment, total Spacers size (thickness) is determined by the combined thicknesses of the spacer 134 along with the oxide 124, 130. Thus, the NFET devices 118 have a thinner total Spacer Size and hence a Shorter extension and lower extension resistance. The Source/drain extension implant is made at this point.</p>

Claim	Claim Language	Exemplary Disclosures in Additional References
		<div></div> <p>See 2[a]</p>

Claim	Claim Language	Exemplary Disclosures in Additional References
2 [c]	the first insulating spacers are thinner than the second insulating spacers.	<p>The following references disclose and/or render obvious a “the first insulating spacers are thinner than the second insulating spacers” as further described below.</p> <p>See, e.g., U.S. Pat. App. Pub. No. 2004/0188769 to Tsuno (“Tsuno”) at:</p>

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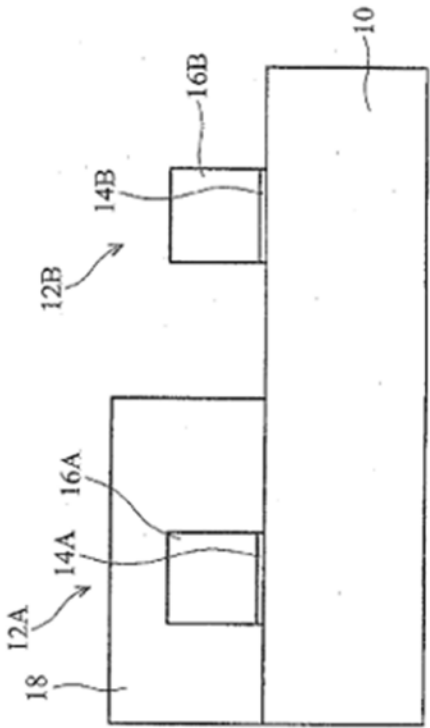
Claim	Claim Language	Exemplary Disclosures in Additional References
		<p>[0034] First, the structure of a semiconductor device according to a first embodiment of the present invention will be described. FIG. 9 is a cross-sectional view of the structure of the Semiconductor device in accordance with the first embodiment.</p> <p>[0037] A gate insulation film 19A is formed on the n-type well region 12 between the source/drain regions 16, and a gate electrode 20A is formed on the gate insulation film 19A. Offset spacers 21A are formed on either side of the gate electrode 20A. Gate sidewall films 22A are formed on the side of the offset spacers 21A.</p> <p>[0038] A gate insulation film 19B is formed on the p-type well region 13 between the Source/drain regions 18, and a gate electrode 20B is formed on the gate insulation film 19B. Offset spacers 21B whose thickness differs from that of the offset spacer 21A are formed on either side of the gate electrode 20B. Gate sidewall films 22B whose thickness differs from that of the gate sidewall films 22A are formed on the side of the offset spacer 21B.</p> <p>[0039] The offset spacer 21B is thinner than the offset spacer 21A. For example, the bottom portion of the offset spacer 21B, which contacts the Semiconductor Substrate 11, is about 6 nm to 10 nm in thickness and the bottom portion of the offset spacer 21A, which contacts the semiconductor substrate 11, is about 12 nm in thickness. The gate sidewall film 22B is thinner than the gate sidewall film 22A. For example, the bottom portion of the gate Sidewall film 22A, which contacts the semiconductor Substrate 11, is about 70 nm in thickness and thicker than the bottom portion of the gate Sidewall film 22B which contacts the Semiconductor Substrate 11.</p> <p>[0040] The offset spacers 21A and 21B are each made of an insulation film Such as a TEOS (tetraethylorthosilicate) film and a silicon nitride film. The offset spacer 21B includes an element that is not contained in the offset spacer 21A and more specifically an element that enhances the etching rate. The element that enhances the etching rate is, for example, arsenic (AS), phosphorus (P), boron (B), indium (In), carbon (C) and germanium (Ge). The offset spacer 21B includes at least one of these elements.</p>

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Claim	Claim Language	Exemplary Disclosures in Additional References
		<p>[0041] The gate sidewall films 22A and 22B are each made up of an insulation film such as a multilayer film including a TEOS film, a silicon nitride film and a BSG (borosilicate glass) film. The gate sidewall film 22B includes an element that is not contained in the gate sidewall film 22A and more specifically an element that enhances the etching rate. The element that enhances the etching rate is, for example, arsenic (As), phosphorus (P), boron (B), indium (In), carbon (C) and germanium (Ge). The gate Sidewall film 22B includes at least one of these elements.</p> <p>[0043] A pMOSFET includes a n-type well region 12, extension regions is, Source/drain regions 16, a gate insulation film 19A, a gate electrode 20A, offset spacers 21A and gate sidewall films 22A. An nMOSFET includes a p-type well region 13, extension regions 17, source/drain regions 18, a gate insulation film 19B, a gate electrode 20B, offset spacers 21B and gate sidewall films 22B.</p> <p>[0044] 0044) In the semiconductor device described above, the offset Spacers and/or the gate Sidewall films can be varied in thickness between the nMOSFET and pMOSFET. Thus each of the offset Spacers and the gate Sidewall films may be optimized in thickness without deteriorating from predetermined characteristics of nMOSFETs and pMOSFETs. In particular, the offset spacers can be adjusted in thickness between the nMOSFET and pMOSFET and thus the location of the extension regions, which is formed on the underside of the gate sidewall films formed outside of the offset spacers, can be controlled. Accordingly, the characteristics of the nMOSFET and pMOSFET can be optimized.</p> <p>[0045] Moreover, the offset spacer and the gate sidewall film, which were undesirably thick, can be thinned. Further miniaturization of a Semiconductor integrated circuit including the nMOSFETs and the pMOSFETs can be achieved.</p>

Claim	Claim Language	Exemplary Disclosures in Additional References
		<div data-bbox="272 233 812 1371"> </div> <p style="text-align: center;">FIG. 9</p> <p><i>See, e.g., U.S. Pat. App. Pub. No. 2009/0039445 to Wu ("Wu '445") at:</i></p> <p>[0002] This invention generally relates to processes for forming semiconductor device integrated circuits including CMOS and MOSFET devices and more particularly to mixed signal devices (i.e., analog and digital) and a method for forming the same to simultaneously optimize offset spacer widths to improve performance of both analog and digital CMOS devices including system on chip (SOC) devices.</p> <p>[0011] provides MOSFET gate structures including respective multiple width offset spacers and a method of forming the same.</p>

Claim	Claim Language	Exemplary Disclosures in Additional References
		<p>[0012] In a first embodiment, the method includes providing a semiconductor substrate including at least two gate structures; growing a silicon oxide layer having a respective differential thickness over the at least two gate structures; forming a dielectric layer on the silicon oxide layer having an etching selectivity with respect to the silicon oxide layer; forming offset spacers having a differential thickness including the dielectric layer and the silicon oxide layer adjacent either side of the at least two respective gate structures; and, carrying out an ion implant process adjacent the offset spacers to form doped regions in the semiconductor substrate forming at least two MOSFET devices.</p> <p>[0020] Referring to FIG. 1B, a patterned photoresist layer 18 is then formed to cover selected gate structures. For example, in the dual device gate structure formation process shown, gate structure 12A is covered while leaving gate structure 12B uncovered. Following formation of patterned photoresist layer 18, in an important aspect of the invention, an ion implantation process is carried out to ion implant uncovered gate structure 12B and adjacent substrate areas with one of a thermal oxidation rate enhancing or thermal oxidation rate suppressing ion implant. For example, in the embodiment as shown, fluorine ions (e.g., F-) are used in the ion implant process to enhance a subsequent thermal oxidation rate in growing a thermal oxide (SiO₂) over the gate structures 12A and 12B as well as adjacent substrate areas. Alternatively, a thermal oxidation rate suppressing ion implant such as a nitrogen (e.g., N-) implant may be used to suppress a subsequent thermal oxidation rate and thereby a subsequent SiO₂ thermal oxide thickness is reduced.</p>

Claim	Claim Language	Exemplary Disclosures in Additional References
		 <p data-bbox="748 951 792 1115">FIG. 1B</p> <p data-bbox="881 191 1279 1396">[0021] Referring to FIG. 1C, following the ion implant process and stripping of the patterned photoresist layer 18, a conventional thermal oxide growth process is carried out, for example, a wet or dry oxidation process at temperatures of about 900° C. to about 1050° C., to grow a silicon oxide (SiO₂) layer over gate structures 12A and 12B as well as adjacent substrate 10 portions. In an important aspect of the invention, the SiO₂ layer formed over the gate structures are formed to have a differential thickness. For example, in the embodiment shown, SiO₂ layer portion 20B, grown over the area subjected to the fluorine ion implant including gate structure 12B, is formed have a relatively greater thickness compared to SiO₂ layer portion 20A grown over the photoresist covered area including gate structure 12A. The differential thickness is advantageously formed as a result of the oxide growth rate enhancing fluorine ion implantation over the gate structure 12B and adjacent substrate portions.</p>

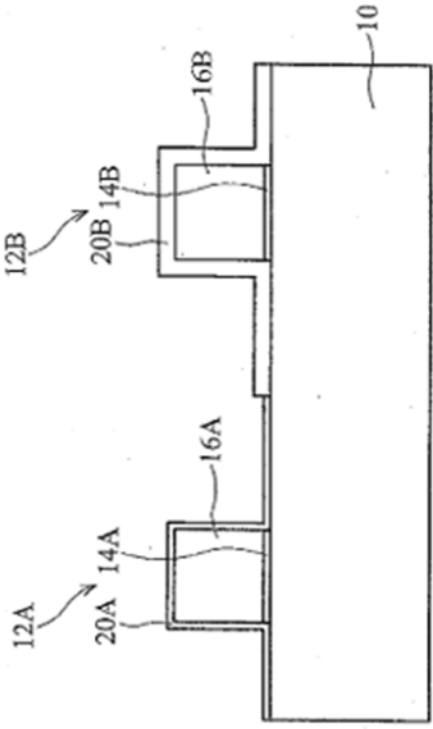
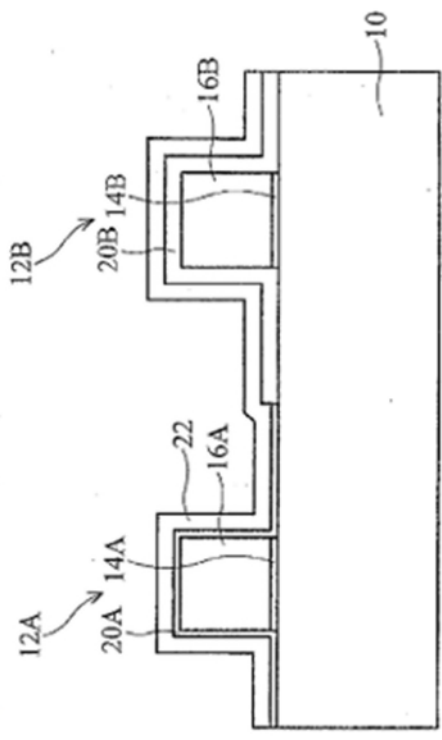
Claim	Claim Language	Exemplary Disclosures in Additional References
		 <p data-bbox="738 955 771 1123">FIG. 1C</p> <p data-bbox="795 191 1193 1396">[0022] It will be appreciated that an oxide growth suppressing ion implant may be used to form the differentially thick SiO₂ thermal oxide layer. For example, a nitrogen ion implant may be carried out over gate structure 12A while covering gate structure 12B with photoresist such that the similar differentially thick SiO₂ layer portions 20A and 20B will be formed. It will also be appreciated that a greater differential thickness between oxide layer portions e.g., 20A and 20B may be formed by carrying out both an oxide growth enhancing implant over one gate structure e.g., 12B as well as an oxide growth suppressing implant over another gate structure e.g., 12A. Preferably, the relatively thinner oxide layer portion e.g., 20A is formed at a thickness between about 10 Angstroms to about 50 Angstroms and the relatively thicker oxide layer portion e.g., 20B is formed at a thickness between about 20 Angstroms to 80 Angstroms</p> <p data-bbox="1234 191 1372 1396">[0023] Referring to FIG. 1D a dielectric layer 22 is blanket deposited, e.g., by CVD or PECVD over the oxide layers 20A and 20B. The dielectric layer 22 preferably has an etching selectivity with respect to the underlying thermal oxide layer portions e.g., 20A and 20B, for example, formed of a nitride material such as silicon nitride (e.g., SiN) and/or silicon</p>

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Claim	Claim Language	Exemplary Disclosures in Additional References
		<p>oxynitride (e.g., SiON). The dielectric layer 22 is preferably deposited having a thickness range of about 20 Angstroms to about 80 Angstroms.</p>  <p style="text-align: center;">FIG. 1D</p> <p>[0024] Referring to FIG. 1E, conventional dry and/or wet etching processes, are then carried out to etch back the dielectric layer 22 and oxide layer portions, 20A and 20B, to form composite oxide/nitride offset spacers e.g., 24A and 24B, adjacent either side of the gate structures 12A and 12B.</p>

Claim	Claim Language	Exemplary Disclosures in Additional References
		<div data-bbox="256 310 857 1354"> </div> <p data-bbox="878 701 932 919" style="text-align: center;">FIG. 1E</p> <p data-bbox="987 191 1094 1396">[0028] It will also be appreciated that the method of the present invention may be used to form CMOS devices on a single chip having multiple widths as well as the dual width offset spacer (analog/digital) CMOS devices shown in the exemplary embodiment.</p> <p data-bbox="1133 191 1354 1396">[0029] It will additionally be appreciated that the dual offset spacer widths may be used to form logic and SRAM devices, for example the relatively thicker offset spacer width forming a portion of SRAM transistors and the relatively thinner offset spacer widths forming a portion of logic transistors. In addition, dual spacer widths may be used to form an NMOS SRAM cell transistor (relatively thicker offset spacer width) and a PMOS SRAM cell transistor (relatively thinner offset spacer width).</p>

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Claim	Claim Language	Exemplary Disclosures in Additional References
		<p>[0030] Referring to FIG. 2, is shown a process flow diagram including several embodiments of the present invention. In process 201, gate structures are provided on a semiconductor substrate. In process 203, a thermally grown oxide layer is formed over the gate structures and adjacent substrate portions to form at least two different thermal oxide layer thicknesses over respective gate structures. In process 205, a dielectric layer with an etching selectivity with respect to the thermal oxide layer is formed on the thermal oxide layer. In process 207, etching processes are carried to form at least two different pair of offset spacers and associated respective maximum widths adjacent respective gate structures. In process 209, ion implant processes are carried out to form doped regions adjacent the offset spacers to form at least two operationally different transistor devices.</p>

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Claim	Claim Language	Exemplary Disclosures in Additional References
		<pre> graph TD 201[provide gate structures on a semiconductor substrate] --> 203[form at least two different thermal oxide layer thicknesses over respective gate structures] 203 --> 205[form a dielectric layer on the thermal oxide layer] 205 --> 207[form at least two different pair of offset spacer widths adjacent respective gate structures] 207 --> 209[carry out ion implant to form at least two operationally different transistor devices] </pre> <p style="text-align: center;">FIG. 2</p> <p><i>See, e.g., U.S. Pat. No. 6,946,709 to Yang ("Yang") at:</i></p> <p>3:51-62: A first embodiment of the invention is shown in FIGS. 1-9. FIG. 1 Shows the PFET 120 and NFET 118 devices separated by a shallow trench isolation (STI) region 122 in the Substrate 110. The gate conductor 112 is patterned and a thin Spacer 114 is formed to offset extension ion implants to the channel. FIG. 2 shows a thin oxide liner 124 (such as 100 Å</p>

Claim	Claim Language	Exemplary Disclosures in Additional References
		<p>thick LTO) that is deposited over the gate conductors 112 and the thin Spacers 114. A protective mask 128, Such as a photoresist, is applied and patterned to cover PFET devices 120 in FIG. 3. Then, the thin oxide 124 is removed to the expose NFET devices 118 by either reactive ion etching (RIE) or wet etching chemicals, as shown in FIG. 4. The mask 128 is then removed.</p> <p>The diagrams illustrate the process of removing thin oxide 124 to expose NFET devices 118. FIG. 2 shows a cross-section of the device with gate conductors 112, thin spacers 114, and a thin oxide layer 124. A protective mask 128 is applied over the PFET devices 120. FIG. 3 shows the mask 128 being patterned to cover the PFET devices 120. FIG. 4 shows the thin oxide 124 being removed to expose the NFET devices 118.</p>

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Claim	Claim Language	Exemplary Disclosures in Additional References
		<p>3:65-4:10: A second thin oxide layer 130, as shown in FIG. 5, (such as 50 Å thick LTO) is deposited after the photoresist 128 is removed from the wafer. This process adds thickness to the oxide 124. Therefore, the oxide 124 is thicker than the oxide 130 and the PFET devices 120 have a thicker total oxide layer 124 than the NFET devices 118. FIG. 6 shows a spacer 134 (such as Si₃N₄) that is formed to offset source and drain ion implants. In this embodiment, total Spacers size (thickness) is determined by the combined thicknesses of the spacer 134 along with the oxide 124, 130. Thus, the NFET devices 118 have a thinner total Spacer Size and hence a Shorter extension and lower extension resistance. The Source/drain extension implant is made at this point.</p>

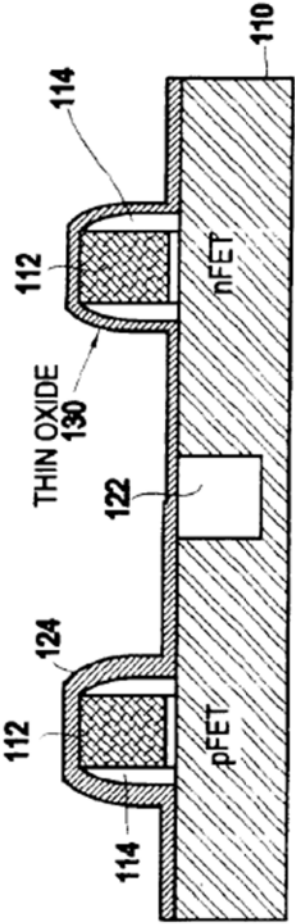
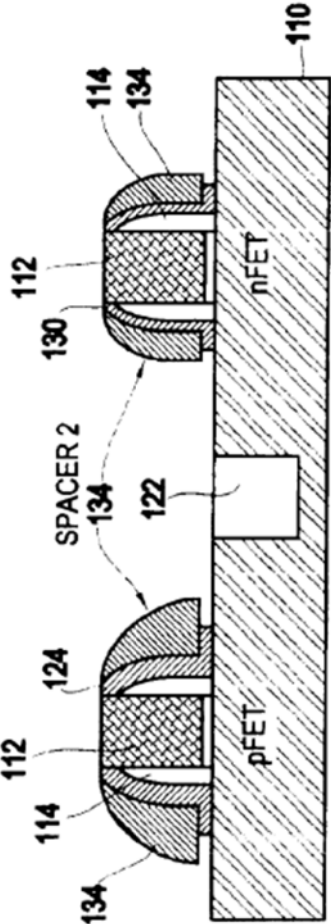
Claim	Claim Language	Exemplary Disclosures in Additional References
		<div><p>FIG. 5</p></div> <div><p>FIG. 6</p></div> <p>4:11-38: FIG. 7 shows that the wafer is wet cleaned in HF chemicals as normally required before silicide (e.g., cobalt) formation. The amount of recess of oxide 138 under the spacer nitride 134 is determined by the oxide 124 thickness in the PFET device 120. The same is true for the NFET device 118. Since the NFET has a thinner oxide layer 130 it has a thinner recess 136. FIG. 8 shows that metal is sputtered and Silicidation anneals are performed to form Silicide over the Spacers to form a shallow silicide (item 140 for the PFET devices 120 and item 142 for the NFET devices 118) in the extension regions to reduce Series resistance.</p>

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Claim	Claim Language	Exemplary Disclosures in Additional References
		<p>The contact etch Stopping layer 150 is deposited, as shown in FIG. 9, and additional, well-known process Steps are performed to complete the Structure. In the second embodiment, shown in FIGS. 10-13, the NFET 118 oxide spacer 124 may be thinned or completely removed (as shown in FIG. 10) to further reduce NFET extension length. More specifically, FIG. 10 shows that the NFET 118 thin oxide layer 114 and oxide spacer 124 is etched using, for example, HF containing chemicals. Again, a thick oxide (such as 50 Å thick LTO) 130 is deposited after the photoresist 128 is removed in FIG. 11. The Si3N4 spacer 134 is formed in FIG. 12. With this embodiment, an even shorter NFET extension is realized. FIG. 13 shows the Structure after the Silicidation is performed, which again reduces extension resistance for both NFET and PFET devices.</p> <p>See 2[a]-[b]</p>

Claim	Claim Language	Exemplary Disclosures in Additional References
7	<p>The semiconductor device of claim 2, wherein each of the first insulating spacers and the second insulating spacers is made of a silicon nitride film.</p>	<p>The following references disclose and/or render obvious a “The semiconductor device of claim 2, wherein each of the first insulating spacers and the second insulating spacers is made of a silicon nitride film” as further described below.</p> <p>See, e.g., U.S. Pat. App. Pub. No. 2004/0188769 to Tsuno (“Tsuno”) at:</p> <p>[0039] The offset spacer 21B is thinner than the offset spacer 21A. For example, the bottom portion of the offset spacer 21B, which contacts the Semiconductor Substrate 11, is about 6 nm to 10 nm in thickness and the bottom portion of the offset spacer 21A, which contacts the semiconductor substrate 11, is about 12 nm in thickness. The gate sidewall film 22B is thinner than the gate sidewall film 22A. For example, the bottom portion of the gate Sidewall film 22A, which contacts the semiconductor Substrate 11, is about 70 nm in thickness and thicker than the bottom portion of the gate Sidewall film 22B which contacts the Semiconductor Substrate 11.</p> <p>[0040] The offset spacers 21A and 21B are each made of an insulation film Such as a TEOS (tetraethylorthosilicate) film and a silicon nitride film. The offset spacer 21B includes an</p>

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Claim	Claim Language	Exemplary Disclosures in Additional References
		<p>element that is not contained in the offset spacer 21A and more specifically an element that enhances the etching rate. The element that enhances the etching rate is, for example, arsenic (AS), phosphorus (P), boron (B), indium (In), carbon (C) and germanium (Ge). The offset spacer 21B includes at least one of these elements.</p> <p>See 2[a]-[b]</p>

Claim	Claim Language	Exemplary Disclosures in Additional References
12	<p>The semiconductor device of claim 1, wherein each of the first and second high dielectric constant insulating films contains hafnium or zirconium.</p>	<p>The following references disclose and/or render obvious a “The semiconductor device of claim 1, wherein each of the first and second high dielectric constant insulating films contains hafnium or zirconium.” as further described below.</p> <p>See, e.g., U.S. Pat. No. 6,787,421 to Gilmer et al. (“Gilmer”) at: [3:44-4:7] Now that gate dielectrics of two different thicknesses have been formed, a high-k dielectric (generally with $k > 4$, preferably with $k > 6$, and most preferably with $k > 7$) is deposited over semiconductor device 10. In a preferred embodiment, this high-k dielectric is a metal oxide, Such as metal oxide 26 shown in FIG. 3. Suitable materials for metal oxide 26 preferably include hafnium oxide (HfO₂), hafnium silicate (HfSiO₂), or lanthanum aluminate (LaAlO₃), but lanthanum oxide, hafnium aluminate, Zirconium oxide, and Zirconium Silicate, and other like materials, may also be Suitable high-k dielectrics. The thickness of the high-k dielectric layer will be dependent on the particular device requirements in each region of the Substrate (the core region and the I/O region), but generally it is believed the thickness of a metal oxide will be between about 15-50 angstroms (1.5-5.0 nanometers). The underlying thicknesses of first gate dielectric 16 and Second gate dielectric 20 will also affect the choice of thickness of the high-k dielectric. The thickness of the high-k dielectric should be chosen So that its equivalent oxide thickness (EOT), when added to the EOT of the first gate dielectric 16 (I/O device dielectric) thickness or Second gate dielectric 20 (core device dielectric) thickness, provides a total EOT appropriate for the I/O and core device, respectively. Similarly, this calculation should be used to determine the initial deposited or grown thicknesses of the first and Second gate dielectrics. Because metal oxide</p>

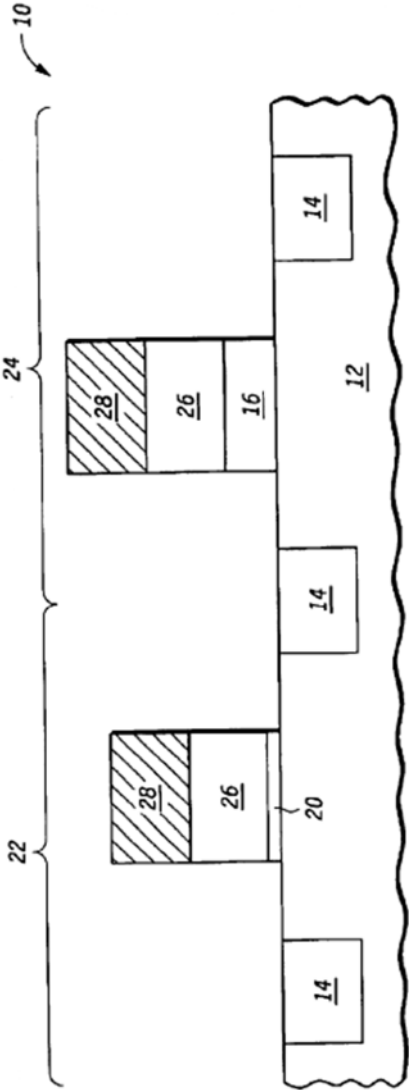
Claim	Claim Language	Exemplary Disclosures in Additional References
		<p>26 is deposited as a single blanket deposition, its thickness will not vary much across the Substrate Surface and thus one should use the thicknesses of the first and Second dielectrics as the “variables” to achieve the final EOTs for the core and I/O devices.</p>  <p>FIG. 4</p> <p><i>See, e.g., Japanese Patent App. Pub. No. JP2006/060155 to Yasuhira et al. (“Yasuhira”) at:</i></p> <p>In the above invention, the high dielectric constant insulating film is made of hafnia (HfO₂), zirconia (ZrO₂), hafnium silicate (HfSiOx), zirconium silicate (ZrSiOx), hafnium aluminate (HfAlOx), or zirconium aluminate (ZrAlOx). And at least one insulating film selected from the group consisting of:</p> <p>That is, an n well layer 2 is formed on the surface portion of the silicon substrate 1, and the surface portion of the n well layer 2 is partitioned by an element isolation region 3 by STI. In the MISFET in the peripheral circuit portion, the base oxide film 4 having a thickness of 4 to 6 nm and the nitride layer 4a whose surface is modified to a nitrogen-containing layer, the High-k film 5 and the surface thereof are modified to a nitrogen-containing layer. A first gate insulating film 6 made of a laminated film of the nitrided layer 5a is formed. Then, a gate electrode 9 is constituted by the polycrystalline silicon layer 7 containing the p-conductivity</p>

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Claim	Claim Language	Exemplary Disclosures in Additional References
		<p>type or n-conductivity type impurity formed on the first gate insulating film 6 and the silicide layer 8, and the first gate insulating film 6. A sidewall insulating film 10 is provided on the side wall of the gate electrode 9. Here, the base oxide film 4 is formed of a silicon oxide film, and the high-k film 5 is formed of hafnia (HfO₂), zirconia (ZrO₂), hafnium silicate (HfSiO_x), zirconium silicate (ZrSiO_x), hafnium aluminate (An insulating film having a thickness of 2 to 3 nm made of HfAlO_x) or zirconium aluminate (ZrAlO_x) is preferable. Alternatively, the High-k film 5 may be configured by an insulating film having a stacked structure in which two or more types of insulating films are selected from the high dielectric constant insulating films and stacked. A source / drain region including a source / drain diffusion layer 11 and a silicide layer 8 is provided on the surface of the n well layer 2.</p> <p>Next, a High-k film 5 is deposited on the entire surface so as to cover the base oxide film 4 and the base film 12. As the High-k film 5, for example, a thin film of HfAlO_x, HfSiO_x or HfO₂ having a relative dielectric constant of 10 to 20 is formed. It is preferable to use an ALD (Atomic Layer Deposition) method or an MOCVD (Metal Organic Chemical Vapor Deposition) method for the growth of such a High-k film. For example, when HfAlO_x is formed as the high-k film by using the ALD method, the substrate temperature is 300 ° C., and hafnium tetrachloride (HfCl₄) and trimethylaluminum (TMA) are used as the film forming raw materials. A thin film of HfAlO_x having a film thickness of 2 nm to 3 nm is formed using water vapor (H₂O) or ozone (O₃) as an oxidant (FIG. 3A). In the formation of the high-k film 5, the thin base film 12 prevents an interface reaction between the high-k film 5 and the silicon substrate 1 on the surface of the n-well layer 2.</p>

Claim	Claim Language	Exemplary Disclosures in Additional References
		<p>【図 1】</p> <p>内部回路部 周辺回路部</p> <p>See, e.g., U.S. Pat. No. 8,349,695 to Scheiper et al. (“Scheiper”) at: 3:24-62: In addition to enhancing performance of gate electrode structures by incorporating a high-k dielectric material in 25 Sophisticated semiconductor devices, frequently, transistor elements of different characteristics, for instance of different leakage behavior, have to be provided, thereby requiring a gate dielectric material of different material composition and/or of different thickness. In some conventional approaches, 30 the high-k dielectric material in combination with any work function adjusting species are provided in an early manufacturing stage, wherein a different thickness of the gate dielectric material may also be provided in different device regions in order to provide different transistor types, or any other 35 circuit</p>

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Claim	Claim Language	Exemplary Disclosures in Additional References
		<p>elements, such as polysilicon resistors and the like. It turns out, however, that the conventional process strategy for providing gate electrode structures with differently composed gate dielectrics may result in significant threshold Voltage variations, as will be described in more detail with reference to FIGS. 1a-1g.</p> <p>FIG. 1c schematically illustrates the semiconductor device 100 when exposed to a deposition ambient 106 in which a high-k dielectric material. Such as hafnium oxide, is deposited above the active regions 102A, 102B, thereby forming a high-k dielectric layer 153. Thus, the layers 152 and 153 in combination may represent the gate dielectric material of a transistor formed in and above the semiconductor region 102A, thereby providing the required characteristics for high performance transistors, while the layer 153 in combination with the “thick” silicon dioxide material 151 represents the dielectric material for transistors and other circuit elements in which a Superior performance with respect to reduced leakage currents and the like is required. It should be appreciated that the deposition process 106 may be performed on the basis of any appropriate deposition recipe, for instance, by chemical vapor deposition (CVD), physical vapor deposition (PVD) and the like. For example, a thickness of the high-k dielectric layer 153 may be in the range of one to several nanometers, depending on the overall requirements in view of capacitive coupling, leakage currents and the like.</p>

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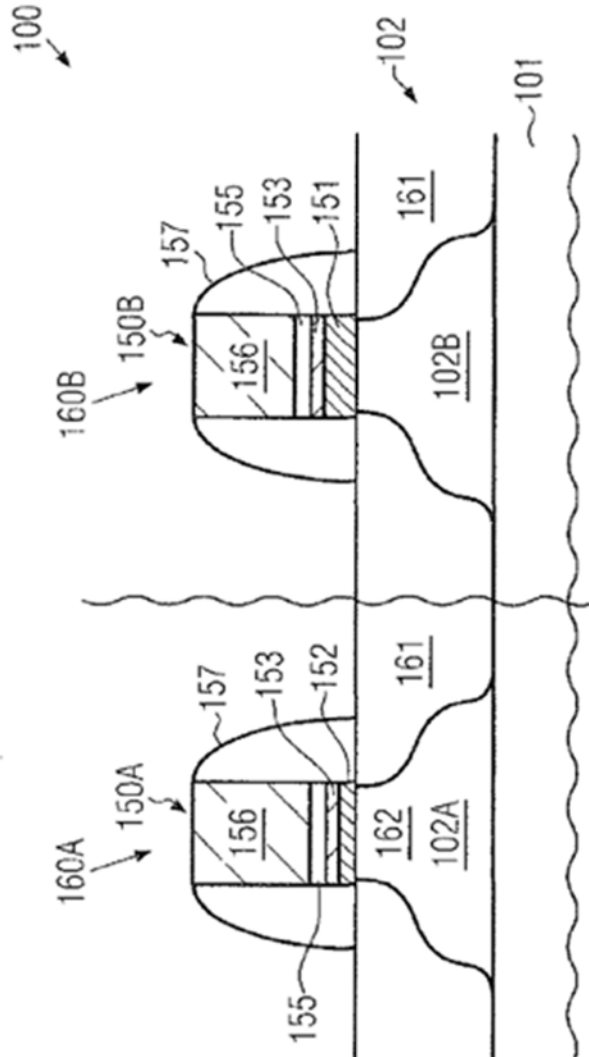
Claim	Claim Language	Exemplary Disclosures in Additional References
		 <p>FIG. 1g (prior art)</p> <p>See, e.g., U.S. Pat. No. 7,335,561 to Sakai ("Sakai '561") at: [2:31-53] The typical ones of the inventions disclosed in this application will be briefly described as follows. A semiconductor integrated circuit device of the present invention comprising: a semiconductor Substrate; a first MIS transistor including a pair of first semiconductor regions formed in the semiconductor substrate and a first conductive piece formed above the semiconductor Substrate through a first gate insulation film in a region between the pair of the first semiconductor regions; and a second MIS transistor including a pair of second semiconductor regions formed in the semiconductor Substrate and a second conductive piece formed above the semiconductor Substrate through a second gate insulation film in a region between the pair of the second semiconductor regions, wherein the thickness</p>

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Claim	Claim Language	Exemplary Disclosures in Additional References
		<p>of the first gate insulation film is larger than the thickness of the second gate insulation film and the first gate insulation film is comprised of the first insulation film located on the semiconductor Substrate and the second insulation film located on the first insulation film; and wherein the second gate insulation film is comprised of a third insulation film located on the semiconductor substrate and the dielectric constant of the second and third insulation films is larger than the dielectric constant of the first insulation film.</p> <p>[5:19-22] FIG. 35 is a major part sectional view of a semiconductor substrate showing an example of the manufacturing method of a semiconductor integrated circuit according to an embodiment of the present invention in the order of steps;</p> <p>[8:11-26] Next, as shown in FIG. 20, high dielectric constant insulation film 10, for example, alumina film is formed on the semiconductor substrate 1. The high dielectric constant insulation film 10 can be deposited according to, for example, sputtering method. The thickness of the high dielectric constant insulation film 10 formed on the semiconductor substrate 1 is set so that its effective thickness is about 5 nm. For example, the alumina film is deposited in the thickness of about 10 nm considering dielectric constant. Consequently, gate insulation film 11 comprised of the high dielectric constant insulation film 10 about 5 nm in terms of its effective thickness is formed in the region B and gate insulation film 12 comprised of stacked film of the high dielectric constant film 10 and the silicon oxide film 9 about 9 to 10 nm in terms of its effective thickness is formed in the region A</p> <p>[8:27-31] Before forming the aforementioned high dielectric constant insulation film 10 on the semiconductor substrate 1, silicon oxide film or silicon nitride film, or silicon oxide nitride film less than 1 nm or less may be formed to stabilize an interface with the semiconductor substrate 1.</p> <p>[11:5-18] As described above, according to this embodiment, after the silicon oxide film 9 is formed on the surface of the semiconductor substrate 1, the silicon oxide film 9 in the region B (region in which a gate insulation whose effective thickness is small is formed) is removed with diluted HF and after that, by forming high dielectric constant insulation film 10 on the semiconductor Substrate 1, a damage or pollution to the surface of the semiconductor</p>

Claim	Claim Language	Exemplary Disclosures in Additional References
		<p>substrate 1 is prevented so as to form two kinds of the gate insulation films, that is, the gate insulation film 12 comprised of stacked film of the high dielectric constant insulation film 10 and the silicon oxide film 9 and the gate insulation film 11 comprised of the high dielectric constant insulation film 10 on the same semiconductor Substrate 1.</p> <p>[11:19-24] Because the gate insulation film 12 in the region A is comprised of stacked film of the high dielectric constant insulation film 10 and the silicon oxide film 9, the difference in level between the region A and region B can be reduced compared to the stacked film comprised of two high dielectric constant insulation films.</p> <p>[11:31-32] Next, an example of an inverter circuit applying an embodiment of the present invention is shown in FIG. 41.</p> <p>[11:33-46] In the same Figure, a region Surrounded by dotted lines indicates a CMOS inverter and Tkp and Tnp denote p-channel MIS transistor while Tkn and Tnn denote n-channel MIS transistor. The gate insulation film of the MIS transistors Tnp, Tnn constituting the CMOS inverter is thinner than the gate insulation film of the MIS transistors Tkp, Tkn. For example, the gate insulation film of the MIS transistors Tnp, Tnn constituting the CMOS inverter is formed of high dielectric constant insulation film and its effective thickness is about 3.5 nm. The gate insulation film of the MIS transistors Tkp, Tkn is constituted of stacked film of high dielectric constant insulation film and silicon oxide film and its effective thickness is about 6 nm.</p> <p>[13:10-16] For example, although in the above-described embodiment, the high dielectric constant insulation film is regarded as alumina film, the present invention is not restricted to this example, but this high dielectric constant insulation film may be comprised of titanic oxide film (TiO), zirconium oxide film (ZrO), hafnium oxide film (HfOx), tantalum oxide film (TaC) or ruthenium oxide film (RuO).</p> <p>[13:20-37] Because the gate insulation film comprised of stacked film of high dielectric constant insulation film and silicon oxide film and the gate insulation film comprised of the high dielectric constant insulation film can be formed on the same semiconductor Substrate</p>

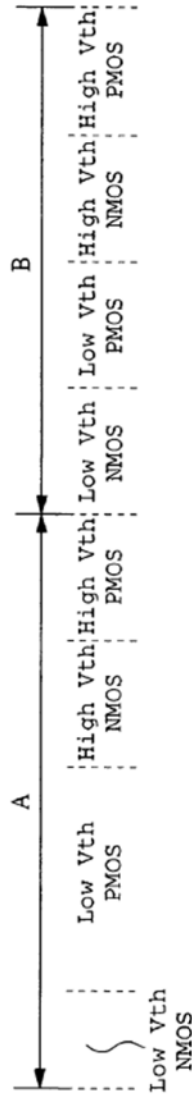
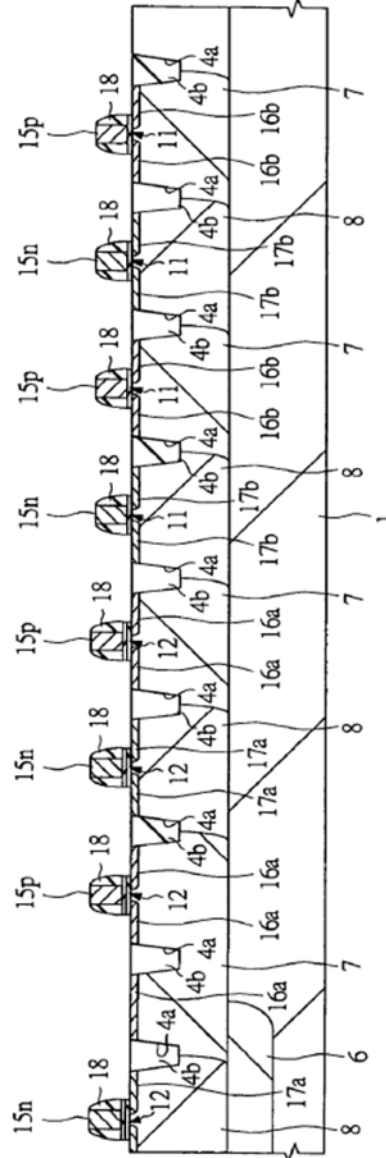
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Claim	Claim Language	Exemplary Disclosures in Additional References
		<p>so as to Suppress damage or pollution to the surface of the semiconductor substrate, plural gate insulation films each having a different thickness and a high reliability can be formed. Further, because the gate insulation film having a high effective thickness is constituted of stacked film of the high dielectric constant insulation film and silicon oxide film, a difference in step between a region in which the gate insulation film having a large effective thickness is formed and a region in which the gate insulation film having a small effective thickness is decreased as compared to a stacked film in which two high dielectric constant insulation films are stacked, so that subsequent manufacturing of the MIS transistor is facilitated.</p> <p>[Claim 1] 1. A method of manufacturing a semiconductor integrated circuit device comprising the steps of (a) forming a first insulation film over a surface of a semiconductor Substrate in a first region and a second region different from said first region of said semiconductor substrate; (b) selectively removing said first insulation film in said second region, with said first insulation film being left in said first region; (c) forming a second insulation film over said semiconductor Substrate of said second region; (d) forming a third insulation film over said first insulation film in said first region and over said second insulation film in said second region; (e) forming a first conductive layer over said third insulation film; and (f) forming a first conductive piece in said first region and a second conductive piece in said second region by patterning said first conductive layer, wherein the thickness of said first insulation film is larger than the thickness of said second insulation film; said first insulation film includes silicon and at least one of oxygen and nitrogen; said second insulation film includes silicon and at least one of oxygen and nitrogen; said third insulation film has a greater dielectric constant than each of said first and second insulation films; and the thickness of said third insulation film is larger than the thickness of said first insulation film and said second insulation film</p> <p>[Claim 8] 8. The method of manufacturing a semiconductor integrated circuit device according to claim 1, wherein said third insulation film is made of an alumina film, a titanium oxide film, a Zirconium oxide film, a hafnium oxide film, a tantalum oxide film, or a ruthenium oxide film</p>

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Exemplary Disclosures in Additional References

FIG. 35



See, e.g., U.S. Pat. App. Pub. No. 2009/0039445 to Wu ("Wu '445") at:

[0018] Still referring to FIG. 1A, the gate structures 12A and 12B may be formed by conventional CVD deposition, lithographic patterning, and plasma (dry) etching methods known in the art. The gate dielectric portions 14A and 14B may be formed by any process known in the art, e.g., thermal oxidation, nitridation, sputter deposition, chemical vapor deposition, or combinations thereof. The gate dielectric portions 14A and 14B may be formed of silicon oxide, silicon nitride, silicon oxynitride, and high-K dielectrics (e.g., $K > 8$)

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Claim	Claim Language	Exemplary Disclosures in Additional References
		<p>including transition metal oxide and rare earth metal oxides. For example, high-K dielectrics may be formed of aluminum oxides (e.g., Al₂O₃), hafnium oxides (e.g., HfO₂), hafnium oxynitrides (HfON), hafnium silicates (e.g. HfSiO₄), hafnium silicon oxynitrides (e.g., HfSixOyNz), zirconium oxides (e.g., ZrO₂), zirconium oxynitrides (e.g., ZrON), zirconium silicon oxides (e.g., ZrSiO₂), yttrium oxides (Y₂O₃), lanthanum oxides (La₂O₃), cerium oxides (CeO₂), titanium oxides (TiO₂), tantalum oxides (Ta₂O₅), or combinations thereof. The high-k dielectric layer may be formed by known CVD methods such as atomic layer CVD (ALCVD) and metal-organic CVD (MOCVD). It will be appreciated that the high-K dielectric layer may include a lowermost interfacial layer formed on the semiconductor substrate such as an oxide or oxynitride (not shown).</p> <p>See 1[d]-[e]</p>

Claim	Claim Language	Exemplary Disclosures in Additional References
13	The semiconductor device of claim 1, wherein the first and second high dielectric constant insulating films are equal in thickness.	<p>The following references disclose and/or render obvious a “The semiconductor device of claim 1, wherein the first and second high dielectric constant insulating films are equal in thickness.” as further described below.</p> <p>See, e.g., U.S. Pat. No. 6,787,421 to Gilmer et al. (“Gilmer”) at:</p> <p>[3:44-4:7] Now that gate dielectrics of two different thicknesses have been formed, a high-k dielectric (generally with $k > 4$, preferably with $k > 6$, and most preferably with $k > 7$) is deposited over semiconductor device 10. In a preferred embodiment, this high-k dielectric is a metal oxide, Such as metal oxide 26 shown in FIG. 3. Suitable materials for metal oxide 26 preferably include hafnium oxide (HfO₂), hafnium silicate (HfxSlyOz), or lanthanum aluminate (LaAlO₃), but lanthanum oxide, hafnium aluminate, Zirconium oxide, and Zirconium Silicate, and other like materials, may also be Suitable high-k dielectrics. The thickness of the high-k dielectric layer will be dependent on the particular device requirements in each region of the Substrate (the core region and the I/O region), but generally it is believed the thickness of a metal oxide will be between about 15-50 angstroms (1.5-5.0</p>

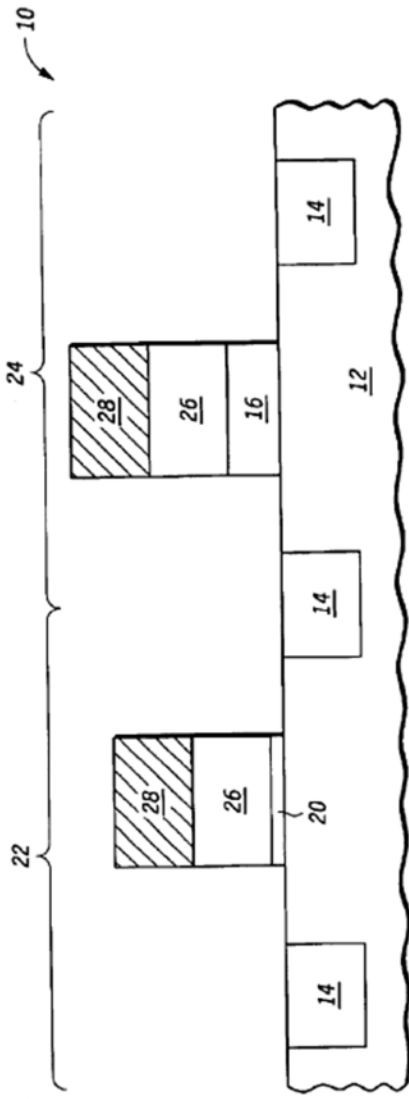
Claim	Claim Language	Exemplary Disclosures in Additional References
		<p>nanometers). The underlying thicknesses of first gate dielectric 16 and Second gate dielectric 20 will also affect the choice of thickness of the high-k dielectric. The thickness of the high-k dielectric should be chosen So that its equivalent oxide thickness (EOT), when added to the EOT of the first gate dielectric 16 (I/O device dielectric) thickness or Second gate dielectric 20 (core device dielectric) thickness, provides a total EOT appropriate for the I/O and core device, respectively. Similarly, this calculation should be used to determine the initial deposited or grown thicknesses of the first and Second gate dielectrics. Because metal oxide 26 is deposited as a single blanket deposition, its thickness will not vary much across the Substrate Surface and thus one should use the thicknesses of the first and Second dielectrics as the “variables” to achieve the final EOTs for the core and I/O devices.</p>  <p><i>FIG. 4</i></p> <p>See, e.g., U.S. Pat. No. 8,349,695 to Scheiper et al. (“Scheiper”) at: 3:24-62: In addition to enhancing performance of gate electrode structures by incorporating a high-k dielectric material in 25 Sophisticated semiconductor devices, frequently, transistor elements of different characteristics, for instance of different leakage behavior, have to be provided, thereby requiring a gate dielectric material of different material composition and/</p>

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Claim	Claim Language	Exemplary Disclosures in Additional References
		<p>or of different thickness. In some conventional approaches, 30 the high-k dielectric material in combination with any work function adjusting species are provided in an early manufacturing stage, wherein a different thickness of the gate dielectric material may also be provided in different device regions in order to provide different transistor types, or any other 35 circuit elements, such as polysilicon resistors and the like. It turns out, however, that the conventional process strategy for providing gate electrode structures with differently composed gate dielectrics may result in significant threshold Voltage variations, as will be described in more detail with reference to FIGS. 1a-1g.</p> <p>4:37-56: FIG. 1c schematically illustrates the semiconductor device 100 when exposed to a deposition ambient 106 in which a high-k dielectric material. Such as hafnium oxide, is deposited above the active regions 102A, 102B, thereby forming a high-k dielectric layer 153. Thus, the layers 152 and 153 in combination may represent the gate dielectric material of a transistor formed in and above the semiconductor region 102A, thereby providing the required characteristics for high performance transistors, while the layer 153 in combination with the “thick” silicon dioxide material 151 represents the dielectric material for transistors and other circuit elements in which a Superior performance with respect to reduced leakage currents and the like is required. It should be appreciated that the deposition process 106 may be performed on the basis of any appropriate deposition recipe, for instance, by chemical vapor deposition (CVD), physical vapor deposition (PVD) and the like. For example, a thickness of the high-k dielectric layer 153 may be in the range of one to several nanometers, depending on the overall requirements in view of capacitive coupling, leakage currents and the like.</p>

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Claim	Claim Language	Exemplary Disclosures in Additional References
		<p>between the pair of the first semiconductor regions; and a second MIS transistor including a pair of second semiconductor regions formed in the semiconductor Substrate and a second conductive piece formed above the semiconductor Substrate through a second gate insulation film in a region between the pair of the second semiconductor regions, wherein the thickness of the first gate insulation film is larger than the thickness of the second gate insulation film and the first gate insulation film is comprised of the first insulation film located on the semiconductor Substrate and the second insulation film located on the first insulation film; and wherein the second gate insulation film is comprised of a third insulation film located on the semiconductor substrate and the dielectric constant of the second and third insulation films is larger than the dielectric constant of the first insulation film.</p> <p>[5:19-22] FIG. 35 is a major part sectional view of a semiconductor substrate showing an example of the manufacturing method of a semiconductor integrated circuit according to an embodiment of the present invention in the order of steps;</p> <p>[8:11-26] Next, as shown in FIG. 20, high dielectric constant insulation film 10, for example, alumina film is formed on the semiconductor substrate 1. The high dielectric constant insulation film 10 can be deposited according to, for example, sputtering method. The thickness of the high dielectric constant insulation film 10 formed on the semiconductor substrate 1 is set so that its effective thickness is about 5 nm. For example, the alumina film is deposited in the thickness of about 10 nm considering dielectric constant. Consequently, gate insulation film 11 comprised of the high dielectric constant insulation film 10 about 5 nm in terms of its effective thickness is formed in the region B and gate insulation film 12 comprised of stacked film of the high dielectric constant film 10 and the silicon oxide film 9 about 9 to 10 nm in terms of its effective thickness is formed in the region A</p> <p>[8:27-31] Before forming the aforementioned high dielectric constant insulation film 10 on the semiconductor substrate 1, silicon oxide film or silicon nitride film, or silicon oxide nitride film less than 1 nm or less may be formed to stabilize an interface with the semiconductor substrate 1.</p>

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		<p>[11:5-18] As described above, according to this embodiment, after the silicon oxide film 9 is formed on the surface of the semiconductor substrate 1, the silicon oxide film 9 in the region B (region in which a gate insulation whose effective thickness is small is formed) is removed with diluted HF and after that, by forming high dielectric constant insulation film 10 on the semiconductor Substrate 1, a damage or pollution to the surface of the semiconductor substrate 1 is prevented So as to form two kinds of the gate insulation films, that is, the gate insulation film 12 comprised of stacked film of the high dielectric constant insulation film 10 and the silicon oxide film 9 and the gate insulation film 11 comprised of the high dielectric constant insulation film 10 on the same semiconductor Substrate 1.</p> <p>[11:19-24] Because the gate insulation film 12 in the region A is comprised of stacked film of the high dielectric constant insulation film 10 and the silicon oxide film 9, the difference in level between the region A and region B can be reduced compared to the stacked film comprised of two high dielectric constant insulation films.</p> <p>[11:31-32] Next, an example of an inverter circuit applying an embodiment of the present invention is shown in FIG. 41.</p> <p>[11:33-46] In the same Figure, a region Surrounded by dotted lines indicates a CMOS inverter and Tkp and Tnp denote p-channel MIS transistor while Tkn and Tnn denote n-channel MIS transistor. The gate insulation film of the MIS transistors Tnp, Tnn constituting the CMOS inverter is thinner than the gate insulation film of the MIS transistors Tkp, Tkn. For example, the gate insulation film of the MIS transistors Tnp, Tnn constituting the CMOS inverter is formed of high dielectric constant insulation film and its effective thickness is about 3.5 nm. The gate insulation film of the MIS transistors Tkp, Tkn is constituted of stacked film of high dielectric constant insulation film and silicon oxide film and its effective thickness is about 6 mm.</p> <p>[13:10-16] For example, although in the above-described embodiment, the high dielectric constant insulation film is regarded as alumina film, the present invention is not restricted to this example, but this high dielectric constant insulation film may be comprised of titanic</p>

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		<p>oxide film (TiO), zirconium oxide film (ZrO), hafnium oxide film (HfOx), tantalum oxide film (TaC) or ruthenium oxide film (RuO).</p> <p>[13:20-37] Because the gate insulation film comprised of stacked film of high dielectric constant insulation film and silicon oxide film and the gate insulation film comprised of the high dielectric constant insulation film can be formed on the same semiconductor Substrate so as to Suppress damage or pollution to the surface of the semiconductor substrate, plural gate insulation films each having a different thickness and a high reliability can be formed. Further, because the gate insulation film having a high effective thickness is constituted of stacked film of the high dielectric constant insulation film and silicon oxide film, a difference in step between a region in which the gate insulation film having a large effective thickness is formed and a region in which the gate insulation film having a small effective thickness is decreased as compared to a stacked film in which two high dielectric constant insulation films are stacked, so that subsequent manufacturing of the MIS transistor is facilitated.</p> <p>[Claim 1] 1. A method of manufacturing a semiconductor integrated circuit device comprising the steps of (a) forming a first insulation film over a surface of a semiconductor Substrate in a first region and a second region different from said first region of said semiconductor substrate; (b) selectively removing said first insulation film in said second region, with said first insulation film being left in said first region; (c) forming a second insulation film over said semiconductor Substrate of said second region; (d) forming a third insulation film over said first insulation film in said first region and over said second insulation film in said second region; (e) forming a first conductive layer over said third insulation film; and (f) forming a first conductive piece in said first region and a second conductive piece in said second region by patterning said first conductive layer, wherein the thickness of said first insulation film is larger than the thickness of said second insulation film; said first insulation film includes silicon and at least one of oxygen and nitrogen; said second insulation film includes silicon and at least one of oxygen and nitrogen; said third insulation film has a greater dielectric constant than each of said first and second insulation films; and the thickness of said third insulation film is larger than the thickness of said first insulation film and said second insulation film</p>

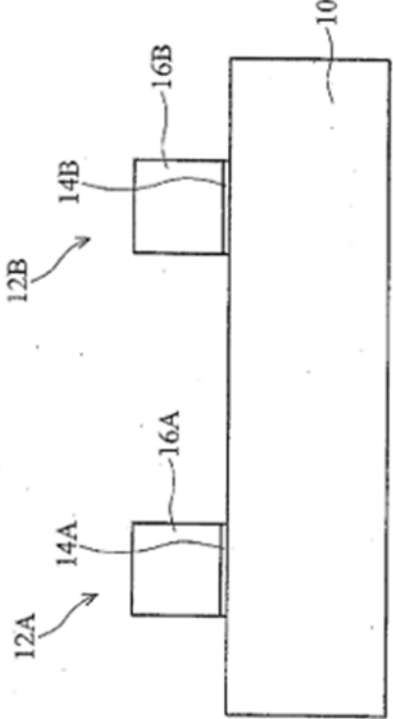
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		<p>[Claim 8] 8. The method of manufacturing a semiconductor integrated circuit device according to claim 1, wherein said third insulation film is made of an alumina film, a titanium oxide film, a Zirconium oxide film, a hafnium oxide film, a tantalum oxide film, or a ruthenium oxide film</p> <p>FIG. 35</p> <p>See, e.g., U.S. Pat. App. No. 2009/0039445 to Wu ("Wu '445") at:</p>

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		<p>[0017] Referring to FIG. 1A, in an exemplary implementation of the present invention, is shown a semiconductor substrate 10 having overlying gate structures 12A and 12B including respective gate dielectric portions 14A and 14B and respective overlying gate electrode portions 16A and 16B. Gate dielectric portions and overlying gate electrode portions of gate structures 12A and 12B may be formed by conventional deposition, lithographic and etching processes. The semiconductor substrate 10, may include, but is not limited to, silicon, silicon on insulator (SOI) stacked SOI (SSOI), stacked SiGe on insulator (S—SiGeOI), SiGeOI, and GeOI, or combinations thereof. It will be appreciated that an electrical isolation structure such as a shallow trench isolation (STI) structure (not shown) may be provided between gate structures 12A and 12B to isolate the respective MOSFET devices.</p> <p>[0018] Still referring to FIG. 1A, the gate structures 12A and 12B may be formed by conventional CVD deposition, lithographic patterning, and plasma (dry) etching methods known in the art. The gate dielectric portions 14A and 14B may be formed by any process known in the art, e.g., thermal oxidation, nitridation, sputter deposition, chemical vapor deposition, or combinations thereof. The gate dielectric portions 14A and 14B may be formed of silicon oxide, silicon nitride, silicon oxynitride, and high-K dielectrics (e.g., K>8) including transition metal oxide and rare earth metal oxides. For example, high-K dielectrics may be formed of aluminum oxides (e.g., Al₂O₃), hafnium oxides (e.g., HfO₂), hafnium oxynitrides (HfON), hafnium silicates (e.g. HfSiO₄), hafnium silicon oxynitrides (e.g., HfSixOyNz), zirconium oxides (e.g., ZrO₂), zirconium oxynitrides (e.g., ZrON), zirconium silicon oxides (e.g., ZrSiO₂), yttrium oxides (Y₂O₃), lanthanum oxides (La₂O₃), cerium oxides (CeO₂), titanium oxides (TiO₂), tantalum oxides (Ta₂O₅), or combinations thereof. The high-k dielectric layer may be formed by known CVD methods such as atomic layer CVD (ALCVD) and metal-organic CVD (MOCVD). It will be appreciated that the high-K dielectric layer may include a lowermost interfacial layer formed on the semiconductor substrate such as an oxide or oxynitride (not shown).</p> <p>[0019] The gate electrode portions, 16A and 16B may be formed of poly gate such as polysilicon, amorphous polysilicon, doped polysilicon, polysilicon-germanium, or metal gate such as TaC, TaN, TiN, MoN or combinations thereof). For example, a gate dielectric layer is first formed by CVD, sputtering or thermal growth processes followed by deposition of an</p>

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		<p>overlying gate electrode material and an optional hardmask layer (not shown). Conventional lithographic patterning and dry etching processes are then carried out to form the gate structures 12A and 12B.</p>  <p>FIG. 1A</p> <p>See 1[d]-[e]</p>