INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	
	Filing Date	
	First Named Inventor	Chin-I Liao
	Art Unit	N/A
	Examiner Name	N/A
	Attorney Docket Number	NAUP1863USA3

U.S.PATENTS						
Examiner Initial*	Cite No	Patent Number	Kind Code	Issue Date	Name	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	8455313	B1	2013-06-04	Basker	
	2	6043138		2000-03-28	Ibok; Effiong E.	all
	3	6492216		2002-12-10	Yeo; Yee-Chia	all
	4	6921963		2005-07-26	Krivokapic; Zoran	all
	5	7087477		2006-08-08	Fried; David M.	all
	6	7091551		2006-08-15	Anderson; Brent A.	all
	7	7247887		2007-07-24	King; Tsu-Jae	all
	8	7250658		2007-07-31	Doris; Bruce B.	all

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
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	Art Unit	N/A
	Examiner Name	N/A
	Attorney Docket Number	NAUP1863USA3

	9	7309626		2007-12-18	Ieong; Mei-Kei	all
	10	7352034		2008-04-01	Booth, Jr.; Roger Allen	all
	11	7470570		2008-12-30	Beintner; Jochen	all
	12	7531437		2009-05-12	Brask; Justin K.	all
	13	7569857		2009-08-04	Simon, legal representative; David	all
	14	6888181		2005-05-03	Liao	
	15	8362575		2013-01-29	Kwok	

U.S.PATENT APPLICATION PUBLICATIONS

Examiner Initial*	Cite No	Publication Number	Kind Code	Publication Date	Name	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	20130200470	A1	2013-08-08	Liu	
	2	20040195624		2004-10-07	Liu, Chee-Wee;	all

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	
	Filing Date	
	First Named Inventor	Chin-I Liao
	Art Unit	N/A
	Examiner Name	N/A
	Attorney Docket Number	NAUP1863USA3

	3	20050051825		2005-03-10	Fujiwara, Makoto;	all
	4	20060099830		2006-05-11	Walther; Steven R.;	all
	5	20060286729		2006-12-21	Kavalieros; Jack;	all
	6	20070108528		2007-05-17	Anderson; Brent A.;	all
	7	20070158756		2007-07-12	Dreeskornfeld; Lars;	all
	8	20080157208		2008-07-03	Fischer; Kevin J.;	all
	9	20090124097		2009-05-14	Cheng; Kangguo;	all
	10	20090242964		2009-10-01	Akil; Nader;	all
	11	20090269916		2009-10-29	KANG; Inkuk;	all
	12	20100048027		2010-02-25	Cheng; Kangguo;	all
	13	20100072553		2010-03-25	XU; Jeff J.;	all

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	
	Filing Date	
	First Named Inventor	Chin-I Liao
	Art Unit	N/A
	Examiner Name	N/A
	Attorney Docket Number	NAUP1863USA3

	14	20100144121		2010-06-10	Chang; Cheng-Hung;	all
	15	20100167506		2010-07-01	LIN; Simon Su-Horng;	all
	16	20110042744		2011-02-24	Cheng	
	17	20110298058	A1	2011-12-08	Kawasaki	

.

FOREIGN PATENT DOCUMENTS

Examiner Initial*	Cite No	Foreign Document Number	Country Code	Kind Code	Publication Date	Name	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	
	1							

NON-PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	
	1	Liu, Source: 2012 symposium on VLSI technology short course; Title: FinFET history, fundamentals and future, 2012/06/11	
	2	Kavalieros, Source: intel corporation; Title: Tri-gate transistor architecture with high-K gate dielectrics, metal gates and strain engineering, 2006/06/13	

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (**Not for submission under 37 CFR 1.99)**	Application Number	
	Filing Date	
	First Named Inventor	Chin-I Liao
	Art Unit	N/A
	Examiner Name	N/A
	Attorney Docket Number	NAUP1863USA3

EXAMINER SIGNATURE			
Examiner Signature		Date Considered	
*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.			

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (**Not for submission under 37 CFR 1.99)**		
	Application Number	
	Filing Date	
	First Named Inventor	Chin-I Liao
	Art Unit	N/A
	Examiner Name	N/A
	Attorney Docket Number	NAUP1863USA3

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

☐ See attached certification statement.

☐ Fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ None

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Scott Margo/	Date (YYYY-MM-DD)	2015-03-02
Name/Print	Scott Margo	Registration Number	56277

PTO/AIA/80 (07-12)
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POWER OF ATTORNEY TO PROSECUTE APPLICATIONS BEFORE THE USPTO

I hereby revoke all previous powers of attorney given in the application identified in the attached statement under 37 CFR 3.73(c).

I hereby appoint:

☑ Practitioners associated with Customer Number: 27765

OR

☐ Practitioner(s) named below (if more than ten patent practitioners are to be named, then a customer number must be used):

Name	Registration Number	Name	Registration Number

As attorney(s) or agent(s) to represent the undersigned before the United States Patent and Trademark Office (USPTO) in connection with any and all patent applications assigned only to the undersigned according to the USPTO assignment records or assignments documents attached to this form in accordance with 37 CFR 3.73(c).

Please change the correspondence address for the application identified in the attached statement under 37 CFR 3.73(c) to:

☑ The address associated with Customer Number: 27765

OR

☐	Firm or Individual Name		
	Address		
	City		
	Country		
	Telephone		Email

Assignee Name and Address:
UNITED MICROELECTRONICS CORP.
No.3, Li-Hsin Road 2, Science-Based Industrial Park, Hsin-Chu City, Taiwan, R.O.C.

A copy of this form, together with a statement under 37 CFR 3.73(c) (Form PTO/SB/96 or equivalent) is required to be Filed in each application in which this form is used. The statement under 37 CFR 3.73(c) may be completed by one of The practitioners appointed in this form, and must identify the application in which this Power of Attorney is to be filed.

SIGNATURE of Assignee of Record
The individual whose signature and title is supplied below is authorized to act on behalf of the assignee

Signature	/Chia Tsung Hung/	Date	SEP 26 2012
Name	Chia-Tsung Hung	Telephone	+886-3-5782258
Title	CHAIRMAN		

This collection of information is required by 37 CFR 1.31, 1.32 and 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

NAU.0

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STATEMENT UNDER 37 CFR 3.73(c)

Applicant/Patent Owner: UNITED MICROELECTRONICS CORP.

Application No./Patent No.: _____ Filed/Issue Date: _____

Titled: SEMICONDUCTOR DEVICE WITH EPITAXIAL STRUCTURES

UNITED MICROELECTRONICS CORP., a corporation

(Name of Assignee) (Type of Assignee, e.g., corporation, partnership, university, government agency, etc.)

states that, for the patent application/patent identified above, it is (choose **one** of options 1, 2, 3 or 4 below):

1. ☑ The assignee of the entire right, title, and interest.

2. ☐ An assignee of less than the entire right, title, and interest (check applicable box):

   ☐ The extent (by percentage) of its ownership interest is _____%. Additional Statement(s) by the owners holding the balance of the interest must be submitted to account for 100% of the ownership interest.

   ☐ There are unspecified percentages of ownership. The other parties, including inventors, who together own the entire right, title and interest are:

   Additional Statement(s) by the owner(s) holding the balance of the interest must be submitted to account for the entire right, title, and interest.

3. ☐ The assignee of an undivided interest in the entirety (a complete assignment from one of the joint inventors was made). The other parties, including inventors, who together own the entire right, title, and interest are:

   Additional Statement(s) by the owner(s) holding the balance of the interest must be submitted to account for the entire right, title, and interest.

4. ☐ The recipient, via a court proceeding or the like (*e.g.*, bankruptcy, probate), of an undivided interest in the entirety (a complete transfer of ownership interest was made). The certified document(s) showing the transfer is attached.

The interest identified in option 1, 2 or 3 above (not option 4) is evidenced by either (choose **one** of options A or B below):

A. ☑ An assignment from the inventor(s) of the patent application/patent identified above. The assignment was recorded in the United States Patent and Trademark Office at Reel _____, Frame _____, or for which a copy thereof is attached.

B. ☐ A chain of title from the inventor(s), of the patent application/patent identified above, to the current assignee as follows:

1. From: _____ To: _____

   The document was recorded in the United States Patent and Trademark Office at

   Reel _____, Frame _____, or for which a copy thereof is attached.

2. From: _____ To: _____

   The document was recorded in the United States Patent and Trademark Office at

   Reel _____, Frame _____, or for which a copy thereof is attached.

This collection of information is required by 37 CFR 3.73(b). The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450**.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

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STATEMENT UNDER 37 CFR 3.73(c)

3. From: _____ To: _____

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4. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at

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5. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at

Reel _____, Frame _____, or for which a copy thereof is attached.

6. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at

Reel _____, Frame _____, or for which a copy thereof is attached.

☐ Additional documents in the chain of title are listed on a supplemental sheet(s).

☑ As required by 37 CFR 3.73(c)(1)(i), the documentary evidence of the chain of title from the original owner to the assignee was, or concurrently is being, submitted for recordation pursuant to 37 CFR 3.11.

[NOTE: A separate copy (i.e., a true copy of the original assignment document(s)) must be submitted to Assignment Division in accordance with 37 CFR Part 3, to record the assignment in the records of the USPTO. See MPEP 302.08]

The undersigned (whose title is supplied below) is authorized to act on behalf of the assignee.

/Scott Margo/	03/02/2015
Signature	Date
Scott Margo	56277
Printed or Typed Name	Title or Registration Number

COMBINE DECLARATION (37 CFR 1.63) FOR UTILITY OR DESIGN APPLICATION USING AN APPLICATION DATA SHEET (37 CFR 1.76) AND ASSIGNMENT

Title of Invention:
SEMICONDUCTOR DEVICE

As the below named inventor, I hereby declare that:
This declaration is directed to:

☑ The attached application, or

☐ United States application number _____ filed on _____, or

☐ PCT international application number _____ filed on _____

The above-identified application was made or authorized to be made by me.

I believe that I am the original inventor or an original joint inventor of a claimed invention in the application.

I hereby acknowledge that any willful false statement made in this declaration is punishable under18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both.

In consideration of the payment by **UNITED MICROELECTRONICS CORP.** having a postal address of

No.3, Li-Hsin Road 2, Science-Based Industrial Park, Hsin-Chu City 300, Taiwan, R.O.C.

(referred to as "ASSIGNEE"below) to I of the sum of One Dollar ($ 1.00), the receipt of which is hereby acknowledged, andfor other good and valuable consideration.

I hereby sell, assign and transfer to ASSIGNEE and the successors and assignees of the ASSIGNEE the entire right, title and interest in and to any and all improvements which are disclosed in the invention as above-identified application and, in and to, all Letters Patent to be obtained for said invention by the above application or any continuations, continuation-in-part, divisions, renewals, substitutes, or extensions thereof, and as to Letters Patent any reissue or re-examination thereof.

I hereby covenant that no assignment, sale, agreement or encumbrance has been or will be made or entered into which would conflict with this assignment;

I further covenant that ASSIGNEE will, upon its request, be provided promptly with all pertinent facts and documents relating to said invention and said Letters Patent and legal equivalents as may be known and accessible to I and will testify as to the same in any interference, litigation proceeding related thereto and will promptly execute and deliver to ASSIGNEE or its legal

representatives any and all papers, instruments or affidavits required to apply for, obtain, maintain, issue and enforce said application, said invention and said Letters Patent and said equivalents thereof which may be necessary or desirable to carry out the proposes thereof.
IN WINTNESS WHEREOF, I have hereunto set hand and seal this AUG 0 1 2013 (Date of signing)

Note: An application data sheet (PTO/SB/14 or equivalent), including naming the entire inventive entity, must accompany this form. Use this form for each additional inventor.

Docket No NAUP1863USA

LEGAL NAME OF INVENTOR(ASSIGNOR)

Inventor: **Chin-I Liao** Date: AUG 01 2013

Signature: Chin I Liao

COMBINE DECLARATION (37 CFR 1.63) FOR UTILITY OR DESIGN APPLICATION USING AN APPLICATION DATA SHEET (37 CFR 1.76) AND ASSIGNMENT

Title of Invention:
SEMICONDUCTOR DEVICE

As the below named inventor, I hereby declare that:
This declaration is directed to:

☑ The attached application, or

☐ United States application number _____ filed on _____, or

☐ PCT international application number _____ filed on _____

The above-identified application was made or authorized to be made by me.

I believe that I am the original inventor or an original joint inventor of a claimed invention in the application.

I hereby acknowledge that any willful false statement made in this declaration is punishable under18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both.

In consideration of the payment by **UNITED MICROELECTRONICS CORP.** having a postal address of

No.3, Li-Hsin Road 2, Science-Based Industrial Park, Hsin-Chu City 300, Taiwan, R.O.C.

(referred to as "ASSIGNEE"below) to I of the sum of One Dollar ($ 1.00), the receipt of which is hereby acknowledged, andfor other good and valuable consideration.

I hereby sell, assign and transfer to ASSIGNEE and the successors and assignees of the ASSIGNEE the entire right, title and interest in and to any and all improvements which are disclosed in the invention as above-identified application and, in and to, all Letters Patent to be obtained for said invention by the above application or any continuations, continuation-in-part, divisions, renewals, substitutes, or extensions thereof, and as to Letters Patent any reissue or re-examination thereof.

I hereby covenant that no assignment, sale, agreement or encumbrance has been or will be made or entered into which would conflict with this assignment;

I further covenant that ASSIGNEE will, upon its request, be provided promptly with all pertinent facts and documents relating to said invention and said Letters Patent and legal equivalents as may be known and accessible to I and will testify as to the same in any interference, litigation proceeding related thereto and will promptly execute and deliver to ASSIGNEE or its legal

representatives any and all papers, instruments or affidavits required to apply for, obtain, maintain, issue and enforce said application, said invention and said Letters Patent and said equivalents thereof which may be necessary or desirable to carry out the proposes thereof.
IN WINTNESS WHEREOF, I have hereunto set hand and seal this AUG 0 1 2013 (Date of signing)

Note: An application data sheet (PTO/SB/14 or equivalent), including naming the entire inventive entity, must accompany this form. Use this form for each additional inventor.

Docket No NAUP1863USA

LEGAL NAME OF INVENTOR(ASSIGNOR)

Inventor: **Chun-Yu Chen** Date: AUG 01 2013

Signature: Chun Yu Chen

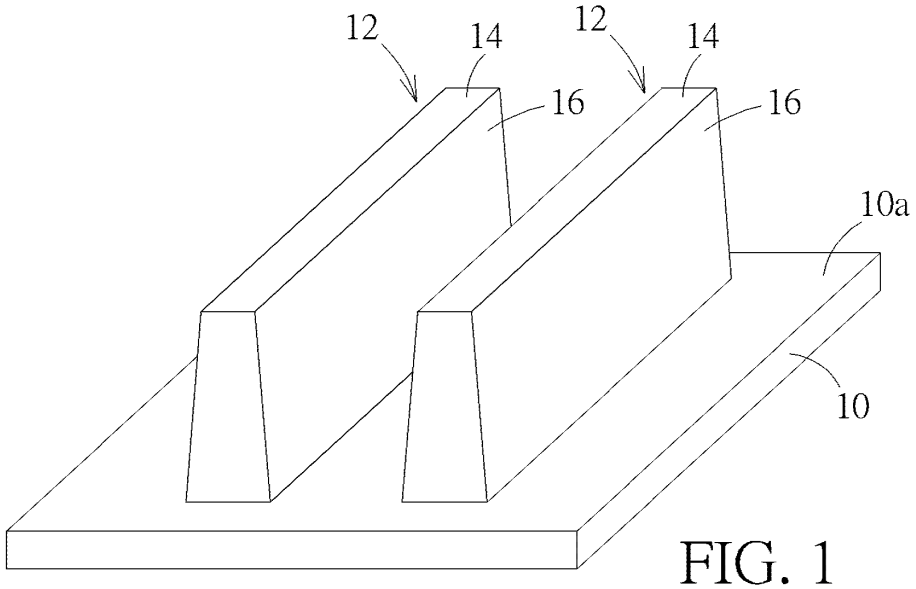


FIG. 1

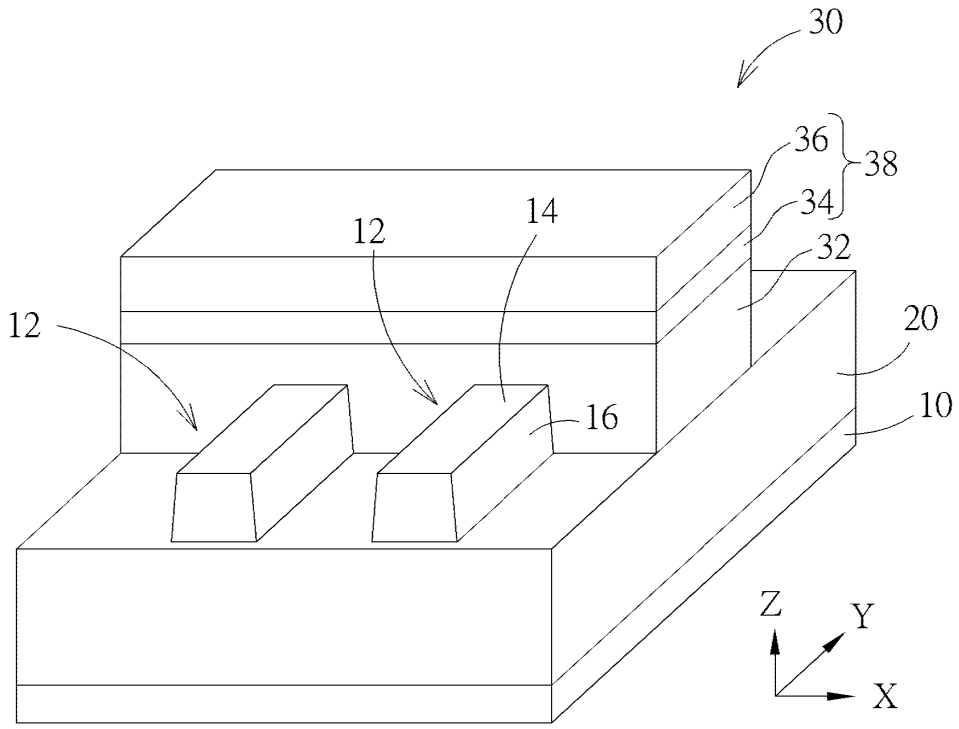


FIG. 2

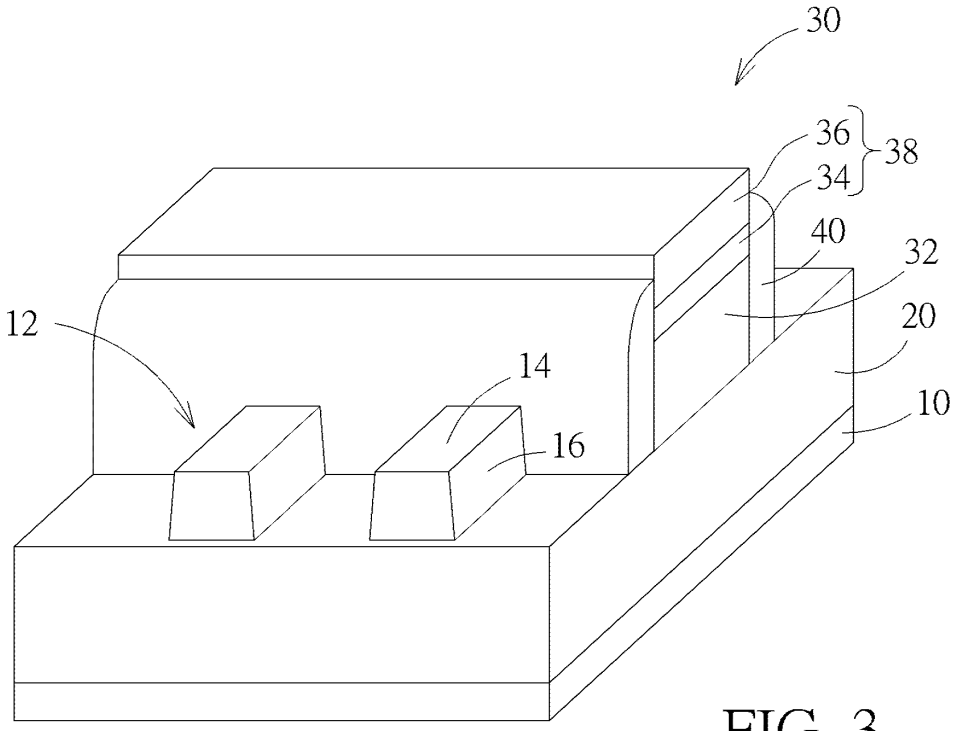


FIG. 3

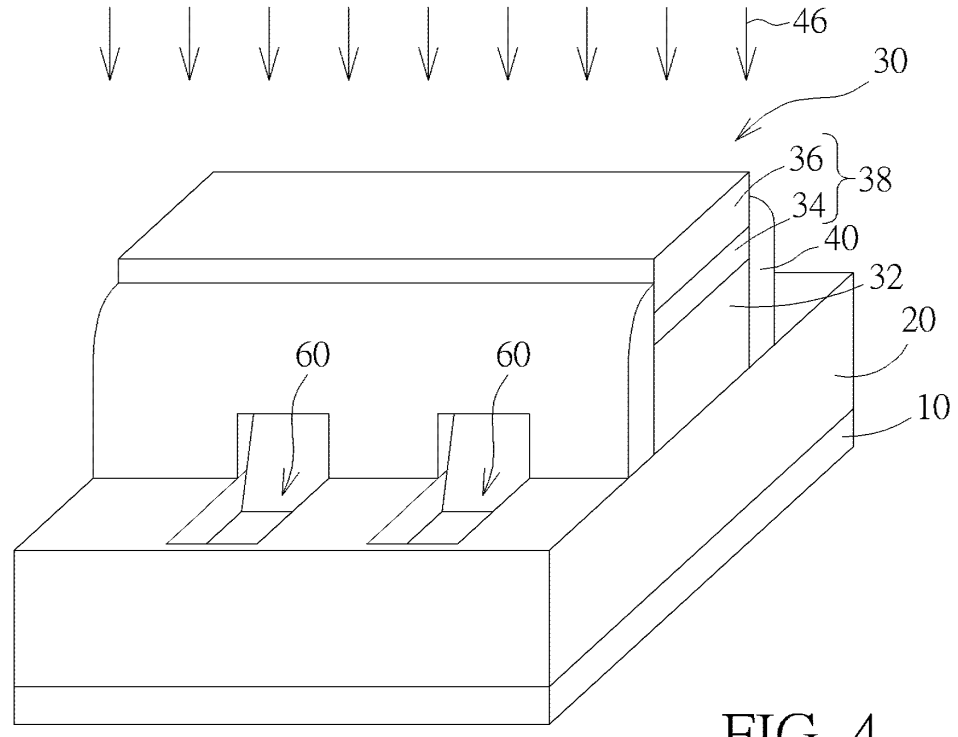


FIG. 4

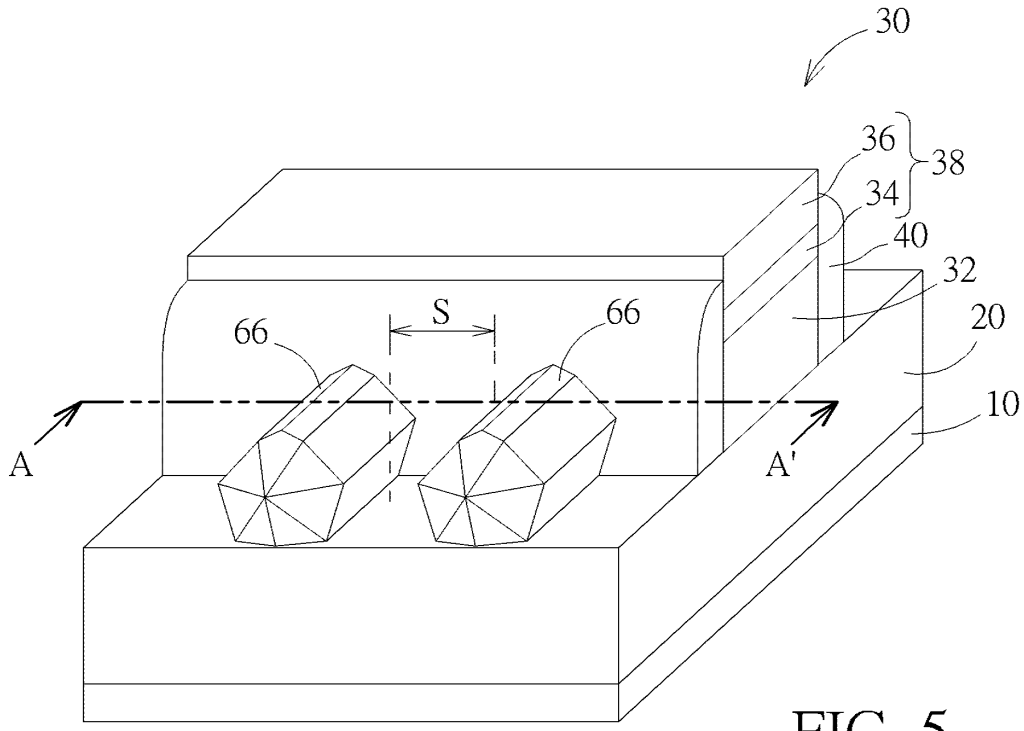


FIG. 5

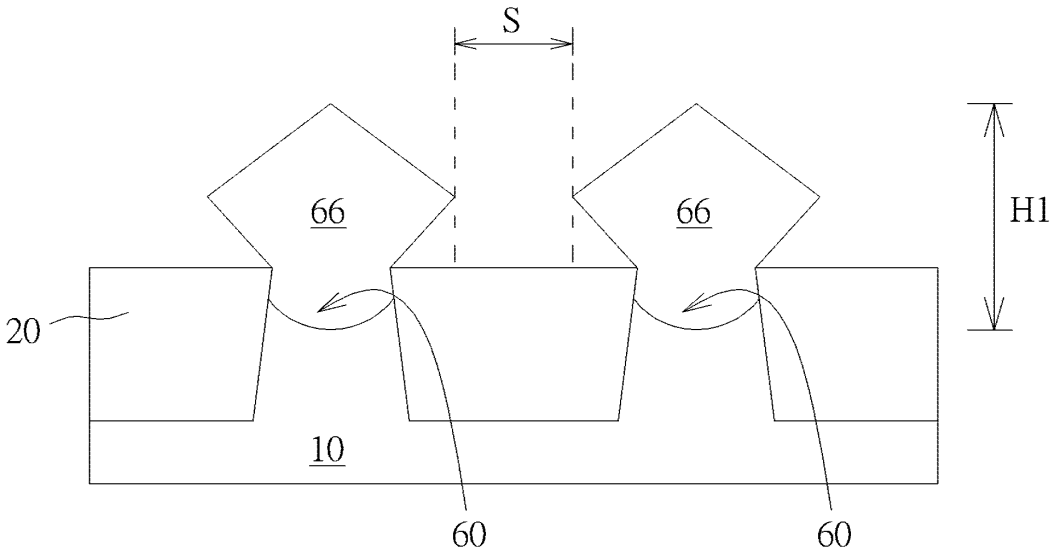


FIG. 6

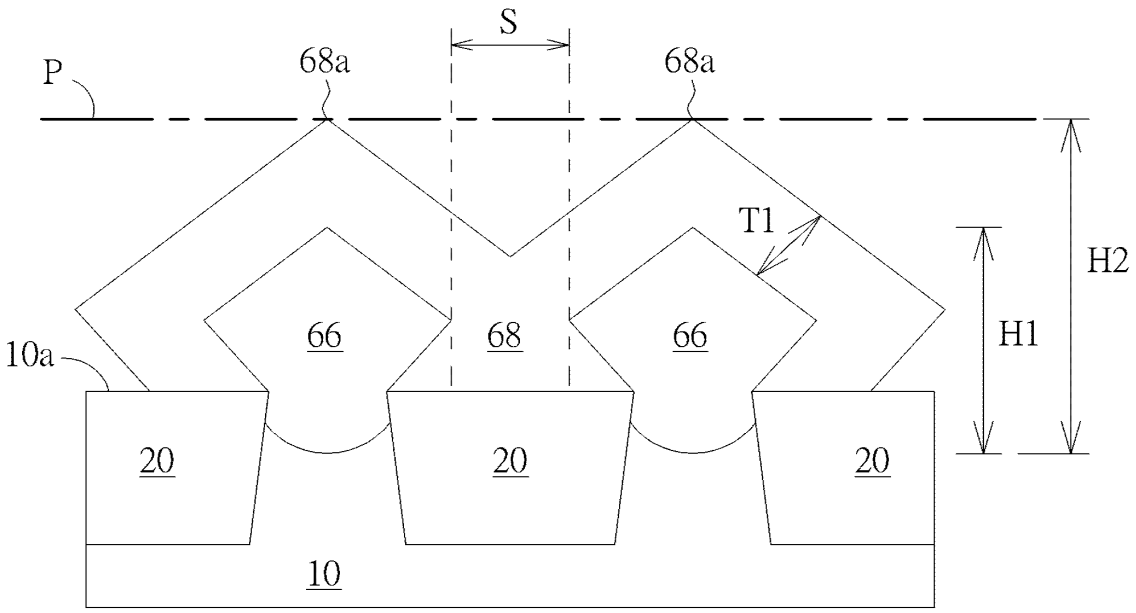

S
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H2
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FIG. 7

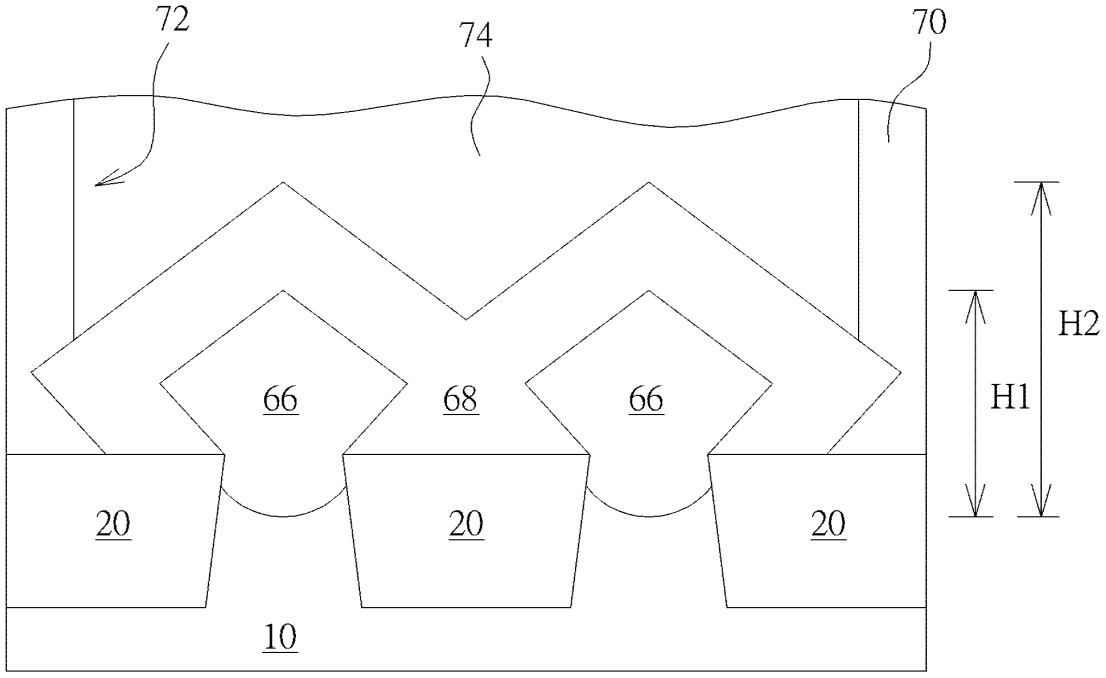

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FIG. 8

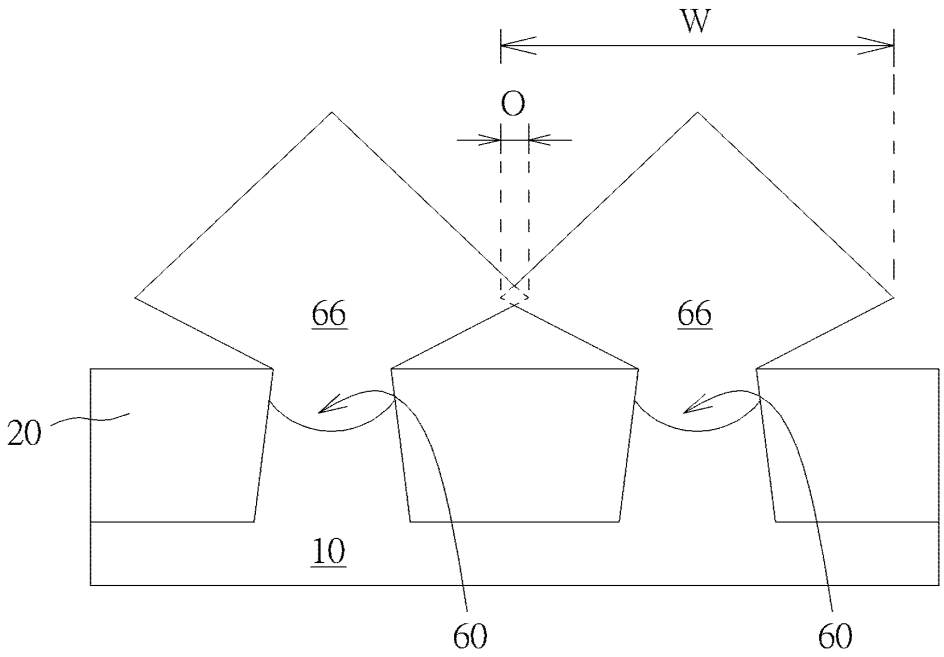


FIG. 9

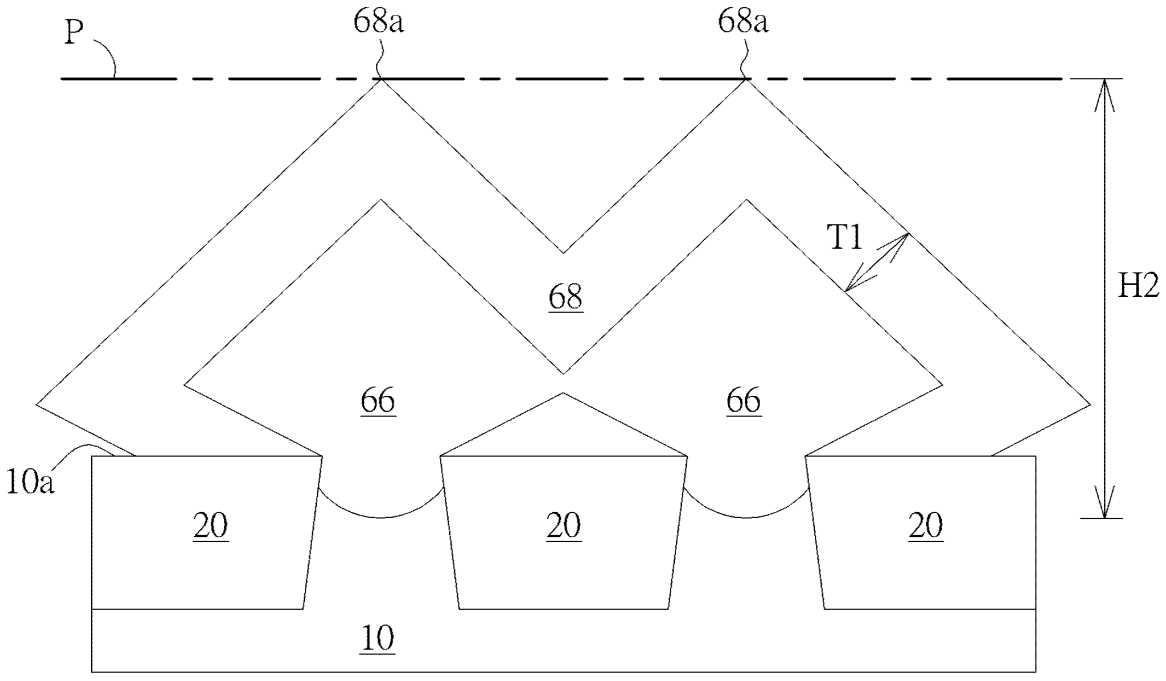


FIG. 10

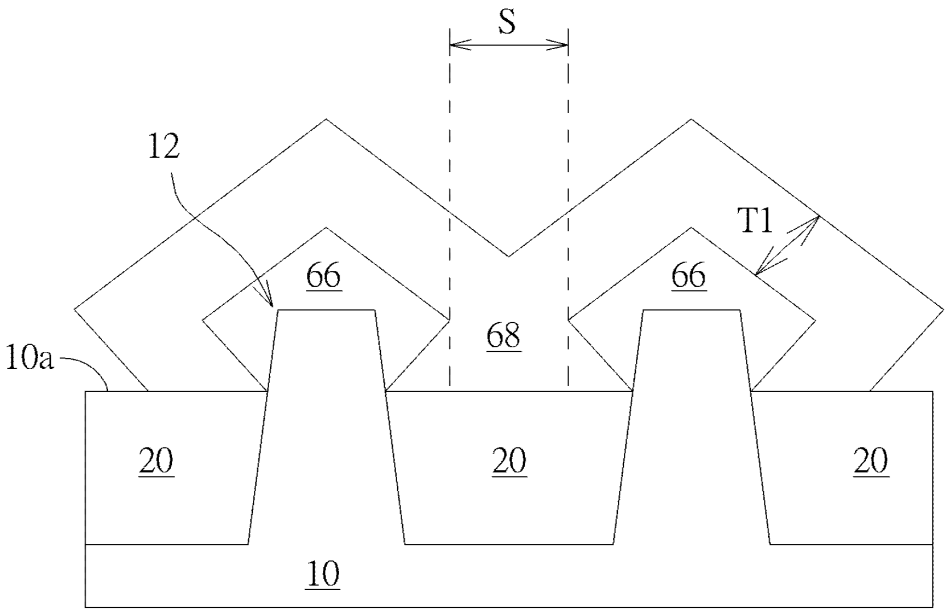


FIG. 11

Abstract of Disclosure

A semiconductor device includes at least two fin-shaped structures, a gate structure, at least two epitaxial structures and a cap. The fin-shaped structures are disposed on a substrate and are covered by the gate structure. The epitaxial structures spaced apart from each other are disposed at one side of the gate structure and respectively directly contact each fin-shaped structure. The cap simultaneously surrounds the epitaxial structures, and at least two adjacent caps are merged together.

Claims

What is claimed is:

1. A semiconductor device, comprising:

at least two fin-shaped structures, disposed on a substrate;

a gate structure, covering the fin-shaped structures;

at least two epitaxial structures, disposed at one side of the gate structure and respectively directly contacting each fin-shaped structure, wherein the epitaxial structures are spaced apart from each other; and

at least two caps, respectively surrounding the epitaxial structures, wherein at least two adjacent caps are merged together.

2. The semiconductor device according to claim 1, further comprising at least two recesses, respectively disposed at an end of each of the fin-shaped structures, wherein each of the epitaxial structures respectively fills up each of the recesses.

3. The semiconductor device according to claim 1, wherein the epitaxial structures respectively cover an end of each of the fin-shaped structures.

4. The semiconductor device according to claim 1, further comprising at least an insulating layer, disposed between the epitaxial structures.

5. The semiconductor device according to claim 4, wherein the caps directly cover the insulating layer between the epitaxial structures.

6. The semiconductor device according to claim 1, wherein each of the epitaxial structures comprises a low doped epitaxial layer, a high doped epitaxial layer and a liner.

7. The semiconductor device according to claim 1, wherein a

composition of each of the epitaxial structures comprises silicon germanium, silicon phosphide or silicon carbide.

8. The semiconductor device according to claim 1, wherein each of the epitaxial structures comprises a top portion and the top portions are substantially in a same plane.

9. The semiconductor device according to claim 1, wherein the caps have a concavo-convex profile.

10. The semiconductor device according to claim 1, wherein the caps are made of monocrystalline silicon.

11. The semiconductor device according to claim 1, further comprising:
a dielectric layer, covering the gate structure and the cap; and
at least a contact structure, disposed in the dielectric layer and in direct contact with the caps.

Title

SEMICONDUCTOR DEVICE WITH EPITAXIAL STRUCTURES

Cross Reference To Related Applications

[0001] This application is a continuation of U.S. application Ser. No. 13/960,816, filed on Aug. 7, 2013, the disclosure of which is hereby incorporated herein by reference in its entirety.

Background of the Invention

1. Field of the Invention

[0002] The present invention relates generally to non-planar semiconductor devices, and more particular to non-planar semiconductor devices with epitaxial structures.

2. Description of the Prior Art

[0003] With the trend in the industry being towards scaling down the size of metal oxide semiconductor transistors (MOS), three-dimensional or non-planar transistor technology, such as the fin field effect transistor technology (Fin FET) has been developed to replace planar MOS transistors. The three-dimensional structure of a fin FET increases the overlapping area between the gate and the fin-shaped structure of the silicon substrate, and, accordingly, the channel region is more effectively controlled. The drain-induced barrier lowering (DIBL) effect and short channel effect (SCE) are therefore reduced. The channel region is also longer under the same gate length, and thus the current between the source and the drain is increased.

[0004] In another aspect, in order to further improve the devices performances, a strained-silicon technology has also been developed. The main principle in the strained-silicon technology is that strains are applied to predetermined regions within the semiconductor device which in turn make the semiconductor device work better by enabling charge carriers, such as electrons or holes, to pass through the lattice of the channel more easily. In detail, one main technology

generally used in the strained-silicon technology is to dispose epitaxial structures with lattice constants different from that of the crystal silicon in the source/drain regions of the semiconductor devices. The epitaxial structures are preferably composed of silicon germanium (SiGe), carbon-doped silicon (SiC) and so forth, which have lattice constants different from that of the crystal silicon. Since the epitaxial structures have lattice constants larger or smaller than that of the crystal silicon, carrier channel regions adjacent to those epitaxial structures could sense external stresses and both the lattice structure and the band structure within these regions are altered. As a result, the carrier mobility and the performances of the corresponding semiconductor devices are improved effectively.

[0005] However, along with the continuous decrease in the size and dimensions of the semiconductor devices, there are still some newly generated technological problems that need to be overcome, even though the non-planar transistor and the strained-silicon technology are already adopted. For example, two adjacent epitaxial structures within the semiconductor device often generate unwanted lattice defects on their interfaces. Therefore, how to effectively eliminate these defects and improve the performance of the semiconductor devices are important issues in this field.

Summary of the Invention

[0006] One purpose of the present invention is to provide a semiconductor device with epitaxial structures, which has few lattice defects in the epitaxial structures and has enhanced stresses imposed onto the channel region.

[0007] To this end, a semiconductor device is provided according to a preferred embodiment of the present invention. The semiconductor device includes at least two fin-shaped structures, a gate structure, at least two epitaxial structures and a cap. The fin-shaped structures are disposed on a substrate and are covered by the gate structure. The epitaxial structures spaced apart from each other are disposed

at one side of the gate structure and respectively directly contact each fin-shaped structure. The cap simultaneously surrounds the epitaxial structures, and at least two adjacent caps are merged together.

[0008] These and other objectives of the present invention will no doubt become obvious to those of ordinary skill in the art after reading the following detailed description of the preferred embodiment that is illustrated in the various figures and drawings.

Brief Description of the Drawings

[0009] FIG. 1 to FIG. 8 are schematic diagrams showing a method for fabricating a MOSFET according to a preferred embodiment of the present invention.

[0010] FIG. 9 to FIG. 10 are schematic diagrams showing a method for fabricating a MOSFET according to another preferred embodiment of the present invention.

[0011] FIG. 11 is a schematic diagram showing a method for fabricating a MOSFET according to still another preferred embodiment of the present invention.

Detailed Description

[0012] In the following description, numerous specific details are given to provide a thorough understanding of the invention. It will, however, be apparent to one skilled in the art that the invention may be practiced without these specific details. Furthermore, some well-known system configurations and process steps are not disclosed in detail, as these should be well-known to those skilled in the art.

[0013] Likewise, the drawings showing embodiments of the apparatus are not to scale and some dimensions are exaggerated for clarity of presentation. Also, where multiple embodiments are disclosed and described as having some features in common, like or similar features will usually be described with same reference numerals for ease of illustration and description thereof.

[0014] FIG. 1 to FIG. 8 are schematic diagrams showing a method for fabricating a semiconductor device according to a first preferred embodiment of the present invention. Please refer to FIG.1. FIG. 1 is a schematic perspective view showing a semiconductor device at the beginning of the fabrication process. As this stage, a semiconductor device having a substrate 10 and a plurality of fin-shaped structures 12 disposed thereon is provided. The main surface 10a of the substrate may have a specific orientation and the long axial direction of each fin-shaped structure 12 is aligned with a predetermined direction. For example, for a bulk silicon substrate, the main surface 10a of the substrate may have a orientation (100) and the long axial direction of each fin-shaped structure 12 is aligned with a direction 〈110〉, but not limited thereto. In addition to the bulk silicon substrate, the substrate 10 may be chosen from another semiconductor substrate such as a silicon containing substrate, a III-V semiconductor-on-silicon (such as GaAs-on-silicon) substrate, or a graphene-on-silicon substrate. Preferably, the substrate 10 is not a silicon-on-insulator (SOI) substrate.

[0015] More precisely, the method for fabricating the fin-shaped structures 12 may include the following processes, but not limited thereto. First, a bulk substrate (not shown) is provided and a hard mask layer (not shown) is formed thereon. The hard mask layer is then patterned through a photolithographic and an etching process, so as to define the location for forming fin-shaped structures 12 in the bulk substrate. Afterwards, an etching process is performed to form fin-shaped structures 12 in the bulk substrate. After the above processes, the fabrication method for the fin-shaped structures 12 is complete. In this case, the fin-shaped structures 12 may be regarded as protruding from the surface 10a of the substrate 10 and the compositions of the fin-shaped structures 12 and the substrate 10 may be the same, such as monocrystalline silicon. In another case, when the substrate is chosen from a III-V semiconductor-on-silicon substrate rather than the above-mentioned bulk silicon substrate,

the main compositions of the fin-shaped structures may be the same as that of the III-V semiconductor and differ from that of the underlying substrate.

[0016] In this embodiment, the hard mask layer (not shown) is optionally removed in a later process after the formation of the fin-shaped structures 12, so that a tri-gate MOSFET can be formed in the following processes. There are three contact faces 14 and 16 between each fin-shaped structure 12 and the following formed dielectric layer serving as a carrier channel region. Compared with planar MOSFETs, the tri-gate MOSFETs have a wider channel width for a same channel length. When a driving voltage is applied, the tri-gate MOSFET may produce an on-current twice higher than conventional planar MOSFETs. Alternatively, the hard mask layer (not shown) may be reserved to form a fin field effect transistor (FinFET), which is another kind of multi-gate MOSFET. Since the hard mask layer is reserved in the fin field effect transistor, there are only two contact surfaces between each fin-shaped structure 12 and the following formed dielectric layer.

[0017] Please refer to FIG. 2. FIG. 2 is a schematic perspective diagram showing the semiconductor device after the formation of a dummy gate structure. An isolating structure 10 is formed on the substrate 10 and the lower portion of each fin-shaped structure 12 is embedded in the isolating structure 20. In this way, subsequently-formed transistors may be electrically isolated from one another by the isolating structure 20. The isolating structure 20 may have the configuration shown in FIG. 2. The isolating structure 10, for example, may be a shallow trench isolation (STI) structure, which may be formed through a STI fabrication process. Since the fabrication process for the STI structure is well-known to those skilled in the art, the detailed description of this is therefore omitted, and is not limited thereto.

[0018] Still referring to FIG. 2, in a following step, a gate

dielectric layer (not shown), a sacrificial electrode layer (not shown) and a cap layer (not shown) are sequentially formed to cover the substrate 10 and the fin-shaped structures 12. Then, the gate dielectric layer, the sacrificial electrode layer and the cap layer are patterned to form a stack structure. The stack structure may be regarded as a gate structure 30 including the gate dielectric layer (not shown), the sacrificial electrode layer 32 and the cap layer 38. The gate structure 30 crosses over at least two fin-shaped structures 12 and covers the isolating structure 20 between them. Specifically, the gate structure 30 may cover a top surface 14 and two side surfaces 16 of portions of each fin-shaped structure 12, and may cover a top surface of portions of the isolating structure 20. Additionally, the gate structure 30 is preferably aligned along a first direction X, while the fin-shaped structures 12 are preferably aligned along a second direction Y and protruding from the substrate 10 along a third direction Z. In this embodiment, the first direction X, the second direction Y, and the third direction Z are mutually orthogonal to one another, but not limited thereto.

[0019] For the sake of clarity, only one gate structure 30 is depicted in FIG. 2 to FIG. 8. The number of which, however, may be increased depending on the requirements for different products. For example, more than one mutually parallel gate structure may be disposed on the substrate so that one fin-shaped structure may be concurrently covered by more than one gate structure. Besides, the same mono gate structure 30 is preferably used as a gate for transistors with the same conductivity type, like gates for PMOS transistors or gates for NMOS transistors.

[0020] In this embodiment, a gate-last for high-k last process is used so that the gate structure 30 may be regarded as a dummy gate structure. In other words, the gate dielectric layer will be replaced with a gate dielectric layer having a high dielectric constant in later processes and the sacrificial electrode layer 32 will be replaced with a conductive metal layer. Therefore, the material of the gate

dielectric layer may be just a sacrificial material suitable for being removed in later processes. The sacrificial electrode layer 32 may be made of polysilicon, but not limited thereto. The cap layer 38 may be a single-layered or a multi-layered structure composed of a nitride layer or an oxide layer used to serve as a patterned hard mask. In this embodiment, the cap layer 38 is a double-layered structure composed of a bottom layer 34 and a top layer 36. The bottom layer 34 may be a nitride layer and the top layer 36 may be an oxide layer, but not limited thereto.

[0021] In the above paragraphs, a gate-last for high-k first process is used. However, the present embodiment may also adopt a gate-last for high-k last process. In this case, the gate dielectric layer is a gate dielectric layer having a high dielectric constant, which may be the group selected from hafnium oxide (HfO_2), hafnium silicate ($HfSiO_4$), hafnium silicon oxynitride (HfSiON), aluminum oxide (Al_2O_3), lanthanum oxide (La_2O_3), tantalum oxide (Ta_2O_5), yttrium oxide (Y_2O_3), zirconium oxide (ZrO_2), strontium titanate ($SrTiO_3$), zirconium silicate ($ZrSiO_4$), hafnium zirconate ($HfZrO_4$), strontium bismuth tantalate ($SrBi_2Ta_2O_9$, SBT), lead zirconate titanate ($PbZr_xTi_{1-x}O_3$, PZT) and barium strontium titanate ($BaxSr_{1-x}TiO_3$, BST), but it is not limited thereto. Additionally, a barrier layer (not shown) may be formed on the gate dielectric layer to serve as an etching stop layer to protect the gate dielectric layer during the removal of the sacrificial electrode layer and to prevent above disposed metals from diffusing downwards to the gate dielectric layer and from polluting the gate dielectric layer. The barrier layer (not shown) may be a single layer structure or a multilayer structure composed of tantalum nitride (TaN) or titanium nitride (TiN) etc.

[0022] Please refer to FIG. 3. After the formation of the gate structure, at least a spacer 40 is formed on the sidewalls of the gate structure 30 to define the position of epitaxial structures. In this embodiment, the spacers 40 are respectively formed on each side of the gate structure 30 and cover portions of the isolating

structure 20. More precisely, the method for forming the spacers 40 may include the following steps. A material layer (not shown) is deposited on the gate structure 30 and the substrate 10, and then an etching process is performed to form the spacers 40. The spacers 40 may be single-layered structures, such as a silicon nitride layer or a silicon oxynitride layer, or double-layered structures, such as a silicon oxide/silicon nitride layer, but not limited thereto. In this embodiment, the spacers 40 represent spacers for defining and forming epitaxial structures, so that other spacers may be formed before/after the spacers 40 are formed to form a lightly doped source/drain region (not shown) or a source/drain region (not shown).

[0023] Please refer to FIG. 4. FIG. 4 is a schematic perspective view showing the semiconductor device after etching the fin-shaped structures. As shown in FIG. 4, an etching process 46 is carried out to etch the fin-shaped structures 12 under the gate structure 30 and the spacers 40. After the etching process, recesses 60 may be respectively formed in each fin structure 12 at at least one side of the gate structure 30. In detail, the above etching process may include at least a dry etching step and/or at least a wet etching step. For example, the substrate 10 may be etched down to a predetermined depth through a dry etching step and then laterally etched to form a desired profile of the recess 60 through a wet etching step, but not limited thereto. In this embodiment, each recess 60 has an upwardly-curved cross-sectional profile, but not limited thereto, as the cross-sectional profile of the recess depends upon the specific requirements.

[0024] Please refer to FIG. 5 and FIG. 6. FIG. 5 is a schematic perspective view showing the semiconductor device after the formation of epitaxial structure. FIG. 6 is a schematic cross-sectional diagram taken along a line A-A' in FIG. 5. Referring to FIG. 5, after the formation of the optional recesses 60, epitaxial structures 66 are respectively formed in the corresponding recesses 60 through performing an epitaxial growth process. Preferably, two adjacent

epitaxial structures 66 are disposed individually and spaced apart from each other so as to ensure that they don't merge together according to this embodiment. For example, in a case where a pitch ranges from 10 nanometers (nm) to 14 nm between two adjacent fin-shaped structures 12, when the epitaxial structures 66 have a height H1 ranging from 300 Angstroms to 600 Angstroms, a distance S ranging from 30 Angstroms to 150 Angstroms may exist between two adjacent epitaxial structures 66; that is to say, two adjacent epitaxial structures 66 don't merge together, but it is not limited thereto. In detail, the above-described epitaxial growth process may be a molecular beam epitaxy (MBE) process, a co-flow epitaxial growth process, a cyclic selective epitaxial growth process or the likes.

[0025] Furthermore, the composition of the epitaxial structure 66 may be correspondingly modified according to the conductivity types of the semiconductor devices. In this way, proper stresses could be imposed on certain regions within the semiconductor devices. For example, for a P-type semiconductor device, the epitaxial structure 66 may be a structure used to apply compressive stresses to the adjacent channel regions so that its composition may be doped or un-doped silicon germanium layer. Besides, the epitaxial structure 66 may include a multilayer or a surrounding structure with a different germanium concentration gradually varying from the inside to the outside or/and from bottom to top. For example, the epitaxial layer 66 may include epitaxial Si, at least a layer of epitaxial SiGe with a relatively low concentration of Ge, at least a layer of epitaxial SiGe with a relatively high concentration of Ge, an epitaxial Si layer and so forth, which are disposed sequentially from bottom to top. In another case, in an N-type semiconductor device, the composition of the epitaxial structure 66 may include silicon phosphorous (SiP), silicon carbide (SiC), phosphorus-doped silicon carbide or the likes, so as to provide tensile stresses to the channel regions.

[0026] Please refer to FIG. 7. After the formation of the epitaxial structures 66, another epitaxial layer, such as a silicon cap 68

composed of monocrystalline silicon, may be formed on the surface of each of the epitaxial structures 66 through another epitaxial growth process. During the epitaxial growth process for the silicon cap 68, the silicon cap 68 continuously grows on the surface of each of epitaxial structure 66 and gradually fills up the space between two adjacent epitaxial structures 66 until two adjacent silicon caps 68 merge together as shown in FIG. 7. In other words, in order to obtain a merged silicon cap 68, the thickness T1 of the silicon cap 68 is at least greater than one-half of the distance S. For example, when the distance S ranges from 10 nm to 20 nm, the thickness T1 of the silicon cap 68 may range from 6 nm to 11 nm or may be greater than 11 nm. The actual thickness of the silicon cap 68 depends on different requirements. Still referring to FIG. 7, the merged silicon cap 68 may cover the entire surface of the epitaxial structures 66 and has an approximately periodic concavo-convex profile. In detail, the merged silicon cap 68 may have top portions 68a having the same height H2 or being in the same plane P. Besides, the plane P is substantially parallel to the main surface 10a of the substrate 10 or the isolating structure 20, but not limited thereto.

[0027] Please refer to FIG. 8. After the formation of the above epitaxial structures, the following semiconductor processes may be optionally carried out. For example, a replacement metal gate (RMG) process and a process for contact structures may be carried out sequentially. Through the RMG process, the gate structure composed of polysilicon inside may be replaced with a metal gate structure. Besides, the RMG process may be further classified into two types: a high-k first RMG process and a high-k last RMG process. The high-k last RMG process may include the following processes: (1) depositing an interlayer dielectric 70 to surround the gate structure (not shown); (2) removing the gate structure to leave a trench (not shown); (3) forming a gate dielectric layer (not shown) to conformally cover the sidewalls and the bottom of the trench; and (4) forming a metal gate (not shown) to fill up the trench. The metal gate may contain one or a plurality of metal layers such as a barrier layer (not shown),

a work function metal layer (not shown), and a low-resistance metal layer (not shown), but not limited thereto.

[0028] Still referring to FIG. 8, after the RMG process, a subsequent process for contact structures may be further carried out so as to form a structure shown in FIG. 8. Precisely, the contact structures may be contact plugs 74 and are used to electrically connect the epitaxial structures 66 to the subsequently formed external circuit (not shown). The steps of forming the contact plugs 72 are described below. For example, first, at least a contact hole 72 with a circular or a slot opening is formed in the interlayer dielectric 70 so as to expose the corresponding silicon cap 68. Then, a barrier/adhesive layer (not shown) and a seed layer (not shown) are conformally filled into the contact hole 72 to cover the silicon cap 68. Afterwards, a conductive layer (not shown) is deposited to fill up the contact hole 72. In this way, a contact plug 74 filling up the contact hole 72 is obtained.

[0029] It should be noted that, in order to increase the conductivity of the silicon cap 68, a salicide process may be performed optionally during the process for forming the contact structures. For example, at the timing between forming the contact hole and filling up the contact hole with the conductive layer, a metal source layer (not shown) may be filled into the contact hole 72 and a rapid thermal anneal (RTA) process may be conducted. In this way, the metal source layer adjacent to the silicon cap 68 may partially or entirely react with the underlying silicon cap 68 so as to produce a layer of silicide layer (not shown). Then, the residual metal source layer is removed and the salicide process is accomplished. After the salicide process, the remaining process for forming contact structure may be further carried out. The metal source layer may consist of cobalt (Co), titanium (Ti), nickel (Ni), platinum (Pt), or an alloy thereof, but not limited thereto.

[0030] In the following paragraphs, several modified embodiments of

the above embodiment are disclosed and the description below is mainly focused on their differences. In addition, like or similar features will usually be described with same reference numerals for ease of illustration and description thereof.

[0031] Please refer to FIG. 9 and FIG. 10. Another semiconductor device with epitaxial structures similar to the one previously described is also provided according to a modification embodiment of the present invention. However, one main difference between this modification embodiment and the above first preferred embodiment is that the epitaxial structures may merge together during the corresponding epitaxial growth process. Precisely, referring to FIG. 9, after the epitaxial growth process similar to that described in the first preferred embodiment, the epitaxial structures 66 in the respective recesses 60 may be slightly merged and constitute a consecutive epitaxial structure. Furthermore, there may be an overlapped portion O, also called connecting portion, defined between the two adjacent epitaxial structures 66 and used to physically connect them. Besides, there may be a proportional relationship between the overlapped portion O and the width W of each of the epitaxial structures 66. For example, the ratio between these dimensions (O/W) may range from 0.001 to 0.25, and preferably from 0.001 to 0.05. Under this specific ratio, even if the two adjacent epitaxial structures 66 are slightly merged, each of the epitaxial structures 66 may keep a monocrystalline structure without generating unwanted lattice defects.

[0032] Please refer to FIG. 10. After the process corresponding to FIG. 9, another epitaxial layer similar to that described in the first preferred embodiment, such as a silicon cap 68 composed of monocrystalline silicon, may be formed on the surface of each of the epitaxial structures 66 through another epitaxial growth process. It should be noted that the silicon cap 68 depicted in FIG. 10 is a consecutive layer disposed on the surface of the epitaxial structures 66 according to this modification embodiment. Therefore, the thickness T1 of the silicon cap 68 is not restricted to any specific

value as long as it can constitute a consecutive layer. Similarly, the silicon cap 68 may cover the entire surface of the epitaxial structures 66 and has an approximate periodic concavo-convex profile. In detail, the merged silicon cap 68 may also have the top portions 68a having the same height H2 or being in the same plane P. Besides, the plane P is substantially parallel to the main surface 10a of the substrate 10 or the isolating structure 20, but not limited thereto.

[0033] Please refer to FIG. 11. A semiconductor device with epitaxial structures similar to those of the first preferred embodiment is also provided according to another modification embodiment. However, one main difference between this modification embodiment and the above-described first preferred embodiment is that the epitaxial structures respectively directly grow on the surface of the corresponding fin-shaped structures. That is to say, there are no recesses in the fin-shaped structures. Precisely, referring to FIG. 11, since an etching process for forming the recesses is not carried out according to this modification embodiment, the epitaxial structures 66 formed in the subsequent epitaxial growth process may directly cover the corresponding fin-shaped structures 12 and there is a distance between two adjacent epitaxial structures 66. Similarly, another epitaxial layer, such as silicon cap 68 composed of monocrystalline silicon, may be formed on each of the epitaxial structures 66 in a subsequent process. The silicon caps 68 may continuously grow on the epitaxial structures 66 so that the two adjacent silicon caps 68 could merge together. This structure is depicted in FIG. 11. Alternatively, the epitaxial structures may be slightly merged prior to the formation of the silicon cap so that the subsequent formed silicon cap is no longer merged in this case. Since the structure and the fabrication processes described in this modification embodiment are mostly similar to those described in the first preferred embodiment, the detailed description of those is therefore omitted for the sake of clarity.

[0034] It should be noted that, according to the above embodiments,

the epitaxial structures and the silicon cap covering thereon are preferably disposed in source/drain regions of semiconductor devices with the same conductivity type. For example, the epitaxial structures made of SiGe and the overlaying silicon caps are all disposed in P-type semiconductor devices and are at least disposed in source/drain regions at one side of the gate structures.

[0035] To summarize, each preferred embodiment or modification embodiment of the present invention provides a semiconductor device. In these semiconductor devices, the two adjacent epitaxial structures are spaced apart from each other or slightly merged together. In the first case, another epitaxial layer disposed on the epitaxial structures may fill up the space between the two adjacent epitaxial structures. In the latter case, another epitaxial layer may constitute a continuous layer disposed on the surface of the epitaxial structures. In either case, no lattice defects exist in the epitaxial structures or in the overlapped region between two adjacent epitaxial structures. As a result, stresses provided by the epitaxial structures are increased and the performances of the semiconductor devices are enhanced.

[0036] Those skilled in the art will readily observe that numerous modifications and alterations of the device and method may be made while retaining the teachings of the invention. Accordingly, the above disclosure should be construed as limited only by the metes and bounds of the appended claims.

Electronic Patent Application Fee Transmittal	
Application Number:	
Filing Date:	
Title of Invention:	SEMICONDUCTOR DEVICE WITH EPITAXIAL STRUCTURES
First Named Inventor/Applicant Name:	Chin-I Liao
Filer:	Winston Hsu/Hitomi Lin
Attorney Docket Number:	NAUP1863USA3
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Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Utility application filing	1011	1	280	280
Utility Search Fee	1111	1	600	600
Utility Examination Fee	1311	1	720	720
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Miscellaneous:				
		Total in USD ($)		**1600**

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Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Application Data Sheet	2189367.PDF	1671139 6e1e36e4626afca96c96b54799b14de83ff61ea1	no	7
Warnings:					
Information:					
2	Information Disclosure Statement (IDS) Form (SB08)	2189364.PDF	37112 b6de1ec39c1acf02b67c01dea5b91a06e7f4b079	no	6
Warnings:					
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3	Authorization to access Appl. by Trilateral Office	2189363.PDF	37333 e10560c806ee36e50efffc7367cf505110f0fa3c	no	1
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Warnings:					
Information:					
5	Power of Attorney	2189361.pdf	1261114 b6e80db9af35cdce8bb804ded993f713a9b9d06b	no	7
Warnings:					
Information:					
6	Drawings-only black and white line drawings	2187613.PDF	91305 00a21947cc8e5e2ad60fe6ffd0992b04826b69d2	no	6
Warnings:					
Information:					
7	Abstract	2187612.PDF	24251 d405c5f52fd5a4e4091be4737654361f652700dc	no	1
Warnings:					
Information:					

8	Claims	2187611.PDF	27371 be77d001a0bfcadb03270fe6ceeb63c89eb4bbe3	no	2
Warnings:					
Information:					
9	Specification	2187610.PDF	98001 d7962565a16d55eef333b4e858f967e8ace55f62	no	14
Warnings:					
Information:					
10	Non Patent Literature	NPL1.pdf	19547261 a0081e66a72ad92da885c4f956cecd627f00e368	no	55
Warnings:					
Information:					
11	Non Patent Literature	NPL2.pdf	7291639 15d80bfb2ad4afbe73f7b0c67e12d8f84542f11d	no	34
Warnings:					
Information:					
12	Fee Worksheet (SB06)	fee-info.pdf	34964 262396ab8a56d2f99d33df95e08f582017981f5d	no	2
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If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	NAUP1863USA3
	Application Number	
Title of Invention	SEMICONDUCTOR DEVICE WITH EPITAXIAL STRUCTURES	

The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76.
This document may be completed electronically and submitted to the Office in electronic format using the Electronic Filing System (EFS) or the document may be printed and included in a paper filed application.

Secrecy Order 37 CFR 5.2

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Prefix	Given Name	Middle Name	Family Name	Suffix
	Chun-Yu		Chen	

Residence Information (Select One) ○ US Residency ◉ Non US Residency ○ Active US Military Service

City	Taichung City	Country of Residence i	TW

Mailing Address of Inventor:

Address 1	No.112-1, Sec. 5, Shatian Rd., Longjing Dist.
Address 2	

City	Taichung City	State/Province	
Postal Code		**Country** i	TW

All Inventors Must Be Listed - Additional Inventor Information blocks may be generated within this form by selecting the **Add** button. Add

Correspondence Information:

PTO/AIA/14 (12-13)
Approved for use through 01/31/2014. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	NAUP1863USA3
	Application Number	
Title of Invention	SEMICONDUCTOR DEVICE WITH EPITAXIAL STRUCTURES	

Enter either Customer Number or complete the Correspondence Information section below. For further information see 37 CFR 1.33(a).			
☐ An Address is being provided for the correspondence Information of this application.			
Customer Number	27765		
Email Address	scottmargo@naipo.com	Add Email	Remove Email

Application Information:

Title of the Invention	SEMICONDUCTOR DEVICE WITH EPITAXIAL STRUCTURES		
Attorney Docket Number	NAUP1863USA3	**Small Entity Status Claimed** ☐	
Application Type	Nonprovisional		
Subject Matter	Utility		
Total Number of Drawing Sheets (if any)	6	**Suggested Figure for Publication (if any)**	

Filing By Reference :

Only compete this section when filing an application by reference under 35 U.S.C. 111(c) and 37 CFR 1.57(a). Do not complete this section if application papers including a specification and any drawings are being filed. Any domestic benefit or foreign priority information must be provided in the appropriate section(s) below (i.e., "Domestic Benefit/National Stage Information" and "Foreign Priority Information").

For the purposes of a filing date under 37 CFR 1.53(b), the description and any drawings of the present application are replaced by this reference to the previously filed application, subject to conditions and requirements of 37 CFR 1.57(a).

Application number of the previously filed application	Filing date (YYYY-MM-DD)	Intellectual Property Authority or Country i

Publication Information:

☐ Request Early Publication (Fee required at time of Request 37 CFR 1.219)

☐ **Request Not to Publish.** I hereby request that the attached application not be published under 35 U.S.C. 122(b) and certify that the invention disclosed in the attached application **has not and will not** be the subject of an application filed in another country, or under a multilateral international agreement, that requires publication at eighteen months after filing.

Representative Information:

Representative information should be provided for all practitioners having a power of attorney in the application. Providing this information in the Application Data Sheet does not constitute a power of attorney in the application (see 37 CFR 1.32).
Either enter Customer Number or complete the Representative Name section below. If both sections are completed the customer Number will be used for the Representative Information during processing.

Please Select One:	◉ Customer Number	○ US Patent Practitioner	○ Limited Recognition (37 CFR 11.9)
Customer Number	27765		

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	NAUP1863USA3
	Application Number	
Title of Invention	SEMICONDUCTOR DEVICE WITH EPITAXIAL STRUCTURES	

Domestic Benefit/National Stage Information:

This section allows for the applicant to either claim benefit under 35 U.S.C. 119(e), 120, 121, or 365(c) or indicate National Stage entry from a PCT application. Providing this information in the application data sheet constitutes the specific reference required by 35 U.S.C. 119(e) or 120, and 37 CFR 1.78.
When referring to the current application, please leave the application number blank.

Prior Application Status	Pending		Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)
	Continuation of	13960816	2013-08-07

Additional Domestic Benefit/National Stage Data may be generated within this form by selecting the **Add** button. Add

Foreign Priority Information:

This section allows for the applicant to claim priority to a foreign application. Providing this information in the application data sheet constitutes the claim for priority as required by 35 U.S.C. 119(b) and 37 CFR 1.55(d). When priority is claimed to a foreign application that is eligible for retrieval under the priority document exchange program (PDX) [i] the information will be used by the Office to automatically attempt retrieval pursuant to 37 CFR 1.55(h)(1) and (2). Under the PDX program, applicant bears the ultimate responsibility for ensuring that a copy of the foreign application is received by the Office from the participating foreign intellectual property office, or a certified copy of the foreign priority application is filed, within the time period specified in 37 CFR 1.55(g)(1).

Remove

Application Number	Country [i]	Filing Date (YYYY-MM-DD)	Access Code [i] (if applicable)

Additional Foreign Priority Data may be generated within this form by selecting the **Add** button. Add

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications

☐ This application (1) claims priority to or the benefit of an application filed before March 16, 2013 and (2) also contains, or contained at any time, a claim to a claimed invention that has an effective filing date on or after March 16, 2013.
NOTE: By providing this statement under 37 CFR 1.55 or 1.78, this application, with a filing date on or after March 16, 2013, will be examined under the first inventor to file provisions of the AIA.

PTO/AIA/14 (12-13)
Approved for use through 01/31/2014. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	NAUP1863USA3
	Application Number	
Title of Invention	SEMICONDUCTOR DEVICE WITH EPITAXIAL STRUCTURES	

Authorization to Permit Access:

☒ Authorization to Permit Access to the Instant Application by the Participating Offices

If checked, the undersigned hereby grants the USPTO authority to provide the European Patent Office (EPO), the Japan Patent Office (JPO), the Korean Intellectual Property Office (KIPO), the World Intellectual Property Office (WIPO), and any other intellectual property offices in which a foreign application claiming priority to the instant patent application is filed access to the instant patent application. See 37 CFR 1.14(c) and (h). This box should not be checked if the applicant does not wish the EPO, JPO, KIPO, WIPO, or other intellectual property office in which a foreign application claiming priority to the instant patent application is filed to have access to the instant patent application.

In accordance with 37 CFR 1.14(h)(3), access will be provided to a copy of the instant patent application with respect to: 1) the instant patent application-as-filed; 2) any foreign application to which the instant patent application claims priority under 35 U.S.C. 119(a)-(d) if a copy of the foreign application that satisfies the certified copy requirement of 37 CFR 1.55 has been filed in the instant patent application; and 3) any U.S. application-as-filed from which benefit is sought in the instant patent application.

In accordance with 37 CFR 1.14(c), access may be provided to information concerning the date of filing this Authorization.

Applicant Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

Applicant 1 Remove

If the applicant is the inventor (or the remaining joint inventor or inventors under 37 CFR 1.45), this section should not be completed. The information to be provided in this section is the name and address of the legal representative who is the applicant under 37 CFR 1.43; or the name and address of the assignee, person to whom the inventor is under an obligation to assign the invention, or person who otherwise shows sufficient proprietary interest in the matter who is the applicant under 37 CFR 1.46. If the applicant is an applicant under 37 CFR 1.46 (assignee, person to whom the inventor is obligated to assign, or person who otherwise shows sufficient proprietary interest) together with one or more joint inventors, then the joint inventor or inventors who are also the applicant should be identified in this section.

Clear

◉ Assignee	○ Legal Representative under 35 U.S.C. 117	○ Joint Inventor
○ Person to whom the inventor is obligated to assign.	○ Person who shows sufficient proprietary interest	

If applicant is the legal representative, indicate the authority to file the patent application, the inventor is:

Name of the Deceased or Legally Incapacitated Inventor :

If the Applicant is an Organization check here. ☒

Organization Name	UNITED MICROELECTRONICS CORP.

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	NAUP1863USA3
	Application Number	
Title of Invention	SEMICONDUCTOR DEVICE WITH EPITAXIAL STRUCTURES	

Mailing Address Information:			
Address 1	No.3, Li-Hsin Road 2,		
Address 2	Science-Based Industrial Park		
City	Hsin-Chu City	**State/Province**	
Country i TW		Postal Code	
Phone Number		Fax Number	
Email Address			

Additional Applicant Data may be generated within this form by selecting the Add button. Add

Assignee Information including Non-Applicant Assignee Information:

Providing assignment information in this section does not subsitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

Assignee 1

Complete this section if assignee information, including non-applicant assignee information, is desired to be included on the patent application publication . An assignee-applicant identified in the "Applicant Information" section will appear on the patent application publication as an applicant. For an assignee-applicant, complete this section only if identification as an assignee is also desired on the patent application publication.

Remove

If the Assignee or Non-Applicant Assignee is an Organization check here. ☐

Prefix	**Given Name**	Middle Name	**Family Name**	Suffix

Mailing Address Information For Assignee including Non-Applicant Assignee:

Address 1			
Address 2			
City		**State/Province**	
Country i		Postal Code	
Phone Number		Fax Number	
Email Address			

Additional Assignee or Non-Applicant Assignee Data may be generated within this form by selecting the Add button. Add

PTO/AIA/14 (12-13)
Approved for use through 01/31/2014. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	NAUP1863USA3
	Application Number	
Title of Invention	SEMICONDUCTOR DEVICE WITH EPITAXIAL STRUCTURES	

Signature:

Remove

NOTE: This form must be signed in accordance with 37 CFR 1.33. See 37 CFR 1.4 for signature requirements and certifications					
Signature	/Scott Margo/			Date (YYYY-MM-DD)	2015-03-02
First Name	Scott	Last Name	Margo	Registration Number	56277
Additional Signature may be generated within this form by selecting the Add button. Add					

This collection of information is required by 37 CFR 1.76. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 23 minutes to complete, including gathering, preparing, and submitting the completed application data sheet form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these records.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

COMBINE DECLARATION (37 CFR 1.63) FOR UTILITY OR DESIGN APPLICATION USING AN APPLICATION DATA SHEET (37 CFR 1.76) AND ASSIGNMENT

Title of Invention:
SEMICONDUCTOR DEVICE

As the below named inventor, I hereby declare that:
This declaration is directed to:

☑ The attached application, or

☐ United States application number _____ filed on _____, or

☐ PCT international application number _____ filed on _____

The above-identified application was made or authorized to be made by me.

I believe that I am the original inventor or an original joint inventor of a claimed invention in the application.

I hereby acknowledge that any willful false statement made in this declaration is punishable under18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both.

In consideration of the payment by **UNITED MICROELECTRONICS CORP.** having a postal address of

No.3, Li-Hsin Road 2, Science-Based Industrial Park, Hsin-Chu City 300, Taiwan, R.O.C.

(referred to as "ASSIGNEE"below) to I of the sum of One Dollar ($ 1.00), the receipt of which is hereby acknowledged, andfor other good and valuable consideration.

I hereby sell, assign and transfer to ASSIGNEE and the successors and assignees of the ASSIGNEE the entire right, title and interest in and to any and all improvements which are disclosed in the invention as above-identified application and, in and to, all Letters Patent to be obtained for said invention by the above application or any continuations, continuation-in-part, divisions, renewals, substitutes, or extensions thereof, and as to Letters Patent any reissue or re-examination thereof.

I hereby covenant that no assignment, sale, agreement or encumbrance has been or will be made or entered into which would conflict with this assignment;

I further covenant that ASSIGNEE will, upon its request, be provided promptly with all pertinent facts and documents relating to said invention and said Letters Patent and legal equivalents as may be known and accessible to I and will testify as to the same in any interference, litigation proceeding related thereto and will promptly execute and deliver to ASSIGNEE or its legal

representatives any and all papers, instruments or affidavits required to apply for, obtain, maintain, issue and enforce said application, said invention and said Letters Patent and said equivalents thereof which may be necessary or desirable to carry out the proposes thereof.
IN WINTNESS WHEREOF, I have hereunto set hand and seal this AUG 0 1 2013 (Date of signing)

Note: An application data sheet (PTO/SB/14 or equivalent), including naming the entire inventive entity, must accompany this form. Use this form for each additional inventor.

Docket No NAUP1863USA

LEGAL NAME OF INVENTOR(ASSIGNOR)

Inventor: **Chin-I Liao** Date: AUG 01 2013

Signature: Chin I Liao

COMBINE DECLARATION (37 CFR 1.63) FOR UTILITY OR DESIGN APPLICATION USING AN APPLICATION DATA SHEET (37 CFR 1.76) AND ASSIGNMENT

Title of Invention:
SEMICONDUCTOR DEVICE

As the below named inventor, I hereby declare that:
This declaration is directed to:

☑ The attached application, or

☐ United States application number _____ filed on _____, or

☐ PCT international application number _____ filed on _____

The above-identified application was made or authorized to be made by me.

I believe that I am the original inventor or an original joint inventor of a claimed invention in the application.

I hereby acknowledge that any willful false statement made in this declaration is punishable under18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both.

In consideration of the payment by **UNITED MICROELECTRONICS CORP.** having a postal address of

No.3, Li-Hsin Road 2, Science-Based Industrial Park, Hsin-Chu City 300, Taiwan, R.O.C.

(referred to as "ASSIGNEE"below) to I of the sum of One Dollar ($ 1.00), the receipt of which is hereby acknowledged, andfor other good and valuable consideration.

I hereby sell, assign and transfer to ASSIGNEE and the successors and assignees of the ASSIGNEE the entire right, title and interest in and to any and all improvements which are disclosed in the invention as above-identified application and, in and to, all Letters Patent to be obtained for said invention by the above application or any continuations, continuation-in-part, divisions, renewals, substitutes, or extensions thereof, and as to Letters Patent any reissue or re-examination thereof.

I hereby covenant that no assignment, sale, agreement or encumbrance has been or will be made or entered into which would conflict with this assignment;

I further covenant that ASSIGNEE will, upon its request, be provided promptly with all pertinent facts and documents relating to said invention and said Letters Patent and legal equivalents as may be known and accessible to I and will testify as to the same in any interference, litigation proceeding related thereto and will promptly execute and deliver to ASSIGNEE or its legal

representatives any and all papers, instruments or affidavits required to apply for, obtain, maintain, issue and enforce said application, said invention and said Letters Patent and said equivalents thereof which may be necessary or desirable to carry out the proposes thereof.
IN WINTNESS WHEREOF, I have hereunto set hand and seal this AUG 0 1 2013 (Date of signing)

Note: An application data sheet (PTO/SB/14 or equivalent), including naming the entire inventive entity, must accompany this form. Use this form for each additional inventor.

Docket No NAUP1863USA

LEGAL NAME OF INVENTOR(ASSIGNOR)

Inventor: **Chun-Yu Chen** Date: AUG 01 2013

Signature: Chun Yu Chen

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	TOT CLAIMS	IND CLAIMS
14/637,412	03/04/2015	2812	1600	NAUP1863USA3	11	1

CONFIRMATION NO. 5822

27765
NORTH AMERICA INTELLECTUAL PROPERTY CORPORATION
P.O. BOX 506
MERRIFIELD, VA 22116

FILING RECEIPT

OC00000073977748

Date Mailed: 03/16/2015

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Inventor(s)

Chin-I Liao, Tainan City, TAIWAN;
Chun-Yu Chen, Taichung City, TAIWAN;

Applicant(s)

United Microelectronics Corp., Hsin-Chu City, TAIWAN

Power of Attorney: The patent practitioners associated with Customer Number 27765

Domestic Priority data as claimed by applicant

This application is a CON of 13/960,816 08/07/2013

Foreign Applications for which priority is claimed (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see http://www.uspto.gov for more information.) - None.
Foreign application information must be provided in an Application Data Sheet in order to constitute a claim to foreign priority. See 37 CFR 1.55 and 1.76.

Permission to Access - A proper **Authorization to Permit Access to Application by Participating Offices** (PTO/SB/39 or its equivalent) has been received by the USPTO.

If Required, Foreign Filing License Granted: 03/13/2015

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 14/637,412**

Projected Publication Date: 06/25/2015

Non-Publication Request: No

Early Publication Request: No

Title

SEMICONDUCTOR DEVICE WITH EPITAXIAL STRUCTURES

Preliminary Class

438

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications: No

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at http://www.uspto.gov/web/offices/pac/doc/general/index.html.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, http://www.stopfakes.gov. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4258).

LICENSE FOR FOREIGN FILING UNDER

Title 35, United States Code, Section 184

Title 37, Code of Federal Regulations, 5.11 & 5.15

GRANTED

The applicant has been granted a license under 35 U.S.C. 184, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" followed by a date appears on this form. Such licenses are issued in all applications where the conditions for issuance of a license have been met, regardless of whether or not a license may be required as set forth in 37 CFR 5.15. The scope and limitations of this license are set forth in 37 CFR 5.15(a) unless an earlier license has been issued under 37 CFR 5.15(b). The license is subject to revocation upon written notification. The date indicated is the effective date of the license, unless an earlier license of similar scope has been granted under 37 CFR 5.13 or 5.14.

This license is to be retained by the licensee and may be used at any time on or after the effective date thereof unless it is revoked. This license is automatically transferred to any related applications(s) filed under 37 CFR 1.53(d). This license is not retroactive.

The grant of a license does not in any way lessen the responsibility of a licensee for the security of the subject matter as imposed by any Government contract or the provisions of existing laws relating to espionage and the national security or the export of technical data. Licensees should apprise themselves of current regulations especially with respect to certain countries, of other agencies, particularly the Office of Defense Trade Controls, Department of State (with respect to Arms, Munitions and Implements of War (22 CFR 121-128)); the Bureau of Industry and Security, Department of Commerce (15 CFR parts 730-774); the Office of Foreign AssetsControl, Department of Treasury (31 CFR Parts 500+) and the Department of Energy.

NOT GRANTED

No license under 35 U.S.C. 184 has been granted at this time, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" DOES NOT appear on this form. Applicant may still petition for a license under 37 CFR 5.12, if a license is desired before the expiration of 6 months from the filing date of the application. If 6 months has lapsed from the filing date of this application and the licensee has not received any indication of a secrecy order under 35 U.S.C. 181, the licensee may foreign file the application pursuant to 37 CFR 5.15(b).

SelectUSA

The United States represents the largest, most dynamic marketplace in the world and is an unparalleled location for business investment, innovation, and commercialization of new technologies. The U.S. offers tremendous resources and advantages for those who invest and manufacture goods here. Through SelectUSA, our nation works to promote and facilitate business investment. SelectUSA provides information assistance to the international investor community; serves as an ombudsman for existing and potential investors; advocates on behalf of U.S. cities, states, and regions competing for global investment; and counsels U.S. economic development organizations on investment attraction best practices. To learn more about why the United States is the best country in the world to develop technology, manufacture products, deliver services, and grow your business, visit http://www.SelectUSA.gov or call +1-202-482-6800.

PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number: 14/637,412

APPLICATION AS FILED - PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY FEE($)
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	280
SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	600
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	720
TOTAL CLAIMS (37 CFR 1.16(i))	11 minus 20 =	*			OR	x 80 =	0.00
INDEPENDENT CLAIMS (37 CFR 1.16(h))	1 minus 3 =	*				x 420 =	0.00
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						0.00
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							0.00
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	1600

APPLICATION AS AMENDED - PART II

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY ADDITIONAL FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE($)
AMENDMENT A	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE($)	ADDITIONAL FEE($)		RATE($)	ADDITIONAL FEE($)
AMENDMENT B	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest found in the appropriate box in column 1.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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P.O. Box 1450
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www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
14/637,412	03/04/2015	Chin-I Liao	NAUP1863USA3

CONFIRMATION NO. 5822

27765
NORTH AMERICA INTELLECTUAL PROPERTY CORPORATION
P.O. BOX 506
MERRIFIELD, VA 22116

PUBLICATION NOTICE

OC000000075945561

Title:SEMICONDUCTOR DEVICE WITH EPITAXIAL STRUCTURES

Publication No.US-2015-0179645-A1
Publication Date:06/25/2015

NOTICE OF PUBLICATION OF APPLICATION

The above-identified application will be electronically published as a patent application publication pursuant to 37 CFR 1.211, et seq. The patent application publication number and publication date are set forth above.

The publication may be accessed through the USPTO's publically available Searchable Databases via the Internet at www.uspto.gov. The direct link to access the publication is currently http://www.uspto.gov/patft/.

The publication process established by the Office does not provide for mailing a copy of the publication to applicant. A copy of the publication may be obtained from the Office upon payment of the appropriate fee set forth in 37 CFR 1.19(a)(1). Orders for copies of patent application publications are handled by the USPTO's Office of Public Records. The Office of Public Records can be reached by telephone at (703) 308-9726 or (800) 972-6382, by facsimile at (703) 305-8759, by mail addressed to the United States Patent and Trademark Office, Office of Public Records, Alexandria, VA 22313-1450 or via the Internet.

In addition, information on the status of the application, including the mailing date of Office actions and the dates of receipt of correspondence filed in the Office, may also be accessed via the Internet through the Patent Electronic Business Center at www.uspto.gov using the public side of the Patent Application Information and Retrieval (PAIR) system. The direct link to access this status information is currently http://pair.uspto.gov/. Prior to publication, such status information is confidential and may only be obtained by applicant using the private side of PAIR.

Further assistance in electronically accessing the publication, or about PAIR, is available by calling the Patent Electronic Business Center at 1-866-217-9197.

Office of Data Managment, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/637,412	03/04/2015	Chin-I Liao	NAUP1863USA3	5822

27765 7590 10/07/2015

NORTH AMERICA INTELLECTUAL PROPERTY CORPORATION
P.O. BOX 506
MERRIFIELD, VA 22116

EXAMINER
PATTON, PAUL E

ART UNIT	PAPER NUMBER
2822	

NOTIFICATION DATE	DELIVERY MODE
10/07/2015	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

Patent.admin.uspto.Rcv@naipo.com
mis.ap.uspto@naipo.com

Office Action Summary	Application No. 14/637,412	Applicant(s) LIAO ET AL.	
	Examiner PAUL PATTON	Art Unit 2822	AIA (First Inventor to File) Status Yes

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *March 4, 2015*.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

5)☒ Claim(s) *1-11* is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6)☐ Claim(s) _____ is/are allowed.

7)☒ Claim(s) *1-11* is/are rejected.

8)☐ Claim(s) _____ is/are objected to.

9)☐ Claim(s) _____ are subject to restriction and/or election requirement.

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☒ The drawing(s) filed on *March 4, 2015* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☐ All b)☐ Some** c)☐ None of the:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☒ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b) Paper No(s)/Mail Date *3/4/2015*.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

4) ☐ Other: _____.

DETAILED ACTION

Notice of Pre-AIA or AIA Status

1. The present application, filed on or after March 16, 2013, is being examined under the first inventor to file provisions of the AIA.

Double Patenting

2. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory double patenting rejection is appropriate where the claims at issue are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the reference application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of

activities undertaken within the scope of a joint research agreement. A terminal disclaimer must be signed in compliance with 37 CFR 1.321(b).

The USPTO internet Web site contains terminal disclaimer forms which may be used. Please visit http://www.uspto.gov/forms/. The filing date of the application will determine what form should be used. A web-based eTerminal Disclaimer may be filled out completely online using web-screens. An eTerminal Disclaimer that meets all requirements is auto-processed and approved immediately upon submission. For more information about eTerminal Disclaimers, refer to http://www.uspto.gov/patents/process/file/efs/guidance/eTD-info-I.jsp.

3. Claims 1 – 11 are rejected on the ground of nonstatutory double patenting as being unpatentable over claims 1 -11 of U.S. Patent No. 9006805. Although the claims at issue are not identical, they are not patentably distinct from each other because applicant has described the same invention as the reference patent except for stating that the cap layer is formed from two merged cap layers resulting in the identical structure. Hence, the same invention is described in only slightly different terms..

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to PAUL PATTON whose telephone number is (571)272-9762. The examiner can normally be reached on 7:00 - 5:30 Monday through Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Brett A. Feeney can be reached on 571-270-5484. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Paul E Patton
Examiner
Art Unit 2822

/P. P./
Examiner, Art Unit 2822

Notice of References Cited	Application/Control No. 14/637,412	Applicant(s)/Patent Under Reexamination LIAO ET AL.	
	Examiner PAUL PATTON	Art Unit 2822	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	CPC Classification	US Classification
*	A	US-9,006,805 B2	04-2015	Liao; Chin-l	H01L29/41791	257/288
	B	US-				
	C	US-				
	D	US-				
	E	US-				
	F	US-				
	G	US-				
	H	US-				
	I	US-				
	J	US-				
	K	US-				
	L	US-				
	M	US-				

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	CPC Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	14637412	LIAO ET AL.
	Examiner	Art Unit
	PAUL PATTON	2822

CPC- SEARCHED		
Symbol	Date	Examiner
H01L29/66795 H01L29/66628 H01L29/41791 H01L29/7851	9/25/2015	PEP

CPC COMBINATION SETS - SEARCHED		
Symbol	Date	Examiner

US CLASSIFICATION SEARCHED			
Class	Subclass	Date	Examiner

SEARCH NOTES		
Search Notes	Date	Examiner
Search History Attached	9/25/2015	PEP

INTERFERENCE SEARCH			
US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	
	Filing Date	
	First Named Inventor	Chin-I Liao
	Art Unit	N/A
	Examiner Name	N/A
	Attorney Docket Number	NAUP1863USA3

U.S.PATENTS						
Examiner Initial*	Cite No	Patent Number	Kind Code	Issue Date	Name	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	8455313	B1	2013-06-04	Basker	
	2	6043138		2000-03-28	Ibok; Effiong E.	all
	3	6492216		2002-12-10	Yeo; Yee-Chia	all
	4	6921963		2005-07-26	Krivokapic; Zoran	all
	5	7087477		2006-08-08	Fried; David M.	all
	6	7091551		2006-08-15	Anderson; Brent A.	all
	7	7247887		2007-07-24	King; Tsu-Jae	all
	8	7250658		2007-07-31	Doris; Bruce B.	all

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /P.P./

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	
	Filing Date	
	First Named Inventor	Chin-I Liao
	Art Unit	N/A
	Examiner Name	N/A
	Attorney Docket Number	NAUP1863USA3

	9	7309626		2007-12-18	Ieong; Mei-Kei	all
	10	7352034		2008-04-01	Booth, Jr.; Roger Allen	all
	11	7470570		2008-12-30	Beintner; Jochen	all
	12	7531437		2009-05-12	Brask; Justin K.	all
	13	7569857		2009-08-04	Simon, legal representative; David	all
	14	6888181		2005-05-03	Liao	
	15	8362575		2013-01-29	Kwok	
U.S.PATENT APPLICATION PUBLICATIONS						
Examiner Initial*	Cite No	Publication Number	Kind Code	Publication Date	Name	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	20130200470	A1	2013-08-08	Liu	
	2	20040195624		2004-10-07	Liu, Chee-Wee;	all

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /P.P./

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	
	Filing Date	
	First Named Inventor	Chin-I Liao
	Art Unit	N/A
	Examiner Name	N/A
	Attorney Docket Number	NAUP1863USA3

	3	20050051825		2005-03-10	Fujiwara, Makoto;	all
	4	20060099830		2006-05-11	Walther; Steven R.;	all
	5	20060286729		2006-12-21	Kavalieros; Jack;	all
	6	20070108528		2007-05-17	Anderson; Brent A.;	all
	7	20070158756		2007-07-12	Dreeskornfeld; Lars;	all
	8	20080157208		2008-07-03	Fischer; Kevin J.;	all
	9	20090124097		2009-05-14	Cheng; Kangguo;	all
	10	20090242964		2009-10-01	Akil; Nader;	all
	11	20090269916		2009-10-29	KANG; Inkuk;	all
	12	20100048027		2010-02-25	Cheng; Kangguo;	all
	13	20100072553		2010-03-25	XU; Jeff J.;	all

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /P.P./

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	
	Filing Date	
	First Named Inventor	Chin-I Liao
	Art Unit	N/A
	Examiner Name	N/A
	Attorney Docket Number	NAUP1863USA3

	14	20100144121		2010-06-10	Chang; Cheng-Hung;	all
	15	20100167506		2010-07-01	LIN; Simon Su-Horng;	all
	16	20110042744		2011-02-24	Cheng	
	17	20110298058	A1	2011-12-08	Kawasaki	

.

FOREIGN PATENT DOCUMENTS

Examiner Initial*	Cite No	Foreign Document Number	Country Code	Kind Code	Publication Date	Name	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	
	1							

NON-PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	
	1	Liu, Source: 2012 symposium on VLSI technology short course; Title: FinFET history, fundamentals and future, 2012/06/11	
	2	Kavalieros, Source: intel corporation; Title: Tri-gate transistor architecture with high-K gate dielectrics, metal gates and strain engineering, 2006/06/13	

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /P.P./

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	
	Filing Date	
	First Named Inventor	Chin-I Liao
	Art Unit	N/A
	Examiner Name	N/A
	Attorney Docket Number	NAUP1863USA3

EXAMINER SIGNATURE			
Examiner Signature	/Paul Patton/	Date Considered	09/25/2015
*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.			

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /P.P./

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S1	41	((liao near (chin adj l))(chen near (chun adj yu))).in. and "257".clas.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2014/06/23 20:46
S2	10568	(H01L29/66795 H01L29/66628 H01L29/41791 H01L29/7851).cpc.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2014/06/23 21:03
S3	4	S1 and fin same epitaxial same recess	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2014/06/23 21:05
S4	83	S2 and fin same epitaxial same recess	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2014/06/23 21:05
S5	14	US-6043138-$.DID. OR US-6492216-$.DID. OR US-6921963-$.DID. OR US-7087477-$.DID. OR US-7091551-$.DID. OR US-7247887-$.DID. OR US-7250658-$.DID.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2014/06/23 22:25
S6	13	US-7352034-$.DID. OR US-7470570-$.DID. OR US-7531437-$.DID. OR US-7569857-$.DID. OR US-6888181-$.DID. OR US-8362575-$.DID.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2014/06/23 22:25
S7	16	"20040195624" "20050051825" "20060099830"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2014/06/23 22:26
S8	38	"20060286729" "20070108528"	US-PGPUB;	OR	OFF	2014/06/23

		"20070158756" "20080157208" "20090124097" "20090242964" "20090269916" "20100048027" "20100072553" "20100144121" "20100167506"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB			22:27
S9	5	"20110042744"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2014/06/23 22:27
S10	86	S5 S6 S7 S8 S9	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2014/06/23 22:27
S11	4	"7531437".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2014/12/09 18:26
S12	3	"20110298058"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2014/12/11 15:02
S13	0	(two and fin and shaped and disposed and substrate and gate and sructure and covering and two and epitaxial and respectively and contacting and spaced and apart and silicon and cap and simultaneously and surrounding).clm. and "257".clas.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2014/12/11 15:31

EAST Search History (Interference)

< This search history is empty>

9/ 25/ 2015 3:33:03 PM
C:\ Users\ ppatton\ Documents\ EAST\ Workspaces\ 14-637412.wsp

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United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
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Alexandria, Virginia 22313-1450
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BIB DATA SHEET

CONFIRMATION NO. 5822

SERIAL NUMBER	FILING or 371(c) DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
14/637,412	03/04/2015 RULE	257	2822	NAUP1863USA3

APPLICANTS
United Microelectronics Corp., Hsin-Chu City, TAIWAN;

INVENTORS
Chin-I Liao, Tainan City, TAIWAN;
Chun-Yu Chen, Taichung City, TAIWAN;

**** CONTINUING DATA ***************************
This application is a CON of 13/960,816 08/07/2013 PAT 9006805

**** FOREIGN APPLICATIONS ***************************

**** IF REQUIRED, FOREIGN FILING LICENSE GRANTED ****
03/13/2015

Foreign Priority claimed	35 USC 119(a-d) conditions met	Verified and Acknowledged	Met after Allowance	STATE OR COUNTRY	SHEETS DRAWINGS	TOTAL CLAIMS	INDEPENDENT CLAIMS
☐ Yes ☑ No	☐ Yes ☑ No	/PAUL E PATTON/ Examiner's Signature	☐ PEP Initials	TAIWAN	6	11	1

ADDRESS
NORTH AMERICA INTELLECTUAL PROPERTY CORPORATION
P.O. BOX 506
MERRIFIELD, VA 22116
UNITED STATES

TITLE
SEMICONDUCTOR DEVICE WITH EPITAXIAL STRUCTURES

FILING FEE RECEIVED	FEES: Authority has been given in Paper	
1600	No._____ to charge/credit DEPOSIT ACCOUNT No._____ for following:	☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit

BIB (Rev. 05/07).

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	14637412	LIAO ET AL.
	Examiner	Art Unit
	PAUL PATTON	2822

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	09/25/2015								
	1	✓								
	2	✓								
	3	✓								
	4	✓								
	5	✓								
	6	✓								
	7	✓								
	8	✓								
	9	✓								
	10	✓								
	11	✓								

SEMICONDUCTOR DEVICE WITH EPITAXIAL STRUCTURES

Appl. No.	: 14/637,412	Confirmation No.	5822
First Named Inventor	: Chin-I Liao		
Filed	: March 4, 2015		
TC/A.U.	: 2822		
Examiner	: PATTON, PAUL E		
Docket No.	: NAUP1863USA3		
Customer No.	: 27765		

Commissioner for Patents
P.O. Box 1450
Alexandria VA 22313-1450

INTRODUCTORY COMMENTS

In response to the Office action of October 07, 2015, please amend the above-identified application as follows:

Remarks begin on page 2 of this paper.

PTO/AIA/26 (04-13)
Approved for use through 04/30/2013. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

TERMINAL DISCLAIMER TO OBVIATE A DOUBLE PATENTING REJECTION OVER A "PRIOR" PATENT	Docket Number (Optional) NAUP1863USA3

In re Application of: Chin-I Liao et al.

Application No.: 14/637,412

Filed: Mar. 04, 2015

For: SEMICONDUCTOR DEVICE WITH EPITAXIAL STRUCTURES

The applicant, UNITED MICROELECTRONICS CORP., owner of 100 percent interest in the instant application hereby disclaims, except as provided below, the terminal part of the statutory term of any patent granted on the instant application which would extend beyond the expiration date of the full statutory term of **prior patent** No. 9,006,805 as the term of said **prior patent** is presently shortened by any terminal disclaimer. The applicant hereby agrees that any patent so granted on the instant application shall be enforceable only for any during such period that it and the **prior patent** are commonly owned. This agreement runs with any patent granted on the instant application and is binding upon the grantee, its successors or assigns.

In making the above disclaimer, the applicant does not disclaim the terminal part of the term of any patent granted on the instant application that would extend to the expiration date of the full statutory term of the **prior patent**, "as the term of said **prior patent** is presently shortened by any terminal disclaimer," in the event that said **prior patent** later:

expires for failure to pay a maintenance fee;
is held unenforceable;
is found invalid by a court of competent jurisdiction;
is statutorily disclaimed in whole or terminally disclaimed under 37 CFR 1.321;
has all claims canceled by a reexamination certificate;
is reissued; or
is in any manner terminated prior to the expiration of its full statutory term as presently shortened by any terminal disclaimer.

Check either box 1 or 2 below, if appropriate.

1. ☐ The undersigned is the applicant. If the applicant is an assignee, the undersigned is authorized to act on behalf of the assignee.

I hereby acknowledge that any willful false statements made are punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both.

2. ☑ The undersigned is an attorney or agent of record. Reg. No. 56277

/Scott Margo/ — Signature
12/14/2015 — Date

Scott Margo — Typed or printed name

Agent of Record — Title
Voice Mail:3027291562 — Telephone Number

☑ Terminal disclaimer fee under 37 CFR 1.20(d) included. USD 160.00

WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.

This collection of information is required by 37 CFR 1.321. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Electronic Patent Application Fee Transmittal	
Application Number:	14637412
Filing Date:	04-Mar-2015
Title of Invention:	SEMICONDUCTOR DEVICE WITH EPITAXIAL STRUCTURES
First Named Inventor/Applicant Name:	Chin-I Liao
Filer:	Winston Hsu/Lydia Wei
Attorney Docket Number:	NAUP1863USA3
Filed as Large Entity	
Filing Fees for Utility under 35 USC 111(a)	

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Miscellaneous:				
Statutory or Terminal Disclaimer	1814	1	160	160
		Total in USD ($)		**160**

Electronic Acknowledgement Receipt	
EFS ID:	24344751
Application Number:	14637412
International Application Number:	
Confirmation Number:	5822
Title of Invention:	SEMICONDUCTOR DEVICE WITH EPITAXIAL STRUCTURES
First Named Inventor/Applicant Name:	Chin-I Liao
Customer Number:	27765
Filer:	Winston Hsu/Lydia Wei
Filer Authorized By:	Winston Hsu
Attorney Docket Number:	NAUP1863USA3
Receipt Date:	14-DEC-2015
Filing Date:	04-MAR-2015
Time Stamp:	22:34:47
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	$160
RAM confirmation Number	8600
Deposit Account	503105
Authorized User	HSU, WINSTON
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: Charge any Additional Fees required under 37 C.F.R. Section 1.16 (National application filing, search, and examination fees) Charge any Additional Fees required under 37 C.F.R. Section 1.17 (Patent application and reexamination processing fees)	

Charge any Additional Fees required under 37 C.F.R. Section 1.19 (Document supply fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.20 (Post Issuance fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.21 (Miscellaneous fees and charges)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Applicant Arguments/Remarks Made in an Amendment	2432990.PDF	580446 469391d11a830d5caaefe0bc8fbf89aa54df9433	no	2
Warnings:					
Information:					
2	Amendment/Req. Reconsideration-After Non-Final Reject	2432989.PDF	74011 7b66a831706ce39e4b82398e2b613f0a751d3b80	no	1
Warnings:					
Information:					
3	Terminal Disclaimer Filed	2432913.PDF	643165 a5188f5b069ae1ed29eb06dc5a6302f17f4590ad	no	1
Warnings:					
Information:					
4	Fee Worksheet (SB06)	fee-info.pdf	30310 621fd80354b2a4afa1920af14cd41e82a5781dd8	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	1327932		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

REMARKS

Recognizing that Internet communications are not secure, I hereby authorize the USPTO to communicate with me concerning any subject matter of this application by electronic mail. I understand that a copy of these communications will be made of record in the application file.

1. Double Patenting

Claims 1-11 were rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1-11 of U.S. Patent No. 9,006,805.

Response

A terminal disclaimer of the present application (U.S. Patent Application No. 14/637,412) is therefore submitted herewith to overcome the nonstatutory obviousness-type double patenting rejection made to the present application as being unpatentable over claims 1-11 of U.S. Patent No. 9,006,805. Without disclaimer as to the merits of the claims filed in the present application, the terminal disclaimer is in compliance with 37 CFR 1.321(c) or 1.321(d). Acceptance of the terminal disclaimer and withdrawal of the nonstatutory obviousness-type double patenting rejection are respectfully requested.

Applicant respectfully requests that a timely Notice of Allowance be issued in this case.

Sincerely yours,

/Scott Margo/ Date: 12/14/2015

Scott Margo, Patent Agent No. 56,277
P.O. BOX 506, Merrifield, VA 22116, U.S.A.
Voice Mail: 302-729-1562
Facsimile: 806-498-6673
e-mail : ScottMargo@naipo.com

Note: Please leave a message in my voice mail if you need to talk to me. (The time in D.C. is 13 hours behind the Taiwan time, i.e. 9 AM in D.C. = 10 PM in Taiwan.)

Application Number	Application/Control No.	Applicant(s)/Patent under Reexamination	
	14/637,412	LIAO ET AL.	

Document Code - DISQ	Internal Document – DO NOT MAIL

TERMINAL DISCLAIMER	☒ APPROVED	☐ DISAPPROVED
Date Filed : 12/14/15	This patent is subject to a Terminal Disclaimer	

Approved/Disapproved by:

Felicia D. Roberts

9,006,805

U.S. Patent and Trademark Office

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

27765 7590 03/14/2016

NORTH AMERICA INTELLECTUAL PROPERTY CORPORATION
P.O. BOX 506
MERRIFIELD, VA 22116

EXAMINER
PATTON, PAUL E

ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 03/14/2016

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/637,412	03/04/2015	Chin-I Liao	NAUP1863USA3	5822

TITLE OF INVENTION: SEMICONDUCTOR DEVICE WITH EPITAXIAL STRUCTURES

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$960	$0	$0	$960	06/14/2016

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

For purposes of this notice, small entity fees are 1/2 the amount of undiscounted fees, and micro entity fees are 1/2 the amount of small entity fees.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

27765 7590 03/14/2016

NORTH AMERICA INTELLECTUAL PROPERTY CORPORATION
P.O. BOX 506
MERRIFIELD, VA 22116

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/637,412	03/04/2015	Chin-I Liao	NAUP1863USA3	5822

TITLE OF INVENTION: SEMICONDUCTOR DEVICE WITH EPITAXIAL STRUCTURES

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$960	$0	$0	$960	06/14/2016

EXAMINER	ART UNIT	CLASS-SUBCLASS
PATTON, PAUL E	2822	257-192000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

❑ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

❑ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,

(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 _____

2 _____

3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ❑ Corporation or other private group entity ❑ Government

4a. The following fee(s) are submitted:

❑ Issue Fee

❑ Publication Fee (No small entity discount permitted)

❑ Advance Order - # of Copies _____

4b. Payment of Fee(s): **(Please first reapply any previously paid issue fee shown above)**

❑ A check is enclosed.

❑ Payment by credit card. Form PTO-2038 is attached.

❑ The director is hereby authorized to charge the required fee(s), any deficiency, or credits any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)

❑ Applicant certifying micro entity status. See 37 CFR 1.29

NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.

❑ Applicant asserting small entity status. See 37 CFR 1.27

NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.

❑ Applicant changing to regular undiscounted fee status.

NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

PTOL-85 Part B (10-13) Approved for use through 10/31/2013. OMB 0651-0033 U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/637,412	03/04/2015	Chin-I Liao	NAUP1863USA3	5822

27765 7590 03/14/2016

NORTH AMERICA INTELLECTUAL PROPERTY CORPORATION
P.O. BOX 506
MERRIFIELD, VA 22116

EXAMINER	
PATTON, PAUL E	
ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 03/14/2016

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(Applications filed on or after May 29, 2000)

The Office has discontinued providing a Patent Term Adjustment (PTA) calculation with the Notice of Allowance.

Section 1(h)(2) of the AIA Technical Corrections Act amended 35 U.S.C. 154(b)(3)(B)(i) to eliminate the requirement that the Office provide a patent term adjustment determination with the notice of allowance. See Revisions to Patent Term Adjustment, 78 Fed. Reg. 19416, 19417 (Apr. 1, 2013). Therefore, the Office is no longer providing an initial patent term adjustment determination with the notice of allowance. The Office will continue to provide a patent term adjustment determination with the Issue Notification Letter that is mailed to applicant approximately three weeks prior to the issue date of the patent, and will include the patent term adjustment on the patent. Any request for reconsideration of the patent term adjustment determination (or reinstatement of patent term adjustment) should follow the process outlined in 37 CFR 1.705.

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

OMB Clearance and PRA Burden Statement for PTOL-85 Part B

The Paperwork Reduction Act (PRA) of 1995 requires Federal agencies to obtain Office of Management and Budget approval before requesting most types of information from the public. When OMB approves an agency request to collect information from the public, OMB (i) provides a valid OMB Control Number and expiration date for the agency to display on the instrument that will be used to collect the information and (ii) requires the agency to inform the public about the OMB Control Number's legal significance in accordance with 5 CFR 1320.5(b).

The information collected by PTOL-85 Part B is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450. Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No. 14/637,412	Applicant(s) LIAO ET AL.	
	Examiner PAUL PATTON	Art Unit 2822	AIA (First Inventor to File) Status Yes

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *Terminal Disclaimer filed December 14, 2015*.
   ☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on_____.
2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.
3. ☒ The allowed claim(s) is/are *1-11*. As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov .
4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

   Certified copies:

   a) ☐ All b) ☐ Some *c) ☐ None of the:
   1. ☐ Certified copies of the priority documents have been received.
   2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
   3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
4. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
5. ☐ Examiner's Amendment/Comment
6. ☒ Examiner's Statement of Reasons for Allowance
7. ☐ Other _____.

/ROY POTTER/
Primary Examiner, Art Unit 2822

DETAILED ACTION

Notice of Pre-AIA or AIA Status

1. The present application, filed on or after March 16, 2013, is being examined under the first inventor to file provisions of the AIA.

2.

Terminal Disclaimer

3. The terminal disclaimer filed on December 14, 2015 disclaiming the terminal portion of any patent granted on this application which would extend beyond the expiration date of US Patent 9,006,805 has been reviewed and is accepted. The terminal disclaimer has been recorded.

Allowable Subject Matter

4. Claims 1 – 11 are allowed.

5. The following is an examiner's statement of reasons for allowance: The prior art of record, taken alone or in combination, fails to anticipate or render obvious a semiconductor device, comprising: at least two fin-shaped structures, disposed on a substrate; a gate structure, covering the fin-shaped structures; at least two epitaxial structures, disposed at one side of the gate structure and respectively directly contacting each fin-shaped structure, wherein the epitaxial structures are spaced apart from each other; and at least two caps, respectively surrounding the epitaxial structures, wherein at least two adjacent caps are merged together as recited in claim 1 along with all the other limitations of the claims.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled “Comments on Statement of Reasons for Allowance.”

Any inquiry concerning this communication or earlier communications from the examiner should be directed to PAUL PATTON whose telephone number is (571)272-9762. The examiner can normally be reached on 7:00 - 5:30 Monday through Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner’s supervisor, Brett A. Feeney can be reached on 571-270-5484. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Paul E Patton
Examiner
Art Unit 2822

/P. P./
Examiner, Art Unit 2822

/ROY POTTER/
Primary Examiner, Art Unit 2822

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	14637412	LIAO ET AL.
	Examiner	**Art Unit**
	PAUL PATTON	2822

CPC						
Symbol					**Type**	**Version**
H01L		27	/	0886	F	2013-01-01
H01L		29	/	41791	I	2013-01-01
H01L		29	/	7851	I	2013-01-01
H01L		29	/	1608	I	2013-01-01
H01L		29	/	161	I	2013-01-01
H01L		29	/	165	I	2013-01-01
H01L		29	/	267	I	2013-01-01
H01L		29	/	7848	I	2013-01-01
H01L		29	/	66795	I	2013-01-01
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CPC Combination Sets							
Symbol					**Type**	**Set**	**Ranking**	**Version**
			/					
			/					

/PAUL PATTON/ Examiner.Art Unit 2822 (Assistant Examiner)	2/25/2016 (Date)	**Total Claims Allowed:** 11	
/ROY POTTER/ Primary Examiner.Art Unit 2822 (Primary Examiner)	02/29/2016 (Date)	O.G. Print Claim(s) 1	O.G. Print Figure 5

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	14637412	LIAO ET AL.
	Examiner	Art Unit
	PAUL PATTON	2822

US ORIGINAL CLASSIFICATION		INTERNATIONAL CLASSIFICATION									
CLASS	SUBCLASS	CLAIMED					NON-CLAIMED				
		H	0	1	L	29 / 66 (2006.01.01)					
CROSS REFERENCE(S)											
CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)										

/PAUL PATTON/ Examiner.Art Unit 2822	2/25/2016	Total Claims Allowed:	
(Assistant Examiner)	(Date)	11	
/ROY POTTER/ Primary Examiner.Art Unit 2822	02/29/2016	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	5

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	14637412	LIAO ET AL.
	Examiner	Art Unit
	PAUL PATTON	2822

☒ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
1	1														
2	2														
3	3														
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10	10														
11	11														

/PAUL PATTON/ Examiner.Art Unit 2822	2/25/2016	Total Claims Allowed:	
(Assistant Examiner)	(Date)	11	
/ROY POTTER/ Primary Examiner.Art Unit 2822	02/29/2016	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	5

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	14637412	LIAO ET AL.
	Examiner	Art Unit
	PAUL PATTON	2822

CPC- SEARCHED		
Symbol	Date	Examiner
H01L29/66795 H01L29/66628 H01L29/41791 H01L29/7851	9/25/2015	PEP

CPC COMBINATION SETS - SEARCHED		
Symbol	Date	Examiner

US CLASSIFICATION SEARCHED			
Class	Subclass	Date	Examiner

SEARCH NOTES		
Search Notes	Date	Examiner
Search History Attached	9/25/2015	PEP
Consult with K. Picardat	2/25/2016	PEP
Updated Search	2/25/2016	PEP

INTERFERENCE SEARCH			
US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner
H01L29/$		2/25/2016	PEP

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S1	41	((liao near (chin adj l))(chen near (chun adj yu))).in. and "257".clas.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2014/06/23 20:46
S2	10568	(H01L29/66795 H01L29/66628 H01L29/41791 H01L29/7851).cpc.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2014/06/23 21:03
S3	4	S1 and fin same epitaxial same recess	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2014/06/23 21:05
S4	83	S2 and fin same epitaxial same recess	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2014/06/23 21:05
S5	14	US-6043138-$.DID. OR US-6492216-$.DID. OR US-6921963-$.DID. OR US-7087477-$.DID. OR US-7091551-$.DID. OR US-7247887-$.DID. OR US-7250658-$.DID.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2014/06/23 22:25
S6	13	US-7352034-$.DID. OR US-7470570-$.DID. OR US-7531437-$.DID. OR US-7569857-$.DID. OR US-6888181-$.DID. OR US-8362575-$.DID.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2014/06/23 22:25
S7	16	"20040195624" "20050051825" "20060099830"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2014/06/23 22:26
S8	38	"20060286729" "20070108528"	US-PGPUB;	OR	OFF	2014/06/23

		"20070158756" "20080157208" "20090124097" "20090242964" "20090269916" "20100048027" "20100072553" "20100144121" "20100167506"	USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB			22:27
S9	5	"20110042744"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2014/06/23 22:27
S10	86	S5 S6 S7 S8 S9	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2014/06/23 22:27
S11	4	"7531437".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2014/12/09 18:26
S12	3	"20110298058"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2014/12/11 15:02
S13	0	(two and fin and shaped and disposed and substrate and gate and sructure and covering and two and epitaxial and respectively and contacting and spaced and apart and silicon and cap and simultaneously and surrounding).clm. and "257".clas.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2014/12/11 15:31

EAST Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	0	(fin and shaped and structure and disposed and gate and covering and epitaxial and side and respectively and directly and contacting and spaced and apart and cap and surrounding and merged and together).clm.	USPAT; UPAD	OR	OFF	2016/02/25 17:50

2/25/2016 5:51:29 PM
C:\Users\ppatton\Documents\EAST\Workspaces\14-637412.wsp

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

BIB DATA SHEET

CONFIRMATION NO. 5822

SERIAL NUMBER	FILING or 371(c) DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
14/637,412	03/04/2015 RULE	257	2822	NAUP1863USA3

APPLICANTS
United Microelectronics Corp., Hsin-Chu City, TAIWAN;

INVENTORS
Chin-I Liao, Tainan City, TAIWAN;
Chun-Yu Chen, Taichung City, TAIWAN;

**** CONTINUING DATA ***************************
This application is a CON of 13/960,816 08/07/2013 PAT 9006805

**** FOREIGN APPLICATIONS ***************************

**** IF REQUIRED, FOREIGN FILING LICENSE GRANTED ****
03/13/2015

Foreign Priority claimed	35 USC 119(a-d) conditions met	Verified and Acknowledged	Met after Allowance	STATE OR COUNTRY	SHEETS DRAWINGS	TOTAL CLAIMS	INDEPENDENT CLAIMS
☐ Yes ☑ No	☐ Yes ☑ No	/PAUL E PATTON/ Examiner's Signature	☐ PEP Initials	TAIWAN	6	11	1

ADDRESS
NORTH AMERICA INTELLECTUAL PROPERTY CORPORATION
P.O. BOX 506
MERRIFIELD, VA 22116
UNITED STATES

TITLE
SEMICONDUCTOR DEVICE WITH EPITAXIAL STRUCTURES

FILING FEE RECEIVED		
1600	FEES: Authority has been given in Paper No._____ to charge/credit DEPOSIT ACCOUNT No._____ for following:	☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit

BIB (Rev. 05/07).

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

27765 7590 03/14/2016

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Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission
I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

Bertha Chang	(Depositor's name)
/Bertha Chang/	(Signature)
04/08/2016	(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/637,412	03/04/2015	Chin-I Liao	NAUP1863USA3	5822

TITLE OF INVENTION:

SEMICONDUCTOR DEVICE WITH EPITAXIAL STRUCTURES

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	No	$960	$0	$0	$960	06/14/2016

EXAMINER	ART UNIT	CLASS-SUBCLASS
PATTON, PAUL E	2822	257-192000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
- ☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
- ☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) the names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 Winston Hsu
2 Scott Margo
3

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE: UNITED MICROELECTRONICS CORP.

(B) RESIDENCE: (CITY and STATE OR COUNTRY): No.3, Li-Hsin Road 2, Science-Based Industrial Park, Hsin-Chu City, Taiwan, R.O.C.

Please check the appropriate assignee category or categories (will not be printed on the patent) : ☐ Individual ☑ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:
- ☑ Issue Fee
- ☐ Publication Fee (No small entity discount permitted)
- ☐ Advance Order - # of Copies _____

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- ☐ A check is enclosed.
- ☐ Payment by credit card. Form PTO-2038 is attached.
- ☑ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number 50-3105 (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)
- ☐ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27.
- ☐ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature /Winston Hsu/ Date 04/07/2016

Typed or printed name Winston Hsu Registration No. 41526

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Electronic Patent Application Fee Transmittal

Application Number:	14637412
Filing Date:	04-Mar-2015
Title of Invention:	SEMICONDUCTOR DEVICE WITH EPITAXIAL STRUCTURES
First Named Inventor/Applicant Name:	Chin-I Liao
Filer:	Winston Hsu/Bertha Chang
Attorney Docket Number:	NAUP1863USA3

Filed as Large Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Utility Appl Issue Fee	1501	1	960	960

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Extension-of-Time:				
Miscellaneous:				
			Total in USD ($)	**960**

Electronic Acknowledgement Receipt	
EFS ID:	25433463
Application Number:	14637412
International Application Number:	
Confirmation Number:	5822
Title of Invention:	SEMICONDUCTOR DEVICE WITH EPITAXIAL STRUCTURES
First Named Inventor/Applicant Name:	Chin-I Liao
Customer Number:	27765
Filer:	Winston Hsu/Bertha Chang
Filer Authorized By:	Winston Hsu
Attorney Docket Number:	NAUP1863USA3
Receipt Date:	08-APR-2016
Filing Date:	04-MAR-2015
Time Stamp:	04:06:31
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	$960
RAM confirmation Number	7042
Deposit Account	503105
Authorized User	HSU, WINSTON
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: Charge any Additional Fees required under 37 CFR 1.16 (National application filing, search, and examination fees) Charge any Additional Fees required under 37 CFR 1.17 (Patent application and reexamination processing fees)	

Charge any Additional Fees required under 37 CFR 1.19 (Document supply fees)

Charge any Additional Fees required under 37 CFR 1.20 (Post Issuance fees)

Charge any Additional Fees required under 37 CFR 1.21 (Miscellaneous fees and charges)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Issue Fee Payment (PTO-85B)	NAUP1863USA3_AN_1_NP072.pdf	334797 ddb1fe3f4d6bff70c1fce096402d0ea8b0160e09	no	1
Warnings:					
Information:					
2	Fee Worksheet (SB06)	fee-info.pdf	30601 41ada9a9eb3efe3ad560762a36339a2493f866ab	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	365398		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

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APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/637,412	05/10/2016	9337193	NAUP1863USA3	5822

27765 7590 04/20/2016

NORTH AMERICA INTELLECTUAL PROPERTY CORPORATION
P.O. BOX 506
MERRIFIELD, VA 22116

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment is 0 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Data Management (ODM) at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site http://pair.uspto.gov for additional applicants):

Chin-I Liao, Tainan City, TAIWAN;
United Microelectronics Corp., Hsin-Chu City, TAIWAN;
Chun-Yu Chen, Taichung City, TAIWAN;

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