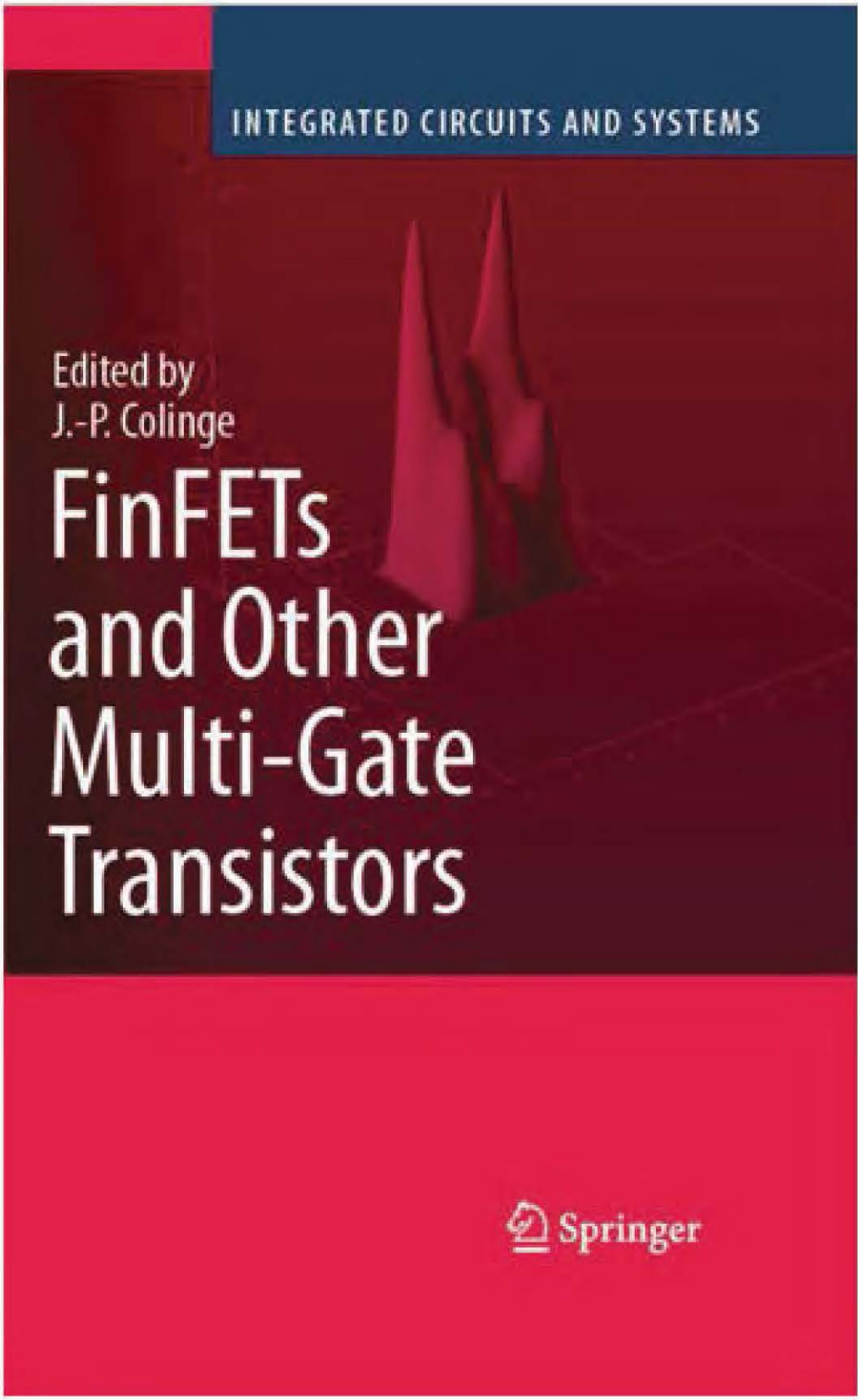


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Editor

FinFETs and Other Multi-Gate Transistors

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2 Multigate MOSFET Technology

Weize (Wade) Xiong

2.1 Introduction

Manufacturing a self-aligned double-gate MOSFET has been the holy grail of device engineers and researchers ever since it was proposed by Sekigawa and Hayashi in 1984.[1] The first modern self-aligned vertical multi-gate MOSFET was called DELTA (fully **DE**pleted **L**ean channel **T**r**A**nsistor).[2] This device was proposed by D. Hisamoto *et al.* in 1989. Figure 2.1 shows a cross section of the DELTA MOSFET.

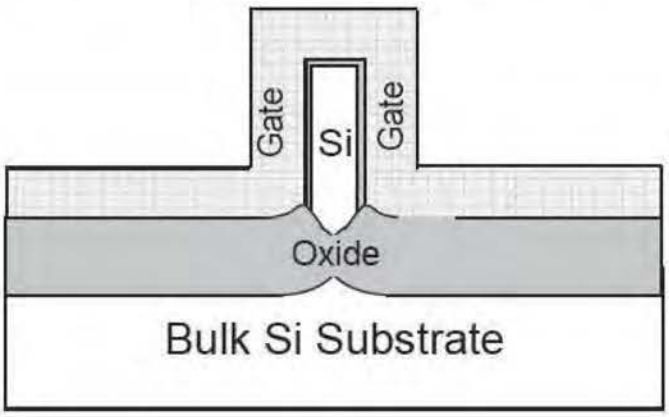


Fig. 2.1. DELTA MOSFET [1-2]. The oxide under the Si fin was formed through LOCOS oxidation while the Si fin was protected by the nitride hard mask and a nitride spacer prior to the oxidation process.

The two key features of the DELTA MOSFET are: 1) front and back MOSFET gates are inherently self-aligned and 2) the channels are on the sidewall of the silicon body/fin. The compatibility of the DELTA FET with existing planar CMOS processing is the main reason why it was

adopted as the mainstream multi-gate structure. FinFETs, Tri-gate and Π/Ω gate devices have all evolved from of this original concept [3-8].

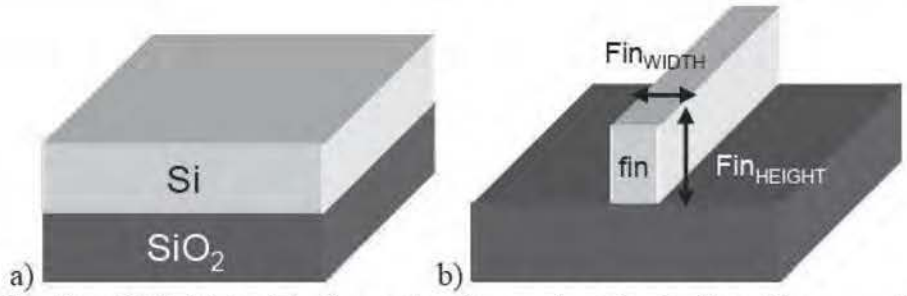
The critical fabrication steps in the front-end processing of a multi-gate MOSFET include, sequentially: 1) fin formation, 2) gate stack formation, 3) source and drain extension implant, 4) spacer formation, 5) epitaxial raised source/drain formation, and 6) deep source/drain implantation and activation anneal.

The fabrication flow of a Tri-gate MOSFET on an SOI substrate is shown in Figure 2.2. The SOI silicon top layer (T_{si}) thickness defines the fin height (Fin_{HEIGHT}). The fin pattern and the critical dimension of fin width (Fin_{WIDTH}) can be defined by optical lithography or by spacer image transfer (*SIT*) [9-10], followed by plasma etching.

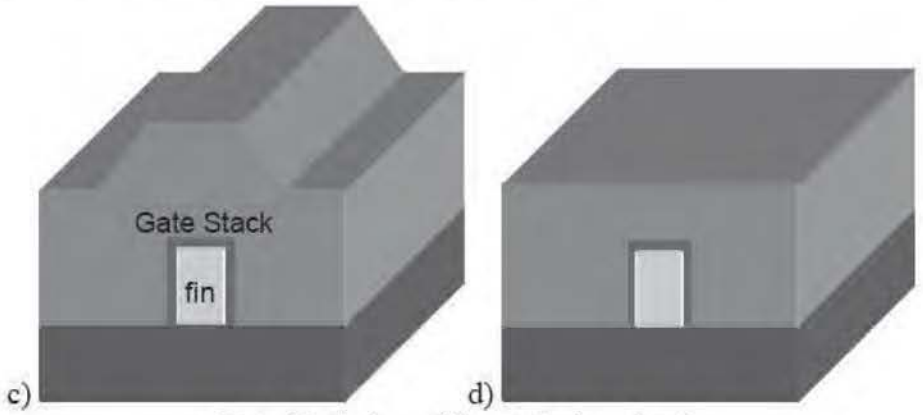
After fin etch, the fin sidewall surfaces are rough. Therefore, oxidation and H_2 annealing are often used to smooth the sidewalls.[11-12] Next, the gate dielectric is grown and metal gate is deposited. It is suitable to tune the threshold voltage (V_{th}) of the MOSFET by using a gate material that has the appropriate effective workfunction rather than by doping the channel. Sections 2.3, 2.5 and 2.6 will show that it is highly desirable to have intrinsic or lightly doped channels.

Since the gate stack is over the fin topography, a planarization step is desirable to flatten the gate surface, which reduces the burden on photolithography and gate etch. Significant overetch of the gate material is required to clear the bottom of the fins. As a result, the gate etch must have a high selectivity to the gate dielectric on top of the fin, if one wants to avoid damage to the fin during gate etch. Source and drain (S/D) extensions are formed after gate patterning using low-energy and large-tilt angled implants.[13-14] Next, S/D offset spacers are formed along the sidewalls of the gate and fin. The sidewall spacers on the fins are subsequently removed to expose the fin to grow raised source and drain using selective epitaxy.[13-15] The raised source and drain structure helps to reduce the parasitic resistance associated with thin fins.[13]

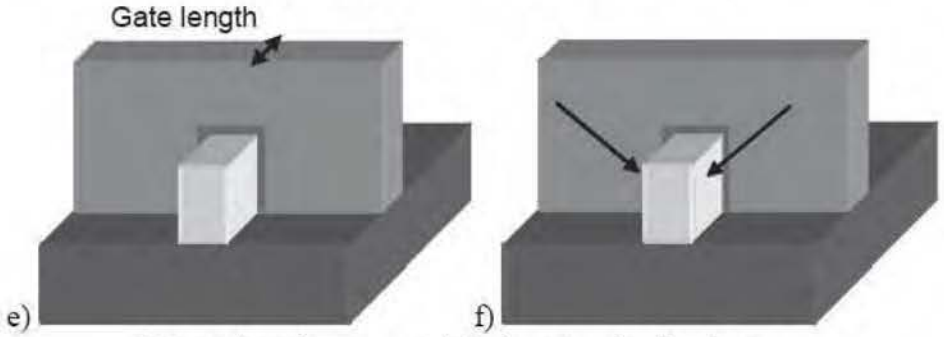
The rest of this chapter is divided into sections according to multi-gate device fabrication sequences. Section 2.2 covers fin formation, Section 2.3 describes gate stack structures, Section 2.4 describes source and drain formation and Section 2.5 highlights mobility and strain engineering.



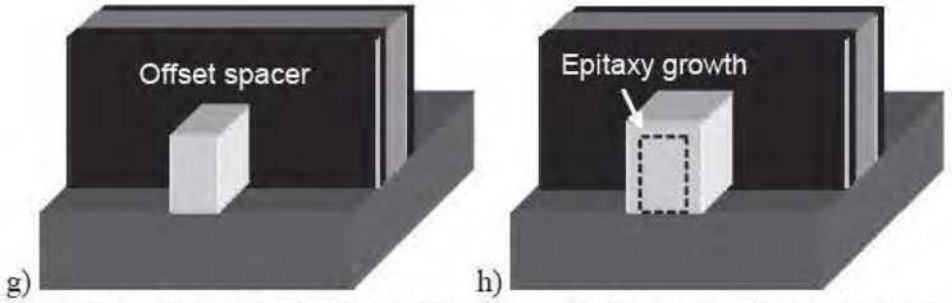
Starting SOI Material; fin patterning and etch. Define Fin_{WIDTH}; the fin height is the thickness of the silicon top SOI layer.



Gate Stack deposition and planarization



Gate etch and source and drain extension implant



Spacer formation and selective epitaxal growth. Removing the spacer on the sidewall of the fin while keeping the gate spacer is a critical step.

Fig. 2.2. General Fabrication Sequence of a Tri-gate MOSFET.

2.2 Active Area: Fins

2.2.1 Fin Width

As the MOSFET gate length, L_g, continues to shrink, year after year, the drain starts to compete with the gate electrode for control of the channel potential. The resulting "short-channel effects" (SCE) are: 1) higher sub-threshold leakage, 2) a threshold voltage (V_{th}) roll-off, and 3) a form of punch-through between the drain and source when V_{DS} is equal to the supply voltage.[16]

To reduce the drain influence in the channel, scaled planar bulk MOSFETs and PDSOI MOSFETs rely on: 1) gate oxide thickness reduction and 2) higher channel doping. The use of a thinner gate oxide increases the gate-to-channel capacitance. A higher channel doping concentration reduces charge sharing between the gate and drain in the channel, and it creates a large potential barrier between source and drain.

However, in modern MOSFETs, direct tunneling current through the gate dielectric prevents further scaling of the gate oxide thickness. The use of high channel doping concentrations reduces carrier mobility and increases Gate Induced Drain Leakage (GIDL).[17-18]

Another way to control SCEs is to use two or more gate electrodes and a thin, fully depleted semiconductor body. The idea is to create a large potential curvature in the source and drain direction by introducing a large electrical field gradient in the direction vertical to the gate. The key parameter in this approach is the thickness of the thin, fully depleted semiconductor body. In the case of the multi-gate technologies, the fin width is the thickness of the thin, fully depleted semiconductor body.

Chapter 1 introduced a powerful concept called natural length, λ, with:

$$\lambda = \sqrt{\frac{\varepsilon_{si}}{2\varepsilon_{ox}} t_{si} t_{ox}} \quad \text{for a double-gate MOSFET} \tag{2.1}$$

λ is a measure of the short-channel effect. It represents the distance of penetration of the drain electric field in the channel. A small value λ is desirable to minimize the SCE.

λ is proportional to the square root of the product of the device body thickness t_{si}, (or Fin_{WIDTH} in multi-gate technology) and gate oxide thickness t_{ox}. Thus, one can trade off t_{ox} scaling with Fin_{WIDTH} reduction. This approach is not possible for bulk or PDSOI MOSFETs.[17]

In a double-gate MOSFET, the center of the fin is the furthest away from the gate electrodes. Therefore, gate control is the weakest at this point. Should punchthrough occur, it would be in the center of the fin.[20] This implies using a slightly different boundary condition than Equation 2.1, which assumes the punch through is along the channel surfaces.

In this section, we will derive a new value for λ based on the assumption that punchthrough occurs in the center of the channel. The new λ has the same physical meaning as Equation 2.1, but it can better explain some of the experimental results shows later in this section. We will use the same coordinate system as in Figure 1.11. Starting with Poisson's equation, we can write:

$$\frac{d^2\Phi(x,y,z)}{dx^2}+\frac{d^2\Phi(x,y,z)}{dy^2}+\frac{d^2\Phi(x,y,x)}{dz^2}=\frac{qN_{sub}}{\varepsilon_{si}} \tag{2.2}$$

For single-gate or double-gate devices $\frac{d\phi}{dz}=0$, such that Equation 2.2 is reduced to:

$$\frac{d^2\Phi(x,y)}{dx^2}+\frac{d^2\Phi(x,y)}{dy^2}=\frac{qN_{sub}}{\varepsilon_{si}} \tag{2.3}$$

Assuming a parabolic potential distribution in the y-direction [21] we can write:

$$\Phi(x,y)\approx c_0(x)+c_1(x)y+c_2(x)y^2 \tag{2.4}$$

We now apply the boundary condition $\left.\frac{d\Phi(x,y)}{dy}\right|_{y=0}=0$ at $y=\frac{t_{si}}{2}$,

which yields:

$$\Phi(x,y)=\Phi_f(x)+\frac{\varepsilon_{ox}}{\varepsilon_{si}}\frac{\Phi_s(x)-\Phi_{gs}}{t_{ox}}y-\frac{1}{t_{si}}\frac{\varepsilon_{ox}}{\varepsilon_{si}}\frac{\Phi_s(x)-\Phi_{gs}}{t_{ox}}y^2 \tag{2.5}$$

where $\Phi_s(x)$ is the front- and back-surface potential and $\Phi_{gs} = V_{gs} - V_{FBF}$ is the front gate voltage V_{gs} minus the flat-band voltage, V_{FB}. Since the potential at the center of the fin, $\Phi_c(x)$, is the most relevant to SCE, we extract a relationship between $\Phi_c(x)$ and $\Phi_s(x)$ from 2.5 by substituting $y = \frac{t_{si}}{2}$ as follows:

$$\Phi_s(x) = \frac{1}{1 + \frac{\varepsilon_{ox}}{4\varepsilon_{si}} \frac{t_{si}}{t_{ox}}} \left(\Phi_c(x) + \frac{\varepsilon_{ox}}{4\varepsilon_{si}} \frac{t_{si}}{t_{ox}} \Phi_{gs} \right) \tag{2.6}$$

Expressing $\Phi(x, y)$ as a function of $\Phi_c(x)$ we obtain:

$$\Phi(x,y) = \left(1 + \frac{\varepsilon_{ox}}{\varepsilon_{si}} \frac{y}{t_{ox}} - \frac{\varepsilon_{ox}}{\varepsilon_{si}} \frac{y^2}{t_{ox} t_{si}} \right) \cdot \left(\frac{\Phi_c(x) + \frac{\varepsilon_{ox}}{4\varepsilon_{si}} \frac{t_{si}}{t_{ox}} \Phi_{gs}}{1 + \frac{\varepsilon_{ox}}{4\varepsilon_{si}} \frac{t_{si}}{t_{ox}}} \right) - \left(\frac{\varepsilon_{ox}}{\varepsilon_{si}} \frac{y}{t_{ox}} \Phi_{gs} - \frac{\varepsilon_{ox}}{\varepsilon_{si}} \frac{y^2}{t_{ox} t_{si}} \Phi_{gs} \right) \tag{2.7}$$

Substituting 2.7 back in 2.3 we get:

$$\frac{d^2 \Phi_c(x)}{dx^2} + \frac{\Phi_{gs} - \Phi_c(x)}{\lambda^2} = \frac{qN_A}{\varepsilon_{si}} \tag{2.8}$$

where natural length λ is now written:

$$\lambda = \sqrt{\frac{\varepsilon_{si}}{2\varepsilon_{ox}} \left(1 + \frac{\varepsilon_{ox}}{4\varepsilon_{si}} \frac{t_{si}}{t_{ox}} \right) t_{si} t_{ox}} \tag{2.9}$$

Numerical simulations in [17] show that for reasonable short-channel effect control, the gate length needs to be 5-10 times greater than λ.

We have established a theoretical relationship between L_g and λ. For a device designer, it would be more relevant to establish a guideline for the L_g to t_{si} ratio to control short-channel effects. Equation 2.9 does not separate the effects of t_{si} and t_{ox}. To walk around the problem, let us

assume a good SCE control can be achieved with $L_g = n\lambda$, where n is some arbitrary number. We now have:

$$\frac{L_g}{n} = \lambda = \sqrt{\frac{\varepsilon_{si}}{2\varepsilon_{ox}}\left(1+\frac{\varepsilon_{ox}}{4\varepsilon_{si}}\frac{t_{si}}{t_{ox}}\right)t_{si}t_{ox}} \tag{2.10}$$

In the limiting case when $L_g = 0$, we can write:

$$\frac{\varepsilon_{si}}{2\varepsilon_{ox}}\left(1+\frac{\varepsilon_{ox}}{4\varepsilon_{si}}\frac{t_{si}}{t_{ox}}\right)t_{si}t_{ox} = 0 \tag{2.11A}$$

which implies:

$$t_{si} = -4\frac{\varepsilon_{si}}{\varepsilon_{ox}}t_{ox} \tag{2.11B}$$

The right-hand term of Equation 2.11B represents the intercept point of the L_g *vs.* Fin_{WIDTH} plot for $L_g = 0$. Thus, one can define an effective fin width, $FinW_{eff}$, as:

$$FinW_{eff} = Fin_{WIDTH} + 4\frac{\varepsilon_{si}}{\varepsilon_{ox}}t_{ox} \tag{2.12}$$

Equation 2.12 shows that the impact of gate oxide can be considered equivalent to a constant offset of physical fin width. The validity of Equation 2.12 was demonstrated in reference [22]. Fig 2.3 shows contours of subthreshold swing on a L_g *vs.* Fin_{WIDTH} plot with 48 devices having 6 different Fin_{WIDTH} values and 8 different gate lengths. Each line represents a fixed short channel effect control. Since all devices have the same gate oxide (1.6nm oxynitride), they all intercept $L_g = 0$ at the same point. This point is approximately equal to $-4\frac{\varepsilon_{si}}{\varepsilon_{ox}}t_{ox}$.

Figure 2.4 shows the experimental double-gate FinFET results of $L_g/FinW_{eff}$ *vs.* subthreshold swing (or Subthreshold Slope, SS).[22] If we assume that a SS value of 90mV/dec is acceptable, then $L_g/FinW_{eff}$ is ~ 1.5. A triple-gate MOSFET with enhanced gate electrostatic control of the channel provides a lower L_g/Fin_{WIDTH} ratio than a double-gate FinFET for a same SCE control.[23] L_g/Fin_{WIDTH} as low as 1.0 was reported for Ω-Gate devices in [8]. *It is worthwhile noting that the minimum feature size in multi-gate technology is the fin width (Fin_{WIDTH}), and not the gate length.*

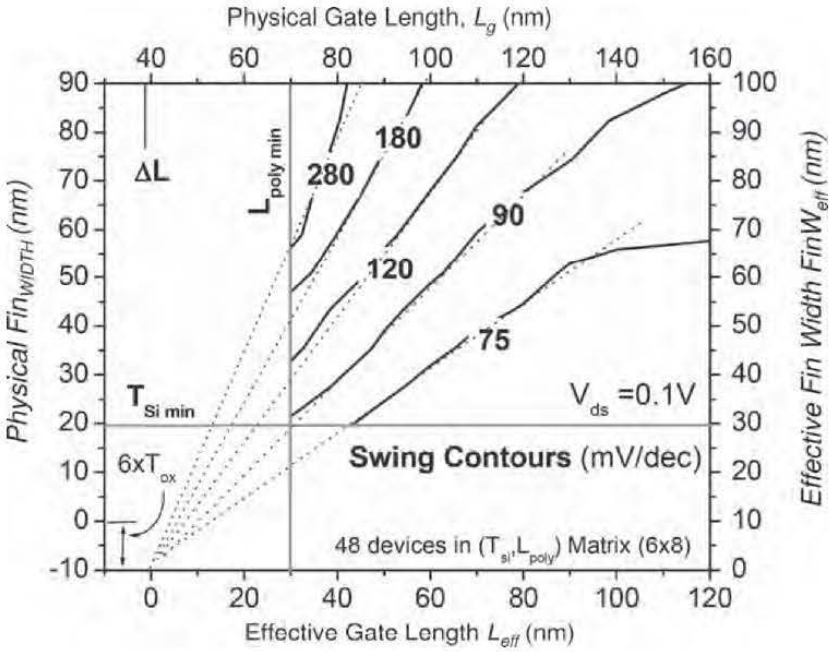


Fig. 2.3. Subthreshold swing contours for NMOS FinFET devices, V_d=0.1V. Fin_{WIDTH} varies from 20nm to 82.5nm in steps of 12.5nm, physical gate length; L_g varies from 70nm to 157.5nm in steps of 12.5nm. Contours are extrapolated with dotted lines to a common origin.[22] Copyright© 2001 IEEE.

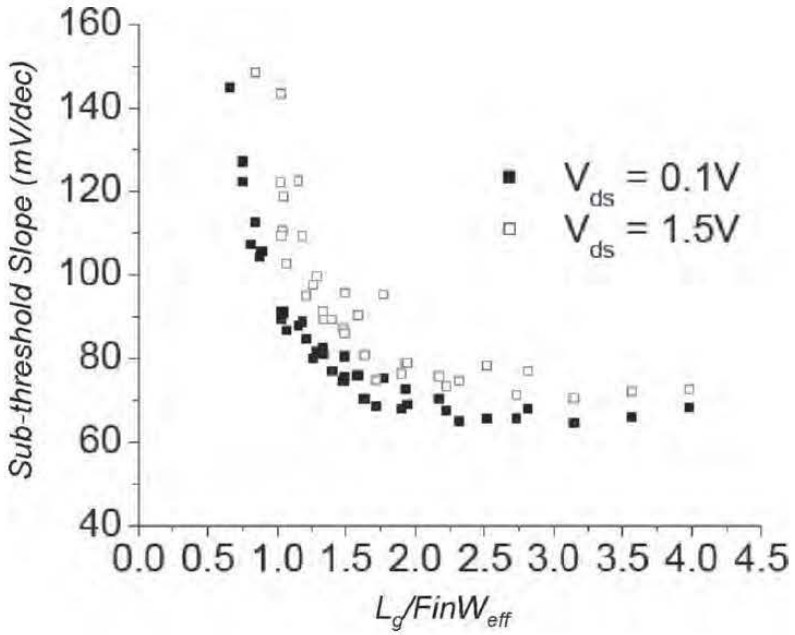


Fig. 2.4. Measured subthreshold swing *vs.* $L_g/FinW_{eff}$. Fin_{WIDTH} varies from 20nm to 90nm; L_g varies from 30nm to 120nm. The subthreshold slope is shown for both for V_d=0.1V and 1.5V.[22] Copyright© 2001 IEEE.

2.2.2 Fin Height and Fin Pitch

Having understood the requirements on Fin_{WIDTH} for SCE control, let us look at how fin pitch and fin height affect the drive current. For a double-gate FinFET, the channels are on the sidewalls of the fins. The effective channel width is thus equal to: [24]

$$W_{eff} = 2\,n\,Fin_{HEIGHT} \tag{2.13}$$

Where n is an integer number that is equal to the number of fins in a device. W_{eff} of multi-gate devices can only be increased or decreased by a discrete amount equal to $2\times Fin_{HEIGHT}$.[25]

The fin pitch, P_{FIN}, is the spacing between the fins plus the fin width. P_{FIN} is limited by the lithography pattern capability. Exactly one fin can be placed in one P_{FIN}. Therefore, the effective channel width per pitch is $2\times Fin_{HEIGHT}$. Figure 2.5 shows the layout comparison between a planar device and a FinFET. For the planar MOSFET, the effective device channel width, W_{eff}, is equal to the footprint on the substrate, W_{foot}. For FinFET, W_{eff} is related to W_{foot} through:

$$W_{eff} = 2Fin_{HEIGHT}\frac{W_{foot}}{P_{FIN}} \tag{2.14}$$

If we want the FinFET layout to be "competitive", we need $W_{eff} \geq W_{foot}$, or:

$$2Fin_{HEIGHT} \geq P_{FIN} \tag{2.15}$$

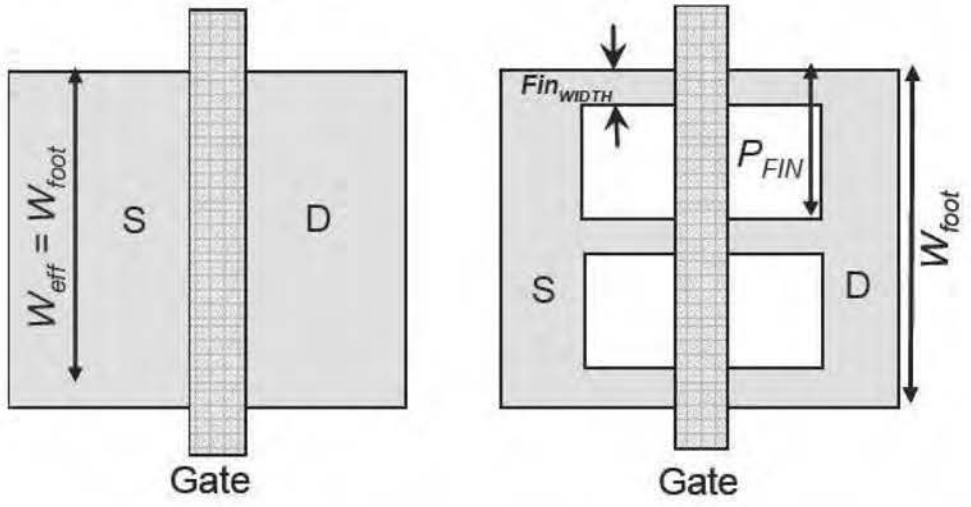


Fig. 2.5. Layout comparison between a planar MOSFET and a typical FinFET.

The analysis of the tri-gate channel width is further complicated by the "volume inversion" or "bulk inversion" effect reported in [26]. For thin fins, the inversion charge is not limited to the device surfaces. A large portion of the inversion charge is in the bulk of the fins, even at high gate voltages. Thus, without activating the top gate, multi-gate devices already have a significant charge at the top surface of the fins. Figure 2.6 shows the two-dimensional numerical simulation of carrier density on the top surface of 1) a tri-gate, 2) a double-gate and 3) a FinFET with a hard mask on top of the fin.

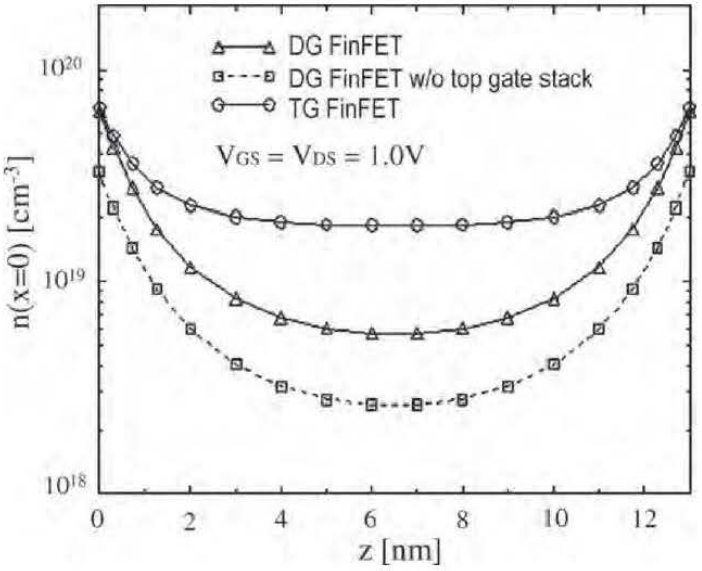


Fig. 2.6. Davinci prediction of on-state electron density along the top fin surface at the center of the channel (x =1/2 L_{eff}). DG stands for double gate. TG stands for tri-gate. Due to bulk inversion, the electron density on the top fin surface for DG FinFET is comparable to that in the TG device [26]. Copyright© 2005 IEEE.

Due to this "bulk inversion", the effective width, ΔW_{eff}, of the top gate in a tri-gate MOSFET is only a fraction of the physical top gate width. Numerical simulation in [26] shows ΔW_{eff} is a function of fin height and fin width.

For tri-gate devices, Equation 2.12 becomes: $2Fin_{HEIGHT} + \Delta W_{eff} \geq P_{FIN}$

Fins can be defined by conventional photolithography and reactive ion etch. Fins with width less than 20nm have been reported with 193nm dry photolithography processing.[27-28] Figure 2.7 shows the TEM cross section of some of these fins.[27-31] Continuing advances in lithography pitch and line dimension, including emerging 193nm photolithography and Extreme UV (EUV) lithography pave the way for further Fin_{WIDTH} and P_{FIN} reduction.

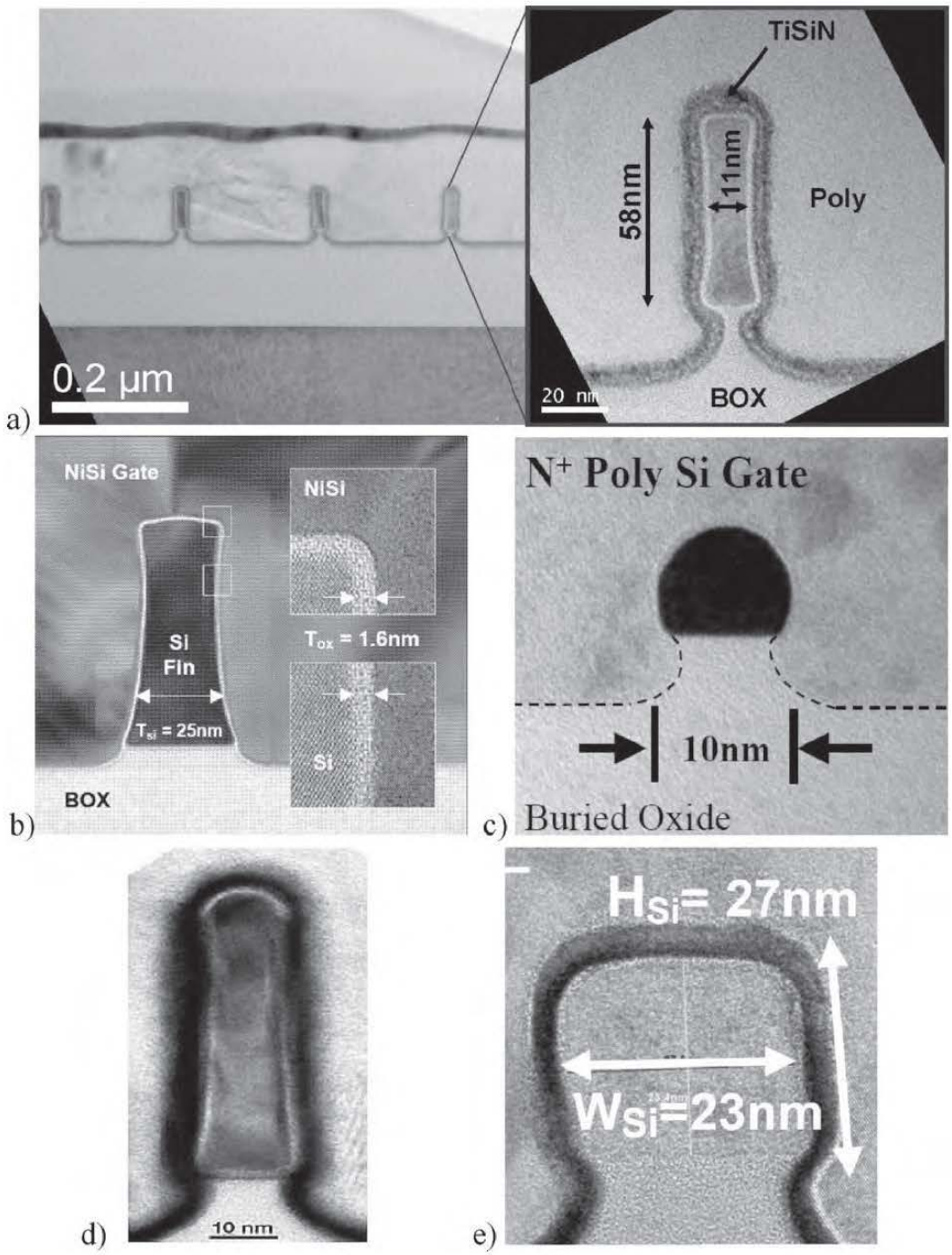


Fig. 2.7. Cross-sectional TEM of fins under gates. a) [27] Copyright© 2006 IEEE, b) [28] Copyright© 2002 IEEE, c) [29] Copyright© 2004 IEEE, d) [30] Copyright© 2005 IEEE, e) [31] Copyright© 2006 IEEE.

To increase the current drive per unit W_{foot}, we can increase Fin_{HEIGHT}, or reduce P_{FIN}. Both options have practical limitations. Increasing Fin_{HEIGHT} undermines the fin stability and increases the difficulty of gate patterning.

P_{FIN} is limited by the optical lithography capability. In order to improve P_{FIN} beyond optical lithography capability, spacer-defined fin patterning has been proposed.[32] Figure 2.8 shows the general concept. First a sacrificial pattern is defined with conventional optical lithography. Then spacers are formed on the sidewalls of the sacrificial pattern through thin film deposition and anisotropic reactive ion etch (RIE). The sacrificial pattern is subsequently selectively removed leaving the remaining spacers to serve as hard mask for fin etch.

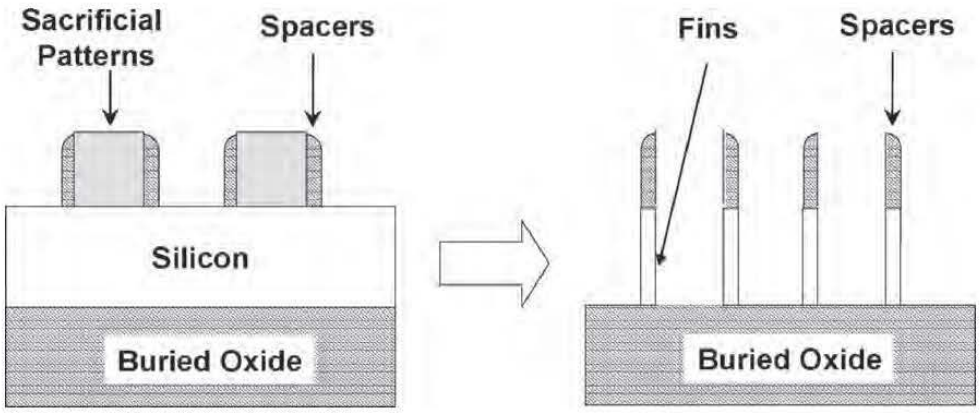


Fig. 2.8. Illustration of a spacer-defined fin formation process.

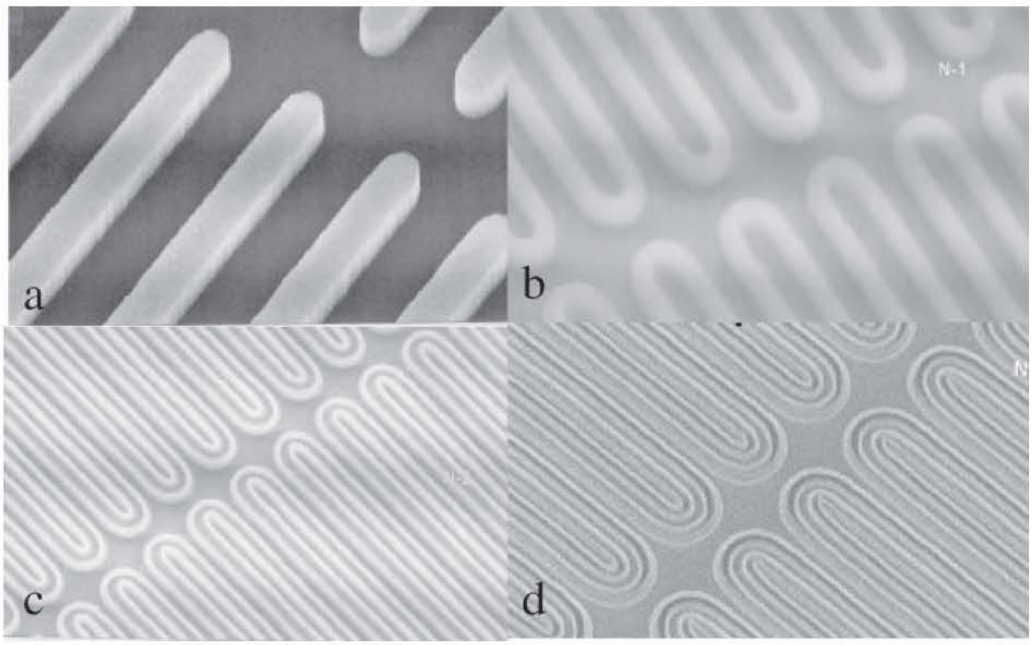


Fig. 2.9. SEM pictures of three progressive spacer-defined fin formation processes. a) initial optical lithography of sacrificial pattern. b) after first spacer imaging; c) after second spacer imaging; and d) after third spacer imaging. The final pattern pitch is 6 times smaller than the optical lithography pitch. REPRINTED WITH PERMISSION FROM [33]. COPYRIGHT 2003 AMERICAN INSTITUTE OF PHYSICS.

There are two advantages to spacer-defined fin formation. First, it doubles the number of fins for a given lithography pitch, *i.e.*: it reduces the fin pitch to half of the lithography pitch. In fact, when the spacer process is used twice, the pitch can be reduced by a factor of four. Figure 2.9 shows the SEM images of spacer imaging technique progressively being used three times.[33] Second, the fin width is defined by the thickness of deposited film, which has the potential to 1) be narrower than a lithography-defined fin, 2) have better CD control and 3) have reduced line-edge roughness.[32] The disadvantage of spacer-defined fin is that a clean-up mask is required to remove the fins where designers do not want them.[25] CMOS FinFET devices have been successfully fabricated using this imaging technique. Successful conversion of a planar microprocessor design into a spacer-defined FinFET microprocessor was also demonstrated in [25].

2.2.3 Fin Surface Crystal Orientation

Electrons and holes mobility depends on the orientation of the silicon surface as well as on the current flow direction.[34-36] Figure 2.10 shows the measured surface mobility of electrons and holes as a function of the inversion layer charge density.[37] For electrons, the highest mobility surface is (100) and the lowest mobility surface is (110). For holes, the (110) surface has the highest mobility and the (100) surface has the lowest mobility. Electrons and holes at a (111) surface have mobilities laying somewhere between those at (100) and (110) surfaces. The origins of the above differences are due to the anisotropy of effective mass and surface scattering.[35,36]

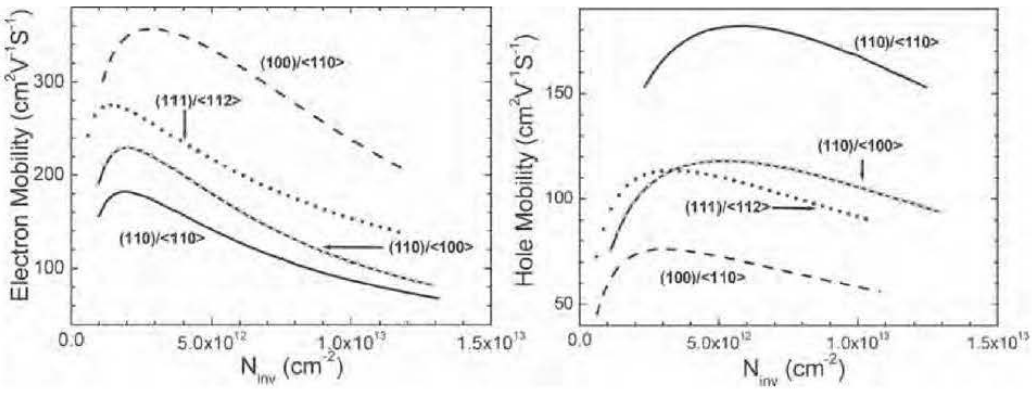


Fig. 2.10. Effective surface mobility of electrons and holes as a function of inversion layer charge density, for different surface orientations.[37] Copyright© 2003 IEEE.

Multi-gate MOSFETs have been fabricated on all 3 major Si surfaces [27,32,19]. The directions of the current flow for the respective surfaces are <100> for (100), <110> for (110) and <112> for (111). (110) Fin sidewall surfaces are made by patterning fins at 0 or 90 degrees with respect to the <110> notch on silicon wafers with a (001) surface orientation. This layout style is the same as for conventional planar devices. (100) fin surfaces are made by rotating the fin layout by a 45 degree angle with respect to the <110> notch direction. Figure 2.11 shows the layout directions of (100) fin surfaces and (110) fin surfaces.[38] Alternately, the Si top layer of the SOI wafers can be rotated by a 45 degree angle with respect to the substrate during bonding, to have the (100) surface fin layout at 0 and 90 degrees and the (110) surface at a 45 degree rotation.[39]

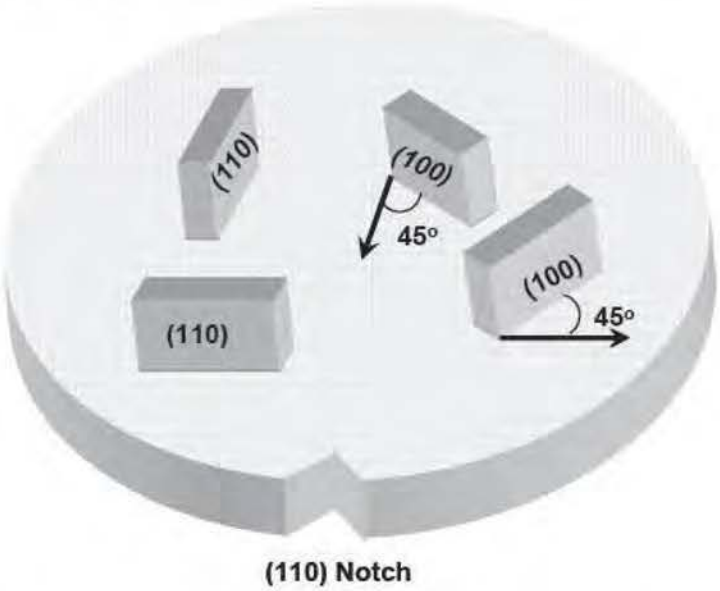


Fig. 2.11. Fins with (110)/<110> and (100)/<100> surfaces/directions can be readily made using standard Si substrate by rotating the fin layout by 45 degrees.

Having fins with both (110) and (100) surface orientation on the same chip allows one to optimize electron (NMOS) and hole (PMOS) mobility simultaneously. The price to pay for such devices is an increased layout area [41] and a higher photolithography process complexity. Optimizing optical lithography lines at 0, 90 and 45 degree angles is challenging. Figure 2.12 shows the comparison of a 6-transistor SRAM cell layout containing both (110) and (100) fins directions (mixed layout) with a standard layout with only one fin orientation. The mixed layout results in a 16.6% larger cell area.[41]

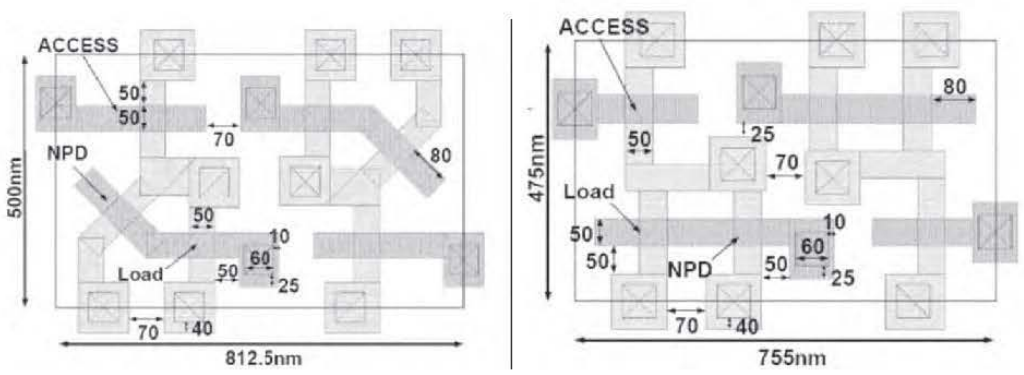


Fig. 2.12. 6-transistor SRAM cell layout comparison: standard layout (right) and layout with NMOS pull-down transistors rotated by 45 degrees (left).[41] Copyright© 2005 IEEE.

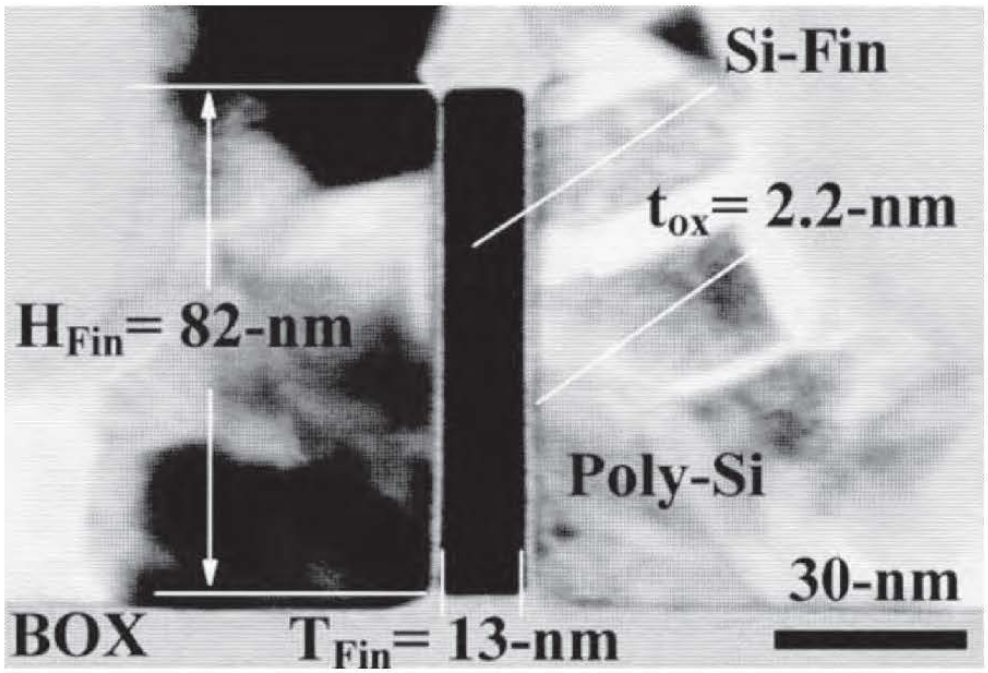


Fig. 2.13. Cross-sectional TEM of a (111)-surface sidewall fin. The smooth rectangular shaped fins were formed using surface-orientation dependent wet etch chemistry.[19] Copyright© 2003 IEEE.

The formation of (111) surface fins on (110) surface SOI substrates has been demonstrated.[19,42] In this experiment, fin patterns were aligned parallel to the <112> direction. The advantage of the (111) surface fins is that very smooth and straight fins can be formed by a wet etch process. The (111) surface silicon has an extremely low etch rate in tetramethylammonium hydroxide (TMAH) solution, compared with other crystallographic planes. The etch rate ration at 50°C for (110) planes

versus (111) planes is 20:1. Thus, after initial plasma fin etch, an additional wet etch in TMAH can ensure very straight and smooth (111)-surface fins. Figure 2.13 shows the TEM of a smooth and vertical (111)-sidewall surface fin. One can appreciate the nearly perfect rectangular shape of the fin. The smoothness of the (111) surface fin using surface orientation dependent wet etch chemistry is very attractive. However, the drawback of this technique is that (111) surface carriers mobility is rather low. Furthermore, the mobility enhancement with strain engineering is not currently as well characterized on (111) as on the other two surfaces. Strain engineering will be further discussed in Section 2.5.

2.2.4 Fin Surface Preparation

The fin surfaces exhibit significant roughness right after plasma etch. In addition, the fin corners are sharp. Gate oxide grown on these surfaces is prone to defects and localized thinning. Without proper treatments, silicon crystal defects such as twin formation in the fin corners could happen.[40] Sharp corners also result in a kink in the subthreshold region if the fin doping level is high.[43] Such kinks are caused by parasitic corner devices, which have a lower threshold voltage than the sidewalls due to the higher electrical field in the corners. The fin corner problem is similar to the parasitic STI edge device effect that can be found in planar CMOS technologies.

Carrier mobility along the fin sidewalls without treatment is rather poor.[44] The simplest way to repair surface roughness and damage from the plasma etch is through oxidation. The requirement for fin sidewall smoothing oxidation is similar to STI liner oxidation. It is desirable to have conformal oxidation with a growth rate that is insensitive to the fin surface orientation. In-Situ-Steam-Generated (ISSG) rapid thermal oxidation has such desired properties.[45-46]. ISSG typically uses pressure above 5 Torr. Hydrogen and oxygen are introduced simultaneously into the chamber. The reactants remain as free species (O_2 and H_2) until they reach the wafer surface, where heat induces a local reaction. O_2 and H_2 react to form steam and oxygen radicals. The unstable oxygen radicals promote further oxidation. As a result, the oxidation is conformal and has no surface orientation preference. In addition, ISSG has the advantage of being insensitive to the doping level in the silicon and it provides better corner rounding than conventional oxidation.

The sacrificial smoothing oxide is typically removed using a hydro-fluoride (HF)-based isotropic wet etch step.[40] Some of the buried oxide

in the SOI substrate is etched at the same time as the sacrificial oxide. As a result, buried oxide recesses below the bottom fin surface and creates the Π/Ω-shaped gate (See Fig. 2.8a). Π/Ω-Gate MOSFETs take advantage of such buried oxide recess to improve the gate electro-static control of the channel.[7-8] However, such a recess can undermine the fin stability if the fin width is scaled below 10nm.

H_2 annealing is another way to smooth the fin surfaces and round the corners. H_2 annealing has been shown to: 1) improve electron mobility, 2) reduce gate leakage and 3) lower 1/f noise.[11,12,47] The H_2 annealing process conditions have a great impact on the final shape of the fins. If the temperature is too high and/or the pressure is too low, the Si fins can agglomerate and break. The narrower the fins, the more sensitive they are to the H_2 annealing conditions.

2.2.5 Fins on Bulk Silicon

The fins we described so far are fabricated on SOI wafers. MuGFETs can also be made on bulk silicon wafers.[48-53] In some references they are called body-tied FinFETs or bulk FinFETs. The main advantages of using bulk silicon over SOI substrates are 1) lower wafer cost and 2) better substrate heat transfer rate. However, bulk multi-gate MOSFET require additional isolation steps, which increase the cycle time and cost. Furthermore, the fin height of bulk-based multi-gate devices are entirely determined by the fin etch step. This puts more pressure on etch variation control, since any fin height variation translates into transistor width variation.

The control of the electrical potential by the gate in bulk fins is as good as in their SOI counterparts. But underneath the fin, in bulk devices, the source and drain have to be separated by heavy channel stop implants to prevent sub-surface punchthrough. As a result, multi-gate devices made on bulk silicon suffer from higher source and drain diode leakage and higher junction capacitance than devices made in SOI.

The bulk silicon under the fin can be accessed by a body contact. But the body factor of a bulk FinFET is very low, since the electrostatic potential inside the fins is dominated by the gate, not by the body. Therefore, body bias is not effective in changing the threshold voltage of a bulk multi-gate MOSFET. Figure 2.14 illustrates the general fabrication process of a bulk MuGFET.

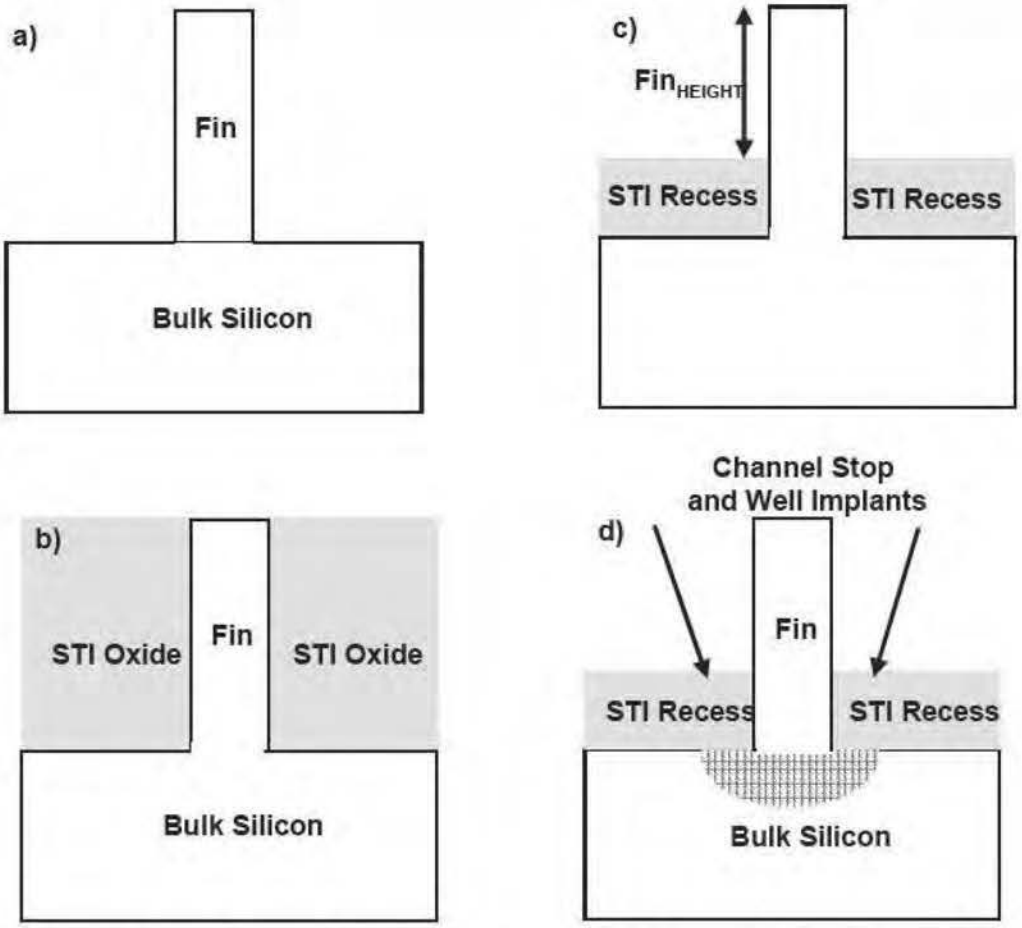


Fig. 2.14. General process flow for making a FinFET on a bulk silicon bulk wafer. a) Fin etched in bulk silicon, the initial Fin_{HEIGHT} is greater than final device Fin_{HEIGHT} to allow some STI (Shallow trench Isolation) oxide. b) STI oxide deposition and planarization. c) STI oxide recess to expose silicon fin with desired FinHEIGHT. d) Channel stop and Well implants. Channel stop is needed to prevent the source and drain punch through below the fin in the bulk silicon.

2.2.6 Nano-wires and Self-Assembled Wires

The ultimate MOSFET structure is a cylindrical wire-like gate all-around device, as show in Figure 2.15. This structure provides the best electrostatic control of the channel by the gate [54]. The natural length, λ, for such a device is given by Equation 2.16.

$$\lambda = \sqrt{\frac{2\varepsilon_{si} t_{si}^{\,2} \ln(1+\frac{2t_{ox}}{t_{si}}) + \varepsilon_{ox} t_{si}^{\,2}}{16\varepsilon_{ox}}} \tag{2.16}$$

where t_{si} is the diameter of the wire. To keep short-channel effects under control, t_{si} shrinks with gate length. When t_{si} is below 10nm, the device structure is typically called a "nanowire MOSFET".

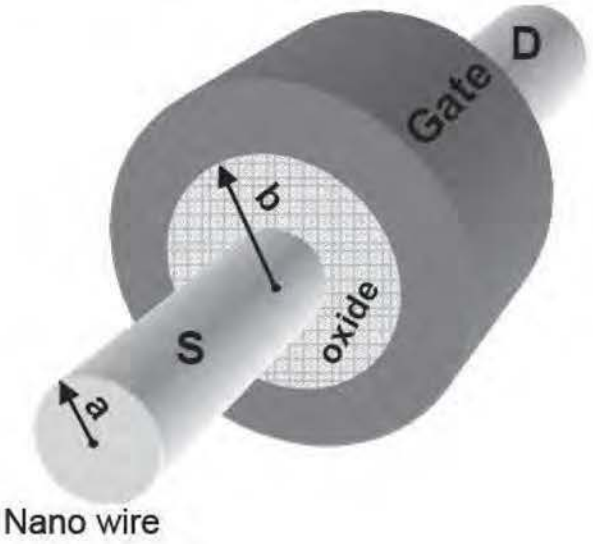


Fig. 2.15. Illustration of a silicon nanowire transistor. The gate stack is wrapped around the semiconductor nanowire. a is the radius of the nanowire.

Because the nanowire transistor has a cylindrical cross section, its capacitance can no longer be calculated using a simple parallel-plate model. Considering Figure 2.15, the inversion charge in the nanowire can be approximated by a charge sheet on the outer surface of the wire. The charge on the gate is on the inner wall of the gate electrode. The capacitance can be obtained by calculating the voltage drop across the gate oxide. Applying Gauss's law to an infinitely long cylinder one can find the electrical field outside the cylindrical wire:

$$E = \frac{Q}{2\pi\varepsilon_{ox} r} \tag{2.17}$$

Where Q is the charge per unit length at the surface of the wire, and r is the radius of the wire. The voltage drop across the gate oxide can be found by integrating the electrical field along a radial line:

$$\Delta V = \frac{Q}{2\pi\varepsilon_0 r}\int_a^b \frac{1}{r}dr = \frac{Q}{2\pi\varepsilon_{ox} r}\ln(\frac{b}{a}) \tag{2.18}$$

where a is the nanowire radius, and $b = a+t_{ox}$. The capacitance per unit gate length is:

$$\frac{C}{L_g} = \frac{Q}{\Delta V} = \frac{2\pi\varepsilon_{ox}}{\ln(\frac{b}{a})} \tag{2.19}$$

Converting Equation 2.19 to a capacitance per unit area of the nanowire surface, we obtain:

$$\frac{C}{A} = \frac{2\pi\varepsilon_{ox}}{\pi a \ln(\frac{b}{a})} = \frac{2\varepsilon_{ox}}{a \ln(\frac{b}{a})} \tag{2.20}$$

Equation 2.20 indicates the effective gate capacitance of the nanowire transistor is a function of the nanowire radius as well as the gate oxide thickness. This relationship can be exploited to reduce the effective gate oxide thickness without using higher k dielectric. As an example, a nanowire MOSFET with a=4nm, t_{ox} = 2nm, the effective gate oxide thickness is 1.62nm. The above calculation does not take bulk inversion or quantum-induced volume inversion effects into account. In those cases, the effective nanowire radius is decreased, since the charges are not limited to the nanowire surface.

Silicon nanowires can be made with conventional patterning described in section 2.2.2. A circular cross section can be made by first removing the buried oxide below the silicon, and then rounding of the wires to an approximately circular cross section can be achieved using H_2 annealing.[29]

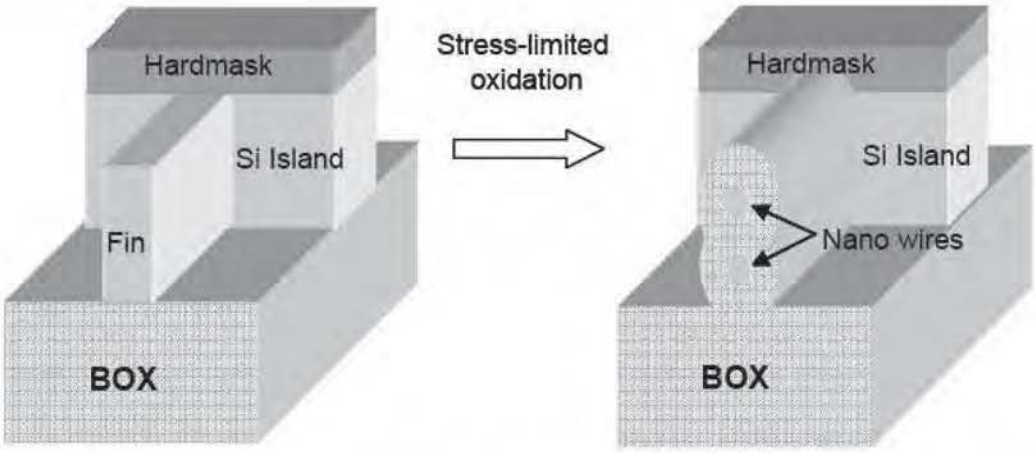


Fig. 2.16: Twin Si nanowires formed through stress-limited oxidation. A hard mask is needed to keep the Si island region from oxidizing. The presence of Si island at the end of the wires is needed to anchor the wires.

A twin-wire structure has been made using stress-limited oxidation of tall fins. The stress-limited oxidation oxidizes the wire slower than planar silicon, which produces a final structure comprising two Si wires, one on the top of the fin, and the one other at the bottom of the fin (Figure 2.16). It is important to protect the source and drain region during the oxidation. After removing the oxide, two silicon wires are formed.[55] Twin nanowires can also be formed by oxidation using doping-dependent oxidation rate effects.[126]

The formation of high-density, self-assembled nanowires has been demonstrated using cylindrical-phase diblock copolymers.[56] The polymer has the ability to divide a lithographic pattern (W) into integer number of sub-unit with a distance, l, between cylinders. l is intrinsic length of the polymer which determine the number of sub-units (n) fits in W. The relationship between n and l is defined by Equation 2.21.

$$n = \frac{2}{\sqrt{3}}\left(\frac{W}{l}\right) \tag{2.21}$$

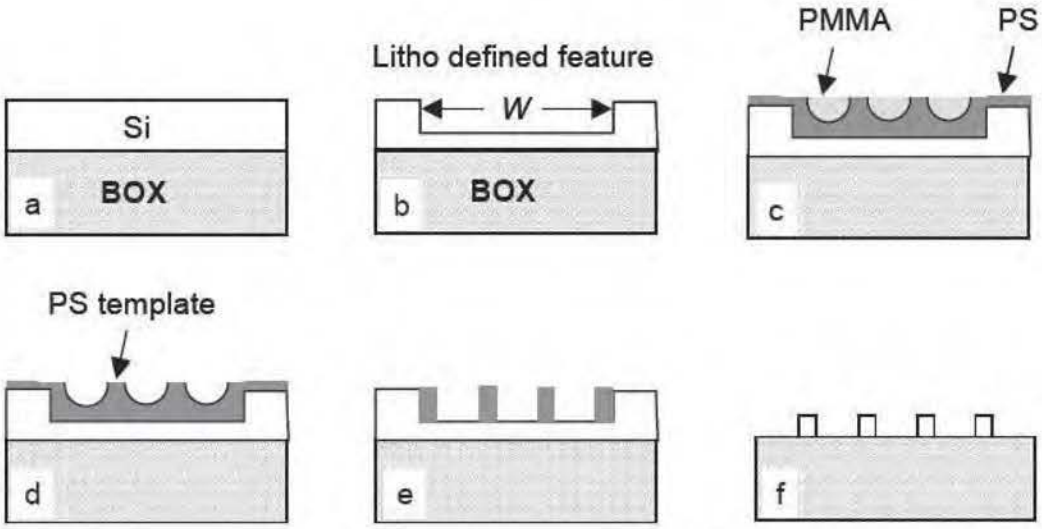


Fig. 2.17: Self-assembled nanowire formation. The initial lithothography-defined pattern on an SOI wafer (a,b) is divided into self-aligned patterns by cylindrical-phase diblock copolymers (c). d) PS template formation for plasma etching (e). The remaining PS features are used as mask to etch the silicon nanowires (f).

The self-assembly process is illustrated in Figure 2.17. The sidewalls of the lithography-defined trench initiate the assembly of the polymer domain. In Reference 56, diblock copolymers composed of 70% polystyrene (PS) and 30% poly (methyl-methacrylate) (PMMA) (70:30 PS:PMMA) with total molecular weight Mn=64 kg/mol are shown to form

hexagonal lattices of 20 nm diameter cylindrical PMMA domains (l =35 nm) in a matrix of PS. After film assembly, PMMA is removed from the half-cylinder domains by immersing the substrate in acetic acid. Plasma etch is then used to define the Si nanowires.

2.3 Gate Stack

2.3.1 Gate Patterning

This section presents the process steps used in the gate formation of a multi-gate MOSFET. The topography created by the fins presents many challenges. One of these challenges is illustrated in Figure 2.18: photoresist has a surface planarization effect when deposited on a non-planar topography. The wavy gate material stepping over the fins results in different photoresist thickness along the width of the transistor. The photoresist critical dimension (CD) after exposure is a function of the resist thickness. This effect is known as "swing curves". Without gate planarization, gate CD will vary periodically through the entire width of the device, with a period equal to the fin pitch (Figure 2.18). Therefore, the use of a planarized gate is highly desirable.

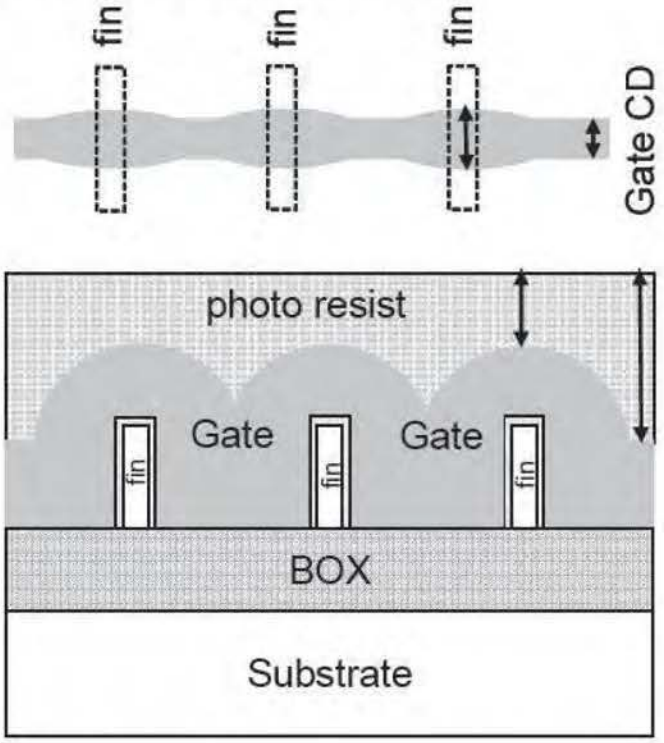


Fig. 2.18. Patterning gate on an irregular topography results in wavy gate CD due to the variation in resist thickness. A planarization step is required.

The gate etching process must also be adjusted to account for the fin topography. Gate etch first reaches the fin top surface, then over-etch is required to clear all of the gate material between the fins. The overetch must be selective to the gate dielectric material for tri-gate type devices. A hard mask on top of the fin can help to protect the fins from gate etch. Additional isotropic etch is required for Ω-gate devices in order to clear the gate material in the undercut region of the fin (Figure 2.19).

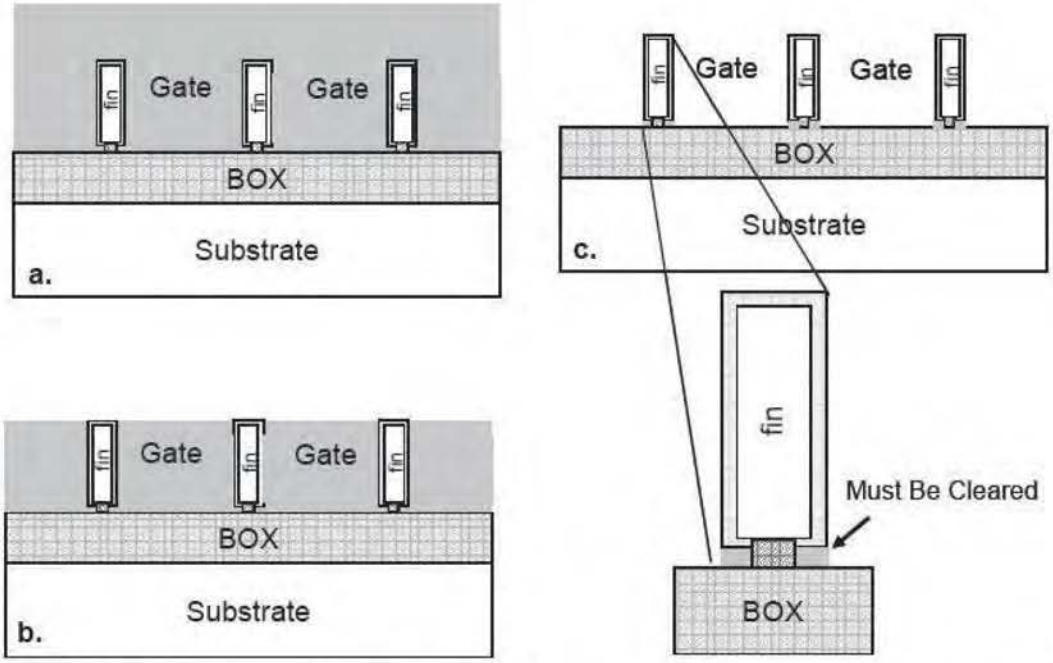


Fig. 2.19. The key aspects of the gate etch are the ability to etch the gate material between the fins without damaging the fin (a,b), the removal of the gate material in the undercut region between the fin and buried oxide (c).

2.3.2 Threshold Voltage and Gate Workfunction Requirements

The threshold voltage of a long-channel MOSFET, V_t, is classically is defined by Equation 2.22.[57]

$$V_t = \phi_{ms} + 2\phi_f + \frac{Q_D}{C_{ox}} - \frac{Q_{ss}}{C_{ox}} \tag{2.22}$$

where Q_{ss} represents the charges in the gate dielectric, C_{ox} is the gate capacitance, Φ_{ms} is the workfunction difference between the semiconductor and the gate electrode, Φ_f is the difference between the semiconductor Fermi level E_F and the intrinsic semiconductor Fermi level

E_{Fi}, and Φ_f is the Fermi potential, given by Equation 2.23 for P-type silicon:

$$\phi_f = \frac{kT}{q}\ln(\frac{N_a}{n_i}) \tag{2.23}$$

In a planar bulk MOSFET, strong inversion occurs when the band bending (surface potential) at the semiconductor surface reaches $2\Phi_f$. Q_D is the depletion charge in the channel. In a fully depleted double-gate MOSFET Q_D is given by Equation 2.24.

$$Q_D = q\frac{1}{2}Fin_{WIDTH}N_a \tag{2.24}$$

Let us now examine if this V_t definition is applicable to ultra-thin body devices. Let us assume a metal gate electrode with a workfunction equal to the middle of the band gap of the silicon. The silicon body is doped p-type with N_a=2x10^{15}/cm^3. The fin cross section is 11nm x 60nm and the gate dielectric is 1.8nm-thick SiO_2. Let us also keep in mind that for 11nm fin width quantum effects on V_t are negligible. The Fermi potential, Φ_f, can be calculated by Equation 2.23 and is equal to 0.33V at room temperature. Since the gate material has a midgap workfunction Φ_{ms} = - Φ_f and Equation 2.22 becomes:

$$V_t = \phi_f + \frac{Q_D}{C_{ox}} - \frac{Q_{ss}}{C_{ox}} \tag{2.25}$$

Considering the width of the fin, the total depletion charge Q_D contributes 0.05mV to Equation 2.25. If the gate dielectric charge Q_{ss} is under 1x10^{12}/cm^2, the contribution to Equation 2.25 is less than a few μV. Thus, V_t from Q_D and Q_{ss} is negligible compared to Φ_f. We can conclude that V_t in our example should be equal to 0.33V. But this is 0.12V less than experimentally observed using maximum g_m method in reference [58].

This discrepancy is due to the estimation of the surface potential at the threshold of inversion in thin-body devices. For undoped ultra-thin body devices, the availability of inversion charges is quite limited when the surface potential is at $2\Phi_f$. The surface potential at the onset strong inversion (and thus at threshold) is higher than $2\Phi_f$. Therefore, Equation 2.22 needs to be modified:

$$V_t = \phi_{ms} + 2\phi_f + \frac{Q_D}{C_{ox}} - \frac{Q_{ss}}{C_{ox}} + V_{inv} \tag{2.26}$$

where V_{inv} represents the additional surface potential to $2\Phi_f$ that is needed to bring enough inversion charge into the channel for the transistor to reach threshold. Several publications tackle the issue of modeling V_{inv}. V_{inv} is a function of fin width and doping concentration. The narrower the fin and the lower the doping level, the higher the value of V_{inv}. The use of wide fins and higher doping concentration reduces V_{inv} and brings Equation 2.26 closer to Equation 2.22.[58-60]

The contribution of the depletion charge Q_D to the threshold voltage is negligible unless the doping concentration is very high. Therefore, the threshold voltage of a MuGFET is primarily determined by the effective workfunction of the gate stack (the workfunction of the gate electrode and the charges in the gate dielectric or at the interfaces). Figure 2.20 shows the required gate stack workfunction for various devices.

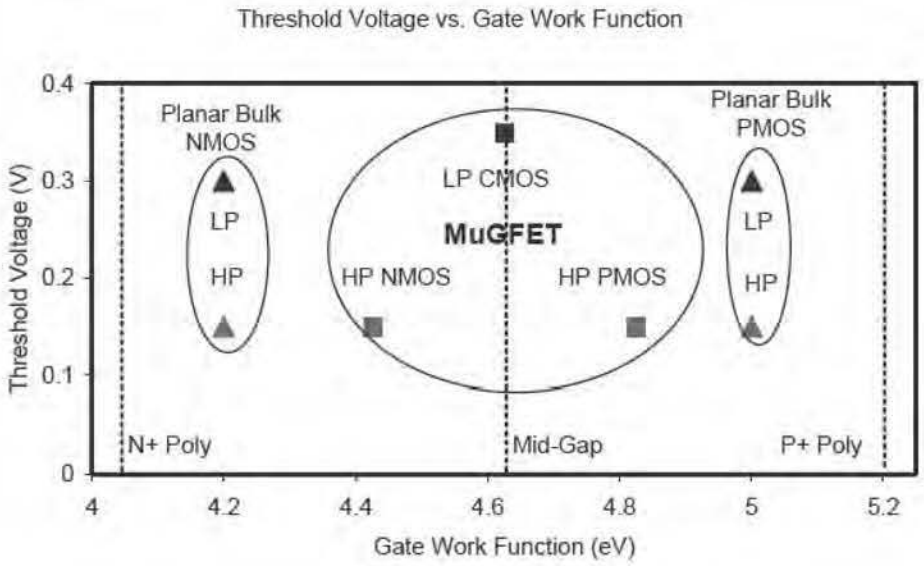


Fig. 2.20. Gate workfunctions for different device types. High Performance (HP) and Low Power (LP) planar bulk MOSFETs need workfunctions close to the silicon band edges, while HP and LP multi-gate MOSFETs need workfunction values close to the midgap of the silicon.

For high-performance CMOS, where low threshold voltages are desired, a two-workfunction metal gate system is required. For n-channel FETs, the workfunction needs to be ~200mV below the midgap of the silicon. For p-channel devices, the workfunction needs to be ~200mV above the

midgap of silicon. In low-power CMOS, a single midgap metal gate system can be used to obtain a symmetrical threshold voltage for n-channel and p-channel devices at approximately ±350mV.[58]

2.3.2.1 Polysilicon Gate

Heavily doped polysilicon gates have an effective workfunction close to the band edges. For depletion-mode operation, if N^+ poly is used for the NMOS devices, V_t is less than zero, and if P^+ poly is used for PMOS devices, their V_t is greater than zero. These values are not suitable for standard digital applications.

To obtain more acceptable threshold voltage values, attempts have been made to place an N^+ poly gate on one side of the fin and a P^+ poly gate on the other side.[22,62] The resulting device is commonly referred to as an asymmetrical double-gate FinFET. Figure 2.21 illustrates the process used to make an N^+/P^+ poly-gate FinFET. Two high-tilt-angle gate implants were used to dope the gate on one side of the fin N^+ and the other side P^+. This process requires a thin polysilicon gate and tall fins so that an implant "shadow" effect can be used to prevent sidewall gates from receiving both implants. The threshold voltages observed experimentally in [22] are 0.15V for NMOS transistor sand -0.1V for PMOS devices.

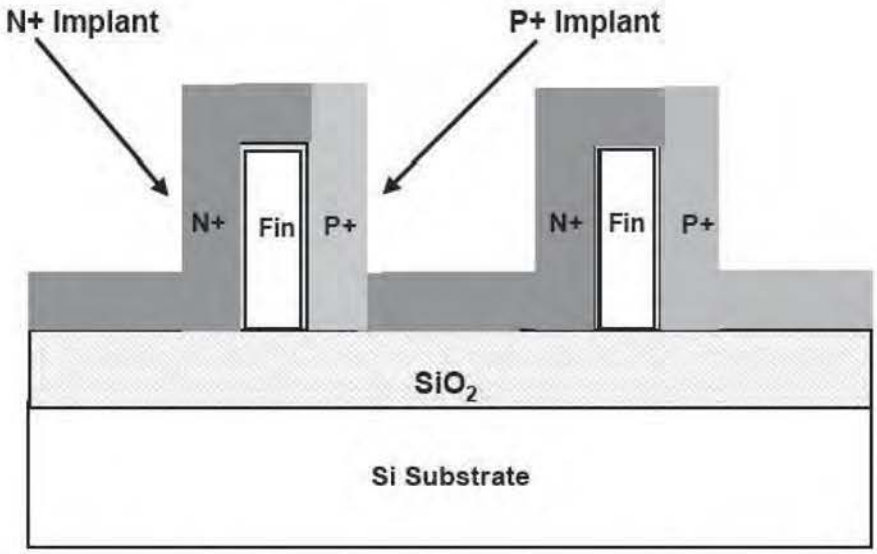


Fig. 2.21. N^+ and P^+ asymmetrical poly-gate formation. Large-tilt-angle gate implant is employed to dope the gates on one side of the fin N^+, and the other side P^+. The implant shadowing effect created by the tall fin helps to achieve this result.

The advantage of such an approach is that the gate material is familiar to semiconductor manufacturing. The disadvantages are: 1) higher Gate Induced Drain Leakage (GIDL) due to the high offset workfunction on one side of the gate [63,64] (more on GIDL in Section 2.3.1.4); 2) V_t is not tunable through gate stack; 3) P^+ poly-silicon gate is not compatible with high-K gate dielectrics due to Fermi level pinning [65,66] and; 4) there is a poly depletion effect which increases the effective oxide thickness.

2.3.2.2 Metal Gate

The use of a metal gate eliminates the poly depletion problem. It increases carrier mobility by reducing the transverse electrical field at a given gate overdrive. Metal gate and high-K dielectrics are key scaling enablers for all MOS technologies. Integrating metal gate electrodes into the MOSFET front-end processes is difficult. One of the main reasons is most metals are not compatible with high-temperature (>1000°C) processing.

Some metal nitrides are stable at very high temperatures, on the other hand. Examples are TiN, TiSiN, TaN and TaCN. The workfunctions of these metals after high-temperature annealing are typically between 4.4eV to 4.7eV, depending on: 1) the layer thickness, 2) alloy composition, 3) crystal orientation and 4) on the gate dielectric material. Metal nitrides are not suitable gate materials for planar CMOS, but they do have the right workfunction for low-power, multi-gate CMOS applications, and have thus been used to fabricate multi-gate MOSFETs.[67] The digital circuit performance of MuGFET made with TiN and TiSiN has been demonstrated to exceed the planar technology with similar gate length (see Chapter 7).

The integration of metal nitride with multi-gate devices is straightforward. A thin layer of metal nitride is deposited either by Atomic Layer Deposition (ALD) or by Chemical Vapor Deposition (CVD). ALD and CVD give conformal step coverage of the fin sidewalls, which is important for high aspect ratio fins. The metal layer is then covered with a thick polysilicon capping layer for gate patterning. The polysilicon capping layer serves as a planarization medium and reduces gate resistance after silicidation (Figure 2.18).

2.3.2.3 Tunable Workfunction Metal Gate

For high-performance CMOS applications, gate stacks with workfunctions at +/- 200mV away from the silicon midgap are sufficient to

set the threshold voltages, but this requires integrating two or more workfunction metal gate systems onto the same chip, one for N-channel transistors and one for P-channel devices.

Several integration schemes have been proposed to produce gates with tunable workfunction materials: Fully Silicide (FUSI) metal gate, metal layer inter-diffusion, the use of multiple metal thicknesses, and nitrogen-implanted molybdenum (Mo) gates.

2.3.2.3.1 Fully Silicided Metal Gate (FUSI)

The use of Fully Silicided (FUSI) metal gate on multi-gate device was first reported in [68]. FUSI metal gates are formed through a silicidation process after the dopant activation anneal, which avoids the problem of compatibility issues of the metal gate with front-end thermal cycles. Figure 2.22 illustrates the general principle of FUSI metal gate formation on a planar device.

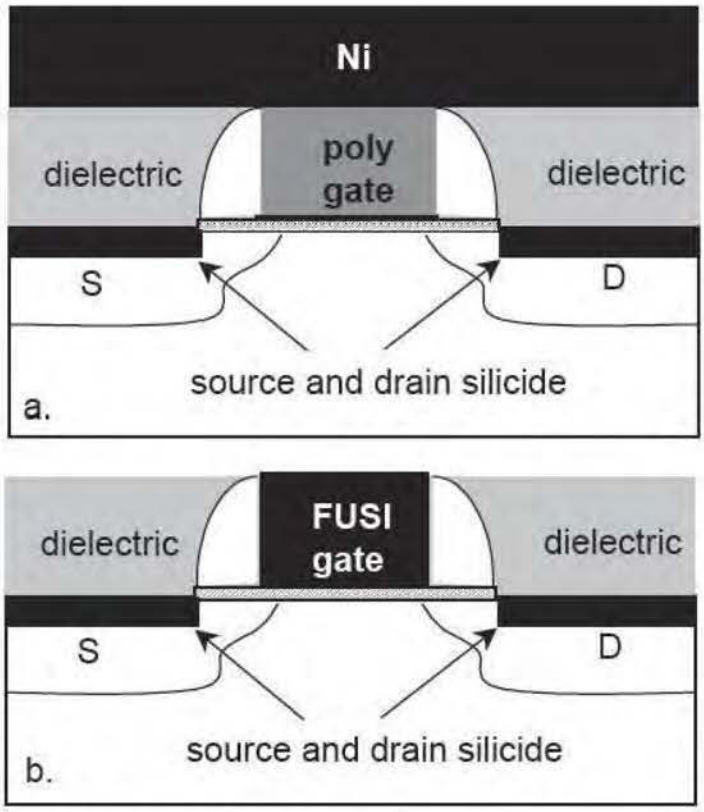


Fig. 2.22. Planar MOSFET Fully Silicided (FUSI) metal gate fabrication concept.

The front-end process, up to the gate silicide formation step, is the same as for a standard polysilicon gate device. After source and drain activation

and silicidation, a layer of filling dielectric material is deposited and polished until the gate is reached. Then, a thick layer of metal (usually Ni or Co) is deposited on top of the gate. After proper thermal anneal, the gate is completely silicided all the way to the gate dielectric. Any unreacted metal is then stripped off using a wet process.

The FUSI gate used in a multi-gate MOSFET fabrication process is similar to that used for planar devices. Due to the differential gate poly thickness caused by the fin topography, however, the deposited Ni needs to be thick enough to form a silicide layer all the way to the buried oxide. It is important to control the formation a uniform silicide phase throughout the gate and keeping the Ni from diffusing though the gate dielectric (Figure 2.23).

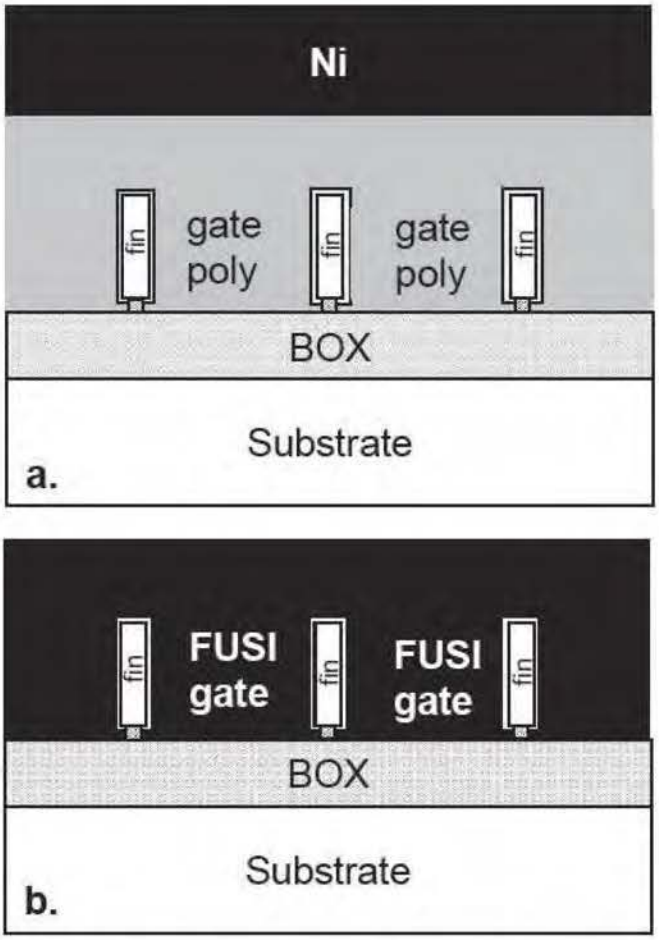


Fig. 2.23. Multi-gate FUSI metal gate formation, a) after metal deposition and b) after silicide formation. Fin topography creates differential gate poly thickness between the fin top and fin bottom. The silicide formation front first reaches the fin top, and must continue to the bottom of the fin. The silicide phase uniformity throughout the gate thickness must be controlled and metal diffusion through the gate dielectric through the extended silicidation process must be limited.

The most commonly used silicides, NiSi and $CoSi_2$, have workfunctions near midgap. In order to adjust the workfunction, a high concentration of dopant is implanted into the polysilicon prior to the gate silicide formation. The effect of dopants on the final effective workfunction of FUSI gate depends on the type of gate dielectric used: on a nitrided gate oxide, boron- and aluminum-doped FUSI have been reported to increase the workfunction up to 4.9eV, while phosphorus, arsenic and antimony can reduce the workfunction down to 4.2eV.[66-68]

The origin of such effective workfunction changes with pre-doped poly silicon is a dopant segregation effect that occurs during silicide formation. Doping atoms have much smaller solid solubility in NiSi than in polysilicon. As Ni consumes Si to form NiSi, dopants in the polysilicon start to segregate out and are pushed toward the gate dielectric interface. When the silicon in the gate is completely consumed and transformed in NiSi, an extremely high concentration of dopant is formed at the interface between the silicide and the gate dielectric, which alters the effective workfunction of the gate stack.

The "dopant segregation" effect is less pronounced on high-K dielectrics. Boron doping has little impact on the workfunction due to Fermi level pinning.[72]. The use of nickel-rich silicides can help to reduce the Fermi level pinning. A workfunction of 4.85eV was achieved with Ni_2Si.[73] Extremely high concentrations of Ytterbium in NiSi was used to move the workfunction up to 4.22eV.[74] Unfortunately, the simultaneous integration of multi-phase Ni silicides on the same chip is by no means an easy task.

2.3.2.3.2 Metal Nitride Thickness and Nitrogen Content

The effective workfunction (EWF) of TiN and TiSiN has been found to change with the thickness of the layer.[75,76] Up to 250mV workfunction shift were observed when TiN thickness was increased from 3nm to 20nm. The workfunction saturates at mid band gap for TiN layers thicker than 20nm. TiSiN has a workfunction that varies from 4.44eV to 4.83eV when the layer thickness is increased from 2.5nm to 20nm.[77,78,127] Similarly, the workfunction of TiSiN saturate at 20nm (Figure 2.24). The origin of the workfunction shift with TiN and TiSiN thickness is the effective nitrogen content in the metal. The top portion of the TiN is oxidized and become nitrogen deficient. For thin TiN layers, a relatively Ti-rich TiN is formed, which yields a lower workfunction value.

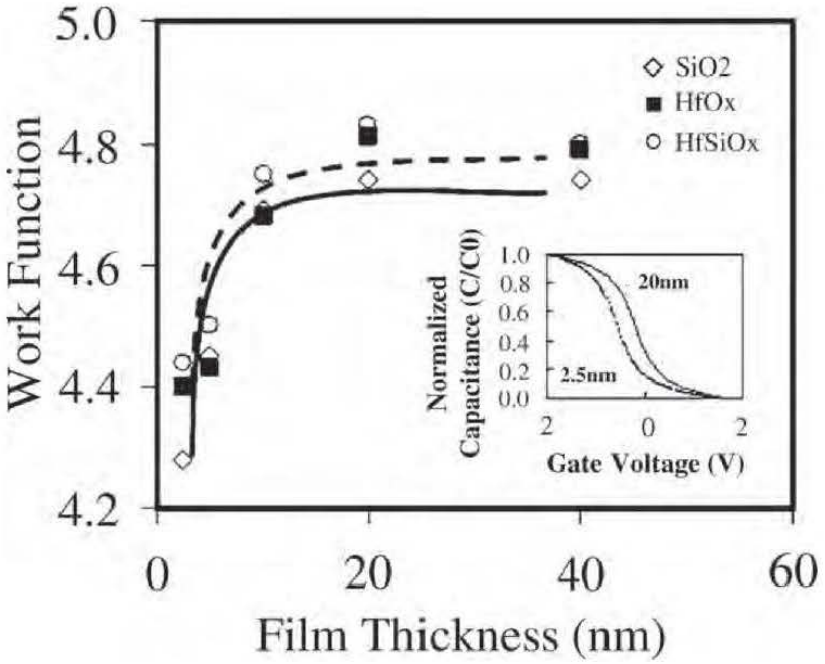


Fig. 2.24. TiSiN effective workfunction as a function of the TiSiN film thickness and gate dielectric materials. REPRINTED WITH PERMISSION FROM [17]. COPYRIGHT 2006 AMERICAN INSTITUTE OF PHYSICS.

The effective workfunction of molybdenum (Mo) varies with the nitrogen content in the metal.[79] Molybdenum is a good candidate for gate material because its high melting temperature (2623°C) makes it compatible with CMOS processing. In addition, it has a low resistivity.[80] The workfunction of Mo is 4.9eV. Nitrogen implant can reduce the Mo effective workfunction to 4.5eV. The amount of workfunction shift is a function of the implanted nitrogen dose and the thermal anneal done after the implant. Low nitrogen implant energy should be used to avoid penetration of nitrogen ions in the gate dielectric.

2.3.3 Gate EWF and Gate Induced Drain Leakage (GIDL)

Gate Induced Drain Leakage (GIDL) is caused by band-to-band tunneling in the drain region under the gate.[81-84] When there is a large drain-to-gate bias, enough band-bending occurs in the Si at the gate dielectric interface, causing valence band electrons to tunnel into the conduction band. In the case of n-channel devices, the generated electrons flow to the drain while holes flow to the lowest potential electrode, *i.e.* to the source.

The band-to-band tunneling current is a function of the total electrical field in the drain overlap region, and a function of the bandgap of the semiconductor.[85-86] For direct-bandgap materials, J_{GIDL} can be modeled by Equation 2.27.

$$J_{GIDL} = AE_{TOT} \exp(\frac{-B}{E_{TOT}}) \tag{2.27}$$

where A is a pre-exponential parameter given by Equation 2.28 and B is a physically-based exponential parameter given by Equation 2.29. E_{TOT} is the electrical field at point the maximum band-to-band tunneling.

$$A = \frac{2qm_r \pi E_g^2}{h^3} \tag{2.28}$$

$$B = \frac{\pi^2 \sqrt{m_r} E_g^{3/2}}{qh\sqrt{2}} \tag{2.29}$$

E_g is the energy bandgap of the semiconductor channel. E_g has a strong influence on the band-to-band tunneling current. E_{TOT} depends on 1) the doping profile of the drain overlap region, 2) the gate oxide thickness and 3) the applied bias. CMOS scaling requires an abrupt doping profile and a thin gate dielectric. Both of these requirements increase E_{TOT} and the GIDL current. Figure 2.25 illustrates the GIDL current component in the $I_d(V_g)$ curve of a device. GIDL is most pronounced at large negative gate-to-drain biases.

A large component of the E_{TOT} is the surface electrical field E_S. E_S is defined by Equation 2.30. If we ignore the doping gradient effect, Equation 2.30 is the E_{TOT}.

$$E_S = \frac{V_{DG} - V_{FB} - 1.2}{3T_{OX}} \tag{2.30}$$

where V_{GD} is the drain to gate bias and V_{FB} is the flat-band voltage. Equation 2.30 is not directly applicable to double-gate devices, since E_s depends on the silicon body thickness.[87] The transverse electric field is reduced when the silicon film thickness is decreased. Fully depleted double-gate devices have lower surface electrical field than planar bulk MOSFETs and FDSOI devices.

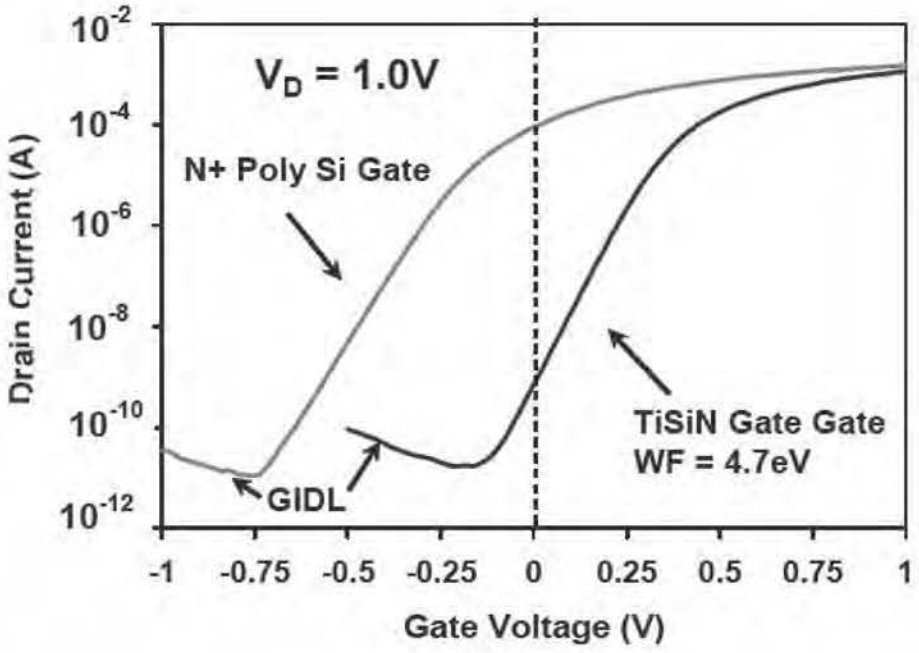


Fig. 2.25. GIDL current as a function of gate voltage and gate electrode workfunction. Using a higher gate effective workfunction shifts the $I_d(V_g)$ curve to the right and increases the GIDL current at any given gate voltage.[67]

Equation 2.30 indicates that the flat-band voltage partially determines E_S. V_{FB} for mid-band gap metal gate is, by definition, different from heavily doped poly-silicon gate by half a bandgap, $E_g/2$. Thus, the use of a midgap metal gate will cause a higher electric field and a higher GIDL current. A simple way to interpret the change in GIDL caused by the use of different gate workfunctions is shown in Figure 2.25. Using a gate material with a higher workfunction shifts the entire $I_d(V_g)$ curve to the right. As a result, for any given gate-to-drain voltage, the midgap metal gate will give rise to a higher GIDL. In principle, the use of a thin-body, double-gate structure reduces the surface field, while the use of a midgap metal gate increases E_S. The final GIDL performance is determined by the overall device design.

The generation of GIDL current is limited to the drain overlap region under the gate. The amount of overlap plays an important role in determining the total current. If the drain is pushed away from the gate edge and if no drain-to-gate overlap exists (underlap), the electrical field is reduced significantly. Several papers have suggested improved I_{on} *vs.* I_{off} performance can be obtained in MuGFETs with drain underlap.[88-90]. Such a design can reduce GIDL to negligible values compared to

subthreshold leakage. Figure 2.26 illustrates the source and drain underlap structure concept.

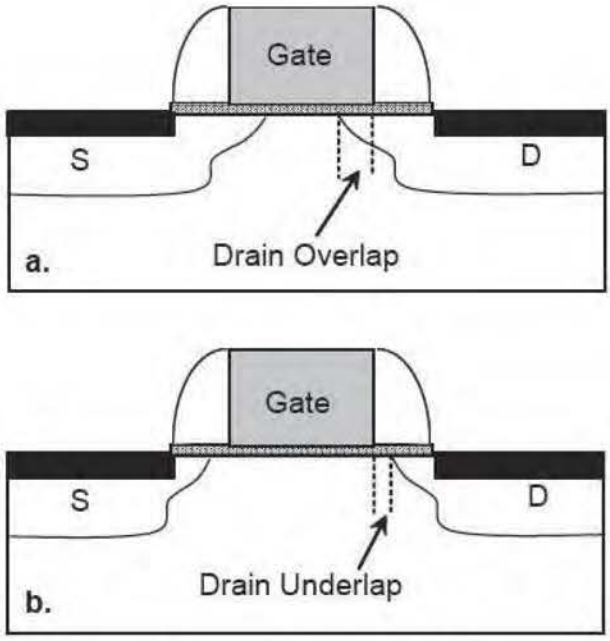


Fig. 2.26. a) Drain overlap MOSFET: GIDL occurs in the overlap region; b) Drain underlap MOSFET: Drain is moved away from the gate. As a result, the electrical field and the GIDL current are reduced.

2.3.4 Independently Controlled Gates

It is possible to fabricate FinFETs in which the two gates can be biased independently.[91-94] These devices are commonly called Multiple Independent Gate MOSFETs (MIGFETs) or 4 terminally–driven MuGFET (4T-MuGFET). The four terminals are the source, the drain, Gate 1 (G1) and Gate 2 (G2) (see Figure 2.27). 4T-MuGFET enables the threshold voltage of G1 to be raised or lowered by G2 to achieve a higher range of I_{on}/I_{off} performance (Figure 2.28). The 4T-MuGFET structure can be particular useful in power management, where high I_{on}/I_{off} ratio header and footer transistors are used.

The relationship between the threshold voltage of Gate 1, V_{tG1} and G2 bias can be modeled by Equation 2.31.[95] This is a simplified model, since it uses a charge sheet approximation of the channel carrier distribution. It also ignores SCE and quantum mechanical effects. Nevertheless, Equation 2.31 gives a simple way to understand how the G1

threshold voltage changes with G2 bias. C_{ox1} is the G1 gate oxide capacitance and C_{ox2} is the G2 gate oxide capacitance, $C_{Fin} = \varepsilon_{si}/Fin_{WIDTH}$ is the depletion capacitance of the silicon fin.

$$\frac{\Delta Vt_{G1}}{\Delta V_{G2}} = -\frac{C_{Fin}C_{ox2}}{C_{ox1}(C_{Fin} + C_{ox2})} \approx -\frac{3t_{ox1}}{3t_{ox2} + Fin_{WIDTH}} \tag{2.31}$$

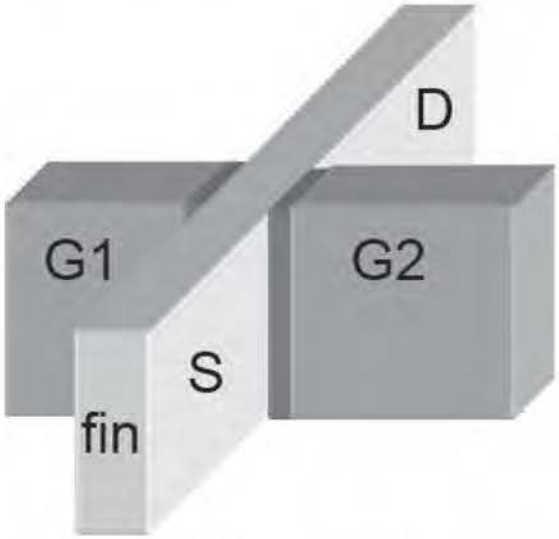


Fig. 2.27. 4T-MuGFET, Gate 1 (G1) and Gate 2 (G2) are electrically isolated from one another. This configuration allows for the independent biasing of G1 and G2.

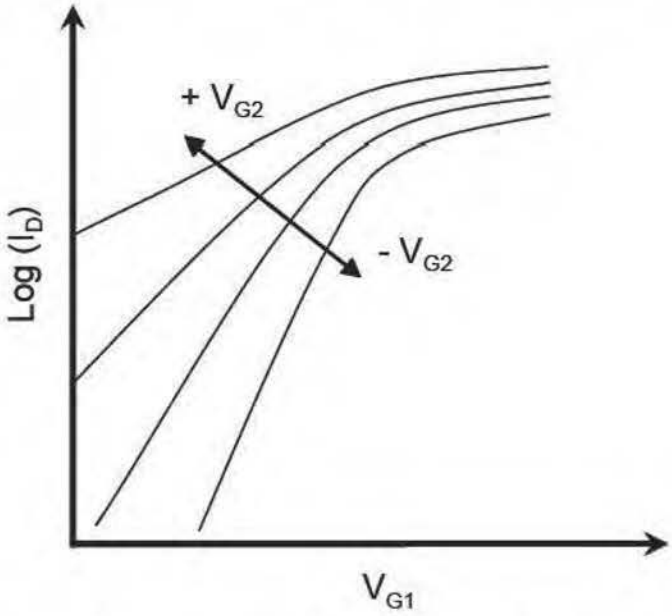


Fig. 2.28. 4T-MuGFET drain current as a function of G1 voltage (V_{G1}) and G2 voltage (V_{G2}). V_{G2} affects the I_D *vs.* V_{G1} curves.

Further analysis of the $\Delta V_{tG1}/\Delta V_{G2}$ relationship by Zhang *et al.* [96] reveals that V_{G1} and V_{G2} both control the charge density and the inversion charge centroid position in the fin. The change of inversion carrier centroid position within the fin changes the effective thickness of $t_{ox1(eff)}$ and $Fin_{WIDTH(eff)}$. Equation 2.32 can be modified based on the position of the inversion layer charge centroid in the fin, x_c, where $0 < x_c < Fin_{WIDTH}$.

$$\frac{\Delta Vt_{G1}}{\Delta V_{G2}} \approx -\frac{3t_{ox1(eff)}}{3t_{ox2} + Fin_{WIDTH(eff)}} = \frac{3(t_{ox1} + \frac{x_c}{3})}{3t_{ox2} + (Fin_{WIDTH} - x_c)} \tag{2.32}$$

To fabricate a 4T-MuGFET, the gate material on top of the fin needs to be removed to provide electrical isolation between G1 and G2. Chemical Mechanical Polishing (CMP) can be used, providing a fin hardmask is in place to stop the CMP before it starts to etch the fin. This approach converts all the devices on the chip to 4T-MuGFETs (Figure 2.29). If only some devices on the chip need to become 4T-MuGFETs, a photo mask step must be employed to selectively open the area just on top of the fin. In this case, plasma etch is used to remove the gate material. The etch end point signal can be provided by the fin hardmask.

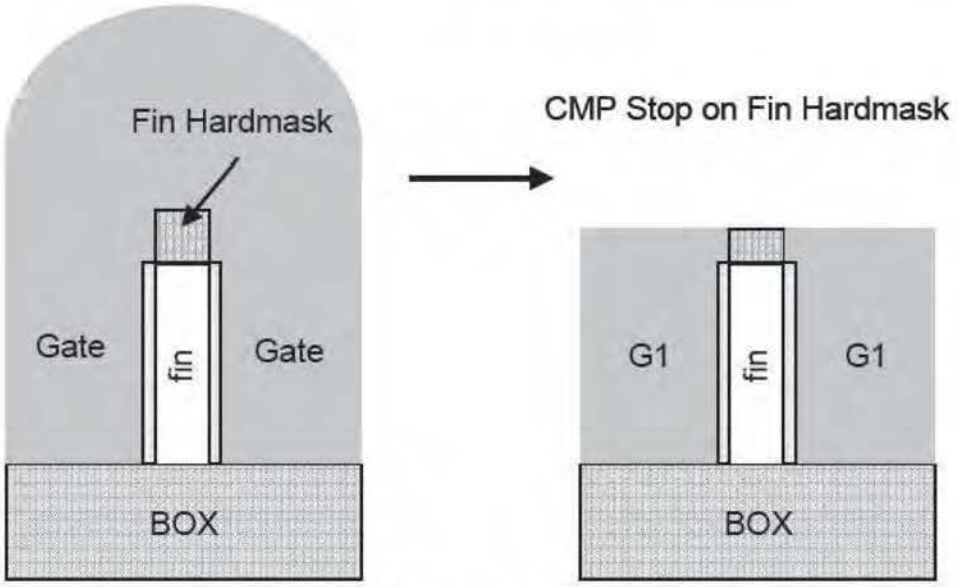


Fig. 2.29: Fabrication of a 4T-MuGFET: The unwanted gate electrode material is removed by Chemical Mechanical Polishing (CMP). The fin hardmask serves as CMP etch stop.

2.4 Source/Drain Resistance and Capacitance

2.4.1 Doping the Thin Fins

Since multi-gate channels are on the sidewall of the fins, the source and drain should be uniformly doped along the sidewalls to avoid variable parasitic resistances across fin height. Large-angle, two-pass, tilted implants are widely used to dope the source and drain extensions and the deep source and drain. Figure 2.30 illustrates the implant process. Two adjacent fins will cast implant shadows on each other. The maximum tilt angle that is allowed while avoiding that the shadow effect blocks the implant from reaching the adjacent fin is limited by the fin height and the fin spacing. It is given by Equation 2.33:

$$Tilt\_Angle \leq \arctan\left(\frac{P_{FIN} - Fin_{WIDTH}}{Fin_{HEIGHT}}\right) \tag{2.33}$$

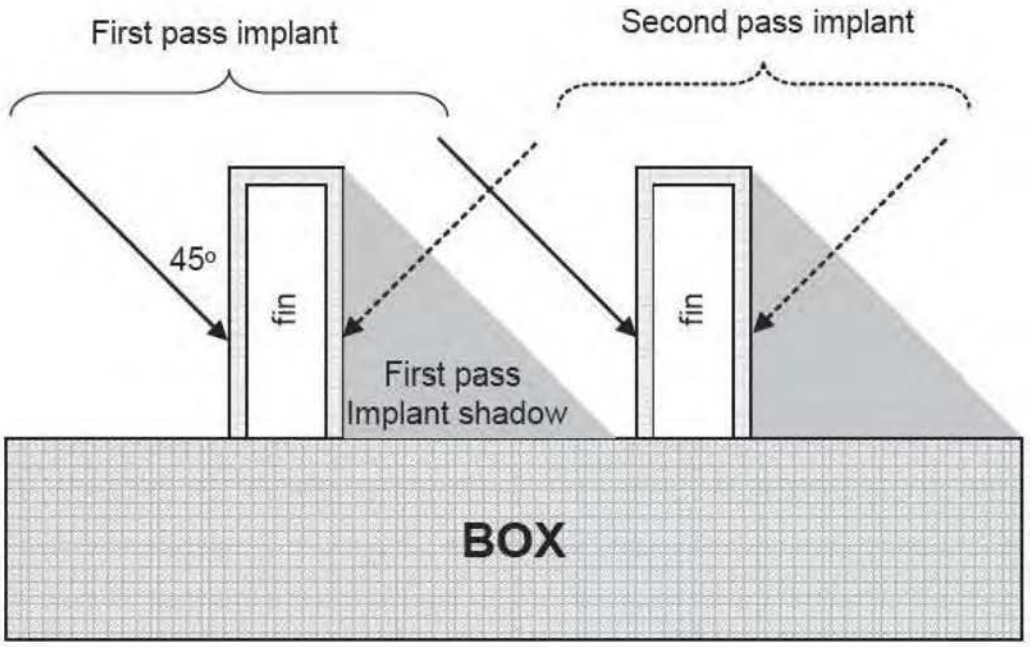


Fig. 2.30. Tilted S/D implant.

If the fin top surface is exposed to the implantation, as in Figure 2.30, the top portion of the fin will receive two implants. Furthermore, if the implant tilt is less than 45 degrees, the incident angle of the ion beam for the top surface is higher than for the sidewalls. Thus, the top surface will receive a higher implant dose and the dopants will penetrate deeper. This

results in lower resistance for the top portion of the fin and smaller effective channel length for the top portion compared to the bottom portion. Figure 2.31 illustrates this effect.

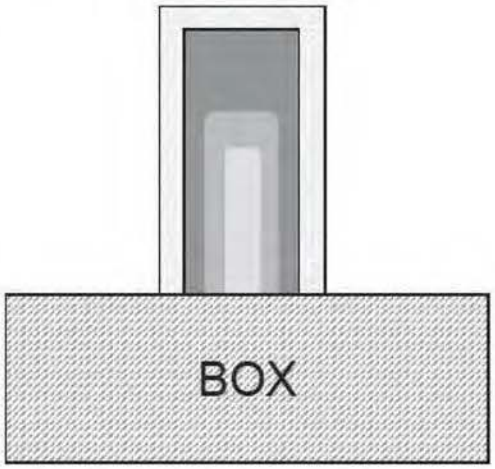


Fig. 2.31. Illustration of the impact of tilted implant on the doping profile in the fin. The darker color represents a higher doping concentration. Double implants on the top of the fin result in non-uniform doping concentration and resistance.

Larger tilt implant angles can reduce the problem [97], but the best way to dope the fin uniformly is through isotropic implant. Pulsed Plasma Doping (PLAD) has been developed for high throughput, sub-1keV implants. The ion incident angle distribution can be scattered depending on process parameters to achieve isotopic implantation. Details on the PLAD implant technique can be found in [98].

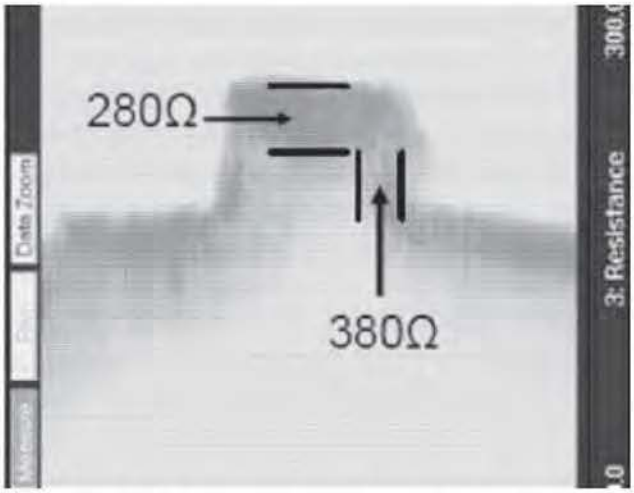


Fig. 2.32. SSRM profile of a PLAD implanted fin. The doping uniformity of the fin top and fin sidewall is not perfect, but it is better than what can be achieved by 45 degree tilt implant.[100] Copyright© 2006 IEEE.

Scanning Spreading Resistance Microscopy [99] has been used to study the 2-dimentional resistance distribution of the fin cross section, which can be used to approximate the doping profile. Figure 2.32 shows the SSRM scan of a fin that was implanted with a PLAD process. The resistance ratio between the sidewall and fin top surface is 1.4. This is better than the 2:1 achieved by 45 degree tilted implant. [100]

2.4.2 Junction Depth

The physical Fin_{WIDTH} limits the maximum junction depth in a multi-gate MOSFET to one half of the fin width. Therefore, the junction depth is no longer limited by implant energy and thermal cycle. It is still important to control the implant energy and thermal cycle of multi-gate MOSFET, since dopants will move laterally. The lateral movement of the dopants determines the source and drain overlap or underlap, and therefore, the effective channel length. Furthermore, the parasitic resistance is highly dependent on the junction abruptness and doping gradient in the source and drain extension. Smaller gradients and abrupt junctions reduce the extension resistance, but increase short channel effects.

2.4.3 Parasitic Resistance/Capacitance and Raised Source and Drain Structure

In Section 2.2.1 we have shown that in order to maintain a good SCE control, fin width needs to be less than the gate length. Continued scaling of the CMOS will inevitably push the fin width below 20nm. Sources and drains made in such thin fins have a high resistance.

One way to reduce this resistance in the source and drain regions is to widen the fin outside the gate area by selective epitaxial growth (SEG) (Figure 2.34).[13,101] The resulting structure is commonly referred to as Raised Source and Drain (RSD). The RSD structure reduces the R_{SD} component of the parasitic resistance, however, R_{ext}, the resistance in the source and drain extension regions under the gate spacer (Figure 2.33) remains high due to the thin fin. Placing the raised source and drain closer to the gate reduces R_{ext}, but increases the parasitic capacitance C_{ext}. To optimize the AC performance, design trade-off between R_{ext} and C_{ext} is required. The advantage of the raised source and drain structure is not just limited to R_{SD} reduction. It also gives more process margin to form silicided source and drain and gives a larger contact landing area.

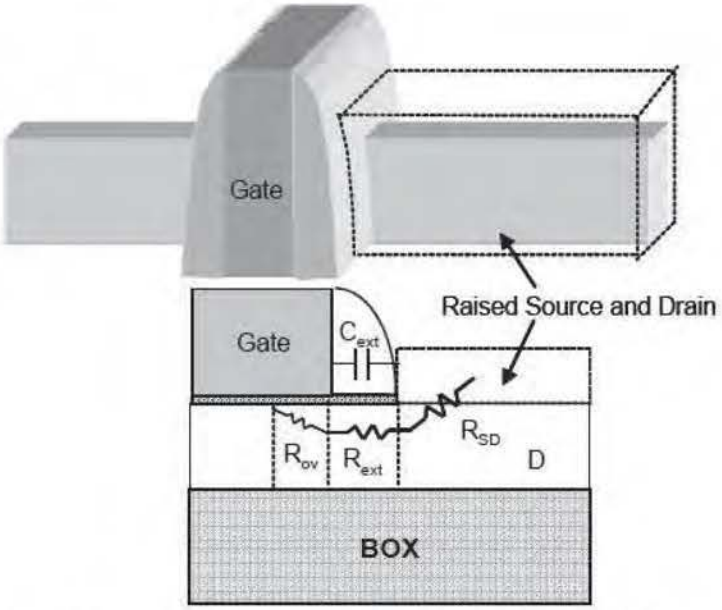


Fig. 2.33. The raised source and drain structure reduces the R_{SD} but increasess C_{ext}.

The RSD process integration is complicated by the gate spacers left on the sidewalls of the fins (Figure 2.34a). Spacers on the sidewall of the fins must be removed prior to epitaxial growth. One way to remove the fin sidewall spacers is to use a gate hardmask taller than the fins. In this approach, dry etch can remove all the spacers on the sidewall of the fins, while leaving enough hardmask and spacer on the gate (Figure 2.34).[13]

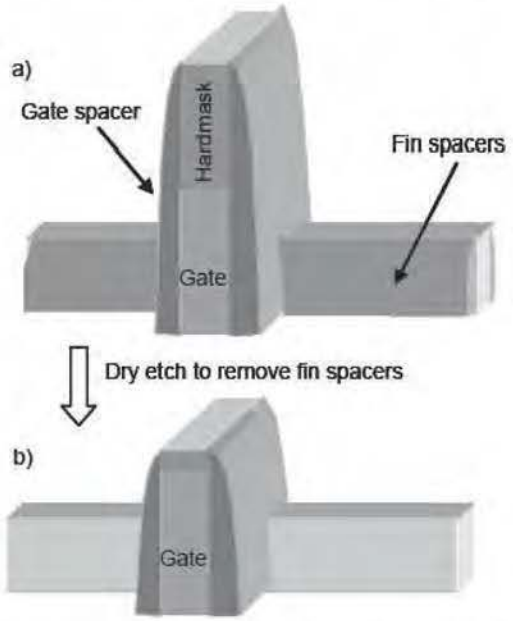


Fig. 2.34. Parasitic fin spacers are formed at the same time as gate spacer. The fin spacer must be removed prior to RSD growth process.

It is important to leave enough gate spacers and gate hardmask to prevent "mushroom" and "Mickey Mouse Ears" defects from forming. "Mushroom" formation happens when the gate hardmask is completely removed from exposing the gate to surface to SEG. "Mickey Mouse Ears" happens if the gate top corners are exposed during SEG. Both "mushroom" and "Mickey Mouse Ears" defects can cause shorts between gate and the source and drain (Figure 2.35).

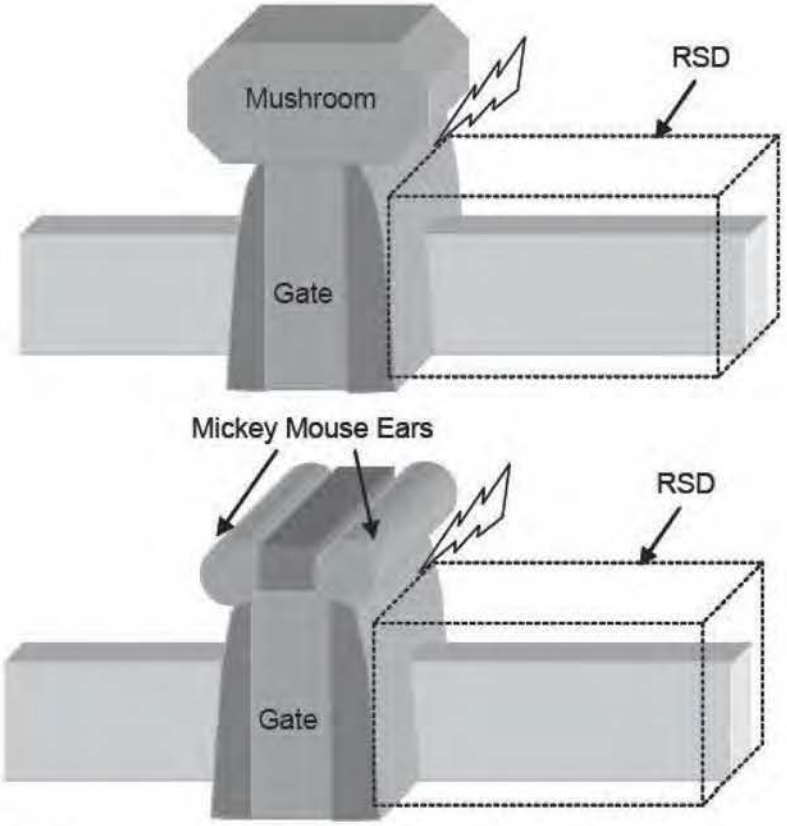


Fig. 2.35. If the polysilicon gates are NOT completely covered by protective dielectric, gate "mushroom" or "Mickey Mouse Ears" defects will occur. Both defects can cause short circuit between gate and source and drain.

Another integration method, proposed by Kaneko *et al.* [102] avoids the formation of parasitic fin sidewall spacer altogether. After gate formation, a filling material is deposited and planarized by CMP. An etch-back process recesses the filling material below the gate hardmask. Then spacers are formed on the sides of the exposed gate hardmask. At this time the fins are still embedded in the filling material. After etching the filling material using the newly formed spacer as a hardmask, spacers are only formed along the sidewall of the gate, and not on the sidewalls of the fins (Figure 2.36).

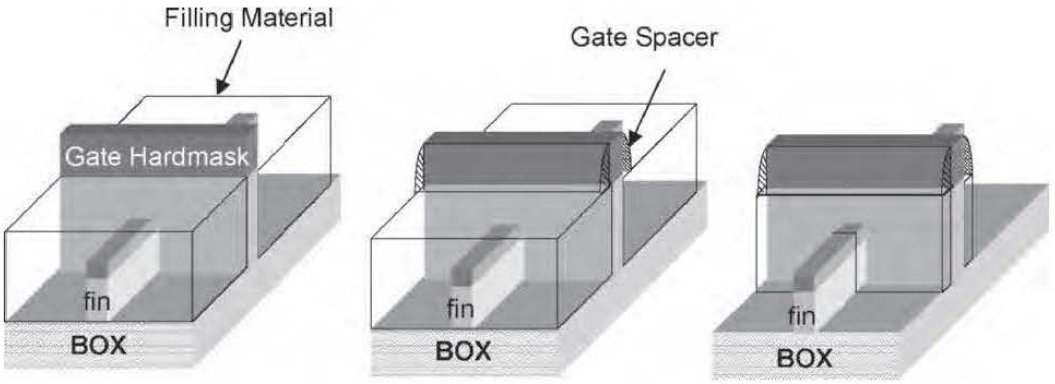


Fig. 2.36. Integration scheme to form gate spacer without parasitic fin spacer.

The preparation of the silicon surface before epitaxial growth is important. An in-situ hydrogen pre-bake step at temperature ~ 800°C is typically used before the growth process. Thin silicon fins are susceptible to damage at this temperature at low H_2 partial pressure.[47] The deposition of a nitride hardmask on top of the fin can help to protect the fins.[102]

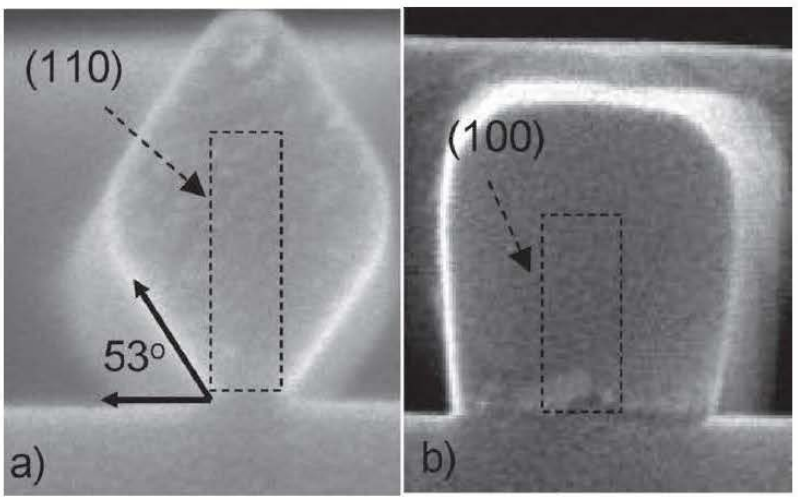


Fig. 2.37. Cross sectional SEM images on fins after epitaxial growth. a) (110) side wall surface result in diamond-shaped fin; b) (100) sidewall surface result in square-shaped fin.

The selective epitaxial growth (SEG) surface faceting is different for different surfaces. The faceting determines the final shape of the source and drain region. For (100) sidewall surfaces, a rectangular shaped fin is possible. For (110) sidewall surface, the faceting will result in a diamond shaped surface [102] (Figure 2.37). Diamond-shape fins present challenges to interlayer dielectric fill. Any unfilled region could become a potential defect site in the contact and back-end of the line processes.

2.5 Mobility and Strain Engineering

2.5.1 Introduction

The carrier mobility, μ, can be defined by Drude's Equation

$$\mu = \frac{q\tau}{m^*} \tag{2.31}$$

where q is the elemental charge, τ is the mean scattering time and m^* is the effective mass of the carriers. The value of both τ and m^* can be modified through strain engineering. Under external applied stress, the Si crystal lattice constant (or inter-atomic spacing) is altered, thus changing the band structure, the density of states and the effective mass of the carriers. The strain effects on mobility are anisotropic.[103-104] It highly depends on the surface orientation and the channel direction. A more detailed theoretical discussion of strain engineering can be found in Chapter 5.

Strain effect on carrier mobility was first used to fabricate piezoresistance-based sensors.[105] The application of strain engineering to CMOS can be traced to the 1980s [106-107], where a thin Si layer was first grown on SiGe. The Si lattice takes on the larger lattice constant of SiGe, which produces biaxial tensile strain in the silicon. Since then, uniaxial strain techniques (stressors) have been adopted as one of the main performance boosters for planar CMOS.[108-109]. Drain current improvement in excess of 50% for PMOS transistors and 32% for NMOS devices has been reported.[110]

In order for multi-gate MOSFET technology to be successful, it must be compatible with these powerful performance booster techniques. The following sections describe the response of the multi-gate MOSFET to various strain techniques.

As mentioned in Sections 2.2.1 and 2.5.1 the surface orientation and current flow directions of a FinFET can be (110)/<110>, (100)/<100>, as well as (111)/<111>, respectively. Each surface orientation and channel direction has a different mobility response to a given stress. Since most of the multi-gate devices made to date have been on (100) and (110) surfaces, we will focus our discussion of process strain techniques on these surfaces.

2.5.2 Wafer Bending Experiment

The basic responses of multi-gate channel mobility to various stress components were studied in a wafer bending experiment.[111] Figure 2.38 illustrates the wafer bending apparatus.[112] Circular ridges were used to produce a bi-axial stress in Reference 111. The surface stain is measured based on the sample thickness and the radius of the curvature.

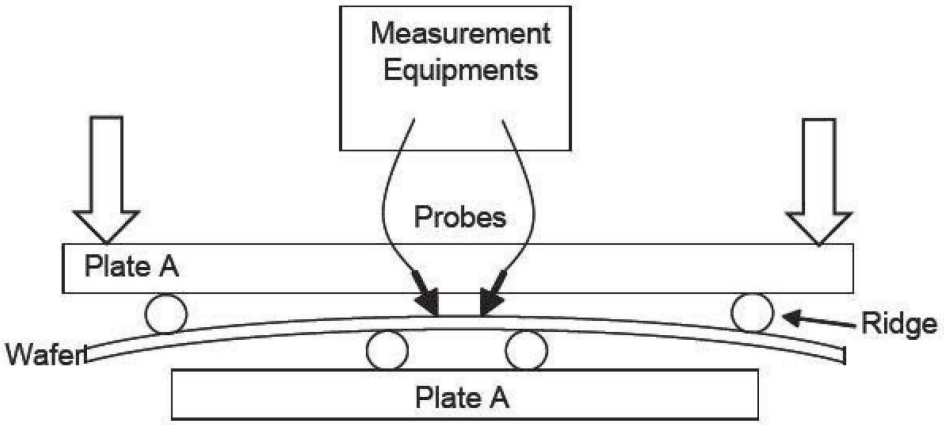


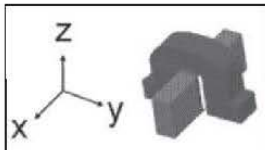
Fig. 2.38. Wafer bending apparatus. A wafer or a piece of wafer containing devices is bent by pressing Plate A toward Plate B. Bi-axial stress is applied to the wafer through the circular ridges.

For a 0.11% surface strain (~200MPa), the peak electron mobility was shown to improve by +14% for (100)/<100> fins and +26% for (110)/<110> fins. The peak hole mobility shift with the same surface strain was +8% in (100)/<100> devices and -3% in (110)/<110> PMOS devices. Table 2.1 summarizes the experimental results and the estimated stress levels based on the bulk silicon piezoresistance (PR) coefficients from reference.[111]

There are three stress components: 1) σ_{xx} is the stress in the direction parallel to channel current flow; 2) σ_{yy} is in the plane of the channel conduction, perpendicular to the current flow; 3) σ_{zz} is in the direction vertical to the plane of the channel conduction. (See the figure in the insert of Table 2.1.)

The estimated stress in each direction is similar to the applied stress in the experiment. These wafer bending exercise prove that strain engineering is possible in multi-gate MOSFET, and the response of carrier mobility to stress is similar to planar bulk devices. It is now an engineering undertaking to make the processes work.

Table 2.1. Projected stress in each crystal direction using bulk PR coefficients. [111] Copyright© 2006 IEEE.

	STRESS (Mpa)			MOBILITY IMPROVEMENT (%)			
	σ_{xx}	σ_{yy}	σ_{zz}	(100) NMOS	(100) PMOS	(110) NMOS	(110) PMOS
Experiment				14.4	8.1	25.9	-2.6
PR Theory	290	350	-160	14.4	1.7	25.6	-2.6

2.5.3 Nitride Stress Liners

Depending on the deposition condition, a nitride film can be either tensile or compressive. Tensile nitride film is a common stressor used to improve NMOS performance. Tensile films tend to shrink, thus when deposited on top of the gate and over the source and drain, the portion of the nitride film on top of the source and drain produces tensile stress in the channel direction (σ_{xx}). The nitride film on the sidewall of the gate exerts a compressive stress in vertical to the channel (σ_{yy}) (Figure 2.39). (100)/<110> Electrons mobility is enhanced by tensile stress in the σ_{xx} direction and compressive stress in the σ_{yy} direction, therefore a net gain in electron mobility is achieved with tensile stressor.

The amount of the strain in the channel is a function of: 1) the stress level in the stressor film, 2) the transistor spacer width, 3) the gate height, 4) the size of the source and drain, and 5) the gate length. Narrow spacers bring the stressor closer to the gate, and therefore improve the stress transfer into the channel. A tall gate allows more stressor volume to induce compressive stress in the σ_{yy} direction. For the same reason, long sources and drains produce higher stress levels in the channel.[114] Therefore, in Figure 2.39, the drain side induces higher channel strain than the source side. As the gate length increases, the stressor is located further away from the channel center, therefore the overall channel strain induced by the stressors become smaller. For this reason, the nitride stressors are not effective in improving long-channel device performance.

Hole mobility is enhanced by the opposite channel stress. A compressive liner can be used for PMOS. The difference between PMOS and NMOS is that the hole mobility is not sensitive to the stress in the σ_{yy} direction, unlike the electron mobility. Tensile and compressive nitride stressors on multi-gate have been theoretically studied in [115]. The stress induced in the channel by stressors is the same for multi-gate devices as

for planar devices. Stress-induced improvement in drive current has been demonstrated experimentally.[116-118]

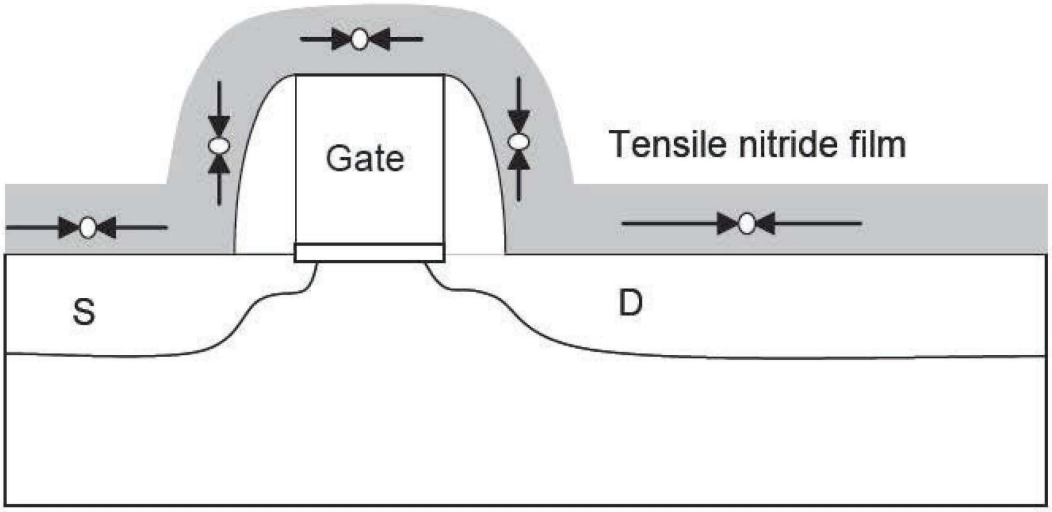


Fig. 2.39. A tensile stressor tends to shrink. The stressor on the source and drain pulls apart the ends of the channel and produce a tensile strain σ_{xx} in the silicon. The stressor on top of the gate squeezes the gate and produces a compressive stress σ_{zz}.

2.5.4 Embedded SiGe and SiC Source and Drain

Embedded SiGe source and drain was first investigated for the purpose of reducing the contact resistance for in PMOS devices. SiGe has a lower Schottky barrier height for holes than Si. The experimental results have shown a larger than expected drive current improvement when SiGe source and drain structures are used.[106] It was later found that SiGe, with its larger lattice constant than Si, produces a compressive stress in the channel which improves the hole mobility. Figure 2.40 illustrates the compressive stress SiGe source and drain exert in the Si channel. The amount of strain in the channel increases with Ge content (larger SiGe lattice). The SiGe lattice constant $\alpha_{Si_{(1-y)}Ge_y}$ is a function of the Ge content and can be estimated by Equation 2.32. [119]

$$\alpha_{Si_{(1-y)}Ge_y} = (1-y)\alpha_{Si} + y\alpha_{Ge} \tag{2.32}$$

where y is the Ge fraction (between 0 and 1). α_{Si} is the Si lattice constant equal to 5.431Å and α_{Ge} is the Ge lattice constant, equal to 5.646Å.

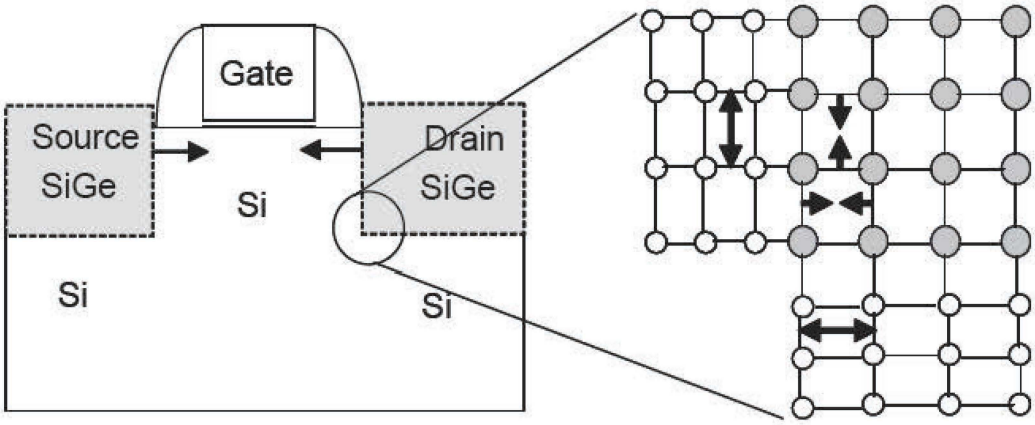


Fig. 2.40. The lattice mismatch between SiGe and Si results in channel compressive stress in the σ_{xx} direction and tensile stress in the σ_{yy} direction. σ_{xx} compressive stress improves hole mobility.

The stress in the channel is not just depended on the lattice mismatch; it also depends on the SiGe volume (size) of the source and drain and the proximity of the SiGe to the channel. A larger volume produces more stress. Therefore, the SiGe impact on PMOS device performance depends on the layout, gate spacer width and gate length, similar to the effect created by a nitride film described in the previous section.

SiGe sources and drains were used in multigate MOSFETs in [31,120]. 25% to 40% drive current improvement was seen compared to samples without SiGe. The improvement is less than what has been reported for planar bulk MOSFETs with (001)/<110> orientation. The reduced improvement can be explained by: 1) reduced PR coefficient for (110)/<110> surface/direction and 2) reduced SiGe volume in the source and drain of the multi-gate MOSFETs.

SiC has a smaller lattice constant than silicon. Thus, the lattice mismatch for a SiC source and drain structure produces a tensile stress in the Si channel, which improves the mobility of electrons. SiC has been successfully demonstrated on multi-gate MOSFETs where one percent C in SiC source and drain produced 20% improvement in transistor current. [121]

2.5.5 Local Strain from Gate Electrode

The gate electrode of a multigate device wraps around the fin from three sides. If stress can be directly applied from the gate, it will have a large impact on the channel mobility. Furthermore, gate stressor would have

reduced gate/active pitch dependence. Some metal deposition processes can produce a large intrinsic stress in the metal film. Tensile stress in the gigapascal range has been reported in metal gates.[27] When such a high tensile metal gate is applied to a multi-gate device, the electron mobility on the (110)/<110> surface/direction can increase by ~100%. Such a tensile stress gate electrode does not change the electron mobility for the (100)/<100> surface/direction, however and it has no impact on hole motility, regardless of the surface orientation and channel direction.[27,75] This approach makes the (110) surface very attractive for MOSFET fabrication.

Metal gate can produce further stress from subsequent processing.[122] Typical metals have thermal expansion coefficients very different from that of silicon. If a SiN capping layer is placed on top of the gate, a limited upward expansion of the metal gate takes place during high temperature processes. The result is a compressive stress in the channel. Since the metal gate is squeezing the silicon fin from both sides, tensile stress is induced in the direction of the current flow, and the electron mobility is increased (Figure 2.41).

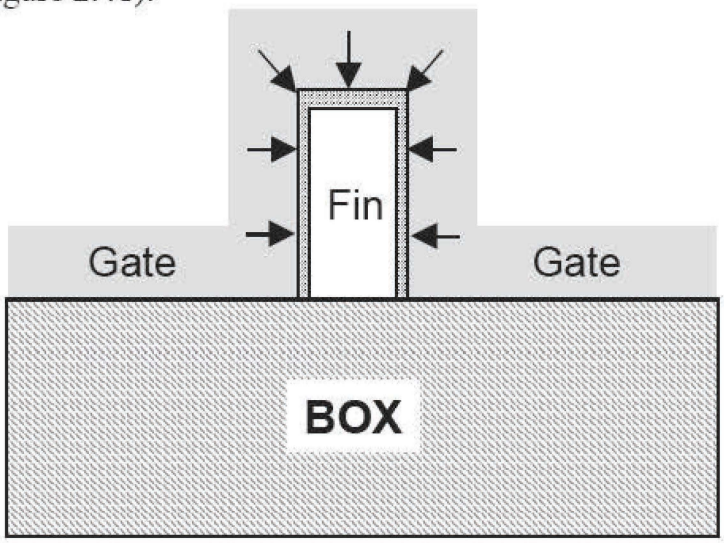


Fig. 2.41. Expansion of metal gate electrode during thermal processing exerts a compressive stress in the fin.

It is interesting to note that the mobility improvements brought about by tensile gate stress were reported on long channel devices. This is very different from other process induced local strain, where the improvement in mobility decreases as the channel length is increased. The main reason for this difference is that the stress is applied from the electrode directly to the channel. For this reason, gate induced stress is not layout dependent.

2.5.6 Substrate Strain: Strained Silicon on Insulator

This final section on strain engineering focuses on substrate-induced strain. Strain is generated in thin Si layers grown on SiGe. The Si lattice takes on the larger lattice constant of SiGe and is submitted to a biaxial tensile strain. Biaxial tensile strain has been shown to improve electron mobility and, if the strain is large enough, hole mobility can be improved as well.[123] However, the IC industry has not adopted the substrate strain for manufacturing, largely due to the relatively poor quality of the substrates: misfit defects and threading dislocations present in these wafers give rise to unacceptable leakage currents.[124]

Strained silicon on insulator (sSOI) can help to reduce above problems by eliminating the need for a SiGe layer below the strained silicon.[125] Figure 2.42 illustrates the manufacturing process of a sSOI wafer. The process starts with a bulk sSi (strained silicon) wafer, where a thin silicon film is grown on a relaxed SiGe layer. The sSi wafer is first implanted with hydrogen and bonded to a host wafer. Then after applying a layer transfer (ion-cut) process, the SiGe layer is selectively etched away, leaving the strained silicon layer directly on the insulator. The oxide below the strained silicon helps to keep the strain intact. An optional epitaxial process can then be used to increase the strain silicon layer thickness without reducing the strain. This approach eliminates the SiGe buffer underneath strained silicon, therefore reducing defect density and Ge up-diffusion. sSOI films with a thickness in excess of 60nm are commercially available.

Thick sSOI layers have been used to fabricate multi-gate MOSFETs. Since channel conduction is located at the sidewall of the fin, the bi-axial stress of sSi produces tensile stress in σ_{xx} direction, compressive stress in σ_{zz} direction and tensile stress in σ_{yy} direction. For narrow fins, the σ_{yy} stress is expected to relax, while the σ_{xx} and σ_{yy} stresses are intact. Experimental data indicates that the (110)/<110> electron mobility is improved by 60% [39] and the (100)/<100> electron mobility is improved by 30%. The stress from sSOI is additive to those generated by a tensile nitride liner and a metal gate.[27,117-118] Improvements of drive current up to 40% has been observed when sSOI, tensile nitride liner and metal gate electrode are used. The tensile stress in the σ_{xx} direction degrades the (110)/<110> p-channel performance, but increases the (100)/<100> hole mobility.

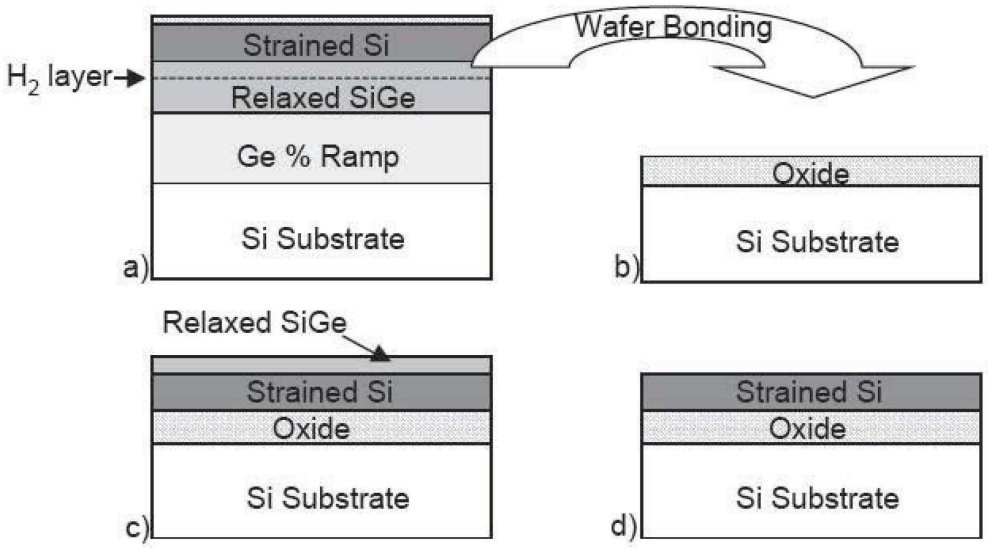


Fig. 2.42. Illustration of the fabrication sequence of a sSOI wafer. a) Starting bulk sSi wafer is implanted with H_2. b) The sSi wafer is bonded to a host wafer, and c) an ion-cut process is used for layer transfer. d) The remaining SiGe is selectively etched away from the strained Silicon on Insulator material.

2.6 Contacts to the Fins

Since the back end of the line process for a MuGFET is the same as for a planar MOSFET, the final section of this chapter reviews the contact formation process for MuGFETs. The unique layout of MuGFET gives three major options for contact: 1) Dumbbell source and drain contact, 2) Saddle contact (individual and slot), and 3) Contact on merged fins. These three options are illustrated in Figure 2.43.

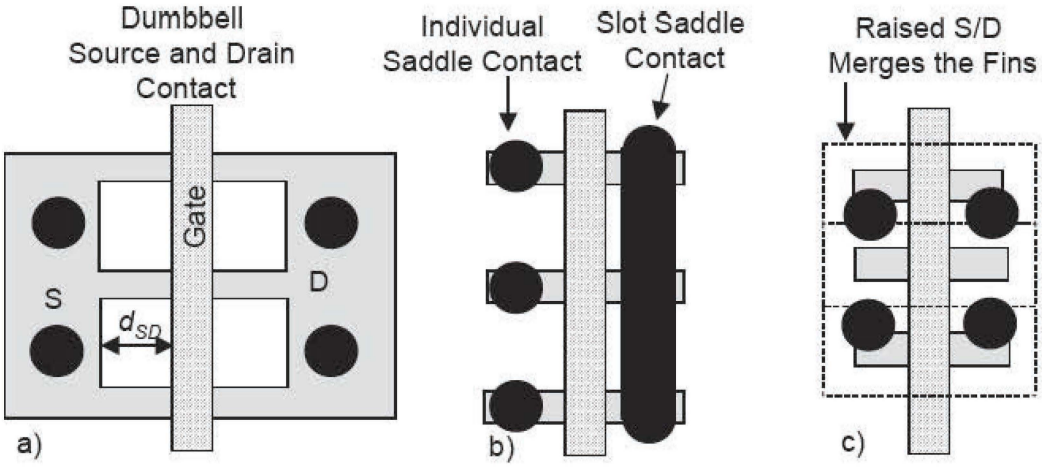


Fig. 2.43. Three contact options for MuGFETs: a) contact to the dumbbell source and drain; b) saddle contact to individual fin, or slot contact; c) contact to the merged-fin source and drain.

2.6.1 Dumbbell Source and Drain Contact

Dumbbell layout provides the most straightforward contact process since it is identical to a planar MOSFET contact. The dumbbell layout is not area efficient, however. The contact to gate spacing is limited by the dumbbell-to-gate distance d_{SD} (Figure 2.43a).

2.6.2 Saddle Contact

The saddle contact is attractive for the following reasons: 1) contact-to-gate spacing can be smaller than for the dumbbell layout, and 2) the saddle contact touches the fin top surface, as well as the fin sidewall surfaces, potentially giving rise to a larger contact area, which can reduce contact resistance (Figure 2.44a). In order to realize a saddle contact, one needs to form a metal silicide on the sidewall of the fin.

The concern with the saddle contact is the alignment of the contact to the active fin. If the contact landing only touches one sidewall of the fin, the contact resistance will be higher than if the contact touches both sides of the fin (Figure 2.44b). Therefore the contact alignment is very tight. This is especially important when the contact size is similar to the fin width in the source and drain area.

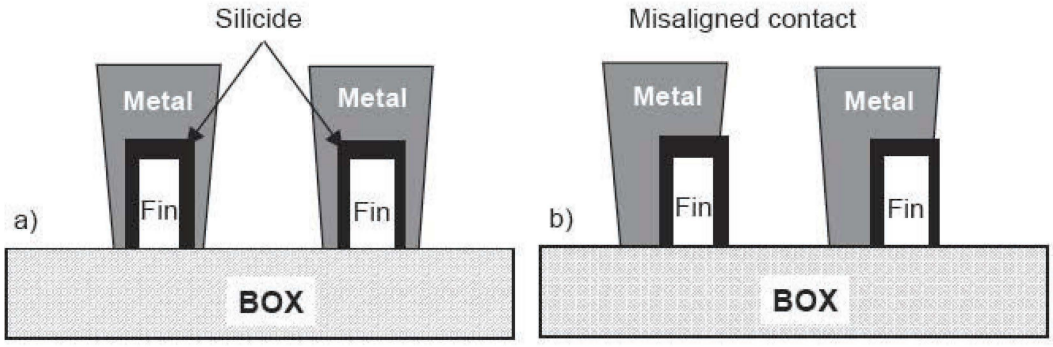


Fig. 2.44. Saddle contact: a) perfect contact to fin alignment; b) misaligned contact.

The major issue with saddle the contact is the contact pitch. If the contact pitch cannot be the same as small as the fin pitch, then making a saddle contact to individual fins is not possible. Slot contacts must be used instead. The alignment constraints on slot contacts are less strict than on saddle contacts (Figure 2.44b). However, slot contacts increase the gate-to-contact capacitance due to the extra contact metal between the fins.

2.6.3 Contact to Merged Fins

To eliminate the contact to fin pitch matching requirement, one can also use epitaxial growth to merge adjacent fins. This is possible since a tight fin pitch is desirable in order to increase drive current per footprint of a transistor. In addition, raised source and drain structure (RSD) is needed to reduce parasitic source and drain resistance. If the increase in fin width from RSD formation is equal to 50% of the fin spacing, adjacent fins will touch one another. In this configuration, the contact to the source and drain will not touch the fin sidewalls. The topography of the source and drain surface will depend on the source and drain epitaxial faceting and the fin conditions (Section 2.4.3, Figure 2.37). For (110) sidewalls the final fin cross section is either hexagonal or diamond-shaped. The contact will land on a non-planar surface (Figure 2.45a). Some contact overetch is needed to ensure that the contact lands on silicide when the landing area is in the groove. For (100) sidewalls the cross section of the epitaxially grown silicon is rectangular and contacts will land on a flat surface (Figure 2.45b). Contacts to merged fins have been shown to reduce parasitic capacitance, compared to other types of contacts described in previous sections.[15]

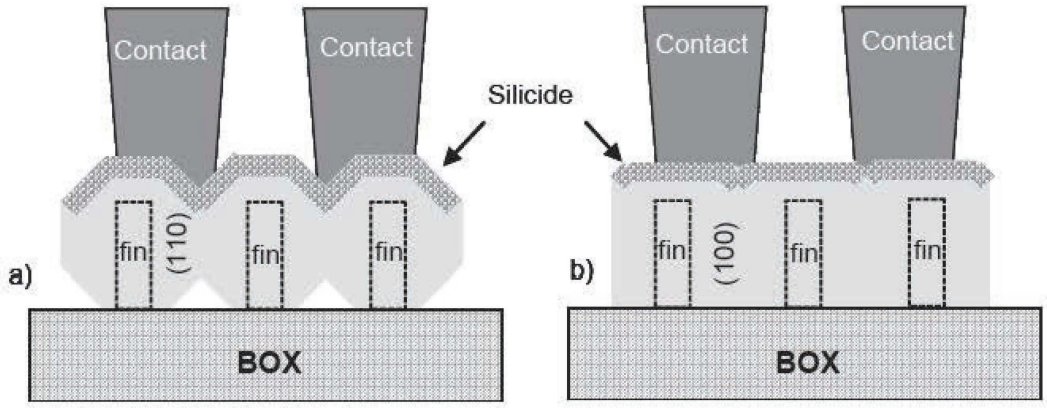


Fig. 2.45. Contact to merged fin: a) if the fin sidewall surface is (110), the contact lands on a wavy topography; b) if the fin sidewall surface is (100), the contact lands on a flat surface.

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