INTRODUCTION

Photolithography produces a three-dimensional pattern on the surface of the wafer using a light-sensitive photoresist material and controlled exposure to light. Other terms for the photolithography process are *photo, lithography, masking,* and *patterning.* In general, lithography refers to any printing process that transfers a pattern to a planar surface. For this reason, photolithography is sometimes referred to as "printing." For semiconductor manufacturing, *microlithography* describes the process used to pattern the ultraminiature features necessary for submicron wafer fabrication. The terms microlithography and photolithography are used interchangeably in this text.

Photolithography Concepts

Photolithography is at the center of the wafer fabrication process, as evidenced by how wafers repeatedly flow into and out of the photolithography operation in the fabrication process (see Figure 13.1). Photolithography is often considered the most critical step in the IC process, requiring superior performance to achieve high yield in other process areas. It is estimated that lithography accounts for nearly one third of the total wafer fabrication cost.[1]

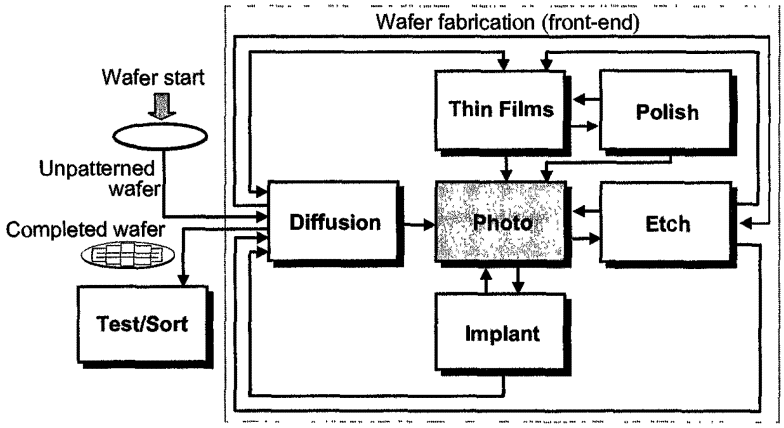


FIGURE 13.1 Wafer Fabrication Process Flow
(Used with permission from Advanced Micro Devices)

The shape of the photolithography pattern transferred to the wafer surface depends entirely on the wafer layer being constructed. Possible patterns are semiconductor devices in the silicon wafer, isolation trenches, contacts, the metal interconnects, and vias to interconnect metal layers. The patterns are transferred into a light-sensitive photoresist material to prepare the substrate for etch (see Chapter 16) or ion implantation (see Chapter 17). The patterned photoresist images are three-dimensional because there are width, length, and height to the pattern in the photoresist (see Figure 13.2). There may be hundreds of identical chips on a wafer, each needing the appropriate pattern to be transferred to each die.

Photolithography technology employs a light-sensitive photoresist, or resist, that is applied on the substrate surface as a polymer solution. The resist is then baked, which drives out the solvent. Next, the resist is exposed to a controlled light. The light passes through a reticle that defines the desired pattern. The photoresist is a temporary material placed on the wafer surface solely to transfer the necessary pattern and is removed once the pattern is etched or implanted onto the wafer surface material.

The *reticle* is a quartz plate that contains the pattern to be reproduced on the wafer, just as the negative of a camera film has the pattern for a photograph. This pattern may contain a single die or several die. A *photomask,* often called a *mask* and often used interchangeably with the term reticle, is a quartz plate that contains the full die array needed to define one process layer for the entire wafer. For this text, reticle refers to the pattern for a die or set of die, whereas mask refers to the entire array or matrix of die necessary for an entire wafer layer. Since light is critical for transferring the pattern to the resist and is controlled through optics, photolithography is sometimes referred to as *optical lithography.*

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U.S. Patent 9,337,193

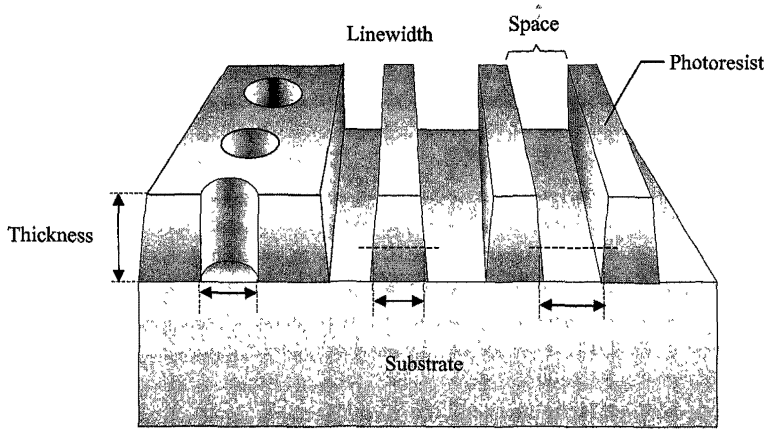
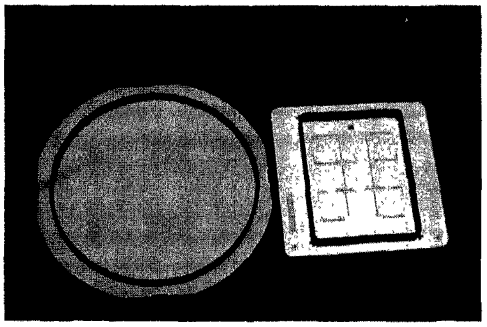


FIGURE 13.2 Three Dimensional Pattern in Photoresist

Advanced CMOS ICs can have up to 30 mask layers needed to pattern the multiple layers on a chip.[2] Each reticle has the unique pattern needed for the particular image, or feature, to be placed on the wafer surface and is stepped across the entire wafer to complete one layer. To fabricate an entire layer, the wafer must be processed into the photolithography operation and then out to undergo subsequent operations (e.g., etch or implantation).

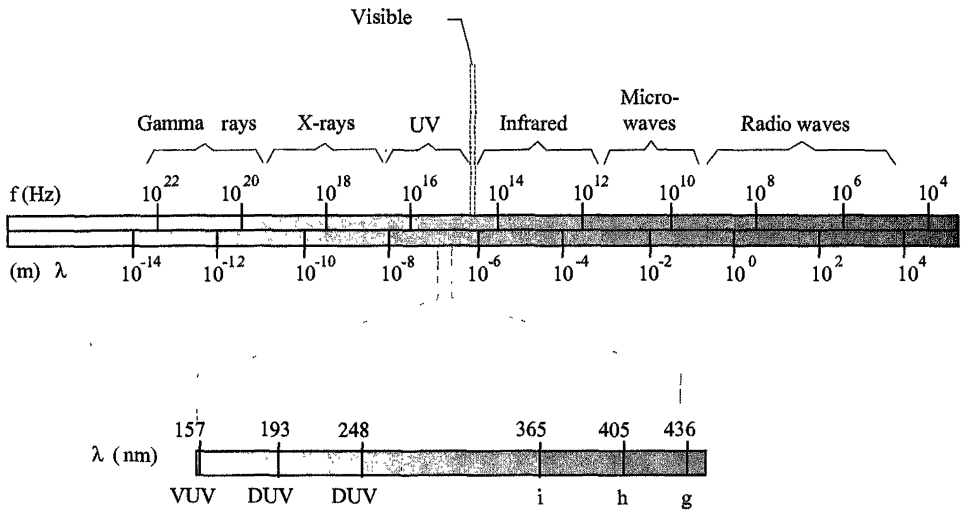


Reticle versus Photomask for Microlithography (Photo courtesy of Advanced Micro Devices)

Critical Dimension Generations ■ Microlithography has traditionally been the technology in semiconductor manufacturing that defines the critical dimension (CD) on a wafer (e.g., the polysilicon gate length on a microprocessor). Since the CD is the most difficult dimension to control during fabrication, it becomes the required dimension for other process areas to achieve. The critical dimension in photolithography is often used to describe device technology nodes or generations. Some sub-0.25 μm technology nodes are 0.18 μm, 0.15 μm, and 0.1 μm. The ability to reduce the critical dimension permits more die to be placed on a single wafer, thus lowering fabrication costs significantly and improving profitability.

Light Spectrum ■ Energy is required to activate the photoresist and transfer the pattern from the reticle. The source of energy is in the form of radiation, typically an ultraviolet (UV) light source. Light-sensitive photoresists are designed to chemically respond to a certain UV wavelength. UV light has been the most common energy source for photolithography patterning and this will probably continue for the near future (including devices fabricated at the 0.10-μm technology node and possibly lower).

The electromagnetic spectrum is used to introduce the UV light spectrum of most interest for photolithography, as shown in Figure 13.3 on page 338. The different UV wavelengths important for photolithography are shown in Table 13.1 on page 338. In general, deep UV (DUV) describes wavelengths less than 300 nm. Additional details about light and the UV spectrum for photolithography will be provided in Chapter 14.



Common UV wavelengths used in optical lithography.

FIGURE 13.3 Section of the Electromagnetic Spectrum

TABLE 13.1 Important UV Wavelengths for Photolithography Exposure

UV Wavelength (nm)	Wavelength Name	UV Emission Source
436	g-line	Mercury arc lamp
405	h-line	Mercury arc lamp
365	i-line	Mercury arc lamp
248	Deep UV (DUV)	Mercury arc lamp or krypton fluoride (KrF) excimer laser
193	Deep UV (DUV)	Argon fluoride (ArF) excimer laser
157	Vacuum UV (VUV)	Fluorine (F_2) excimer laser

Resolution ■ An important performance measurement in photolithography is the resolution of each image. *Resolution* is the ability to differentiate between two closely spaced features on the wafer surface. The actual dimensions of the patterned images on the wafer are the feature sizes. The minimum feature size dimension is the critical dimension (CD), such as 0.18 μm. However, this does not mean that every feature on the wafer has exactly this CD. On a critical layer, there are critical dimensions, such as a contact opening in the first interlayer dielectric or the polysilicon gate length, and other features that are noncritical and larger than the CD. Resolution is important for critical dimensions.

Over the past 30 years, the CD in wafer fabrication has decreased at about 11% per year. The reduction of device feature sizes has been done to achieve improved performance from device scaling, increased circuit density and decreased die size. However, the CD can only be reduced as much as the photolithography process will permit. An important challenge of lithography for achieving the smaller resolution has been the need to reduce the wavelength of the exposing light to be about the same length as the CD (to be discussed in Chapter 14).

Overlay Accuracy ■ As we shall see in Chapter 14, photolithography requires precise alignment between the pattern on the mask and the existing features on the wafer surface. This quality measure is known as *overlay accuracy.* Alignment is critical because the mask pattern must be precisely transferred to the wafer from layer to layer (see Figure 13.4). Since multiple masks are used during patterning, any overlay misalignment contributes to the total placement tolerances between the different features on the wafer surface. This condition is known as the *overlay budget.* A large overlay budget essentially reduces the circuit density, which limits device feature sizes and, therefore, IC performance.

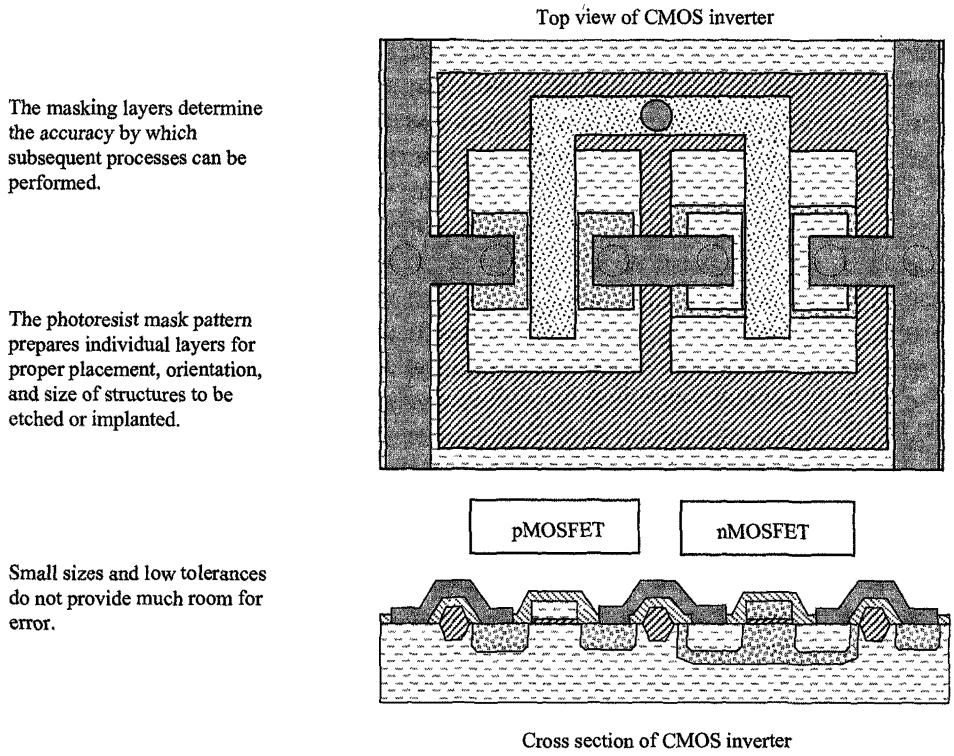


FIGURE 13.4 Importance of Mask Overlay Accuracy

Different types of misalignments affect the overlay budget. Misregistration is caused by poor alignment between the mask and the wafer. *Runout* is a net difference in the distance from die to die.[3] It can be caused by temperature variations. These types of misalignment are controlled in modern alignment systems by global wafer alignment and site-to-site alignment schemes (discussed in Chapter 14).

Process Latitude ■ There are many process variables involved in photolithography. Examples of process variables are equipment settings, types of materials, human performance, machine alignments, and the stability of materials over time. *Process latitude* represents the capability of the photolithography process to consistently produce products that meet the specified requirements. The objective is to achieve the largest process latitude possible to make the process more capable of producing good parts. Process engineers define the settings for the different process variables to obtain the largest process latitude. For photolithography, high process latitude means critical dimensions can be met within the specified limits even with all the process variations encountered during production.

PHOTOLITHOGRAPHY PROCESSES

Photolithography consists of two basic types of processes: negative and positive lithography. *Negative lithography* prints a pattern on the wafer surface that is the opposite of the pattern in the mask. *Positive lithography* prints a pattern on the wafer that is the same pattern as that on the mask. The major difference between these two basic processes is the type of photoresist used. How the photoresist material reacts when exposed to light depends on whether it is a negative or a positive resist material.

Negative Lithography

The primary feature of negative lithography is that the photoresist will become insoluble and harden by crosslinking when exposed to light. Once hardened, the crosslinked resist cannot be washed away in solvents. Resists of this type are known as *negative resists* because the image formed in the

resist is the negative of the pattern found on the reticle (see Figure 13.5). Negative resists were the earliest types of photoresist used in semiconductor photolithography.

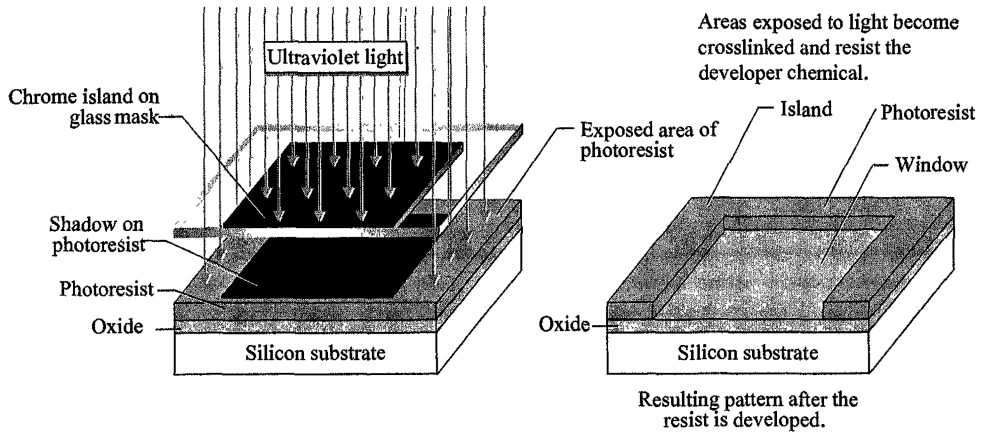


FIGURE 13.5 Negative Lithography

It can be seen in the diagram in Figure 13.5 that the mask for the negative resist is a transparent plate of quartz. The dark portion of the mask is a thin film of chromium deposited and patterned to form the desired mask artwork. The chrome is opaque (not transparent) and does not permit the passage of the ultraviolet light. For a negative resist, the regions underneath the opaque chrome of the mask are not exposed to light and therefore remain unchanged. The resist remains soft and dissolves when exposed to the developer chemical. UV light passes through the clear areas of the mask and hardens the resist so that it does not dissolve in the subsequent developer chemical. In this manner, the negative resist has a pattern that is the opposite of the pattern on the mask.

Positive Lithography

In positive lithography, the pattern printed on the wafer surface has the same image as the pattern on the mask. The areas of the resist exposed to the UV light undergo a photochemical reaction and become soluble and soften in the developer. In this manner, regions of the positive resist exposed to light are removed in a developer solution, whereas resist not exposed to light underneath the opaque mask pattern remains on the wafer (see Figure 13.6). This type of resist is referred to as a *positive resist* because the image formed in the resist is the same pattern formed on the reticle. The resist that remains was already hardened before light exposure and remains on the wafer surface to protect the top layer during subsequent processing, such as etch. The resist is removed when the follow-on processing is done. During the 1970s, positive resist became the dominant resist type for submicron microlithography and remains so today (see the following section for a discussion of the benefits from positive resist).

The pattern transferred into the photoresist can be considered a window or an island. A summary of the results from the two different types of masks and photoresists is shown in Figure 13.7.

Another way to describe masks is by their outward appearance. A mask is referred to as a *dark-field mask* if much of the quartz plate is coated with chrome. A *clear-field mask* is one that has very thin patterns of chrome with large areas of clear quartz. When comparing masks for positive and negative lithography, if a clear-field mask is required for a specific masking layer using a positive resist, then a dark-field mask of the same pattern would be used for negative resist.

Using positive lithography as an example, some common dark-field masks are the masks that are used prior to source/drain implant, LDD implant, and contact etch. A clear-field mask is used for applications such as preceding gate etch and metal interconnect etch. Figure 13.8 illustrates examples of the two types of masks based on positive photoresist lithography.

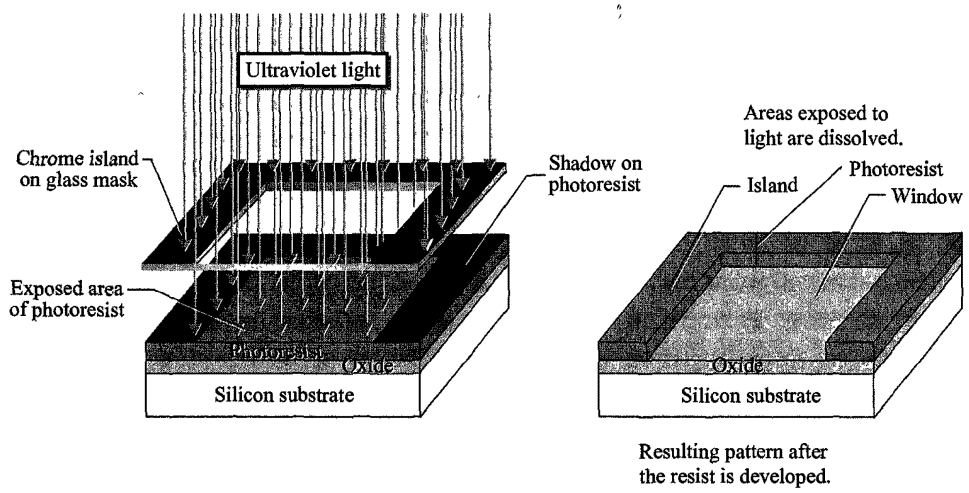


FIGURE 13.6 Positive Lithography

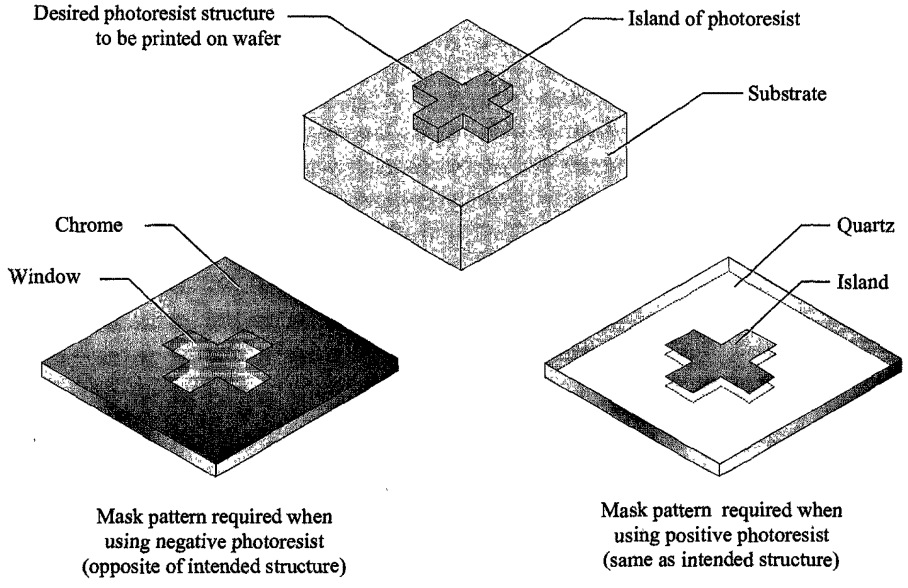


FIGURE 13.7 Relationship Between Mask and Resist

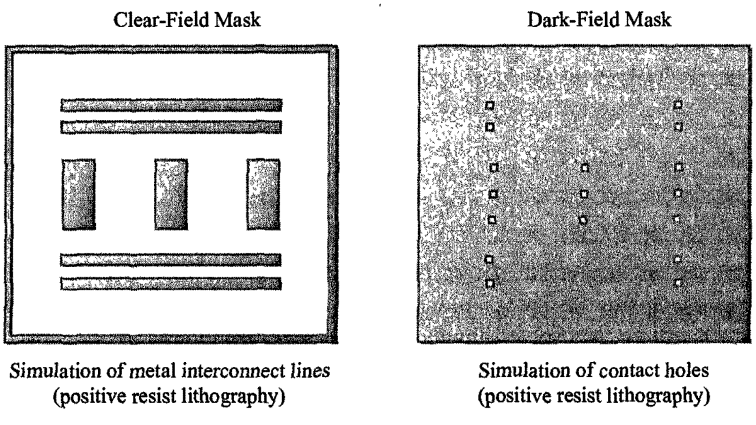


FIGURE 13.8 Clear-Field and Dark-Field Masks

EIGHT BASIC STEPS OF PHOTOLITHOGRAPHY

Photolithography is a complex process with many variables contributing to its process latitude, such as reduced feature size, alignment tolerance, number of masking layers, and cleanliness of the wafer surface. For convenience, we can divide the patterning process of photolithography into an eight-step procedure (see Table 13.2). Figure 13.9 provides a pictorial overview of the eight process steps. In the wafer fab these steps are often referred to as operations. Breaking the large photo process into these eight steps simplifies the various aspects of microlithography. This chapter will first provide a short overview of the eight basic steps, followed by an in-depth analysis of the materials, equipment, and processes used in each photolithography step. The in-depth analyses of the steps are covered at the end of this chapter and in the following three chapters. Table 13.2 indicates the specific steps that are covered in a chapter.

TABLE 13.2 Eight Steps of Photolithography

Step	Chapter
1. Vapor prime	**13**
2. Spin coat	**13**
3. Soft bake	**13**
4. Alignment and exposure	14
5. Post-exposure bake (PEB)	15
6. Develop	15
7. Hard bake	15
8. Develop inspect	15

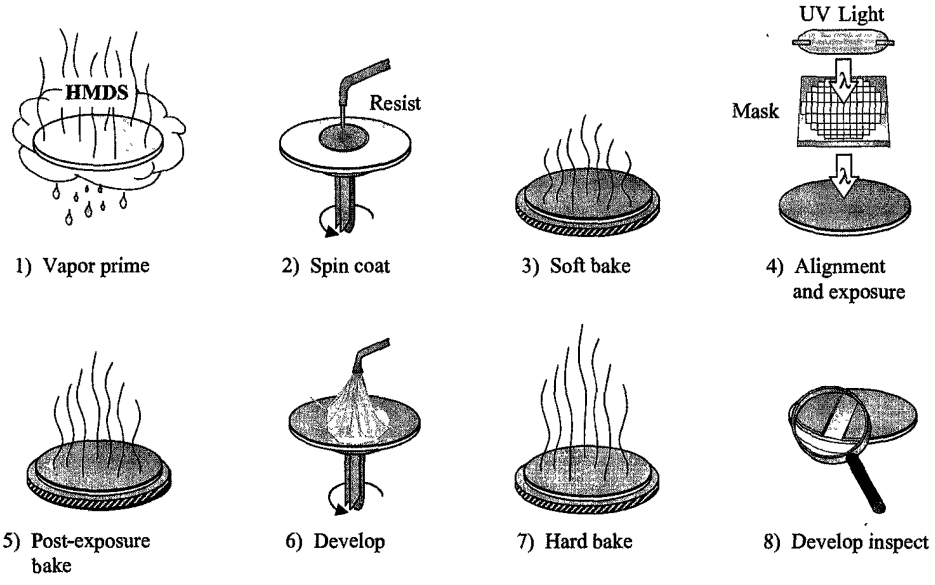
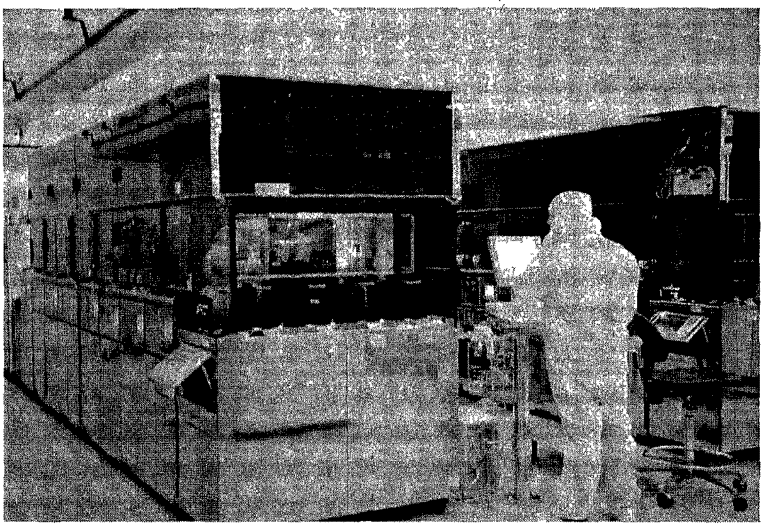


FIGURE 13.9 Eight Steps of Photolithography

The photolithography process has undergone significant equipment integration. Automated equipment, referred to as a *coater/developer track system,* or *tracks,* employs robots, automated material handling, and computers to perform all eight steps without human intervention. Integrated tracks offer many benefits over the previous stand-alone manual tooling for photolithography. This integration improved process control by controlling delays between process steps, processing wafers efficiently, increasing flexibility, reducing contamination due to environmental control and minimal operator handling, and increasing safety due to reduced operator exposure to chemicals.



Photolithography Track System
(Photo courtesy of Advanced Micro Devices)

Step 1: Vapor Prime

The first step in photolithography is to clean, dehydrate, and prime the surface of the wafer. The purpose of these steps is to promote good adhesion between the photoresist and the wafer surface.

Wafer cleaning may involve a wet clean and DI water rinse to remove contaminants. Most wafer cleaning is performed before entering the photolithography workbay. A dehydration dry bake is done in a closed chamber to drive off most of the adsorbed water on the surface of the wafer. The wafer surface must be clean and dry. Immediately after the dehydration bake, the wafer is primed with hexamethyldisilazane (HMDS), which acts as an adhesion promoter.

Step 2: Spin Coat

After priming, the wafer is coated with the liquid photoresist material by a spin coating method. The wafer is mounted on a vacuum chuck, which is a flat metal or teflon disc that has small vacuum holes on its surface to hold the wafer. A precise amount of liquid photoresist is applied to the wafer and then the wafer is spun to obtain a uniform coating of resist on the wafer (see Figure 13.10).

Different resists require different spin coating conditions, such as an initial slow spin (e.g., 500 rpm), followed by a ramp up to a maximum rotational speed of 3,000 rpm or higher. Some important quality measures for photoresist application are time, speed, thickness, uniformity, particulate contamination, and resist defects such as pinholes.

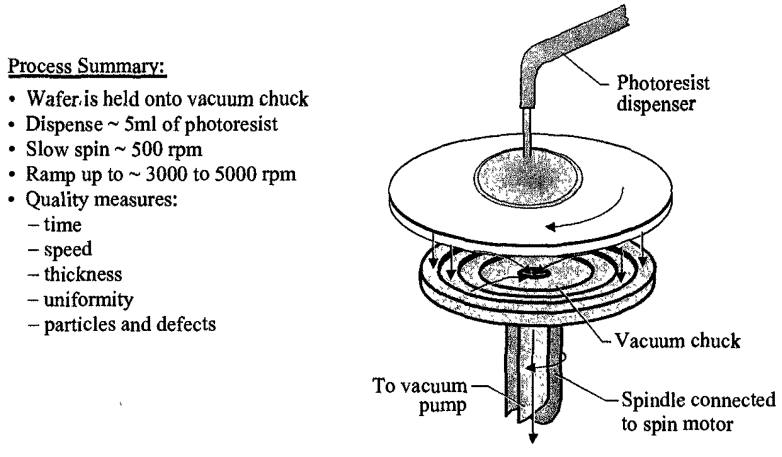


FIGURE 13.10 Spin Coat

Step 3: Soft Bake

After the resist has been applied to the wafer surface, it must undergo a soft bake. The purpose of this bake is to drive off most of the solvent in the resist. The soft bake process improves adhesion, promotes resist uniformity on the wafer, and yields better linewidth control during etching. Typical soft bake temperatures are 90 to 100°C for 30 seconds on a hot plate, followed by a cooling step on a cool plate to achieve wafer temperature control for uniform resist characteristics.

Step 4: Alignment and Exposure

The next step is referred to as alignment and exposure. The mask is aligned to the correct location of the resist-coated silicon wafer. The wafer surface could be bare silicon but usually has an existing pattern previously defined on its surface. Once aligned, the mask and wafer are exposed to controlled UV light to transfer the mask image to the resist-coated wafer (see Figure 13.11). The light energy activates the photosensitive components of the photoresist. Important quality measures for alignment and exposure are linewidth resolution, overlay accuracy, and particles and defects.

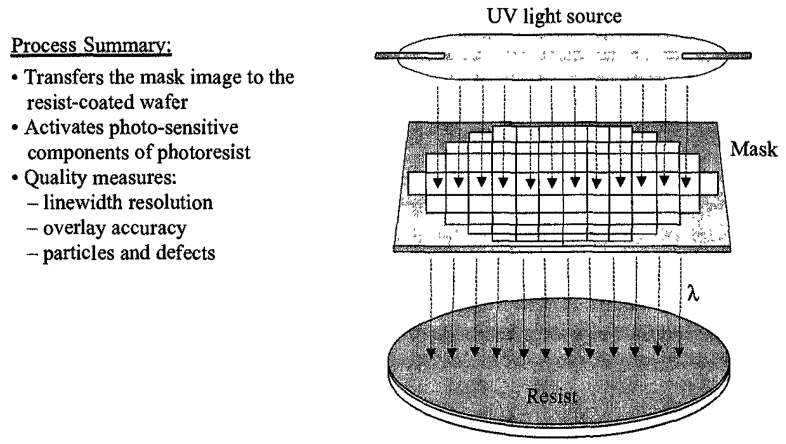


FIGURE 13.11 Alignment and Exposure

Step 5: Post-Exposure Bake (PEB)

There is a post-exposure bake on a hot plate at 100 to 110°C that is necessary for the deep UV (DUV) resists. This bake follows immediately after the photoresist exposure. A few years ago, it was an optional step for non-DUV conventional resists, but it has become a virtual standard even for conventional resists.

Step 6: Develop

Develop is the critical step for creating the pattern in the photoresist on the wafer surface. The soluble areas of the photoresist are dissolved by liquid developer chemicals, leaving visible patterns of islands and windows on the wafer surface. The most common methods for development are spin, spray, and puddle (see Figure 13.12). Following development, the wafers are rinsed in deionized (DI) water and then spin-dried.

Step 7: Hard Bake

A post-development thermal bake, referred to as hard bake, is required to evaporate the remaining photoresist solvent and improve the adhesion of the resist to the wafer surface. This is the critical step for stabilizing the resist for the following etch or implant processing. The hard bake temperature for positive resists is about 120 to 140°C. This is a higher temperature than soft bake, but it cannot be too high or else the resist will flow and deform the pattern.

Process Summary:

- Soluble areas of photoresist are dissolved by developer chemical
- Visible patterns appear on wafer
  - windows
  - islands
- Quality measures:
  - line resolution
  - uniformity
  - particles and defects

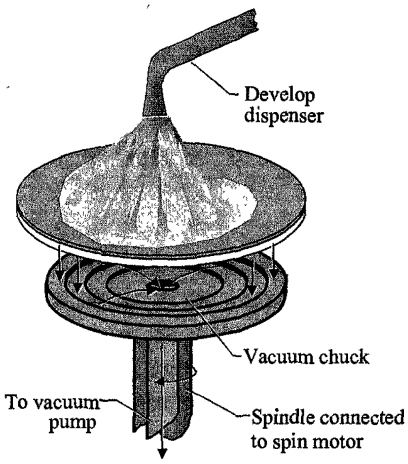


FIGURE 13.12 Photoresist Development

Step 8: Develop Inspect

Once the resist is patterned on the wafer, an inspection is done to verify the quality of the resist pattern. The inspection system is nearly always automated for patterning on highly integrated critical layers. The purpose of this inspection is twofold: to identify wafers that have quality problems with the resist and to characterize the performance of the photoresist process to make improvements. If the resist is determined to be defective, it can be removed through resist stripping and the wafer can be reprocessed.

The goal of the photolithography process, as in any manufacturing process, is a defect-free product. However, it would be catastrophic to not inspect and leave defects in the resist. Develop inspect is one of the few areas in the wafer fabrication process where errors can be detected and corrected. Once defective wafers are moved to the next patterning step, usually etch, then there is no further chance to correct mistakes. If a wafer is etched incorrectly, it has a fatal defect, is considered scrap, and is of no further value to the company. This is why inspection data to characterize and improve the photoresist process is so important.

VAPOR PRIME

To successfully manufacture integrated circuits, wafers must be meticulously clean at all steps of the wafer fabrication process. Cleaning steps are necessary due to the inevitable contamination that occurs during storage and handling between process steps. Wafer surface preparation is critical to achieving a high-yield photolithography process, since many types of defects can be traced back to contaminated wafers.

Wafer Cleaning

The first step of photolithography is to clean and prepare the surface of the wafer, usually before the wafers arrive at the photolithography workbay. Wafer contaminants and the appropriate cleaning processes were discussed in Chapter 6. As a review, undesirable surface contaminants are particles, metallic impurities, organic contamination, and native oxide. There are many sources of these contaminants, including people, process chemicals, process equipment, packaging and storage, wafer handling methods, and environmental conditions. Thin layers of contaminants on the wafer can consist of ionic (metallic) impurities and atomic and polymeric (organic) layers, which are all difficult to detect. Refer to Chapter 6 for a discussion of types of contamination and cleaning processes.

One of the major effects of contaminants on the wafer surface during photolithography is poor adhesion of the photoresist to the wafer. This condition creates a yield problem of resist lifting during development or the subsequent etch operation. Resist lifting leads to undercutting of the underlying film layer during the etch process (see Figure 13.13 on page 346). Particulate contamination in the resist can lead to uneven resist coating and pinholes in the resist.

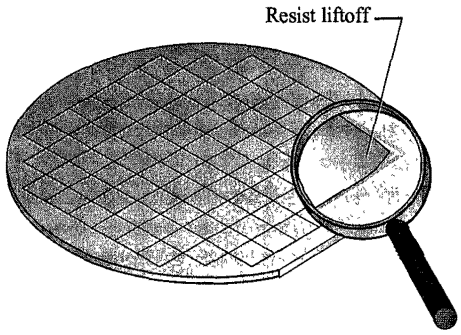


FIGURE 13.13 Effect of Poor Resist Adhesion Due to Surface Contamination

Often wafers entering the photolithography process will have just completed an oxidation or deposition operation and will be in a clean condition. The best situation is to coat these clean wafers with resist as soon as possible. To achieve this, some fabs will place time limits on how long wafers can wait before undergoing photolithography processing to minimize contamination adsorption on the wafer surface.

Dehydration Bake

Silicon wafers readily adsorb moisture on their surface. A wafer surface exposed to moisture is called *hydrophilic* (also called *hydrated*). For resist adhesion, it is important to have a dry, or *hydrophobic,* wafer surface. A hydrophobic wafer is also called *dehydrated* and promotes good resist adhesion. One way to maintain a hydrophobic wafer surface is to coat the wafer with photoresist as quickly as possible after leaving the previous process. Another method is to maintain a controlled room humidity below 50% relative humidity.

Due to the criticality of having a dry wafer surface for resist adhesion, a *dehydration bake* is usually done before priming and resist spin coating. The actual bake temperature varies, with 200 to 250°C commonly used. Dehydration bake temperatures usually do not exceed 400°C, and often cannot attain this temperature due to the temperature sensitivity of the underlying layers (e.g., aluminum). Total wafer surface dehydration occurs at temperatures above 750°C. However, moisture from the atmosphere is quickly reabsorbed back on the wafer surface during cooling; therefore, there is little benefit to heating to this temperature.[4]

Dehydration bake is typically done in a convection oven with a dry inert gas (such as nitrogen) or in a vacuum oven. It can also be done on a hot plate, which is followed by a cold plate to quickly reduce the wafer temperature. Since nearly all wafer fabs use automated wafer track systems, the dehydration bake process is integrated into the wafer handling system.

Wafer Priming

Right after dehydration bake the wafer is primed with *hexamethyldisilazane (HMDS),* which serves as an adhesion promoter. This process is similar to a paint primer being used to prepare wood for a coat of paint. The HMDS reacts with the silicon surface to tie up molecular water, while also forming a bond with the resist material. It essentially serves as a link between the silicon and the resist so that these materials become chemically compatible.

An important aspect of wafer priming is that the wafer should be coated with resist quickly after the prime operation to minimize moisture problems. It is recommended that coating be performed no later than 60 minutes after completing the priming step.[5] This priming is typically controlled by software on the automated track system.

Priming Techniques ■ HMDS may be applied by puddle, spray, and vapor methods. The method used to prime the wafer is integrated onto the wafer track system.

Puddle Dispense and Spin. The puddle dispense and spin method is used for single wafer processing (see Figure 13.14). The temperature and volume are easily controlled and the system requires a drain and exhaust. This method consumes a large amount of HMDS, which can be a disadvantage.

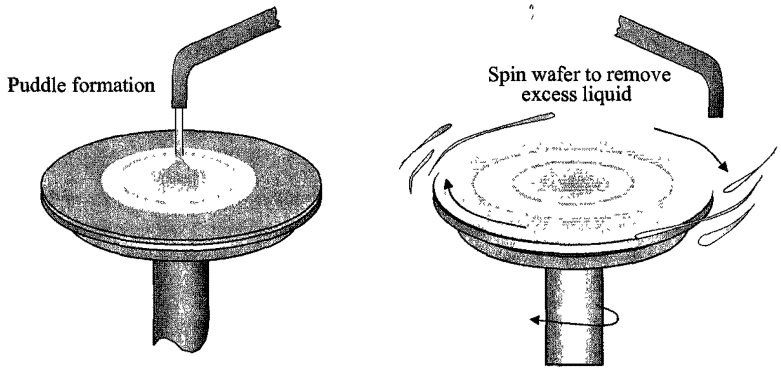


FIGURE 13.14 HMDS Puddle Dispense and Spin

Spray Dispense and Spin. Spray dispense uses a nozzle spray to deposit a fine mist of HMDS on the wafer surface. An advantage of this approach is the spray will assist in particle removal from the wafer surface. A disadvantage is a longer application time and a high consumption of HMDS.

Vapor Prime and Dehydration Bake. The most common method for applying HMDS to the wafer surface is with a *vapor prime coating*. The vapor priming is done at a typical temperature and time of 200 to 250°C for 30 seconds. An advantage of vapor priming is there is no contact with the wafer, which reduces the possibility of particulate contamination from the liquid HMDS. Vapor priming also minimizes consumption of HMDS. Adequate priming of the wafer surface is confirmed with a contact angle meter (see Chapter 7).

One approach is to first perform a dehydration bake followed by a vapor prime of single wafers by thermal conduction heating on a hot plate (see Figure 13.15). The wafer holder is typically made of quartz. Advantages of this approach are inside-out baking of the wafer, low defect density, uniform heating, and repeatability.

Process Summary:

- Dehydration bake in enclosed chamber with exhaust
- Hexamethyldisilazane (HMDS)
- Clean and dry wafer surface (hydrophobic)
- Temp ~ 200 to 250°C
- Time ~ 60 sec.

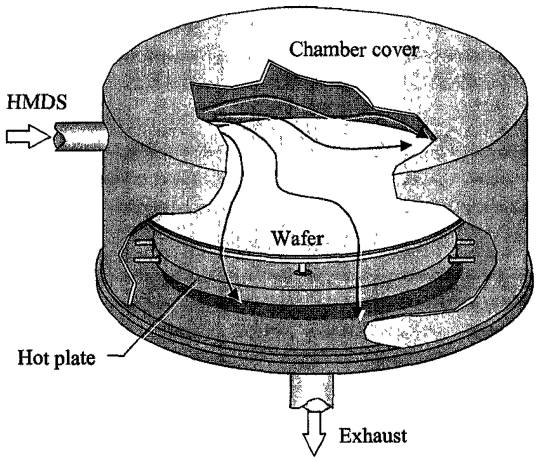


FIGURE 13.15 HMDS Hot Plate Dehydration Bake and Vapor Prime

Another method for dehydration bake in conjunction with vapor priming is to use a vacuum chamber with a nitrogen carrier gas. This is a batch process where the wafers are placed in a quartz holder in the oven chamber. The heated chamber is evacuated and back-filled to a preset pressure with HMDS vapor in the nitrogen carrier gas. At the completion of the pretreatment, the oven is evacuated and back-filled with nitrogen at atmospheric pressure.

SPIN COAT

Once the wafer surface has been cleaned, dehydrated, baked, and primed, it is ready for the application of photoresist. Photoresist is applied by spin coating, where the wafer is spun to form a thin film of resist on the wafer surface. Before considering the photoresist spin process, we will review the different chemistries of photoresists.

Photoresist

Photoresist is an organic compound that experiences a change in solubility in a developer solution when exposed to ultraviolet (UV) light. Photoresists used in wafer fabrication are applied to the wafer surface as a liquid but dried into a film. The purpose of photoresist in wafer fabrication is:

1. To transfer the mask pattern to the resist on the top layer of the wafer surface.
2. To protect the underlying material during subsequent processing (e.g., etch or ion implantation barrier).

As successive generations of device circuit density have reduced critical dimensions, resist technology has undergone improvements in order to transfer the submicron linewidth patterns to the wafer surface. These resist improvements include:

1. Better image definition (resolution).
2. Better adhesion to semiconductor wafer surfaces.
3. Better uniformity characteristics.
4. Increased process latitude (less sensitivity to process variations).

Types of Photoresists ■ The two major types of optical photoresists are negative resist and positive resist. This classification is based on how the resist material responds to UV light. For a negative resist, the UV-exposed regions become crosslinked and hardened. This makes the exposed photoresist less soluble in the developer solution; the photoresist is not removed in the developer liquid. A negative mask image is patterned in the resist. For a positive resist, UV-exposed regions of the resist become more soluble and a positive mask image appears in the resist. A positive resist breaks down during exposure to light and the exposed areas are easily washed away in the developer solution.

We can also group photoresists based on the smallest CD the resist can pattern. A major group is conventional resists capable of patterning linewidth dimensions down to and including 0.35 μm. A new resist technology introduced in the late 1990s was chemically amplified (CA) resist for deep UV (DUV) wavelengths (see the following section). Chemically amplified resist technology can pattern fine-geometry CDs of 0.25 μm and below in high-volume production. This patterning has also been demonstrated in a lab environment for a CD of 0.05 μm. For fabrication of high-performance ICs, a wafer may be patterned with conventional resist for noncritical layers and CA resist for critical layers. We will refer to all optical resists that are not chemically amplified as conventional resists. There are also special resists used for the nonoptical photolithography techniques of e-beam pattern reproduction and X-ray exposure systems (discussed in Chapter 15). Our focus will be on the conventional and chemically amplified optical resists used in wafer fabrication.

Negative Versus Positive Resists ■ As previously outlined, negative photoresist hardens when exposed to light and becomes insoluble. When developed, the image is the opposite of the original mask pattern. Positive photoresist softens when exposed to light and becomes soluble. When developed, the image is the same as the original mask pattern.

The earliest resists in semiconductor microlithography were primarily negative resists until the mid-1970s. Negative resists of this era exhibited good adhesion to the wafer substrate and good resistance to etching. However, due to the swelling and distortion during develop, negative resists typically have a resolution limit of about 2 μm.[6] As long as the circuit linewidth CD remained above this dimension, then negative resists were acceptable. With the introduction of VLSI and ULSI technology and their associated micron and submicron circuit image sizes, the negative resist

type was replaced by positive resist. Positive resist had been around for many years, but it had poorer adhesion and its capability for improved resolution was not needed.

This change in the 1970s from negative to positive resist presented a fundamental change in the photolithography process. It required changing the polarity of the photomasks, meaning clear-field regions became dark (opaque) and dark-field regions became transparent. However, this change did not simply involve changing the fields in the mask-making process. Mask dimensions print differently with the two resists. As an example, for a negative resist with a clear-field mask, the dimensions in the resist are smaller than the corresponding photomask dimensions because of light scattering (diffracting) around the image. It is the opposite for a positive resist and a dark-field mask, as diffraction will tend to enlarge the image in the resist. Thus, changing from negative to positive resist required new masks and different adjustments to the mask during construction. Positive resists remain the dominant type of resist today.

Photoresist Physical Properties

In its most elemental form, photoresist is a polymer solution in an organic solvent. The photoresist must perform well under all the different process conditions, including coating, spinning, baking, develop, ion implantation, and etch. There are many different types of photoresists used in wafer applications, each with its own physical properties that are directly related to the photolithography process requirements. A particular resist is selected based on the following physical properties:

- Resolution
- Contrast
- Sensitivity
- Viscosity
- Adhesion
- Etch resistance
- Surface tension
- Storage and handling
- Contaminants and particles

Resolution. Resolution is the ability to differentiate between two or more closely spaced patterned features on the wafer surface. A practical way to interpret resolution is by the smallest feature that can be printed on a wafer and meets specified quality requirements. The smaller the critical dimension produced, the better the resolution capability of the resist and the photolithography system.

Contrast. The *contrast* represents the sharpness of the transition from exposure to non-exposure in photoresists (see Figure 13.16). Contrast represents the ability of the resist to become exposed only in those areas defined by the clear region of the photomask. It is desirable to have high-contrast to produce vertical resist sidewalls.

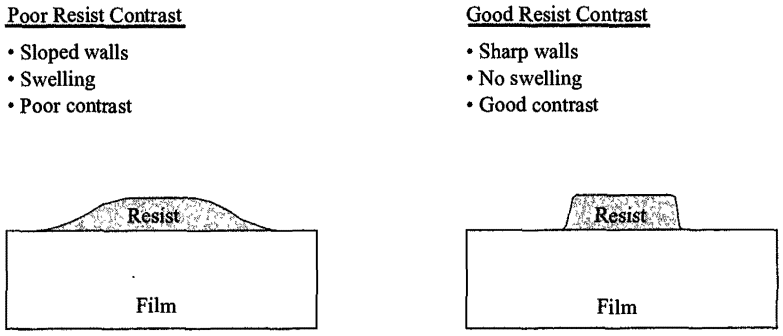


FIGURE 13.16 Resist Contrast

Sensitivity. *Sensitivity* is the minimum amount of light energy (measured in millijoules/cm^2 or mJ/cm^2) at a certain wavelength that is needed to produce a good pattern in the photoresist on the wafer surface. The amount of light energy supplied to a resist is commonly called the *exposure dose.* Sensitivity is important for new resists because of the low energy levels emitted at the shorter UV wavelengths (e.g., deep UV). Resist manufacturers sensitize their resist formulations for maximum absorption in the areas of optimum energy output of the radiation sources available.

Viscosity. The *resist viscosity* represents a quantitative measure of flow characteristics for the liquid resist. Viscosity is time-dependent in that it increases as the solvent in the resist evaporates during usage. Viscosity is important because it affects resist thickness and the uniformity of the resist over the wafer surface topography such as steps and small gaps. As viscosity increases, the resist has less tendency to flow and its thickness on the wafer increases. A thicker resist provides better step coverage and better dry etch resistance but makes the resolution of small openings more difficult. Thick resist also has less probability of having pinholes, which are microscopically small voids that pass completely through the resist to the substrate material. Pinholes are undesirable for subsequent etch processing because the etch chemicals can pass through the small voids and damage the underlying substrate material. Low viscosity resist has more tendency to flow and will lead to thinner coverage of the wafer surface.

Solid content represents the amount of the liquid resist that would remain as a solid if the solvent were evaporated. Specific gravity (SG) is a measure of the resist density and is related to the solid content in the resist. A higher SG means there are more solids in the resist, which indicates a higher viscosity and lower tendency to flow.

Viscosity is measured in the unit of poise. Photoresist viscosity is measured in centipoise (1/100th of a poise), or cps. Viscosity may be reported in centistokes (cs), which is the kinematic viscosity, whereas the centipoise is the absolute viscosity. The kinematic viscosity is found by dividing the absolute viscosity (centipoise) by the density (specific gravity). For instance, a 70-cps resist with an SG of 0.8 would produce a kinematic viscosity of:

$$\begin{aligned}\text{Kinematic viscosity} &= [\text{absolute viscosity (cps)}] \,/\, (\text{specific gravity}) \\ &= (70 \text{ cps}) \,/\, 0.8 \text{ SG} \\ &= 87.5 \text{ centistokes (cs)}\end{aligned}$$

Adhesion. *Resist adhesion* describes how strongly the resist sticks to the substrate. The resist must adhere to many different types of surfaces, including silicon, polysilicon, silicon dioxide (doped and undoped), silicon nitride, and different metals. Lack of resist adhesion leads to distorted patterns on the wafer surface. The resist adhesion must withstand exposure, development, and subsequent processing (e.g., etch and ion implantation).

Etch Resistance. The resist film must maintain its adhesion and protect the substrate surface from the subsequent wet and dry etch processes (see Chapter 16). This property is known as *etch resistance*. Some dry-etch processes are done at higher temperatures (e.g., 150°C), which require a resist that has thermal stability to maintain its shape.

Surface Tension. *Surface tension* refers to the molecular attraction forces in a liquid that tend to pull surface molecules toward the body of the liquid. An example of high surface tension is water beading up on a waxed automobile surface (see Figure 13.17). Resist has molecular forces that create a relatively high surface tension so that the resist molecules hold together during the various process steps. At the same time, the surface tension of resist must be low enough to provide for good flow and wafer coverage during application.

Storage and Handling. Photoresist chemicals are activated in the presence of energy, either as light or heat, which requires carefully controlled storage and usage conditions. Resists are specified with a shelf life and storage temperature environment. Crosslinking of negative resists and sensitizer-delay of positive resists can occur with extended storage time or elevated temperature. If the solvent on the resist was allowed to evaporate due to an unsealed container, the viscosity would change rapidly and solids could precipitate from the liquid.

Resist manufacturers have developed automated dispense mechanisms to control contamination and evaporation. The resist containers are often a closed system, such as collapsible pouches that are opaque to light and loaded directly into the wafer tracks to avoid opening in the atmosphere.

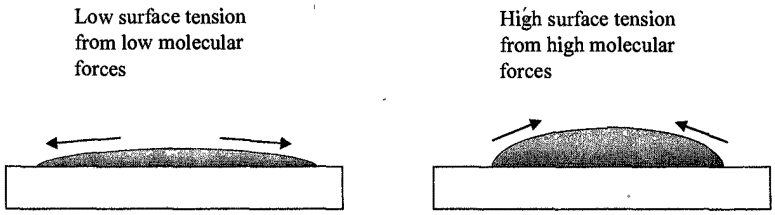


FIGURE 13.17 Surface Tension

Contaminants and Particles. As with any chemical used in wafer fabrication, the purity of the resist material is important. The most critical purity concerns for resist are mobile ionic contaminants (MICs) and particles. The resist is applied to the wafer surface material and can easily introduce detrimental contamination to the wafer. To control contamination and particles, resist suppliers meet extremely tight filtration and packaging procedures. Localized point-of-use resist filtration with membrane filters just before resist application can control contamination in the resist to < 1 ppb.

Conventional I-Line Photoresists

Conventional i-line photoresists for optical microlithography are those suitable for i-line UV wavelengths (365 nm), which corresponds to noncritical layers with a CD down to 0.35-μm. This condition includes both positive and negative resists, although positive resists are the most common. Note that the characteristics of i-line photoresist also represent the same basic properties for resists used at g-line (436 nm) and h-line (405 nm) wavelengths.

I-line photoresists are composed of three basic components,[7] and frequently have a fourth component of special additives (see Figure 13.18):

1. Resin (polymer material)
2. Sensitizer
3. Solvent
4. Additives (optional)

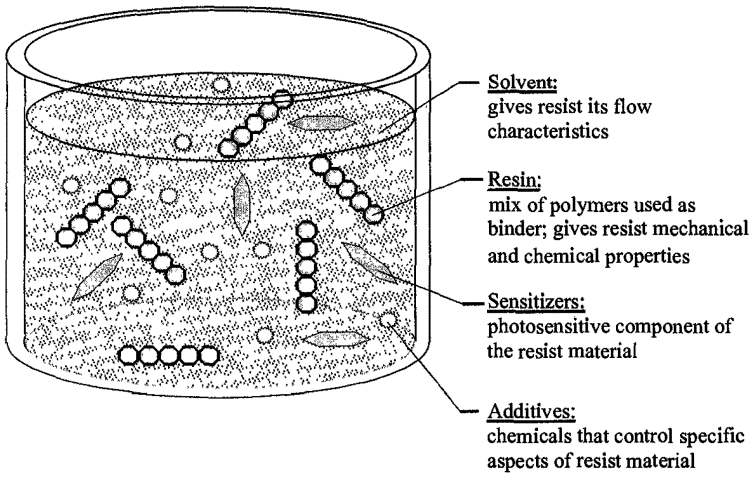


FIGURE 13.18 Components of Photoresist

Resin. The resist resin is an inert matrix of polymers (large organic molecules containing carbon, hydrogen, and oxygen) which is used as a binder to hold together the different materials in the resist. Resin gives the resist its mechanical and chemical properties, such as adhesion, etch resistance film thickness, flexibility, and thermal flow stability. The resin material is typically insensitive to light, meaning it does not undergo chemical change upon exposure to UV light.

Sensitizer. The resist sensitizer is the photosensitive component of the resist material that reacts in response to radiant energy in the form of light, especially in the UV region. The sensitizer reacts photochemically in response to light energy.

Solvent. The resist solvent keeps the resist in its liquid state until it is applied to the wafer substrate. Most solvents are evaporated from the resist before the exposure is done and have little effect on the photochemistry of the resist.

Additives. Resist additives are usually proprietary chemicals, which means the contents are developed by the manufacturer and not disclosed to the public for competitive reasons. Additives are used to control or modify specific chemical or light response aspects of the resist material. It also includes dyes to control the reflectivity of the resist.

Negative I-Line Photoresists ■ The resin for i-line negative resist is typically a chemically inert polyisoprene polymer that is a natural rubber. The polyisoprene is suspended in a solvent such as xylene. The resist sensitizer is a photoactive agent that releases nitrogen gas on exposure to UV light with the proper wavelength, generating free radicals that form crosslinks between the rubber molecules. This crosslinked rubber formed from UV light exposure becomes insoluble in the organic developer solution (see Figure 13.19). At the same time, the unexposed (and therefore unpolymerized) areas of the resist are rinsed away in the developer. These basic steps for crosslinking of negative resist are shown in Table 13.3.

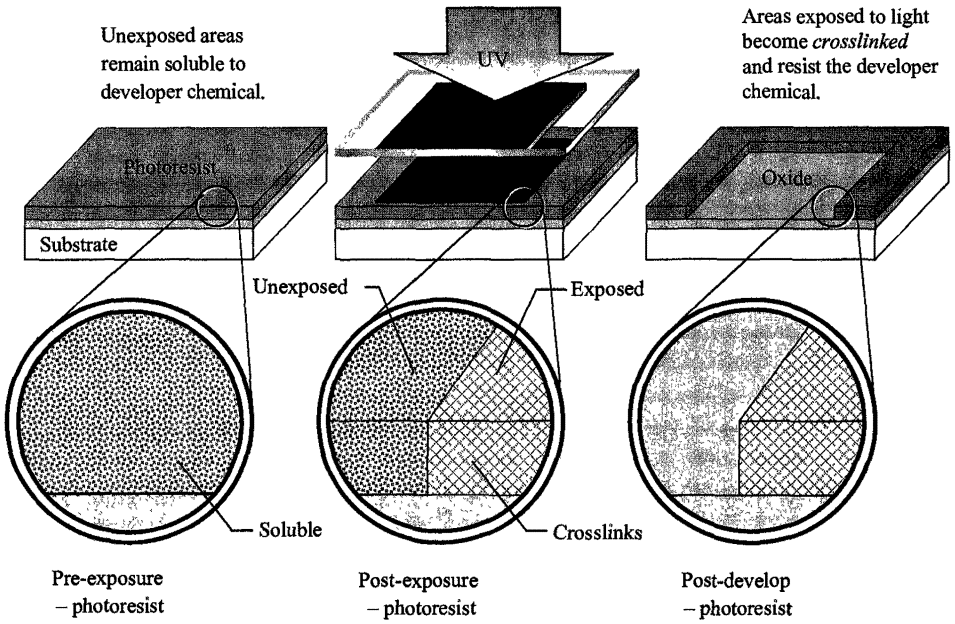


FIGURE 13.19 Negative Resist Crosslinking

TABLE 13.3 Steps to Negative Resist Crosslinking

1. Resist resin is polyisoprene rubber polymer suspended in solvent (soluble in developer solution).
2. Photoactive sensitizer agent releases N_2 during exposure.
3. Release of N_2 generates radicals.
4. Radicals polymerize resist by crosslinking rubber polymer (insoluble in developer solution).

A major disadvantage of conventional negative resists has been their solvent-induced swelling of the exposed resist regions during development. This swelling distorts the resist pattern on the wafer surface and is unacceptable for fine-geometry features with micron and submicron critical dimensions. Another disadvantage is the resist's reactivity with oxygen during UV exposure that can inhibit crosslinking. There is, however, research into new negative resist formulations that

do not swell or distort patterns.[8] A negative resist has high exposure speed (which translates into higher throughput of wafers) and good wafer adhesion.

Positive I-Line Photoresists ■ Positive i-line photoresist is the most common resist in IC photolithography. The resin material in positive i-line photoresists is a phenol-formaldehyde polymer called *novolak*. An example of a common use of novolak is the glue that binds the different layers of plywood lumber. Novolak is a long chain polymer that forms the key resist film properties, such as good adhesion and chemical resistance, making it an acceptable barrier to subsequent processes such as etch. Novolak resin dissolves in developer solution when there is no dissolution inhibitor present.

The sensitizer in positive i-line photoresist is referred to as a *photoactive compound (PAC)*, the most common being a diazonapthoquinone (DNQ). Before exposure to light, the DNQ serves as a strong dissolution inhibitor, reducing the dissolution rate. After exposure to UV light, DNQ promotes dissolution in the developer by a factor of about 100 or more (see Figure 13.20).[9] This i-line resist is often called *DNQ-novolak*, representing the mixture of diazonapthoquinone (DNQ) and novolak resin. It originally evolved from materials used to make blueprints. Note the mask in Figure 13.20 is the direct opposite of the mask used in Figure 13.19.

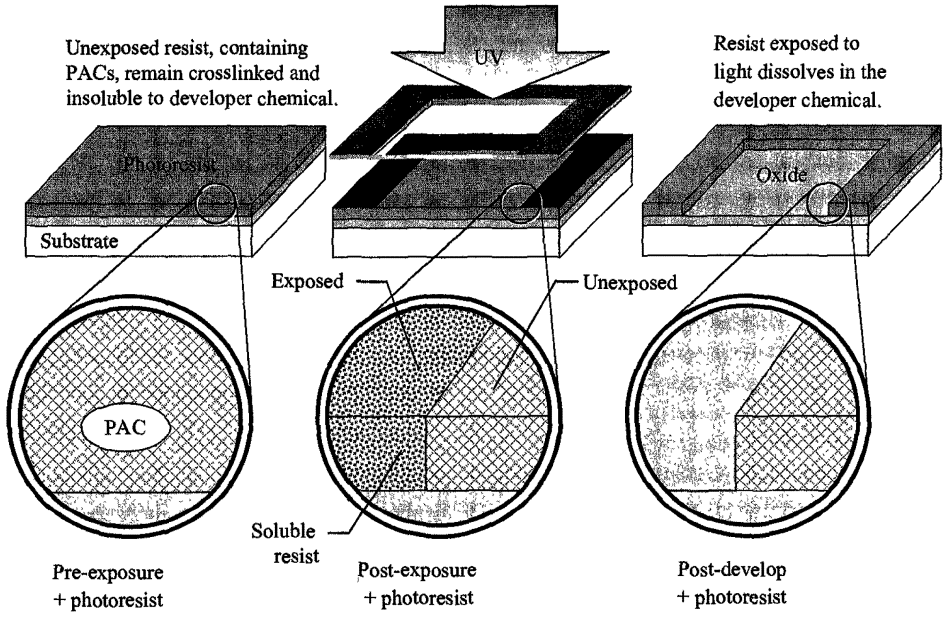


FIGURE 13.20 PAC as Dissolution Inhibitor in Positive I-Line Resist

When exposed to light energy of the proper wavelength, the diazonapthoquinones (DNQs) photochemically decompose in the resist. The exposed DNQ now becomes a dissolution promoter in exposed regions of the resist. This change is accomplished when decomposition of the DNQ creates carboxylic acid, which is highly soluble in the developer solution. In this manner, exposed positive resist changes from an insoluble to a soluble form and dissolves in the developer solution. This is the dissolution of the positive resist (see Table 13.4 on page 354). With this process, areas of the resist that correspond to transparent mask areas will dissolve, thus creating a positive image. In the DNQ resist, regions exposed to light are about 100 times more soluble in the developer than unexposed resist regions.[10]

TABLE 13.4 Steps to Positive I-line Resist Dissolution in Developer

1. Resin is phenol-formaldehyde polymer (novolak) suspended in solvent.
2. Sensitizer photoactive compound DNQ added to novolak as strong dissolution inhibitor (insoluble in developer).
3. During exposure, DNQ photochemically decomposes and creates carboxylic acid.
4. Carboxylic acid promotes dissolution of novolak in exposed areas of resist (resist becomes soluble in developer).

A major advantage of a positive resist is that the unexposed areas of the resist are not affected by the developer, since the resist is initially insoluble and remains as such. Thus the pattern of fine lines that is transferred to the resist will maintain the linewidths and shape during the photolithography process, producing good linewidth resolution. Older positive resists had marginal adhesion strength, but modern positive resists have been designed with more acceptable adhesion.

A reason why positive resist has good resolution is contrast. The positive resist can distinguish better between the light and dark areas of the mask, making a sharp transition from exposure to nonexposure in the resist. Positive photoresist has good contrast characteristics, which produces improved line resolution due to sharp resist sidewalls (see Figure 13.21).

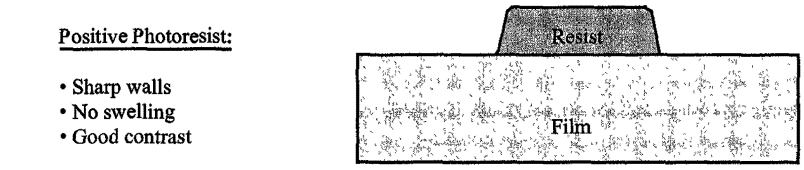
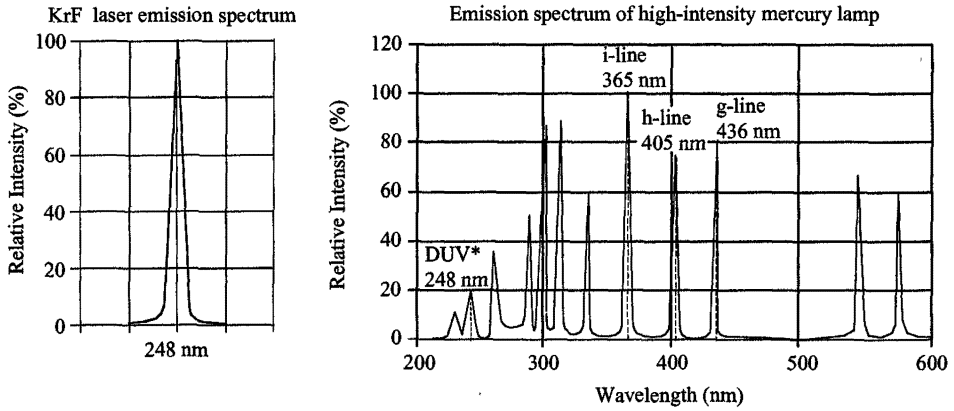


FIGURE 13.21 Good Contrast Characteristics of Positive I-Line Photoresist

Deep UV (DUV) Photoresists

For optimum pattern resolution, a goal in microlithography has been for the wavelength of the exposure light to be proportional to the critical linewidth dimension (this is explained in Chapter 14). For exposure with an i-line wavelength of 365 nm in the mid-1990s, a CD of 0.35 μm was achievable. In order to achieve a CD of 0.25 μm on critical layers in the latter 1990s, it was necessary to reduce the wavelength of the exposure light source to a value of around 250 nm (0.25 μm). This value corresponds to the 248 nm UV wavelength referred to as *deep UV (DUV).* This wavelength is shown in Figure 13.22.



* *Intensity of mercury lamp is too low at 248 nm to be usable in DUV photolithography applications. Excimer lasers, such as shown on the left provide more energy for a given DUV wavelength.*

FIGURE 13.22 DUV Emission Spectrum Mercury Lamp Spectrum
(Used with permission from USHIO Specialty Lighting Products)

Standard i-line photoresists are generally not acceptable at the DUV wavelengths necessary for CDs of 0.25 μm and below due to lack of sensitivity to smaller wavelengths. Resists have a sensitivity to the minimum amount of light energy required to transfer an acceptable pattern. The DNQ i-line resist system has excessive light absorption and lacks sensitivity at the low light intensity of the shorter DUV wavelength.[11] If the i-line resist has excessive light absorption, then the light never penetrates the full thickness of the resist, leading to incomplete exposure and poor image formation. The lower light sensitivity of the i-line resist would require longer exposure time, causing a decrease in wafer throughput. This low sensitivity is a serious problem when the light source is a mercury lamp with its limited output at the DUV wavelength of 248 nm. For this reason, i-line photoresists are used on noncritical wafer layers of 0.35 μm linewidths and above.

Chemical Amplification for DUV Resists ■ A major change in photoresist technology occurred with the introduction of a new type of photoresist for DUV wavelengths based on chemical amplification. *Chemical amplification (CA)* is a means to increase the sensitivity of the resist substantially over that of the DNQ-novolak i-line resists. All positive and negative tone 248-nm resists are chemically amplified.[12] The researchers who developed chemically amplified resist in the 1980s at IBM (International Business Machines) realized that the light absorption and sensitivity of the i-line resist system was unacceptable for shorter DUV wavelengths, creating the need for a new photoresist that offered the benefits of chemical amplification.[13]

Chemically amplified DUV resists are formulated to react at an accelerated rate to the exposing DUV light source based on an acid-catalyzed reaction. This action is accomplished by boosting the resist sensitivity with the use of a sensitizer known as a *photoacid generator (PAG).* The PAG produces an acid upon exposure to radiation from deep UV light. This acid is only produced in the resist regions exposed to light. In the areas of resist where there is no light exposure, the acid is not created. Most well-known acid generators used in DUV resists are onium salts, such as iodonium and sulfonium salts.[14]

CA DUV resist technology has undergone significant development over the years. The basic principle for all CA DUV resist resins is that the resin requires a chemical protecting group that makes it insoluble in aqueous (water-based) developer. The acid generated by the PAG in the DUV-exposed areas of the resist then removes the protecting group (referred to as *deprotection*) through a catalytic reaction while heated during the post-exposure bake step. After heating the DUV resist, the exposed resin becomes soluble in the developer.

An early CA DUV resin developed and used at IBM in the 1980s to manufacture DRAMs using DUV lithography was t-BOC (tert-butoxycarbonyl).[15] The t-BOC is the protecting group for the resin known as PHS or PHOST (poly[hydroxystyrene]). Once the photo-generated acid removes the t-BOC-protecting group (referred to as an acid-catalyzed t-BOC deprotection reaction), then the PHS resin becomes soluble in developer.

PHS resin is well-established for use in CA DUV positive resists (note that all major resist manufacturers are actively researching "new generation" CA DUV resists).[16] PHS resin is a phenolic copolymer that has protecting groups that make it dissolve poorly in an aqueous-based solution. During deep UV exposure, the PAG acid is photochemically generated in all exposed resist regions. This acid is the chemical catalyst that removes (cleaves) the protecting group during post-exposure thermal bake. This operation renders the exposed PHS highly soluble in the aqueous developer (see Figure 13.23 on page 356). Essentially, these chemical reactions transform the exposed regions of the DUV resist from an insoluble resist into a highly soluble resist in an aqueous-based developer. Table 13.5 on page 356 outlines the four steps to developing a CA DUV resist.

The first commercial CA DUV resist was a negative system based on crosslinking a phenolic resin with an acid catalyst. All negative CA resists are built on this phenolic resin crosslinking. Negative CA resists have poor process latitude in imaging small contact holes because of the clear-field image during exposure. At the same time, negative DUV resists are resistant to thermal flow for temperatures below 150°C, due to the crosslinking of the phenolic resin polymer.[17] This condition can be beneficial in some etch applications.

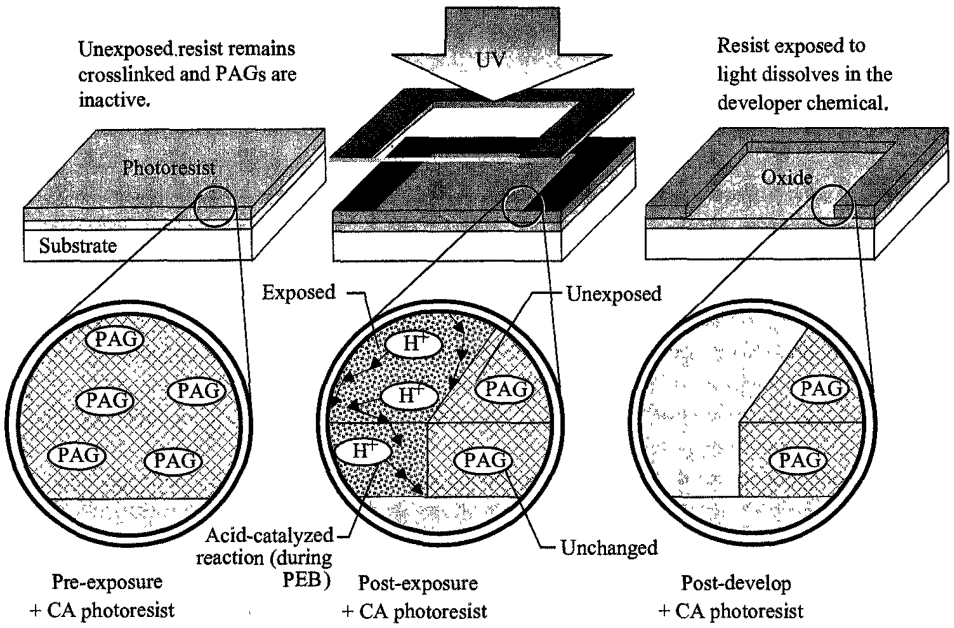


FIGURE 13.23 Chemically Amplified (CA) DUV Resist

TABLE 13.5 Exposure Steps for Chemically Amplified DUV Resist

1. Resin is phenolic copolymer with protecting group that makes it insoluble in developer.
2. Photoacid generator (PAG) generates acid during exposure.
3. Acid generated in exposed resist areas serves as catalyst to remove resin-protecting group during post-exposure thermal bake.
4. Exposed areas of resist without protecting group are soluble in aqueous developer.

Positive CA resists are the dominant type for patterning wafers with 0.18-μm generation devices using DUV wavelengths. One of the main benefits of CA DUV resists is the speed of resist exposure. CA chemistry is capable of providing a 10-fold improvement in the exposure speed over DNQ-novolak-based resist systems without a major compromise in any of the resist lithographic performance areas.[18] Chemical amplification in DUV resist improves the sensitivity of the resist for low-intensity light sources. In addition, DUV offers high-contrast imaging with vertical sidewall profiles and high resolution suitable for resists used on wafers with critical dimensions of 0.25 μm and below.[19]

193 nm DUV Resists. Suitable chemically amplified DUV resists are being introduced into production at this time for 193 nm wavelength exposure light capable of imaging a CD resolution of 0.18 μm. The biggest change is the unacceptability of resists based on phenolic polymers (DNQ i-line resist) or hydroxystyrene (248 nm DUV resist). Some early 193 nm resists are based on polyvinyl phenol and polymethylmethacrylate (PMMA).[20] Another chemical platform under investigation is cyclic olefin polymer materials, which offer superior etch properties.[21] These resists may be used with multilayer resist technology using top surface imaging (see the advanced lithography section in Chapter 15).

DUV Process Requirements ■ DUV resists are very sensitive to contamination, specifically amines (an organic compound such as ammonia) that are found in the ambient atmosphere. Less than several parts per billion (ppb) exposure to amines commonly found in air will lead to undesirable CD variation in the top of the resist profile. This resist variation leads to unacceptable linewidths after etch. Amine sensitivity in CA DUV resists requires that the air in all photolithography equipment be chemically filtered.[22] Monitoring equipment used in photolithography can detect down to 500 parts per trillion amines.

CA resists for DUV are also dependent on the bake temperature at the post-exposure bake (discussed in Chapter 15) for reducing CD variation. Early DUV resists had significant temperature sensitivities, whereas newer resists have less temperature sensitivity. In addition, early DUV resists required the time between resist exposure and post-exposure bake processing to be limited to a few minutes. Recent DUV resists can be delayed slightly longer, up to about 30 minutes.

Photoresist Dispensing Methods

For semiconductor microlithography, the most widely used method to apply the liquid photoresist to achieve a uniform coating on the wafer surface is *spin coating*. There are four basic steps to applying resist by spin coating (see Figure 13.24):[23]

1. **Dispense.** The resist is dispensed onto the wafer while it is stationary or spinning very slowly.
2. **Spin-up.** Quickly accelerate the wafer rotation to a high rpm (revolutions per minute) spin speed to spread the resist over the entire wafer surface.
3. **Spin-off.** Throw off excess resist to obtain a uniform resist film coating on the wafer.
4. **Solvent evaporation.** Continue to spin the coated wafer at a constant rpm until the solvent evaporates and the resist film is nearly dry.

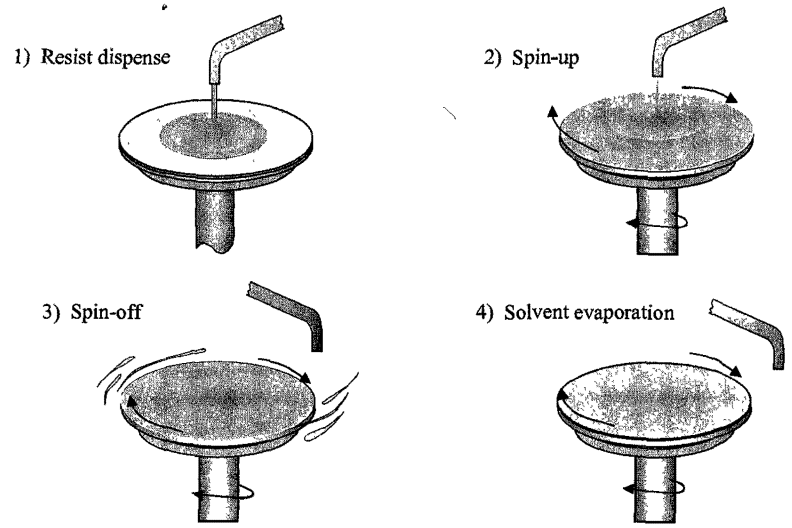


FIGURE 13.24 Four Steps of Photoresist Spin Coating

The two goals in resist spin coating are to have a uniform film coating on a wafer and to achieve a repeatable resist thickness that is maintained from wafer to wafer over extended periods. The target resist thickness is specified for a particular application and is typically on the order of 1 μm. Thickness variation of the resist film on a wafer should be measured less than 20 to 50 Å across the entire wafer surface. Wafer-to-wafer resist thickness control is typically less than 30 Å measured over many wafers.[24]

Spin Coating Equipment ■ Wafer spin coating takes place in an automated wafer track system with wafer handling equipment to move the wafers from operation to operation (see Figure 13.25 on page 358). Robotic handling is preferred over conveyors to minimize particle generation and wafer damage.

The complexity of the automated wafer track is that there are many different operations being performed simultaneously. At any one time, the wafer track could be processing 15 to 20 wafers through different photolithography operations, such as vapor prime resist spin coat, develop, baking, and chilling. Track systems are connected to the wafer stepper and must interface with the stepper so that wafers are delivered and picked up at the correct time with limited waiting.

To spin coat the wafer, robotic handlers position the wafer on a vacuum chuck at the spin coat station in the wafer track. The chuck is a hollow, flat metal disc with holes in its surface that is

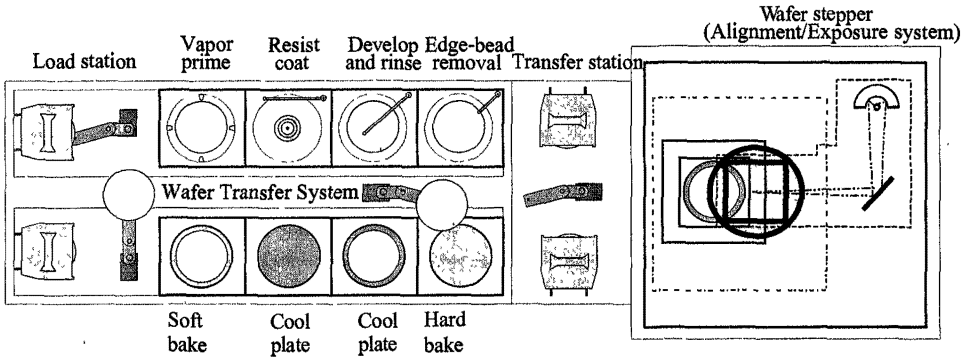


FIGURE 13.25 Automated Wafer Track System for Photolithography

connected to a vacuum. When the wafer is placed on the chuck surface, the vacuum pulls the wafer into intimate contact with the chuck to hold it while spinning.

The resist is dispensed on the wafer through a dispenser nozzle that should deliver a steady stream of resist (see Figure 13.26). The nozzle has a suckback feature to prevent after-dispense drips on the wafer surface. The nozzle is controllable in the X, Y, Z, and θ directions, giving the process engineer flexibility to position the nozzle in a location to optimize thickness, uniformity, and the amount of resist dispensed. A particular dispense method is called radial dispense, where the arm is actually moved across the wafer while the resist is dispensed. This action minimizes the amount of resist dispensed. The movement is computer controlled and can be from edge-to-center or center-to-edge.

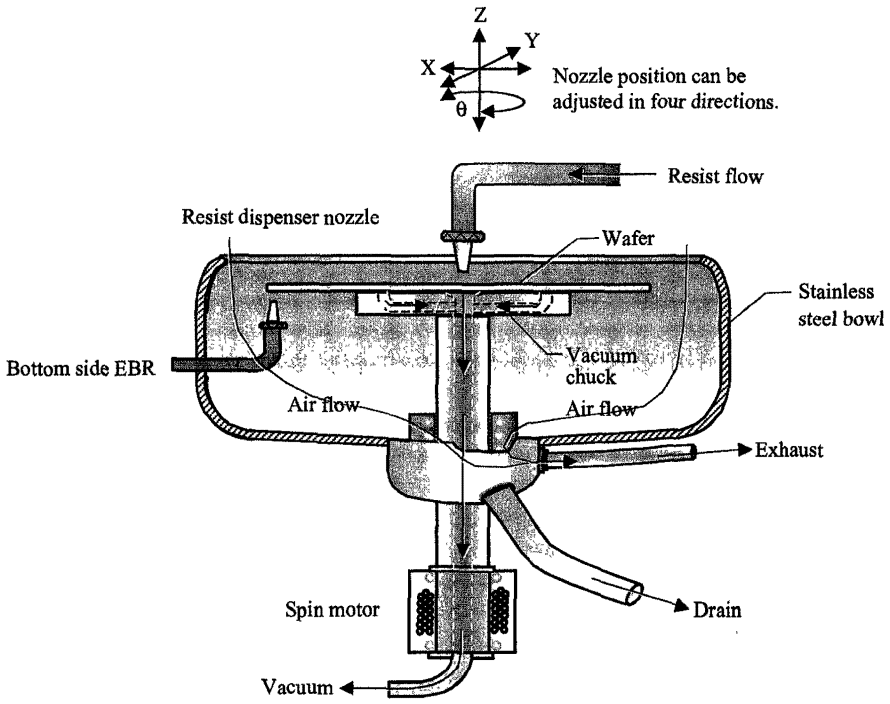


FIGURE 13.26 Photoresist Dispense Nozzle

Spin Coating Parameters ■ The manner of dispensing the liquid resist varies depending on the parameters defined for the application by the process engineer. The resist can be dispensed on a wafer while it is not rotating, known as *static dispense*. After the static dispense, the wafer is first spun at a low rpm to uniformly spread the resist. Once the resist approaches the wafer edge, the rpm is accelerated to the final spin speed (e.g. a typical final speed may be 4,000 rpm). Another approach

is to dispense the resist on a wafer that is spinning slowly (e.g., 100 to 200 rpm) in order to uniformly coat the wafer, followed by acceleration to the final spin speed. This is referred to as a *dynamic dispense.*

The amount of resist dispensed depends to a large degree on the viscosity of the resist. For example, a high-viscosity resist with a viscosity of 55 cps may require 2.4 cc of resist for a good coat. On the other hand, a low-viscosity resist with an 8 cps viscosity may need only 1.3 cc of resist. Lower viscosity resists typically have a thinner target thickness.[25]

Resist thickness and uniformity on a wafer are critical quality measures. Thickness is not controlled by the amount of resist deposited since most of the resist flies off the wafer (less than 1% remains on the wafer). The most critical parameters for resist thickness are spin speed and resist viscosity. Many resist manufacturers publish thickness versus spin speed data for their resist formulation (see Figure 13.27). This data assists in determining the optimum final spin speed. Higher viscosities and slower spin speeds will produce thicker layers of photoresist. In general, the resist thickness has been found to vary with spin speed as:[26]

$$\text{Resist thickness } \alpha \frac{1}{(\text{RPM})^{1/2}}$$

Where RPM is the spin speed in revolutions per minute.

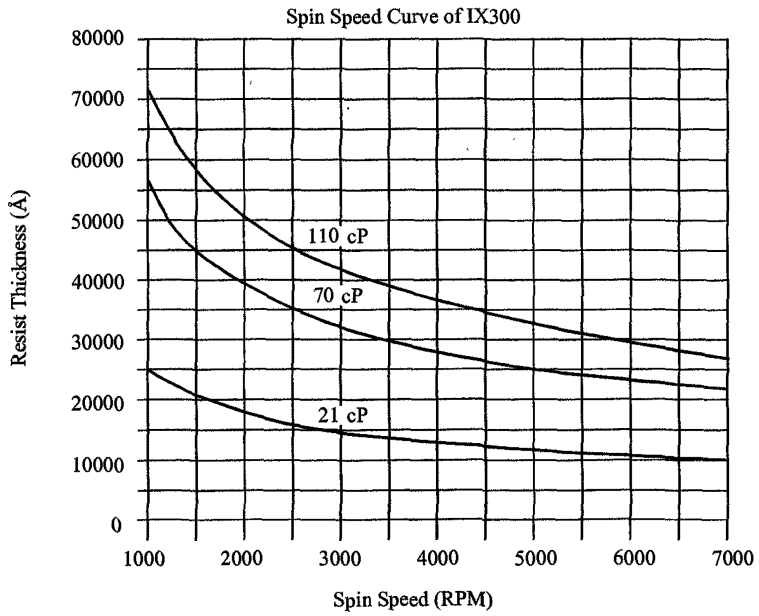


FIGURE 13.27 Resist Spin Speed Curve
(Used with permission from JSR Microelectronics, Inc.)

Different parameters affect resist thickness and uniformity. The acceleration ramp rate to attain the final spin speed is controllable on most spin coaters. High ramp rates usually produce better film uniformity than slow ramp rates. Another parameter is the height of the nozzle and its location during the dispense.

Another important parameter for resist dispense is environmental control. The wafer track system is a closed environment in order to control temperature, humidity, exhaust, and particulate contamination during application of the photoresist coating. Temperature and humidity strongly affect resist uniformity across the wafer. The minienvironment of a wafer track system for photolithography is often controlled for particulate contamination to a class 0.1 level. In addition, the exhaust air flow rate around the spin coater must be properly controlled to avoid negatively impacting resist thickness and uniformity. Too much air flow due to strong exhaust can cause excessive drying of the resist, while poor exhaust flow can cause particles to deposit on the wafer instead of being carried away by the air flow.

Edge-Bead Removal ■ During the wafer spin process, resist flows outward due to centrifugal force toward the wafer edge and onto the backside. This ridge of resist on the wafer edge and backside is called edge bead. When dry, the resist flakes off and causes particles. These particles can land on active circuit areas, on wafer carriers, and inside process equipment, leading to increased defect densities on the wafer. Furthermore, the resist on the back of the wafer can create problems by causing it to stick to wafer chucks.

Resist spin coat stations are equipped with an *edge-bead removal* (*EBR*) device (see Figure 13.26 on page 358). A common approach is to use a spray nozzle assembly to spray a small amount of solvent on the underside of the spinning wafer. The solvent laps up over the beveled edge to the topside, with careful control to ensure the solvent does not reach the topside of the resist (this control is important for defect density reduction). Typical solvents to remove the edge bead are propylene glycol monomethyl ether acetate (PGMEA) or ethylene glycol monomethyl ether acetate (EGMEA).

Some photolithography tools use a laser to expose the edge of wafers right after the normal wafer exposure has taken place. The exposure softens the resist and allows the edge-bead resist to be removed during the normal develop step or by a designated solvent nozzle. This step can be performed in the same track system that was used to spin coat the wafers.

SOFT BAKE

Following the application of resist on the wafer by spin coating, wafers are subjected to an elevated temperature step referred to as *soft bake* (also called *pre-bake*). The reasons for the soft bake of the resist are:[27]

1. Drive off the solvent from the coated resist on the wafer.
2. Improve the adhesion of the resist so that it adheres adequately during the development step.
3. Relieve stresses in the resist film that occurred during the spin process.
4. Prevent resist from getting all over the equipment (keep the tool clean).

The soft bake temperature and time depend on the particular resist and process conditions. The starting point for setting the soft bake parameters is the process recommended by the resist manufacturer. After that, the process is optimized to achieve the adhesion and dimensional control required for the product. The soft bake temperature is usually in the range of 85 to 120°C. The duration of the soft bake varies for different resists, but 30 to 60 seconds is a typical time.

If the resist film were not soft baked and continued directly to alignment and exposure after resist apply, the following problems would occur:[28]

1. The resist film would be tacky and susceptible to particulate contamination.
2. Inherent stresses in the resist film from spin coating would lead to adhesion problems.
3. The high solvent levels would cause inadequate discrimination between exposed and unexposed resist for proper dissolution during development.
4. Outgassing from the resist (from heat during exposure) could contaminate the lens of the optical system.

Before spin coating, photoresist typically contains between 65 to 85% solvents. After spinning, the solvent has been reduced to 10 to 20%, yet the film should still be considered in a liquid state.[29] The ideal amount of solvent after soft bake is about 4 to 7%. Because the solvent is reduced in the soft bake process, the thickness of the resist film also decreases.

Soft Bake Equipment

The preferred method for resist soft bake is heat conduction from a wafer on a vacuum hot plate[30] (see Figure 13.28). In this method, heat is quickly conducted from the hot plate through contact with the backside of the wafer to the resist. The resist is heated from the wafer-resist interface outward, which minimizes the potential for solvent entrapment. Because of the short cycle time (e.g., 30 to 60 seconds), this single-wafer hot plate method is suitable for the flow of multiple wafers through the process steps of an automated wafer track system. In the wafer track process flow, the heating

step is usually followed by a cooldown step on a cooling plate. This step rapidly cools the wafer for the next operation. The vacuum hot plate design is the same type as that used for dehydration bake. There is also the option of infrared (IR), microwave, and convection heating for soft bake, but these methods are not commonly used.

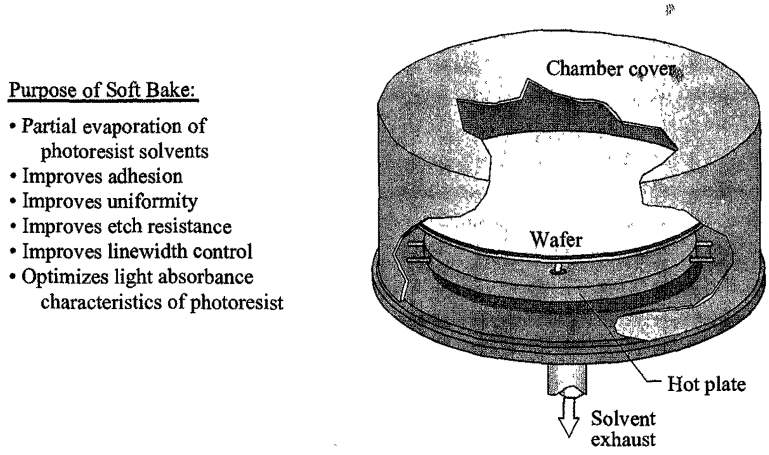


FIGURE 13.28 Soft Bake on Vacuum Hot Plate

Process Characterization

The soft bake process requires characterization to determine optimum settings. Reasons to optimize soft bake settings are to have better control over critical dimensions, improve the resist sidewall angle, increase resolution, improve contrast, and achieve wider process latitude.

The solvent content of the resist can be measured as a function of temperature with a *thermogravimetric analysis (TGA)*. TGA uses the principle of volatization, or polymer weight loss during heating, to represent the amount of solvent loss and thermal decomposition as a function of temperature.[31] To perform this test, a sample is coated with resist and placed immediately into an oven without soft baking. While heating, the sample's weight is measured and plotted (see Figure 13.29).

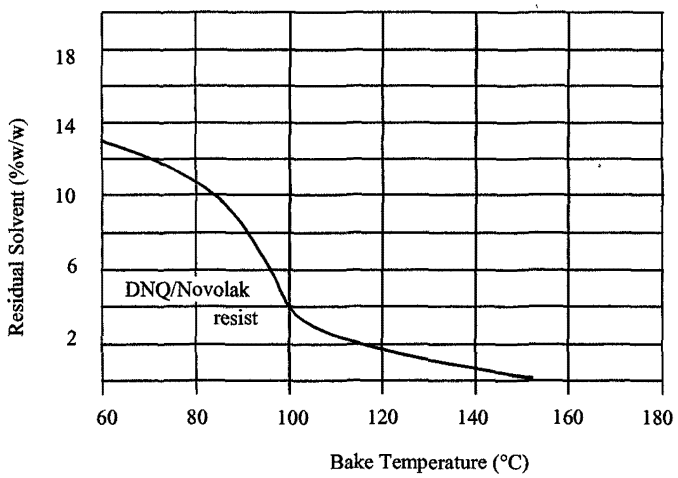


FIGURE 13.29 Solvent Content of Resist versus Temperature During Soft Bake

Another method to characterize the amount of solvent removal is to measure the change in resist thickness as a function of temperature. As solvent evaporates, the resist will become thinner. The temperature at which the resist thickness stabilizes is where most solvents are removed.

PHOTORESIST QUALITY MEASURES

Quality measures for photoresist processing are provided in Table 13.6.

TABLE 13.6 Key Quality Measures for Photoresist

Quality Parameter	Types of Defects	Remarks
1. Resist adhesion.	A. Resist dewetting, which is also called lift-off. The resist does not adhere to the substrate, causing problems during subsequent etch or ion implantation processing.	Possible causes of resist lift-off are: • Contamination on wafer surface. • Inadequate HMDS priming or dehydration bake resulting in moisture on wafer surface (measured by contact angle meter as described in Chapter 7). • Excessive HMDS priming can cause resist "popping," which is failure of poorly adhered resist. • SiO_2 is a difficult surface to achieve good adhesion because it is a hydrophilic surface (water attracting).*
2. General quality of resist coating on wafer.	A. Pinholes (very small holes) in the resist.	• Particulate contamination on mask/reticle (evident after exposure) or on wafer. Check surface preparation cleaning.
	B. Splashback (drops of resist fall on resist coating).	• Improper exhaust level in spin coater. • Adjust vacuum suckback on dispense nozzle to stop drops from forming and dripping on resist.
	C. Resist skinning (thin layer of insoluble resist dried on top of resist coating).	• Spin rate is too high. High spin speeds can cause striations (lines) in the resist. • Exhaust rate too high in spin coater. • For DUV resists, ensure coated resist is not exposed to amines inside track system (check carbon filtration).
3. Thickness of resist coating.	A. Coated resist thickness is out of control. Resist thickness must be uniform: wafer-to-wafer mean thickness requirement is often <30 Å total indicated runout (TIR, which is maximum minus minimum thickness).	Parameters that affect thickness of resist are: • Check spin acceleration and speed. Higher spin speeds produce thinner resist (recall that thickness is inversely proportional to the square root of spin speed). Verify spin speed versus thickness characteristic curve of resist manufacturer. At low spin speeds, irregular solvent loss leads to thickness nonuniformity. • Verify correct spin time. Resist reaches stable thickness in several seconds and requires additional time for thickness uniformity. • Check for correct resist type and viscosity. • Verify no mechanical vibration or air turbulence during high speed spin dry.

* B. Smith, "Resist Processing," *Microlithography, Science and Technology,* ed. J. Sheats and B. Smith, (New York: Marcel Dekker, 1998), p. 529.

PHOTORESIST TROUBLESHOOTING

Common troubleshooting problems for photoresist are provided in Table 13.7.

TABLE 13.7 Common Photoresist Troubleshooting Problems

Problem	Probable Cause	Corrective Actions
1. Excessive resist usage during spin coating (DUV resist costs $2,000 to $5,000 per gallon).	A. Sub-optimum setting of process variables during spin coating process.*	Optimize process variables for spin coating: • First, determine minimum volume of resist needed to coat the wafer (referred to as cut-off volume). • Second, evaluate the following critical parameters using design of experiments: dispense spin speed, exhaust flow rate during dispense and drying steps, dispense rate, resist temperature, cool plate temperature, and ambient air temperature.
	B. Improper spin coater tool setup.	Check the spin coater setup for the following: • Incorrect nozzle size, height, or position. • Calibration of coater equipment. • Wrong software process recipe for wafer.
2. Wafers damaged (broken or chipped) during normal processing in the wafer track.	A. Improper setup of different tools used in track for processing wafers.	Check the following equipment for proper setup: • Improper calibration of robot arms during wafer handoff from one track tool to another. • Loss of chuck vacuum during spin. • Spin coat machine is not leveled properly and has mechanical vibration. • Excessive spin speed. • Verify calibration of cassette indexer to index wafers in cassette for robot pickup. • Warped cassettes cause equipment malfunction.
3. DNQ-novolak resist becomes unstable and contaminated with articles.	A. DNQ-novolak resist has aged due to shelf life.	Excessive shelf life of DNQ-novolak resist (> several months, with maximum of six months to one year) can lead to the following:** • Increase in absorption at longer wavelengths. • Susceptible to thermal degradation of the DNQ, leading to crosslinking and increase of high molecular-weight resist components. • Formation of undesirable acids in the resist. • Precipitation (falling out of solution) of sensitizer to form crystallized particles that contaminate resists. This especially occurs at high-temperature storage. • Point-of-use filtration is common practice for production applications to control resist consistency. Typical filter size is 0.05 μm for 0.25 μm feature size.

* B. Lorefice et al., "How to Minimize Resist Usage During Spin Coating," *Semiconductor International* (June 1998): p. 182.

** B. Smith, "Resist Processing," *Microlithography, Science and Technology,* ed. J. Sheats and B. Smith,

SUMMARY

Photolithography transfers a pattern from a mask to a UV light-sensitive photoresist on the wafer surface. Resolution is the smallest feature that can be patterned. Photolithography requires process latitude to consistently pattern wafers that meet the requirements. Negative lithography prints a pattern in the wafer that is opposite the mask pattern, whereas positive lithography prints the same mask pattern in the wafer. Photolithography can be divided into eight basic steps: (1) vapor prime, (2) spin coat, (3) soft bake, (4) alignment and exposure, (5) post-exposure bake, (6) develop, (7) hard bake, and (8) develop inspection. The wafer is prepared for resist application by cleaning, dehydration bake, and HMDS vapor prime. Negative photoresist hardens (crosslinks) with UV exposure, while positive resist softens (dissolves). Soft areas are washed away in developer solution. Positive resist is used for submicron lithography. Conventional i-line resist responds to 365 nm UV light for a CD of 0.35 μm and is common on noncritical layers. Positive i-line resist has DNQ-novolak chemistry and is activated by a photo-active compound (PAC). Wafer critical layers (CD of 0.25 μm and below) are patterned with a deep UV (DUV) resist that is chemically amplified. The DUV wavelength is 248 nm and is being reduced to 193 nm. A chemically amplified resist has a chemical protecting group that makes it insoluble in aqueous developer. A photoacid generator (PAG) generated in the DUV-exposed areas deprotects the resist when heated and makes the exposed resist soluble in developer. Liquid photoresist is applied to the wafer by spin coating, followed by edge-bead removal. A soft bake is used to drive off solvents and improve resist adhesion.

KEY TERMS

photolithography (also photo, lithography, masking, or patterning)
microlithography
reticle
photomask (also mask)
optical lithography
resolution
overlay accuracy
overlay budget
runout
process latitude
negative lithography
positive lithography
negative resist
positive resist
dark-field mask
clear-field mask
coater/developer track system (also tracks)
hydrophilic (also hydrated)
hydrophobic (also dehydrated)
dehydration bake
hexamethyldisilazane (HMDS)
vapor prime coating
photoresist
contrast
sensitivity
exposure dose
resist viscosity
resist adhesion
etch resistance
surface tension
conventional i-line photoresists
novolak
photoactive compound (PAC)
DNQ-novolak
deep UV (DUV)
chemical amplification (CA)
photoacid generator (PAG)
spin coating
static dispense
dynamic dispense
edge-bead removal (EBR)
soft bake (also pre-bake)
thermogravimetric analysis (TGA)

REVIEW QUESTIONS

1. What is photolithography?
2. Describe the difference between a reticle and a photomask.
3. List the different UV wavelengths used in photolithography and the name for each wavelength used between 436 and 157 nm.
4. Define resolution.

5. What is overlay accuracy, and how does this contribute to the mask overlay budget?
6. Discuss process latitude.
7. Explain the difference between negative and positive lithography.
8. Describe a clear-field mask.
9. Explain what a dark-field mask is.
10. List the eight steps of photolithography, and give a short explanation of each step.
11. What is one of the major effects of contamination on the wafer surface?
12. Explain the difference between a hydrophilic and a hydrophobic wafer surface.
13. Why is a dehydration bake done?
14. What is HMDS and what purpose does it serve?
15. Describe the most common method of applying HMDS.
16. Define a photoresist.
17. Give two purposes of a photoresist in wafer fabrication.
18. How has photoresist been improved since the early days of wafer fabrication?
19. List and describe the two major types of photoresist.
20. What is the resolution limit of negative resist? Which resist is used for submicron lithography?
21. Define contrast.
22. Explain sensitivity and discuss how this condition is related to the exposure dose.
23. Describe resist viscosity and explain why it is important.
24. Explain resist adhesion.
25. Why is etch resistance an important resist property?
26. What is surface tension, and why is it important for a photoresist?
27. Explain why storage and handling are important for resist.
28. List and describe the four components to an i-line resist.
29. What are two disadvantages of a negative photoresist?
30. What is the most common photoresist used in IC photolithography?
31. State and describe the resin used in i-line positive photoresist.
32. Describe the sensitizer used in i-line positive photoresist.
33. List the four steps to dissolution of i-line positive resist.
34. Give a reason why positive i-line resist has good resolution.
35. Why are i-line resists unacceptable at the DUV wavelengths?
36. What does chemical amplification accomplish in a resist?
37. Describe the purpose of a photoacid generator (PAG).
38. List and describe the four exposure steps for CA DUV resists.
39. What is one of the main benefits of CA DUV resists for wafer fabrication?
40. In what manner are DUV resists sensitive to contamination?
41. How is photoresist applied to a wafer?
42. List and describe the four basic steps to spin coating.
43. Explain the difference between static dispense and dynamic dispense.
44. What does resist thickness vary with? State the formula that describes this relationship.
45. Describe edge-bead removal.
46. State the four reasons for soft bake.
47. What is the ideal amount of solvent remaining in the resist after soft bake?
48. What problems would occur if the resist were not soft baked?
49. Describe the preferred method for performing soft bake.
50. What does TGA stand for and why is this analysis done?

PHOTORESIST MATERIALS AND EQUIPMENT SUPPLIERS' WEB SITES

Allied Signal	http://www.electronicmaterials.com/
Arch Chemicals (aka Olin)	http://www.olinmicro.com/default.asp
Ashland Specialty Chem.	http://www.ashland-act.com/
Clariant Corporation	http://www.azresist.com/
Dainippon Screen Mfg. Co.	http://www.screen.co.jp./eed/index_E.html
DuPont	http://www.dupont.com/semiconductor/
Eastman Chemical	http://www.eastman.com/
EKC Technology	http://www.ekctech.com/ekctech.nsf
FSI International	http://www.fsi-intl.com/
JSR Microelectronics, Inc.	http://www.jsrusa.com/index2.html
J.T. Baker	http://www.jtbaker.com
Karl Suss Inc.	http://www.suss.com/
Olin Microelectronics	http://www.olinmicro.com/
Rite Track	http://www.ritetrack.com/
SEMI	http://www.semi.org/

Shipley Company	http://www.shipley.com/
Silicon Valley Group	http://www.svg.com
TEL, Tokyo Electron Ltd.	http://www.teainet.com
USHIO	http://www.ushio.com/index2.html

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CHAPTER 14

PHOTOLITHOGRAPHY: ALIGNMENT AND EXPOSURE

Optical lithography is similar to photography with a camera. A camera uses light and lens to transfer an image of an object to a negative film. The develop process then transfers the film's image to paper from which a picture is obtained. In photolithography, the photomask and its pattern are the objects to be photographed. Optics and a light source are used to project the image of the pattern of the mask onto the resist-coated wafer. Once the resist is developed, just as with a negative film for a camera, the mask pattern appears in the resist. Subsequent processing, such as etch, creates a permanent pattern of the mask image on the wafer surface.

Many variables affect the quality of a photograph, such as the type of film, the lighting conditions, whether the object is in focus, and the type of camera lens. A wide range of variables also affect photolithography in wafer fabrication. Examples are the physical conditions of the material on the wafer surface, the type of photoresist, the resolution power of the optics, the nature of the light, and the focusing accuracy of the system. To optimize the photolithography process for submicron critical dimensions, the production team must understand how all factors affect the final image. Team members have an important role because of their daily interaction with the equipment and product. They also should know where the wafers come from and the condition of the wafers prior to processing them in photolithography.

The alignment and exposure process represents a major equipment subsystem for modern photolithography. The wafer is first positioned within the focus range of the optical system. Wafer alignment features are aligned to similar matching features on the photomask, and the UV light is projected through the optics and the mask pattern. The mask pattern appears as light and dark features on the wafer; thus, exposing the photoresist. The numerous variables associated with alignment and exposure are reviewed in this chapter to understand their contribution toward achieving a high-quality, deep submicron patterning process.

OBJECTIVES

After studying the material in this chapter, you will be able to:

1. Explain the purpose of alignment and exposure in photolithography.
2. Describe the properties of light and exposure sources important for optical lithography.
3. State and explain the critical aspects of optics for optical lithography.
4. Explain resolution, describe its critical parameters, and discuss how it is calculated.
5. Discuss each of the five equipment eras for alignment and exposure.
6. Describe reticles, explain how they are manufactured, and discuss their use in microlithography.
7. Discuss the optical enhancement techniques for subwavelength lithography.
8. Explain how alignment is achieved in lithography.

INTRODUCTION

Modern photolithography equipment is based on *optical lithography*, which uses optics to accurately project and expose a mask pattern onto a resist-coated wafer. Basically it consists of an ultraviolet (UV) light source, an optical system, a reticle with the die pattern, an alignment system,

and a wafer covered with a light-sensitive photoresist. Optics is at the heart of photolithography's ability to pattern deep-submicron features. Photolithography is at the center of the wafer fabrication process, with wafers spending more time in this process area than any other operation (by some estimates, up to 60% of their fabrication time). Table 14.1 reviews the eight steps of photolithography and highlights the alignment and exposure step covered in this chapter.

TABLE 14.1 Eight Steps of Photolithography

Step	Chapter Covered
1. Vapor prime	13
2. Spin coat	13
3. Soft bake	13
4. Alignment and exposure	**14**
5. Post-exposure bake	15
6. Develop	15
7. Hard bake	15
8. Develop inspect	15

We learned in Chapter 13 about the photoresist material and its importance to successful photolithography. The critical equipment for photolithography is the step-and-repeat aligner (referred to as aligner, but commonly called stepper). Steppers align and expose successive reticle patterns by stepping from one exposure site to another on the resist-coated wafer surface. The industry has recently converted to the step-and-scan system for DUV resists, called step-and-scan technology (discussed later in this chapter).

In photolithography, wafer steppers have three basic purposes—all of which must meet the customers' specifications for accuracy and repeatability:

1. Focus and align the wafer surface to the quartz plate reticle (containing the patterns).
2. Reproduce a high-resolution reticle image on the wafer through exposure of photoresist.
3. Produce an adequate quantity of acceptable wafers per unit time to meet production requirements.

The alignment and exposure operation of the wafer stepper commences once the wafer surface has been coated with the photoresist and soft baked. Resist-coated wafers are automatically loaded onto a wafer stage in the stepper. At this stage the wafer is raised or lowered as needed to bring it into the focus range of the stepper optics. The wafer is aligned to the reticle so that the pattern can be transferred to the proper location on the wafer surface. Once the best focus and alignment are obtained, a shutter opens to allow UV light to pass from the illuminator to the reticle through a projection lens and then onto the resist-coated wafer (see Figure 14.1). The entire focusing, wafer alignment, and exposure operation is done by the stepper. Once a pattern is exposed, the stepper will step to the next location on the wafer and repeat the alignment and exposure (which explains the name step-and-repeat). The stepper is typically attached to an automated wafer track machine, which processes wafers for all other basic photolithography operations.

Importance of Alignment and Exposure

Integrated circuits are fabricated with semiconductor devices in the upper few microns of the silicon wafer, followed by successive deposition and patterning of material layers to form the circuits that interconnect the devices. Circuit designers, using computers with special design software, define the layout of the devices, metal lines, via connections, and other special circuit designs necessary for a chip to function. This is done layer by layer and structure by structure within a layer for the entire wafer. Like creating a stencil, the circuit design pattern for one or more die is transferred to a reticle, with multiple reticles needed to attain the final structure on the wafer surface (see Figure 14.2).

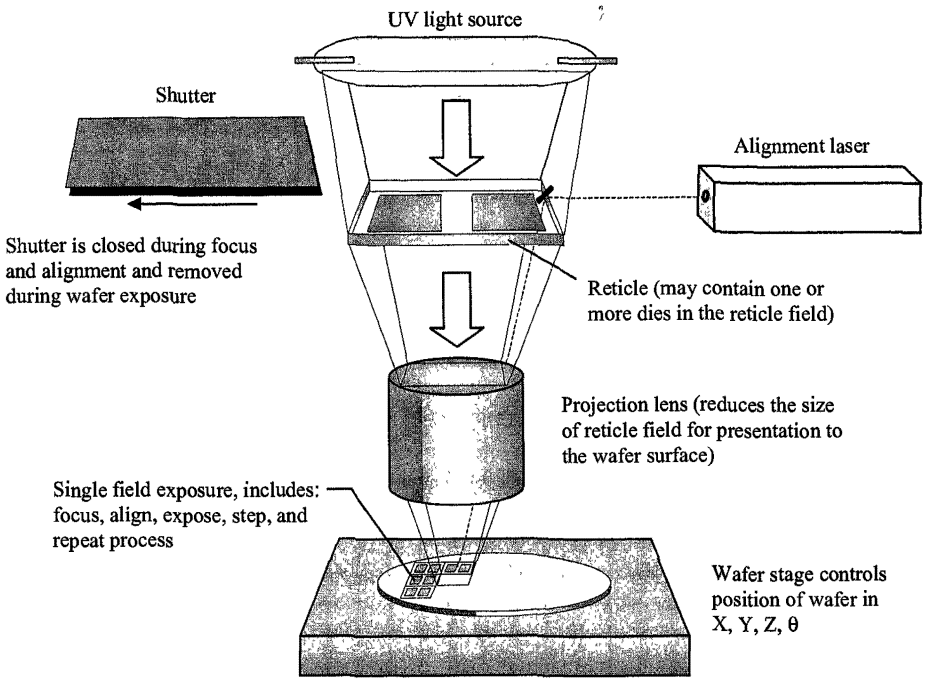


FIGURE 14.1 Reticle Pattern Transfer to Resist

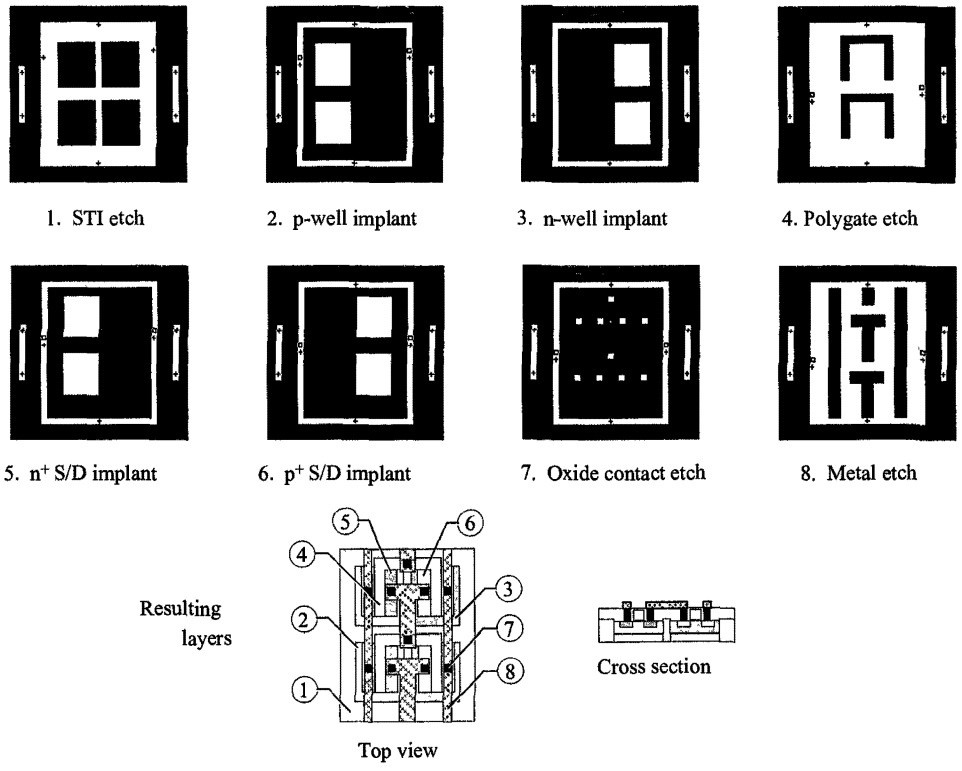


FIGURE 14.2 Layout and Dimensions of Reticle Patterns

The circuit design follows a set of design ground rules that specify the reticle pattern and its required dimensions. The design rules specify parameters such as linewidth, spacing between lines, contact size, via diameter, and the spacing between patterns defined on a reticle. Violation of design rules lead to poor production yield or unreliable product performance.

Each image defined in a reticle pattern has a particular function, such as a contact opening or metal lines. Patterns relate to a distinct material (e.g., oxide, aluminum, and so on) with dimensions and tolerances. Reticles overlay these patterns on top of one another during photolithography to form the devices and circuits on the wafer. The reticle overlay process has alignment specifications, previously referred to as the overlay budget. It is this overlay of reticle patterns onto existing features that poses the special alignment challenge for photolithography—how to accurately overlay patterns with submicron dimensions. Overlay accuracy must be met while maximizing product reliability and producing wafers in high volume.

Optical Exposure ■ During exposure, light from an illumination source passes through the aligned reticle. The reticle has opaque and transparent areas that define a pattern to be transferred to the photoresist on the wafer surface. The goal of exposure is for the reticle pattern to be accurately replicated (within specification) in the resulting image in the resist.

An aspect of exposure is, with all other factors being equal, the shorter the wavelength of the exposing light, the smaller the feature size that can be exposed. This fact has been a driving force for the continual reduction in feature sizes on wafers. Furthermore, the exposing light produces a certain amount of energy that is necessary to produce the photochemical reaction in the resist. This light energy must be uniformly distributed across the exposure field. Photolithography requires an intense exposure at the desired short wavelength to achieve the critical dimensions of today's microlithography.

OPTICAL LITHOGRAPHY

Optical lithography has traditionally been the major limiting factor to the continual reduction in microchip feature sizes since the beginning of wafer fabrication. The demise of optical lithography has been regularly predicted over the years. For instance, in 1985 it was predicted that optical lithography would be incapable of resolving a critical dimension smaller than 0.5 μm.[1] It is now believed that optical lithography is capable of resolutions down to a CD of 0.1 μm and beyond. Lithography is often considered the engine that is driving the performance improvements of Moore's law.[2]

Photolithography for wafer fabrication has been based largely on optical lithography. The longevity of optical lithography is attributed to the basic improvements that have been made to the equipment and process. We will now review the fundamental variables in optical lithography and the basis for these ongoing improvements. At the end of Chapter 15, we will study other next-generation lithography systems that are under investigation for advanced lithography applications and that may become viable for wafer fabrication in the future: extreme UV, e-beam, X-ray, and ion-beam lithography. Nevertheless, it appears that optical lithography will continue to dominate photolithography for the near future.

Light

A light source is needed in optical lithography to project the reticle pattern on the photoresist and cause a photochemical reaction. A practical description of *light* is an electromagnetic wave that is visible to the eye. Light is also radiant energy. These two descriptions reflect the dual nature of light as a wave and a particle. Light travels in waves similar to sound waves. Since light is a wave, it can be described by wavelength (λ) and frequency (f). The relationship of the two is given by the formula shown in Figure 14.3, where v is the velocity of light.

Interference of Light Waves ■ Waves are sinusoidal in nature. Sinusoidal waves of any type (e.g., light, electrical, or sound) that have the same frequency (monochromatic) can have interference between the individual waves. For example, wave interference may be two water ripples interacting with each other and partially canceling each other out. There are two types of interference based on whether the waves are in phase or out of phase (see Figure 14.4):

Constructive interference: Two waves in phase that add to each other.
Destructive interference: Two waves out of phase that subtract from each other.

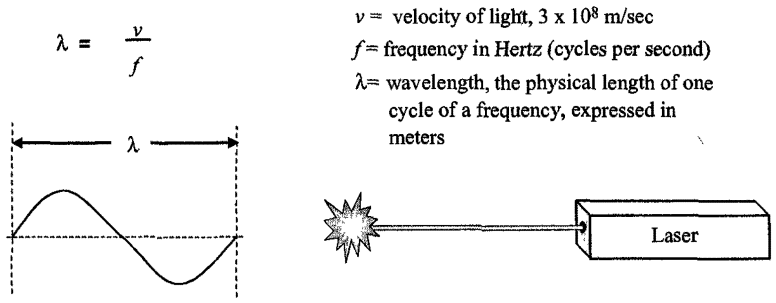


FIGURE 14.3 Light Wavelength and Frequency

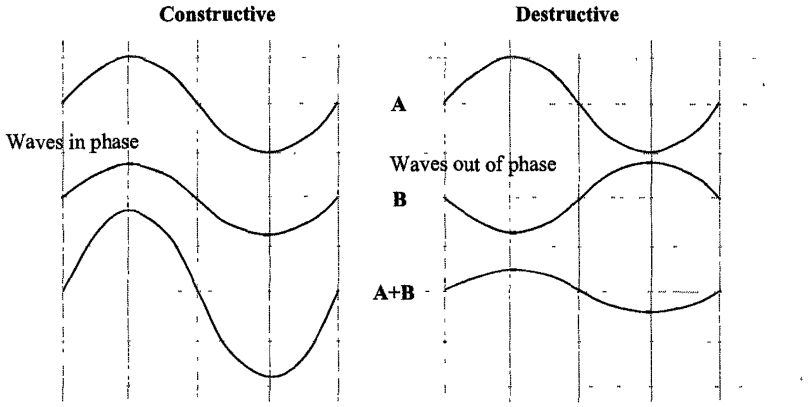


FIGURE 14.4 Wave Interference

Optical Filters. *Optical filters* use light interference to block unwanted incident light through either reflection or interference to obtain a light with a particular wavelength (see Figure 14.5). Optical filters will typically be made of glass and will have one or more layers of thin film coatings. The type of coating and its thickness will determine which wavelengths are blocked through destructive interference or passed through the glass.

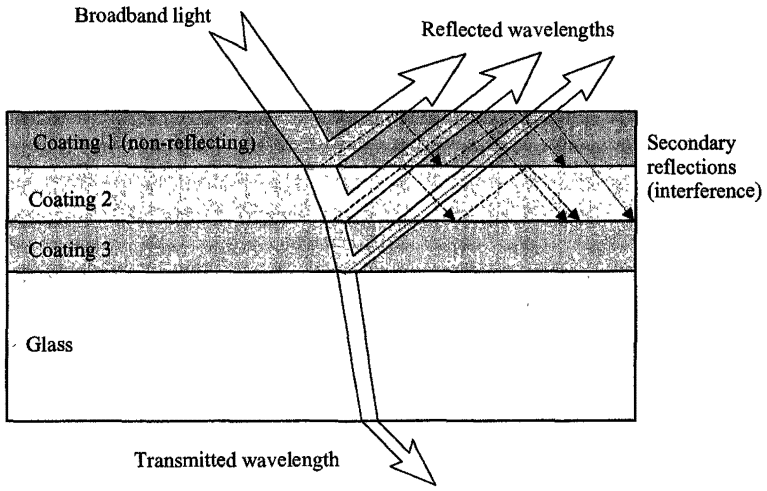


FIGURE 14.5 Optical Filtration

Electromagnetic Spectrum ■ The entire group of visible and nonvisible electromagnetic waves is called the *electromagnetic spectrum,* consisting of radiant energy that varies from very short to very long wavelengths. The visible portion of the spectrum has a wavelength between 390 nm and

780 nm. White light is composed of all the wavelengths of light in the visible spectrum. The UV spectrum ranges from 4 nm to about 450 nm, with a small overlap with the visible spectrum (see Figure 14.6). The deep ultraviolet (DUV) wavelengths are presently used for patterning critical layers in production. The vacuum ultraviolet (VUV) wavelength of 157 nm is the most likely UV successor after the DUV wavelengths of 248 nm and 193 nm. The short wavelength and high photon energy of VUV are strongly absorbed by oxygen absorption bands; therefore, operation is necessary in a vacuum or inert gas ambient (thus the name VUV). Research and development (R & D) is underway in the semiconductor industry into the future technology of using 13 nm UV wavelength, referred to as extreme UV (EUV).

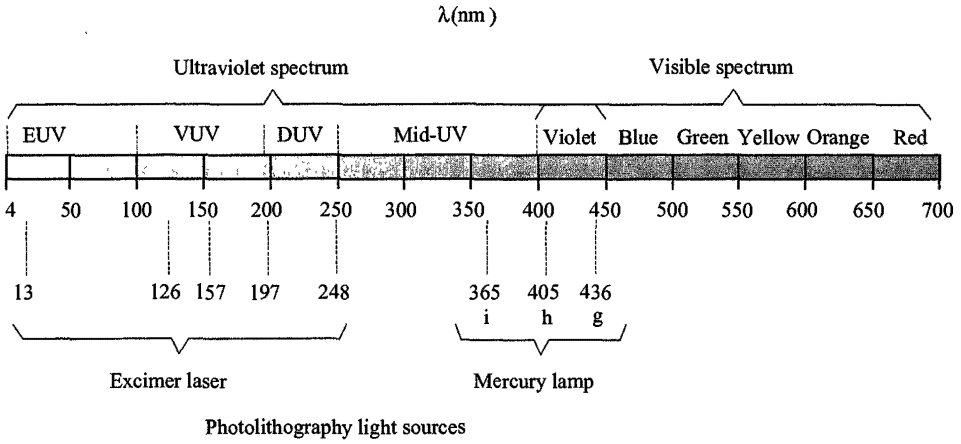


FIGURE 14.6 Ultraviolet Spectrum

Since the UV spectrum overlaps a portion of the visible spectrum, white light also contains a portion of UV (e.g., sunlight is visible and is white light, but it has UV wavelength also). Yellow light is commonly used in the photolithography area of the wafer fab because it is in the portion of the visible spectrum with little UV and, therefore, does not affect photoresists.

Exposure Sources

During exposure of the resist, photochemical transformations occur in the resist material to transfer the pattern from the mask. This is a critical step in photolithography. It must occur in the shortest amount of time and be repeatable for high-volume production of wafers.

Ultraviolet (UV) light is used to expose resist because the resist material reacts to light at this particular wavelength. Wavelength is also important because light with a smaller wavelength allows for the resolution of smaller features on the photoresist (explained in detail later in this chapter). The two types of UV exposure sources most often used today for optical lithography are:

- Mercury arc lamp
- Excimer laser

Besides these more commonly used light sources, other sources used to expose resist in advanced or special applications are X-ray, electron beam, and ion beam. These sources and their unique resist material will be discussed in Chapter 15 in sections on advanced technologies.

Mercury Arc Lamp ■ The high-pressure *mercury arc lamp* is used as the UV illumination source in all conventional i-line steppers. In this type of lamp, electrical current is passed through a tube of mercury-xenon gas to create a discharge arc. This arc emits a characteristic light spectrum, with the useful UV wavelength emissions for a mercury arc lamp between about 240 nm and 500 nm in length (see Figure 14.7).

The mercury arc lamp light spectrum has several intensity peaks. Some have been given letter names that come from the early days of spectrometry. The major intensity peaks are shown in Table 14.2.

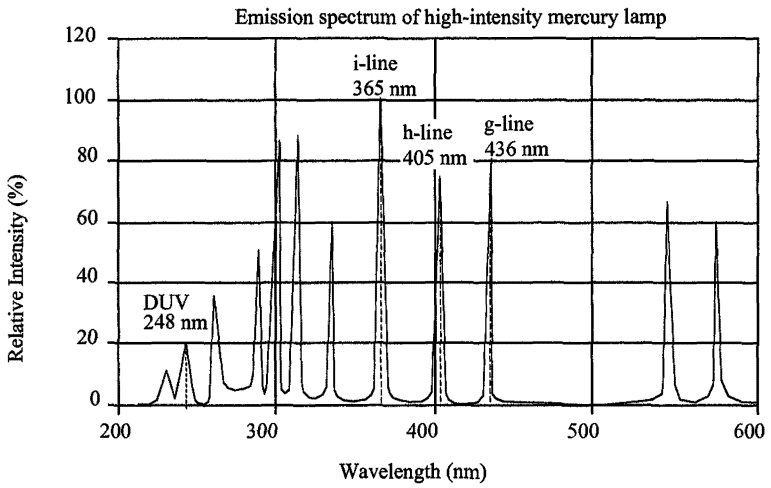


FIGURE 14.7 Emission Spectrum of Typical High Pressure Mercury Arc Lamp (Used with permission from USHIO Specialty Lighting Products)

TABLE 14.2 Mercury Arc Lamp Intensity Peaks

UV Light Wavelength (nm)	Descriptor	CD Resolution (μm)
436	g-line	0.5
405	h-line	0.4
365	i-line	0.35
248	Deep UV (DUV)	0.25

A conventional photoresist will have a certain spectral response that corresponds to a particular UV wavelength during exposure. For instance, a DNQ-novolak i-line resist, which is used for CD feature sizes down to 0.35 μm, responds to the UV i-line wavelength of 365 nm. To expose a resist to the proper UV wavelength, a set of filters is used to block the unwanted wavelengths and any infrared wavelengths. The exposure wavelength is chosen to match the critical feature size on the wafer.

An important aspect of the exposure source is the *light intensity,* which is defined by power per unit area (mW/cm^2), and measured on the surface of the resist. Another way to interpret intensity is the quantity of light per unit area, or brightness. Energy is the product of power and time. If the light intensity (which is power per unit area) is multiplied by the time of exposure, this represents the amount of exposure energy, or exposure dose, in (mJoules/cm^2, or mJ/cm^2) received by the surface of the photoresist.

A typical i-line resist requires an exposure dose of 100 mJ/cm^2 for its exposure.[3] Consider the emission spectrum shown in Figure 14.7 for a mercury arc lamp. The DUV emission at 248 nm is approximately five times less intense than the i-line emission at 365 nm. For an equivalent i-line photoresist at 248 nm, the low mercury arc lamp light intensity at the DUV wavelength would require five times more exposure time. In other words, if light intensity decreases, then the exposure time must increase by a proportional amount. This new exposure time is too long for acceptable wafer production and was a primary reason for the development of chemically amplified DUV photoresists and laser light sources with more power (see Figure 14.8 on page 374).

An undesirable parameter for the resist resin is excessive absorbance of incident radiation. With excessive resist absorption, the light intensity at the bottom of the resist is considerably less than that received at the top. This discrepancy produces image profiles with sloping sidewalls (see Figure 14.9 on page 374). To achieve straight-wall images, the resist must absorb only a small portion of the incident radiation, typically less than 20%.[4] Minimizing resist absorbance requires optimization between the wavelength, light source dose, and the type of resist.

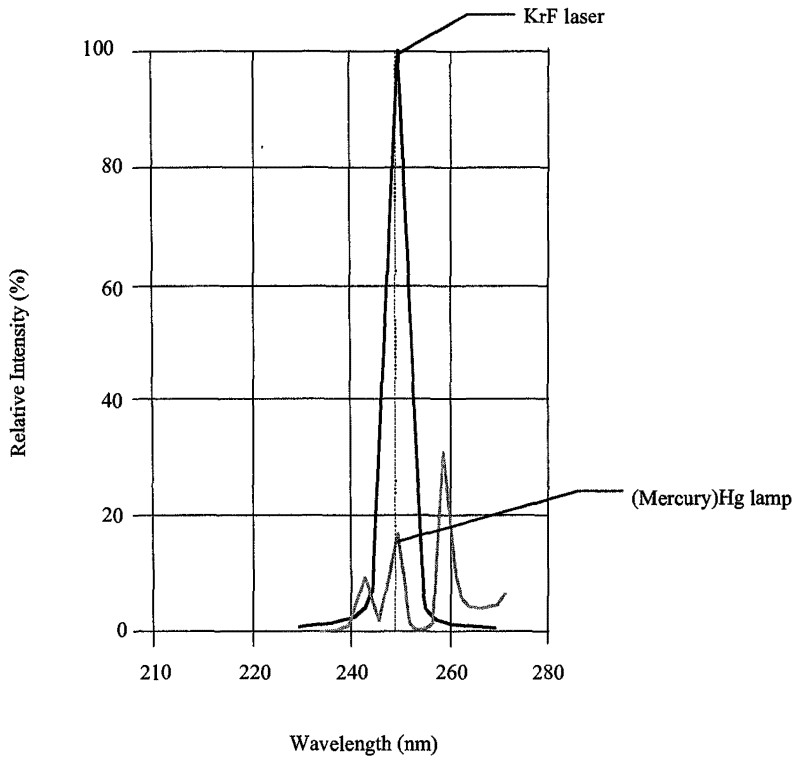


FIGURE 14.8 Spectral Emission Intensity of 248 nm Excimer Laser Versus Mercury Lamp

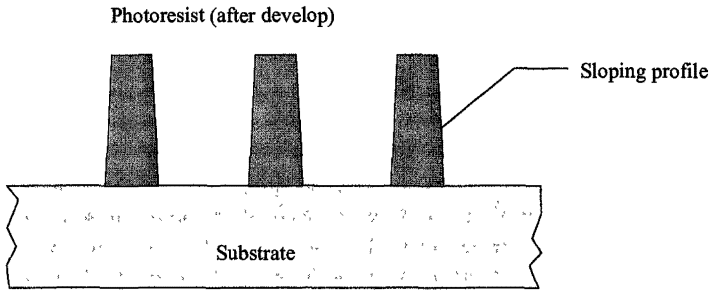


FIGURE 14.9 Excessive Resist Absorption of Incident Light

Excimer Laser ■ Laser light sources for photolithography have been available since the mid-1980s, but reliability and performance concerns delayed their implementation in wafer production until the mid-1990s. Their main benefit has been to provide more light intensity at the DUV wavelengths of 248 nm and below, since the mercury arc lamp is an inefficient emitter at these wavelengths.

The only laser light source used thus far for photolithography exposure is the *excimer laser.* An excimer is an exotic molecule formed from an atom of a noble gas and halogen, such as argon fluoride (ArF), where the molecule exists only in a quasi-stable, excited state.[5] The word excimer actually comes from the expression *exc*ited d*imer*, which is a molecule formed from two identical atoms, such as F_2. It also is used to represent the noble gas and halogen molecules.

Most excimer lasers today contain a high-pressure mixture of two or more elements that are bound in the excited state. Laser light emission occurs when the excited state decays and the exotic molecule falls apart into its two constituent atoms. The laser maintains a condition of more molecules in the excited state than in the ground state by using a high-voltage (10 to 20 kV) pulse discharge across two flat-plate electrodes to excite a high-pressure mixture of the noble gas and halogen.[6]

The most common excimer laser used for DUV resist is krypton-fluoride (KrF) with a wavelength of 248 nm. The KrF laser typically has a power range of 10 to 20 W at a frequency of 1 kHz, which produces high-power pulses of radiant light energy to expose the resist. Table 14.3 highlights excimer laser sources for wafer fabrication photolithography.[7] The argon-fluoride (ArF) laser, at a wavelength of 193 nm, is also envisioned to achieve DUV exposure. Notice that the fluorine (F_2) laser at the 157-nm wavelength has low output energy, which makes it less desirable for future production use because of the longer exposure time required. There has been recent improvement in the F_2 laser output energy to make it equivalent to the KrF and ArF lasers.[8]

TABLE 14.3 Excimer Laser Sources for Semiconductor Photolithography

Material	Wavelength (nm)	Maximum Output (mJ/pulse)	Frequency (pulses/sec)	Pulse Length (ns)	CD Resolution (μm)
KrF	248	300 to 1500	500	25	≤0.25
ArF	193	175 to 300	400	15	≤0.18
F_2	157	6	10	20	≤0.15

As seen in Table 14.3, the excimer laser produces extremely short pulses of light. The peak power of each short pulse is high and can cause damage to optical materials and lens coatings. To minimize this damage, longer laser pulse lengths are desirable and lenses are designed with features to avoid the high concentrations of light from the laser source. Another problem with early excimer lasers was excessive pulse-to-pulse energy variations. To overcome this variation, a sufficiently large number of pulses is required. Improvements to the excimer laser pulse stability continue, which reduces the number of pulses required to achieve acceptable exposure dose uniformity. With fewer pulses needed, the scanning speed of the step-and-scan system can increase, which ultimately increases productivity.[9]

The excimer laser will probably be used as an exposure source for at least another technology generation with the argon-fluoride (ArF) laser at a wavelength of 193 nm. There are no fundamental laser changes required to change from a 248-nm KrF laser to a 193-nm ArF laser. However, optical materials have undesirable absorbance and are more sensitive to laser damage from factors such as optical system heating at the 193-nm wavelength.[10] This condition requires lens systems that are laser damage resistant. An industrial grade F_2 excimer laser at a wavelength of 157 nm has been demonstrated as a potential light source for 0.15 μm critical dimension.

Spatial Coherence. Recall that light is an electromagnetic wave. A light beam has *spatial coherence* when points on different waves remain in phase to one another as the waves propagate. The light waves move in unison (see Figure 14.10). A standard room light bulb has no spatial coherency (completely incoherent). Light beams from excimer lasers have a low amount of spatial coherence, which differs from the beams of conventional lasers. Spatial coherence is

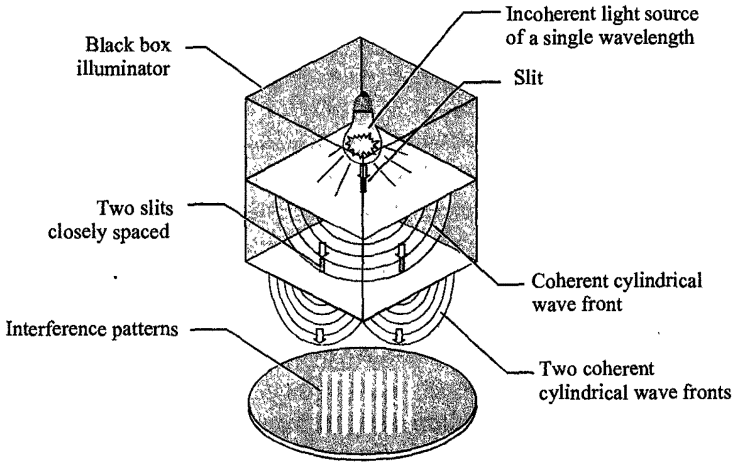


FIGURE 14.10 Spatial Coherence

controlled through optics to minimize interference patterns that can be formed in the image. If not controlled, the interference may appear as a grainy pattern of bright and dark spots on the resist, referred to as speckle.[11]

Exposure Control. ■ A uniform dose of UV light is critical for resist exposure. The exposure dose must be repeatable from exposure to exposure and from wafer to wafer. The exposure latitude for a DUV resist is around 1% in dose variability.[12] The variation in photolithography processes, equipment, and materials requires stringent exposure control.

Exposure control in photolithography is achieved by measuring the intensity of the UV light source at the surface of the wafer with a *dose monitor.* The exposure dose is measured at different locations in the exposure field, permitting the calculation of the percent uniformity of the dose. A photodetector and an electronics circuit are used on automated steppers and step-and-scan systems to monitor and control the exposure dose through use of a shutter or by varying the speed of the scan.

Optics

Optics is the study of the physical properties and composition of light. Optics is important because lithography is based on an optical imaging process used to transfer the reticle pattern to the photoresist. The quality of the resist pattern can be limited by poor-quality optics. All photolithography equipment currently used for high-volume wafer fabrication is based on optical lithography.

Reflection of Light ■ The *law of reflection* describes the relationship between an incident light ray and the corresponding reflected ray, stating that the angle of incidence is equal to the angle of reflection (see Figure 14.11). This law is true whether the reflecting surface is rough or smooth.

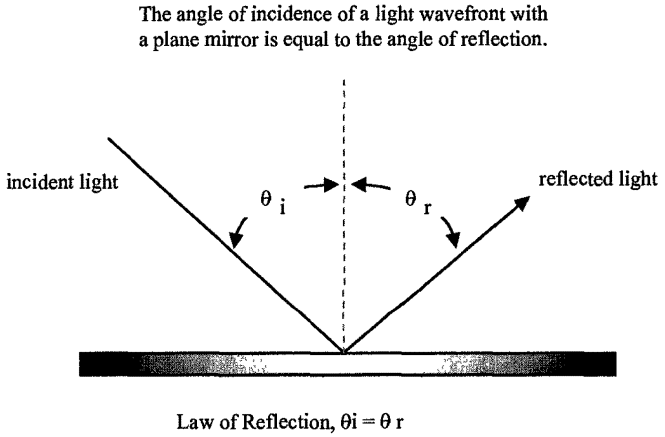


FIGURE 14.11 Law of Reflection

An example of the law of reflection is a plane mirror. A mirror reflects light from its surface and creates a virtual reversed image of an object. The image is said to be virtual because it appears to the viewer as though the object exists behind the mirror, whereas the image on the mirror surface is actually a reversed image reflection of the real object. Mirrors and reflective optics have many applications in steppers and step-and-scan systems, such as for beam orientation or for illuminators that shape and focus light (see Figure 14.12).

Refraction of Light ■ When light passes from one transparent medium into another, such as from air through a glass window, the light changes direction. The change in direction of a light ray when passing from one transparent medium into another is called *refraction.* Refraction of light is caused by the difference in the speed of light in two different media. Light traveling through a uniform medium, such as air, travels at a certain speed. As light enters into and passes through a new medium, such as glass, its speed actually decreases. This decrease occurs because the glass is optically a more dense material. The *relative index of refraction, n,* represents how much the light ray

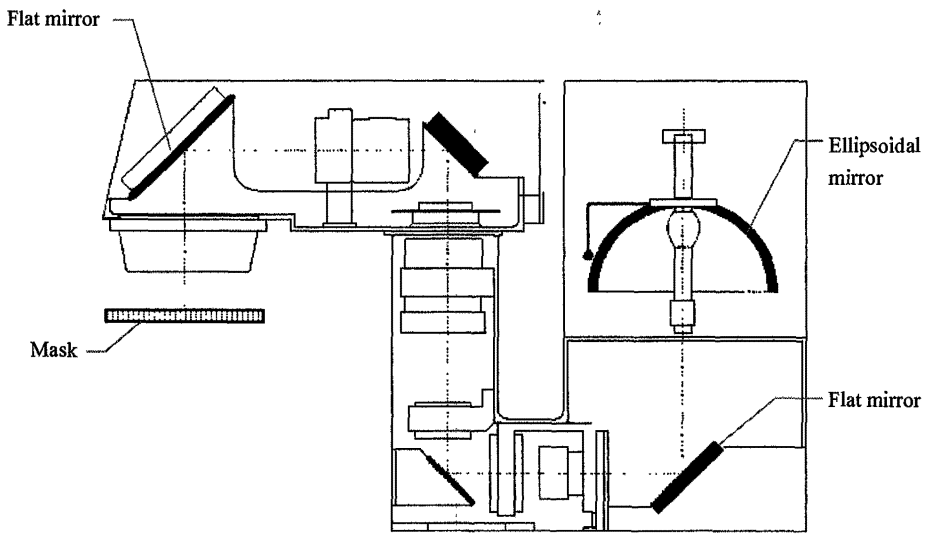


FIGURE 14.12 Application of Mirrors
(Used with permission from Canon USA, illuminator for mask aligner)

bends as it passes through the interface of the two media based on its change in velocity (see Figure 14.13). The *absolute index of refraction* compares the speed of light in a vacuum to the speed of light in the chosen medium. Therefore it is only stated for one medium and the vacuum is assumed. Examples of absolute index of refraction for different media are given in Table 14.4.[13] The refraction of light is also dependent on the wavelength, λ, of the light ray that passes from one medium into another medium.

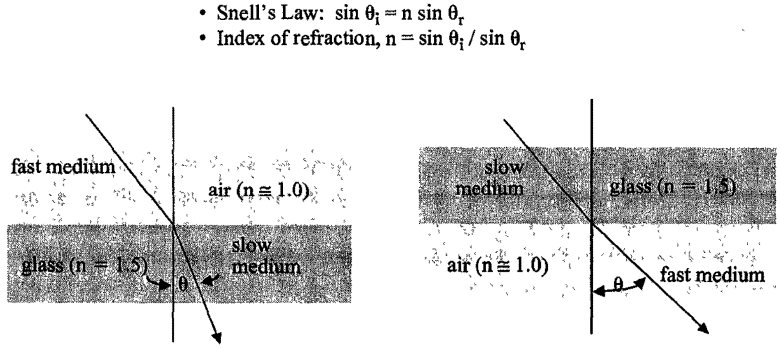


FIGURE 14.13 Refraction of Light Based on Two Mediums

TABLE 14.4 Absolute Index of Refraction for Select Materials

Material	Index of Refraction (n)
Air	1.000293
Water	1.33
Fused silica (amorphous quartz)	1.458
Diamond	2.419

Lens ■ A *lens* is defined as an optical element that refracts light from an object passing through it to form an image of the object. We will consider an individual lens, but optical systems in photolithography consists of many different lenses (refractive) and mirrors (reflective) in the optical system (see Figure 14.14.) Lenses are important in the optical system of photolithography equipment because of the need to project the image of the reticle pattern onto the photoresist. This projection must be done with the proper resolution, dimensional control, and alignment. Lenses and refractive optics in photolithography steppers and step-and-scan systems play a critical role in achieving the resolution needed to achieve the CD linewidths in modern wafer fabrication.

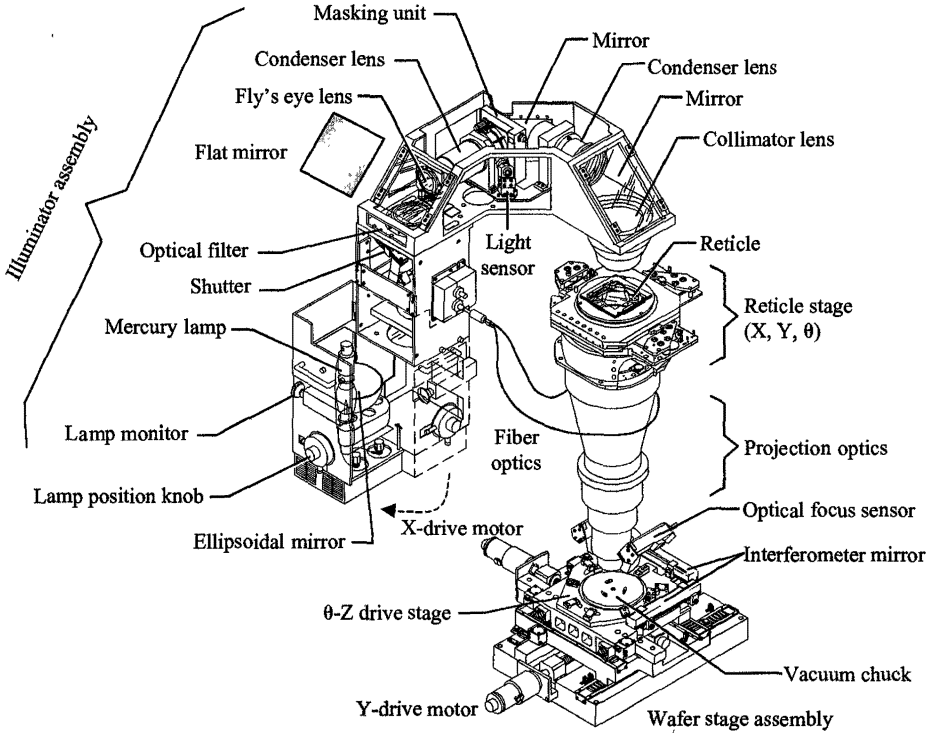


FIGURE 14.14 Optical System of Lenses
(Used with permission from Canon USA, FPA-2000 iI exposure system)

A lens has either one or both surfaces as spherical-shaped, which defines whether the lens is converging (convex) or diverging (concave). Lenses refract light in such a way that light rays converge (see Figure 14.15) or diverge (see Figure 14.16) on a principal focus. The principal focus, or *focal point,* is where the light rays are refracted and will converge—the image carried by the light is sharp and in focus. The distance from the center of the lens to the focal point is called the *focal length.*

Lens Material. Lenses have traditionally been made of glass. The lens material is an important variable as the exposure wavelength is continually reduced. For 248-nm wavelength DUV, a suitable lens material is fused silica. It has less light absorption at the DUV wavelengths. At the 193-nm DUV and 157-nm VUV wavelength, calcium fluoride (CaF_2) is being investigated as a possible candidate for lens material.

Traditional optical materials such as glass have greater absorbance and are more sensitive to laser damage at the 248-nm KrF wavelength.[14] Absorption causes a loss in exposure power and induces heat in the optics, which leads to refractive index changes and imaging problems. Thermal effects can also cause focus changes due to optical system heating from DUV laser light sources.

Another concern regarding lens materials is that a laser beam can create compaction damage. *Lens compaction* is a structural rearrangement of the lens material that causes densification of the lens material (see Figure 14.17). Compaction occurs in lens materials, including fused silica. It is not well understood, but it occurs due to the total cumulative laser beam exposure and peak power density.

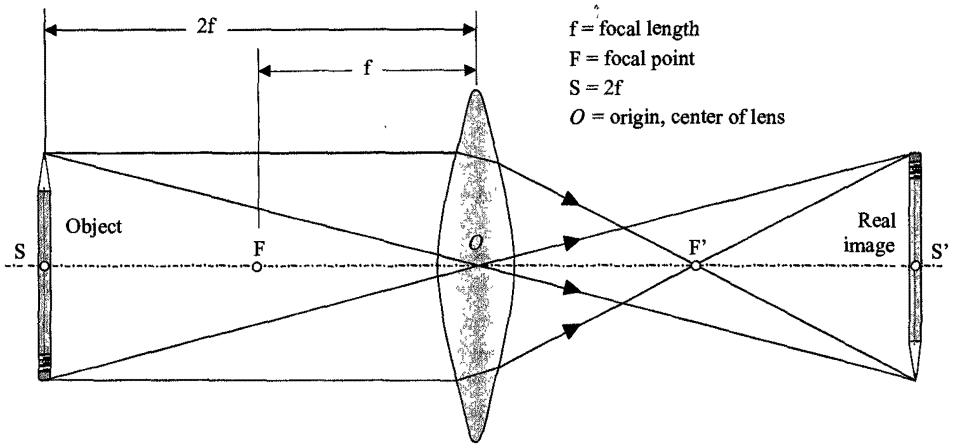


FIGURE 14.15 Converging Lens with Focal Point

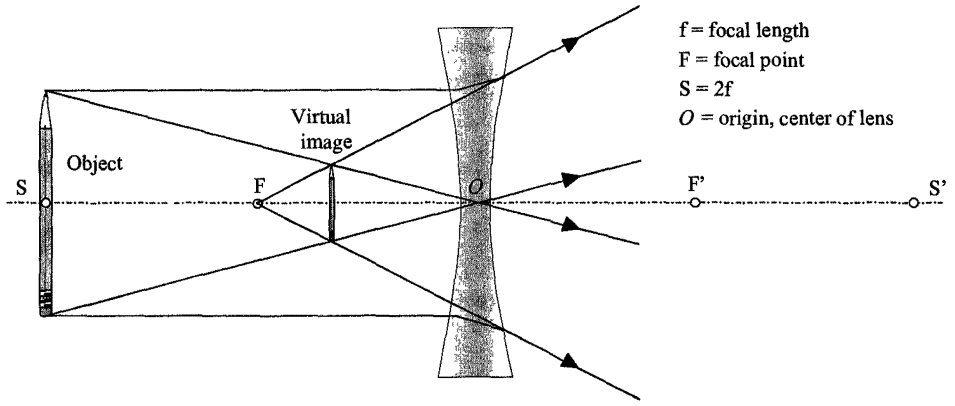


FIGURE 14.16 Diverging Lens with Focal Point

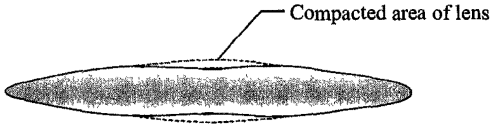


FIGURE 14.17 Laser-Induced Lens Compaction

It can increase the lens material's refractive index in the region traversed by the laser beam. If the index of refraction changes even slightly, then there could be a change in the light wave path, which would lead to loss of image quality. The control of compaction for DUV wavelengths is being researched.

Lenses used in photolithography optical systems are of the finest quality materials and workmanship, but they are not perfect. Deviations from the ideal lens behavior that result from design, fabrication, or usage flaws are referred to as *aberrations.* There are different types of aberrations, such as inaccurate lens surfaces. For the most part, the lens system designer designs the optical system to minimize individual lens aberrations.[15]

Diffraction ■ Light travels in straight lines. When light passes through a narrow opening or past a sharp edge, interference patterns occur along the edge of the opening. The effect is a fuzzy image rather than the expected sharp edge that occurs between light and shadow (see Figure 14.18 on page 380). The light appears to bend around the slit edges. This phenomenon is referred to as *diffraction.*

- Light travels in straight lines.
- Diffraction occurs when light hits edges of objects.
- Diffraction bands, or interference patterns, occur when light waves pass through narrow slits.

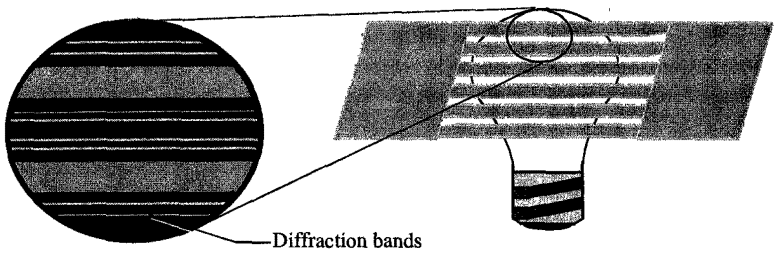


FIGURE 14.18 Interference Pattern from Light Diffraction at Small Opening

You can experience diffraction by putting two fingers close together and looking through them toward a light. The edge of your fingers is not sharp. Diffraction of light passing through a small opening causes an unexpected light intensity profile. In essence, regions outside the boundary are illuminated and the light intensity profile does not have a sharp edge. The central spot is bright and bounded by bands of decreasing intensity which are called *diffraction orders*. The amount of diffraction depends on the width of the opening and the wavelength of the light.

Light diffraction is a concern in photolithography because of the extremely small patterns of sharp edges and narrow spaces on reticles. Light during exposure must pass through these patterns (see Figure 14.19). Diffraction patterns rob exposure energy and scatter it, leading to exposure of unwanted areas of the photoresist. The problem is worse in small holes, such as small contact openings of 200 nm. The interference patterns caused by diffraction can make small contact holes and small lines difficult to print.

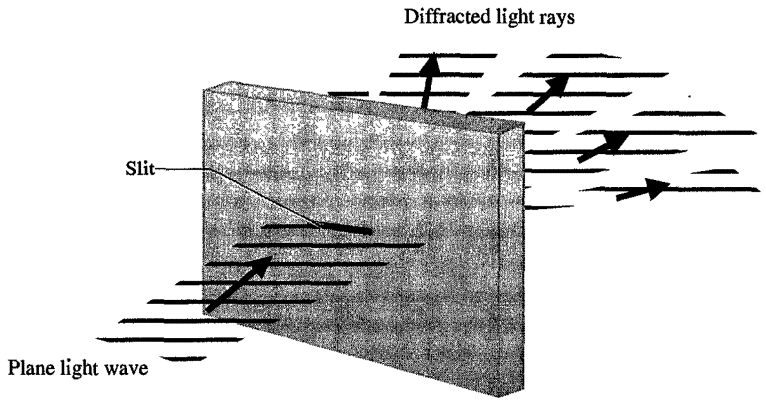


FIGURE 14.19 Diffraction in a Reticle Pattern

Numerical Aperture ■ A lens is able to capture some diffracted light (see Figure 14.20). The ability of a lens to collect diffracted light is referred to as the *numerical aperture* (*NA*) of the lens. For a given lens, the NA is a measure of how much diffracted light the lens can accept and image by converging the diffracted light to a single point.

The numerical aperture is defined by the following formula:

$$NA = (n) \sin \theta_m \approx (n) \frac{\text{radius of lens}}{\text{focal length of lens}}$$

Where, n = index of refraction of the image medium ($n \approx 1$ for air)
θ_m = angle between the optical principal axis and the marginal ray at the edge of the lens

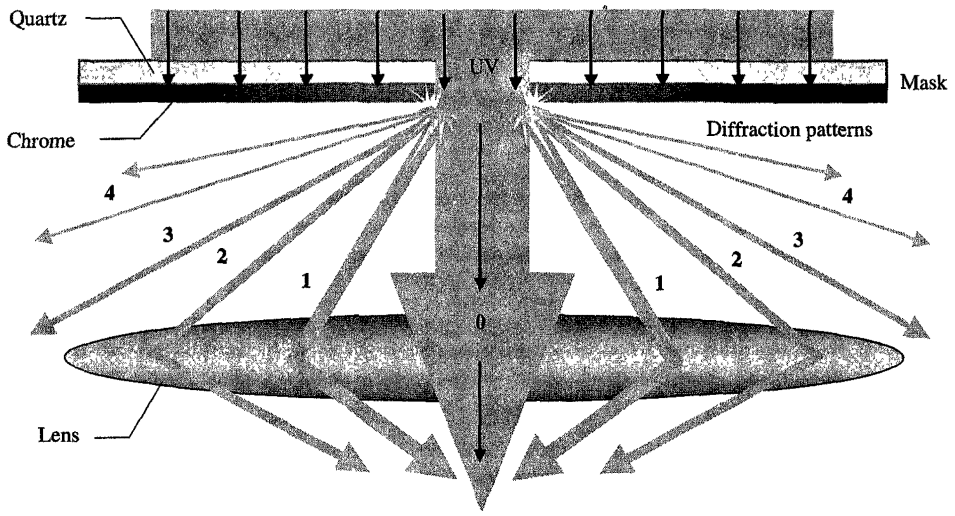


FIGURE 14.20 *Lens Capturing Diffracted Light*

Note that the value for sin θ_m can be approximated by using its trigonometric relationship. This approximation highlights how increasing the radius of the lens will increase the NA and capture more diffracted light. With an increased NA, more of the diffracted light can be converged to a single point for imaging (see Figure 14.21). However, increasing the radius of the lens to increase the NA also means more complicated and costly optical systems.

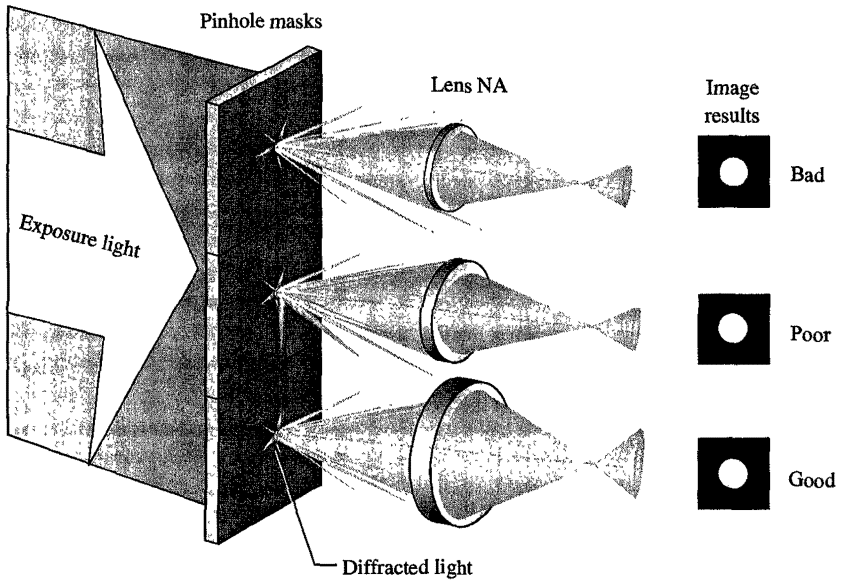


FIGURE 14.21 Effect of Numerical Aperture on Imaging

NA values are typically specified for photolithography steppers and step-and-scan systems. NA has improved considerably over the years. For an air or vacuum medium, the NA value must be less than or equal to 1. Some typical NA values for photolithography equipment are provided in Table 14.5.

TABLE 14.5 Typical NA Values for Photolithography Tools

Type of Equipment	NA Value
Scanning projection aligner with mirrors (1970s technology)	0.25
Step-and-repeat	0.60 to 0.68
Step-and-scan	0.60 to 0.68

Antireflective Coatings ■ Exposure light passes through a reticle to pattern the resist. Below the resist is the underlying layer that will ultimately be etched and patterned. If this underlying film is reflective, as with metal and polysilicon layers, then light rays reflect off this film and potentially damage the adjacent resist. This damage can adversely affect CD control. The two primary light reflectivity problems are reflective notching and standing waves. *Reflective notching* occurs when vertical surfaces on the sides of etched structures reflect light into the resist where exposure is not intended (see Figure 14.22).

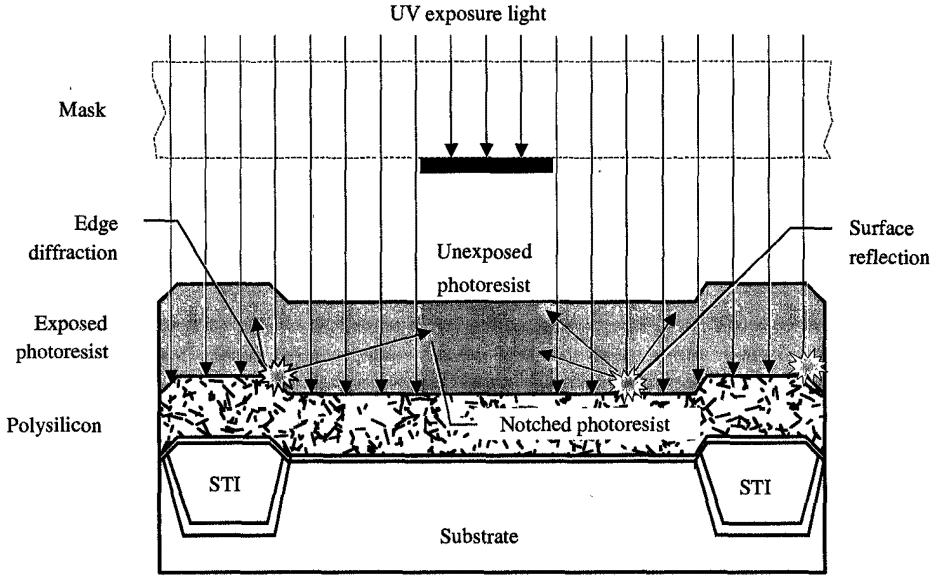
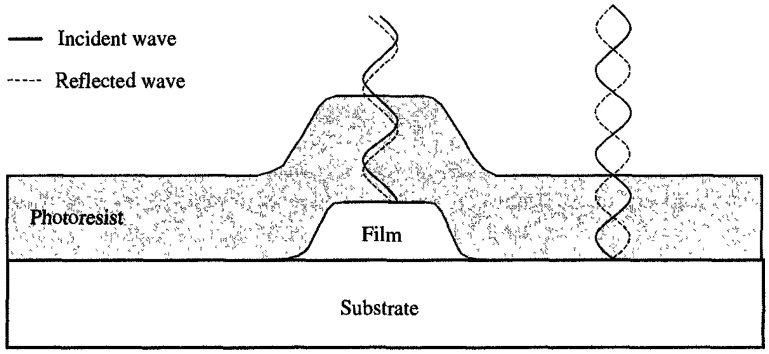


FIGURE 14.22 Photoresist Reflective Notching Due to Light Reflections

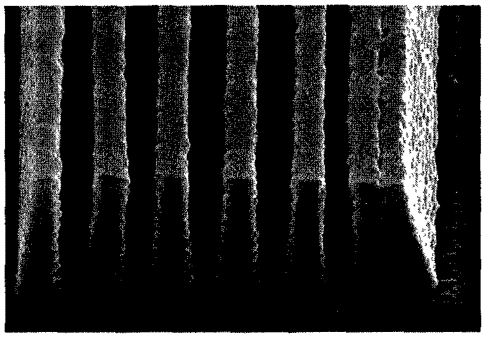
Standing Waves. An example of wave reflection and interference in photolithography is the phenomenon of standing waves. If a layer of photoresist is applied to a reflective wafer surface and exposed to monochromatic light, then the incident light wave striking the resist passes through the resist layer and is reflected from the surface of the wafer (see Figure 14.23). *Standing waves* represent interference between the incident light waves and reflected light waves, which causes nonuniform exposure along the thickness of the photoresist film. The occurrence of standing waves is more pronounced with DUV resists because many wafer surfaces (e.g., oxide, nitride, and polysilicon) are more reflective at the shorter DUV wavelengths.[16] After exposure, the sides of the resist features have striations of overexposed and underexposed areas. Standing waves essentially degrade the resolution of the image in the resist.

Using an *antireflective coating* (*ARC*) applied directly to the reflective substrate surface reduces standing wave effects in photoresist (see Figure 14.24). ARCs reduce unintended light reflection by suppressing the exposure light, with the latest ARCs capable of suppressing 99%



Standing waves cause nonuniform exposure along the thickness of the photoresist film.

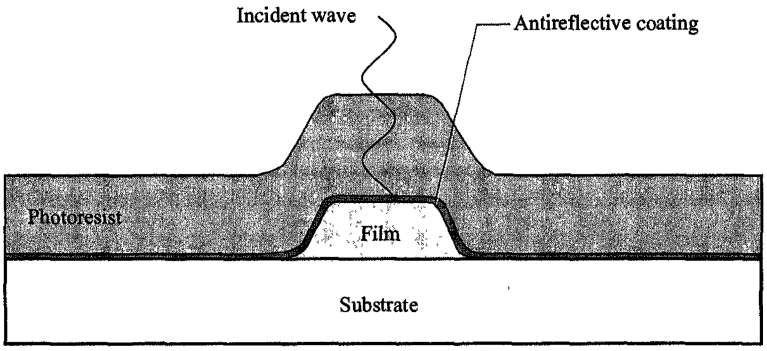
FIGURE 14.23 Incident and Reflected Light Wave Interference in Photoresist



Effect of Standing Waves in Photoresist
(Photo courtesy of Grant Willson's research group at the University of Texas at Austin)

of the substrate-reflected light. They are deposited on the wafer as a thin layer, typically from 200 to 2000 Å, depending on the type of ARC and material used.[17] Dyes can also be added to the resist to help prevent light wave interference. In addition, a post-exposure bake (PEB) between exposure and development can reduce the extent of standing wave striations in conventional i-line resists. The PEB redistributes the photoactive compound (PAC) in the resist and allows for straighter resist sidewall profiles by reducing standing waves.

There are two basic types of ARCs: bottom antireflective coating beneath the photoresist to reduce substrate reflections, and top antireflective coating deposited over the resist to reduce secondary reflections from the resist surface. The bottom ARC has emerged as the most effective method in reducing reflections and problems such as standing waves and, therefore, will be the focus of our discussion.



The use of antireflective coatings, dyes and filters can help prevent interference.

FIGURE 14.24 Antireflective Coating to Prevent Standing Waves

Bottom ARCs. A *bottom antireflective coating (BARC)* is used to suppress unintended light reflection from a reflective layer that is below the resist, as shown in Figure 14.25 on page 384. The BARC material is an organic or inorganic dielectric material that is applied to the wafer before the photoresist.

Organic ARCs reduce reflection by absorbing light and are typically spin-coated on the wafer in the same manner as the photoresist. Inorganic ARCs are deposited by plasma-enhanced chemical vapor deposition (PECVD). Inorganic ARCs do not absorb light but instead work by phase-shift cancellation of specific wavelengths based on the refractive index, film thickness, and other parameters (see Figure 14.26 on page 384). Successful phase cancellation of light requires very tight control of process parameters, such as a thickness tolerance for the BARC of 15 Å.[18] TiN, used as a diffusion barrier for interconnect metal, is also a good antireflective coating. However, the reflectivity of materials changes for shorter wavelengths, making interference effects more difficult to control.

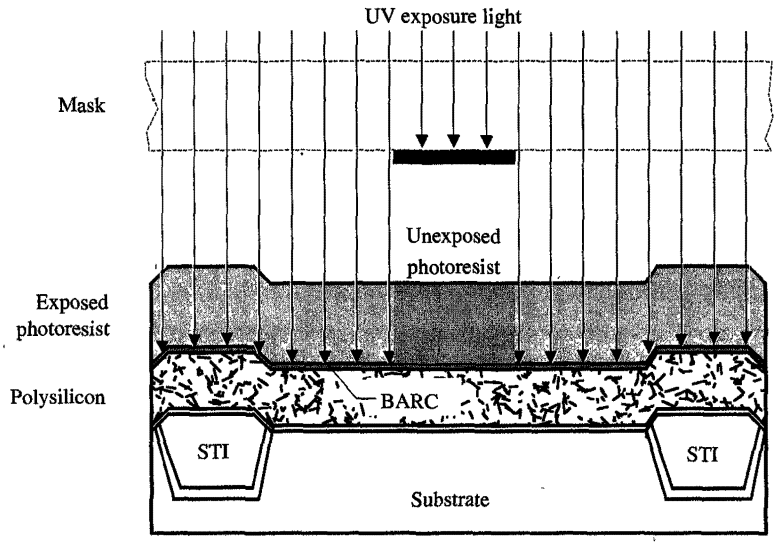


FIGURE 14.25 Light Suppression with Bottom Antireflective Coating

One factor in selecting an ARC is its ability to be removed after the completion of the photolithography process step. In some cases organic ARCs (primarily top ARCs) are aqueous-based and relatively easy to remove by rinsing during the development step. Inorganic ARCs are more difficult to remove, especially if their chemistry is similar to the underlying layer. This ARC layer is sometimes left on the wafer surface and becomes a part of the device.

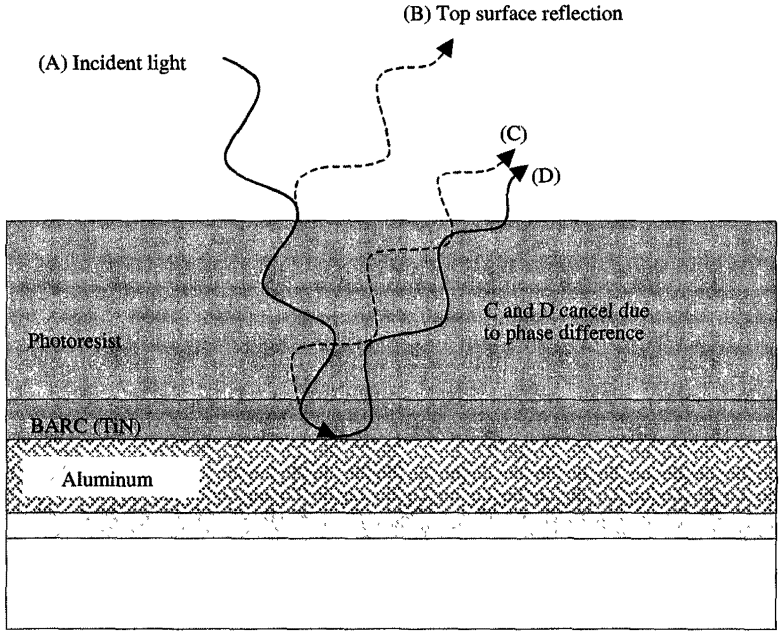


FIGURE 14.26 BARC Phase-Shift Cancellation of Light

Top ARCs. The *top antireflective coating* (*TARC*) reduces reflection at the interface between the resist surface and air (see Figure 14.27). TARC materials do not absorb light, but instead act as a transparent thin-film interference layer that uses destructive interference between light rays to eliminate reflectance.[19]

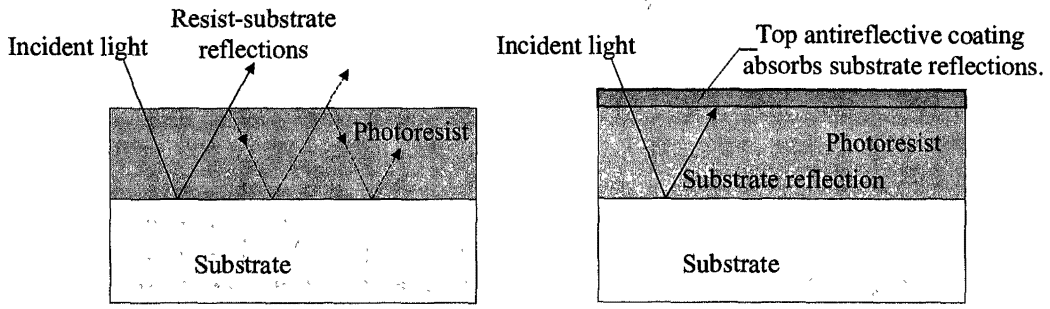


FIGURE 14.27 Top Antireflective Coating

Resolution

In photolithography, *resolution* is defined as the ability to discretely discern pairs of closely spaced features on the wafer (e.g., equal lines and spaces). This quality is shown in Figure 14.28. Resolution is critical given the high packing density for wafer features in advanced IC semiconductor manufacturing. Resolution is an important parameter for any optical system and is critical for photolithography because of the need to print extremely small features sizes for wafer fabrication.

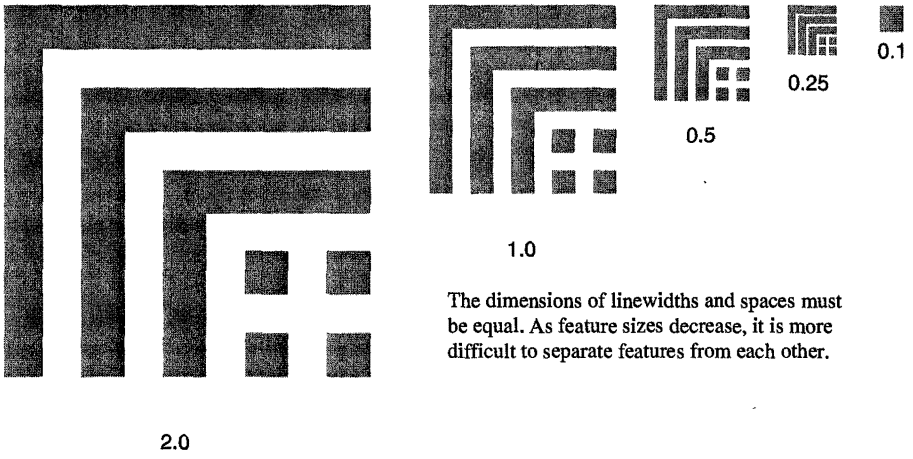


FIGURE 14.28 Resolution of Features

The formula for resolution, R, is:

$$R = \frac{k\lambda}{NA}$$

Where, k = factor that represents specific applications, with a range between 0.6 to 0.8
λ = wavelength of the light source
NA = numerical aperture of the exposure system

This formula shows that there are three parameters in photolithography that affect the ability to resolve fine geometry patterns in photoresist:

1. wavelength, λ
2. numerical aperture, NA
3. process factor, k

It should now be obvious why decreasing the wavelength, λ, of the exposing light source is important for improving resolution. A decrease in λ will improve the resolution capability of the lithography system. In other words, smaller wavelength is better. The other important parameter for

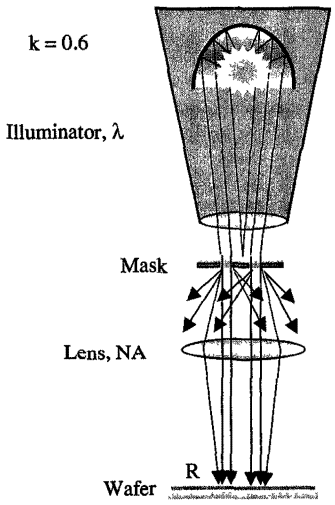
improving resolution is increasing the NA of the projection lens. Lenses with a high NA also have a high resolution. However, recall that to increase NA also requires a larger diameter lens, which becomes costly.

The third parameter, k, represents process factors of the optical system and can affect resolution. However, there are practical limitations to decreasing k much below 0.6. There are some resolution enhancement techniques available, such as phase-shift masks (PSM) and optical proximity correction (OPC) that are becoming important for reducing k to improve pattern resolution. These techniques are discussed later in this chapter.

Calculating Resolution ■ When given the wavelength, λ, numerical aperture, NA, and process factor, k, it is possible to calculate the predicted resolution, R, of an optical system (see Figure 14.29). Consider the following example:

$$\lambda = 193 \text{ nm}$$
$$NA = 0.60$$
$$k = 0.6$$
$$R = \frac{k\lambda}{NA} = \frac{(0.6)\,(193 \text{ nm})}{0.6} = 193 \text{ nm}$$

For this optical system, the resolution of the smallest printable pattern is predicted to be 193 nm. If the wavelength of the exposure source is decreased, then the resolution will decrease. As the NA increases, the resolution will decrease. However, as explained in the following section, there is a price to pay for increasing the NA of the system, and that is decreased depth of focus.



$$R = \frac{k\lambda}{NA}$$

	λ	NA	R
i-line	365 nm	0.45	486 nm
	365 nm	0.60	365 nm
DUV	193 nm	0.45	257 nm
	193 nm	0.60	193 nm

FIGURE 14.29 Calculating Resolution for a Given λ, NA, and k

Depth of Focus ■ The range around the focal point over which the image is continuously in focus is called the *depth of focus*, or *DOF* (see Figure 14.30). The *center of focus* (*COF*) is the point from the center of the lens where the best imaging occurs. The depth of focus is the range above and below the center of focus where the exposure energy is relatively constant. The COF may not be exactly at the middle of the resist layer, while the DOF should extend beyond the upper and lower surface of the resist coating. The actual usable DOF of any exposure system should be confirmed through tests conducted with the relevant processing parameters and environmental conditions. The goal is to find and maintain the best focus across the wafer and from wafer to wafer.

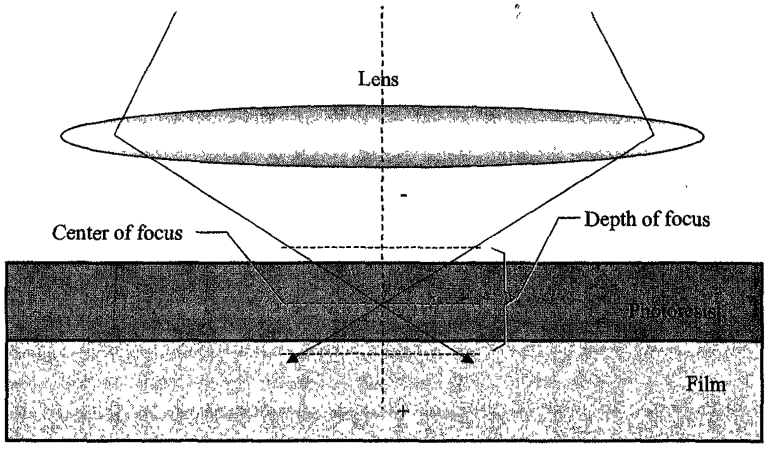


FIGURE 14.30 Depth of Focus (DOF)

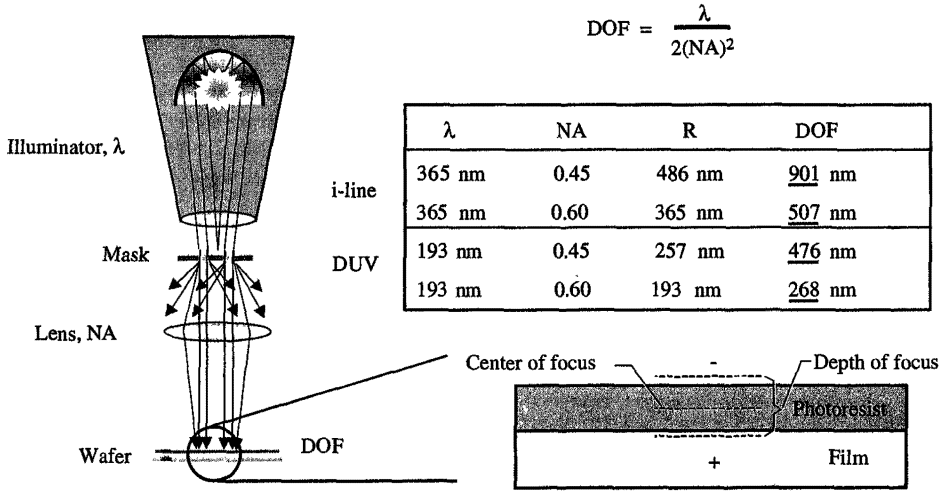
The equation to describe the DOF is:

$$\text{DOF} = \frac{\lambda}{2(\text{NA})^2}$$

Where, λ = wavelength of the exposing light
NA = numerical aperture of the optical system

Depth of focus, also known as *depth of field* (*DOF*), is commonly used in photography work to indicate the acceptable focus range of a camera's lens. Have you ever seen a picture of someone in which the background is out of focus? The photograph was taken with a camera of reduced DOF. Whereas a depth of focus of 30 cm for handheld cameras is common, in semiconductor photolithography DOF values of 1 μm or less are the norm.

The DOF is calculated using the λ of the illumination source and the NA of the projection lens. As the numerical aperture of a lens increases, more optical detail is captured and the resolution capability of the system increases. The significance of the DOF equation is that if resolution is increased, then the depth of focus will decrease (see Figure 14.31). Improving patterning resolution is imperative for submicron feature sizes. However, the resulting decrease in the DOF severely reduces the process latitude of the optical system.



	λ	NA	R	DOF
i-line	365 nm	0.45	486 nm	901 nm
	365 nm	0.60	365 nm	507 nm
DUV	193 nm	0.45	257 nm	476 nm
	193 nm	0.60	193 nm	268 nm

FIGURE 14.31 Resolution Versus Depth of Field for Varying NA

Resolution Versus Depth of Focus ■ In optical lithography, two critical parameters for the image quality are resolution and depth of focus. The semiconductor industry has always been challenged by the competing goals of achieving better resolution to pattern critical dimensions while simultaneously maintaining acceptable depth of focus. Any aspect of the photolithography tool or process that interferes with the ability of the wafer to lay flat, stable, and parallel to the focal plane of the lens will affect the focus quality of the exposure process. If the image plane moves away from the plane of best focus in the resist, image quality suffers. Imagine a stepper having a DOF = 1 μm. Suppose a human hair (diameter ≈ 100 μm) were to fall between the wafer stage and the wafer. The wafer would be lifted roughly 99 μm beyond the focal point of the stepper's lens. The tool would not be able to achieve focus nor be able to successfully align or expose the wafer to the reticle. Photolithography tools have introduced techniques in their equipment that compensate for factors such as poor wafer flatness and equipment vibration but cannot compensate for gross conditions of contamination and damaged parts.

The wafer surface has traditionally been nonplanar due to surface topography introduced during deposition and etching steps. In the 1980s, this wafer surface topography limited resolution because the optical system was not able to adequately focus on all wafer surfaces. Many different techniques were introduced to try to reduce the surface topography during this era.

Surface Planarity. The most important technique to planarize (make flat) wafer surfaces is a planarization process known as chemical mechanical planarization (CMP). CMP was introduced into wafer fabrication in the 1990s and has made a significant contribution toward planarizing the wafer surface to meet reduced depth of focus requirements (which permits increased pattern resolution). CMP has been a major factor in reducing nonplanar wafer surface topography for 0.25-μm critical dimensions and below. The significance of CMP for photolithography is that it makes possible the reduction of the depth of focus to achieve a higher pattern resolution.

PHOTOLITHOGRAPHY EQUIPMENT

The history of photolithography since the early days of wafer fabrication can be separated into five major equipment eras. Each era is roughly based on the type of equipment needed to achieve the CD resolution necessary at the time. The five microlithography equipment eras are:

- Contact aligner
- Proximity aligner
- Scanning projection aligner (scanner)
- Step-and-repeat aligner (stepper)
- Step-and-scan system

Contact Aligner

The *contact aligner* was the primary method of photolithography during the SSI era until the early 1970s. It was used in production mode for linewidth dimensions of about 5 μm and above. Although linewidths of 0.4 μm are possible, the contact aligner is not widely used today.

The mask for a contact aligner has the complete array of all die patterns to be photographed on the wafer surface. The wafer is coated with photoresist and mounted on a stage that has manual knobs to control left, right, and rotational position (a stage is a generic name for a positioning device with x, y, and rotational, or θ, positioning). The mask and wafer are both viewed simultaneously through a microscope having split vision optics (see Figure 14.32). The mask pattern is then aligned to the pattern on the wafer through manual operator control of the stage position.

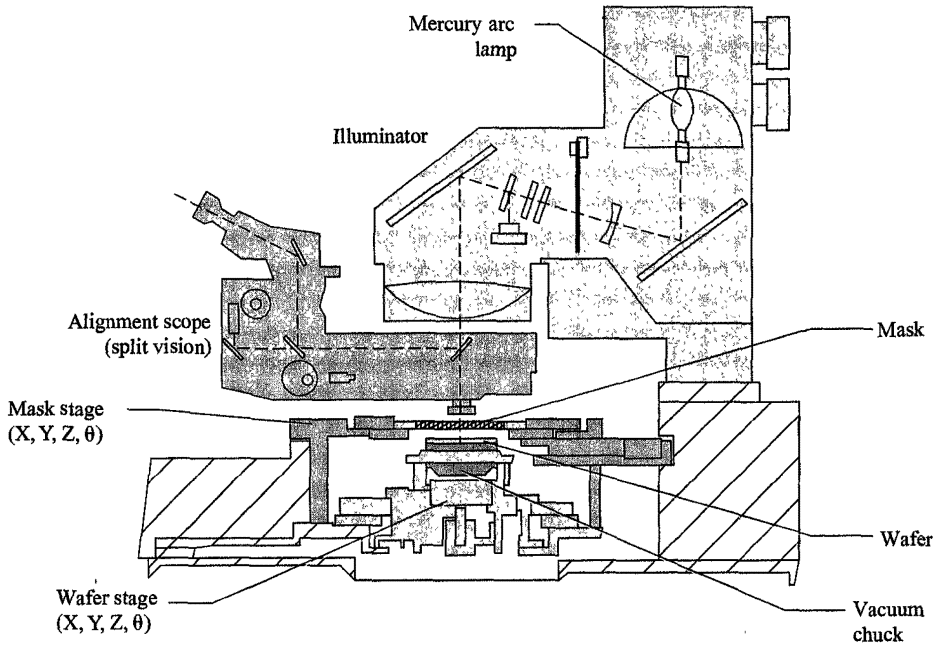


FIGURE 14.32 Contact/Proximity Aligner System
(Used with permission from Canon USA)

Once the mask is aligned to the wafer, then the mask is brought into direct contact with the resist coating on the wafer surface, which is why the equipment is called a contact aligner. At this time, the wafer and mask are exposed to ultraviolet (UV) rays. The UV rays pass through the transparent portions of the mask and the mask pattern is transferred to the resist.

Contact aligner systems were operator dependent and prone to contamination because the mask was placed in direct contact with the resist. Particulate contamination damaged the soft resist layer, the mask, or both, requiring the mask to be replaced every 5 to 25 operations. There were also resolution problems in the immediate area of any particle. As wafer sizes increased, there were overlay accuracy problems from attempting to pattern the entire wafer with one mask because alignment tolerances had to be held over wider areas.

Contact aligner printing actually can produce good image resolution on the wafer surface because the mask pattern and wafer are as close to each other as possible. This proximity reduces image distortion. However, contact alignment is very operator dependent, which introduces problems with repeatability and control.

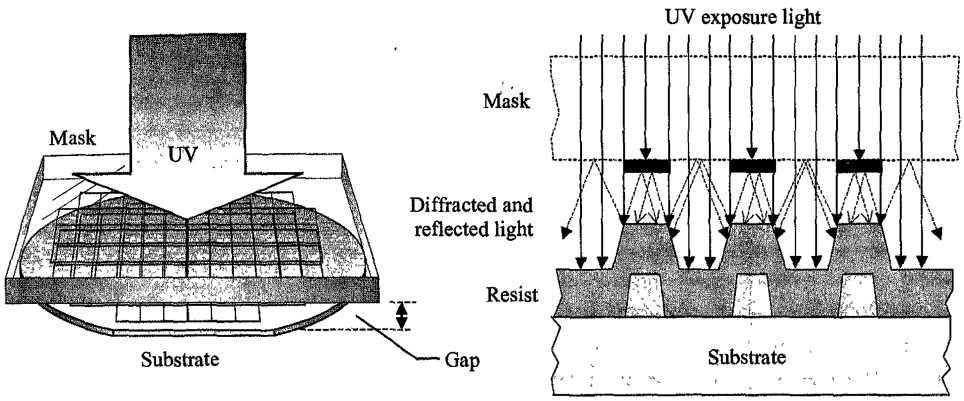
Proximity Aligner

The *proximity aligner* evolved from the contact aligner and was common in the early 1970s during the SSI and early MSI era. These aligners are still used today in low-volume laboratory applications or older wafer fabs for discrete components where retooling is not economically feasible. They are suitable for linewidth dimensions of 2 to 4 μm, depending on factors such as the reflectivity of the substrate surface.

In proximity alignment the mask, which continues to transfer the entire wafer pattern, does not make direct contact with the resist. It is positioned in close contact to the resist surface, with a gap of approximately 2.5 to 25 μm between the mask and the resist on the wafer surface. The light originating from the source is collimated, which means the light rays are forced to be parallel with each other.

The proximity aligner was an attempt to alleviate the contamination problems associated with the contact aligner by creating a gap between the resist surface and mask that would not necessarily trap particles. Even though the magnitude of the gap was controlled, the performance of the proximity aligner was reduced because of the light scattering as the UV rays passed through the transparent regions of the mask and the air (see Figure 14.33 on page 390). This condition impaired

the system's resolution capability, which was a major problem due to the need to reduce the linewidth critical dimension.



Diffraction of light on edges results in reflections from underside of mask causing undesirable resist exposure.

FIGURE 14.33 Edge Diffraction and Surface Reflectivity on Proximity Aligner

Scanning Projection Aligner

The industry recognized the need to move away from any form of contact or near contact alignment system due to its contamination problems, edge diffraction, resolution limitations, and operator dependency. The development of the *scanning projection aligner* (also referred to as *scanner*) in the early 1970s attempted to address these problems. Scanning projection aligners were the dominant lithography exposure tool in the late 1970s and early 1980s.[20] These aligners are still used today in older wafer fabs. They are suitable for noncritical layers containing linewidths greater than 1 μm.

The *scanning projection aligner* concept is to project a full wafer mask with a 1:1 image onto the wafer surface using a mirror system (i.e., based on reflective optics). Since the mask is 1X, there is no magnification or reduction involved and the pattern on the mask has the same dimensions as the pattern on the wafer.

The UV light rays are focused onto the wafer through a narrow slit, allowing a uniform source of light (see Figure 14.34). The mask and resist-coated wafer are mounted on a scanning carriage and moved in unison across the narrow beam of UV light to expose the resist on the wafer. As the scanning motion takes place, the image of the mask is eventually printed on the wafer surface.

A major challenge of scanning projection aligners was making a good 1X mask that contained all the chips on the wafer. If the chip had submicron feature sizes, then the mask also had submicron dimensions. As submicron feature sizes were introduced, this photolithography approach made it difficult for the mask maker to have no defects in the mask.

Step-and-Repeat Aligner (Stepper)

The mainstay of the 1990s microlithography equipment for wafer fabrication is the *step-and-repeat aligner* (commonly referred to as a *stepper*). Steppers have their distinct name because the tool projects only one exposure field (which may be one or more chips on the wafer), and then steps to the next location on the wafer to repeat the exposure. Steppers were first commercialized in the early 1980s.[21] Though not universally accepted at first, optical lithography steppers have dominated IC fabrication since the later 1980s, primarily for applications with critical dimensions down to 0.35 μm (conventional i-line photoresist) and some 0.25 μm (DUV photoresist).

A stepper uses a reticle, which contains the pattern in an exposure field corresponding to one or more die. A mask is not used in a stepper since a mask contains the entire die matrix. The optical projection exposure system of steppers uses refractive optics to project the reticle image onto the wafer (see Figure 14.35).

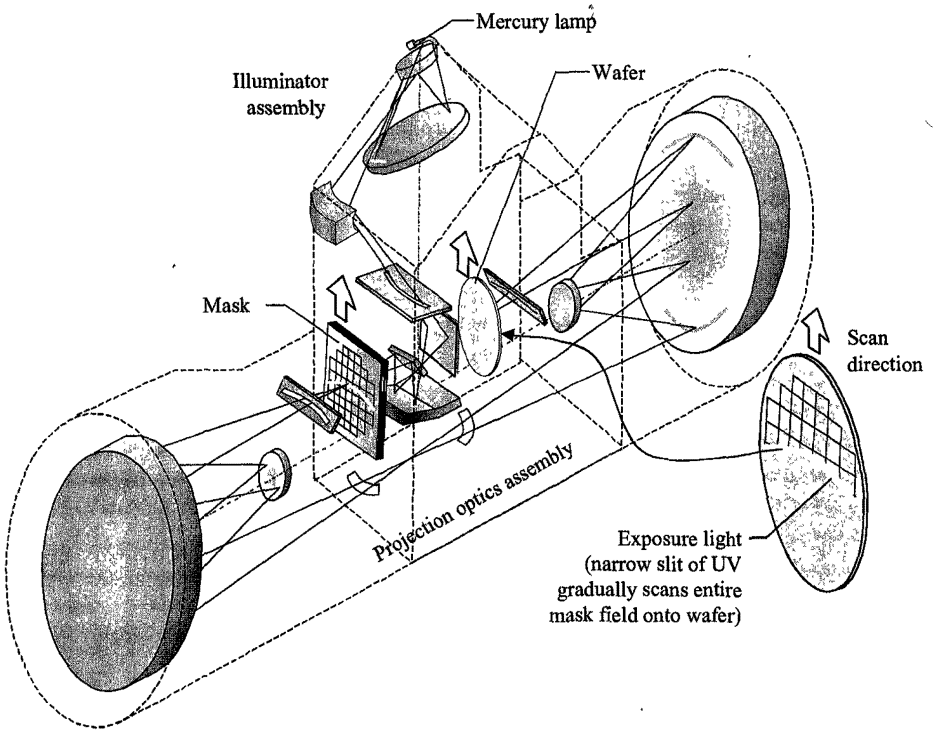


FIGURE 14.34 Scanning Projection Aligner
(Redrawn with permission from Silicon Valley Group Lithography Systems, Perkin-Elmer 500 Micralign)

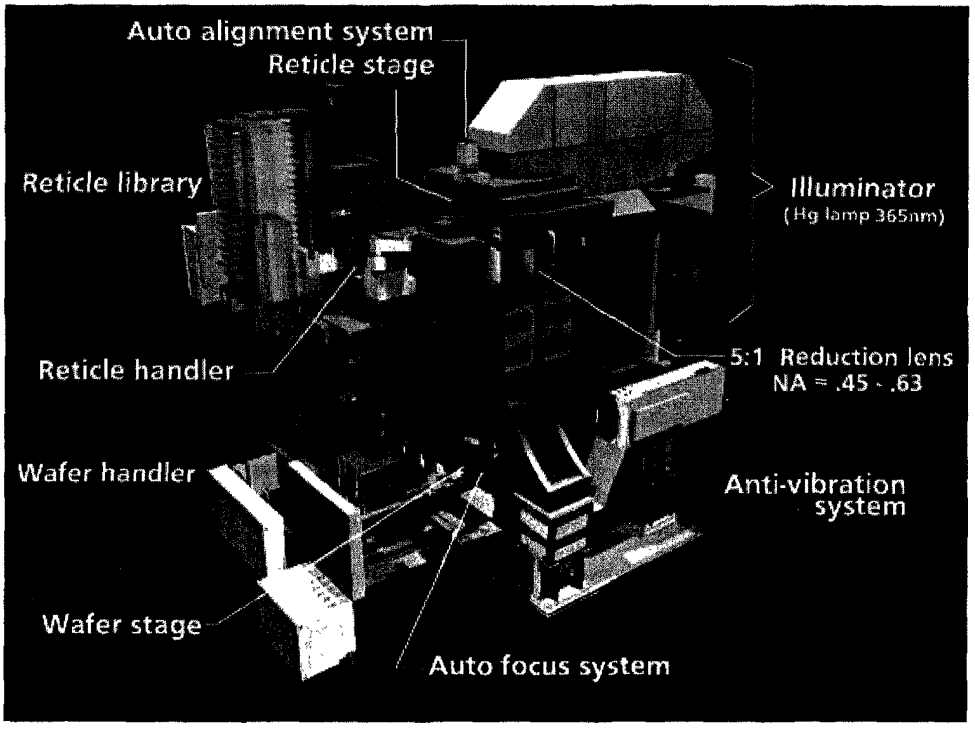


FIGURE 14.35 Step-and-Repeat Aligner (Stepper)
(Used with permission from Canon USA, FPA-3000 i5)

An advantage of optical steppers is their ability to use a reduction lens. Traditionally, i-line stepper reticles are sized 4X, 5X, or 10X larger than the actual image to be patterned (initially steppers used 10X reticles and then later 5X and 4X). To further explain the purpose of a reduction lens, a stepper with a 5X reticle requires a 5:1 reduction lens to transfer the correct image size to the wafer surface. This demagnification factor makes it easier to fabricate the reticle because the features on the reticle are five times larger than the final image on the wafer. At least one stepper manufacturer produces a stepper that provides a 1:1 projected image. The advantage of a nonreduction stepper is a low-cost stepper that can be used on noncritical patterning layers.

At each step in the exposure process, the stepper will focus the wafer and the reticle to the projection lens, align the wafer to the reticle, expose the resist with UV light that passes through the transparent regions of the reticle, and then step to the next location on the wafer to repeat the entire sequence. By following this process, the stepper will ultimately transfer the full die array onto the wafer in a sequence of exposure steps (see Figure 14.36). Because the stepper exposes only a small portion of the wafer at one time (e.g., typically a field size of one die on the wafer for a larger microprocessor die), compensations for variations in wafer flatness and geometry can be easily performed.

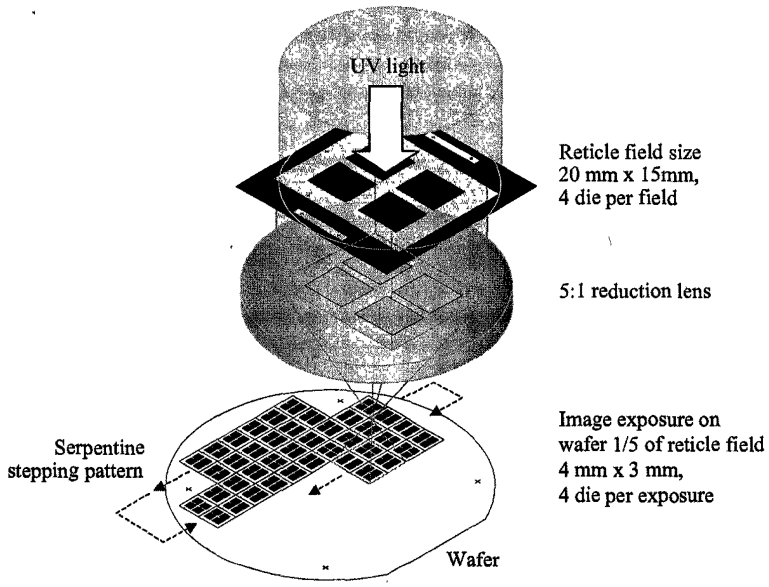


FIGURE 14.36 Stepper Exposure Field

Steppers have used conventional mercury arc lamp illumination sources (for g-line of 436 nm, h-line of 405 nm, and i-line of 365 nm) with a CD down to 0.35 μm. To obtain a 248 nm DUV wavelength source, the mercury arc lamp source is replaced with a KrF (krypton-fluoride) excimer laser. This equipment permits patterning a 0.25-μm CD. Typically, DUV stepper technology is used for patterning critical layers while conventional i-line exposure methods are used for noncritical layers. This mix-and-match approach to lithography is used to reduce production costs.

The growth in the physical size of semiconductor chips along with smaller critical dimensions creates a need for a larger exposure field size and improved lens optics for steppers. This in turn dictates more complex lithographic lens design and fabrication, with the cost of lens systems alone in steppers exceeding $1 million. This cost limits a conventional step-and-repeat exposure field to 22 × 22 mm. To overcome these problems, an evolutionary stepper known as step-and-scan has become predominant for DUV photolithography at technology nodes of 0.25 μm and below.

Step-and-Scan System

A recent development in lithographic exposure equipment employs a technique referred to as a *step-and-scan system.* The step-and-scan optical lithography system is a hybrid tool that combines the technology from scanning projection aligners and step-and-repeat steppers by using a reduction lens to scan the image of a large exposure field onto a portion of the wafer. A focused slit of light is scanned simultaneously across the reticle and wafer (see Figure 14.37). One standard exposure field size for this type of aligner is 25 × 33 mm for a six-inch-square reticle size. Once the scan and pattern transfer is completed, then the wafer is stepped to the next exposure field and the process is repeated.

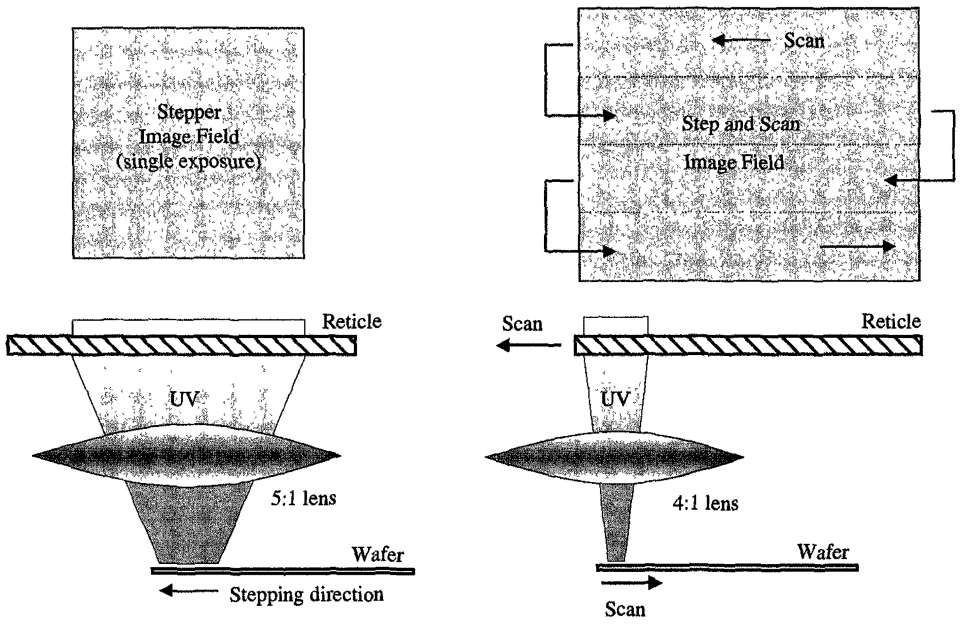


FIGURE 14.37 Wafer Exposure Field for Step-and-Scan (Used with permission from ASM Lithography)

A benefit from using a step-and-scan system to expose wafers is the increased exposure field for larger chip sizes. The lens field only has to be a narrow slit, as in the older full-wafer scanning projection aligners. It scans a reduction reticle (typically a 4X) through a small, well-corrected image field of 26 × 33 mm before stepping to the next location.[22] The optical system can now be designed for this much smaller field, permitting a smaller lens system (see Figure 14.38 on page 394). Another major advantage of a larger field size is the opportunity to put more die on a reticle, thus exposing more die in a single exposure.

Another significant step-and-scan system advantage is the ability to adjust focus throughout a scan (called on-the-fly focus), permitting compensation for lens defects and changes in wafer flatness. This improved control of focus during a scan yields improved CD uniformity control across the exposure field.

The major challenge with step-and-scan systems is the increased demand on mechanical tolerance control due to the motion of the stage controls for the reticle and wafer. Whereas steppers only had to move the wafer rapidly to a new position, a step-and-scan system has to precisely move both the wafer and reticle simultaneously and in opposite directions. These scanning and stepping motions are performed while holding position tolerances to within a few tens of nanometers during the scan.

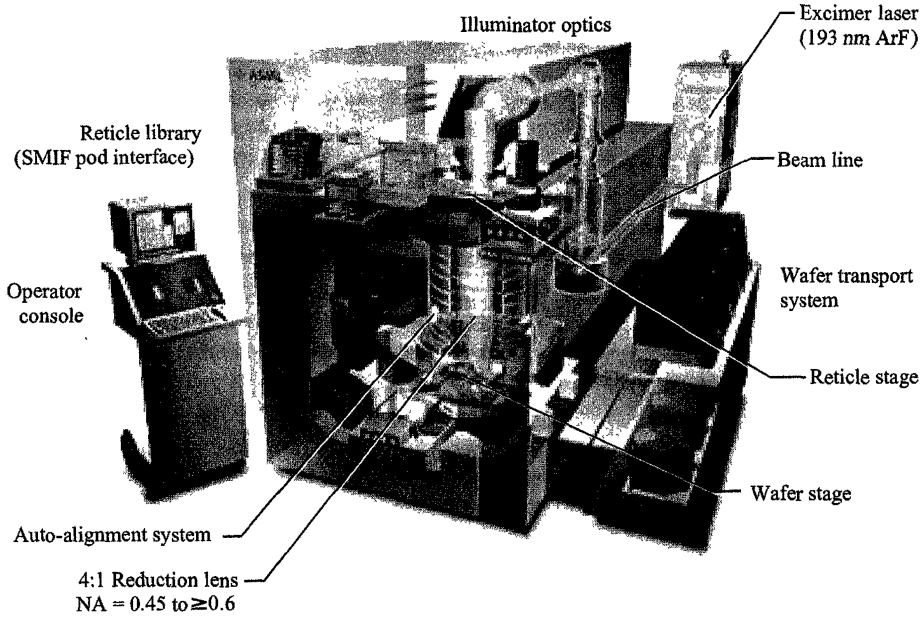


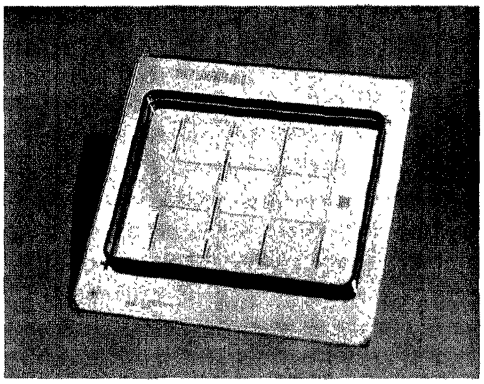
FIGURE 14.38 Step-and-Scan Exposure System
(Used with permission from ASM Lithography, PAS 5500)

Reticles

A *reticle* is a transparent plate that has a pattern image that will be transferred to the photoresist coating on the wafer. Two terms are commonly used in wafer fabrication: reticle and mask. A reticle contains the pattern image for only part of the wafer (e.g., 4 die) that must be stepped and repeated across the entire substrate. Reticles are used for step-and-repeat steppers and step-and-scan systems found in wafer fabrication. A *photomask,* or *mask,* contains the pattern image for a complete wafer die array and the pattern is transferred in a single exposure (1:1 image transfer).[23] Masks are used for older proximity printers and scanning alignment projectors. Table 14.6 compares reticles versus masks to provide insight into why the photolithography industry changed from mask to reticle.

TABLE 14.6 Comparison of Reticle versus Mask

Parameter Number of Exposures	Reticle Multiple Exposures	Mask Single Exposure
Critical Dimension	Easier to pattern submicron dimensions on wafer due to larger pattern size on reticle (e.g., 4:1, 5:1).	Difficult to pattern submicron dimensions on mask and wafer without reduction optics.
Exposure Field	Small exposure field that requires step-and-repeat process.	Exposure field is entire wafer.
Mask Technology	Optical reduction permits larger reticle dimensions—easier to print.	Mask has same critical dimensions as wafer—more difficult to print.
Throughput	Requires sophisticated automation to step-and-repeat across wafer.	Potentially higher (not always true if equipment is not automated).
Die alignment and focus	Adjusts for individual die alignment and focus.	Global wafer alignment, but no individual die alignment and focus.
Defect density	Improved yield but no reticle defect permitted. Reticle defects are repeated for each field exposure.	Defects are not repeated multiple times on a wafer.
Surface flatness	Stepper compensates during initial global prealignment measurements or during die-by-die exposures.	No compensation, except for overall global focus and alignment.



Photolithography Reticle (Photo courtesy of Advanced Micro Devices)

A reticle must be perfectly manufactured. All wafer circuit features ultimately come from patterns on the reticle; therefore, the quality of the reticle plays a key role in achieving high-quality imaging during submicron photolithography. If reticle pattern defects such as distortion and incorrect image placement are not detected, they will be reproduced in the resist on the wafer. Reticles undergo extensive automated testing for defects and particles once they are fabricated.

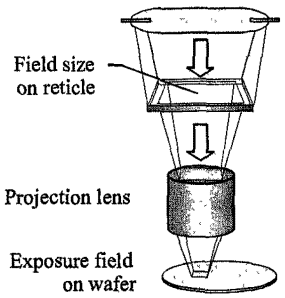
Reticle Materials ■ The primary reticle substrate material for submicron lithography is fused silica. It is always used for DUV lithography because it has high optical transmission in the DUV portion of the spectrum (248 and 193 nm). Fused silica is the most expensive material for reticles and has very low thermal expansion. A low thermal expansion means the reticle is dimensionally stable with changes in temperature. Because of this, there is only minor thermal run-out, which is an increase in a dimension due to a change in the thermal environment. Other desirable properties for reticle material are high optical transmission and no defects on the surface or within the material.

The most common opaque material deposited on the reticle substrate is a thin layer of chromium (referred to as chrome). This chrome layer will undergo patterning to create the necessary design shapes to define the circuitry for the wafer layer (e.g., holes, lines, pads, and so on). The chrome thickness is usually less than 1,000 Å and is sputter deposited. There sometimes is an antireflective layer of chromium oxide (about 200 Å thick) placed on the chrome.

Reticle Reduction and Size ■ Reticles are used in stepper and step-and-scan system applications that require a reduction lens to reduce overlay accuracy during patterning. A stepper commonly uses a reticle reduction ratio of 5:1 or 4:1, whereas a step-and-scan system uses a reticle reduction ratio of 4:1. Each reticle layer usually contains the necessary pattern for one or more die. The small field exposure size on steppers and step-and-scan systems permits close tolerance control during reticle alignment.

Most reticles are currently 6 × 6 inches (152 mm) square, although 5 × 5 inches is still common. Reticles are usually 0.090" to 0.250" thick. A six-inch reticle with a 4X reduction defines a usable field size at the wafer surface, which on current photolithography step-and-scan equipment is about 25 × 25 mm (see Figure 14.39 on page 396). Multiple exposures are required as the reticle is stepped over the wafer. The required exposure field size is forecasted to increase to accommodate the increasing size of DRAM and microprocessor chips. The industry is investigating a changeover to a nine-inch reticle to replace the current six-inch reticles. This will increase the number of die exposed per field, which permits fewer steps in the stepper or step-and-scan to complete the exposure of a complete wafer.[24] However, there is substantial cost to implementing this change, which may negate the benefit.

Reticle Fabrication ■ A common method for creating a pattern on a reticle is by the use of an electron beam (e-beam). This technique uses direct writing of the pattern from electronically stored original patterns. There is an immense amount of data involved in this process, and the total time to write a pattern on a reticle can be several hours. The basic steps for patterning a reticle are similar to those for a wafer.



Lens Type	10:0	5:1	4:1	1:1
Reticle Field Size (mm)	100 x 100	100 x 100	100 x 100	30 x 30
Exposure Field on Wafer (mm)	10 x 10	20 x 20	25 x 25	30 x 30
Die per Field of Exposure (assume 5mm x 5mm die size)	4	16	25	36

FIGURE 14.39 Comparison of Reticle Reduction Versus Exposure Field

E-Beam Lithography. The direct-write method of *electron beam* (*e-beam*) lithography is capable of transferring a high-resolution pattern directly to the reticle surface. In e-beam lithography, an electron source produces many electrons that are accelerated and focused in the shape of a beam toward the reticle (see Figure 14.40). The electron beam is focused either magnetically or electrostatically and is scanned in the desired pattern across a special e-beam resist on the reticle surface. The beam can be scanned across the entire reticle (raster scan) or scanned only over the printed areas (vector scan) to eventually transfer the pattern to the reticle.

To apply the e-beam resist on the reticle, the reticle is cleaned and the chrome film is spin coated with a suitable photoresist, then soft baked. The standard e-beam resist is a positive-tone poly(butene 1 sulfone), or PBS. However, this resist is not suitable for submicron linewidths. Alternative resists are being developed, such as chemically amplified resists.[25] Advanced e-beam mask writers are capable of patterning 0.36-μm minimum feature sizes on a reticle.[26]

After exposing and developing the resist, the final patterned surface is etched into the chrome film with a wet- or dry-etch process (advanced reticle fabrication uses dry etch). Recall that the mask features are four or five times larger than the wafer images (due to lens reduction in steppers and step-and-scan tools). However, the dimensional tolerances are very tight on mask features in order to produce acceptable critical dimensions on wafers.

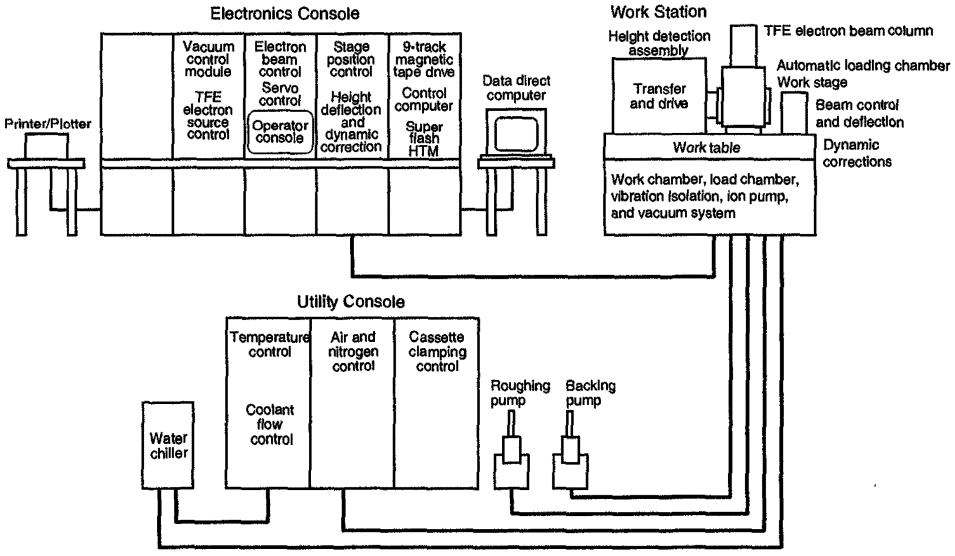


FIGURE 14.40 Principles of Electron Beam Lithography
(Used with permission from Etec Systems, Inc., MEBES 4500 System)

E-beam replaced optical resist patterning on reticles because it has a shorter wavelength and higher exposure speed compared to UV sources. These qualities produce better dimensional control with increased production throughput.[27] E-beam is a reliable method with high resolution and flexibility, but speed and system complexity are disadvantages for its use to pattern wafers.[28] It does have applications in very specialized wafers, such as application-specific integrated circuits (ASICs) that benefit from no reticle to achieve a quick turnaround time from development to production.

Sources of Reticle Damage ■ Reticles on advanced steppers and step-and-scan systems are moved into and out of the tool with automated storage and handling. A reticle must be meticulously clean for it to create perfect images during its many exposures to pattern a wafer layer. Recall that a stepper will step-and-repeat one image over the entire wafer. If there is even one foreign particle on a reticle circuit image, then it is repeated at every site on the wafer.

There are actually many possible sources of damage during use of a reticle, such as dropping the reticle, scratches on the surface, electrostatic discharge (ESD), and particles of dirt. ESD causes a problem if the reticle is handled by an improperly grounded technician. This condition could potentially discharge a small surge of current through the micron-sized chromium lines on the reticle surface, melting a circuit line and destroying the pattern.

If an airborne particle of dirt lands on a critical region of the reticle, this could damage the circuit and create an imaging defect. A solution to particulate contamination on reticles is to protect the surface with a thin, optically transparent membrane known as a *pellicle*. The pellicle is tightly stretched on a sealed frame about 5 to 10 mm above the mask surface. No dirt particles are able to reach the mask surface. If a dust particle lands on the pellicle, it is far removed from the focal plane and is invisible to the projection optics (see Figure 14.41).

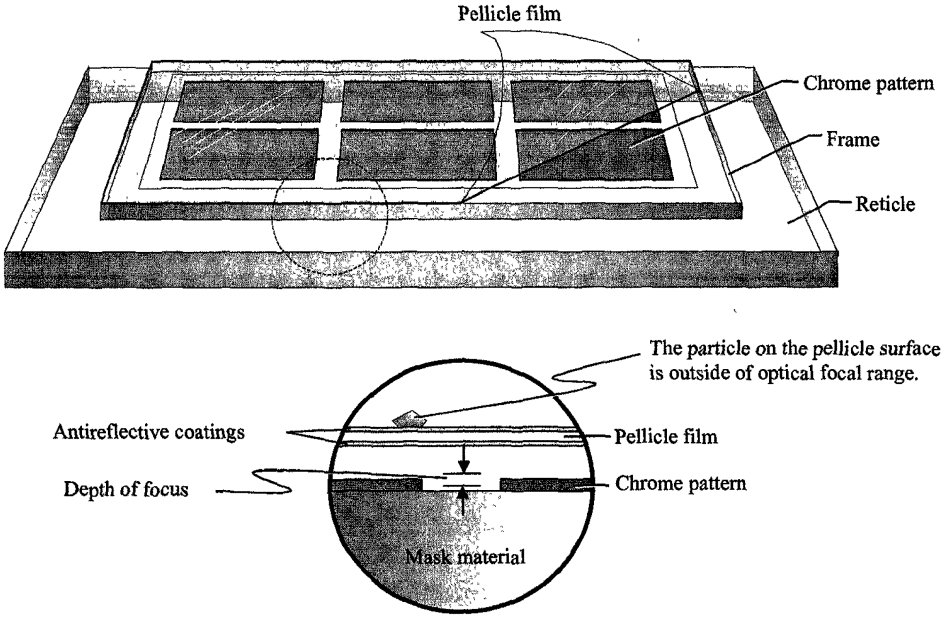


FIGURE 14.41 Pellicle on a Reticle

The pellicle material is transparent to the exposing light energy. There are different materials and thickness used for pellicles, such as nitrocellulose acetate that is typically 0.7 μm thick, or a 12 μm thick Mylar fluorocarbon material. The pellicle is fragile; therefore, any action that would scratch the mask surface will rupture the pellicle membrane (which alerts the user to a potential source of reticle damage). When used for deep UV exposure wavelengths, the optical transparency of the pellicle must be carefully evaluated.

Optical Enhancement Techniques

As wafer critical dimensions decrease to feature sizes of 0.15 μm and below, factors such as diffraction and light scattering prevent reticles from effectively transferring a replica of the pattern to the wafer. Optical enhancement techniques are being used on the reticle to improve the quality and definition of the image. This has become an important area of optical lithography known as *subwavelength lithography,* which permits a wafer to be patterned with a resolution slightly below the light exposure wavelength.

Phase-Shift Mask (PSM) ■ *Phase-shift mask (PSM)* is a method developed in 1982 to overcome problems associated with light diffraction through small openings patterned on the reticle. With PSM, the reticle is modified with an additional transparent layer so that alternating clear regions cause the light to be phase-shifted 180° (see Figure 14.42). As we have learned about interference between out-of-phase waves, there is now destructive interference. The light diffracted into the nominally dark area on the left will encounter destructive interference with the light diffracted from the right clear area. The light diffraction underneath the opaque area is reduced. Phase-shifting techniques on reticles improve image contrast, and has become a critical factor for microlithography at CDs of 0.18 μm and below. There are many approaches to PSM that use the same basic concept, but they are all based on the principle of destructive interference.

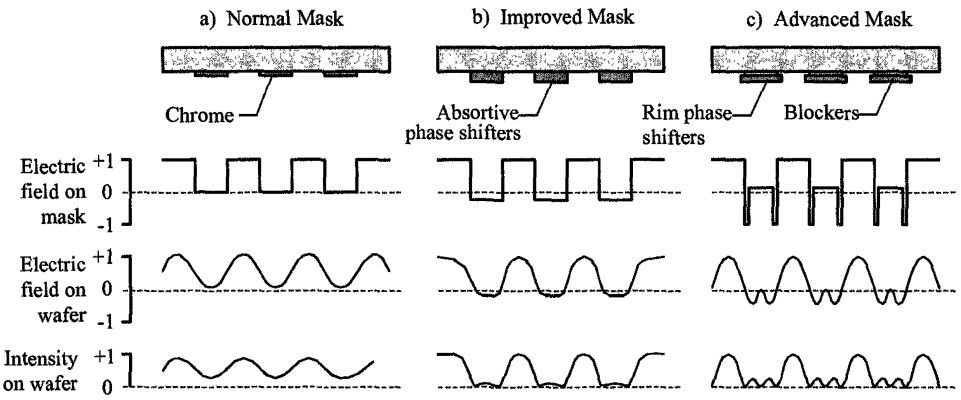


FIGURE 14.42 Phase-Shifting Mask
(Reprinted from the January 1992 edition of *Solid State Technology,* copyright 1992 by PennWell Publishing Company)

Optical Proximity Correction (OPC) ■ Uniformity of feature size dimensions is critical in high-performance ICs, especially in the transistor gate region where varying linewidths will affect the speed of the device. Because of optical proximity effects due to light diffraction and interference between closely spaced features on the reticle, the widths of lines in the lithographic image are affected by other nearby features (see Figure 14.43). Tightly grouped lines will print with a different size than isolated lines, although both have the same linewidth dimension on the reticle. This particular example is referred to as iso-dense bias.

It is possible to introduce selective image size biases (alterations) into the reticle pattern to compensate for optical proximity effects. This is called *optical proximity correction (OPC).* Computer algorithms are available to the reticle designer for generating optical proximity corrections on the reticle for smaller feature sizes. However, producing reticles with this level of control is a challenge in manufacturing, especially since CD feature sizes are already extremely small. As the critical dimension is reduced to less than 0.18 μm, aggressive scaling of dimensions will require increased use of OPC, which will make reticle fabrication more complicated.[29]

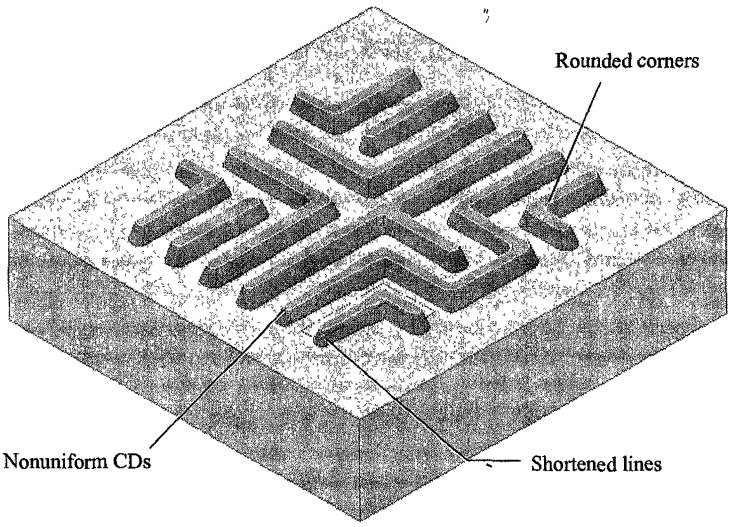


FIGURE 14.43 Optical Proximity Effects

Off-Axis Illumination ■ The conventional form of illumination for lithographic lenses has the exposing light centered on the centerline of the projection optics (see Figure 14.44). However, light diffraction creates a problem as the reticle openings are made smaller and smaller for submicron features sizes, to the point that the imaging lens will not transfer the pattern. A solution is to have the incident light strike the mask at an angle in order to align the diffraction fringes with the lens, which produces a symmetrical intensity profile that corresponds to the reticle pattern. This is referred to as *off-axis illumination* or (*OAI*). This technique reduces the resolution limit and increases the depth of focus for imaging.

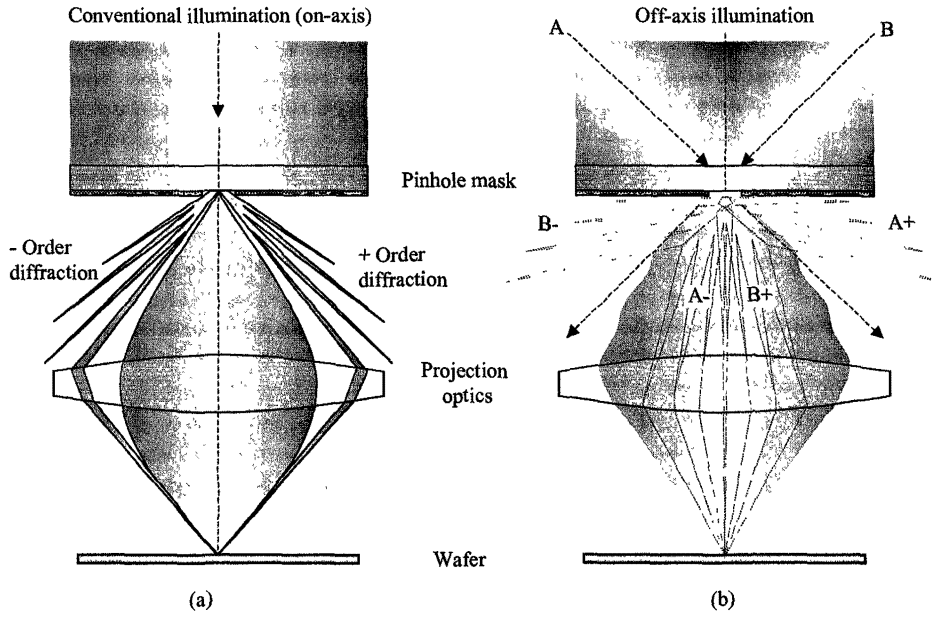


FIGURE 14.44 Off-Axis Illumination

Bias ■ *Print bias* is the difference between a feature dimension on a reticle and the same printed dimension on the wafer. The amount of print bias may be different for varying sized features. An example of print bias is a square contact with dimensions near the optical system resolution that prints with rounded corners. One way to address this problem is by adding serifs to the features on the reticle pattern, which help square features such as contact corners during printing on the wafer (see Figure 14.45 on page 400).[30]

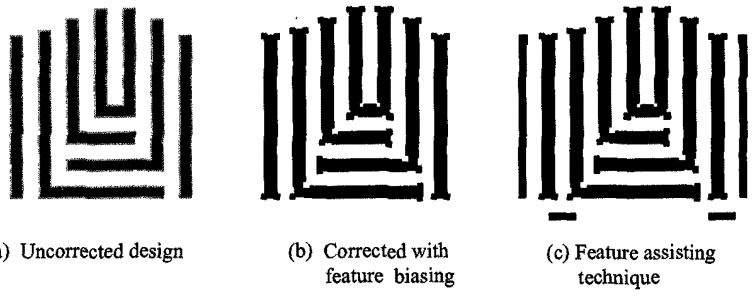


FIGURE 14.45 Serifs to Minimize Rounding of Contact Corners
(Redrawn from "Optical/Laser Microlithography," *SPIE Proceeding VIII* 2440 (February 1995)

Alignment

The alignment process begins with the proper alignment of the reticle to a fixed reference mark on the body of the stepper or step-and-scan system. Once the reticle is aligned to the body of the exposure tool, then the wafer stage positioning is measured with respect to the reticle. This positioning provides any baseline correction data that the alignment software will use to compensate for variations in reticle characteristics. This process is referred to as *baseline compensation* (*BLC*).

To successfully pattern the wafer, the wafer pattern must be correctly aligned to the existing patterns on the reticle pattern. The IC will function properly only if each successive projected image is correctly matched to the wafer patterns. To this end, *alignment* is the process of determining the position, orientation, and distortion of the patterns already on the wafer and then placing them in correct relation to the projected image from the reticle. Alignment should be fast, repeatable, accurate, and precise. The outcome of the alignment process, or how accurately each successive pattern is matched to the previous layer, is known as *registration*.[31]

Overlay accuracy (also known as registration) is the measure of the alignment system's ability to overlay the reticle pattern onto the wafer pattern. Overlay budget describes the maximum relative displacement between a patterned layer and the previously defined layer (see Figure 14.46). In general, the overlay budget is about one-third of the critical dimension. For 0.15 μm design rules, the overlay budget is expected to be 50 nm.[32]

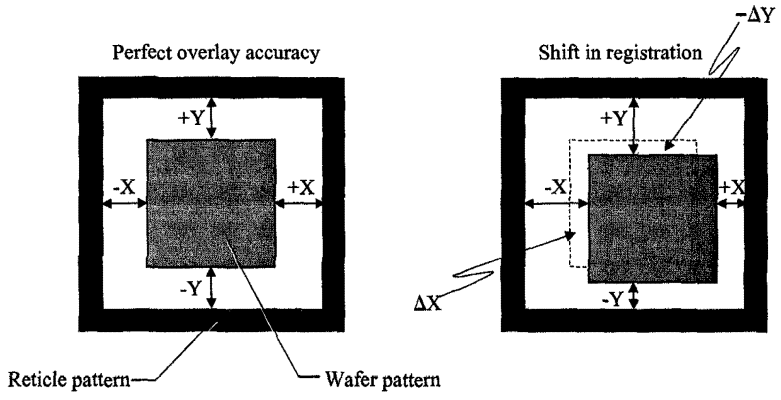


FIGURE 14.46 Overlay Budget

For steppers and step-and scan systems, each reticle pattern is aligned and exposed at multiple locations as the aligner steps across the wafer. Each field corresponds to the reticle pattern of a single large chip or several smaller chips. A *grid* is the particular path that the photo tool follows to step across the wafer and expose the individual fields (see Figure 14.47).

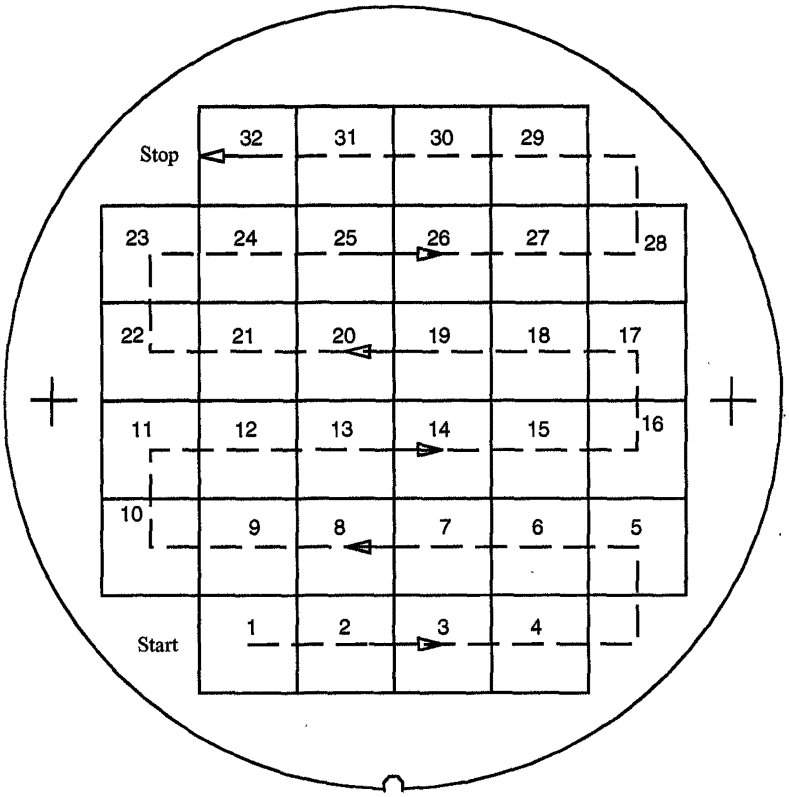


FIGURE 14.47 Grid of Exposure Fields on Wafer

Steppers and step-and-scan systems have a sophisticated automatic alignment system that detects the position and orientation of both the wafer and the reticle and then aligns the wafer to the reticle before exposure (see Figure 14.48 on page 402). The tool's alignment system includes alignment marks on both the reticle and wafer, an alignment detection system, and the electromechanical positioning devices such as motors and drive mechanisms. The goal of alignment detection is to determine as rapidly as possible the position of the different alignment marks in the exposure tool coordinate system. Alignment software algorithms within the tool's process controller calculate offset values and the direction of wafer stage movements necessary to bring the wafer within the overlay budget specified for the tool.

Alignment Marks ■ *Alignment marks* are visible patterns placed on the reticle and the wafer to determine their position and orientation. Marks, also referred to as targets or fiducial marks, may be one or more lines on the reticle, which then become trenches when printed on the wafer. Marks may also be a shape on the reticle which overlays on wafer marks (see Figure 14.49 on page 402). Reticle alignment (RA) marks appear on both the left and right sides of the reticle. The RA marks are aligned to fiducial marks mounted on the stepper's body. Global alignment (GA) marks are printed on the left and right sides of the wafer during first mask exposure. GA marks are used for making coarse alignments of each wafer during subsequent layers. Fine alignment (FA) marks are printed during each field exposure. FA marks are used for making final alignment adjustments between each wafer exposure site and the reticle. The shape and location of marks varies depending on the equipment manufacturer. Once an alignment mark is aligned, it is assumed that the remainder of the reticle patterns is also correctly aligned.

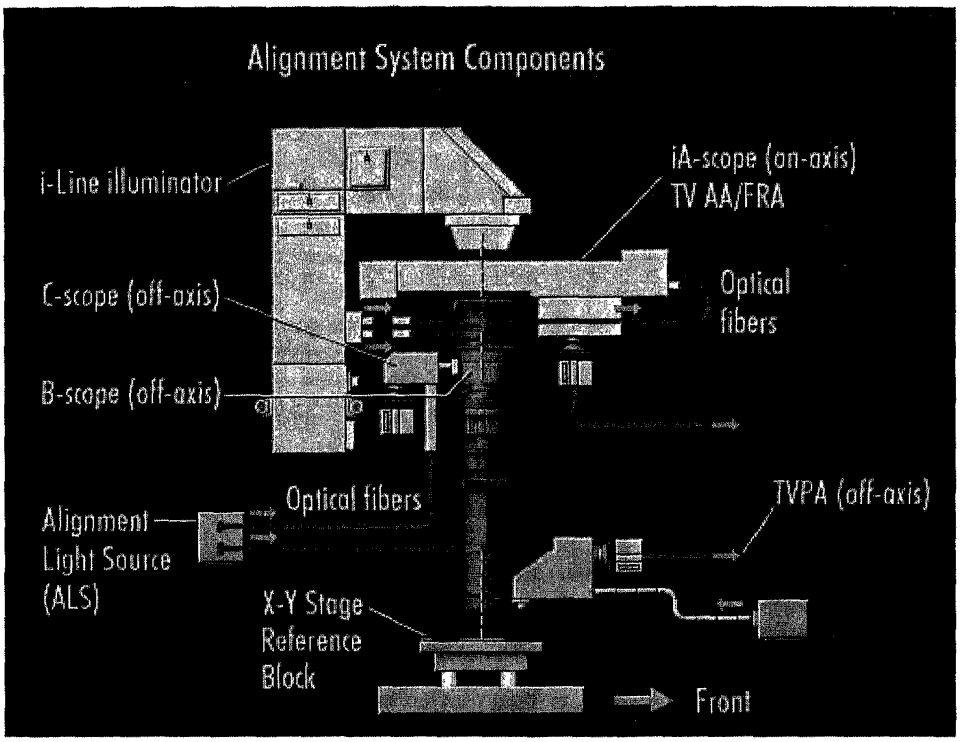


FIGURE 14.48 Step-and-Repeat Alignment System
(Used with permission from Canon USA, FPA-2000 il)

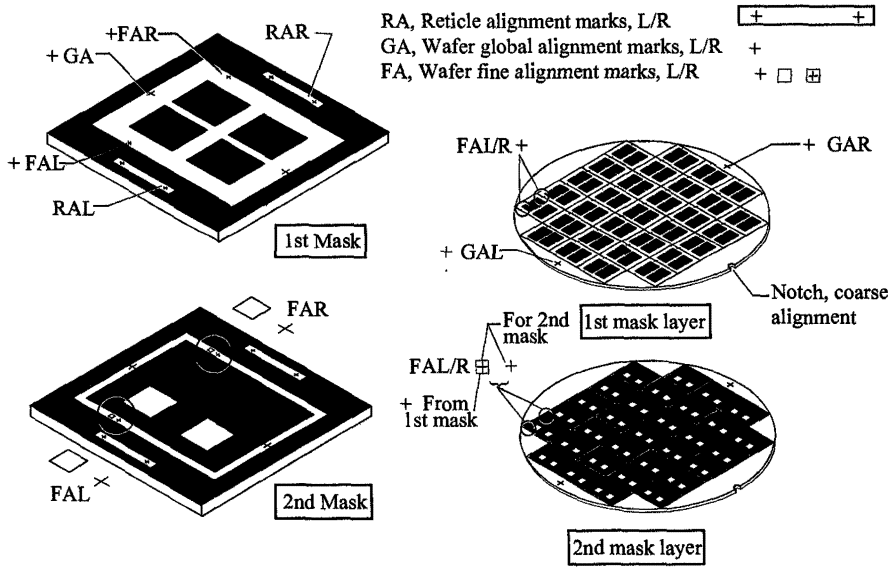


FIGURE 14.49 Alignment Marks

The computer-controlled automatic alignment system identifies the alignment marks. An alignment illumination system projects light through the reticle marks and onto the wafer surface. A common light source is the stepper UV light, with filtering to block unwanted wavelengths that could activate the resist. Another source is a laser such as a helium-neon laser. This laser emits light at 633 nm, which will not activate the resist.

Light illuminates the alignment marks and then photo detectors are used to optically detect the reticle and wafer targets. The alignment illumination system can use the main stepper's projection optics to illuminate the marks (known as on-axis or through-the-lens), or use its own alignment

optics (known as off-axis) (see Figure 14.50). There are many different types of alignment methods in use. Laser beams are also used to precisely control the levelness and position of the X-Y stage that holds the wafer chuck. Laser interferometry is used to measure the position of the wafer stage at all times. Once the position data are measured, the data are fed into the system computer with a software interface to the electromechanical system used to make the correct adjustments to align the wafer to the reticle.

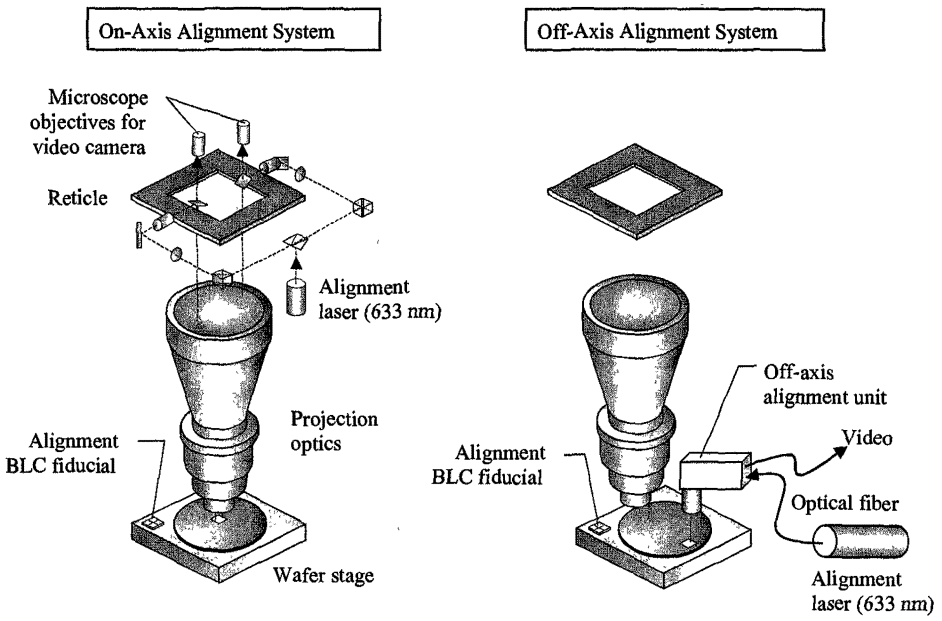


FIGURE 14.50 On-Axis Versus Off-Axis Alignment System
(Used with permission from Canon USA, redrawn after FPA-2000 il schematics)

Step-and-Scan Alignment Marks. An improvement for a step-and-scan system is that multiple alignment marks can be placed in each exposure field, permitting alignment to occur with each field exposure. This means that position parameters such as wafer rotation and X-Y alignment can be adjusted at each scan site, which improves overlay accuracy and reduces the overlay budget.

Alignment Mark Deterioration. The increasing number of film layers on high-performance ICs require greater flatness from one layer to the next. This flatness is achieved by using chemical mechanical planarization (CMP) to planarize the wafer (see Chapter 18). However, CMP also deteriorates alignment marks on the wafer, which makes them more difficult to detect.[33] Stepper and step-and-scan equipment manufacturers have developed alternative approaches to align the wafer. In one case, a laser beam is used to detect a phase change in the beam reflection off the alignment mark relative to a reference signal. Slight phase changes are relatively easy to detect, even with layers that are too flat to measure with the standard light reflection system.

Types of Alignment ■ Each reticle must be aligned to the exposure tool's body when the reticle is mounted on the reticle stage. The reticle alignment marks are illuminated by a laser beam (an example is HeNe) through a fixed referenced mark. Once aligned, the wafer stage is then aligned to the reticle.

The wafer is initially prealigned by holding it in a chuck at the wafer stage and locating the notch or flat. For a *first mask exposure,* the wafer flat or notch is the only alignment feature on the wafer. The blank wafer is "blindly" exposed to the first reticle layer without any further alignment. The only consideration is for ensuring that the lens is properly focused to the wafer prior to each exposure.

For subsequent exposures the wafer and reticle position data are measured with respect to a coordinate system defined for the exposure tool and are then used in a global or field-by-field manner to perform alignment. *Global alignment* (or coarse alignment) uses several marks to align all the exposure fields on the wafer. The goal is to quickly align the entire wafer relative to the reticle.

Field-by-field alignment data (also called fine alignment) is used to align a single field. The stepper steps to each die on the grid, focuses, aligns, and then exposes. This method is the slowest but achieves excellent registration, if necessary, for a critical layer. The specific details of stepper alignment systems are unique to each manufacturer due to the extreme tolerance control required to align the photomask and wafer pattern to within a few nanometers.

Environmental Conditions

The environmental conditions for photolithography steppers and step-and-scan systems are critical for high-yield wafer fabrication. Minor variations in environmental conditions can lead to device defects. Photolithography tools have an enclosed environmental chamber to control conditions such as temperature, humidity, vibration, atmospheric pressure, and particle contamination.

Temperature ■ It is critical to control temperature during photolithography. Temperature can adversely affect all aspects of aligners: mask stage, optical elements, light sources, wafer stage, and alignment systems. Temperatures are typically controlled to within a tenth of a degree Celsius. For this reason, the high-temperature illuminator and heat generating power supplies are generally located away from the main body of the alignment and exposure tool.

Humidity ■ Humidity is carefully controlled inside the fab and within the photolithography environmental chamber. Excessive humidity can affect the resist adhesion to the wafer. Humidity also affects the density of the air, which can adversely affect light passing through it; thus producing adverse effects on interferometer positioning, lens NA, and focusing.

Vibration ■ The occurrence of vibration would create problems for positioning, alignment, focusing, and exposure. Problems could be misregistration, misalignment, defocus, and nonuniform exposure. There are different methods to minimize vibration. In some cases, floors that support the lithography equipment are isolated by large shock absorbers from the other areas of the fab. The photo tools also have their own design features to isolate vibration, such as pneumatic isolation devices and momentum absorption structures.

Atmospheric Pressure ■ Atmospheric pressure changes can affect the refractive index of air in the projection optics and laser interferometers used for stage positioning of steppers. This condition leads to nonuniform CDs and poor registration. For this reason, equipment manufacturers usually include pressure sensors to monitor the atmospheric pressure inside the environmental chamber. The pressure measurement data is fed into a computer for monitoring and control. In some cases, the lens elements are sealed in an airtight housing with a constant air flow and pressure inside the housing.

Particle Contamination ■ Photo tools are designed so that a class 1 or better clean environment is maintained inside the tool chamber. All materials and hardware used in the equipment construction are selected for their low particle generation. Lubricants are avoided. If they are required, then a low vapor pressure lubricant is specified to minimize outgassing. Wafer and reticle handling is done by mechanisms that hold the product from underneath, with automated handling systems used on modern equipment. Air solenoids are vented externally from the tool to avoid scattering particles inside the tool.

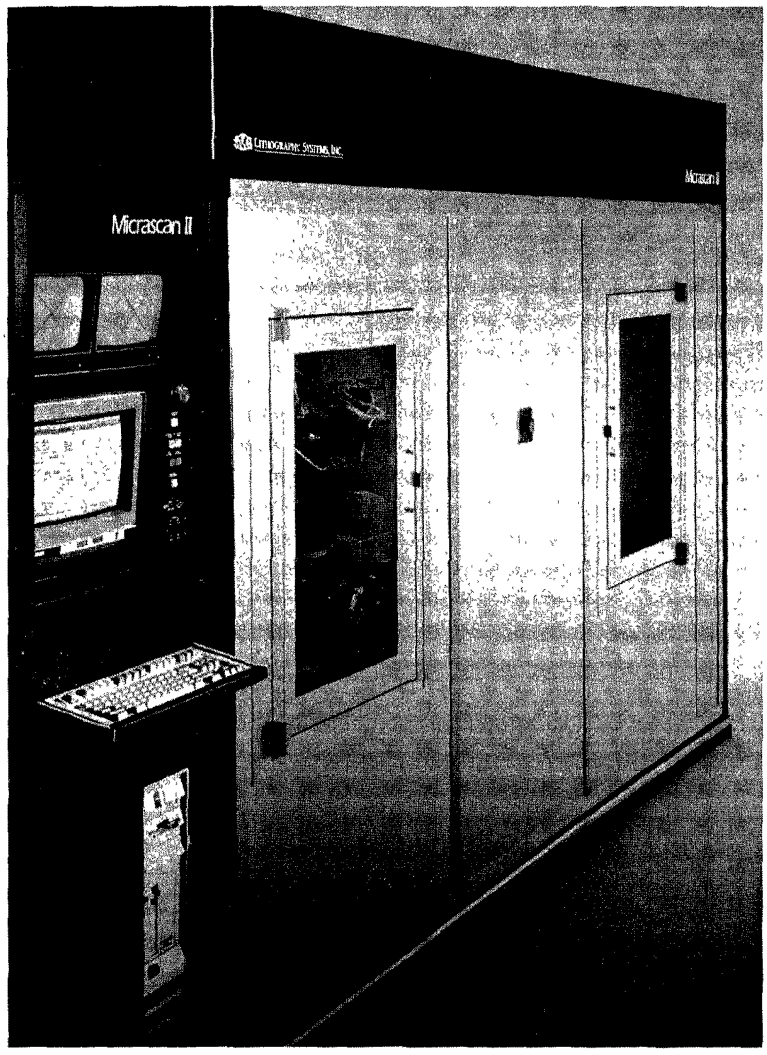
Comparison of Photo Tools

Steppers and step-and-scan systems based on optical lithography are the photolithography workhorses in semiconductor manufacturing for VLSI/ULSI deep submicron feature sizes. A comparison of the various features of steppers and step-and-scan systems is listed in Table 14.7.

TABLE 14.7* Comparison of Photolithography Tools

Model	Wavelength (nm)	Stepper/ Step-and scan	Illumination	Exposure Field Size (mm)	N/A	Resolution (μm)	Overlay Accuracy (nm)
ASML							
PAS5500/22	365	Stepper	Mercury arc	22 × 27.4	0.4	0.70	≤70
PAS5500/60B	365	Stepper	Mercury arc	18 × 24.2	0.54	0.45	≤70
PAS5500/200B	365	Stepper	Mercury arc	22 × 27.4	0.48 to 0.60	0.32	≤50
PAS5500/300B	248	Stepper	KrF laser	22 × 27.4	0.40 to 0.57	0.25	≤45
PAS5500/500	248	Step-and-scan	KrF laser	26 × 34	0.40 to 0.63	0.22	≤45
PAS5500/900	193	Step-and-scan	ArF laser	26 × 33	0.45 to >0.6	0.13 to 0.15	
Canon							
FPA-3000i5	365	Stepper	Mercury arc	22 × 22	0.45 to 0.63	0.35	≤80
FPA-3000EX3	248	Stepper	KrF laser	22 × 22	0.40 to 0.60	0.25	≤80
FPA-4000ES1	248	Step-and-scan	KrF laser	25 × 33	0.40 to 0.63	0.25	≤70
FPA-5000ES2		Step-and-scan		26 × 33	0.68	0.18	
ISI Lithography							
XLS 7500	365	Stepper	Mercury arc	20 × 20	0.55	0.5	≤90
XLS 7800	248	Stepper	KrF laser	22 × 22	0.35 to 0.53	0.35	≤80
Isis 202I	365	Stepper	Mercury arc	22 × 22	0.35 to 0.60	≤0.35	≤60
Isis 302k	248	Stepper	KrF laser	22 × 22	0.35 to 0.55	≤0.25	≤50
ArF MicroStep	193	Stepper	ArF laser	1.5 × 1.5	0.40 to 0.60	≤0.18	
Nikon							
i12D	365	Stepper	Mercury arc	22 × 22	Var. to 0.63	≤0.35	≤55
EX12B	248	Stepper	KrF laser	22 × 22	Var. to 0.55	≤0.28	≤55
S201A	248	Step-and-scan	KrF laser	25 × 33	Var. to 0.60	≤0.25	≤50
SVGL							
MS II+	248	Step-and-scan	KrF laser	22 × 33.5	0.50	0.3	≤70
MS III	248	Step-and-scan	KrF laser	26 × 33.5	0.40 to 0.60	0.25	≤55
MS III+	193	Step-and-scan	ArF laser	26 × 34	0.68	0.18	
Ultratech							
2244I	355 to 375	Stepper		22 × 44	0.32	0.75	≤350
Saturn	355 to 375	Stepper		22 × 44	0.365	0.65	≤250

*Adapted from R. DeJule, "Wafer Stepper Trends," *Semiconductor International* (February 1997), p. 88.



Step-and-Scan System
(Photo courtesy of Silicon Valley Group Lithography Systems)

MIX AND MATCH

Most attention for advancements in wafer fabrication technology is given to leading-edge areas like chemically amplified DUV resists capable of deep submicron CD linewidth control. However, recognize that there can be up to 20 to 30 layers in a high-performance IC. CDs and overlay accuracy are critical quality measures on layers with sub-quarter micron structures. For the subcritical layers, novolak-based DNQ resists with i-line steppers are acceptable and cost-justified.

The total cost of owning and operating equipment for wafer production is referred to as the *cost of ownership,* or *COO.* COO costs include the up-front capital expenditures plus the hidden costs from areas such as maintenance, training, downtime, and reduced process latitude. There is a high COO for operating a high-resolution DUV resist on a subcritical layer where i-line DNQ-novolak resist would suffice. Chip manufacturers have learned it is not cost-effective to use an advanced tool and resist system for patterning subcritical layers.

A *mix-and-match* approach to photolithography matches the photolithography resist and equipment technology to the criticality of the wafer layer. For instance, analysis of a 0.22 μm DRAM device demonstrated that a 0.28 μm i-line stepper with a 70 nm overlay accuracy could image 13 noncritical layers of the total 20 layers on the device. The remaining 7 layers were imaged with a leading-edge DUV step-and-scan system that could achieve the 0.22 μm resolution. In this study, it was estimated that the cost of the i-line product averaged about $5 per layer, vs. $7.50 for the DUV layers.[34] This is the benefit of the mix and match strategy for photolithography technology—to reduce cost of ownership.

ALIGNMENT AND EXPOSURE QUALITY MEASURES

Typical quality measures for alignment and exposure are provided in Table 14.8.

TABLE 14.8 Key Quality Measures for Exposure

Quality Parameter	Types of Defects	Remarks
1. Focus-exposure dose.	A. Incorrect focus-exposure for system. Conduct focus-exposure optimization test while measuring CD linewidth.	• Verify uniform and optimum exposure from illumination source. • Make CD measurements of line versus a series of exposure dose values for a nominal focal position (e.g., 30% from top surface). • With nominal focal position, find optimum dose for producing CD. • Modify focal position and conduct CD measurements. Wide range of acceptable dose exposure at optimum focal position. • Verify the bulk resist meets all quality parameters.
2. Light intensity of illumination source.	A. Non-uniform light intensity in the exposure field.	• Check light intensity for specified energy and uniformity at several locations on a wafer. Most aligners have built-in photodetector (measures in mW/cm^2). • Evaluate resist to ensure it is not outgassing and condensing on optical elements. This will degrade lens transmission and field uniformity (important for DUV resists).*
3. Reticle alignment in stepper or step-and-scan tool.	A. Reticle alignment targets will not align properly with wafer alignment targets.	• Verify appropriate process recipe is loaded for the specific mask layer. • Verify appropriate wafers and reticle are loaded for a specific job. • Check rotation of reticle on reticle stage or wafer on wafer stage due to vacuum leak at chuck or electromechanical problem with stage. • Problem with internal optics of aligner. Possible cause is temperature or pressure change that affects the NA of the lens.
4. Pattern resolution.	A. Poor resolution for CDs on wafer: linewidths and holes do not meet specification.	Resolution is often a focus problem: • Perform focus-exposure test. • Check environment (temperature, pressure). • Wafer is not flat on chuck, possibly due to backside contamination or chuck problem. • Look for possible incoming process-related problems or improper process parameters or reticle. • Look for optics problems (e.g., lens aberrations).

Quality Parameter	Types of Defects	Remarks
5. Reticle quality.	The following are reticle defects: A. Dirt or scratches on reticle. B. Pattern defects on reticles: • Break in line. • Bridge between features. • Missing geometry. • Opaque spot from isolated chrome. • Pinhole in chrome line. C. Glass fracture. D. Lifted chrome (poor adhesion). E. Reticle plate flatness.	• Scratches can remove chrome and cause defect in resist. • A break in line extends completely across the chrome feature. • Bridge will join two chrome features across a clear space on the reticle. • Missing geometry is a pattern not on reticle, such as a missing contact. • Opaque spot is an area of chrome that should not be on reticle. • Pinhole is a hole in a chrome pattern. • Reticles should not have fractures and be controlled for flatness and warpage.

*O. Nalamasu et al., "Single-Layer Resist Design for 193 nm Lithography," *Solid State Technology* (May 1999), p. 29.

ALIGNMENT AND EXPOSURE TROUBLESHOOTING

Troubleshooting problems encountered during alignment and exposure are shown in Table 14.9.

TABLE 14.9 Common Alignment and Exposure Troubleshooting Problems

Problem	Probable Cause	Corrective Action
1. Excessive overlay error.*	A. Incorrect alignment system measurement of reticle and wafer alignment marks	Possible measurement error sources are: • Verify correct process recipe and reticle is used for a specific mask layer. • Verify the calibration and stability of the alignment system to determine the position of the alignment marks. • Verify calibration of alignment mark-to-pattern relationship, including thermal and/or mechanical effects. • If error is within one tool, then optical distortion is probably not source of problem. If error is tool-to-tool, check difference in optical distortion of two different projection optics.
	B. Problem with reticle.	• Verify there is no problem with reticle mounting and/or reticle heating that could change alignment mark-to-pattern position. • Check there is no particulate contamination on alignment marks that makes the alignment system incorrectly determine the mark position.

Quality Parameter	Types of Defects	Remarks
	C. Error in wafer or reticle stage that holds and positions wafer and reticle.	• Wafer and/or reticle stage has errors in position and rotation during exposure that contributes to overlay errors. • Excessive vibration of wafer or reticle stage. Tools have built-in vibration and shock isolation. • Unacceptable wafer or reticle stage heating that distorts wafer or reticle. • Chucking errors that vacuum clamp wafers differently and cause wafer distortion.
	D. Problem with projection optics.	• Calibration error in the lens magnification adjustment causes pattern mismatches. • Focus errors and/or unacceptable field flatness that causes image distortion or shifts. • Unacceptable heating causes optics distortion.
2. Drift in KrF laser parameters.**	A. Laser properties that can change are: • Laser spectral bandwidth and energy distribution. • Wavelength stability. • Output energy and repetition rate. • Pulse-to-pulse energy stability.	All laser measurements and calibrations should be performed after specialized training by the supplier, including: • Use special wavemeter to measure wavelength. Drift in wavelength affects focus at the wafer plane. • Assess background optical noise levels and electronic offsets to determine impact on energy distribution. • Measure bandwidth of laser output using procedure specified by supplier.

*G. Gallatin, "Alignment and overlay," *Microlithography, Micromachining and Microfabrication* vol. 1, ed. J. Sheats and B. Smith (New York: Marcel Dekker, 1998), p. 318.

**P. Das and U. Sengupta, "Krypton Fluoride Excimer Laser for Advanced Microlithography," *Microlithography Science and Technology* ed. J. Sheats and B. Smith (New York: Marcel Dekker, 1998), p. 299.

SUMMARY

Modern photolithography is based on optical lithography. Alignment and exposure are critical in lithography to meet critical submicron resolution requirements. There have been five photolithography equipment eras. The step-and-repeat and step-and-scan tools are the preferred optical lithography tools used today for advanced IC fabrication. The continued success of optical lithography is based on improvements to all subsystems. Light is important to project the pattern on the resist. UV light at certain energy peaks creates the photochemical reaction in the resist. UV exposure sources are the mercury arc lamp for conventional lithography and the excimer laser for deep UV. Reflection and refraction are important parameters for manipulating the light through lens systems for image projection. Diffraction describes how the light bends as it passes through the narrow patterns on the reticle. The ability of a lens to capture light is the numerical aperture (NA). Special antireflective coatings are placed on the wafer surface to diffuse reflected light and avoid damage to the light-sensitive resist. Resolution is the smallest feature printable on the wafer and is limited by wavelength, NA, and process factors. Reducing pattern resolution also leads to reduced depth of focus, which requires a planar wafer surface. This is achieved by chemical mechanical planarization (CMP). Quartz reticles contain the pattern to be imaged, using a 4X or 5X reduction optics to simplify reticle fabrication with e-beam lithography. Optical enhancement techniques such as phase-shift mask and optical proximity correction permit subwavelength lithography. Alignment of the reticle to the wafer is critical for meeting overlay budget requirements. Environmental conditions must be tightly controlled for optimum lithography. A mix-and-match approach uses conventional lithography for noncritical layers and DUV lithography for critical layers.

KEY TERMS

optical lithography
light
optical filters
electromagnetic spectrum
mercury arc lamp
light intensity
excimer laser
spatial coherence
dose monitor
optics
law of reflection
refraction
relative index of refraction, n
absolute index of refraction
lens
focal point
focal length
lens compaction
aberrations
diffraction
numerical aperture (NA)
reflective notching
standing waves
antireflective coating (ARC)
bottom antireflective coating (BARC)
top antireflective coating (TARC)
resolution
depth of focus (DOF)
depth of field
center of focus (COF)
contact aligner
proximity aligner
scanning projection aligner (scanner)
step-and-repeat aligner (stepper)
step-and-scan system
reticle
photomask or mask
electron beam (e-beam)
pellicle
subwavelength lithography
phase-shift mask (PSM)
optical proximity correction (OPC)
off-axis illumination (OAI)
print bias
baseline compensation (BLC)
alignment
registration
overlay accuracy
overlay budget
grid
alignment marks
first mask exposure
global alignment
field-by-field alignment
cost of ownership (COO)
mix and match

REVIEW QUESTIONS

1. Describe optical lithography.
2. What are the three basic purposes of a stepper?
3. Explain why design ground rules are important for alignment.
4. What is the alignment challenge for photolithography?
5. Describe the relationship between light exposure wavelength and image resolution.
6. Define light. Why is it needed in optical lithography?
7. List and explain the two types of light wave interference. What is an optical filter?
8. What is the electromagnetic spectrum, and what is the UV range?
9. List and describe the two UV exposure sources used in optical lithography.
10. What is light intensity and exposure dose, and how are they related? Why is exposure dose important?
11. What happens to resist sidewalls if there is excessive resist light absorbance?
12. Describe how an excimer laser functions.
13. What excimer laser is used as a 248 nm light source? As a 193 nm light source?
14. What is spatial coherence? Why is this controlled in photolithography?
15. What is a typical dose exposure latitude for a DUV resist? How is this measured?
16. What is optics, and why is it important in lithography?
17. State the law of reflection and give an example.
18. What is refraction? Explain the relative index of refraction and the absolute index of refraction.
19. What is a lens? Explain the focal point and focal length.
20. What lens material is used at the DUV exposure wavelength? Why?

21. Explain how lens compaction occurs and what problem it creates.
22. Describe lens aberration.
23. What is diffraction? Why is it a concern in optical lithography?
24. What is numerical aperture (NA)? State its formula, including the approximate formula.
25. What happens to NA if the radius of the lens is increased?
26. List and explain the two primary problems of light reflection from the wafer surface.
27. What is an antireflective coating, and how does it reduce standing waves?
28. State the formula for resolution. What three lithography parameters affect resolution?
29. What happens to resolution if the light wavelength decreases? If NA goes up?
30. Calculate the resolution of a scanner if λ = 248 nm, NA = 0.65, and k = 0.6.
31. Define depth of focus and center of focus. Write the equation to calculate DOF.
32. What happens to depth of focus as resolution inreases?
33. List the two important parameters for image quality in optical lithography.
34. Why is surface planarity important for pattern resolution?
35. Explain the contact alligner. Does it use a mask or reticle?
36. Explain how a proximity aligner works. What problem did it attempt to resolve?
37. Explain how a scanning projection aligner works. What problems did the scanning projection aligner try to resolve?
38. Explain the basic functions of a step-and-repeat stepper.
39. What benefits are gained from step-and-scan technology for lithography?
40. Define a reticle. What is the difference between a reticle and a photomask? What reticle reduction is usually used in a stepper? What reduction is used in a step-and-scan system?
41. What material is used to make a reticle? What opaque material is patterned on a reticle?
42. What is a typical usable field size for a 4:1 reticle?
43. What lithography technology is used to pattern reticles? Why?
44. Explain why a pellicle is used on reticles.
45. Explain phase-shift mask (PSM).
46. Discuss optical proximity correction (OPC).
47. How does off-axis illumination increase the pattern resolution?
48. What is print bias and what is one method to correct it?
49. Explain baseline compensation for alignment.
50. What is alignment? Whjat is registration?
51. Define overlay accuracy. What is the overlay budget? About how much of the critical dimension is the overlay budget?
52. What is a grid?
53. What are alignment marks? Describe RA, GA, and FA alignment marks.
54. How does a step-and-scan system improve alignment?
55. Explain global alignment and field-by-field alignment.
56. List and discuss five environment conditions that must be controlled in steppers and step-and-scan systems.
57. Explain the mix-and-match approach to photolithography. Why is it beneficial?

PHOTORESIST MATERIALS AND EQUIPMENT SUPPLIERS' WEB SITES

ASML	http://www.asml.com/
Canon Semiconductor	http://www.usa.canon.com/indtech/semicondeq/
Charles Evans and Associates	http://www.cea.com
Cymer Inc.	http://www.cymer.com/
Dupont Semiconductor Products	http://www.dupont.com/semiconductor/lith.html
ETEC Systems Inc.	http://www.etec.com/semiprod_frame.html
KLA-Tencor	http://www.kla-tencor.com/product/photo_frame.html
Karl Suss	http://www.suss.com/
Nikon	http://www.nikon.com/
SEMI	http://www.semi.org/
Silicon Valley Group	http://www.svg.com/
SPIE, International Society of Optical Engineering	http://www.spie.org/
Ultratech Stepper	http://www.ultratechstepper.com/
USHIO	http://www.ushio.com/index2.html

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CHAPTER 15

PHOTOLITHOGRAPHY: PHOTORESIST DEVELOPMENT AND ADVANCED LITHOGRAPHY

At this stage of the photolithography process, wafers have been coated with resist and exposed to UV light to produce a photochemical reaction in specified areas of the resist. The resist contains a precise coded image of the reticle pattern and is ready for the development step of photolithography. Photoresist development is where the three-dimensional pattern is physically produced in the resist. This step determines whether the resist image is an accurate replication of the reticle pattern. In deep submicron wafer fabrication, success at this step is critical for subsequent processing.

The advanced lithography section summarizes the next generation lithography tools. Fundamental research into alternative lithography tools is necessary so that the semiconductor industry will be ready to replace optical lithography when it has reached its resolution limit. Optical lithography appears to be the optimum patterning process for at least the next several technology nodes below 0.18 micron.

OBJECTIVES

After studying the material in this chapter, you will be able to:

1. Explain why and how a post-exposure bake is done for conventional and chemically amplified DUV resist.
2. Describe the negative and positive resist development process for conventional and chemically amplified DUV resist.
3. List and discuss the two most common resist development methods and the critical development parameters.
4. State why a hard bake is done after resist development.
5. Explain the benefits of a post-develop inspection.
6. List and describe the four different alternatives for advanced lithography, including the challenges for introducing each alternative into production.
7. Describe and give the benefit for the advanced resist process of top surface imaging.

INTRODUCTION

Following the sequential steps of the eight-step photolithography process, wafers have completed alignment and exposure. The reticle pattern has been aligned to each die on individual wafers and exposed to UV light for image transfer to the resist. Wafers with exposed resist leave the stepper or step-and-scan system and return to the automated track system. The next processing step is often a post-exposure bake and then wafers are ready for development. Photoresist development is the chemical dissolution of the soluble resist in the developer chemical. Development removes those areas of the resist rendered soluble by the exposure step. The insoluble resist remaining on the wafer should be an exact copy of the pattern on the reticle (for a positive-tone resist). Photochemistry renders the exposed regions soluble for positive-tone resists and insoluble for negative resists.

The goal of resist development is to accurately replicate the reticle pattern in the resist while maintaining acceptable resist adhesion. The ability to develop resist with deep submicron geometries is essential for advanced ICs. Resist development and inspection is the intermediate pattern transfer step before the wafer moves into another workbay to undergo etch or ion implantation. An improperly developed resist will cause a high reject rate, whereas a properly developed resist is the foundation for a high-yield process. The quality of the resist pattern determines the success of the subsequent process steps.

In early days of wafer fabrication, resist development was a stand-alone process step, with its own tool and workstation. Cassettes of wafers were manually moved from the exposure tool to the develop operation. The manual processing and lack of tool controls produced excessive variability that is unacceptable for submicron lithography. In modern wafer fabrication automated wafer tracks have integrated the development operation into a comprehensive process of photolithography. This represents steps one through seven of the eight-step photolithography process.

The eight steps to photolithography are in Table 15.1. The highlighted steps are covered in this chapter.

TABLE 15.1 Eight Basic Steps of Photolithography

Step	Chapter Covered
1. Vapor prime	13
2. Spin coat	13
3. Soft bake	13
4. Alignment and exposure	14
5. Post-exposure bake	**15**
6. Develop	**15**
7. Hard bake	**15**
8. Develop inspect	**15**

The procedure used to develop resist depends on whether it is positive-tone or negative-tone, and whether it is a conventional i-line resist (DNQ-novolak) or chemically amplified deep UV (CA DUV) resist. Positive resists are the norm for submicron lithography. Noncritical layers typically use conventional i-line resist (making up the major share of photolithography processing), while critical layers with CDs of 0.25 μm and below use DUV resists.

Advanced Lithography

Optical lithography has thrived while contributing to the continual reduction of device feature sizes. It is now expected by some industry experts that optical lithography will continue as the main lithography process until after the arrival of the 0.1 μm technology node sometime around 2006.[1] The reason optical lithography has continued to succeed in wafer fabrication is the ongoing introduction of improvements in equipment, process, and design. We reviewed new exposure techniques in Chapter 14, such as optical proximity correction (OPC) and phase-shift masks (PSM). At the end of this chapter we will review next generation microlithography technologies.

POST-EXPOSURE BAKE

After the wafer with exposed resist exits the exposure system, it enters the wafer track system and undergoes a short *post-exposure bake* (*PEB*) step. A thermal PEB is necessary for chemically amplified DUV resists to catalyze (initiate) critical resist chemical reactions. For conventional i-line resists based on DNQ chemistry, PEB is done to improve adhesion and reduce standing waves. Resist manufacturers include recommended time and temperature specifications for PEB in their product literature.

DUV Post-Exposure Bake (PEB)

It is during the post-exposure bake (PEB) that the exposed regions of a chemically amplified DUV resist become soluble in the developer. Recall that for a chemically amplified DUV resist, a protecting chemical (e.g., t-BOC) makes the resist insoluble in the developer. During UV exposure, a photoacid generator (PAG) generates an acid in the exposed regions. To make the exposed resist soluble to the developer, the post-exposure bake (PEB) heats the resist, which causes the acid-catalyzed deprotection reaction. The acid removes the protecting group from the resin and the exposed resist is now soluble in the developer solution (see Appendix E).

PEB is an important step in resist processing for chemically amplified DUV resists. The requirement for PEB to catalyze the chemical deprotection reaction must be considered nearly as critical as exposure in terms of control, uniformity, and latitude requirements.[2]

Temperature Uniformity ■ The temperature uniformity and duration of PEB for DUV resist is important. Excessive variations will affect the kinetics of the acid catalytic reaction in the resist. Most often, PEB is done on a hot plate in an automated wafer track system. The actual temperature and time that the coated wafer is heated by the hot plate depends on the type of resist used. A representative PEB temperature and time is 90 to 130°C for 1 to 2 minutes. The PEB temperature is usually 10 to 15°C hotter than the soft bake. The hot plate temperature variation and the bake latitude of the particular DUV resist is critical and can affect the amount of CD variation in the resist during the develop step. For commercially available DUV resist systems, a representative post-exposure bake latitude for CD variation is about 5 nm /°C.[3] To reduce CD inconsistencies, hot plates are set at 130°C and controlled within ± 0.1°C.[4]

PEB Delay ■ Early DUV resists were very sensitive to the delay time from UV exposure to PEB. A delay greater than a few minutes permitted the acid to neutralize due to amine contamination from the ambient air. The neutralization occurred on the top surface of the resist, creating a thin, less-soluble inhibition layer that led to the formation of a "T-top" after development (see Figure 15.1). More recent DUV resists permit a delay of up to about 30 minutes. However, it is still desirable to develop the resist as soon as possible after exposure to minimize any potential chemical reactions that can inhibit the development process.

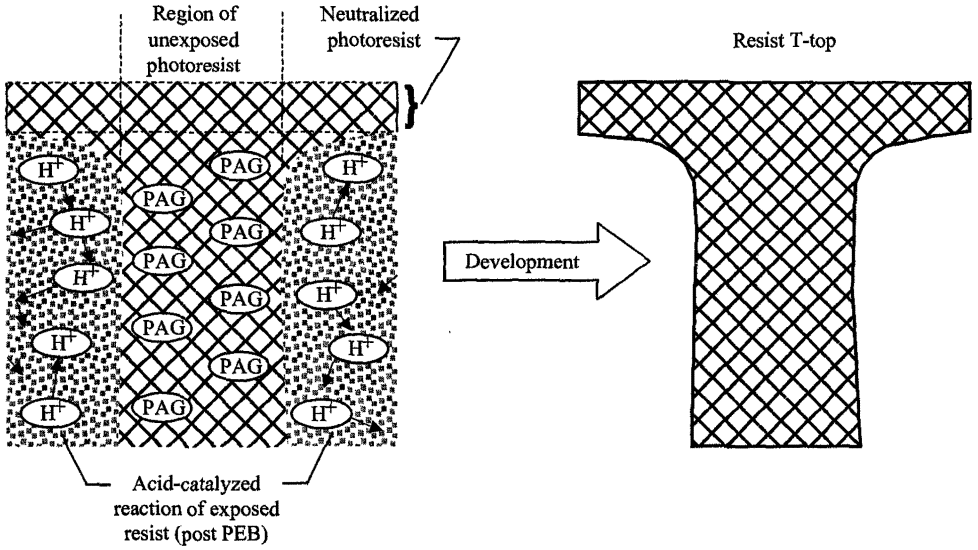
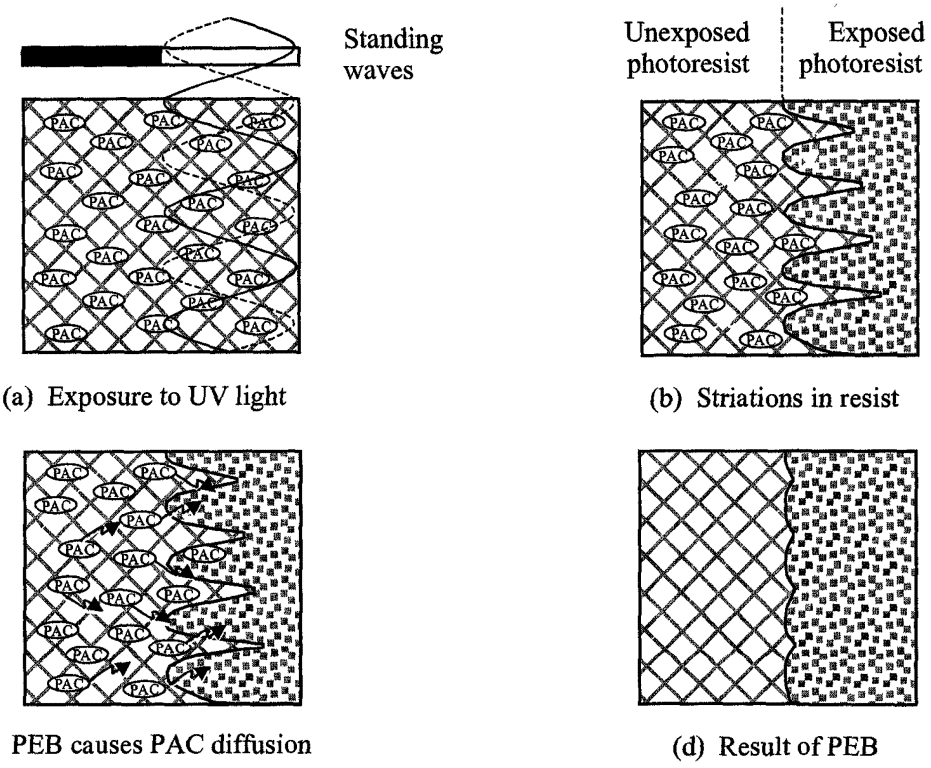


FIGURE 15.1 Amine Contamination of DUV Resist Leading to T-top Formation

Conventional I-Line PEB

It is common practice to perform a PEB for conventional DNQ-novolak i-line resist. The PEB extends some of the same benefits gained by the soft-bake step that occurred before exposure. PEB helps drive out remaining solvents that are left in the resist, reducing solvent content from 7 to 4% (before exposure) to about 5 to 2%.[5] The most significant benefit from PEB for i-line resist is a reduction in the standing wave defect from reflective surfaces during exposure.

Recall from Chapter 14 that standing waves result from light exposure of a resist that is coated on a reflective substrate. Coherent light reflects off the substrate and interference produces a nonuniform intensity in the resist film that appears as standing waves in the sidewall. The PEB minimizes the standing wave effect because the increased temperature causes the PAC sensitizer in the resist to diffuse through the novolak polymer matrix, essentially producing an averaging effect across the standing wave boundary (see Figure 15.2).



(a) Exposure to UV light

(b) Striations in resist

(c) PEB causes PAC diffusion

(d) Result of PEB

FIGURE 15.2 Reduction of Standing Wave Effect Due to PEB

DEVELOP

Photoresist development (develop) uses a liquid chemical developer to dissolve the soluble regions of the resist that were formed during the mask exposure. The primary goal of resist development is to accurately replicate the reticle pattern in the resist material. The emphasis is on producing CD features that meet the required specifications. If the CDs meet the specifications, then all other features are assumed acceptable since the CD is the most difficult structure to develop.

Resist patterning problems occur if the development process is not properly controlled (see Figure 15.3 on page 417). These resist problems can negatively affect production yield, showing up as defects in the subsequent etch process. The three primary types of development problems are underdevelopment, incomplete development, and overdevelopment. The photoresist lines in Figure 15.3 illustrate these types of problems as compared to a normal developed line. An underdeveloped line appears wider than a normal line and will have sloping sidewalls. The incomplete developed line has residual resist on the substrate that should have been removed during develop. Overdevelopment removes too much resist causing features to appear narrower and poorly-defined.

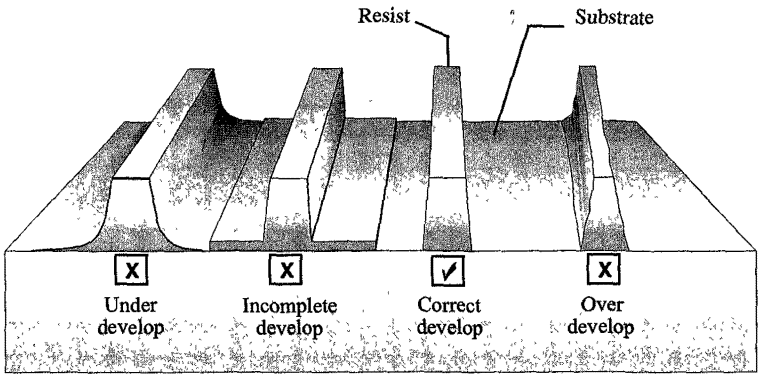


FIGURE 15.3 Photoresist Development Problems

Negative Resist

Negative resist is crosslinked (hardened) by exposure to UV light. This makes the exposed resist nonsoluble in the developer solution (see Figure 15.4).

Very little chemical reaction is necessary for *negative resist development* in the developer solution. This process consists mainly of a solvent wash of the unexposed resist, which is not crosslinked and therefore soft and soluble. The developer is typically an organic solvent such as xylene that is sprayed on the resist while the wafer is spinning on a vacuum chuck. Developer spray may be followed by another organic solvent sprayed on the wafer to stop the develop process.

An organic solvent rinse cycle is then introduced to clean the wafer and remove partially crosslinked pieces of resist. In addition, rinse removes any remaining developer to ensure the development process stops. Rinse typically consists of an organic solvent such as n-butylacetate or an alcohol or trichloroethylene. There is finally a spin-dry step to dry the wafer.

A significant problem with negative resist is swelling and distortion of the crosslinked exposed resist due to absorption of the developer solution during the wash. Because of this, the sidewalls of remaining negative resist on the wafer become jagged and swollen. This absorption is a primary reason why traditional negative resists are not suitable for geometries below about 2 μm. There is ongoing research into improving negative resists to minimize swelling.

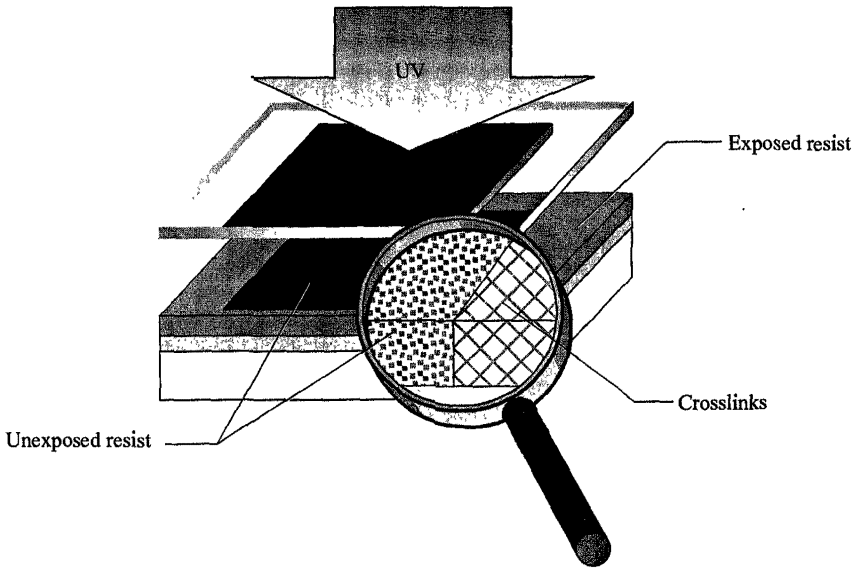


FIGURE 15.4 Negative Resist Crosslinking

Positive Resist

Positive-tone resists are the most common resists used in submicron wafer fabrication due to improved linewidth resolution. The two general types of positive resists used in wafer microlithography are conventional DNQ i-line resists (noncritical layers down to 0.35-μm linewidth) and chemically amplified (CA) DUV resists (critical layers with 0.25-μm linewidth and below). Both of these types of resists use a phenolic-based resin. Conventional i-line resists consist of a novolak resin, while CA DUV resists commonly use a PHS resin. The type of resin is important for resist development because this is the material that the developer will remove in order to pattern the resist. Although these two resists are very different chemically (see Chapter 13), it is generally true that phenolic resin is soluble in a base solution.

Developer ■ *Positive resist development* involves a chemical reaction between the developing solution and the resist to dissolve the exposed resist (see Figure 15.5). The rate at which a developer dissolves the resist is termed the *dissolution rate* (also referred to as the speed of the developer). A fast dissolution rate is desirable for productivity, but too fast a rate can also be bad for resist performance. Developers also have selectivity. High *developer selectivity* means the developer reacts quickly with the exposed resist (fast removal rate) relative to the slow reaction with the unexposed resist (slow removal rate). A developer with high selectivity produces sharper and cleaner resist sidewalls, which is desirable for high-density patterning.

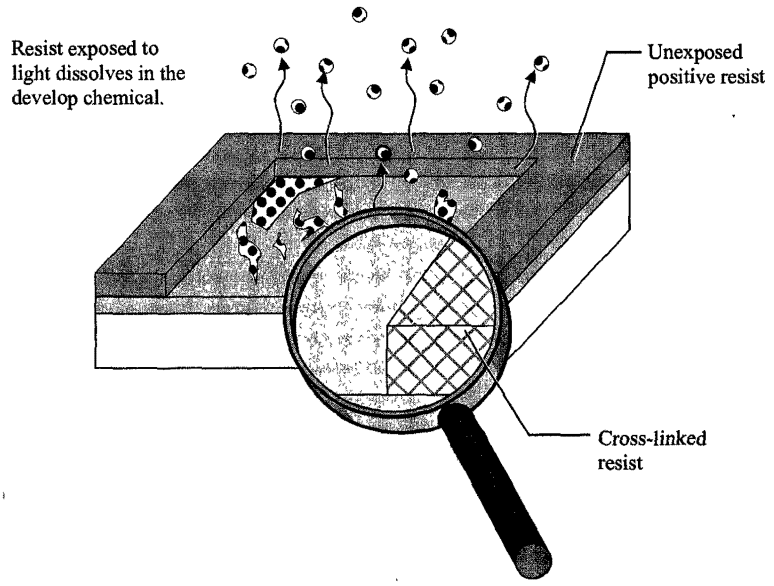


FIGURE 15.5 Development of Positive Resist

The chemical reaction of developer with positive resists is significantly different than the solvent wash needed to dissolve negative-tone resists. Positive resist developer solution is based on a strong alkaline diluted with water (aqueous) developer. Early developer solutions were an alkaline-water mixture of sodium hydroxide or potassium hydroxide. However, both of these solutions contain mobile ionic contaminants (MICs), which are unacceptable for processing high-performance IC circuits sensitive to corrosion. The most common developer today for positive-tone resists is tetramethyl-ammonium hydroxide (*TMAH*). This developer has a very low concentration of metal ions, particularly sodium ions, to avoid introducing MICs on the wafer surface. An advantage of aqueous developers is that the rinse only requires DI water.

Standardized TMAH developer formulations are common in the industry. These developers are more economical and they improve developer repeatability for better quality control. TMAH developer concentrations in the range of 0.2 to 0.3 normality (N) allow sufficient resist selectivity with high contrast between exposed and unexposed resist regions. *Normality* refers to the exact chemical makeup of a particular developer (or any chemical solution); it has a direct effect on developer

dissolution rates. A 0.26 N TMAH solution is becoming a standard for resist processing.[6] The objective is to have a high selectivity toward removing the exposed portions of the resist while leaving the unexposed resist intact on the wafer.

Exposed positive resist dissolves into the TMAH developer. The unexposed resist does not dissolve into nor absorb any of the developer. For this reason positive unexposed resist does not swell as with the negative resist. The lack of swelling makes positive resist desirable for producing submicron geometries.

TMAH requires careful control of the developer strength as measured with pH. It is also important to control the developer solution temperature and DI water rinse temperature. The dissolution rate varies as a function of developer temperature, with a result of faster resist dissolution occurring at lower developer temperatures.[7] Small ppm levels of surfactants are often added to the TMAH developer. A surfactant reduces surfaces tension and increases wetting, which makes a liquid flow across the surface better. This condition improves the dissolution of small geometry features such as contacts. Surfactants also minimize any residual film left on the resist surface.

TMAH developer chemistry for positive resist is highly caustic, meaning it destroys or erodes by chemical action. Alkaline chemicals erode metal as well as human tissue. Proper safety precautions (e.g., chemical protective clothing and eyewear) must be used by technicians when working around develop stations, such as on the automated wafer tracks.

Conventional I-Line Resists. Recall from Chapter 13 that positive i-line resists create carboxylic acid during UV exposure. When TMAH developer is applied to exposed resist, a chemical reaction occurs that neutralizes the carboxylic acid by the alkaline TMAH developer. The neutralized carboxylic acid of the exposed resist rapidly goes into solution. The unexposed (hard) resist does not react with the developer and remains intact on the substrate surface.

Chemically Amplified DUV Resists. To review, chemically amplified (CA) DUV resists often consist of phenolic resin in the form of PHS (poly[hydroxystyrene]). PHS has a protection group (such as t-BOC) that makes the PHS insoluble in the base developer. The PAG (photoacid generator) in the CA DUV generates an acid during exposure. During post-exposure bake, this acid removes (or "cleaves") the protection group away from PHS in exposed regions. The PHS is now highly soluble in the base developer.

The developer does not actually react with the PHS during the development operation. This isbecause there are hydroxyl OH groups that exist in a "corkscrew" configuration along the PHS polymer chain. These OH groups create effective diffusion paths and bring about extremely high dissolution rates for the PHS in the basic developer solution.[8]

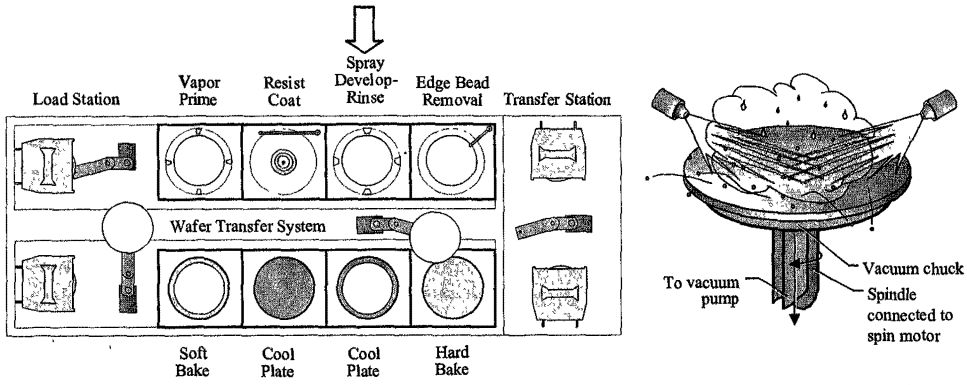
Development Methods

Static immersion of a cassette of wafers into developer solution was an early method for resist development. However, it is no longer used today in high-volume production. Batch production is not suitable for automated wafer tracks that efficiently transport single wafers simultaneously between photolithography operations. Static immersion consumes a large quantity of developer chemicals. Furthermore, batch immersion is not conducive to producing uniform development for high-density ICs across large diameter wafers.

The two most common development techniques used to remove exposed resist on spin-coated wafers today are:

- Continuous spray development
- Puddle development

Continuous Spray Development ■ The dissolution of exposed resist with a *continuous spray develop* tool and solution is a similar process to resist dispense systems. In the past, batch development was done using spray systems similar to a spin-rinse-dryer. Development can also be done in a wafer track system after the wafer has completed post-exposure bake. A single wafer is positioned on a vacuum chuck and spun at a slow speed (e.g., 100 to 500 RPM) while one or more nozzles dispense developer on the resist-coated wafer surface (see Figure 15.6). The developer is dispensed in a fine mist, with some processes using ultrasonic atomization to allow for low-velocity dispersion. A low-velocity exit minimizes adiabatic (constant heat transfer) cooling effects during dispense, where the



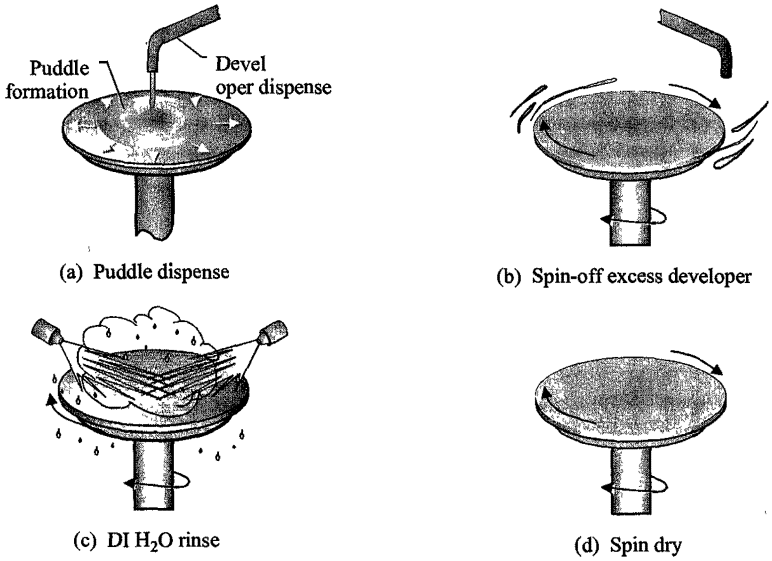
(a) Wafer track system (b) Developer spray dispenser

FIGURE 15.6 Resist Development with Continuous Spray

temperature of the developer drops due to its expansion from a high pressure region to a low pressure region. Early nozzle designs required a heating system for the developer to minimize the cooling effect.

The nozzle spray pattern and speed of the wafer rotation are critical variables to achieve repeatability in the resist dissolution rate and uniformity across the wafer. In recent years the spray process method has been largely replaced by puddle development because the latter method allows more process latitude for these variables.

Puddle Development ■ The *puddle develop* approach uses the same basic equipment as the spray method to develop the resist. A small amount of developer is dispensed onto the wafer and forms a puddle (see Figure 15.7). Adequate developer volume is needed to form a puddle meniscus over the entire wafer. Excessive developer is avoided to minimize backside wafer wetting. The wafer can be stationary or slowly rotating on a heated chuck.



(a) Puddle dispense (b) Spin-off excess developer

(c) DI H_2O rinse (d) Spin dry

FIGURE 15.7 Puddle Resist Development

There are variations as to whether the wafer is static or rotating after the initial developer is puddled on the wafer. In all cases, the developer must be left on the resist for sufficient time to allow the soluble resist areas to become completely dissolved. As an example, a multiple-puddle method is used where the first puddle is left on the wafer for a predetermined time (such as 10 to 30 seconds, depending on the type of developer). It is then spun off and a new puddle is dispensed and

left on the wafer for a defined time. This second puddle replenishes the developer chemicals and rejuvenates the chemical reaction between the developer and the resist. Some manufacturers also spray the developer onto the wafer during the second puddle application.

After the resist has dissolved in developer, the wafer is rinsed with DI water and spun dry. It is important to rinse all remaining chemicals after development from both the topside and backside of the wafer.

For optimal performance, the flow of developer is kept low to reduce variations in development rate at the edge of the wafer. This reduction is an advantage of puddle development over spray because a minimal amount of developer chemical is used. At the same time, adequate developer volume is needed to achieve full and uniform coverage over the entire wafer. Puddle development introduces fresh chemicals for every wafer, which improves wafer-to-wafer uniformity. The puddle development method minimizes temperature gradients and permits control of the variables affecting uniformity of single wafer resist development.

Resist Development Parameters

Critical parameters must be controlled during the development process. These parameters are:

- Developer temperature
- Developer time
- Developer volume
- Wafer chuck
- Normality
- Rinse
- Exhaust flow

Developer Temperature ■ The optimum temperature for developer mixtures is between 15 to 25°C. The temperature must be maintained to within ± 1°C or better from the optimal setpoint once it has been determined. The temperature of the developer has a direct effect on resist dissolution rate. As previously noted, faster resist dissolution for positive resists occurs at lower developer temperatures. For solvent developers (negative resist), the dissolution rate increases with an increase in temperature.

Developer Time ■ Developer continues to react with resist until it is removed by a rinse process. This condition can lead to overdevelopment of the resist and cause unacceptable CD variations. Off-line analysis of CD resist linewidth can be done on a sample of wafers from a batch to determine optimum develop time. However, this sampling gives only limited information and is costly.

An in-situ *dissolution rate monitor* (*DRM*) is used in automated wafer track systems for real-time monitoring of the development process.[9] A DRM uses interferometric signal data collected by an optical sensor that measures the phase difference of light reflected off the baked-on resist film surface and the wafer surface underneath. As the resist dissolves, the phase difference between the two surfaces decreases to zero at the breakthrough point for endpoint (EP) detection. Monitoring each wafer with a DRM provides more useful information about the develop process and permits more accurate control of CDs.

Developer Volume ■ The amount of developer volume dispensed on the wafer is critical for successful resist development. The use of inadequate developer volume results in *scumming*, which is a residue film left on the wafer surface if it has been underdeveloped (such as from inadequate developer volume) or improperly rinsed. Excessive developer is undesirable because the goal is to reduce chemical usage in the fab. Excessive developer is a cost issue, but this condition will not necessarily ruin the resist on the wafer.

Normality ■ *Normality* (*N*) is a concentration unit that refers to the quantity of substances (stoichiometry) in a solution. For a particular developer, normality represents the exact chemical makeup, which in turn indicates how strong or weak the developer is. Normality has a direct effect on resist dissolution rates. It is primarily altered by the addition of moisture, so the chemical distribution system must be carefully controlled to minimize leaks.

Rinse ■ Rinsing is typically done with DI water, which is sprayed onto the wafer, and then the wafer is spun dry. Rinse serves to stop the development process and also remove developer from the wafer surface.

Exhaust Flow ■ The develop module is enclosed on the wafer track machine. The exhaust flow is critical so as not to disturb the developer that is applied in spray form. Too low an exhaust can leave residual developer mist in the developer module, which builds up and reacts with subsequent wafers.

Wafer Chuck ■ The wafer must be held perfectly flat on the wafer chuck during the static or spin development cycle. This placement ensures coverage uniformity during puddle development.

HARD BAKE

A post-development thermal bake, referred to as *hard bake,* is done to evaporate any residual solvent and harden the resist. This action improves the resist's adhesion to the substrate and prepares it for subsequent processing, such as becoming more resistant to etch. Hard bake also removes any residual developer and any water.

Since all light exposure is complete, the baking temperature for hard bake can be elevated toward the solvent boiling point, effectively evaporating the solvent and achieving maximum resist densification. For DNQ-novolak resist, there is also the need to evaporate any remaining DNQ to avoid nitrogen diffusion during subsequent high-energy processes. The nitrogen causes localized resist popping in the densified resist, which disperses resist particles on the wafer surface.[10]

The starting point for the hard bake temperature is the recommended setting determined by the resist manufacturer. After that, the process can be fine-tuned to meet the adhesion and dimensional control necessary for the product. Nominal hard bake temperatures are 130°C for positive resist and 150°C for negative resist. Hard bake is typically done on an in-line hot plate in a wafer track system, or in an in-line oven. Resist is a material that softens and flows when sufficiently heated (see Figure 15.8). Higher hard bake temperatures could cause the resist to flow slightly, which can deform the pattern.

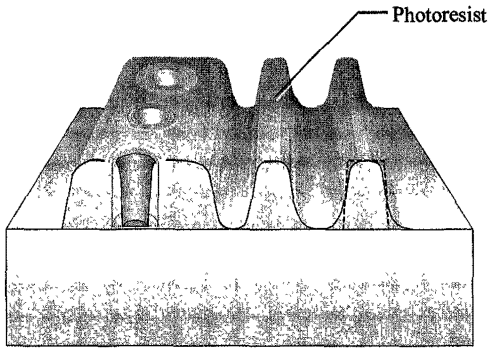
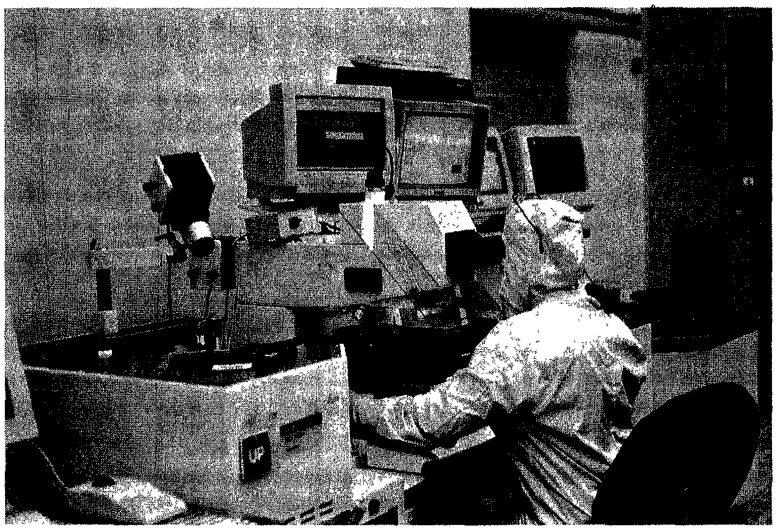


FIGURE 15.8 Softened Resist Flow at High Temperature

Resist Hardening With Deep UV. Resist hardening of DNQ-novolak resist is also achieved by exposing it to deep UV. This exposure causes the positive resist resin to crosslink and form a thin surface crust, which increases the resist thermal stability. The crosslinked resist can now withstand thermal processes up to 210°C without significant resist flow.[11] This condition is beneficial for subsequent processing such as plasma etching and ion implant (see Chapters 16 and 17, respectively), where temperatures can rise up to 125 to 200°C. If the resist is not sufficiently hardened, it risks flowing, which reduces the resolution of the original pattern.

DEVELOP INSPECT

The imaged pattern in the resist undergoes a *post-develop inspection* to find defects. This step is necessary to identify and remove defective wafers before they continue to the following processes of etch or implant. A wafer with a defective resist pattern that is etched or implanted will become scrap. The post-develop inspection is used to characterize the photo process, providing information to the photolithography production team for corrective action.



Automated Inspect Tool for Develop Inspect
(Photo courtesy of Advanced Micro Devices)

Most post-develop defects are relatively large and belong to a wide range of defect types (see the Quality Measure section at the end of this chapter). The defects may occur during all previous photolithography steps plus during the processing before lithography. Post-develop inspection requires a flexible system. Traditionally, this inspection has been a manual, operator-intensive inspection process with an optical microscope. Depending on the criticality of the resist layer, the inspection may be done on a sample basis. Automated inspection equipment for post-develop inspection is becoming more common in advanced fabs, especially for deep submicron lithography where the defects are not detectable with optical microscopes.

There are two possible outcomes for a wafer that fails post-develop inspection. If the wafer has a problem from a previous operation that makes it unacceptable, then the wafer is scrapped. If the problem is associated specifically with the quality of the pattern in the resist film, then the wafer is reworked. Wafer rework is done by stripping the photoresist off the wafer surface and inserting the wafer back into the photolithography process (see Figure 15.9).

This is one of the few operations in the fabrication process where rework of rejected parts is possible. The percent of wafers reworked is monitored and action plans are put in place for rejects. The goal is zero defects, while many fabs run typically less than 2% rejects. If the rework rate is greater than about 4%, then there is a quality problem that requires corrective action.

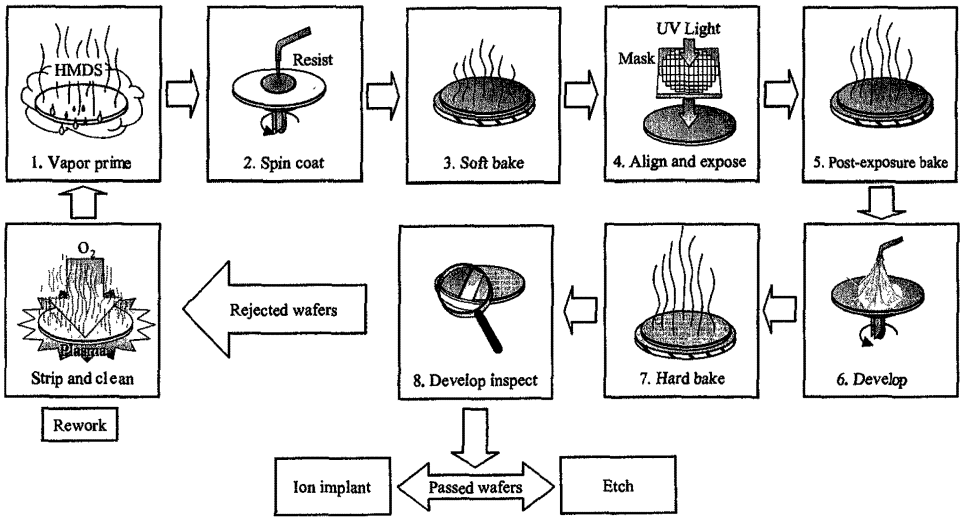


FIGURE 15.9 Develop Inspect Rework Flow

ADVANCED LITHOGRAPHY

The resolution capability of optical lithography has been extended by many equipment and process improvements, especially in the areas highlighted in Table 15.2. These improvements are the basis for a recent development in optical lithography referred to as subwavelength printing. *Subwavelength lithography* images CDs that are significantly less than the light source wavelength. An example is a 248 nm DUV light source used to print CD linewidths at 0.2 μm (200 nm) or below. Recent research activities have demonstrated a 50 nm CD pattern using a 248 nm DUV light source, chemically amplified DUV resist, and phase-shift mask. Subwavelength printing further extends the versatility of optical lithography while lowering its cost of ownership.

TABLE 15.2 Photolithography Improvements

1. Reduction in wavelength of the UV light source.
2. Increase in numerical aperture of optical lithography tools.
3. Chemically amplified DUV resists
4. Resolution enhancement techniques (e.g., phase-shift masks and optical proximity correction).
5. Wafer planarization (chemical mechanical planarization, or CMP) to reduce surface topography.
6. Advances in photolithography equipment (e.g., stepper and step-and-scan).

Next-Generation Lithography

Predicting the actual resolution limit of optical lithography has been a futile exercise for many years. There is some future limit where the extension of optical lithography will not be feasible. Wafer patterning must then transition to an alternative lithography process referred to as *next-generation lithography.* Major research activity is underway to investigate the type of next generation lithography tool that will replace optical lithography. Advanced study of this nature requires many years of research and development effort and sustained funding. There are four major lithography technologies considered as possible successors to optical lithography:[12]

- Extreme UV (EUV)
- SCALPEL
- Ion projection lithography (IPL)
- X-ray

Each of these technologies has demonstrated patterning capability down to 70 nm or below. At the time of this writing, International SEMATECH has selected EUV and SCALPEL for research funding as the next generation lithography tool.

Extreme UV (EUV) ■ *Extreme UV* lithography builds on the production knowledge of optical lithography. It uses a laser-produced plasma source to produce UV wavelengths of ~13 nm and is expected to print images down to about 30 nm.[13] The source operates in a vacuum environment to produce the EUV radiation, which is collected by condenser optics and formed into a beam (see Figure 15.10 on page 425). The beam is reflected off a reflective reticle that scans the pattern through the beam. An all-reflective (meaning mirrors instead of lens) 4X projection optics will image the UV beam onto a resist-coated wafer. The wafer is scanned at one-fourth the reticle speed in the opposite direction.

There are a number of challenges for bringing EUV into wafer production.[14] The precision optics will be difficult to achieve given the stringent requirements for manufacturing the high-quality surfaces. Mirror reflectivities will be optimized by using precision multilayer coatings on the surfaces. The reflective reticle is four times larger than the feature size; therefore, a 100 nm CD has a minimum reticle feature size of 400 nm (at 4X demagnification). The reticle consists of a thin metal absorber patterned on a multilayer coating that is patterned with conventional electron beam mask tools. The short wavelengths and penetration depths will require the use of top surface imaging resists (see the following section) or bi-layer resists with a very thin top layer. For alignment, the total overlay budget is approximately 35 nm for devices at the 0.1 μm design rules. All equipment will be in a vacuum environment.

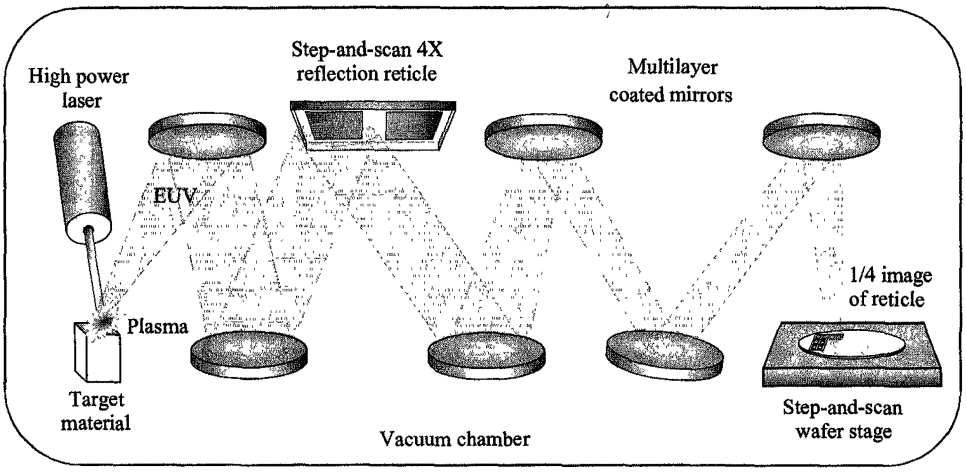


FIGURE 15.10 Concept for Extreme Ultraviolet Lithography
Redrawn from International SEMATECH's Next Generation Lithography Workshop brochure

SCALPEL ■ Feasibility studies are in progress for an electron beam imaging approach referred to as *SCALPEL* (SCattering with Angular Limitation Projection Electron Beam Lithography).[15] SCALPEL, in development since the late 1980s, uses an established electron beam source instead of a light source to image a wafer pattern (see Figure 15.11). A multilayer membrane mask is used that absorbs few electrons. The pattern is formed as the electron beam passes through a high atomic number layer in the mask that scatters the electrons for a high-contrast image at the wafer plane.

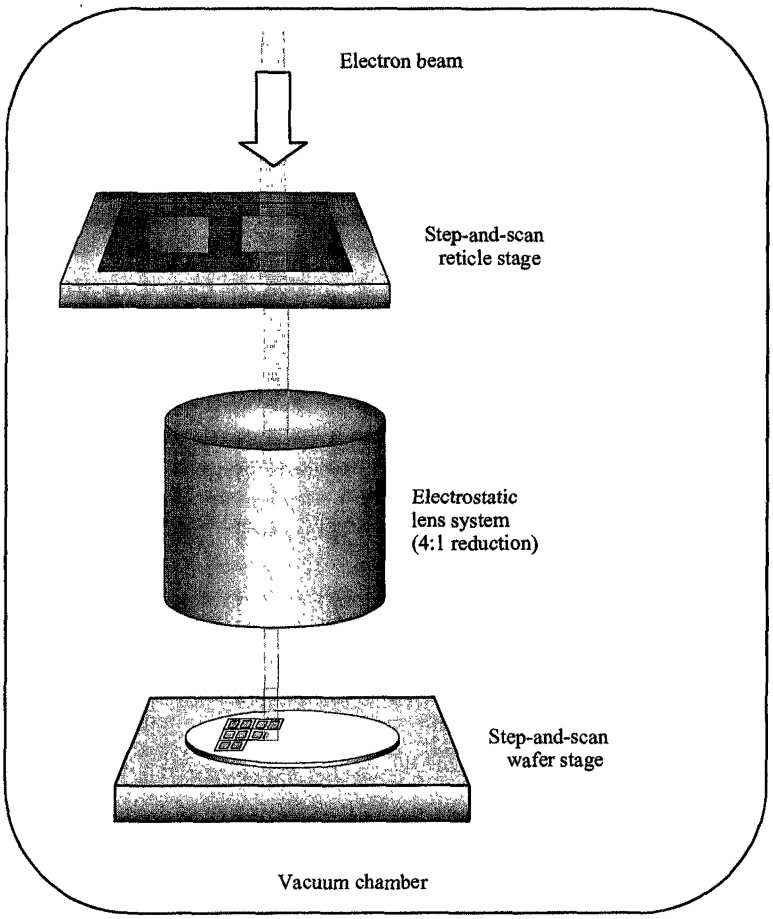


FIGURE 15.11 Concept of SCALPEL
Redrawn from International SEMATECH's Next Generation Litihography Workshop brochure

Increased beam current permits faster exposure but there is also a problem with beam blur caused by space charge effects at higher beam currents. Beam blur occurs when like-charged particles repel one another and cause the image to blur. The mask for SCALPEL is a 4X mask that does not require complicated resolution enhancement techniques, nor does the system need expensive optics.

SCALPEL prints linearly, using a step-and-scan writing strategy that produces stripes of exposed resist. To expose an entire chip, several stripes are stitched together per chip. This approach will require good overlay accuracy so that the stitching does not exceed CD error budgets. The first commercial SCALPEL tools are targeted for 2002.

Ion Projection Lithography (IPL) ■ *Ion projection lithography (IPL)* is a technique in early development that uses ion beams to expose resists, either through a mask or by serially writing on the resist with a finely focused beam (see Figure 15.12). If a mask is used, then a stitched approach is needed, using a broad beam to create small subfields of exposed resist on the wafer surface. IPL uses multielectrode electrostatic optics to direct hydrogen or helium ions to the wafer. Ions transfer their energy more efficiently to the resist than electron beams because ions have a larger mass. There are also fewer secondary electrons produced by ion bombardment and those produced have very low energy, which makes for less backscatter. Backscatter creates proximity effects that determine the limit to the minimum feature size for wafer patterning.[16] Very high resolution is achievable from ion projection lithography, with 50 nm feature sizes already demonstrated in a research environment.

X-Ray ■ *X-ray lithography* is an established technology for imaging patterns on wafers with CDs below 100 nm (0.1 μm). An X-ray source projects X-rays onto a special mask that forms a pattern

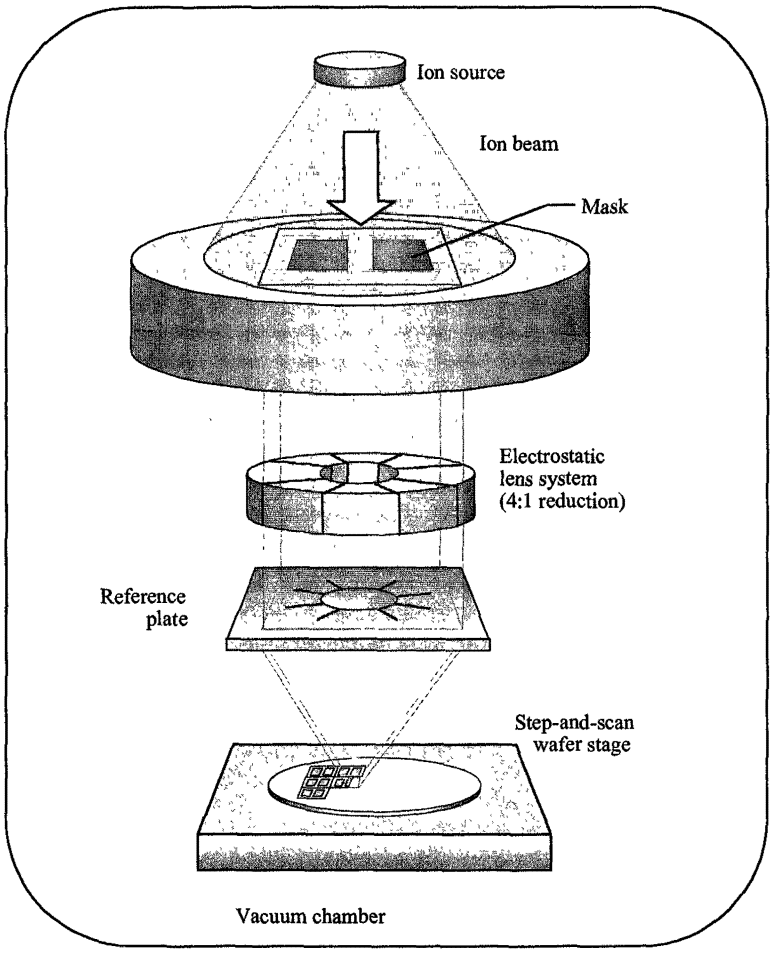


FIGURE 15.12 Ion Projection Lithography
Redrawn from International SEMATECH's Next Generation Litihography Workshop brochure

on a resist-coated wafer. This technique is not widely used for wafer fabrication, primarily due to its high cost of ownership in comparison to optical lithography.[17] One major chipmaker has used X-ray lithography for patterning commercial chips throughout the 1990s, including advanced microprocessors on 200-mm diameter silicon wafers. The system components for X-ray lithography are: (1) a mask that has a pattern of X-ray absorbing materials on a material that transmits X-rays, (2) an X-ray source, and (3) an X-ray resist.

The X-rays used in lithography are known as soft X-rays. They operate in a region of the electromagnetic spectrum from about 0.1 nm to about 10 nm (see Figure 15.13).[18] These differ from the familiar X-rays used in medicine, which have a shorter wavelength and are referred to as hard X-rays.

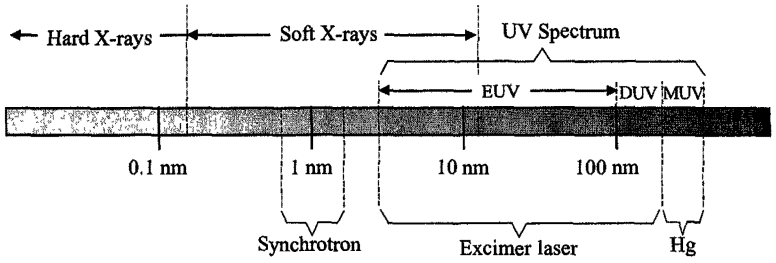


FIGURE 15.13 X-ray Spectrum

The most common X-ray source for lithography is known as a synchrotron (an electron storage ring). High-energy electrons are forced into closed curved paths by magnetic fields and made to accelerate which causes them to emit radiation. This action produces X-ray radiation that is very intense and reasonably collimated (parallel). A projection system based on special mirrors will project the X-rays onto the mask and resist coated wafer. Each synchrotron ring provides radiation for multiple X-ray steppers (e.g., 15 or more).

A special X-ray photomask is used to define the pattern. Because X-ray lithography has such a short wavelength, there are no diffraction interference effects from the mask, producing wide process latitude. An X-ray mask has a membrane substrate (e.g., polyimide) that transmits X-rays and a patterned material that absorbs X-rays, such as gold, tungsten, or tantalum (see Figure 15.14). However, the ability to fabricate masks is one of the many challenges for X-ray lithography. X-ray patterning uses a 1X mask that has the same dimensions as the wafer CDs. This feature eliminates the benefit from having a 4X mask with four times larger feature sizes than the wafer. Mask makers

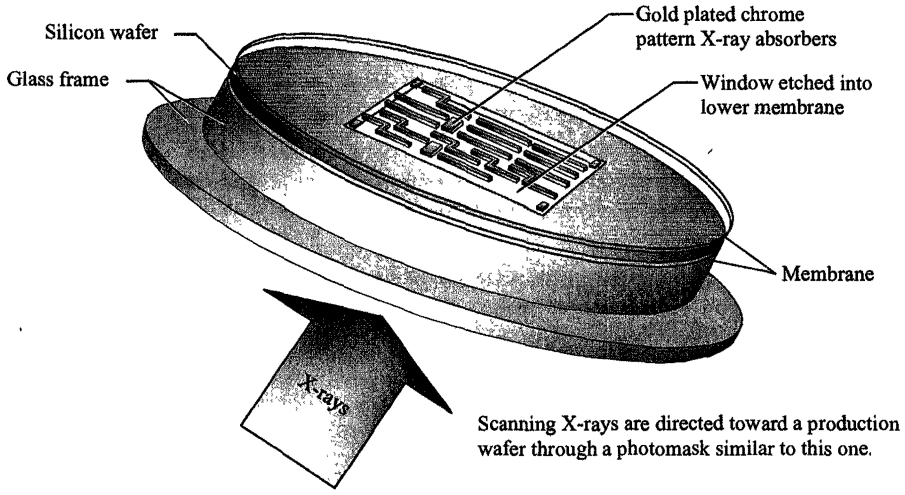


FIGURE 15.14 Concept of X-ray Photomask
Redrawn from K. Nalcamura, Lithography, *ULSI Technology,* ed. by C. Chang and S. Sze (New York: McGraw-Hill, 1996), p. 314.

are challenged to control pattern placement and CDs and minimize mask defects on X-ray masks with existing e-beam mask writers.[19]

Advanced Resist Processing

Photoresist has undergone two basic turning points in semiconductor manufacturing: (1) changing to positive resist, and (2) using chemically amplified deep UV resist (see Figure 15.15). Because resist is the medium that transfers the reticle pattern to the wafer surface material, it is a critical contributor to next-generation lithography.

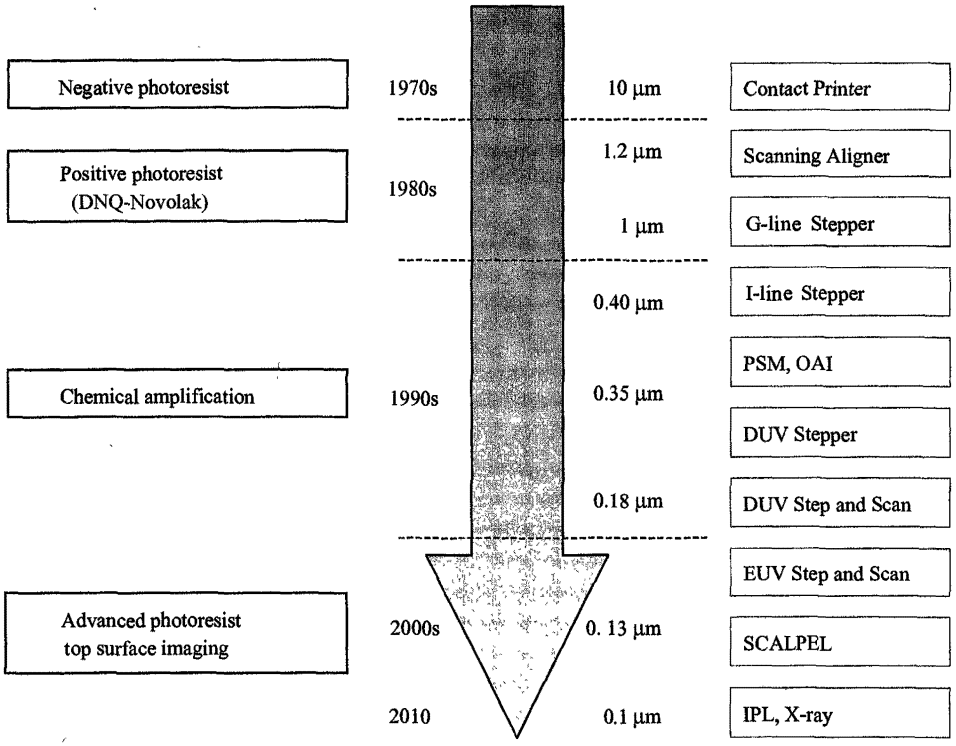


FIGURE 15.15 Development Trends of Photoresist and Lithography

An alternative resist technology that is being evaluated for sub-0.1 μm feature sizes is top-surface imaging resist. In *top-surface imaging*, the photoresist is imaged only at its top surface. This feature action provides a wider process latitude for focus issues than that found on typical resist systems since conventional resist must have its entire resist thickness in focus. At the same time, top-surface imaging permits resist materials to be opaque to the exposure light.[20] This feature could be beneficial since 248 nm DUV resist materials become opaque when the UV wavelength is reduced to 193 nm.

DESIRE Process ■ There are different ways to achieve surface imaging on resists. One method is through a process referred to as DESIRE (diffusion-enhanced silylated resist), which uses *silylation* to selectively place a thin layer of silicon on a resist. This process effectively transfers the reticle pattern to the resist-coated wafer in the form of a silicon pattern on the top surface of the resist.

The silicon is applied by first exposing the spin-coated resist to UV light per the standard process (see Figure 15.16 on page 429). The unexposed resist has the PAC (photoactive compound) sensitizer that is a diffusion inhibitor, while the exposed resist is more susceptible to silicon diffusion. There is often a presilylation bake to crosslink unexposed resist and increase the contrast between the exposed and unexposed region. The silicon is then incorporated into the resist by treating it with a gas-phase silylating agent (such as hexamethyldisilazane, or HMDS) at elevated

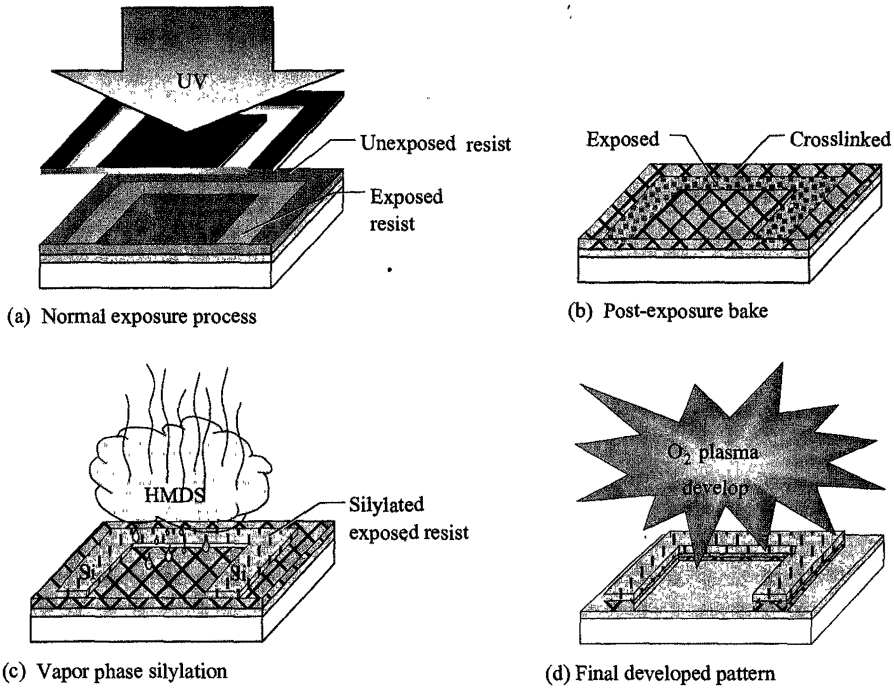


FIGURE 15.16 Top-Surface Imaging

temperatures. The exposed areas of the resist selectively bond chemically to the silicon to a depth of 100 to 200 nm.[21] The silicon-bonded areas of the resist represent the pattern transfer from the reticle to the substrate.

The final step is to dry-develop the wafers in oxygen plasma to remove the unprotected resist. During this plasma etch the silicon is converted into silicon dioxide which forms a thin protective mask that stops the etch process in the resist directly underneath the SiO_2. This is just one example of many silylation-based processes. They all essentially use a single-layer patterning technique that depends on selectively incorporating a silicon-containing compound into the photoresist after the exposure step.

DEVELOP QUALITY MEASURES

There are different types of defects found at post-develop inspect. The quality measures are shown in Table 15.3.

TABLE 15.3 Key Measures at Post-Develop Inspection

Quality Parameter	Types of Defects	Remarks
1. Critical dimensions.	A. Wider CDs than normal.	• Improper stepper focus. • Not enough time or energy during exposure. • Not enough develop time or weak developer solution. • Incorrect process recipes during exposure or develop steps.

Quality Parameter	Types of Defects	Remarks
	B. Narrower CDs than normal.	• Excessive time or energy during exposure. • Excessive develop time or strength of developer solution. • Incorrect process recipes during exposure or develop steps.
2. Contamination.	A. Particles and foreign contamination on the resist surface.	• Equipment needs to be kept clean, with special focus on the track equipment. • Inadequate cleaning and rinsing of wafers. • Developer chemicals and rinse water require point-of-use filters to remove contaminants.
3. Surface defects.	A. Scratches in the resist surface.	• Wafer handling errors or tool misadjustments related to cassette indexers and robotic handling systems.
	B. Particles, spots and stains.	• Chamber exhaust flow, dispenser alignment, dispense pressure, wafer leveling, splashbacks, drips, spin speed, are all possible contributors.
	C. Missing resist, extra resist, or scumming.	• Incorrect puddle time. • Incorrect dispense volume or position. • Improper rinsing after the develop process. • Improper or uneven baking.
	D. Striations in photoresist along the sidewalls of the resist features.	• Standing waves or reflective notches (unacceptable CD variation). • Improper or no antireflective coating (ARC) was used.
4. Overlay registration.	A. Improper alignment or overlaying of one layer over a previous layer.	• This is not a problem caused by the develop process. • It is more likely a stepper-induced problem. • Wrong process recipe or reticle was used. • Poor temperature and humidity control.

DEVELOP TROUBLESHOOTING

Various troubleshooting problems encountered during develop are shown in Table 15.4.

TABLE 15.4 Common Develop Troubleshooting Problems

Problem	Probable Cause	Corrective Actions
1. Linewidths and holes do not meet CD requirements.	A. Underdeveloped or underexposed positive resist across entire wafer.	• Ensure correct stepper process recipe was used. • Check for insufficient exposure time and energy settings. • Check stepper illuminator system. • Verify dose meter (light integrator) is functioning properly. • Ensure correct recipe on developer was used. • Check for insufficient puddle time and quantity settings. • Check developer equipment. • Check bake temperatures.
	B. Overdeveloped or overexposed positive resist across entire wafer.	• Ensure correct stepper process recipe was used. • Check for excessive exposure time and energy settings. • Check stepper illuminator system. • Verify dose meter (light integrator) is functioning properly. • Ensure correct recipe on developer was used. • Check for excessive puddle time and quantity settings. • Check developer equipment. • Check bake temperatures.
	C. No measurable CDs.	• Check exposure or develop operation. • Check reticle or process recipe. • Wafer may have skipped coat, expose, post-exposure bake, or develop step. • Rework wafer.
2. Resist scumming.	A. Resist residue remains on the wafer after the develop operation is completed.	• Check develop equipment process recipe. • Verify puddle time and puddle quantity are correct. • Check the rinser operation. • Check bake oven times and temperatures. • Rework wafer.

Problem	Probable Cause	Corrective Actions
3. Contamination and defects.	A. Possible causes may include the chemicals, rinse water, and process chamber.	• Verify puddle time and puddle quantity are correct. • Clean the develop process chamber, then recheck a test wafer for further contamination. • Check, and if necessary, replace line filters for the developer and rinse water.
	B. Misting or backsplashing from the dispenser can cause contamination.	• Check chamber exhaust level. • Check alignment of dispenser relative to the wafer. • Check for drips from dispenser assembly. • Rework wafer.
4. Collapsing of resist pattern after develop.	A. High aspect ratio (>5:1) will lead to collapsing of resist lines.*	• Verify that the resist is not excessively thick, since this will increase the aspect ratio and make the resist more likely to collapse. • Check that the resist has proper adhesion to the wafer. • The problem resolution may require a material or process change (e.g., more rigid resist).
5. Unacceptable CD variation at top of CA DUV resist profile.	A. Amine contamination of resist after exposure.	• Check integrity of environmental chamber filtering system. • Check to see if coated-wafers may have been exposed to external chemical contamination. • Asses whether resist is best selection for length of delay (newer resists withstand a longer time before PEB).

*J. Yu, et al., "Analysis of Resist Pattern Collapse and Optimization of DUV Process for Patterning Sub-0.20 mm Gate Line," *Advances in Resist Technology and Processing XV, Proceedings of SPIE,* Vol. 333, (Bellingham, WA: SPIE, 1998): p. 880.

SUMMARY

Resist development removes those areas of the resist rendered soluble by the exposure step. After exposure, a post-exposure bake (PEB) is performed for chemically amplified DUV resists to catalyze critical resist chemical reactions. The temperature uniformity, duration, and time delay for the PEB of DUV resist is important. For conventional DNQ-novolak resist, a PEB drives out additional solvent for better adhesion and reduces the standing wave effect. Negative resist development is mainly a solvent wash of unexposed resist. The exposed negative resist tends to swell during development, which limits its use in submicron lithography. Positive resist development involves a chemical reaction between the developer and the exposed resist, with parameters of develop speed and selectivity. The most common positive-tone developer is TMAH. The two most common development methods are continuous spray and puddle, which require the control of critical parameters for an optimum process. Hard bake is a post-development thermal bake used to drive out any residual solvent and harden the resist. A post-develop inspection is performed to characterize defects for corrective action and remove defective wafers from the process before etch or implant.

Lithography improvements have produced subwavelength lithography, where patterning achieves a CD below the exposure light wavelength. Next-generation lithography is evaluating the lithography technology for eventually replacing optical lithography. There are four primary alternatives: Extreme UV (EUV), SCALPEL, ion projection lithography (IPL), and X-ray. EUV uses a UV wavelength of about 13 nm to achieve a pattern resolution of 30 nm. SCALPEL uses an established electron beam for lithography. IPL uses ion beams to expose resist. X-ray lithography projects X-rays with a wavelength from about 0.1 to 10 nm onto a special mask to pattern a resist. Top-surface imaging is a technique usedto image only the top surface of the resist for reduced depth-of-focus and increased resolution.

KEY TERMS

resist development
post-exposure bake (PEB)
negative resist development
positive resist development
dissolution rate
developer selectivity
continuous spray develop
puddle develop
dissolution rate monitor (DRM)
scumming
normality
hard bake
post-develop inspection
subwavelength lithography
next-generation lithography
extreme UV (EUV)
SCALPEL
ion projection lithography (IPL)
X-ray lithography
top surface imaging
silylation

REVIEW QUESTIONS

1. Explain resist development. What is its goal?
2. Why is a post-exposure bake done for chemically amplified DUV resist? Be specific about deprotection.
3. Why is temperature uniformity important for PEB?
4. Describe the benefits of a post-exposure bake for an i-line conventional resist.
5. Explain negative resist development. What is the primary problem for submicron patterning?
6. Why is positive-tone resist the most commonly used resist?
7. What is the developer dissolution rate? Is it desirable for the rate to be high or low?
8. Explain resist selectivity and whether it should be high or low.
9. What is the name for the most common positive-tone developer?
10. Why is a surfactant added to the developer?
11. Explain how the TMAH developer functions for a conventional i-line resist.
12. Is there a chemical reaction between PHS and the developer for chemically amplified DUV resists?
13. List the two methods of resist development.
14. Explain continuous spray development.
15. Describe puddle development.
16. List the seven resist development parameters.
17. Explain why hard bake is done.
18. Describe UV resist hardening.
19. Why is a post-develop inspection performed?
20. What is subwavelength lithography?
21. List four alternative lithography methods under evaluation for next-generation lithography.
22. Explain extreme UV (EUV).
23. Describe SCALPEL lithography.
24. Discuss ion projection lithography (IPL).
25. Explain X-ray lithography. What is one of the major challenges for X-ray lithography?
26. Describe top-surface imaging. Why is silylation used in this process?

PHOTOLITHOGRAPHY MATERIALS AND EQUIPMENT SUPPLIERS' WEB SITES

Allied Signal	http://www.electronicmaterials.com/
Applied Materials	http://www.appliedmaterials.com/products/
Arch Chemicals (aka Olin)	http://www.olinmicro.com/default.asp
Ashland Specialty Chem.	http://www.ashland-act.com/
ASML	http://www.asml.com/
Canon Semiconductor	http://www.usa.canon.com/indtech/semicondeq/
Charles Evans and Associates	http://www.cea.com
Clariant Corporation	http://www.azresist.com/
Cymer Inc.	http://www.cymer.com/
DuPont	http://www.dupont.com/semiconductor/
Eastman Chemical	http://www.eastman.com/

EKC Technology	http://www.ekctech.com/ekctech.nsf
ETEC Systems Inc.	http://www.etec.com/semiprod_frame.html
FSI International	http://www.fsi-intl.com/
International SEMATECH	http://www.sematech.org/
JSR Microelectronics. Inc.	http://www.jsrusa.com/index2.html
J.T. Baker	http://www.jtbaker.com/
Karl Suss Inc.	http://www.suss.com/
Lucent Technologies	http://www.bell-labs.com/project/SCALPEL/
MICRO Magazine	http://www.miciromagazine.com/
Nikon	http://www.nikon.com/
Olin Microelectronics	http://www.olinmicro.com/
Photronics Inc.	http://www.photronics.com/
SEMI	http://www.semi.org/
Semiconductor International	http://www.semiconductor.net/
Shipley Company	http://www.shipley.com/
Silicon Valley Group	http://www.svg.com/
Solid State Technology	http://sst.pennet.com/home/home.cfm
SPIE	http://www.spie.org/
TEL, Tokyo Electron Ltd.	http://www.teainet.com
Ultratech Stepper	http://www.ultratechstepper.com/

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10. B. Smith, "Resist Processing," p. 561.
11. B. Smith, "Resist Processing," p. 562.
12. R. DeJule, "Next-Generation Lithography Tools: The Choices Narrow," *Semiconductor International* (March 1999): p. 48.
13. Ibid.
14. Challenges summarized from A. Hawryluk, N. Ceglio, and D. Markle, "EUV Lithography," *Microlithography Word* (Summer 1997): pp. 18–20.
15. R. DeJule, "Next-Generation Lithography Tools," p. 48.
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17. T. Ueno and J. Sheats, "X-ray Lithography," ed. J. Sheats and B. Smith (New York: Marcel Dekker, 1998), p. 403.
18. T. Ueno and J. Sheats, "X-ray Lithography," p. 405.
19. R. DeJule, "Next-Generation Lithography Tools," p. 48.
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21. K. Nakamura, "Lithography," *ULSI Technology,* ed. C. Chang and S. Sze (New York: McGraw-Hill, 1996), p. 294.

CHAPTER 16

ETCH

A wafer is fabricated into many functional microchips by creating electronic devices in the silicon and then sequentially depositing layers of dielectric and conductive materials to interconnect the devices. This is the concept of planar technology for wafer fabrication, used since the early days of semiconductor manufacturing.

In general, interconnect materials are deposited on the wafer surface and then selectively removed to form the circuit patterns that were defined by photolithography. This selective material removal process, known as etch, follows post-develop inspection. It is critical that etch be performed correctly or else the chip will not function. More importantly, once material is removed by etch, it is difficult to correct a mistake. Improperly etched wafers are most likely scrapped and discarded at a loss to the company.

Etch requirements depend on the type of feature being fabricated, such as the aluminum alloy metal stack, a polysilicon gate, a silicon trench for isolation, or a dielectric via. IC structures are complex, with a range of materials that require different etch parameters. Shrinking feature sizes drive tighter etch dimensional control and make inspections more difficult.

An example of an etch application is aluminum. The traditional metallization process deposits an aluminum alloy layer on the wafer surface. This action is followed by photolithography and etch to form the interconnects. The different metal layers are electrically connected by previously-formed tungsten plugs in interlayer dielectric (ILD) vias.

With the introduction of damascene processing for copper metallurgy, the metallization process becomes a dielectric etch to form a trench in the ILD. Copper is blanket-deposited into the dielectric patterns and polished back to the ILD height using chemical mechanical planarization. With damascene processing, there will be less emphasis on metal etch and more importance placed on dielectric etch.

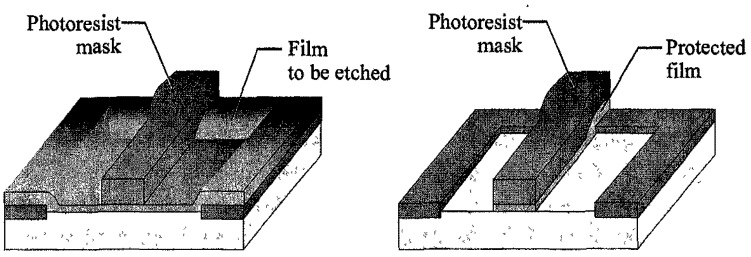
OBJECTIVES

After studying the material in this chapter, you will be able to:

1. List and discuss nine important etch parameters.
2. Explain dry etch, including its advantages, and discuss how etching action takes place.
3. List and describe the equipment systems for seven dry plasma etch reactors.
4. Explain the benefits of high-density plasma (HDP) etch, and discuss the four types of HDP reactors.
5. Give an application example for dielectric, silicon, and metal dry etch.
6. Discuss wet etch and its applications.
7. Explain how photoresist is removed.
8. Discuss etch inspection and its related important quality measures.

INTRODUCTION

Etch is the process of selectively removing unneeded material from the wafer surface by using either chemical or physical means. The fundamental goal of etching is to accurately reproduce the mask features on the resist-coated wafer. The patterned resist layer is not attacked significantly by the etchant. This mask layer is used to protect specific regions of the wafer surface while permitting selective etching through openings in the photoresist layer (see Figure 16.1 on page 436). The etch process follows photolithography in the general CMOS process flow (see Figure 16.2 on page 436). In this manner, etch can be viewed as the last major pattern transfer process step necessary to replicate the desired pattern on the wafer surface.



(a) Photoresist-patterned substrate (b) Substrate after etch

FIGURE 16.1 Applications for Wafer Etch in CMOS Technology

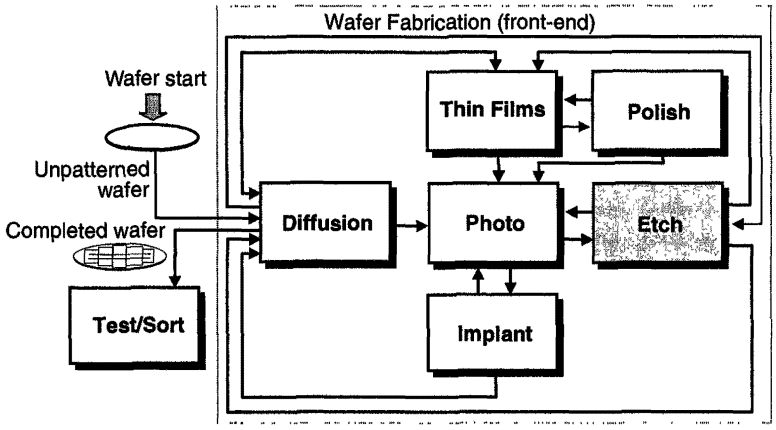


FIGURE 16.2 General CMOS Process Flow
(Used with premission from Advanced Micro Devices)

Etch Processes

Two basic types of etch processes are used in semiconductor manufacturing: dry etch and wet etch. *Dry etch* exposes the wafer surface to a plasma created in the gaseous state. The plasma passes through the openings in the patterned resist and interacts physically or chemically (or both) with the wafer to remove the surface material. Dry etching is the primary method used for etching devices with submicron geometries. Thus, dry etching will receive the most coverage in this text. In *wet etch*, liquid chemicals such as acids, bases, and solvents are used to chemically remove wafer surface material. Wet etch is generally applicable only for larger geometries (>3 μm). It is still used to remove some layers from the wafer and to remove dry etch residues.

Dry etch can also be categorized by the type of material removed. The three major material categories for etching are metal etch, dielectric etch, and silicon etch. *Dielectric etch* is used for applications with dielectric material, such as silicon dioxide. The formation of contact and via structures require a dielectric etch to form openings in the ILD. This is a challenge for etching high-aspect ratio openings (ratio of height to width for an opening). *Silicon etch* (including polysilicon) is used for applications requiring silicon removal, such as etching polysilicon transistor gates and silicon trench capacitors. *Metal etch* is primarily used for removal of aluminum alloy stacks to form interconnect wiring on metal layers. At the time of this writing, there is no acceptable method for etching copper metal with submicron feature sizes (which is an important reason for the introduction of dual-damascene processing into the wafer fab).

Etch can also be categorized as either patterned or unpatterned etching. *Patterned etching* uses a masking layer (patterned photoresist) to define areas of the surface material that are to be etched. Only selected portions of this wafer surface layer are removed during the etch process. Patterned etching is used to form the many different features on the wafer surface, including gates, metal interconnects, vias, contact holes, and trenches. *Unpatterned etching, etchback,* or *stripping,* occurs when the entire wafer surface is etched with no mask present. This etching process is used to strip masking layers (e.g., STI nitride strip and the titanium strip after the salicide process used

to form spacers for transistor implants). Etchback is used when it is desirable to reduce the overall thickness of a specific layer of film (e.g., when planarizing a surface to reduce topographical features). Photoresist is another example of a material stripped off the wafer. In summary, patterned and unpatterned etch processes can be performed using either dry-etch or wet-etch techniques.

ETCH PARAMETERS

Etch has specific requirements it must meet in order to replicate the mask pattern on the wafer surface material. Important parameters for etch are:

- Etch rate
- Etch profile
- Etch bias
- Selectivity
- Uniformity
- Residues
- Polymer formation
- Plasma-induced damage
- Particle contamination and defects

Etch Rate

Etch rate is the speed at which material is removed from the wafer surface during etching (see Figure 16.3). It is usually measured in Å/minute. The depth of the etched opening is known as the *step height.* It is desirable to have a high etch rate in order to keep wafer throughput high. This feature is even more important when using single-wafer processing in cluster tools. The etch rate is determined by process and equipment variables such as the type of material being etched, reactor configuration, gases used for the etch, and the process parameter settings. The etch rate is calculated by the following formula:

$$\text{Etch Rate} = \frac{\Delta T}{t} \qquad (\text{Å/minute})$$

Where, ΔT = amount of material removed (Å or μm)
t = time elapsed during etch (typically minutes)

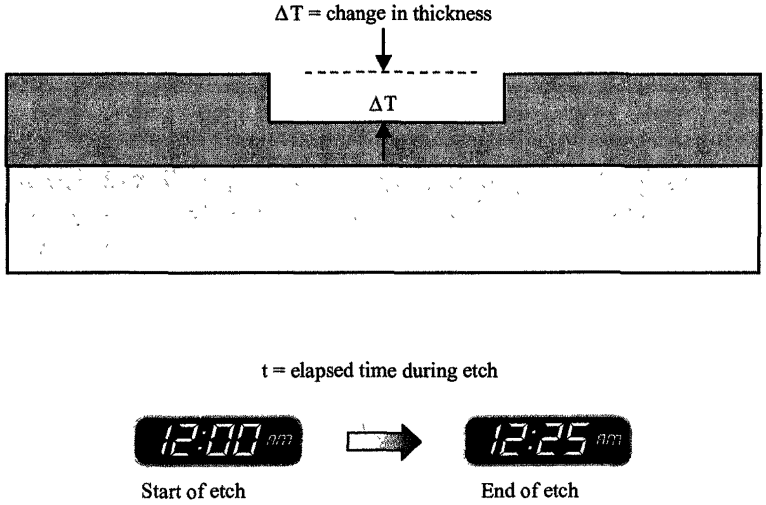


FIGURE 16.3 Etch Rate

Etch rate is generally proportional to the concentration of the etchant. Factors such as wafer surface geometry can affect the wafer-to-wafer etch rates. Wafers with significant surface area for etching will deplete the etchant concentration and etch slower, whereas wafers with small surface areas for etching will etch faster. This condition is referred to as *loading effects.* The decrease in etch rate is caused by the plasma etching reactions consuming most of the available etchant species in the gas phase. The change in etch rate due to loading effects is a primary reason why effective endpoint detection is critical (see the following section).

Etch Profile

Etch profile refers to the shape of the sidewall of the etched feature. There are two basic etch sidewall profiles: isotropic and anisotropic. An *isotropic etch profile* etches at the same rate in all directions (laterally and vertically), leading to undercutting of the etched material under the mask (see Figure 16.4). This action results in an undesirable loss of linewidth. Wet chemical etching is usually isotropic in nature, which is the primary reason why wet etching is not used for selective patterned etching of submicron devices. Some dry plasma systems are also capable of providing an isotropic etch profile. There are instances where isotropic etching may be desirable depending on the specific needs of the material being etched and the requirements of subsequent processing steps.

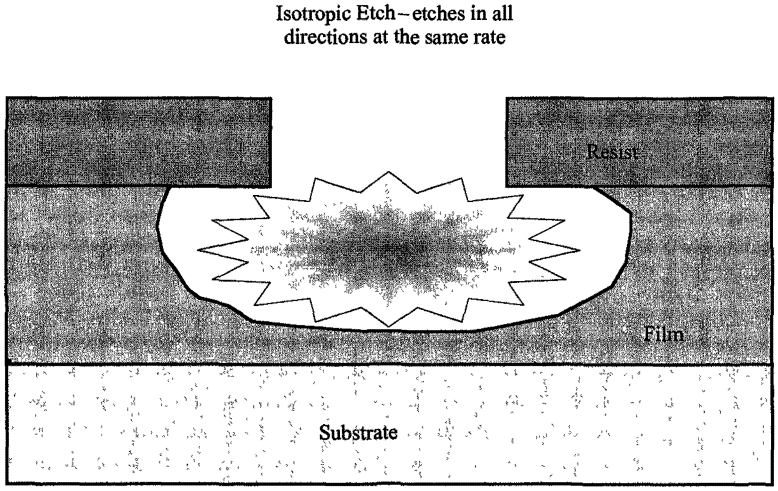


FIGURE 16.4 Wet Chemical Isotropic Etch

The desirable etch sidewall profile for submicron feature sizes is an *anisotropic profile,* where the rate of etching is in only one direction perpendicular to the wafer surface (see Figure 16.5). There is very little lateral etching activity. This leaves vertical sidewalls, permitting a higher packing density of etched features on the chip. Anisotropic etch is critical for the patterning of submicron devices with small linewidths and features. Advanced IC applications usually require 88 to 89° vertical sidewall profiles. Anisotropic etch is achieved with most dry plasma etching. Table 16.1 shows the profile for wet etch and the various profiles achievable with dry etch.

The amount of anisotropic etch can be moderate (slight sidewall angle) or highly anisotropic (vertical sidewalls). Etch profile refers to the shape of the etched film wall. A vertical profile is the result of a highly anisotropic etch.

With smaller geometries, the etch profiles have higher aspect ratios. It is difficult to get etchant chemicals in and reaction by-products out of the high-aspect ratio openings. To overcome this, it is desirable to have *directionality* to drive the plasma into the high-aspect ratio openings. If plasma ions are directional (perpendicular to the wafer surface), then only the surface is bombarded, not the feature's sidewalls. This action forces etchant chemicals into high-aspect ratio openings with little undercutting. For advanced ICs with sub-0.25 μm CDs, directionality is achieved with a high-density plasma source capable of generating enough etchant species to achieve acceptable etch rates.

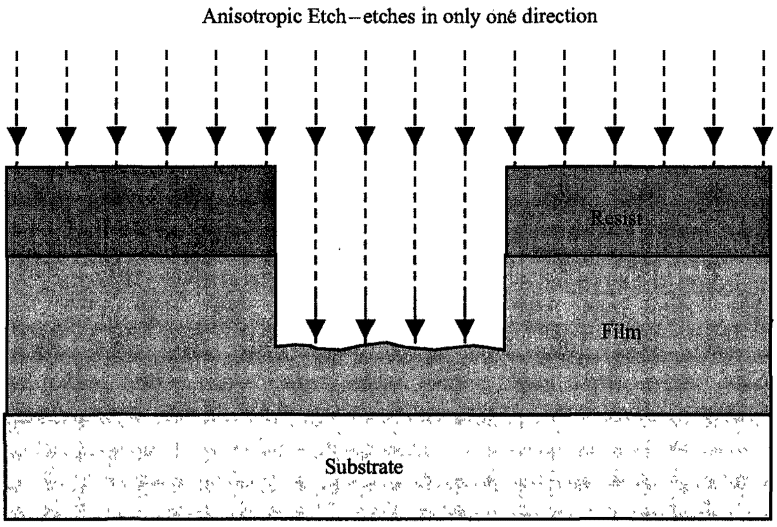


FIGURE 16.5 Anisotropic Etch with Vertical Etch Profile

TABLE 16.1 Sidewall Profiles for Wet Etch Versus Dry Etch

Type of Etch	Sidewall Profile	Diagram
Wet Etch	Isotropic	
Dry Etch	Isotropic (depending on equipment and parameters)	
	Anisotropic (depending on equipment and parameters)	
	Anisotropic—Taper	
	Silicon Trench	

Etch Bias

Etch bias is a measure of the change in linewidth or space of a critical dimension (CD) after performing an etch process (see Figure 16.6 on page 440). It is usually caused by undercutting (see Figure 16.7 on page 440), but can also be the result of an etch profile. Undercutting occurs when

the etch process removes excessive material below the mask, causing the top surface of the etched film to be recessed from the resist edge. The formula to calculate etch bias is:

$$\text{Etch bias} = W_b - W_a$$

Where, W_b = the original linewidth in photoresist before etch.
W_a = the final linewidth of the etched material after resist removal.

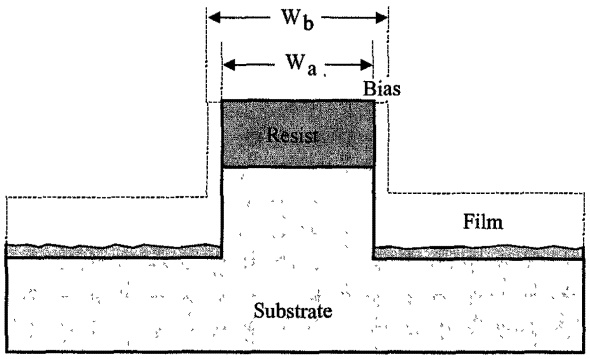


FIGURE 16.6 Etch Bias

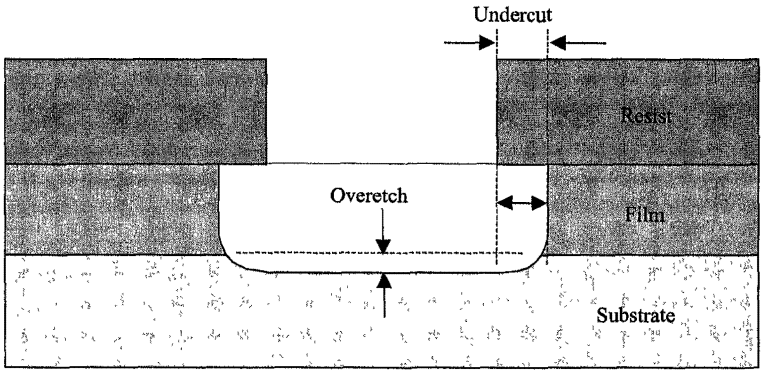


FIGURE 16.7 Etching Undercut and Slope

Selectivity

Selectivity represents how much faster one film etches than another film under the same etch conditions. It is defined as the etch rate of the material being etched relative to the etch rate of another material (see Figure 16.8). High selectivity means that etching only occurs on the desired layer. A high selectivity etch process does not etch the underlying film (etching stops at the right depth) and the protective photoresist is not etched. Shrinking geometries require thinner layers of resist. High selectivity is necessary in most advanced processes to ensure critical dimension and profile control. Specifically, the smaller the critical dimension then the higher the selectivity must be.

$$S = \frac{E_f}{E_r}$$

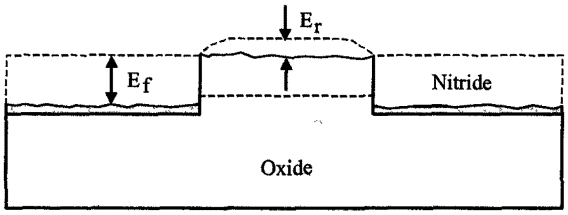


FIGURE 16.8 Etch Selectivity

The selectivity, S_R, for the film undergoing etch and the mask layer (e.g., photoresist) can be calculated from the following formula,

$$S_R = \frac{E_f}{E_r}$$

Where, E_f = the etch rate of the film undergoing etch
E_r = the etch rate of the masking layer (e.g., photoresist)

Based on this formula, selectivity is often expressed as a ratio. A process with poor selectivity may be 1:1 (meaning the film being etched is removed as quickly as the photoresist mask), whereas a good selectivity could be 100:1. Interpret this as the etched film is removed 100 times faster than the film not being etched (e.g., photoresist).

Dry etching frequently does not provide adequate etch selectivity to the layer underneath. In this case, a plasma reactor should be equipped with an endpoint detection system that signals when it is time to stop the etch process with minimal overetching. The endpoint detector notifies the etch equipment controller when the underlying film is beginning to be exposed in order to stop the etch process.

Uniformity

Etch uniformity is a measure of the capability of the process to etch evenly across the entire surface area of the wafer, across the entire wafer lot, and from lot to lot. Uniformity is closely related to selectivity, since nonuniformity results in additional overetch. Maintaining uniformity across the wafer surface is key to ensuring consistent manufacturing performance. The challenge is that etching must be uniform in different types of wafer surface pattern density, such as densely populated wafer areas, large open spaces, and within high-aspect ratio features. Some problems in uniformity occur because etch rates and profiles depend on feature size and pattern density.[1] The etch rate is slower in small openings, to the point that etching can actually stop in small geometries with high aspect ratios. For instance, silicon trenches with a high-aspect ratio opening etch slower than trenches with a small-aspect ratio opening (see Figure 16.9). This phenomenon is known as *aspect ratio dependent etching* (*ARDE*), also referred to as *microloading*. The objective is to minimize ARDE across the wafer surface in order to improve uniformity.

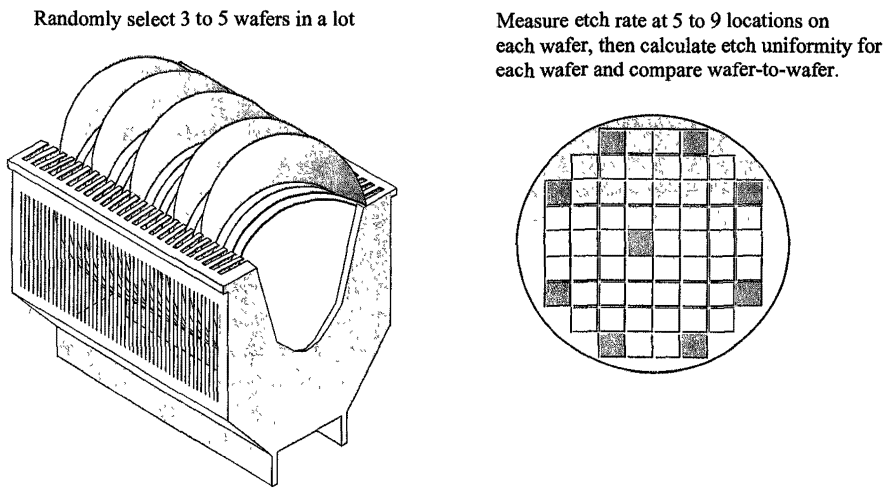


FIGURE 16.9 Etch Uniformity

Residues

Etch residue is the unwanted material remaining on the wafer surface after etch. It often coats the walls of the chamber and the bottom of the feature being etched. It can occur for reasons such as

contaminants in the etched film, improperly chosen etch chemistry (e.g., etching too fast), contaminants in the chamber, and nonuniform dopant distribution in the film. There are different names for the residues left after etch, including stringers, veils, crowns, and fences. Stringers are small residues of the etched material that are not totally removed, are electrically active, and can form an undesirable connecting short between features. Residues are a source of wafer contamination for IC fabrication and can cause problems during resist stripping. An overetch is sometimes done at the end of the etch process to remove residues. In some cases the etch residues can be removed by a resist strip process or by wet chemical etching.

Polymer Formation

A *polymer formation* is sometimes intentionally deposited on the sidewalls of the etch feature to form an etch-resistant film that prevents lateral etching (see Figure 16.10). This produces highly anisotropic features because it blocks the etching of the sidewall, thus increasing the etch directionality. The result is better control of critical dimensions of patterned structures. The polymers come from photoresist carbon converted into polymers during etching and combines with etching gases (i.e., C_2F_4) and etch by-products to form this sidewall polymer.[2] The need for sidewall polymers depends on the type of etching gas used.

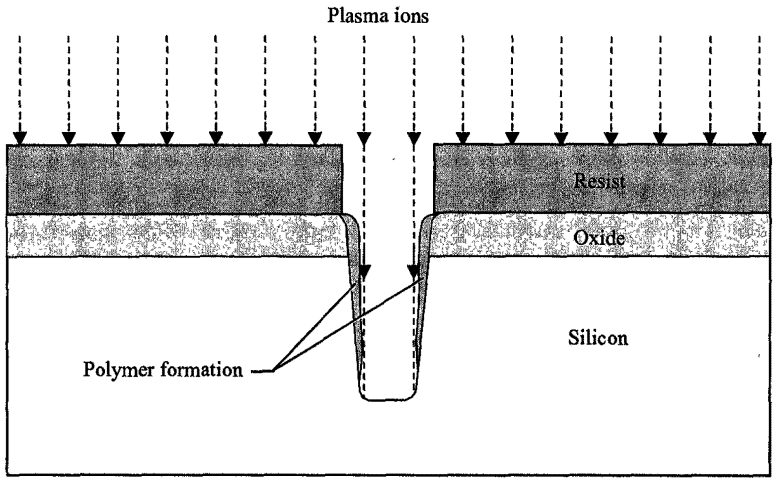


FIGURE 16.10 Polymer Sidewall Passivation for Increased Anisotropy

These sidewall polymers are complex, containing etchant elements and reaction by-products such as aluminum, titanium from barrier layers, oxides, and other inorganic materials. The polymer chains have strong carbon-fluorine bonds that are difficult to oxidize and remove.[3] However, the polymers must be removed after the etch process or device yield and reliability is affected. The cleaning of the sidewall often requires special gas chemistry for a plasma stripping process or possibly a wet clean using strong solvents followed by DI-water rinsing (see the following section).

Unfortunately, an undesirable side effect of polymer deposition is that the internal parts of the process chamber also become coated with polymer. Etch process chambers require periodic cleaning to remove the polymer and to replace parts that can not be cleaned.

Plasma-Induced Damage

Plasma consists of energized ions, electrons, and excited molecules, which can cause *plasma-induced damage* to sensitive devices on the wafer surface. A major type of damage is nonuniform plasma that creates trapped charges on the gate electrode of a transistor, causing a breakdown of the thin gate oxide.[4] Plasma becomes nonuniform due to poor equipment design or from operating the plasma reactor outside of the optimum process window. Another type of device damage is from energetic ion bombardment to gate oxide that is directly exposed to the ions. This damage could occur at the edge of a gate electrode during etching. Plasma damage is sometimes removed from the wafer through anneals or chemical wet etching.

Particle Contamination

Wafer damage from plasma can also come from particle contamination generated by the plasma near the wafer surface. Studies have shown that particles are trapped near the plasma/sheath interface because of the electrical potential difference.[5] When the plasma is turned off, these particles fall onto the wafer surface. Plasma based on fluorine gas chemistries produces fewer particles than chlorine or bromine gas chemistries because fluorine generates etch by-products with a higher vapor pressure. Control of particle contamination is done by an optimized tool design, proper tool operation and shutdown, and use of the appropriate gas chemistry for the film being etched.

DRY ETCH

Dry etch is the primary etching method used to remove surface material in semiconductor manufacturing. The goal of dry etch is to reproduce the image of a mask on the wafer surface with a high degree of integrity. The advantages to using dry etch over wet etch are listed in Table 16.2.

TABLE 16.2 Advantages of Dry Etch Over Wet Etch

Description of Advantages
1. Etch profile is anisotropic with excellent control of sidewall profiles.
2. Good CD control.
3. Minimal resist lifting or adhesion problems.
4. Good etch uniformity within wafer, from wafer-to-wafer, and from lot-to-lot.
5. Lower chemical costs for usage and disposal.

There are disadvantages to using dry etch. The primary disadvantages are poor selectivity to the underlying layer, risk for device damage from plasma, and expensive equipment.

In the dry etching process, a low-pressure plasma discharge is used to remove material in small feature sizes of integrated circuits (the creation of a plasma was discussed in Chapter 8). The plasma interacts with the wafer surface to cause etching action and the subsequent removal of the surface material. The major actions that occur for plasma etching of a substrate material are shown in Figure 16.11.[6]

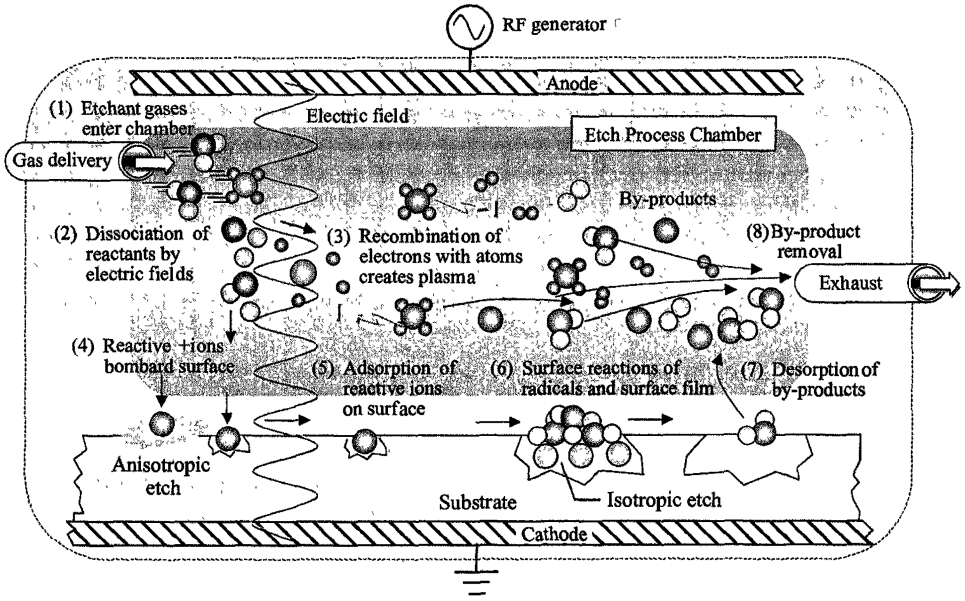


FIGURE 16.11 Plasma Etch Process of a Silicon Wafer

Etching Action

Etching action in dry etch systems is achieved by either a chemical or a physical technique or a combination chemical/physical technique (see Figure 16.12). In a purely *chemical mechanism,* the plasma creates reactive species (free radicals and reactive atoms) that chemically react with the materials on the wafer surface. The gases introduced into the chamber (typically containing chlorine and/or fluorine) are carefully selected to attain high selectivity (that is, to minimize the chemical reaction with the photoresist mask and underlying wafer layer). The chemical etching component of the plasma produces poor CD control because of its isotropic profile. Volatile by-products of the reaction are removed by the low-pressure pumping system.

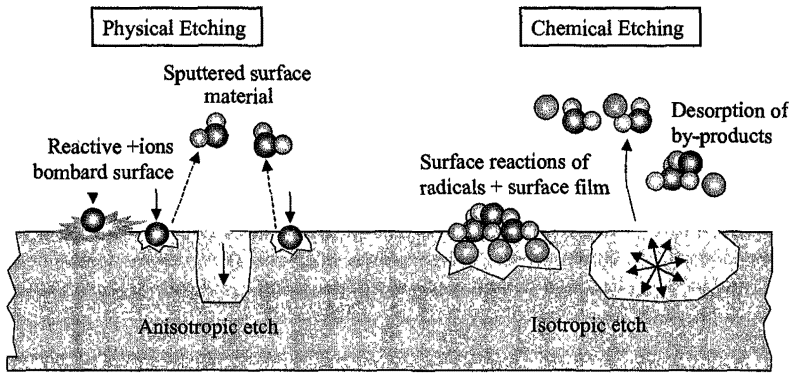


FIGURE 16.12 Chemical and Physical Dry Etch Mechanisms

To achieve etching action with a *physical mechanism,* the plasma provides energetic species (bombarding positive ions) that are accelerated toward the wafer surface by strong electric fields. The ions physically remove the unprotected wafer surface material by a sputter-etch action. Typically a nonreacting gas such as argon (Ar) is used. A benefit to this mechanical etching approach is the strong directionality of the etch, making it possible to achieve highly anisotropic profiles (near-vertical sidewalls) for good CD control. Sputter etching produces a high etch rate; however, it does have poor selectivity. Another problem is that the species removed by sputtering are not volatile and may redeposit back on the wafer, causing particulate and chemical contamination.

There is also a *combined physical and chemical mechanism* where ion bombardment improves the chemical etching action. The etch profile is varied from isotropic to anisotropic by adjusting the plasma conditions and gas composition. Combined physical and chemical etch produces good CD control with fair selectivity and is often preferred for most dry etch processes. Table 16.3 summarizes the different etch parameters for chemical, physical, and combined chemical/physical etching. The advantages from each type depend on the objectives of the etch process.

Note that dry etch systems may be designed to operate either as isotropic or anisotropic etchers depending on the direction of the RF electric field relative to the wafer surface. This means that positive ion sputtering can occur respectively on the wafer surface or on the edge of the wafer. If the field is perpendicular to the wafer surface, then the etching is done by a combination of heavy positive ion sputtering and some radical chemical reactions. If the field is parallel to the surface of the wafer, very little physical sputtering occurs, so the etching is done primarily by chemical reactions between radicals and the surface material.

Potential Distribution

The *plasma potential distribution* in the glow discharge region of a plasma has a strong effect on the etching capability of the system. This is because the amount of particle energy that bombards the etched surface depends on the electrical potential distribution. Figure 16.13 shows a reactor glow discharge between two electrodes. The power electrode has RF power applied, while the ground electrode is at ground potential. The potential of the plasma is positive relative to the

grounded electrode (which is also connected to the reactor walls, making them grounded as well). The plasma region has the most positive potential in the system.

TABLE 16.3 Chemical Versus Physical Dry Plasma Etching

Etch Parameter	Physical etch (RF field perpendicular to wafer surface)	Physical etch (RF field parallel to wafer surface)	Chemical etch	Combined Physical and Chemical
Etch Mechanism	Physical ion sputtering	Radicals in plasma reacting with wafer surface*	Radicals in liquid reacting with wafer surface	In dry etch, etching includes ion sputtering and radicals reacting with wafer surface
Sidewall Profile	Anisotropic	Isotropic	Isotropic	Isotropic to anisotropic
Selectivity	Poor/difficult to increase (1:1)	Fair/good (5:1 to 100:1)	Good/excellent (up to 500:1)	Fair/good (5:1 to 100:1)
Etch Rate	High	Moderate	Low	Moderate
CD Control	Fair/good	Poor	Poor to nonexistent	Good/excellent

*Used primarily for stripping and etchback operations.

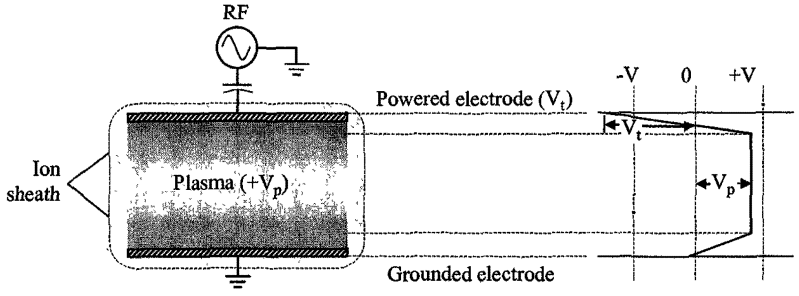


FIGURE 16.13 Schematic View of Reactor Glow Discharge with Potential Distribution

The powered electrode in an etch reactor develops a negative self-bias (DC self-bias or DC bias) voltage relative to ground because fast-moving electrons leave the plasma to strike the electrode. After a certain amount of negative charge, electrons are repelled from the electrode, thus creating the dark space (ion sheath) region with positive ionic charge. The magnitude of the powered electrode self-bias voltage depends on the amplitude and frequency of the RF voltage applied to the electrodes.[7] If the electrodes are of similar area, the potential difference across the dark space of each electrode will be the same. Since the powered electrode develops a negative self-bias, the plasma must assume a positive potential to produce a potential of equivalent magnitude at the grounded electrode. In essence, the plasma forms a compensating positive potential.

There are etch trends that are affected by parameters of the etch process. If the RF frequency is reduced, then ions efficiently cross the plasma dark space in a small fraction of an RF cycle. This action increases the ion energy and etch rate. The amount of ion bombardment depends on the size of the electrodes. For asymmetrical electrode size, if the area of the powered electrode is small, then the positive plasma potential is small. This condition results in a larger dark space potential at the powered electrode and a high-energy ion bombardment of the powered electrode surface.[8] Some basic trends for etching process parameters are provided in Table 16.4 on page 446.

TABLE 16.4 Effects of Changing Plasma Etch Parameters

Increase (↑) or Decrease (↓) in Etch Control Parameters		Ion Energy	DC Bias	Etch Rate	Selectivity	Physical Etch
RF Frequency	↑	↓	↓	↓	↑	↓
	↓	↑	↑	↑	↓	↑
RF Power	↑	↑	↑	↑	↓	↑
	↓	↓	↓	↓	↑	↓
DC Bias	↑	↑	↑	↑	↓	↑
	↓	↓	↓	↓	↑	↓
Electrode Size	↑	↓	↓	↓	↑	↓
	↓	↑	↑	↑	↓	↓

PLASMA ETCH REACTORS

The basic components of a plasma dry etch system include: a reaction chamber where the etching takes place, an RF power supply to ignite the plasma, a gas flow control system, and a vacuum system to remove etch by-products and gases. The etch system includes sensors, gas flow control units, and an endpoint detector. A wide range of gas chemistries is used in etch (see the following section), but in general, fluorine etches SiO_2; chlorine and fluorine etch aluminum; chlorine, fluorine, and bromine etch silicon; and oxygen removes photoresist. Different parameters controlled in dry plasma etching are: vacuum operation, gas mixture, gas flow rate, temperature, RF power, and the wafer position relative to the plasma. The interaction of these different parameters is a function of the dry etch process controller.

Prior to the 1980s, most plasma etch equipment used a barrel reactor designed for batch processing (many wafers processed simultaneously). This type of reactor is no longer common in advanced IC production and is only used in noncritical applications. The current trend in semiconductor manufacturing is for single-wafer processing in integrated cluster tools. This technique achieves manufacturing efficiency by reducing the batch size for single-piece flow. Integrated cluster tools also reduce exposure to contamination between process steps and achieve better wafer uniformity because the reactor parameters are optimized for one wafer. The most important development in dry etch systems for sub-0.25 μm geometries is the high-density plasma reactor.

The different types of dry plasma reactors are:

- Barrel plasma etcher
- Parallel plate (planar) reactor
- Downstream etch systems
- Triode planar reactor
- Ion beam milling
- Reactive ion etch (RIE)
- High-density plasma etchers

Barrel Plasma Etcher

The *barrel reactor* is a cylindrical design with almost pure chemical isotropic etching at a pressure of about 0.1 to 1 torr (see Figure 16.14). Wafers are mounted vertically in a quartz boat with a small separation between wafers. The RF power is applied by placing electrodes on both sides of the cylinder. There is typically a perforated metal cylindrical etch tunnel that confines the plasma to the outer region between the etch tunnel and chamber wall. The wafers are placed parallel to the electric field to minimize physical etching. The etchant species in the plasma diffuse to the etch tunnel, while the energetic ions and electrons of the plasma do not enter this region. The etching is almost purely chemical with isotropic etching and high selectivity.[9] There is minimal plasma-induced

damage because there is no physical sputtering on wafers. The barrel plasma reactor has been used primarily for stripping photoresist from wafers. Oxygen is the primary reactant for stripping photoresist.

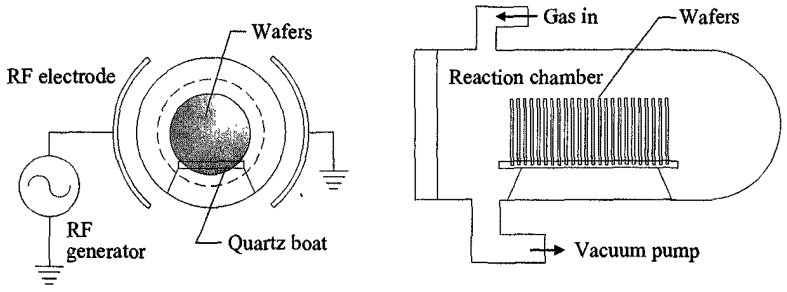


FIGURE 16.14 Typical Barrel Reactor Configuration

Parallel Plate (Planar) Reactor

The *parallel plate (planar) reactor* has two parallel plates that are symmetrical in size and position in the reactor (see Figure 16.15). A wafer can be placed backside down on the grounded electrode cathode with the RF signal applied to the upper electrode. This is the plasma etch mode, with energetic ion bombardment since the plasma potential is always above ground potential. If a wafer is placed directly on the RF-powered electrode, the wafer is in direct contact with the plasma and energetic ions. This contact can result in high-energy ion bombardment and is said to be in the reactive ion etch mode. Physical and chemical etch mechanisms occur in both the plasma etch mode and the reactive ion etch mode. However, energies of the bombarding ions are about ten times higher in the reactive ion etch mode.[10] A reactive gas is needed to form the plasma, such as fluorine (F_2) or oxygen (O_2). The reactor operates at a pressure of about 0.1 to 1 torr, with high RF power to control the etch rate. The planar etcher was one of the early reactors. Single-wafer parallel plate etchers are commonly used today.

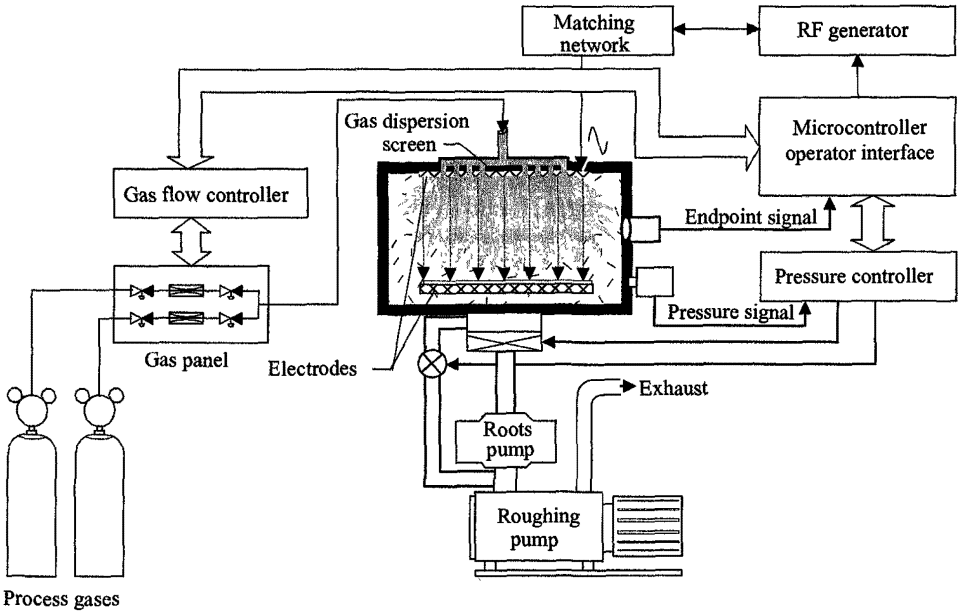


FIGURE 16.15 Parallel Plate Plasma Etching

Downstream Etch Systems

Repeated exposure to ion bombardment at the wafer surface increases the probability of device damage. A means of reducing damage to the wafer surface as well as heat buildup due to ion bombardment is to locate the wafer etch region away from the plasma in a *downstream reactor.* The plasma is formed in a separate source at a pressure of about 0.1 to 1 torr, transferred to the process chamber, and uniformly distributed over the heated wafer surface (see Figure 16.16). Since there are no ions to create directional etching, downstream reactors employ chemical etching, are isotropic, and are often used to remove resists or other noncritical layers (see the following section). A microwave source (2.45 GHz) for exciting the plasma for downstream etching is common because it produces the maximum concentration of atomic oxygen and the lowest concentration of ionic oxygen, which minimizes device damage and yields a high strip rate.

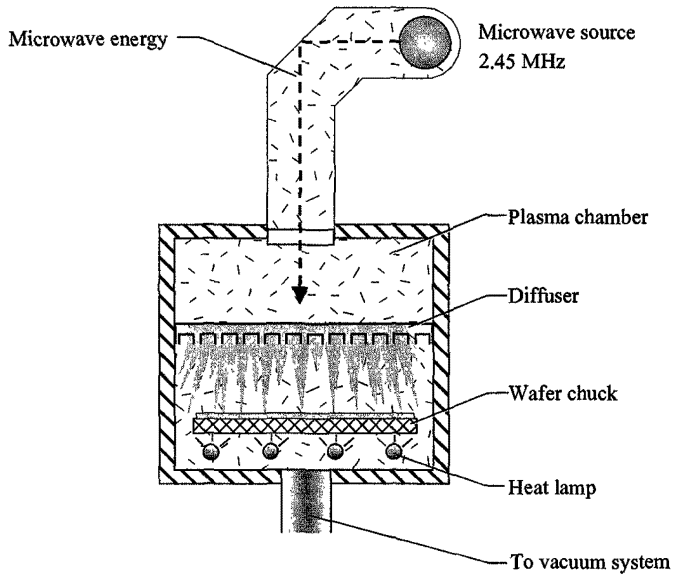


FIGURE 16.16 Schematic of a Downstream Reactor

There are variations of the downstream etching concept used with different etch systems discussed in the following section. The objective is to minimize wafer exposure to plasma ions in order to reduce or eliminate plasma-induced damage.

Triode Planar Reactor

The *triode planar reactor* adds a third electrode to attain control over the amount of ion bombardment. Figure 16.17 shows a setup with two power supplies. The inductively-coupled RF generates the plasma to create the ions and reactive species at a pressure of about 10^{-3} torr. The low-frequency generator controls the ion bombardment. A typical use is in single-crystal silicon trench etching.

Ion Beam Milling

Ion beam milling, also called *ion beam etching* (*IBE*), has a physical etch mechanism with a strongly directional plasma. It is capable of anisotropic etching of small features. The plasma is commonly generated using an RF inductively-coupled source or a microwave source. Fast-moving electrons are emitted by a hot filament. Argon atoms enter the plasma chamber through a diffuser screen. An electromagnet surrounds the plasma chamber. The magnetic field causes electrons to travel in circular paths. This cyclical motion produces a high number of collisions with argon atoms, which results in a high number of positive argon ions. Positive argon ions are drawn out of the plasma source with grid electrodes and formed into a high-density beam using a set of collimated electrodes (see Figure 16.18). A high-voltage accelerator grid boosts ion energy as high as 2.5 keV.

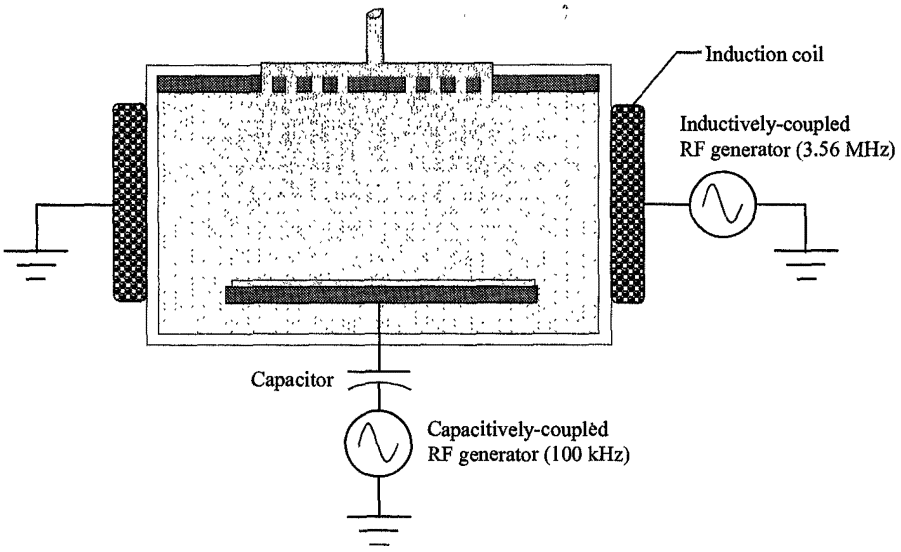


FIGURE 16.17 Triode Planar Reactor

A neutralizing filament emits electrons to recombine with argon atoms to prevent charging of the wafer with the positive ions. Ion beam etchers operate with argon (Ar) gas in the low-pressure range of 10^{-4} torr, which is lower than that commonly used for high-density plasma etching. Ion beam etching is used to etch difficult materials, such as gold, platinum, and copper.[11] The wafer can be tilted to produce variable sidewall geometries. The major problems inhibiting widespread use of ion beam etchers in semiconductor processing are low selectivity (usually below 3:1) and low etch rates, which lead to low wafer throughput.

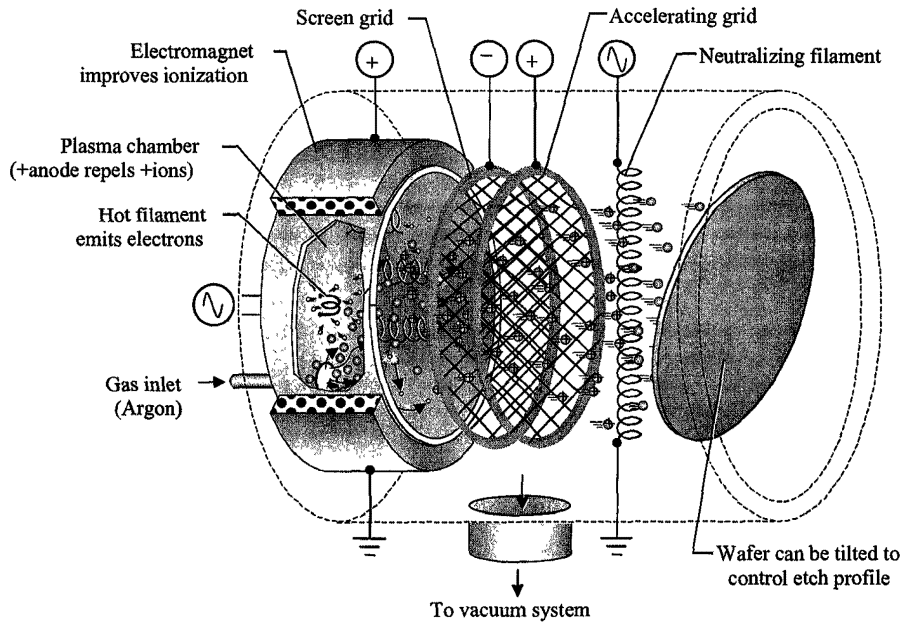


FIGURE 16.18 General Schematic of Ion Beam Etcher
Redrawn from *Advanced Semiconductor Fabrication Handbook,* Integrated Circuit Engineering Corp., pp. 8–12.

Reactive Ion Etch (RIE)

Reactive ion etch (RIE) is a technique for removing material from the wafer surface with both a reactive chemical process and a physical process using ion bombardment. RIE is similar to the standard parallel-plate plasma etcher, except the wafers are placed on the RF-powered electrode (cathode) and the powered electrode size is greatly reduced relative to the grounded electrode size (see Figure 16.19). In this manner a DC self-bias develops on the cathode and the wafers acquire a large voltage difference with respect to the plasma. This condition creates directionality for the ionized species moving toward the wafer, creating improved anisotropic sidewalls for features. There is no sputtering on the anode. The pressure is relatively low at <0.1 torr.

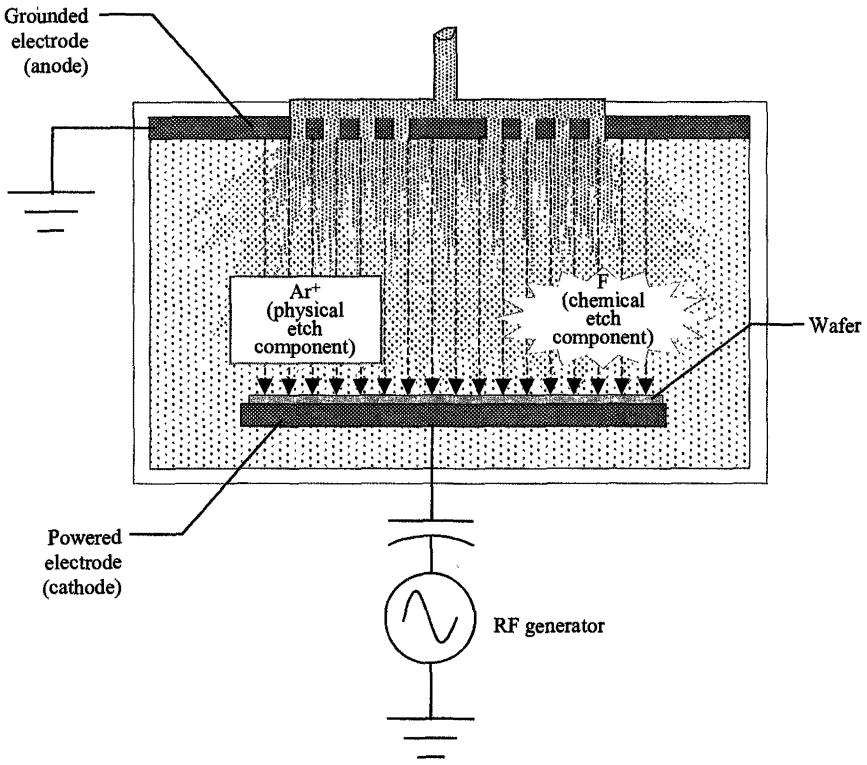
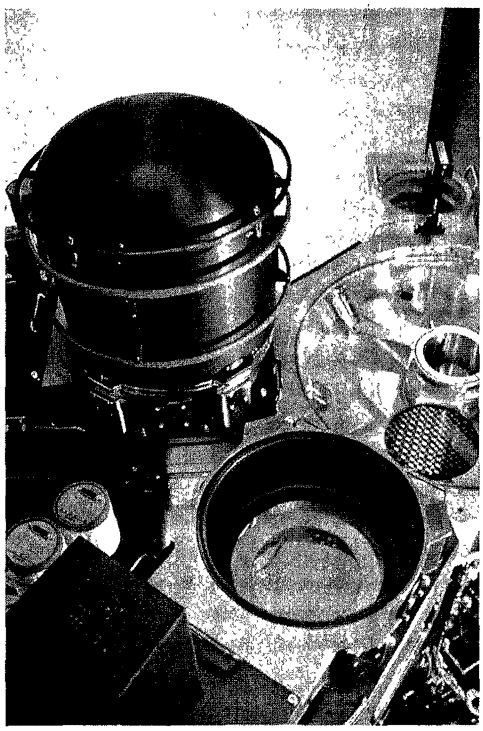


FIGURE 16.19 Parallel-Plate RIE Reactor

High-Density Plasma Etchers

The most predominant dry etching methodology in use for critical layers of advanced ICs is *high-density plasma etch* with single-wafer processing in a cluster tool.[12] Standard plasma systems previously used in wafer fabrication operated in a vacuum regime of a few hundred mtorr, where it is relatively straightforward to create a plasma (such as by applying an RF signal across two parallel plates). However, for 0.25-μm geometries and below, it has become too difficult to get etchant ions into and etch by-products out of high-aspect ratio features. The etching action slows down and will actually stop altogether at the bottom and lower sides of the feature profile.

The solution is to lower the system pressure to about 1 to 10 mtorr to increase the mean free path lengths of gas molecules and ions. This condition effectively reduces collisions that cause loss of profile control. However, a drawback to reduced pressure is the lower etch rate due to the rapid reduction in ion density as pressure decreases. To overcome this concern, a high-density plasma is needed to generate enough ions for an acceptable etch rate with a lower pressure. High-density refers to the number of active species in the plasma relative to conventional plasma at the same process pressure. In conventional plasma, the degree of ionization is typically on the order of 0.01% to 0.1%. High-density plasma more efficiently couples input power with the plasma, resulting in greater dissociation of etch species to achieve a degree of ionization as high as 10%. This technique yields highly directional, low-energy ions that produce anisotropic etching in high aspect ratio openings.



High-Density Plasma Etcher
(Photo courtesy of Applied Materials, Inc.)

High-density plasma etchers generally immerse the plasma in a magnetic field. The reasons for using a magnetic field during plasma etch are: (1) plasma generation is more efficient for creating highly-directional, low-energy ions entering high-aspect ratio openings, yet causes less wafer damage; (2) plasma is denser, with more reactive species and charged particles that increases the etch rate; and (3) the DC bias on the wafer can be reduced, which leads to less wafer bombardment (or damage).

Electron Cyclotron Resonance (ECR) ■ The *electron cyclotron resonance* (*ECR*) reactor was one of the earliest high-density plasma reactors to be developed commercially, first introduced in the early 1980s. It is still used in today's modern wafer fabs for etching 0.25-μm feature sizes and below. The ECR reactor produces very dense plasmas at operating pressures of about 1 to 10 mtorr. ECR etching uses microwave excitation (2.45 GHz) in the presence of a magnetic field to generate high-density plasma (see Figure 16.20 on page 452). A key feature of the ECR reactor is a magnetic field parallel to the direction of reactant flow that causes free electrons to move in a spiral path due to the magnetic force. An efficient transfer of energy occurs from the electric field to the plasma electrons when the electron orbit frequency (known as electron cyclotron resonance) equals the frequency of the applied electric microwave field. This resonance condition increases the probability of electron collisions, which generates a very dense plasma to create a large flux of ions. The reactive ions move toward the wafer surface and react with the surface layer to cause etching.

A low-power RF bias (13.56 MHz) or DC bias can be applied to the electrode holding the wafer to control the energy of the ions striking the surface. This action permits the ECR to operate as a combined chemical and physical etch process and produces an anisotropic etch profile. The main drawback to the ECR reactor for semiconductor manufacturing is its equipment complexity.[13] A variation of the ECR is a system with pairs of magnets and microwave antennas distributed around a central reactor, known as distributed ECR (DECR).

Inductively-Coupled Plasma (ICP) ■ Another high-density, low-pressure etch reactor that has plasma decoupled from the wafer is the *inductively-coupled plasma* (*ICP*) reactor. This reactor is less complicated and less expensive than the ECR and widely used in the United States. The ICP generates plasma by means of a spiral coil separated from the plasma by a dielectric plate or quartz tube (see Figure 16.21 on page 452).[14] The wafer is located away from the coil so it is not affected

by its electromagnetic field. The wafer can be biased to have both chemical and physical etching. This reactor can achieve anisotropic sidewall profiles in high-aspect ratio openings.

Another inductively-coupled reactor that generates a high-density plasma is the *helicon wave.* This system receives power from an RF signal (13.56 MHz) that is inductively coupled into the plasma from a double-loop antenna located outside a quartz source tube.

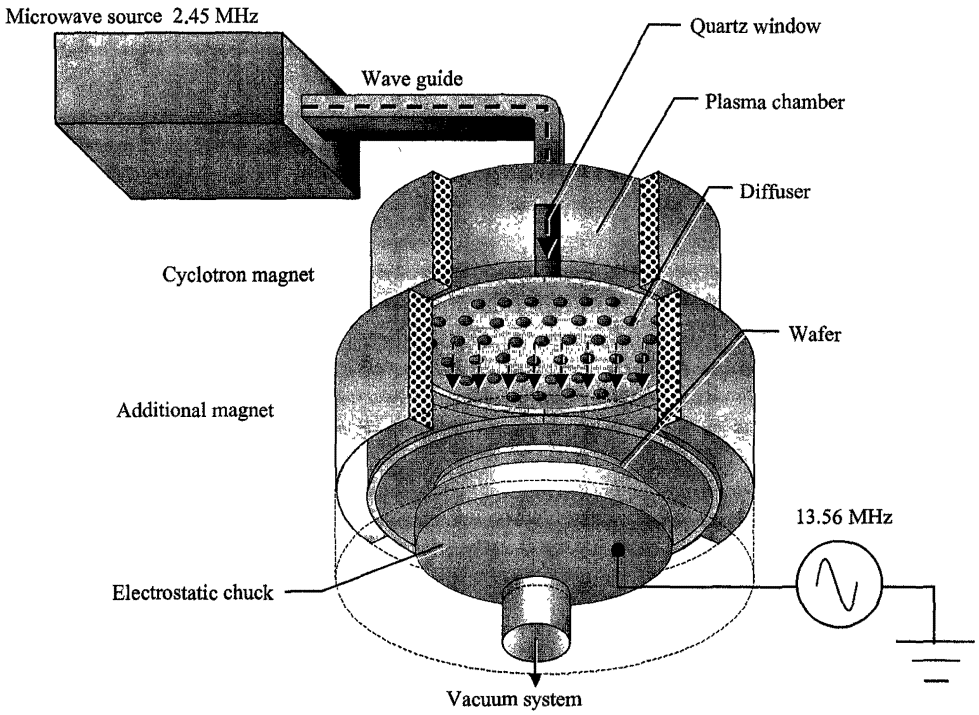


FIGURE 16.20 Schematic of Electron Cyclotron Reactor
Redrawn from Y. Lii, "Etching," *ULSI Technology,* ed. by C. Chang and S. Sze (New York: McGraw-Hill, 1996), p. 349.

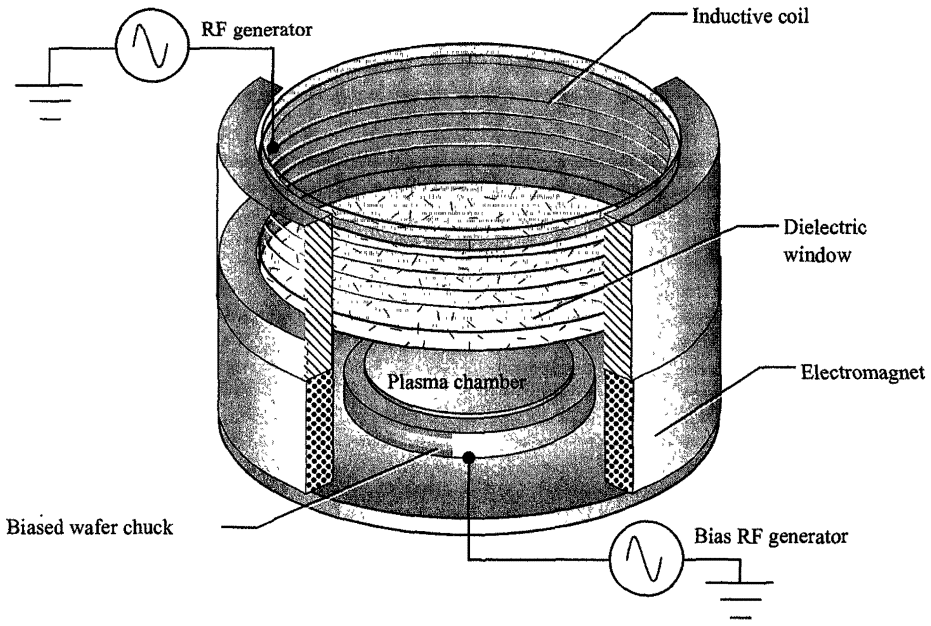


FIGURE 16.21 Inductively-Coupled Plasma Etch
Redrawn from Y. Lii, "Etching," *ULSI Technology,* ed. by C. Chang and S. Sze (New York: McGraw-Hill, 1996), p. 351.

Dual Plasma Source (DPS) ■ Figure 16.22 is a schematic of a *dual plasma source* (*DPS*) etch chamber (also referred to as decoupled plasma source). It has four major components: a source power unit, an upper chamber, a lower chamber with the wafer, and a movable electrode.[15] As with the previous high-density plasma systems, there are two sources of RF power used. The source power unit has an inductive coil for transferring RF power to the plasma in order to generate the reactive ions and neutral species. This is referred to as the source power. The source power unit has a temperature control system. RF power is also supplied to the wafer electrode to bias the wafer substrate and is referred to as the bias power. The wafer cathode is movable in the vertical direction. Only the upper chamber is exposed to the plasma and process gases, which keeps the lower chamber clean and makes it much easier to maintain.

A key aspect of the DPS plasma is the decoupling of the source plasma power from the bias power. This arrangement permits greater control over the ion density and ion energy, which results in a larger process window for physical and chemical etching. The result is improved critical dimension control and less etch residue.

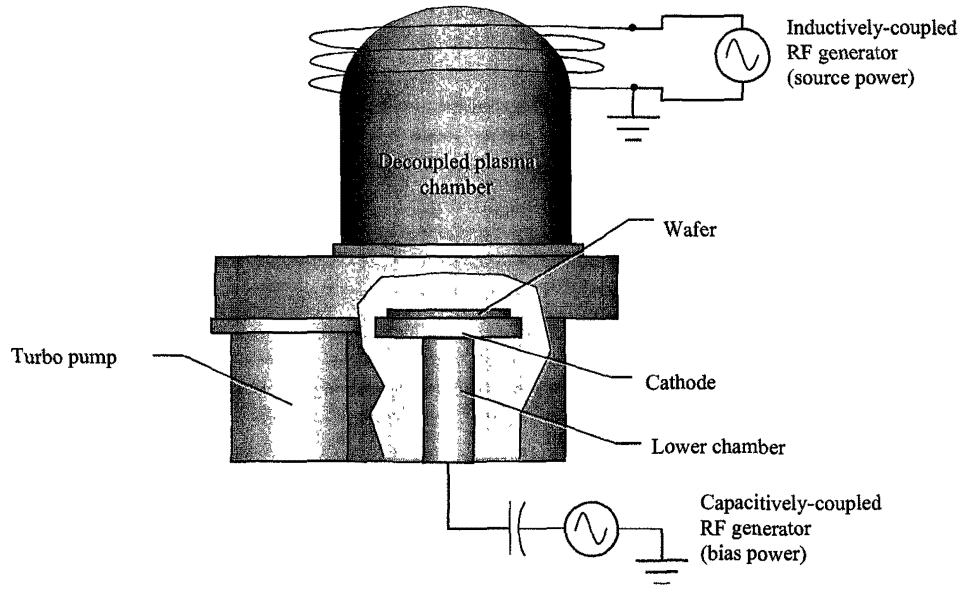


FIGURE 16.22 Dual Plasma Source (DPS)
Redrawn from Y. Ye et al., *Proceedings of Plasma Processing XI*, Vol. 96-12, ed. G. Mathod and M. Meyyoppan (Pennington, NJ: The Electromechanical Society, 1996): p. 222.

Magnetically Enhanced RIE (MERIE) ■ The *magnetically enhanced RIE* (*MERIE*) reactor (also referred to as a *magnetron*) is a combined physical and chemical etch system. It is similar to the RIE reactor except that now there is a magnetic field that holds the plasma away from the chamber walls and increases the electron and ion concentration near the wafer to create a high-density plasma (see Figure 16.23 on page 454). The magnetic field can be rotated electrically by its three-phase AC power supply or physically rotated in a dipole ring magnet system. Confining the plasma with the magnetic field creates a high-density plasma and permits lower pressure, effectively maintaining etch directionality and uniformity, especially when etching high-aspect ratio features.

Etch System Review

Shrinking feature sizes and the introduction of new wafer materials place stringent demands on etch performance. Dry etch systems use physical or chemical or a combination of these two mechanisms to etch material. Some equipment is anisotropic while other equipment is purely isotropic. One can appreciate the wide variety of etch equipment that is available for wafer manufacturing. The capability and control of a particular etch system is critical for successful wafer fabrication. Table 16.5 on page 454 summarizes the important characteristics for each equipment system.

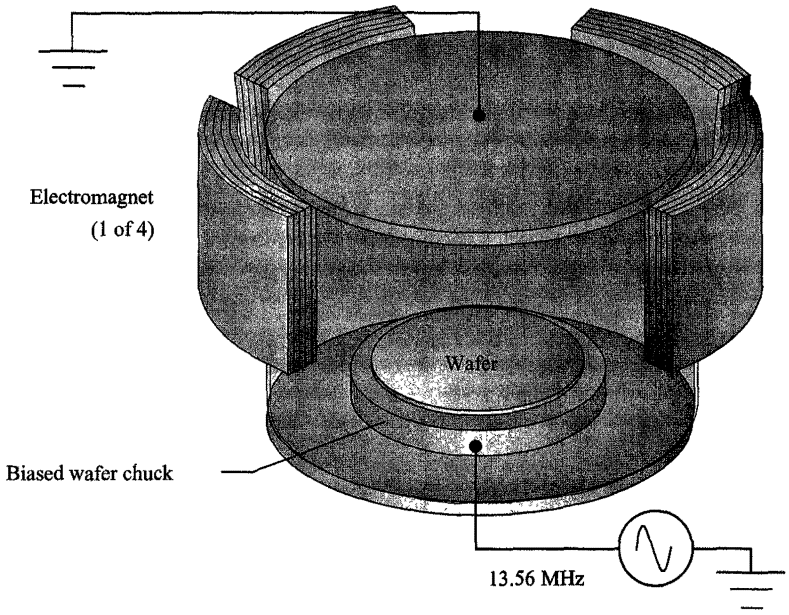


FIGURE 16.23 Magnetically Enhanced Reactive Ion Etch (MERIE)
Redrawn from *Wet/Dry Etch* (College Station, TX: Texas Engineering Extension Service, 1996), p. 165.

TABLE 16.5 Dry Etcher Configurations

Configuration	Etch Mechanism	Pressure (Torr)	Arrangement	High-Density Plasma	Biasing	Bias Source	Profile
Barrel	Chemical	10^{-1} to 1	Coil or electrodes outside vessel	No	In cassette (bulk)	RF	Isotropic
Parallel Plate (Planar)	Physical and Chemical	10^{-1} to 1	Planar diode (two electrodes)	No	On powered electrode (anode or grounded electrode)	RF	Anisotropic and isotropic
Downstream Plasma	Chemical	10^{-1} to 1	Coil or electrodes outside vessel	No	In cassette (bulk) downstream of plasma	RF or Microwave	Isotropic
Triode Planar	Physical	10^{-3}	Triode (three electrodes)	No	On powered electrode		Anisotropic
Ion Beam Milling	Physical and Chemical	10^{-4}	Planar triode	No	On powered electrode (anode)		Anisotropic
Reactive Ion Etch (RIE)	Physical	<0.1	Planar or cylindrical diode	No	On cathode		Anisotropic
Electron Cyclotron Resonance (ECR)	Physical	10^{-4} to 10^{-3} (low)	Magnetic field in parallel with plasma flow	Yes	On cathode	RF or DC	Anisotropic
Distributed ECR	Physical	(low)	Magnets distributed around central plasma	Yes	On cathode	RF or DC	Anisotropic

Configuration	Etch Mechanism	Pressure (Torr)	Arrangement	High-Density Plasma	Biasing	Bias Source	Profile
Inductively-Coupled Plasma (ICP)	Physical	(low)	Spiral coil separated from plasma by dielectric plate	Yes	On cathode	RF or DC	Anisotropic
Dual Plasma Source	Physical	(low)	Independent plasma and wafer biasing	Yes	On cathode	RF or DC	Anisotropic
Magnetically Enhanced RIE (MERIE)	Physical	(low)	Planar diode with magnetic field confining plasma	Yes	On cathode	RF or DC	Anisotropic

Endpoint Detection

Dry etch differs from wet etch in that it usually does not have good etch selectivity to the underlying layer. For this reason, a form of *endpoint detection* is required to monitor the etch process and stop etching to minimize overetching of the underlying layer. Endpoint detection systems measure different parameters, such as a change in the etch rate, the types of etch products removed from the etch process, or a change in the active reactants in the gas discharge (see Figure 16.24). A method used for endpoint detection is optical emission spectroscopy. This measurement tool is integrated into the etch chamber for real-time monitoring of the etch process.

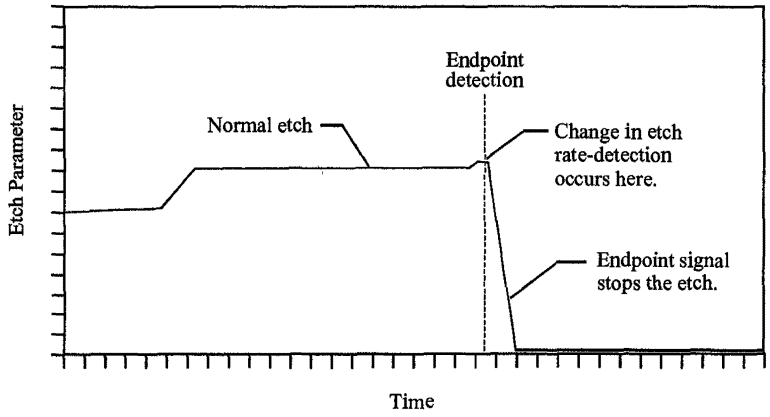


FIGURE 16.24 Endpoint Detection for Plasma Etching

Optical Emission Spectroscopy ■ An excited species emits light at a wavelength that corresponds to a specific material (see Table 16.6 on page 456).[16] The light emitted by excited atoms and molecules in a gas discharge can be analyzed with optical emission spectroscopy to identify the element. The emitted light is passed through a detector with a filter to let light of a specific wavelength pass through that is used to identify the etched materials. The emission intensity is directly related to the relative concentration of a species in a plasma. In this manner the endpoint detector can determine when the etch process has removed the desired material and proceeded into the underlying layer. Optical emission spectroscopy is the most common method for etch endpoint detection because it is easy to implement with high sensitivity.[17]

Optical emission can also be used to perform etch reactor diagnostics. If a system has leaks to the atmosphere, the presence of nitrogen is identified. Water moisture can be detected, which could be caused by inadequate vacuum pumpdown after chamber cleans. Absolute concentrations of species can not be obtained by optical emission spectroscopy.

TABLE 16.6 Characteristic Wavelengths of Excited Species in Plasma Etch

Material	Emitting Species of Etchant Gas	Some Products	Wavelength (nm)
Silicon	CF_4/O_2	SiF	440; 777
	Cl_2	SiCl	287
SiO_2	CHF_3	CO	484
Aluminum	Cl_2	Al	391; 394; 396
	BCl_3	AlCl	261
Photoresist	O_2	CO	484
		OH	309
		H	656
Nitrogen	N_2 (used as a purge gas prior to and after etch)	N_2	337
		NO	248

Vacuum for Etch Chambers

The vacuum system in an etch process is critical because it affects plasma parameters associated with gas flow and pressure. A typical high-density plasma vacuum system for etch will achieve a chamber pressure in the 1 mtorr range or less with gas flows as high as 800 sccm at the wafer surface. The vacuum components must be capable of handling the corrosive by-products produced during etching. The pumps used for an etch process are typically a turbopump, a roots-type blower and a dry backing pump. Typically the turbopump is located close to the chamber to maximize the pump speed at the wafer surface, while the other pumps are located in a service bay or sub fab area.[18] Additional dry pumps are used to evacuate the loadlock and transfer chamber of an integrated cluster tool.

The fluorine, chlorine, and bromine gas chemistries used in etch (see the following section) are effective at removing the wafer surface films because of their reactivity. Unused reactants as well as reaction by-products are removed at a high rate. The high reactivity of etch by-products creates corrosion problems for vacuum system components, requiring special designs such as nitrogen purge of bearings and magnetically levitated (maglev) pumps that only rely on bearings during start-up and shutdown.[19]

DRY ETCH APPLICATIONS

There are many different types of plasma dry etching applications needed to fabricate integrated circuits. These applications are found in all materials used in the fab. For our purposes, we will review dry etch by the type of material to be etched: dielectric, silicon, and metal. The move to smaller critical dimensions, higher aspect ratio openings, and new materials in wafer fabrication creates challenges in etch processing for all three material types. Optimizing etch conditions leads to competing objectives for the production team. In general, the requirements for successful dry etch are:

1. High selectivity to avoid etching materials that are not to be etched (primarily photoresist and underlying materials).
2. Fast etch rate to achieve an acceptable throughput of wafers.
3. Good sidewall profile control.
4. Good etch uniformity across the wafer.
5. Low device damage.
6. Wide process latitude for manufacturing.

Critical etch parameters are determined through optimization activities for each specific dry etch application. Some of these parameters are shown in Figure 16.25. Note that in many cases optimization is being done through process equipment modeling using computer software. This is due to the high cost of conducting prototype hardware testing with actual wafers.

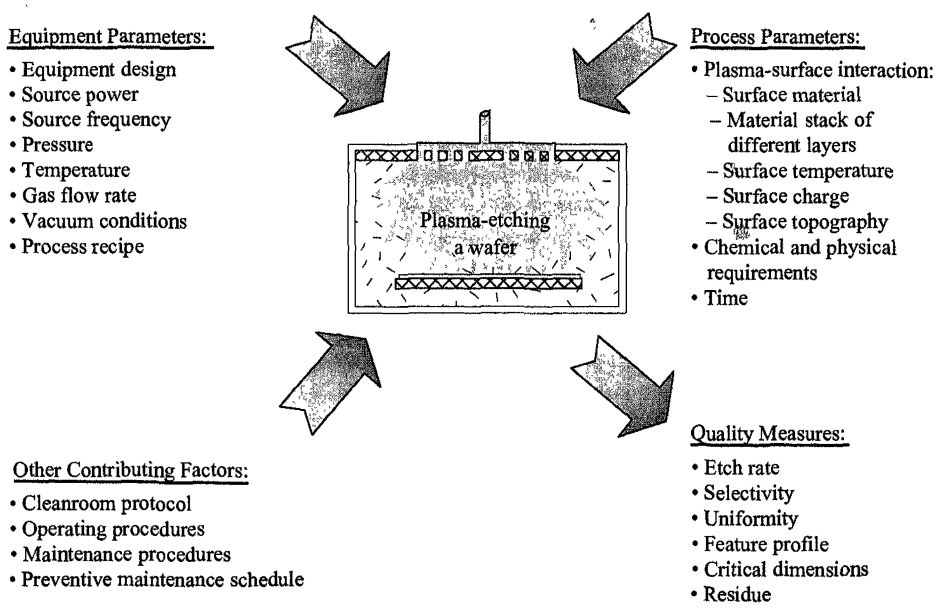


FIGURE 16.25 Dry Etch Critical Parameters

Table F.1 in Appendix F lists the typical gas chemistries used for plasma etching. Dielectric and silicon materials are usually etched with fluorine-based gas etchants such as CF_4. Aluminum etching is typically done with chlorine-based gas chemistries such as BCl_3.

Dielectric Dry Etch

Dielectric dry etch is the most complicated etch process for 200 mm wafers and will remain the biggest etch challenge for 300 mm wafers.[20] The challenges for oxide etching are tighter process specifications because of shrinking feature sizes, new trench etch processes for interlayer dielectrics (ILD) used in the dual-damascene approach for copper metallization, and the need to etch new ILD low-k materials.

Oxide ■ Common reasons for etching oxide are for forming contact holes and vias. These features are critical applications, with requirements such as etching high-aspect ratio openings in the oxide. Aspect ratios for DRAM applications are expected to be at 6:1 for 0.18 μm feature sizes. The required selectivity to underlying silicon and polycide is about 50:1.[21] There are new oxide etch applications such as the dual-damascene structure, with new trench requirements and high-aspect ratio etch. There are also noncritical oxide etch applications such as a low-aspect ratio via etch.

The oxide plasma etching process is commonly based on fluorocarbon chemistry. Fluorocarbon is a fluorinated hydrocarbon. It has one or more of the hydrogen atoms in a hydrocarbon molecule replaced by fluorine (F). In this manner, many gases are sources of fluorine, such as CF_4, C_3F_8, C_4F_8, CHF_3, NF_3, and SiF_4. Common gases are tetrafluoromethane (CF_4), which has a high etch rate but poor selectivity with polysilicon, and trifluoromethane (CHF_3), which has a high rate of polymer formation. Fluorocarbon gases are chemically stable in their ground state (nonplasma state) and will not attack silicon or its oxide because their bonds are stronger than SiF bonds. There are also buffer gases such as Ar and He added to the etch chemistry. Argon has a relatively high mass that is used for physical etching (sputtering). Helium has a low mass and is used to diminish the etchant gas concentration (referred to as a diluent) to enhance plasma uniformity.

The desired fluorocarbon feed gas, which may have a primary gas component such as CF_4, is fed into the plasma and dissociates (see Figure 16.26 on page 458). This reaction forms many different types of reactive ions (radicals) and neutrals.[22] Examples of reactive species are CF_4, CF_2, CHF, HF, and F. It is the radical F species that attacks the oxide and causes etching. The F reactive ions easily form volatile by-products, which are then pumped out of the etch reactor by the vacuum system. The CF_x radicals also serve to passivate the sidewall surfaces with a polymer. A higher carbon-to-fluorine ratio generally means more polymer formation, lower etch rate, and higher oxide-to-silicon

selectivity. In some cases, a silicon source is used above the plasma to getter excess fluorine atoms, thereby increasing the ratio of carbon to fluorine.

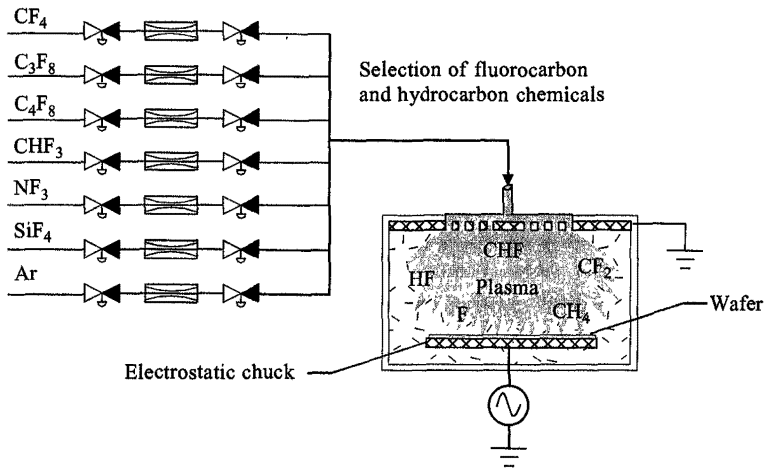


FIGURE 16.26 Oxide Etch Reactor

Underlying Material Selectivity. One of the major challenges for oxide etching is obtaining high selectivity to the underlying material, usually silicon, nitride, or an antireflective coating. For example, high selectivity to silicon is critical during contact etch through the LI oxide dielectric to avoid etching into the source/drain region. High selectivity to silicon is required when etching oxide sidewall spacers on the gate structure (see Chapter 9). For via etch, high selectivity to TiN, W, or Al is a requirement.

One method of achieving selectivity to silicon is by adding oxygen to the gas chemistry to control the selectivity between oxide and silicon. Small concentrations of O_2 improve the etch rate of both oxide and silicon. At greater concentrations of up to about 20% O_2, there is more rapid etching of oxide over silicon, improving the selectivity to minimize etching of the underlying silicon. Another way to improve selectivity is to add hydrogen to the gas mixture as the etch rate of silicon decreases until it reaches almost zero for a H_2 volume of about 40%. At the same time, the oxide etch rate is not affected by H_2 at concentrations below 40%.[23]

Selectivity during oxide etch can be maintained to the underlying material by use of a hard "etch stop" masking layer of silicon nitride, as with etching the contact hole (see Figure 16.27). This action requires good oxide etch selectivity to the nitride layer. A hard mask approach to selectivity adds processing steps and is done only when necessary.

Example: Silicon nitride, SiN_3, serves as etch-stop during LI oxide etch
Note: The numbers show the order of the five operations.

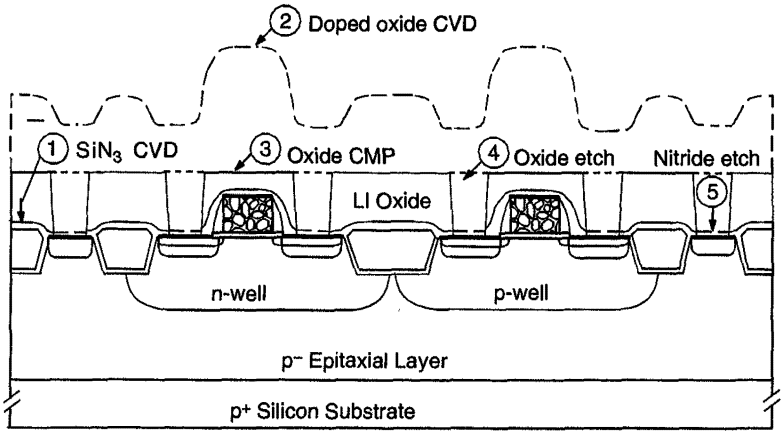


FIGURE 16.27 Etch Stop Hard Mask Layer

Oxide/silicon selectivity is also achieved by forming a passivating polymer layer on top of the silicon as part of the etch process. The polymer residue is introduced into the gas chemistry to inhibit lateral silicon etching. The polymer tends to form more easily on silicon rather than SiO_2, which is thought to occur because the carbon combines with the oxygen from the SiO_2 to form volatile CO or CO_2, which is then pumped away.[24] This approach to selectivity permits continued etching of the oxide while inhibiting the silicon etch. Unfortunately the polymer also deposits on the chamber surfaces during etch and becomes a source of particulate contamination, requiring frequent cleaning of the etch system.

Photoresist Selectivity. Achieving high selectivity to photoresist during oxide etch is important for avoiding tapered sidewalls. The photoresist defines the pattern that is being etched. In the case of contacts and vias, millions of holes are being etched simultaneously, each requiring the removal of a precise amount of surface material, often at different depths (see Figure 16.28). One factor that reduces photoresist selectivity (an undesirable situation) is the effective formation of aggressive fluorine atoms in a high-density plasma. Free fluorine will etch the organic photoresist. This lowers selectivity from about 10:1 from conventional plasma etchers to a range of 4:1 to 7:1 in the high-density plasma tools.[25] In addition, the need to etch through antireflective coating layers, which lengthens the etch time, further reduces the resist thickness. In general, deep UV resists are less resistant than i-line resists to plasma processing, which also lowers resist selectivity.

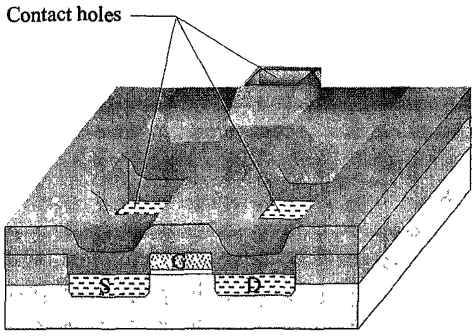


FIGURE 16.28 Contact Etching to Varying Depths

Sidewall Profile. Contact windows in the local interconnect (LI) oxide dielectric layer generally have dimensions equivalent to the smallest feature size with a high-aspect ratio. For this type of application, a high degree of anisotropy with a vertical sidewall profile is needed. The most significant factor is the highly directional ion bombardment of high-density plasma. A factor in obtaining optimum sidewall profile is the amount of resist selectivity. Low resist selectivity can lead to tapered sidewalls in an anisotropic etch process because of gradual photoresist erosion during the etch process.

Silicon Nitride ■ There are two basic types of silicon nitride used in wafer fabrication. One type is deposited with LPCVD at 700° to 800°C, which produces a stoichiometric compound of Si_3N_4 film. The other nitride film is deposited by plasma-enhanced CVD at <350°C that produces a film having lower density.[26] The etch rate is faster for the PECVD film because of its lower density.

Silicon nitride is etched by different gas chemistries. A common primary gas is carbon tetrafluoride (CF_4) that is mixed with O_2 and N_2. Increasing the amount of O_2/N_2 dilutes the concentration of fluorine species and lowers the etch rate of any underlying oxide. A high etch rate of 1200 Å/min and a high selectivity to oxide would be about 20:1 for a nitride film deposited with LPCVD.[27] Selectivity to oxide is important in an application with a thin pad oxide used as an etch-stop, requiring the etch process to quickly slow down when oxide is reached. Other possible primary gases used for nitride etch are SiF_4, NF_3, CHF_3, and C_2F_6.

Silicon Dry Etch

Plasma dry etch of silicon is a critical process in wafer fabrication. The two major layers for plasma etching are (1) polysilicon gate length formation for the MOS gate structure, and (2) single-crystal

silicon trench creation used for either device isolation or capacitor structures in dynamic random-access memories (DRAM).

Polysilicon etch gas chemistries have traditionally been fluorine-based gases, including CF_4, CF_4/O_2, SF_6, C_2F_6/O_2, and NF_3. The fluorine atoms produce a very fast etch reaction but with an isotropic profile and average resist selectivity. The sidewall profile is improved by reducing the fluorine atoms and increasing the ion energy, but this also reduces the poly/oxide selectivity. The energy of the bombarding ions must be low enough to avoid sputtering away an underlying oxide layer.

To overcome these difficulties, polysilicon plasma etch gases are often based on chlorine, bromine, or chlorine/bromine chemistries. Chlorine (Cl_2) produces an anisotropic silicon sidewall profile with good oxide selectivity (>10 selectivity for poly/oxide and poly/nitride). Bromine gas chemistry, as either Br_2 or HBr, etches silicon anisotropically with very high selectivity (>100) to oxide and nitride. This quality is important for applications such as poly gate etching over the gate oxide.[28] Bromine gas chemistry also has better selectivity to photoresist than Cl_2. Another silicon etch chemistry is a blend of chlorine and bromine, such as HBr and Cl_2 with the addition of O_2. Adding O_2 increases the etch rate and the selectivity to oxide. Polymers form during etching with chlorine, and fluorine gas chemistries to deposit on sidewalls and contribute to sidewall profile control. SiF_4, $SiCl_4$, and $SiBr_4$ are some volatile etch by-products for fluorine, chlorine, and bromine gas chemistries.

Poly Gate Etch ■ In MOS devices, doped LPCVD polysilicon is used as the gate conductor material. The linewidth of the doped polysilicon conductor defines the gate length in the active device and therefore affects transistor performance (see Figure 16.29). For this reason, CD control is critical. The poly gate etch process must have high selectivity to the underlying gate oxide with excellent uniformity and repeatability. A high degree of anisotropy is also required since the polysilicon line also serves as an implant barrier during the source/drain doping step. Sloped sidewalls would yield partial doping of the implant species under the polysilicon gate structure.

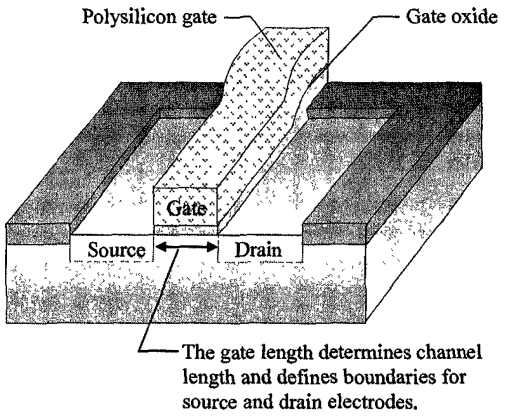


FIGURE 16.29 Polysilicon Conductor Length

Etching polysilicon (and silicon in general) is often a three-step process. This permits optimization for either anisotropy or selectivity during the different etch steps. These three steps are:

1. The first step is a *breakthrough step* that removes the native oxide, hard mask (e.g., SiON) and surface contaminants to achieve a uniform etch (this minimizes etching surface defects from contaminants that act as a micro-mask).
2. This is followed by a *main-etch step* to endpoint. This step removes most of the polysilicon film without damaging the gate oxide and achieves the desired anisotropic sidewall profile.
3. The final step is an *overetch step* that removes the remaining residues and stringers of polysilicon while maintaining high selectivity to the gate oxide. This etch process should be done while avoiding any microtrenching (formation of small trenches) of the gate oxide around the periphery of the polysilicon (see Figure 16.30).

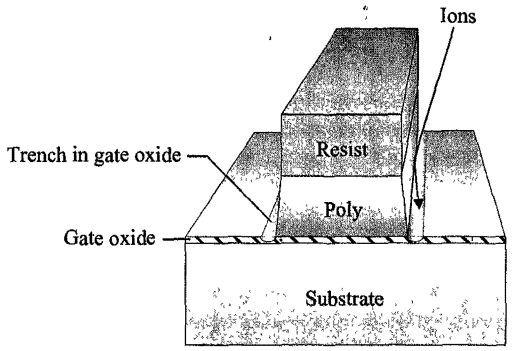


FIGURE 16.30 Undesirable Microtrenching During Polysilicon Gate Etching

The polysilicon gates are difficult structures to etch—requiring care and precision in the etch process. Devices with a 0.15 μm-feature size will have a projected gate oxide thickness of 20 to 30 Å (equivalent thickness of 6 to 10 monolayers of oxide atoms). The process specifications for selectivity of polysilicon etch to oxide typically require no more than a 5 Å loss of oxide thickness (about 1.5 monolayers) across a 70,686 mm^2 surface area on a 300 mm wafer. This will require development of a selectivity >150:1 for the main polysilicon etch process to prevent punchthrough of the gate oxide and an overetch selectivity of >250:1 to remove etch residue and stringers.[29]

Polysilicon etch gas chemistries have traditionally been fluorine-based gases, including CF_4, CF_4/O_2, SF_6, C_2F_6/O_2, and NF_3. The fluorine atoms are instrumental in the etching of silicon, however, this chemical-type of etch results in etch with an isotropic profile. This profile is improved by reducing the fluorine atoms and increasing the ion energy, but this also reduces the polysilicon-to-SiO_2 selectivity. The energy of the bombarding ions must be low enough to avoid sputtering away the gate oxide. To overcome these difficulties, polysilicon plasma etch gases often contain both chlorine and fluorine. Chlorine produces an anisotropic polysilicon sidewall profile with good selectivity to SiO_2. Another common gas chemistry for etching polysilicon is bromine because it gives higher etch selectivity of polysilicon to gate oxide than chlorine. Volatile etch by-products for fluorine, chlorine, and bromine gas chemistries are SiF_4, $SiCl_4$, and $SiBr_4$, all of which are evacuated from the chamber after etching.

Single-Crystal Silicon Etch ■ Single-crystal silicon is etched to form trenches for applications such as device isolation or for the fabrication of vertical capacitors in high-density DRAM ICs. Silicon trench fabrication permits a decrease in the surface area needed for these technologies, which is important as feature sizes continue to decrease on advanced ICs. For STI device isolation in both bipolar and MOS technology, the shallow silicon trenches (depths less than 1 μm to several μms in depth) are filled with oxide dielectric. Capacitors are fabricated by etching a deep trench (a depth greater than 5 μm), oxidizing the sidewalls, and then filling the trench with polysilicon. The vertical capacitor trench design is advantageous because it takes up less surface area and provides higher capacitance values.

Silicon Trench Etching. Silicon trench etching requires precise dimensional control for each trench on the IC. This is a challenge, considering there are millions of capacitor trenches on a high-density IC, with each trench required to have identical smooth, nearly vertical sidewalls, the correct depth, and rounded corners at the bottom and top of the trench. A multistep etch process (as outlined above) is needed, with a modification for the final step where the bottom of the trench is rounded to remove any silicon damage (see Figure 16.31 on page 462).

Sidewall passivation formed by adding carbon to the gas is often used to protect the trench sidewalls from lateral etch attack. The sidewall shape is a function of the wafer temperature—increasing the temperature results in less deposition of sidewall passivation and more lateral etching. Wafer temperature can be controlled by backside cooling of the vacuum chuck with helium.[30]

For plasma dry etching of shallow trenches, fluorine gas chemistry is sometimes used because it has a high silicon etch rate with adequate selectivity to the photoresist that is used as the mask material. For deep trenches (e.g., several microns depth), a chlorine-based or bromine-based gas chemistry is often used because this gas chemistry has a high silicon etch rate and high selectivity

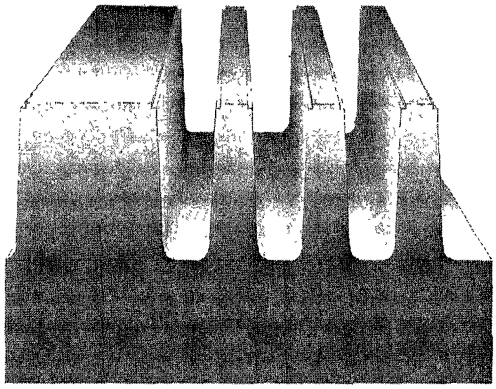


FIGURE 16.31 Silicon Trench Etching

to the oxide mask. Bromine gas chemistry is becoming common in high-density plasma reactors because it is an aggressive etchant that does not require extensive use of carbons for sidewall passivation (which reduces contamination problems). The primary problem with bromine gas chemistry is that it is extremely corrosive to the gas delivery system and reactor. The gas suppliers and equipment manufacturers are addressing this issue.

Metal Dry Etch

A major application in metal etch is aluminum alloy for interconnect wiring. Recall from Chapter 12 that copper alloyed with aluminum reduces electromigration and hillock formation in aluminum, while silicon is added to aluminum to minimize spiking at contact interfaces. Silicon poses no additional etch resistance. Tungsten, barrier metals, and the contact metal are also common metals etched during wafer fabrication. However, copper metal is not dry etched because it does not easily form volatile compounds, which makes plasma etching difficult. Due to the density of interconnect lines on the critical layers of ULSI wafers, an anisotropic dry etch is necessary to attain the desired edge profile and narrow lines. The major requirements for metal etching are:[31]

1. High etch rates (>1000 nm/min).
2. High selectivity to the masking layer (>4:1), interlayer dielectric (>20:1), and the underlying layers.
3. High uniformity with excellent CD control and no microloading (<8% at any location on the wafer).
4. No device damage from plasma-induced electrical charging.
5. Low residue contamination (e.g., copper silicon residue, developer attack, and surface defects).
6. Fast resist strip, often in a dedicated cluster tool chamber, with no residual contamination.
7. No corrosion.

Aluminum and Metal Stacks ■ A chlorine-based chemistry process is commonly used for aluminum etch. Pure chlorine etches aluminum isotropically. To achieve a directional etch process with anisotropic etching, sidewall passivation is needed by adding polymers to the etch gas, such as with CHF_3 or carbon obtained from the photoresist. BCl_3 is also used for aluminum etch, which has heavy molecules for a physical etch and good sidewall profile control. A small amount of N_2 is often added to the gas chemistry to minimize microloading and assist sidewall passivation. Aluminum etching with fluorine-based gas chemistry is unacceptable because of the low vapor pressure of the etch by-product, nonvolatile AlF_3, which means that the etch rate is extremely limited. Bromine-based chemistry has been investigated for metal etch.

A challenge in metal etch for interconnect wiring is the complexity of the multilayer stack that is common in VLSI/ULSI technology (see Figure 16.32). There is often an antireflective coating (ARC) of TiN or other materials and an underlying adhesion barrier (e.g., Ti), which complicates the etch process. To remove ARC films, possible etch gas chemistries are CCl_4/O_2 or SF_6/Cl_2. TiN films are removed in CCl_4/N_2 or Cl_2/Ar or $BCl_3/Cl_2/CHF_3$.[32] Another factor is that aluminum

oxidizes almost instantly when exposed to air and the resulting aluminum oxide (Al_2O_3) inhibits the chlorine etch reactions.

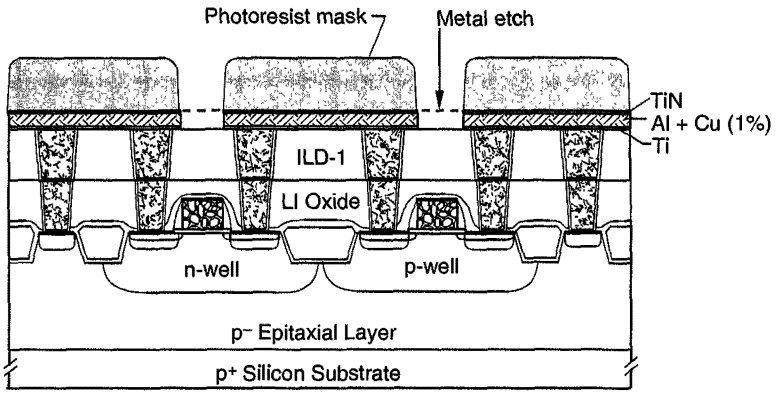


FIGURE 16.32 Metal Stack for VLSI/ULSI Integration

To etch a metal stack structure, multiple steps are used. This includes the first step to remove the native oxide layer (e.g., Al_2O_3 for aluminum) on the surface. The typical steps for etching a metal stack are:

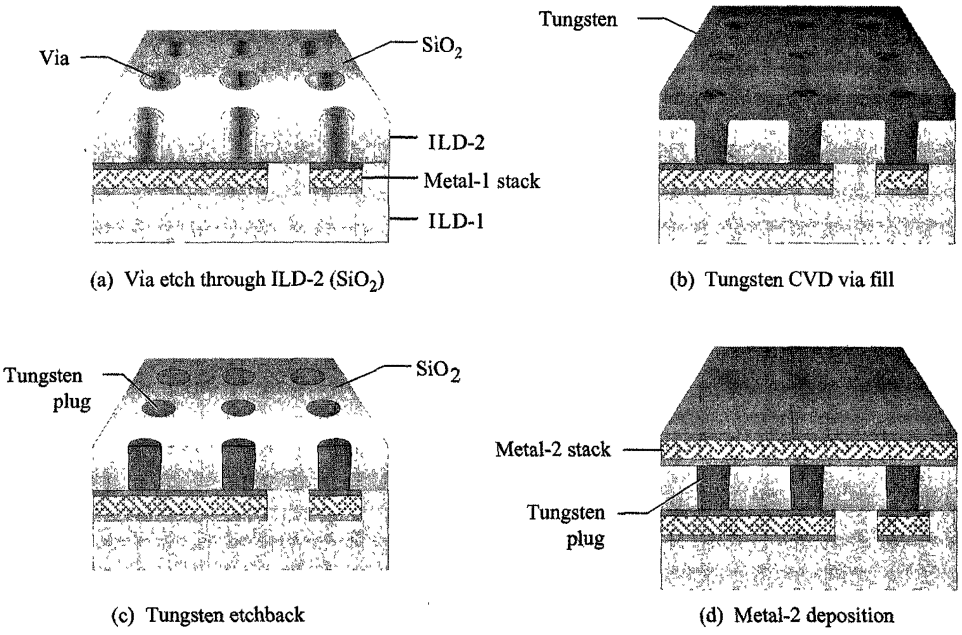
1. Breakthrough step to remove native oxide.
2. ARC layer etch (may be combined with above step).
3. Main etch step of aluminum.
4. Overetch step to remove residue. It may be a continuation of the main etch step.
5. Barrier layer etch.
6. Optional residue removal process to prevent corrosion.
7. Resist removal (see section below).

Thorough corrosion control is essential to device performance after metal etching. Any remaining corrosive by-products of the etch process must be quickly neutralized or removed from the wafer surface. For aluminum etching, the major corrosive by-products are $AlCl_3$ or $AlBr_3$. These by-products react with water to form highly corrosive HCl or HBr, which are damaging acids to aluminum. Control of water vapor and oxygen content is critical in the etch process, which is best achieved in single-wafer etch reactors with a loadlock chamber to isolate the wafers from atmospheric contaminants and moisture. Another approach is to use the resist strip process to remove corrosive compounds while removing the resist, thus reducing their potential for corrosion.[33]The need to minimize the time delay and exposure to moisture are reasons for an etcher to have an integrated photoresist removal chamber.

Tungsten ■ Tungsten (W) is an important metal commonly used for via fill in a multilevel metal structure (see Chapter 12). Tungsten etch can be done with fluorine- and chlorine-based chemistry. However, fluorine-based chemistry, such as SF_6 and CF_4, has poor oxide selectivity. Chlorine-based gas chemistry has good oxide selectivity. N_2 is often added to the gas mixture to give better selectivity to the photoresist mask. Sometimes an O_2 forming gas is added to reduce carbon deposits. A chlorine gas such as Cl_2 or CCl_4 can be used to etch tungsten with improved anisotropy and selectivity.

Tungsten Etchback. *Tungsten etchback* is used as one step in the formation of tungsten plugs. Via openings are first etched in the SiO_2 interlayer dielectric (ILD). The W is blanket-deposited (CVD) into the via openings on top of a TiN barrier layer. This operation is followed by a dry plasma etchback step to remove the excess blanket layer and finish with a tungsten-filled via (see Figure 16.33 on page 464). The etch involves a two-step process. In the first step, 90% of the tungsten is etched at a high rate with excellent uniformity. In the second step, the etch rate is reduced and a gas chemistry is used with a high selectivity to the TiN barrier layer.[34] The etch

reduction serves to decrease gas pressure and wafer temperature to reduce loading effects that may cause a recess in the W plug. Anisotropic etching is not needed, but minimal residue and plug loss are important. This etchback process has been largely replaced for advanced wafer fabrication by chemical mechanical planarization (CMP) to remove excess W and planarize the top surface of the contacts and vias (see Chapter 18).



(a) Via etch through ILD-2 (SiO_2)

(b) Tungsten CVD via fill

(c) Tungsten etchback

(d) Metal-2 deposition

FIGURE 16.33 Tungsten Etchback

Contact Metal Etch ■ Refractory metals alloyed with silicon form the silicides common in wafer fabrication, including $CoSi_2$, WSi_2, $TaSi_2$, and $TiSi_2$ (see Chapter 12). A polycide is a composite of doped polysilicon and a refractory metal. Silicon dioxide does not form an alloy with the refractory metals, and it is the unreacted metal that must be removed during the contact metal etch process. Contact metal etch is critical in MOS device fabrication because the dimensional control will affect the channel length of the device. Contact metal etch with dry plasma can be done with fluorinated and chlorinated gas chemistries. Fluorine-based gas chemistry, such as NF_3 and SF_6, is used because of its good dimensional control with increased etch rate. Since the contact formation is a self-aligning process, no photoresist mask is required for this etch process.

WET ETCH

Wet etching has been associated with wafer fabrication since the beginning of the semiconductor industry. It has been replaced to a large degree by dry etching but still plays an important role in oxide cleaning, residue removal, the stripping of surface layers, and etching for larger geometry applications. Wet cleaning (see Chapter 6) can actually be considered a wet etch process. An example is the residue layer and damaged silicon layer formed by reactive ion etching of a contact hole. The contact residue is removed by downstream microwave ashing followed by wet etching as a form of cleaning to remove residues and silicon damage.[35] The benefits from wet etching over dry etching are good selectivity to the underlying film, no risk of plasma damage to devices, and use of simple equipment. Basic wet-etch parameters (see Table 16.7) must be controlled during the etching process. These parameters are applicable to all wet etching applications.

Wet etching is done by exposing a batch of wafers, usually 25 but sometimes up to 50 wafers, to an appropriate acid bath, either by immersion or spray. Immersion is the simplest method, while spray etching requires less volume of chemicals and is faster than immersion. Wet etching produces an isotropic sidewall with substantial undercutting of the film underneath the edge of the mask material, making it unsuitable for feature sizes <3 μm. Isotropic etching with undercutting is the main

TABLE 16.7 Wet-Etch Parameters

Parameter	Explanation	Difficulty to Control
Concentration	Solution concentration (e.g., ratio of NH_4F:HF to etch oxide).	Most difficult parameter to control because the bath concentration is continually changing.
Time	Time of wafer immersion in the wet chemical bath.	Relatively easy to control.
Temperature	Temperature of wet chemical bath.	Relatively easy to control.
Agitation	Agitation of the solution bath.	Moderately difficult to properly control.
Number of Runs	Solution must be replaced after specified number of runs to reduce particles and to ensure proper solution strength.	Relatively easy to control

reason why the majority of semiconductor etching is done with dry plasma etch. Other disadvantages to wet etch are the chemical safety concerns for wet baths, its tendency to cause resist lifting and bubbles, the difficulty in controlling the bath parameters for uniformity, and the high cost of chemical disposal.

Types of Wet Etch

Wet etching can provide an alternative for high etch selectivity that might not be available with dry etching. In addition, wet etching eliminates plasma damage. As previously stated, wet etch has been widely replaced by plasma dry etching in advanced IC wafer fabrication. Materials such as silicon and aluminum are nearly always dry etched for submicron fabrication. General safety information for wet etch chemicals is provided in Appendix A.

Wet Oxide Etch ■ Oxide can be wet etched by hydrofluoric acid (HF). Selective removal of oxide is done by spraying or immersing the wafer in a dilute solution of HF that is frequently buffered with ammonium fluoride (NH_4F), known as a *buffered oxide etch* (*BOE*) or *buffered HF* (*BHF*). A chemical buffer is a solution that resist changes in pH when small amounts of strong acid or base are added. Buffering the HF with NH_4F provides a well-controlled etch solution that slows and stabilizes the etch and does not appreciably attack the photoresist. The BOE is rinsed from the wafer using DI water and quick dump or cascade overflow rinse equipment. The quick dump rinse is faster and uses less DI water, but cascade rinsing can significantly reduce particulate contamination levels.

SiO_2 is an amorphous material and etches equally well in all directions when exposed to BOE. If a 1 μm thick oxide layer is etched, there is also a lateral etch of 1 μm under the mask material. This lateral etching and the subsequent undercutting is undesirable from a dimensional standpoint, limiting the density of lines and spaces that can be achieved.

The oxide etch rate also depends on whether it is thermal or deposited oxide (see Table 16.8 on page 466). Since dry grown oxide is denser than wet grown oxide, dry grown oxide etches at a slower rate. In addition, doped oxides etch differently and usually faster than undoped oxides.

Wet Chemical Strips ■ Due to the high selectivity of wet etch, *wet chemical strips* are sometimes used to remove surface layers, including photoresist (see the following section) and masking layers. Silicon nitride (Si_3N_4) is widely used in wafer fabrication as a mask material in the isolation technologies of shallow trench isolation (STI), local oxidation of silicon (LOCOS), and self-aligned contact structure. The removal of the nitride masking layer is often done by a wet chemical strip with hot phosphoric acid (H_3PO_4).[36] The wet acid bath solution is typically maintained at around 160°C and has the desirable property of high selectivity to exposed oxide layers. Control of the hot phosphoric nitride removal bath is difficult and it is done as a timed operation (no endpoint detection) with the use of monitor wafers. There is usually some oxynitride formation on the exposed nitride layer that requires a short hydrofluoric acid (HF) deglaze before the nitride removal. If the oxynitride layer is not removed, then there is a risk of nonuniform nitride removal. Another material often

TABLE 16.8* Approximate Oxide Etch Rates in BHF[a] Solution at 25°C

Type of Oxide	Density (g/cm^3)	Etch Rate (nm/s)
Dry grown	2.24 to 2.27	1
Wet grown	2.18 to 2.21	1.5
CVD deposited	<2.00	1.5[b] to 5[c]
Sputtered	<2.00	10 to 20

a) 10 parts of 454 g NH_4F in 680 ml H_2O and one part 48% HF
b) Annealed at approximately 1000°C for 10 minutes
c) Not annealed
*B. El-Kareh, *Fundamentals of Semiconductor Processing Technology* (Boston: Kluwer Academic, 1995), p. 277.

removed by wet strip is the titanium layer deposited to form the titanium silicide at the contacts. Ammonium hydroxide (NH_4OH) and hydrogen peroxide (H_2O_2) are diluted with DI water for this process.

HISTORICAL PERSPECTIVE

Etch technology has undergone many changes throughout the years of wafer fabrication. The initial barrel plasma etcher was a simple tool with limited operator controls. The modern plasma etcher generates a high-density plasma, has independent RF power supplies for plasma generation and wafer bias, endpoint detection, gas pressure and flow control, and is integrated with software control of the etch parameters. Table 16.9 details the advances for polysilicon etching from wet etch technology through reactive ion etch (RIE) and up to modern high-density plasma etch tools for subquarter micron geometries.

PHOTORESIST REMOVAL

One of the last steps after etching is the removal of the photoresist mask. The photoresist serves as the pattern transfer medium from the reticle to the wafer surface and blocks films from being etched or ions from being implanted. Once etch or implantation is complete, the resist serves no further purpose on the wafer surface and must be completely removed. In addition, any trace residues from the etch process are also removed.

Photoresist stripping is the general term that describes the wet removal of the resist. Stripping is sometimes used for resist residues that are difficult to remove. In most applications, wet resist stripping is not cost effective because of the required handling and disposal of wet chemicals. Furthermore, if the resist has previously undergoine dry etch processing, its top surface could be hardened from exposure to fluorinated and chlorinated gas chemistry. This renders the resist insoluble in most wet chemistry stripping solutions. In this case, plasma stripping is required to remove at least the top resist layer.

A major challenge for photoresist removal is that resists are designed and processed to achieve maximum adhesion to the wafer surface. As discussed in Chapter 13, this is required for the resist to withstand the rigors of the etch process and ion implantation. Maximum resist adhesion creates an obvious challenge for photoresist removal. Another challenge is the need for a high resist strip rate to attain a higher wafer throughput. However, a high strip rate generally tends to leave more resist residues, which places more burden on the removal process to effectively remove all resist and residues.

Plasma Ashing

Plasma ashing is the dry removal of resist with oxygen, and is the dominant technique for bulk resist removal.[37] The first plasma ashers in the 1970s used barrel reactor technology, with oxygen

TABLE 16.9* Polysilicon Etch Technology Evolution

Geometry Requirements	Time Frame and Reactor Design	Chemistries	Strengths	Limitations and Problems	Controls
4 to 5 μm, isotropic etch	Pre-1977: wet etch	HF/HNO_3 buffered with acetic acid or H_2O	Batch process	Resist lift; bath aging; temperature sensitive	Operator judgement for endpoint
3 μm	1977: barrel etcher	CF_4/O_2	Batch process	Nonuniformity; isotropic etch; large undercut	Manometer and timer
2 μm	1981: single wafer etch	CF_4O_2	Single wafer; individual etch endpoint, improvement in repeatability	Low oxide selectivity; isotropic process	Endpoint detection
1.5 μm	1982: single wafer RIE	SF_6/Freon 11, SF_6/He	MFCs; independen pressure and gas flow control, improvement in repeatability	Low oxide selectivity; profile control	MFCs; separate gas flow and pressure control
To 0.5 μm	1983: variable gap; load-locked	CCl_4/He, Cl_2/He, Cl_2/HBr	Load-locked chamber; variable gap; improvement in repeatability	Microloading in high-aspect ratios; profile control	Control of electrode gap; computer controls
To 0.25 μm and below	1991: inductively-coupled plasma (ICP)	Cl_2, HBr	High-density plasma; low pressure; simple gas mixtures; improvement in repeatability	Complex tool; many variables	Independent RF control for plasma generation and wafer bias

*Adapted from C. Almgren, "The Role of RF Measurements in Plasma Etching," *Semiconductor International,* (August 1997): p. 100.

plasmas to strip the resist. Barrel reactors have been widely replaced with downstream plasma reactors that strip the resist with an oxygen plasma in single-wafer chambers.

Asher Overview ■ A *photoresist asher* removes the resist layer by reacting atomic oxygen atoms with the resist material in a plasma environment (see Figure 16.34 on page 468). Atomic oxygen (O) is created by using microwave or RF energy to dissociate molecular oxygen (O_2). There are usually forming gases such as N_2 or H_2 added to improve the ash performance and enhance polymer residue removal.[38] Thus, a typical asher gas chemistry would be O_2/N_2. Recall from Chapter 13 that resist is basically a hydrocarbon polymer. The atomic oxygen atoms rapidly react with the resist material to create volatile carbon monoxide (CO), carbon dioxide (CO_2), and water (H_2O) as the main by-products. The asher by-products are pumped away by the vacuum system.

Plasma Damage ■ A concern during the ashing process is plasma damage to devices on the wafer surface from ion bombardment or wafer charging. As gate oxides are scaled thinner, this concern is more critical due to the sensitivity of thin oxides to plasma degradation. Wafer damage from plasma has largely been remedied by using single-wafer downstream ashers that position the wafer away from the damaging plasma ions, allowing only reactive chemical species to reach the wafer. Microwave (2.45 GHz) frequencies are common for source plasma generation in downstream systems. This is because a microwave glow discharge produces more atomic oxygen reactant and a lower proportion of ionic species. This yields lower risk of ion-induced damage.

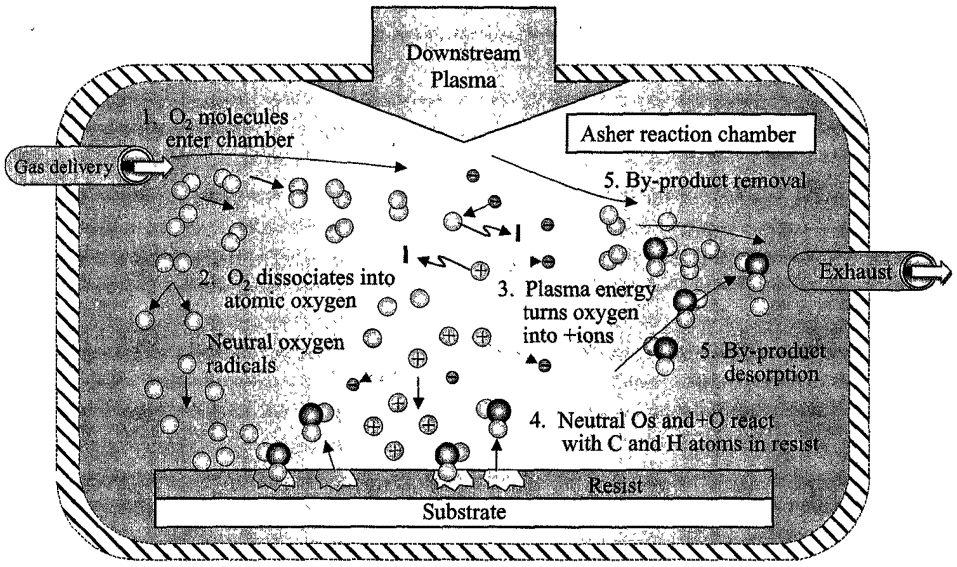


FIGURE 16.34 Atomic Oxygen Reaction with Resist in Asher

Residue Removal ■ Standard ashing has evolved to include the removal of post-etch residues such as sidewall polymers and via veils (see Figure 16.35). As previously discussed, these residues are complex and can contain plasma etching and ashing by-products such as aluminum, titanium, oxides, and silicon. A complicating factor is that ashing may occur at an elevated temperature (e.g., 200°C), which can harden residues and make them harder to remove. If not removed, residues are a source of particles and contaminants that increase the wafer defect density. To fully remove etch residues, especially the inorganic residue materials (e.g., silicon oxides, metal oxides, aluminum, and so on), some ashers are based on alternative plasma chemistries to oxygen, such as NO or N_2O. Other asher systems add a small amount of fluorine to the gas chemistry in the form of CF_4 or NF_3 to more effectively remove residues containing oxide and silicon by making them more water soluble.[39] The ash process is typically followed by a DI water rinse to remove residual particles on the wafer surface.[40] In some cases a strong sulfuric acid (H_2SO_4) mixture with hydrogen peroxide (such as the piranha mixture discussed in Chapter 6) is used to thoroughly clean the remaining stripped photoresist.

Wet cleaning for residue removal still is found in backend processes, particularly for the removal of sidewall passivating residues that have high-density inorganic contaminants. Dry ashing alone is not sufficient to strip and clean residues because of the multitude of inorganic materials present that are not volatized by the plasma. Until recently, wet chemistry residue strippers were commonly based on a hydroxylamine compound. However, there is a corrosion risk to metal and barrier layers from this stripper and new hydroxylamine-free formulations are in use based on a chelation chemistry to strip residues (a chelate is a complex ion that involves metal cations).[41] This new formulation dissolves inorganic residues at low temperature with no corrosion.

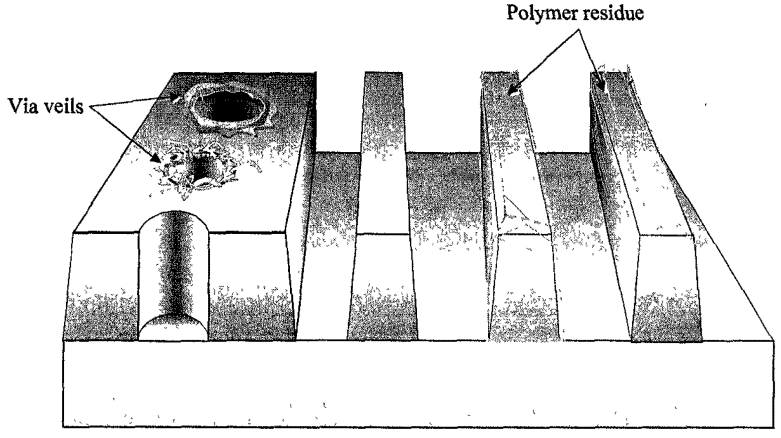


FIGURE 16.35 Post-Etch Via Veil Residue

ETCH INSPECTION

The final step in the etch process is an *etch inspection* to verify quality measures. This inspection occurs on the patterned wafer after all etching and photoresist stripping is completed. It has traditionally been done with a manual microscope inspection that used incident white or ultraviolet light to inspect for defects such as stains and large particulate contamination. Manual microscopes have been largely replaced by automatic inspection systems, especially on critical layers with deep submicron patterning. Advanced metrology instruments are able to automatically inspect patterned wafers for patterned defects and distortions (see Chapter 7). One of the most important inspections that occurs at final inspection is the automated measurement to verify critical dimensions (CD) on a particular mask level. The quality of the etch process is also verified by inspecting for etch problems such as overetching, underetching and undercutting.

Etch inspection is similar to the inspection at develop inspect, except that there is no photoresist and defects usually cannot be reworked. Almost any defect, if numerous enough, will cause the wafer to be scrapped. An exception to this rule is surface particle contamination, which can be cleaned. Representative quality measurements for etch final inspection are described in Table 16.10.

ETCH INSPECTION QUALITY MEASURES

Typical quality measures for etch inspection are provided in Table 16.10.

TABLE 16.10 Quality Measures for Etch Final Inspection

Quality Parameter	Types of Defects	Remarks
1. Critical dimension bias.	A. Linewidth change: excessive difference between photoresist linewidth and final feature linewidth after etch.	• CD bias for linewidth change is measured by comparing pre-etch linewidth in photoresist with post-etch linewidth of the same feature on the wafer. Measurements can be done with an SEM. • Excessive CD bias requires optimization of the etch process for undercutting or slope. • The photoresist profile has an effect on CD bias. Vertical resist profile produces best CD bias.
2. Metal corrosion.	A. Corrosion or attack of metal film after etch.	• Corrosion often results from residual HCl on the wafer that is exposed to water vapor in the air. • Corrosion may be visible as small bubbles along the side of metal lines. This defect is looked for by optical microscope or SEM.
3. Sidewall contaminants after etching.	A. Residual sidewall passivants that remain after etch, including remaining photoresist.	• Minimize formation by optimizing the pre-metal etch photoresist hard bake. • Residues are usually removed by post-etch solvents or dilute buffered HF.*
	B. Contaminants backsputtered onto the sidewall of the metal line or a via hole.	• Backsputtering can occur due to polymer used to passivate sidewall, leaving a "veil" residue (thin overhang along metal line or via sidewall).
4. Loading effects.	A. Microscopic nonuniformity of etch process.	• Etch rate between narrow openings is slower than open-field areas due to reduced density of reactive radicals in small space. • Balance pressure and power of etch process.**

Quality Parameter	Types of Defects	Remarks
5. Shorts after metal etch.	A. Bridging of metal lines after etch leading to electrical short.	• Reduce pattern density effects from microloading.
6. Excessive post-etch residue.	A. The following types of residue may exist after etch: • Stringers (small strings of residue). • Veils (thin residue overhang). • Crowns • Rails • Corrosion after metal etch.	The causes of residue after etch are: • Nonuniform etch process. • Films deposited over topography. • Nonuniform dopant distribution in film. • Contaminants in the film (in addition to intentional alloys such as Cu in Si). • Contaminants in gas or chamber. Check supply filters or clean system. • Incorrect process parameter, such as high etch rate.

*K. Mautz, *Optimization of Single Wafer and Batch Metal Etch Manufacturing Processees* vol. 96-12 (Pennington, NJ: The Electrochemical Society, 1996), p. 283.
**S. Gonzales, J. Quijada, and G. Grivna, *Submicron Metal Etch Integration Study* vol. 2875 (Bellingham, WA: SPIE, 1996), p. 302.

DRY ETCH TROUBLESHOOTING

Problems associated with dry etch equipment and process are provided in Table 16.11.

TABLE 16.11 Common Dry Etch Troubleshooting Problems

Problem	Probable Cause	Corrective Actions
1. Incorrect etch rate.	A. Change in RF power. B. Incorrect temperature. C. Problem with pressure. D. Endpoint detection not functioning properly. E. Improper wafer spacing. F. Improper gas-flow dynamics. G. Improper maintenance. H. Incorrect process recipe.	• Check and troubleshoot RF generator and matching unit. • Check backside wafer cooling system. • Calibrate vacuum gauges (e.g., capacitive manometer) and pressure control system. • Check endpoint detection system. • Check wafer-to-electrode gap. • Verify gas distribution system. • Perform chamber wet clean. • Verify process recipe and parameters.
2. Inadequate selectivity.	A. Etch rate too high. B. Improper gas flow or pressure. C. Endpoint detection problem. D. Wrong wafer temperature. E. Incorrect process recipe.	• Verify etch rate. • Calibrate MFCs and vacuum gauges. • Check/calibrate endpoint detection. • Check wafer cooling system. • Confirm process recipe and parameters.
3. Improper sidewall profile angle.	A. Contamination on sidewall. B. Temperature of wafer. C. System pressure. D. Incorrect process recipe (misprocess).	• Check for polymer buildup in chamber. • Backside contamination of wafer causing nonuniform heating. • Check/calibrate MFCs and perform leak test to check for contamination.

Problem	Probable Cause	Corrective Actions
4. Etch nonuniformity across wafer.	A. Depletion of etchant gas concentration due to ARDE. B. Improper gas flow. C. Temperature of wafer. D. Improperly positioned wafer in chamber. E. Chamber configuration. F. Improper film thickness. G. Improper maintenance.	• Verify acceptable design for dense and nondense areas of wafer. • Check/calibrate gas distribution system. • Check thermocouples and wafer cooling. • Check robotics, wafer handling system, and vacuum chuck • Check reactor plate spacing. • Measure and verify film thickness. • Perform chamber wet clean.
5. Plasma damage.	A. Nonuniform plasma. B. Excessive ion bombardment of gate oxide. C. Excessive RF power. D. Improper maintenance.	• Poorly designed or maintained plasma equipment. • Suboptimum process conditions. • Check recipe and RF generator.
6. Particle Contamination.	A. Leak/contamination from gas lines. B. Tool operation. C. Improper gas chemistry.	• Leaks or faulty MFCs. • Improper tool shutdown, operation, or maintenance. • Wrong process recipe. • Perform wet clean.
7. Metal Corrosion.	A. Moisture. B. Gas flow. C. Contaminants from etch process. D. Wrong maintenance procedure.	• Excessive time delay for post-etch residue cleanup. • Check MFCs for correct process gases. • Control time to resist strip. • Check maintenance procedure.

SUMMARY

Etch selectively removes material from the wafer surface by chemical or physical means. Dry etch uses a plasma, whereas wet etch uses liquid chemicals. Etch is generally divided into categories including dielectric, silicon, and metal etch. There are nine important parameters: etch rate, etch profile, etch bias, selectivity, uniformity, residues, polymer formation, plasma-induced damage, and particle contamination. Plasma etch has many advantages over wet etch and is the most common etch process. Sidewall profiles are generally divided into isotropic and anisotropic. Anisotropic, or vertical sidewalls, are produced by dry plasma etching. Oxide etch requires high selectivity to the underlying material. Silicon etch is used for critical applications such as polysilicon gate formation and trench formation. A main application of metal etch is aluminum interconnect wiring, with the need to etch through complex metal stacks. Wet etch has been largely replaced by dry etch for advanced IC fabrication but is still used for oxide removal, wet cleans, and stripping. The removal of photoresist at the completion of etch or ion implant is known as photoresist ashing. An asher uses a downstream process to minimize plasma-induced damage and is usually followed by a wet etch to remove residues. Etch inspection is the last operation in the etch process and is necessary to ensure defects are identified and corrected.

KEY TERMS

etch
dry etch
wet etch
dielectric etch
silicon etch
metal etch
patterned etching
unpatterned etching (etchback or stripping)
etch rate
step height
loading effects
etch profile
isotropic etch profile
anisotropic etch profile
directionality
etch bias
selectivity
etch uniformity
aspect-ratio-dependent etching (ARDE)
microloading
etch residue
polymer formation
plasma-induced damage
chemical mechanism
physical mechanism
combined physical and chemical mechanism
plasma potential distribution
barrel reactor
parallel plate (planar) reactor
downstream reactor
triode planar reactor
ion beam milling or ion beam etching (IBE)
reactive ion etch (RIE)
high-density plasma etch
electron cyclotron resonance (ECR)
inductively coupled plasma (ICP)
dual plasma source (DPS)
magnetically enhanced RIE (MERIE) or magnetron
endpoint detection
breakthrough step
main-etch step
overetch step
tungsten etchback
buffered oxide etch (BOE) or buffered HF (BHF)
wet chemical strips
photoresist stripping
plasma asher
photoresist asher
etch inspection

REVIEW QUESTIONS

1. Define etch. What is the goal of etching?
2. What are the two types of etch processes? Give a short description of each type.
3. List the three major material categories for dry etch.
4. Explain the difference between patterned and unpatterned etching.
5. List nine important parameters for etch.
6. Define etch rate and state its formula. Why is it desirable to have a high etch rate?
7. Explain loading effects and how this is related to the etch rate.
8. Describe isotropic and anisotropic etch profiles and what are the desirable and undesirable aspects of each profile.
9. Is a dry etch profile isotropic, anisotropic or both? What about a wet etch profile?
10. What is directionality and why is it desirable in etching?
11. What is etch bias and what is it caused by? State and explain the etch bias formula.
12. Define selectivity. Does dry etching have good or poor selectivity? What does high selectivity mean? State and explain the selectivity formula.
13. What is etch uniformity? What is the challenge for etch uniformity? Explain ARDE and discuss how it is related to etch uniformity. What is another name for ARDE?
14. Discuss etch residues, why they occur, and how they are removed.
15. Why is a polymer formation deposited sometimes on feature sidewalls during etch? What is an undesirable side effect of polymer formation?
16. What is plasma-induced damage from etching and what problems occur from this damage?
17. Explain how plasma can cause particle contamination on the wafer surface.
18. What is the goal of dry etch? List the advantages of dry etch over wet etch. What are the disadvantages of dry etch?
19. List the three ways to achieve etching action during dry etch.

20. Explain the chemical mechanism and the physical mechanism for achieving etching action.
21. Describe the combined physical and chemical mechanism for dry etch.
22. Describe the plasma potential distribution and why it is important for etch.
23. What are the etch results if the RF frequency is decreased? RF power is decreased? DC bias is increased? Electrode size is decreased?
24. Describe the basic components of a plasma dry etch system. What gas chemistries are used for silicon dioxide, aluminum, silicon and photoresist?
25. Describe the barrel plasma etcher.
26. Describe the parallel plate (planar) reactor.
27. Why is downstream etching beneficial? Describe a downstream reactor.
28. How does a triode planar reactor function?
29. Explain ion beam milling. For what materials is it used?
30. Describe reactive ion etch (RIE).
31. Explain the principle for how high-density plasma improves etching of high-aspect ratio gaps.
32. Give three reasons for using a magnetic field with a high-density plasma etcher.
33. Describe electron cyclotron resonance (ECR).
34. Explain inductively-coupled plasma (ICP).
35. Describe dual plasma source (DPS).
36. Discuss the MERIE technology for high-density plasma.
37. What is endpoint detection and why is it necessary for dry etch? What is the most common type of endpoint detection?
38. Describe optical emission spectroscopy for endpoint detection.
39. List six requirements for successful dry etch.
40. List three challenges for oxide etching.
41. Oxide plasma etching is usually based on what gas chemistry? Give a specific gas chemistry common for oxide etch.
42. Give an example why oxide etch selectivity to the underlying material is important. Provide two methods for achieving oxide etch selectivity to silicon.
43. What is one factor that reduces photoresist selectivity? Is this desirable or undesirable?
44. Explain the effect of low resist selectivity on contact via etch in the LI oxide.
45. Is the etch rate faster for silicon nitride deposited with PECVD or LPCVD? Why?
46. What gas chemistries are usually used for etching polysilicon and why has these chemistries replaced fluorine chemistries?
47. Give three requirements for polysilicon gate etch.
48. List and describe the three steps for etching polysilicon.
49. Discuss the polysilicon etch gas chemistries.
50. How are silicon trench sidewalls protected during plasma etch from lateral etch attack?
51. What gas chemistry is sometimes used for shallow trench etching? Deep trench etching? Why are these gas chemistries used?
52. List the seven major requirements for metal etching.
53. List the seven steps for etching a metal stack.
54. What control is necessary after metal etching?
55. What gas chemistry has good oxide selectivity during tungsten dry etch?
56. Describe the tungsten etchback process.
57. What is the main reason why dry etch has largely replaced wet etch?
58. List four wet etch parameters, explain each parameter and state how difficult it is to control.
59. How is oxide wet etched? What are the two names of the FF solution buffered with ammonium fluoride?
60. What is the wet etch rate difference for dry grown versus wet grown oxide?
61. Describe the silicon nitride wet chemical strip.
62. What is photoresist stripping?
63. What is plasma ashing? What is the purpose of a photoresist asher?
64. What is a concern from the ashing process? How is this concern resolved?
65. How are post-etch residues removed?
66. What is an important aspect of performing an etch inspection?

ETCH EQUIPMENT SUPPLIERS' WEB SITES

Applied Materials	http://www.appliedmaterials.com/products/
Eaton Corporation	http://www.semiconductor.eaton.com/
Gasonics International	http://www.gasonics.com/
Hitachi	http://www.hitachi.com/semiequipment/products.html
International SEMATECH	http://www.sematech.org
Lam Research Corp.	http://www.lamrc.com/
Leybold-Inficon	http://www.leyboldinficon.com/
MRC, Materials Research Corp.	http://www.materialsresearch.com/
Plasmos	http://www.plasmos.com/
SEMI	http://www.semi.org/
Tegal Corporation	http://www.tegal.com
TEL, Tokyo Electron Ltd.	http://www.teainet.com

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CHAPTER 17

ION IMPLANT

Intrinsic silicon crystal structure is formed by silicon covalent bonds. As explained in Chapter 2, intrinsic silicon is a poor conductor. Silicon only becomes useful as a semiconductor when its structure and conductivity are altered by adding small amounts of impurities called dopants. This process is referred to as doping. The doping of silicon is fundamental to pn junction fabrication in semiconductor devices. Ion implantation is the primary method for doping wafers.

Doping is widely used throughout wafer fabrication. Dopants are precisely and uniformly placed into the device to alter its electrical performance. Silicon chips require doping with Group IIIA and Group VA dopants for many different reasons, which will be discussed in this chapter.

The continual shrinking of chip critical dimensions and the subsequent increase in chip packing density force the scaling of all device elements. An example of this is the reduction of the polysilicon gate length to obtain a narrower channel region. A shorter channel length requires shallower junction depths for the source and drain doped regions. Junction depths are ultrashallow for chips designed at the 0.18 μm and below technology nodes. The junction depth requirements decrease to 30 ± 10 nm for devices with a CD of 0.1 μm.[1]

OBJECTIVES

After studying the material in this chapter, you will be able to:

1. Explain the purpose and applications for doping in wafer fabrication.
2. Discuss the principles and process of dopant diffusion.
3. Provide an overview of ion implantation, including its advantages and disadvantages.
4. Discuss the importance of dose and range in ion implant.
5. List and describe the five major subsystems for an ion implanter.
6. Explain annealing and channeling in ion implantation.
7. Describe different applications of ion implantation.

INTRODUCTION

Doping is the introduction of a dopant into the crystal structure of a semiconductor material to modify its electronic properties (e.g., electrical resistivity). As discussed in Chapter 2, certain Group IIIA and VA elements are used as dopants in wafer fabrication. For review, Table 17.1 on page 476 highlights the four principal dopants used in semiconductor manufacturing.

Dopant species are also referred to as impurities but should not be confused with contaminating impurities. Dopants are introduced into the silicon and other fabrication materials for a variety of reasons. For instance, dopants such as boron and phosphorus are used to form the majority carriers in silicon devices, to form conductive layers in the wafer, or to alter material properties (e.g., doping SiO_2 to form borophosphosilicate glass, or BPSG). The polysilicon gate electrode is doped for conductivity.

There are two techniques in wafer fabrication for introducing dopant elements to the wafer materials: thermal diffusion and ion implantation. *Thermal diffusion* uses high temperature to move the dopant through the silicon lattice structure. This method is dependent on time and temperature. *Ion implantation* introduces dopants into the substrate through a high-voltage ion bombardment. The dopants are implanted into the wafer through high-energy collisions at the atomic level. In the beginning of semiconductor manufacturing, thermal diffusion was the primary method for doping the wafer. However, due to shrinking critical dimensions and the corresponding scaling requirements, nearly all dopant processes in modern wafer fabrication are now done with

TABLE 17.1 Common Dopants Used in Semiconductor Manufacturing

Acceptor Dopant Group IIIA (p-Type)		Semiconductor Group IVA		Donor Dopant Group VA (n-Type)	
Element	**Atomic Number**	**Element**	**Atomic Number**	**Element**	**Atomic Number**
Boron (B)	5	Carbon	6	Nitrogen	7
Aluminum	13	Silicon (Si)	14	Phosphorus (P)	15
Gallium	31	Germanium	32	Arsenic (As)	33
Indium	49	Tin	50	Antimony	51

Note: Common dopants are shaded.

ion implantation (see Figure 17.1). Table 17.2 outlines some critical processes commonly doped with ion implantation versus the limited doping done by diffusion. Figure 17.1 shows these doped regions on a cross section drawing of a CMOS inverter. Note the dopant type (p or n) and concentration (− or +) are also shown. The different doped regions labeled A to O are defined in Table 17.2.

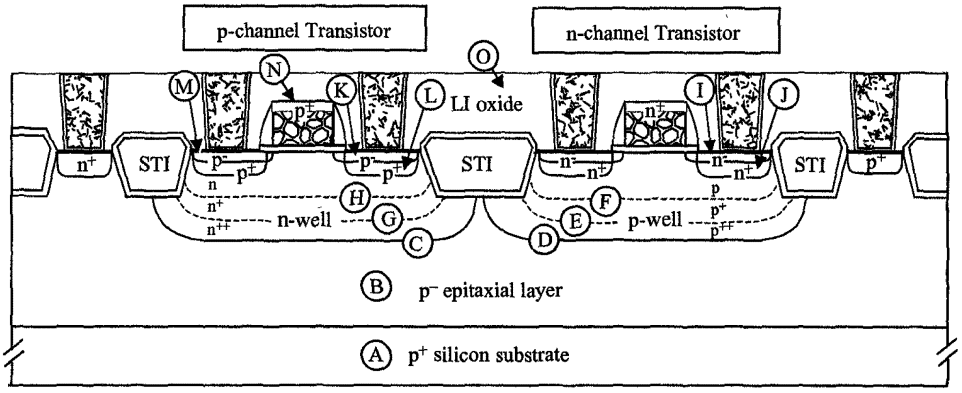


FIGURE 17.1 CMOS Structure with Doped Regions

TABLE 17.2* Common Dopant Processes in Wafer Fabrication

Process Step	Common Dopant Species	Ion Implant or Diffusion	Remarks
A. p^+ Silicon Substrate	B	Diffusion	The monosilicon crystal is doped during the crystal growing process.
B. p^- Epitaxial Layer	B	Diffusion	The epitaxial layer is doped by diffusion during epitaxial silicon growth.
C. Retrograde n-well	P	Ion Implant	Retrograde well has dopant profile with peak concentration buried at a certain depth. The dopant concentration decreases as it approaches the surface.
D. Retrograde p-well	B	Ion Implant	Retrograde well has dopant profile with peak concentration buried at a certain depth.
E. p-Channel Punchthrough	P	Ion Implant	Phosphorous implanted more laterally than source/drain implants to keep electric field of drain from punching through p-channel and reaching source region.

Process Step	Common Dopant Species	Ion Implant or Diffusion	Remarks
F. p-Channel Threshold Voltage (V_T) Adjust	P	Ion Implant	Implant phosphorous to adjust MOS V_T threshold voltage.
G. n-Channel Punchthrough	B	Ion Implant	Boron is implanted more laterally than source/drain implants to keep electric field of drain from punching through n-channel and reaching source region.
H. n-Channel V_T Adjust	B	Ion Implant	Implant boron through oxide layer to adjust MOS threshold voltage.
I. n-Channel Lightly Doped Drain (LDD)	As	Ion Implant	Low-dose implant of arsenic in region adjacent to the n-channel to improve electrical performance by reducing the peak electrical field and therefore hot carriers, which minimizes interface charges trapped in the gate oxide.
J. n-Channel Source/Drain (S/D)	As	Ion Implant	Higher implant dose of arsenic to form n-channel source and drain.
K. p-Channel LDD	BF_2	Ion Implant	Low-dose implant of boron in region adjacent to the p-channel to improve electrical performance between drain and channel region.
L. p-Channel S/D	BF_2	Ion Implant	Higher implant dose of boron to form p-channel source and drain.
M. Silicon	Si	Ion Implant	Implant with nondopant atom to amorphize silicon to reduce transient enhanced diffusion (TED) and channeling effects.
N. Doped Polysilicon	P or B	Ion Implant or Diffusion	Doping of polysilicon gate electrode to make conductive.
O. Doped SiO_2	P or B	Ion Implant or Diffusion	Doped oxide to obtain material benefits (e.g., create better flow and serve as getter).

*Adapted from E. Rimini, *Ion Implantation: Basics to Device Fabrication,* (Boston: Kluwer Academic Publishers, 1995).

Ion implantation typically follows photolithography in the general process flow (see Figure 17.2 on page 478); although, there may be some processes that call for the use of an etched-oxide layer to serve as a mask during either diffusion doping or ion implant. In this case, wafers could flow from etch to diffusion or ion implant. Ion implantation plays a crucial role in chip performance improvement because of the need for smaller dimensions. Transistor performance is increasingly dependent on precise doping profiles in the silicon that are achievable only with ion implant.

Doped Regions

Recall from Chapter 4 that a wafer is uniformly doped with dopant atoms during the crystal growth process to create a p-type or n-type wafer. The type of dopant depends on the manufacturer's specification. During wafer fabrication, dopants are selectively introduced to create the devices on the individual wafers. The selective introduction of dopants into masked openings on the wafer forms a *doped region* where dopants reside within the silicon crystal structure (see Figure 17.3 on page 478). The doped region is characterized by its *dopant profile,* which determines the amount of dopant actually added in the doped region as a function of depth.

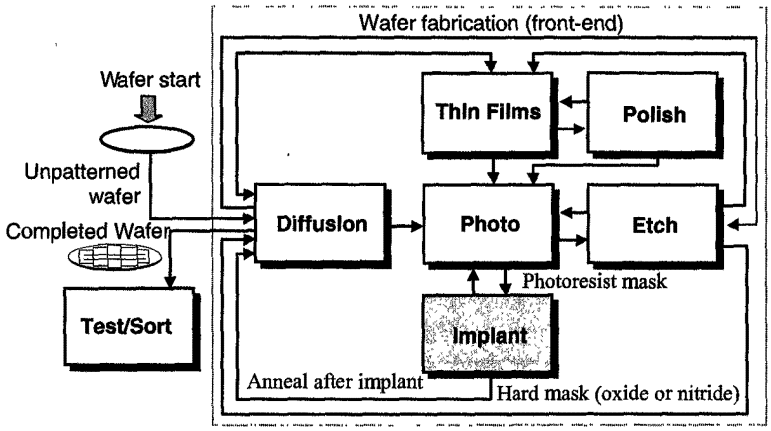


FIGURE 17.2 Ion Implant in Wafer Process Flow
(Used with permission from Advanced Micro Devices)

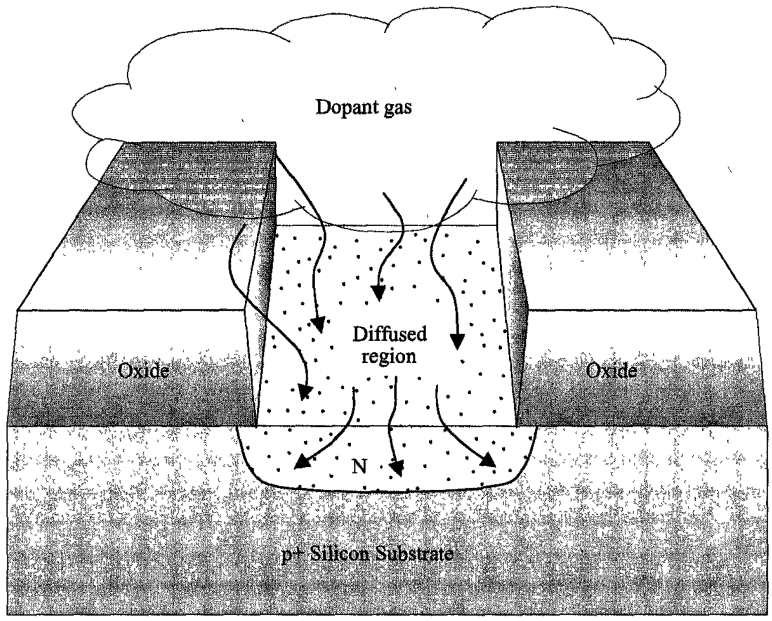


FIGURE 17.3 Doped Region in a Silicon Wafer

The dopant atoms enter the solid silicon through an oxide mask opening. In ion implantation, this mask is often photoresist, but a variety of masks can be used since it is a low-temperature process. Doping by diffusion requires an oxide or nitride mask because this technique is done in a high-temperature furnace.

The doped region can be of the opposite type as the silicon substrate, such as an n-type doped region in a p-type wafer, or it can be the same type with a different dopant concentration (e.g., a heavily doped p^+ region in a p-type wafer). The location where the conductivity of the doped region makes a change from p-type to n-type, or vice versa, is the pn junction. The exact depth in the wafer where the p-type dopant meets the n-type dopant is the *junction depth*, x_j. At the precise location of the junction depth, the concentration of electrons equals the concentration of holes. Another way of looking at this feature is the net dopant concentration at x_j is zero.

The ultimate interest in wafer doping is related to the individual dopant profiles for the devices after all processing is complete. A wafer undergoes many thermal excursions during processing, such as oxide growth, CVD, and so on, all contributing to undesirable dopant diffusion through the silicon. Dopant diffusion can alter critical parameters (e.g., junction depth and concentration) of the initial doped region and affect device performance. This is an important reason for minimizing the wafer thermal budget.

The main focus of this chapter will be doping by ion implantation. We will first review diffusion to analyze basic concepts and explain how intentional and unintentional diffusion occurs in wafer fabrication.

DIFFUSION

Diffusion is a basic property of matter that describes the movement of one material through another. Diffusion occurs from a region of relatively higher concentration into a region of lower concentration, resulting from the motion of atoms, molecules, or ions. In semiconductor fabrication, high-temperature diffusion is the mechanism used to move a dopant through the silicon crystal lattice. Diffusion can occur as a gas-state, liquid-state or solid-state. An example of liquid-state diffusion is a drop of food colorant in a glass of water. The highly concentrated drop of colorant immediately starts to diffuse into the glass of water and will continue until the entire volume of water is the same color as the drop of colorant. The same type of diffusion occurs in the solid-state when a high concentration of dopant material is introduced to a wafer. The dopant material diffuses through the silicon atoms of the solid crystal lattice.

Diffusion Principles

Thermal diffusion of a solid-state dopant in silicon requires three steps: predeposition, drive-in, and activation. During *predeposition,* or *predep,* wafers are loaded into a high-temperature diffusion furnace and a quantity of dopant atoms is transferred from the source cabinet to the diffusion furnace. The furnace temperature setting is typically 800 to 1100°C for 10 to 30 minutes. The dopants are introduced into a very thin layer of the wafer while maintaining a constant concentration of dopants at the surface. A thin oxide layer, referred to as a *cap oxide,* is grown on the surface to prevent dopant atoms from diffusing out of the silicon. The total number of dopant atoms deposited is referred to as *Q*. Note that for ion implantation (discussed later in this chapter), Q is referred to as the dose and also represents the number of dopant atoms implanted.

The predeposition step establishes the concentration gradient for the entire diffusion process. The concentration of dopants is highest at the surface and reduces when moving away from the surface, forming a gradient (or slope). This slope establishes the dopant profile, which can be mapped using four point probes (see Chapter 7). *Fick's laws,* first postulated in 1855, mathematically describe the diffusion process. These laws state in part that the number of particles moving through a cross-sectional area is proportional to the concentration gradient.[2] Fick's laws are used to predict the dopant concentration at some distance, *x*, from the surface.

The second part of thermal diffusion is the *drive-in* step. This is a high-temperature process (1000 to 1250°C) used to move the deposited dopants through the silicon crystal to the desired junction depth in the wafer. No additional dopants are added to the wafer. However, the wafer surface oxidizes in the high-temperature environment, which affects the diffusion of the dopant atoms during drive-in. Some dopants, such as boron, tend to move into the growing oxide layer while others, such as phosphorous, are pushed away from the SiO_2. This modification of dopant concentration due to the silicon surface oxidation is termed *redistribution.*

The third part of thermal diffusion is the *activation* step. Here the temperature of the furnace is raised slightly higher to enable the dopant atoms to bond with the silicon atoms in the lattice structure. This action activates the dopant atoms, which changes the conductivity of silicon.

Dopant Movement ■ Each dopant has a particular *diffusivity* in silicon, which represents the rate (or speed) that the dopant moves in the wafer. The higher the diffusivity, the faster the dopant moves. Diffusivity increases with temperature, which is reflected in a term known as the *diffusion coefficient, D,* of the dopant being diffused. Elements have different diffusion coefficients within the temperature range of the drive-in step that reflect whether they are fast or slow diffusers in silicon. The diffusion coefficient is an equation variable in Fick's laws used to predict the final dopant concentration in silicon.

Within the wafer, dopant atoms move by two different mechanisms: interstitional and substitutional (see Figure 17.4 on page 480). Dopants with high diffusivity, such as gold (Au), copper (Cu), and nickel (Ni), use primarily *interstitional movement* to move between the interstitial space

between regular crystal sites of the silicon lattice. Slower moving dopants, such as arsenic and phosphorus that are common in semiconductor doping, typically use *substitutional movement* where atoms fill empty crystal positions in the lattice.

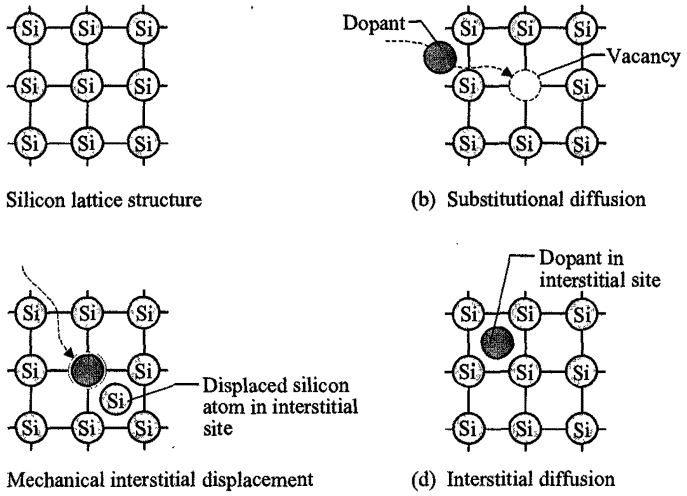


FIGURE 17.4 Dopant Diffusion in Silicon

Dopants are useful to form semiconductor silicon only if they are *activated dopants,* meaning they are part of the silicon lattice structure. An activated dopant can act as a donor or accepter of electrons and is an n-type or p-type dopant with respect to silicon. If the dopant occupies interstitial space, then it is not activated and is ineffective as a dopant. Thermal energy moves dopants into the regular crystal sites, a process known as *crystal activation.* Activation is a regular part of diffusion because it occurs at a high temperature. For ion implant, crystal activation is done with an anneal step.

Solid Solubility ■ At a given temperature, there is a limit to how much dopant can be absorbed by the silicon. This is referred to as the *solid solubility limit.* This is true for most materials, such as pouring salt into a container of water and watching it dissolve. If salt is continually added, at some point the solubility of the salt in the water reaches a limit where it no longer dissolves. Each particular dopant has a solid solubility limit (see Table 17.3). Note that only a fraction of the dopants in silicon are actually activated and contribute electrons or holes for conduction (about 3 to 5%).[3] Most dopants remain in interstitial sites and are electrically inactive.

TABLE 17.3* Solid Solubility Limits in Silicon at 1100°C

Dopant	Solubility Limit (atoms/cm^3)
Arsenic (As)	1.7×10^{21}
Phosphorus (P)	1.1×10^{21}
Boron (B)	2.2×10^{20}
Antimony (Sb)	5.0×10^{19}
Aluminum (Al)	1.8×10^{19}

*SEMATECH "Diffusion Processes," *Furnace Processes and Related Topics* (Austin, TX: SEMATECH, 1994), p. 15.

Lateral Diffusion ■ The diffusion mask is either silicon dioxide (SiO_2) or silicon nitride (Si_3N_4) since a photoresist mask could not withstand the high-temperature process. When atoms diffuse into the wafer, they move in all directions: down into the silicon, laterally, and back out of the wafer. *Lateral diffusion* occurs when dopant atoms travel in a direction along the surface of the wafer. Typically, lateral diffusion during a thermal diffusion process is 75 to 85% of the vertical junction

depth.[4] Lateral diffusion is undesirable in advanced MOS circuits because it can cause a reduction in the channel length, affecting device density and performance.

Diffusion Process

The objective of the diffusion process is to bring the diffusing impurity in contact with a wafer and maintain the specified time and temperature for diffusion to occur. Diffusion takes place in high-temperature diffusion furnaces, discussed in Chapter 10. Typically, one furnace is used for the predeposition, drive-in, and activation steps. Quartz and other furnace parts used in diffusion processes should be segregated from other furnace processes to avoid cross-contamination.

Diffusion should produce reproducible results from run-to-run and wafer-to-wafer. The eight steps required to properly perform diffusion in wafer fabrication are:

1. Run qualification test to ensure the tool meets production quality criteria.
2. Verify the wafer properties using a lot control system.
3. Download the process recipe with the desired diffusion parameters.
4. Set up the furnace, including a temperature profile.
5. Clean the wafers and dip them in hydrofluoric (HF) to remove native oxide.
6. Perform predeposition: load wafers into the deposition furnace and diffuse the dopant.
7. Perform drive-in: increase the furnace temperature to drive-in and activate the dopant bonds, then unload wafers.
8. Measure, evaluate, and record the junction depth and sheet resistivity.

The first six steps are done to prepare wafers for diffusion in the drive-in operation of step 7. A qualification test (or "qual") is performed on the furnace. This test determines the tool's production worthiness in terms of particles and other specified criteria. Once the tool is proven production worthy, the appropriate wafer lots are identified and the proper process recipe is downloaded to the furnace. A thermal profile should always be done to verify furnace temperatures are correct for the process to be performed. In a production environment, a given furnace is dedicated to a specific process step and is maintained at the precise temperature profile.

Wafer Cleaning ■ Wafer cleaning is critical because contaminants can block the diffusion of the dopant atoms into the wafer. Wafers should be cleaned immediately prior to loading the wafers into the furnace to minimize wafer contamination (e.g., native oxide). Cleaning typically includes an immersion in an acid and oxidizer, followed by an etch in an HF solution to remove any remaining oxides (see Chapter 6 for wet cleaning). The use of a dilute HF solution is referred to as a *deglaze* step to remove the poor quality native oxide on the wafer surface.

Dopant Sources ■ Although they may have been used in the early days of the semiconductor industry, it is impractical to use pure elements as a dopant source for submicron IC manufacturing. For instance, boron and phosphorus are solids at room temperature with low vapor pressures, making them difficult to melt or vaporize. Dopant concentration is also difficult to control when using a solid dopant source. Dopants are typically supplied as a gaseous or liquid source in the form of a compound. Some of the most common dopants are listed in Table 17.4 on page 482.

A liquid source (bubbler) has a carrier gas (e.g., nitrogen) bubbled through it and is delivered to the furnace tube as a vapor. Oxygen is also supplied for the dopant source to react and form oxides. Using boron as an example, the boric oxide undergoes a second reaction with silicon to form a boron-rich silicon dioxide layer on top of the wafer. This layer serves as the local source of boron for the predeposition step. The following two reaction equations illustrate how the diborane source is converted into a boron dopant:[5]

1st Reaction:	B_2H_6 (gas) *diborane*	+	$3O_2$ (gas) *oxygen*	→	B_2O_3 (solid) *boric oxide*	+	$3H_2O$ (liquid) *water*
2nd Reaction:	$2B_2O_3$ (solid) *boric oxide*	+	3Si (solid) *silicon*	→	4B (solid) *boron (dopant)*	+	$3SiO_2$ (solid) *silicon dioxide*

TABLE 17.4* Typical Dopant Sources for Diffusion

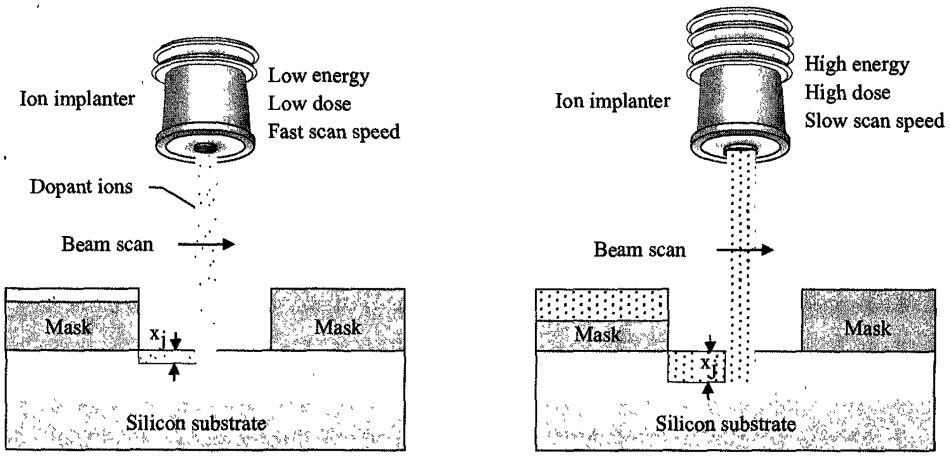
Dopant	Formula of Source	Chemical Name
Arsenic (As)	AsH_3	Arsine (gas)
Phosphorus (P)	PH_3	Phosphine (gas)
Phosphorus (P)	$POCl_3$	Phosphorus oxychloride (liquid)
Boron (B)	B_2H_6	Diborane (gas)
Boron (B)	BF_3	Boron tri-fluoride (gas)
Boron (B)	BBr_3	Boron tri-bromide (liquid)
Antimony (Sb)	$SbCl_5$	Antimony pentachloride (solid)

*SEMATECH "Diffusion Processes," *Furnace Processes and Related Topics,* (Austin, TX: SEMATECH, 1994), p. 7.

Gaseous sources are delivered to the furnace directly from the gas cylinder through a mass flow controller. The dopant is diluted in the cylinder with an inert gas to help prevent system corrosion and control the flow of the gas. A point-of-use filter should always be used to prevent fine particulates from getting into the furnace. Some diffusion sources are highly toxic, especially the gaseous sources. The most toxic of the commonly used dopant sources are arsine (AsH_3) and diborane (B_2H_6). Proper storage and usage is required at all times, especially to avoid a gas leak.

ION IMPLANTATION

Ion implantation is a method for introducing controlled amounts of dopants into the silicon substrate to change its electronic properties. It is a physical process—there are no chemical reactions. A number of applications use ion implantation in modern wafer fabrication (see Table 17.2 on page 476). The main application of ion implantation is the doping of semiconductor materials. Each doping application has specific requirements for the concentration of the dopant material and its depth. Ion implantation is preferred over diffusion in nearly all applications because of its ability to repeatedly control dopant concentration and depth. It has become a critical process to meet the challenges of wafer fabrication with sub-quarter micron feature sizes and larger diameter wafers (see Figure 17.5).



(a) Low dopant concentration (n^-, p^-) and shallow junction (x_j)

(b) High dopant concentration (n^+, p^+) and deep junction (x_j)

FIGURE 17.5 Controlling Dopant Concentration and Depth

Overview

Ion implant processing is done in one of the most complex semiconductor processing tools, called the *ion implanter* (see Figure 17.6). The implanter has an ion source component that creates positive-charged dopant ions from a source material. The ions are extracted and then separated in a mass analyzer to form a beam of the desired dopant ions. The number of ions in the beam is related to the concentration of dopants introduced into the wafer. The beam of ions is accelerated in a voltage field to attain a high velocity (on the order of 10^7 cm/sec).[6] Because of the high velocity, the ions have kinetic energy that is used to implant the dopants into the silicon crystal lattice structure of the target wafer. The beam scans the wafer to provide uniform doping across the wafer surface. Implantation is followed by a thermal anneal step to activate the dopant ions in the crystal structure. All implanter processing is done in a high vacuum.

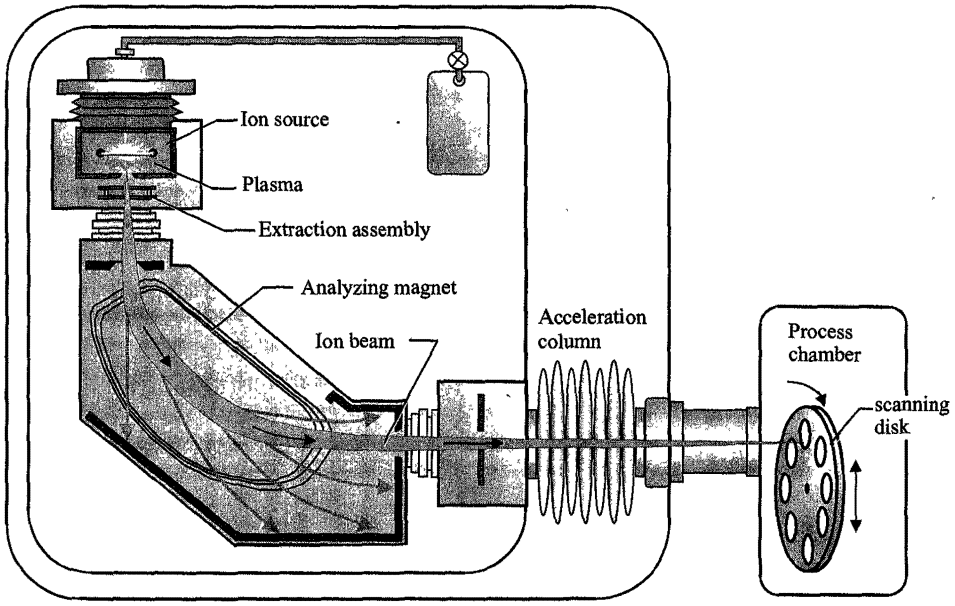
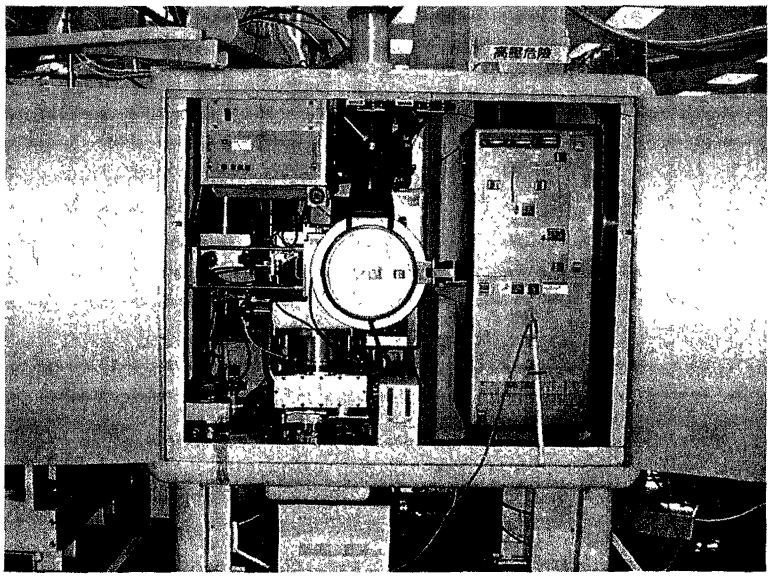


FIGURE 17.6 General Schematic of an Ion Implanter



Ion Implanter (Photo courtesy of Varian Semiconductor Equipment, VIISion 80)

There are two major goals for sub-0.25 μm doping requirements:

1. To introduce a uniform, controlled amount of a specific dopant into the wafer
2. To place the dopants at a desired depth.

Advantages of Ion Implant ■ The primary advantages of ion implantation are listed in Table 17.5. These benefits effectively increase the process flexibility for fabricating wafers with sub-quarter micron technology.

TABLE 17.5 Advantages of Ion Implantation

Advantages	Description
1. Precise control of dopant concentration.	Ability to precisely control the number of implanted dopants over a wide range of concentrations, from 10^{10} to 10^{17} ions/cm^2, and controlled to within ±2% over this range. In contrast, diffusion can control dopant concentration to within 5 to 10% at high concentrations and becomes less effective at low concentrations.
2. Good dopant uniformity.	Controls dopant uniformity by scanning the ion beam over a large wafer area, which is critical for smaller feature sizes on larger wafers.
3. Good control of dopant penetration depth.	Controls the ion energy during the implant to achieve good control of dopant penetration depth. This permits design flexibility, such as buried layers where the maximum dopant concentration is at the buried layer and the minimum concentration is at the wafer surface.
4. Produces a pure beam of ions.	Mass separation techniques produce a pure beam of ions free of contamination. Different impurities can be selected for implantation. It is done in a high vacuum that minimizes contaminants.
5. Low temperature processing.	Implantation is performed at moderate temperatures (<125°C) which permits the use of a variety of masks, including photoresist.
6. Ability to implant dopants through films.	Dopants can be implanted through films, such as an oxide or nitride. This condition allows adjustment of the threshold voltage of MOS transistors after the gate oxide is grown. It increases the flexibility to implant at various stages of the process.
7. No solid solubility limit.	The dopant concentration during implantation is not limited by the solid solubility limit of the silicon wafer.

Disadvantages of Ion Implant ■ The major disadvantage of ion implantation is the damage done to the crystal structure when the energetic dopant ions bombard the silicon host atoms. As the high-energy ions enter the crystal and collide with substrate atoms, energy is transferred and some silicon atoms are displaced from the lattice. This action is referred to as *radiation damage.* Most or all of this crystal damage is corrected with a high-temperature anneal step.

Another drawback of implantation is the complexity of the implanter equipment. However, this drawback is offset by the implanter's capability for dose and depth control and overall process flexibility.

Ion Implant Parameters

Ion implant is a flexible process that must meet stringent chip design and productivity requirements for wafer fabrication. The important ion implant parameters are:

- Dose
- Range

Dose ■ The *dose* (Q) is the number of implanted ions per unit area of wafer surface, with units of atoms/cm^2 (also stated as ions/cm^2). To count the implanted ions, Q is calculated by the following dose equation:

$$Q = \frac{It}{enA}$$

Where, Q = dose in atom/cm^2
I = beam current in coulombs/sec (amperes)
t = implant time in seconds
e = electronic charge equal to 1.6×10^{-19} coulombs
n = charge per ion (for instance, B^+ is equal to 1)
A = area implanted in cm^2

One of the main reasons why ion implantation is so important in wafer fabrication is its ability to repeatedly put the same dose into each wafer. The implanter does this by virtue of the positive charge on each ion. When formed into a beam, the flux of positive dopant ions represents a *beam current* measured in milliamps (mA). A low-to-medium beam current is from less than 0.1 mA up to about 10 mA, while a high beam current is from about 10 mA up to approximately 25 mA. As seen in the equation above, the magnitude of the beam current is a key variable for defining the dose. If the beam current increases, then more dopant atoms are implanted per unit time. A high beam current is often desirable to increase wafer throughput (more ions are implanted per unit time of production), but can also create uniformity problems.

Range ■ The ion *range* is the total distance an ion travels in the silicon during ion implantation. To characterize range it is necessary to understand energy. When the ions are accelerated due to electric potential difference to a high velocity, they gain energy. The ion energy is kinetic energy (KE) due to its motion, and it typically is expressed in units of joules. However, for ion implantation, the energy is usually stated in terms of the number of the electronic charge times the difference in potential, or electron volts (eV). The equation that describes this energy is:

$$KE = nV$$

Where, KE = energy in electron volts (eV)
n = charge state of the ion (e.g., "+" = 1, "++" = 2)
V = voltage difference in volts

For example, if an ion with a single positive-charge state moves in an electric field with a voltage difference of 100,000 volts (100kV), then its energy is:

$$\begin{aligned} KE &= nV \\ &= (1)(100kV) \\ &= 100\ keV \end{aligned}$$

Higher implanter energy means the dopant atom will have an increased range and travel deeper into the wafer. Energy is important in implanters because of the need to control the range and, therefore, junction depth of the dopants. High-energy implanters have an energy greater than 200 keV and may be as high as 2 to 3 MeV. High-energy implant is used in applications such as deep retrograde wells and retrograde triple wells (see Table 17.6 on page 486). A retrograde well has higher doping concentrations deeper in the well than at the surface. Ultralow-energy implanters have energies presently down to about 200 eV to enable doping at very shallow depths for source/drain applications.[7]

There is a *projected range,* R_p, which is how far the implanted ions travel into the wafer, depending on the ion mass and energy, the target mass and the beam direction with respect to the wafer crystal structure (see Figure 17.7 on page 486).[8] At the same time, not all ions come to stop simply at the projected range; some stop at a shorter distance and others at a greater distance. Ions will also move in a lateral direction. Combining all these ion movements produces a distribution of distances traveled by the dopant atoms implanted in the wafer, referred to as *straggle,* or ΔR_p. The R_p (projected range) indicates how shallow or deep the junction depth can be formed, whereas the ΔR_p (straggle) represents the spread of the implanted species around R_p. As the implant energy of

TABLE 17.6 Classes of Implanters

Class of Implanter System	Description and Applications
Low/Medium Current	• Highly pure beam currents <10 mA. • Beam energy is usually <180 keV. • Most often the ion beam is stationary and the wafer is scanned. • Specialized applications of punchthrough stops.
High Current	• Generate beam currents >10 mA and up to 25 mA for high dose implants. • Beam energy is usually <120 keV. • Most often the wafer is stationary and the ion beam does the scanning. • Ultralow energy beams (<4keV down to 200 eV) for implanting ultrashallow source/drain junctions.
High Energy	• Beam energy exceeds 200 keV up to several MeV. • Place dopants beneath a trench or thick oxide layer. • Able to form retrograde wells and buried layers.
Oxygen Ion Implanters	• Class of high current systems used to implant oxygen in silicon-on-insulator (SOI) applications.

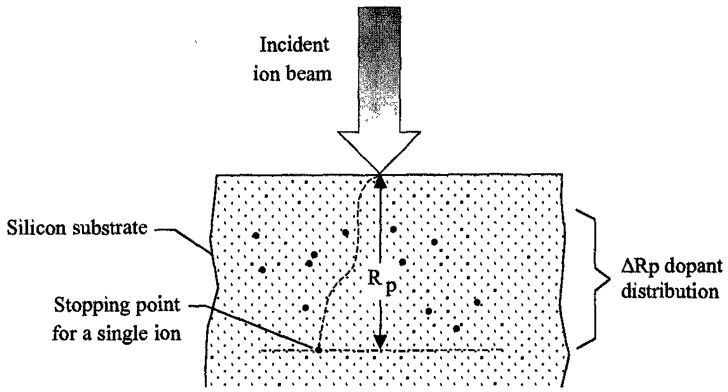


FIGURE 17.7 Range and Projected Range of Dopant Ion

dopant atoms increases, the projected range increases but the peak concentration of dopants decreases because the range straggling increases. Projected range charts are available that predict the projected range for a given implant energy (see Figure 17.8).

The implanted ions will travel some depth into the target wafer before they are brought to rest by energy loss due to collisions with silicon atoms (see Figure 17.9). The two primary energy loss mechanisms are electronic stopping and nuclear stopping.[9] *Electronic stopping* of dopant atoms is caused by interactions with the target electrons, similar to stopping a projectile in a thick medium, such as a child jumping into a pile of plastic balls. *Nuclear stopping* of implanted ions is caused by collisions between atoms that cause a displacement of silicon atoms. It can be visualized as the collision between two hard spheres, such as billiard balls. Depending on the ion mass and energy, an implanted atom can displace as many as 10^4 silicon atoms by nuclear collisions before coming to rest.[10]

The dopant moving through the silicon atoms creates a damage path in the crystal lattice, with the nature of the damage depending on whether the dopant ion is light or heavy (see Figure 17.10). A light dopant atom glances off silicon atoms with little energy transfer and is deflected through a large scattering angle. A heavy ion has a large energy transfer each time it strikes a silicon atom and is deflected through a relatively small scattering angle. Each displaced silicon atom also produces a large number of displacements.

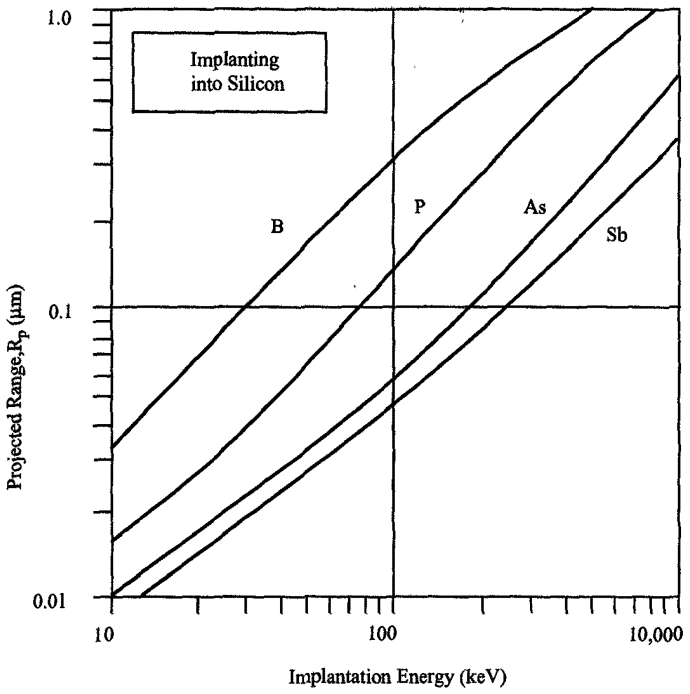


FIGURE 17.8 Projected Range Chart for Implant Energy
Redrawn from B. El-Kareh, *Fundamentals of Semiconductor Processing Technologies,* (Boston: Kluwer, 1995), p. 388.

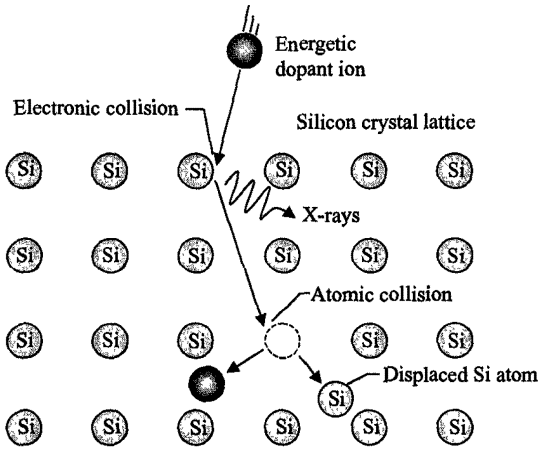


FIGURE 17.9 Energy Loss of an Implanted Dopant Atom

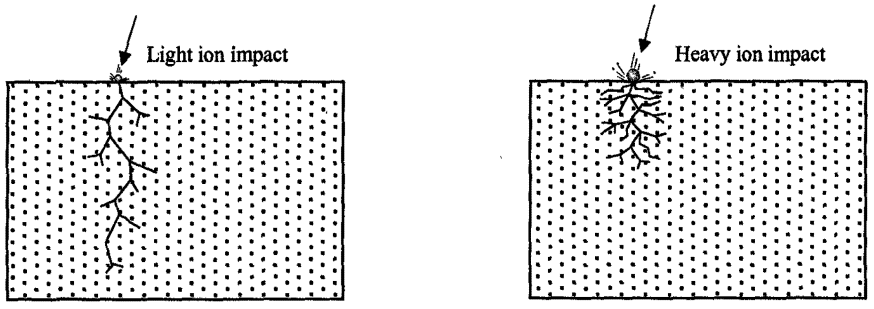


FIGURE 17.10 Crystal Damage Due to Light and Heavy Ions

ION IMPLANTERS

An ion implant tool consists of the following five major subsystems:

- Ion source
- Extraction electrode and ion analyzer
- Acceleration column
- Scanning system
- Process chamber

The ion source and extraction assemblies are generally mounted in the same vacuum chamber (see Figure 17.11). The ion source generates positive ions from a specific dopant gas or solid. The circular suppression electrode attached to the extraction assembly uses the electric field of a negative high voltage to draw the positive ions out of the ion source. Electromechanical controls on the extraction assembly aid in positioning the extraction electrode directly in front of the ion source plasma chamber. On older ion implanters, these controls could be manually adjusted from the operator's control panel. Today these controls are set by a process recipe and maintained by the tool's internal computer software.

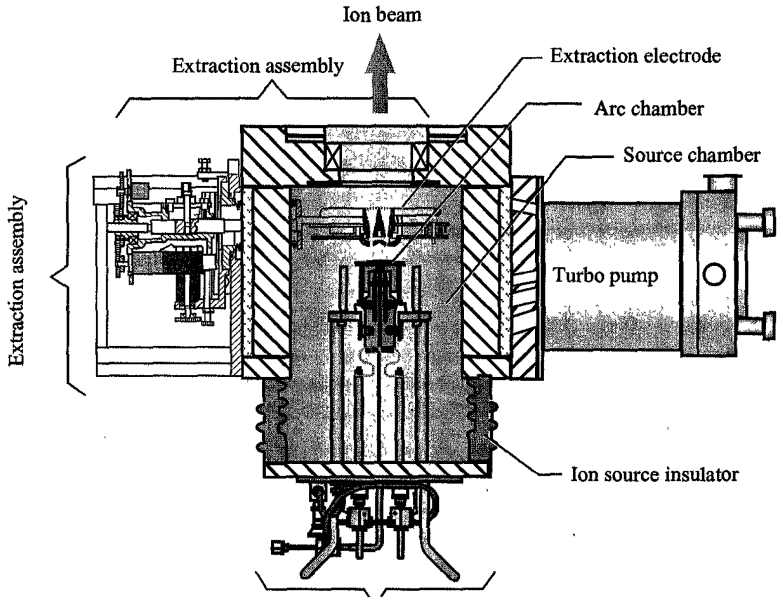


FIGURE 17.11 Ion Source and Extraction Assembly Housing
(Used with permission from Applied Materials, Inc., Precision Implanter 9500)

Ion Source

The species to be implanted must be present in the beam as a charged particle, or ion. Because of their electrical charge, ions can be controlled and accelerated with electric and magnetic fields. Ions for implantation are generated in an *ion source.* A positive ion is formed from a dopant gas source or by vaporizing a solid. Typically B^+, P^+, As^+, and Sb^+ are produced by ionization of atoms or molecules. The most common feed material for a source of dopant atoms is a gas, such as B_2H_6, BF_3, PH_3, and AsH_3. The gas is packaged in a relatively small cylinder (0.4 to 2.2 liters in size) and diluted with hydrogen to reduce the risks associated with inadvertent gas releases.

Another method of supplying the feed material is by heating and vaporizing a solid material, which is sometimes used to obtain arsenic (As) or phosphorus atoms from solid pellets.[11] The solid material is vaporized at about 900°C and the volatile dopant atoms are transported to the ion source chamber. No dilute hydrogen is added, which permits higher maximum beam currents. A disadvantage of a solid source is the long setup time, or tune time, which can be 40 to 180 minutes. Most

of this time is required to heat and stabilize the vaporizer. There is also the need for more frequent maintenance due to the buildup of sputtered materials on the beam-line components. However, many IC manufacturers prefer to use solid dopant sources because it is easier to deal with them from an environmental and safety standpoint.

Ion Creation ■ Ions are generated in the ion source by bombarding the feed gas atoms with electrons. Electrons are often produced by a simple and robust hot tungsten filament source. The *Freeman ion source* is one of the most common electron sources.[12] In this source the rod-shaped cathode filament is held inside an arc discharge chamber with a feed gas inlet. The walls of the arc chamber are the anode. When feed gas is introduced, a plasma is created around the filament in the arc chamber by passing a high current through the filament and applying a voltage of about 100V between the cathode and anode. Positive ions are produced by the collisions between energetic electrons and the feed gas molecules. An external source magnet applies a magnetic field parallel to the filament to increase ionization and to stabilize the plasma. During operation the current between the cathode and anode is adjusted, along with the feed gas, to maintain a stable plasma. A variation of the Freeman ion source is the Bernas ion source that uses a pigtail type of filament and a negative-charged reflector plate to improve electron confinement and efficiency (see Figure 17.12).

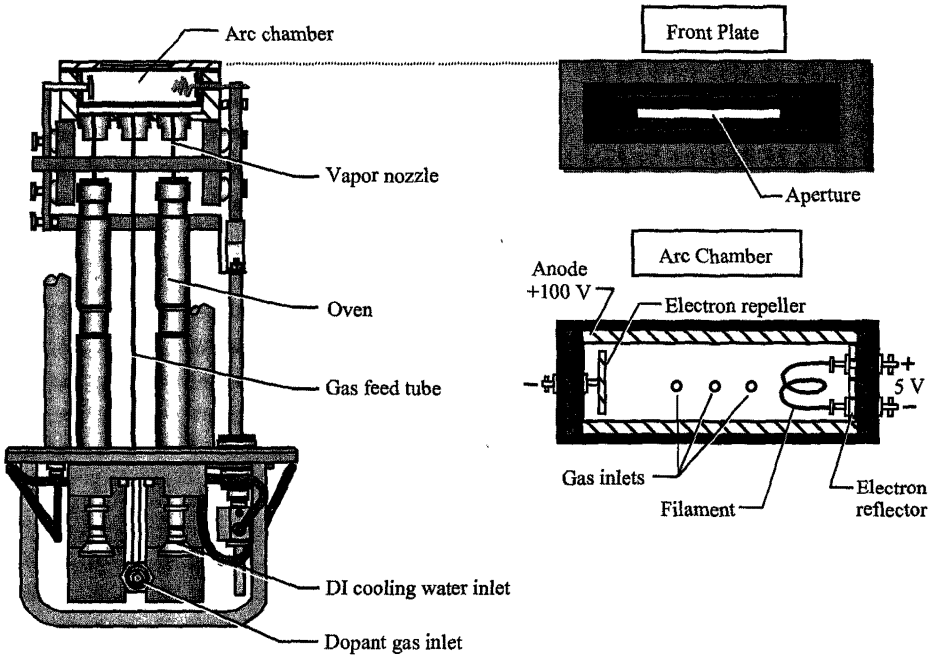


FIGURE 17.12 Schematic of Bernas Ion Source Assembly
(Used with permission from Applied Materials, Inc., Precision Implanter 9500)

The bombardment of electrons breaks up the feed gas molecule into different ion species. Boron trifluoride (BF_3) is often used as a feed gas because boron in its elemental form has a very low vapor pressure, requiring a temperature of 2000°C to vaporize it. BF_3 also has greater mass and lower diffusivity than boron, making it a preferred p-type dopant for forming shallow junctions. In the ion source, BF_3 is broken up into many different species (isotopes), such as B^+, B_{10}^+, B_{11}^+, BF^+, BF_2^+, F^+, and F_2^+. The B^+ ion is the atom desired to be implanted into the wafer and will be selected when the beam passes through the analyzer magnet.

There are alternative designs under evaluation for ion sources, such as an RF (radio frequency) ion source, cold cathode source, and microwave ion source. An RF source excites the feed gas molecules in a magnetic environment, generating a cooler plasma with the possibility of higher beam currents with a longer ion source lifetime.[13]

Extraction and Ion Analyzer

The traditional implanter extraction system collects all the positive ions created inside the ion source and forms them into a beam. The ions are extracted through a slit in the ion source. They are repelled by the positive bias arc chamber (anode) and are attracted to the negative bias (cathode) of the *extraction assembly* (see Figure 17.13). Since positive ions are like little magnets, each with a positive charge, they are attracted to a negative electric field. The higher the electric field, then the faster the ion will move. At the same time, the faster the ion moves, then the higher is its kinetic energy and the farther it will penetrate into the wafer when it strikes the surface. The negative bias of the extraction electrode also repels any stray electrons in the source plasma and forms the positive ions into a beam. A negatively biased *suppression electrode* is used to focus the ion beam into a parallel beam for efficient beam transport through the implanter. This condition is important for delivering high beam currents to wafers.

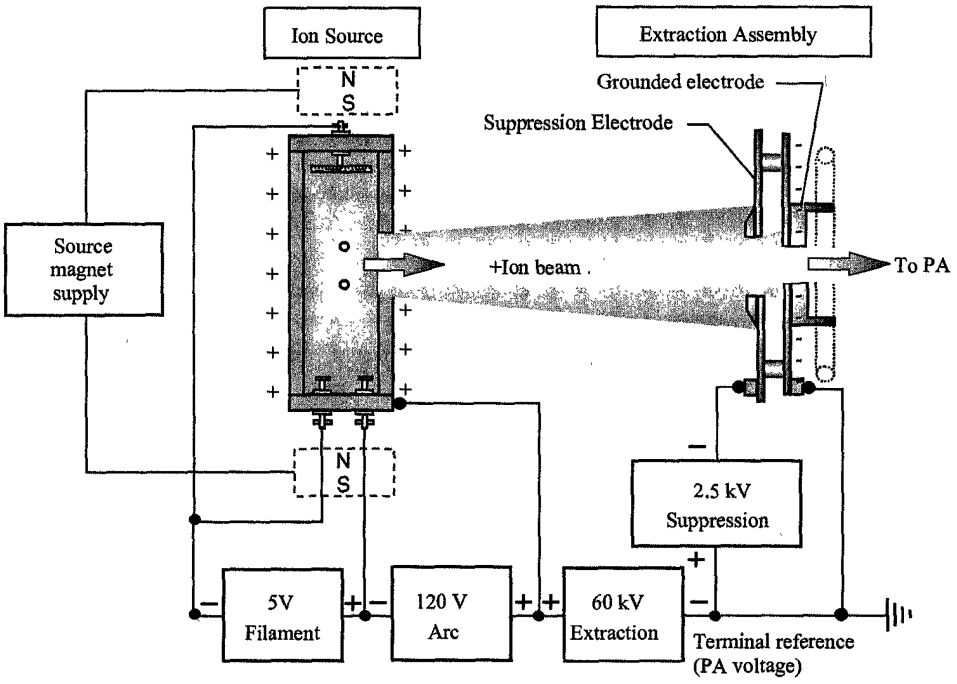


FIGURE 17.13 Interaction of Ion Source and Extraction Assemblies (Used with permission from Applied Materials, Inc., Precision Implanter 9500)

Mass Analyzer Magnet ■ The ions extracted from the source contain many different ion species and travel at a relatively high speed due to the acceleration provided by the extraction voltage. The species in the ion beam have different atomic mass units (amu). In ion implanters, a magnetic *ion analyzer* separates the desired dopant ion from the main body of ion species. As shown in Figure 17.14, the analyzer magnet is shaped in a 90° angle. The magnetic field of the analyzer magnet causes the ion species to be deflected into an arc. A spectrum of ions is formed based on their amu. For a given field strength, ions with heavy masses are not able to bend at the appropriate angle, while lighter ions bend too easily. There is one ion species, however, that bends just enough at the appropriate field strength to allow it to pass through the center of the analyzer magnet. This is the dopant species that eventually gets implanted into the wafer.

The radius of the arc formed by the ion depends on the mass of the individual species, its speed, the strength of the magnetic field, and the ion's electronic charge. The magnetic field strength is adjusted to match the desired path of the dopant ion. This desirable dopant ion passes through a slit at the end of the analyzer while all other ions strike the walls of the analyzing magnet.

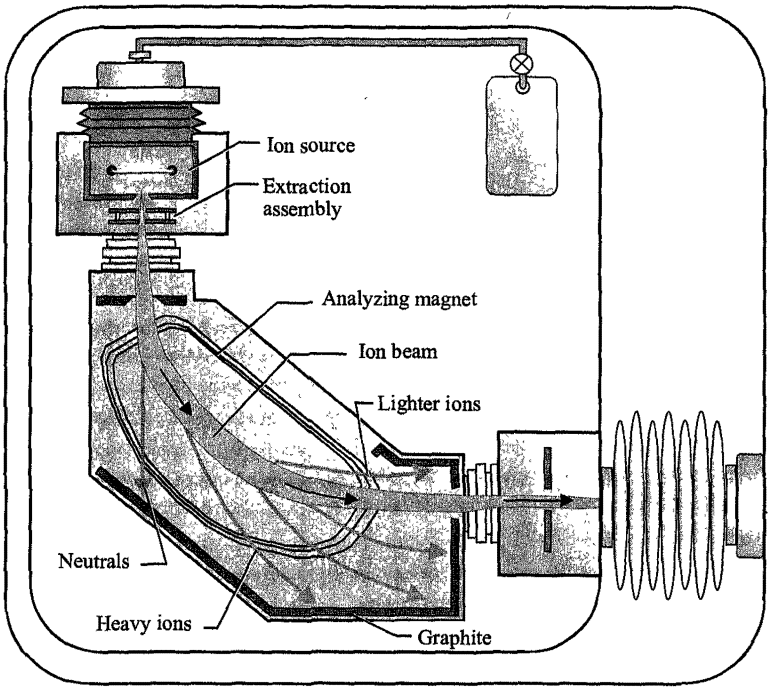
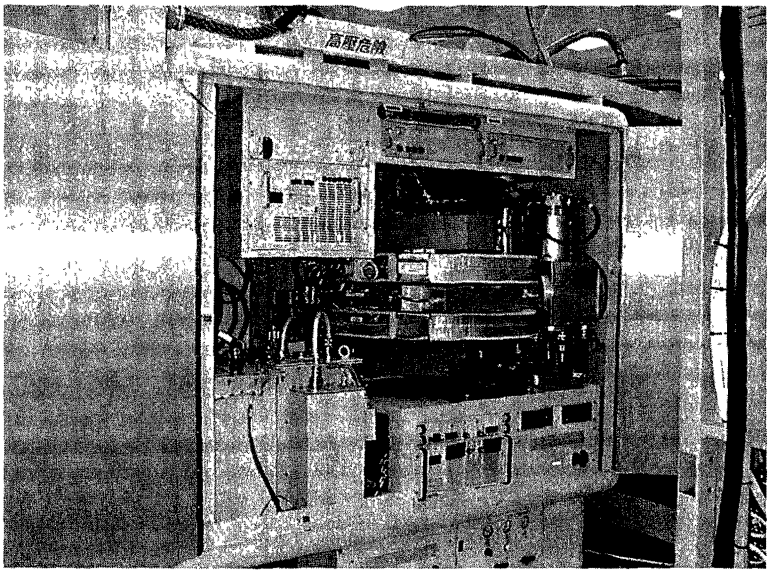


FIGURE 17.14 Analyzing Magnet



Ion Implanter Analyzing Magnet (Photo courtesy of Varian Semiconductor Equipment, VIISion 80)

Acceleration Column

To achieve additional ion acceleration (and therefore energy) beyond the analyzer magnet, positive ions are accelerated in an electric field inside an *acceleration column* (see Figure 17.15 on page 492). This acceleration column is a linear design made of a series of electrodes separated by insulators, each with an increasing negative charge. As the positively charged ions enter the column, they start accelerating. In this manner the total voltage difference in the electrode assembly and the acceleration column accelerates the dopant ions. The higher the total voltage, then the higher the velocity and, therefore, energy. Higher beam energy means the dopant ions are implanted deeper into the wafer, while lower beam energy is used for ultrashallow implants. Different beam energies relative to the dose are shown in Figure 17.16 on page 492.

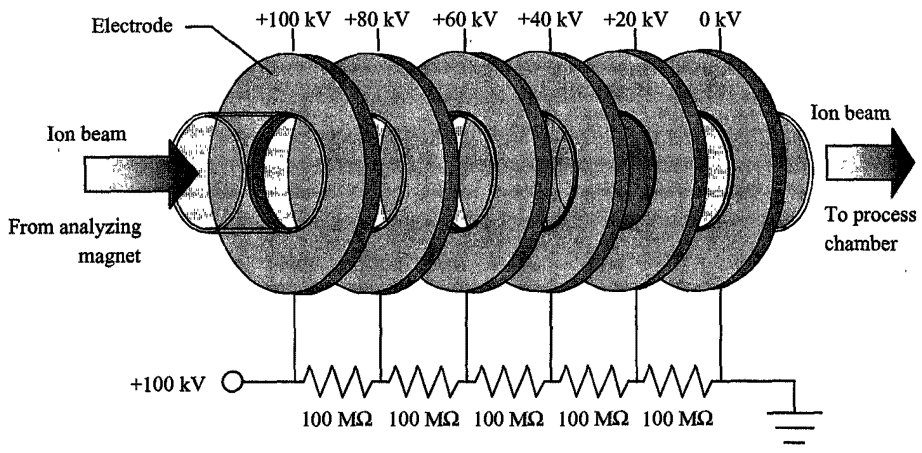


FIGURE 17.15 Acceleration Column

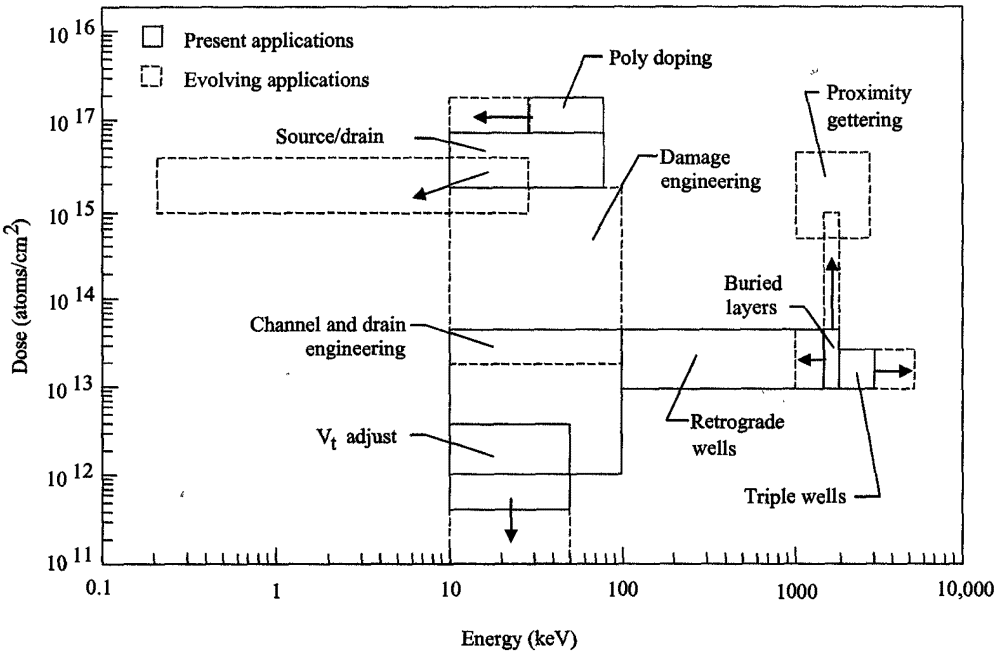


FIGURE 17.16 Dose Versus Energy Map
(Used with permission from Varian Semiconductor Equipment)

The dose versus energy map highlights the importance of energy (range) and dose (concentration) for ion implantation.[14] Beam energy defines the projected range that the ions are implanted in the wafer surface and varies from high energy (>200 keV and into multiple MeV) to low energy (<120 keV and down to 200 eV). Dose is directly related to the concentration of dopants in the wafer and is represented by the beam current, or number of ions in the beam, ranging from low, medium, to high current (>15 mA). Implanters are often classified according to their maximum operating beam current and acceleration energy.

Post-Accelerator ■ There is additional beam focusing that takes place in the *post-accelerator* component of the acceleration column. It typically uses quadrupole lens focusing based on four cylindrical poles in a two-lens system, employing electrostatic or magnetic repulsion to form the ion beam into a focused, circular beam.

High-Current and High-Energy Beam ■ High-energy implanters are used to implant buried dopant layers, such as for retrograde and triple wells. Most commercial high-energy ion implanters employ *linear accelerator* technology to accelerate ions to high velocity and obtain beam energies in excess of 200 keV and into the MeV range.[15] High beam current (up to 25 mA) is desirable to reduce the implant time and increase wafer throughput through the implanter. A linear accelerator is constructed as an alternating series of high-voltage (several 10 kV) electrodes and grounded quadrupole focusing lenses (see Figure 17.17). The timing of the voltage between each electrode and grounded quadrupole is set to match the arrival of the dopant ions at each gap. The ions are accelerated through the gaps, with the final energies up to 20 times higher than the maximum acceleration in a traditional beamline acceleration column. This condition avoids the use of extremely high voltages. The linear accelerator also aids in removing beam contaminants by reducing masses other than the desired species. A traditional bending magnet is located at the end of the linear accelerator that serves as an energy analyzer to ensure that a pure, monoenergetic beam is formed for wafer implant.

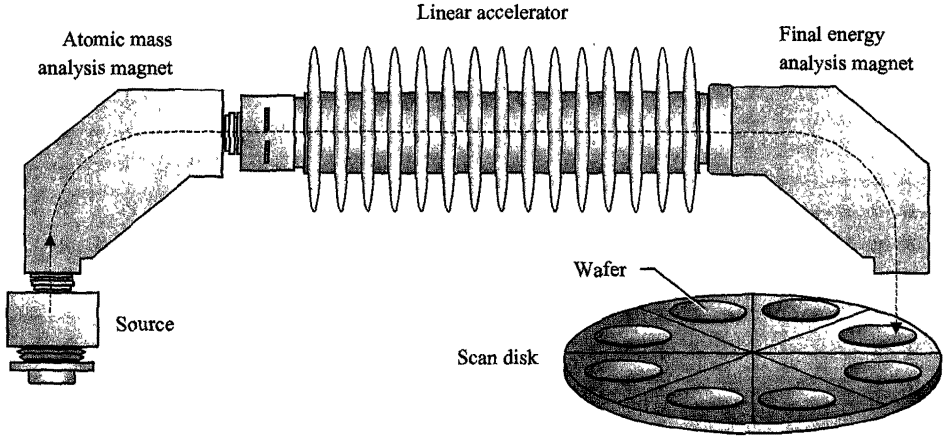


FIGURE 17.17 Linear Accelerator for High-Energy Implanters

High-Current and Low-Energy Beam ■ The need to form ultrashallow implants has promoted the development of high-current, low-energy beams. A low-energy beam accelerates ions to a low velocity so that their projected range is shallow in the target wafer. Maintaining a well-focused beam with low-energy acceleration is difficult because beam size is hard to control and usually increases with high current and low energy. Visualize this action by imagining a bowling ball rolled slowly down a bowling alley lane. It tends to veer to the side and into the gutter much more easily than a bowling ball rolled straight and fast. A method used to achieve a high beam current in a low-energy beam is *beam deceleration,* or *decel.*[16] With this approach, the beam is extracted from the ion source at a high energy and then decelerated down to the desired energy without loss of beam current. An electrode positioned farther down the beamline is used to decelerate the ions from the initial extracted energy. This approach may cause energy contamination of the beam if high-energy ions manage to pass through to the wafer. A variation to decel is the *differential lens,* which combines a short beam path and optimized optics to minimize beam current loss.

Space Charge Neutralization ■ A beam of only positively charged ions is inherently unstable, since like charges repel one another with mutual repulsion. This condition causes *beam blow-up,* meaning the diameter of the beam increases as the ions pass down the beamline, resulting in nonuniform implantation. Beam blow-up is minimized by ensuring that the positive ions in the beam are neutralized with secondary electrons, a condition referred to as *space charge neutralization.*

Secondary electrons are generated when high-energy dopant ions strike a surface (e.g., aperture plates or beam guide assembly) as they pass along the beamline. The secondary electrons become trapped within the beamline due to the negative-biased electrodes along the beam path, including the extraction electrode and the acceleration. The secondary electrons bounce back and forth between the negatively biased plates, unable to leave their specific region in the beamline. The trapped electrons serve to neutralize the beam and prevent or reduce beam blow-up (see Figure 17.18).

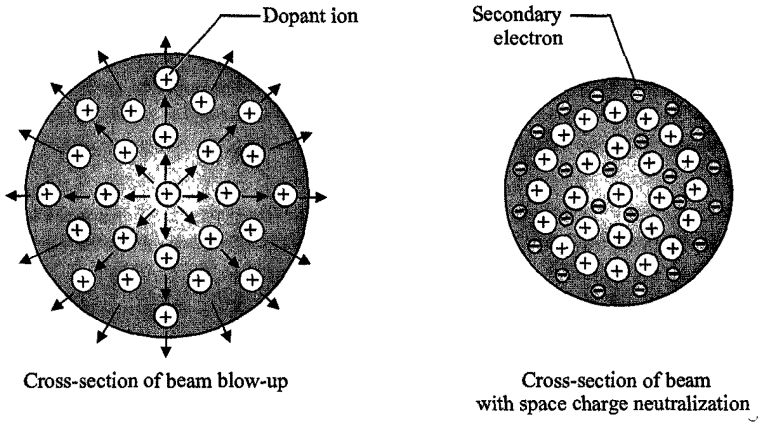


FIGURE 17.18 Space Charge Neutralization

Neutral Beam Trap ■ The positively charged ion beam is formed in a vacuum of less than 10^{-6} torr, but there are always residual gas molecules. Neutral ions are formed in the beam when a dopant ion gains an electron by colliding with a residual gas molecule. They cannot be deflected because of their lack of charge and, if not removed, they will be implanted. A *neutral beam trap* is created by placing a bend in the beamline a short distance before the target chamber using beam-bending electrodes. Since the neutral ions will not be deflected by the electrodes at the bend, they travel straight and collide with a grounded collector plate (see Figure 17.19).

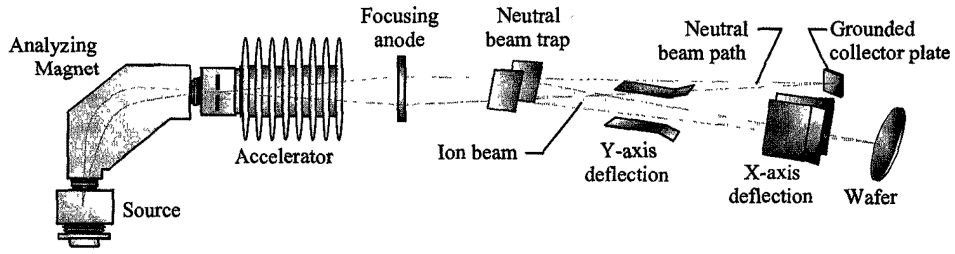


FIGURE 17.19 Neutral Beam Trap
(Used with permission from Varian Semiconductor Equipment)

Scanning System

The goal of the implanter is to form a highly pure ion beam from both a contamination and energy standpoint. This pure beam is implanted into the target wafer. That is, the beam has only the desired dopant ions at a predetermined energy level. Because the focused ion beam is typically small, on the order of 1 cm^2 for medium implanters and 3 cm^2 for high-current implanters, it must be scanned to cover the entire wafer. Wafer scanning is done either by moving the beam over a stationary wafer or moving the wafers through a stationary beam. Scanning plays a critical part in dose uniformity and repeatability.

Traditionally, low- to medium-current implanters keep the wafer stationary, while high-current implanters will keep the ion beam stationary. The different types of scanning systems used in implanters are:

- Electrostatic scanning
- Mechanical scanning
- Hybrid scanning
- Parallel scanning

Electrostatic Scanning ■ *Electrostatic scanning* deflects the ion beam across a stationary wafer by applying a specific controlling voltage to a set of X-Y electrodes (see Figure 17.20). When the polarity of one side of the electrodes is made negative, the positive ion beam will deflect toward it. By properly positioning the two sets of electrodes and constantly varying the voltage, the beam is made to deflect across a wafer. This type of scanning could be compared to spray painting a surface, where the spray needs to be worked back and forth many times to uniformly coat the surface. An electrostatic scan moves the beam across the wafer (x-axis) 15,000 times in one second while it scans up and down (y-axis) 1,200 times per second. Special care is made to ensure the scan is uniform at the outer edges of the wafer where the scan actually has to stop and reverse directions. In electrostatic scanning systems the wafer can be twisted and tilted relative to the ion beam to achieve desired junction characteristics.

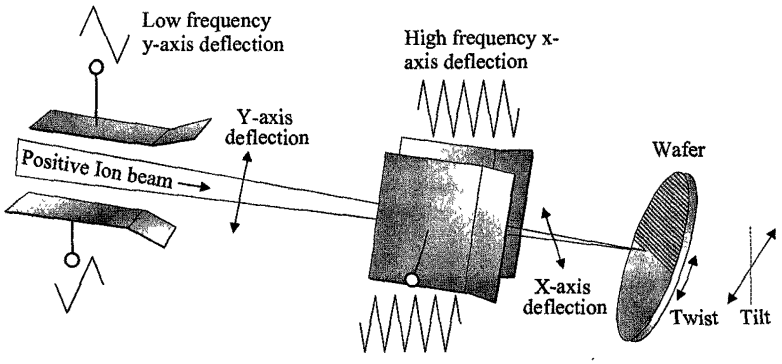
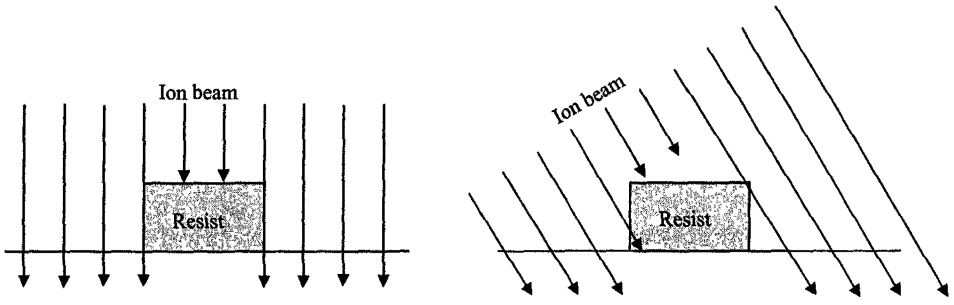


FIGURE 17.20 Electrostatic Ion Beam Scanning of Wafer

Implanting a single wafer at a time is referred to as a serial process and is generally used for low- to medium-current implant applications. In a typical low-current implant operation, a wafer might be scanned for 7 to 10 seconds to obtain uniform dose. Note that this same method of beam deflection can also be accomplished using an electromagnetic field approach instead of an electrostatic approach.

Because the wafer is held fixed during electrostatic scanning with no elaborate mechanical assembly, there is less possibility of particulate contamination. Another advantage to this type of scanning is that electrons and neutrals are not deflected and are eliminated from the beam. The major disadvantage is that the ion beam does not strike perpendicular to the wafer, which leads to undesirable shadowing from the mask material that partially blocks implantation of the ion beam (see Figure 17.21).



(a) Mechanical scanning with no tilt

(b) Electrostatic scanning with normal tilt

FIGURE 17.21 Implant Shadowing

Mechanical Scanning ■ With *mechanical scanning,* the ion beam is fixed and the wafers are mechanically moved through the beam. This method is generally used for high-current implanters because electrostatic beam deflection is difficult at high currents and energies. The beam size may be 1 cm wide by 3 cm high. Mechanical scanning is done by rotating multiple wafers (e.g., up to 25 200-mm wafers) fixed on the outer circumference of a large wheel assembly disk that is simultaneously moving up and down while rotating at 1000 to 1500 rpm (see Figure 17.22). The disk diameter may be 5 feet or larger. While the disk is spinning, it is also moved up and down so that the beam scans from the outer edge to the inner edge of the wafer. The disk can also be tilted relative to the ion beam to prevent channeling through the interstitial spaces of the silicon lattice (see the following section). Moving the wafers relative to the beam resolves any nonuniformity concerns from shadowing. Mechanical scanning is a batch process that effectively averages the beam power over a very large area. An advantage is the reduced wafer heating from the ion beam energy. Throughput is better than with electrostatic scanning. However, there are potentially more particles generated from the mechanical assembly.

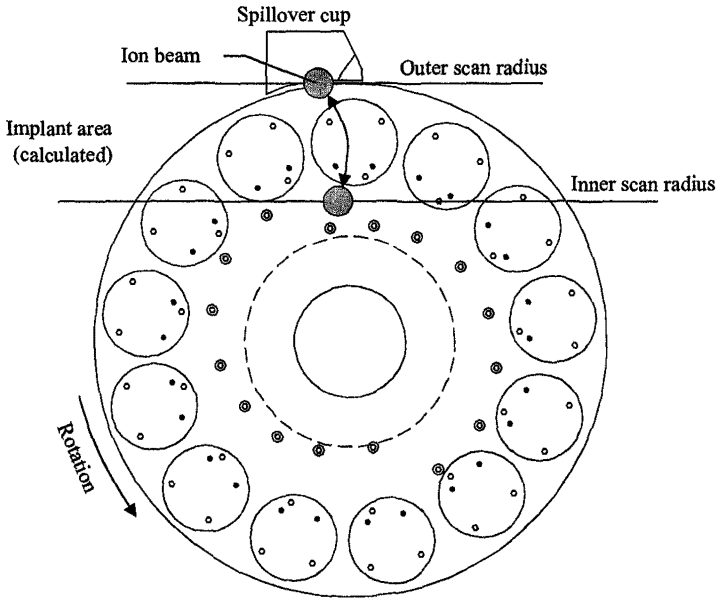


FIGURE 17.22 Mechanical Scanning of Implanted Wafers
(Used with permission from Varian Semiconductor Equipment, VIISion 80 Ion Implanter)

Hybrid Scanning ■ In the *hybrid scanning* system, the wafers are placed on a disk and rotated to scan in the y axis. The beam is then electrostatically (or electromagnetically) scanned in the x-direction. This method is generally used in a serial process for low- to medium-current with a single wafer.

Parallel Scanning ■ In electrostatic scanning, the beam is not scanned perpendicular to the wafer surface, which causes shadowing. *Parallel scanning* is a method used to reduce shadowing and channeling (see the following section) by scanning the ion beam to within $<0.5°$ of the wafer surface.[17] In the parallel scanning method, the beam is first scanned electrostatically. Then the beam passes through another set of magnets which corrects the beam angle and forces it to strike perpendicular to the wafer surface.

Wafer Cooling ■ The energy of the ion beam striking the wafer is converted into heat and will cause the wafer temperature to increase. Wafer cooling is used to control the temperature and prevent problems caused by heating, usually controlling the wafer temperature to $<50°C$. Photoresist will blister and flake off if exposed to temperatures above 100°C and will become difficult to remove during photoresist stripping.[18] This feature is especially critical during high-dose implantation. If the wafer temperature exceeds 300°C, the electrical properties of the device are affected and

partial annealing could occur that could alter the sheet resistivity of the wafer. Factors that affect how much the wafer temperature rises during implantation include ion beam energy, implant time, scan speed, and wafer size.

The two techniques in wide use for wafer cooling in ion implantation are gas cooling and elastomeric cooling.[19] For *gas cooling* the wafer is sealed against a platen (a cooled plate, often with internal circulating water) and a gas such as helium is introduced behind the wafer. The gas provides a thermal conduction path to carry heat from the wafer to the platen. In *elastomeric cooling,* the metal platen is covered with a thin layer of elastomer material. This elastomer is in contact with the backside of the wafer and conforms to the wafer surface to maximize heat transfer between the wafer and platen.

Wafer Charging ■ During implantation, as the ion beam strikes the wafer, some positive ions accumulate in the masking layer, causing *wafer charging.* This condition can lead to a significant electric charge buildup on the wafer, especially for high-current implanters. Such wafer charge buildup can change the charge balance in the ion beam and lead to beam blow-up, causing substantial dose variations across the wafer. Wafer charging can also damage a surface oxide, including damage to the gate oxide leading to device reliability problems.

Control of wafer charging has traditionally been done by flooding the surface of the wafer with low energy electrons using an electron shower known as *secondary electron flood* (see Figure 17.23). In this method, primary electrons with the energy of a few hundred eV are directed to a target located close to the ion beam path. When these primary electrons strike the target, a cloud of low-energy (<20 eV) secondary electrons is generated.[20] These secondary electrons are trapped by the ion beam and are used to neutralize positive charge buildup on the wafer surface. It is important that no high-energy primary electrons reach the wafer or damage may occur to gate oxides.

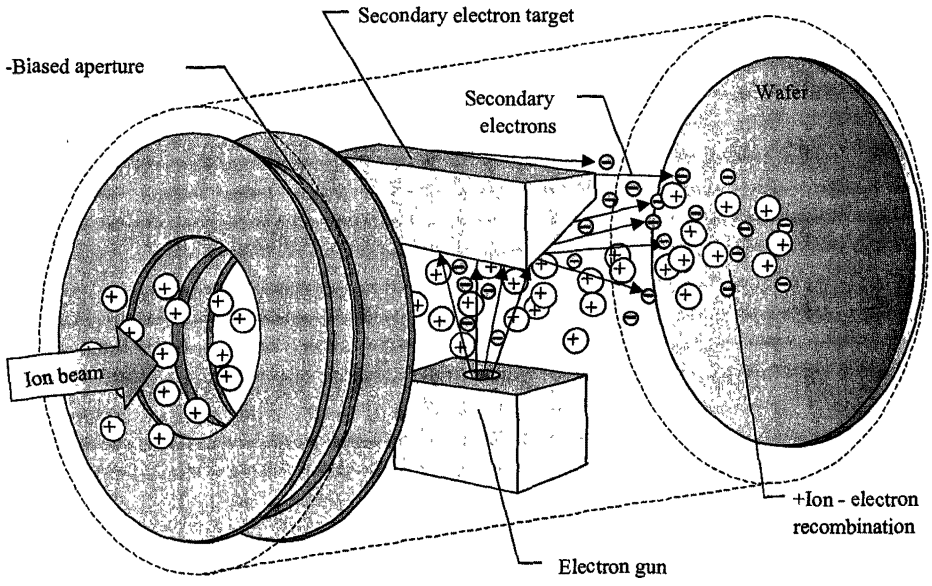


FIGURE 17.23 Electron Shower for Wafer Charging Control
(Used with permission and adapted from Eaton NV10 Ion Implanter, circa 1983)

Control of wafer surface charging is often done now by immersing the ion beam and wafer in a stable, high-density plasma environment, referred to as a *plasma electron flood* system.[21] It is based on the extraction of electrons from a plasma (usually Ar or Xe) maintained in an arc chamber located close to the beam path and wafer (see Figure 17.24 on page 498). The plasma is filtered so that only secondary electrons reach the wafer surface and neutralize the positive charge buildup. The main advantage of plasma flood over the electron shower is that no high-energy electrons are generated in the plasma, which means only low-energy electron energy is used. Plasma flood effectively reduces wafer charge buildup and damage.

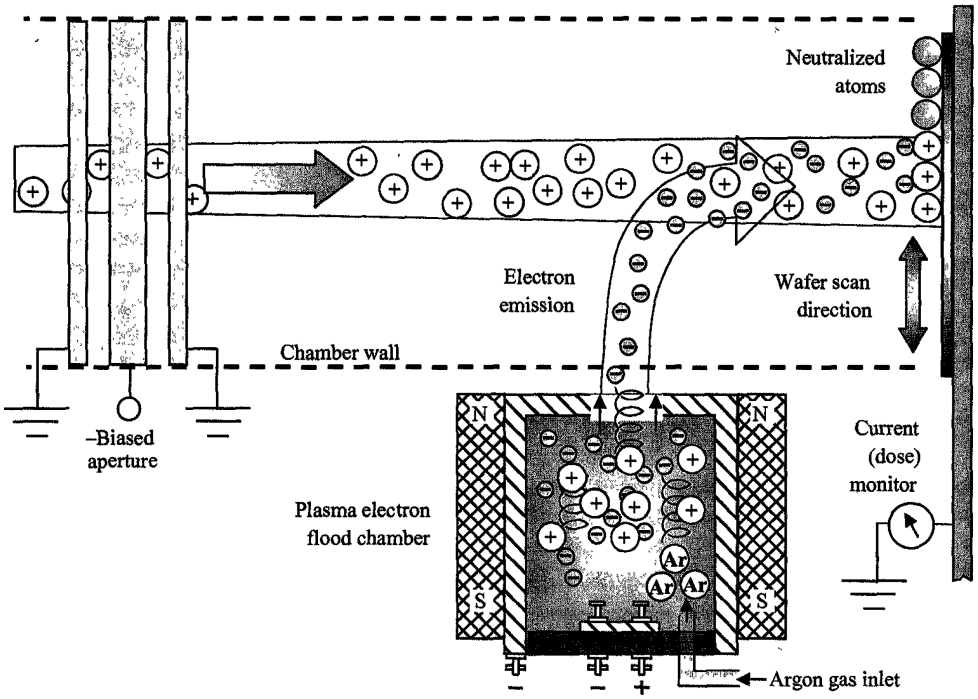
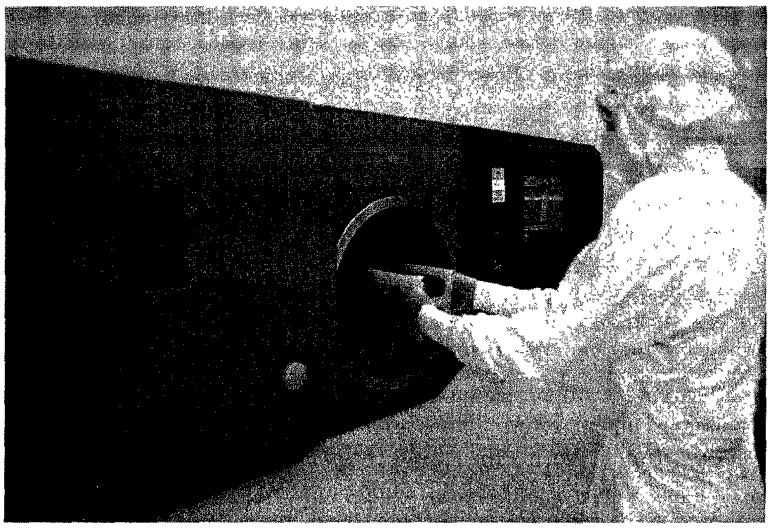


FIGURE 17.24 Plasma Flood to Control Wafer Charging

Process Chamber

The implantation of the ion beam into the wafer takes place in the *process chamber.* The process chamber is a major implanter subassembly that includes the scanning system (discussed above), *end station* with vacuum load locks for loading and unloading wafers, the wafer handler system, and the computer control system. There are also methods for dose monitoring and channeling control (see the following section). The end station can be large if used for mechanical scanning. It is pumped down to the vacuum required for implantation with multiple roughing, turbopumps, and cryopumps to reach base pressure (e.g., typically 10^{-6} torr).



End Station for Ion Implanter (Photo courtesy of International SEMATECH)

Load/unload systems in the end station use robotic handling to move wafers between an input station and the scanning disk in the target chamber (see Figure 17.25). Cassettes are loaded into the input rack and load locks are used to initially seal the input chamber. A roughing pump lowers the pressure around the cassettes. When pressure is low enough, a turbopump continues the pumpdown