

UPCOMING EVENTS

1. **30th IEEE European Test Symposium (ETS) 2025**
May 26 - May 30
2. **Electronic Components and Technology Conference (ECTC) 2025**
May 27 - May 30
3. **Ansys Optics Virtual Deep Dive: Stray Light Analysis**
May 27
4. **TSMC Europe Technology Symposium 2025**
May 27
5. **Webinar: Accelerating Automotive Design with Ansys Fluent Next-Gen Technologies**
May 28

SEARCH SEMIWiki

RECENT SYNOPSYS ARTICLES

The Road to Innovation with Synopsys 224G PHY IP From Silicon to Scale: Synopsys 224G PHY Enables Next Gen Scaling Networks

May 19, 2025

Webinar – Achieving Seamless 1.6 Tbps Interoperability with Samtec and Synopsys

May 15, 2025

SNUG 2025: A Watershed Moment for EDA – Part 2

May 1, 2025

Automotive Functional Safety (FuSa) Challenges

April 29, 2025

Scaling AI Infrastructure with Next-Gen Interconnects

April 29, 2025



SYNOPSYS

Designing with FinFETs

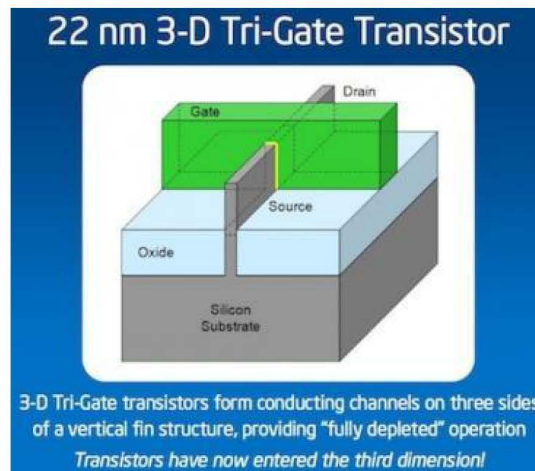
by Daniel Payne on 10-08-2012 at 6:13 pm

Categories: EDA, Synopsys

30 Comments

Intel is the number one semiconductor company in the world and has taken the lead in bringing FinFET (aka Tri-Gate) silicon to market at the 22nm node starting in May 2011, so now we see the pure play foundries playing catch-up and start talking about their own FinFET roadmaps. IC designers and layout engineers want to know how their design methodology will change as they consider using a FinFET process compared to a planar process.

Jamil Kawaat Synopsys has just written a new White Paper, Designing with FinFETs: The Opportunities and the Challenges. This blog summarizes the major points of the White Paper on FinFETs and how it effects the IC design process.



Source: Intel

There's a bit of marketing hype in the Intel statement of transistors now entering the third dimension because all planar transistors have three dimensions, it's just that the FinFET is notably taller than planar CMOS transistors.

The Growing Importance of PVT Monitoring for Silicon Lifecycle Management

April 24, 2025

Achieving Seamless 1.6 Tbps Interoperability for High BW HPC AI/ML SoCs: A Technical Webinar with Samtec and Synopsys

April 17, 2025

SNUG 2025: A Watershed Moment for EDA – Part 1

April 15, 2025

Balancing the Demands of OTP for Advanced Nodes with Synopsys IP

April 14, 2025

Synopsys Webinar: The Importance of Security in Multi-Die Designs – Navigating the Complex Landscape

April 11, 2025

Synopsys Executive Forum: Driving Silicon and Systems Engineering Innovation

April 9, 2025

A Synopsys Webinar Detailing IP Requirements for Advanced AI Chips

April 3, 2025

Evolution of Memory Test and Repair: From Silicon Design to AI-Driven Architectures

April 1, 2025

DVCon 2025: AI and the Future of Verification Take Center Stage

March 6, 2025

TRNG for Automotive achieves ISO 26262 and ISO/SAE 21434 compliance

February 27, 2025

Synopsys Expands Hardware-Assisted Verification Portfolio to Address Growing Chip Complexity

February 25, 2025

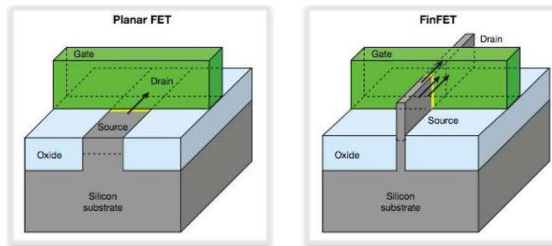
How Synopsys Enables Gen AI on the Edge

February 24, 2025

Synopsys Expands Optical Interfaces at DesignCon

February 17, 2025

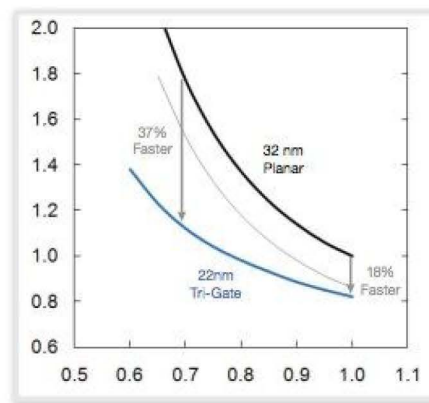
What is Different About Synopsys' Comprehensive,



Simplified transistor comparison not drawn to scale, Planar vs FinFET

Attractive features of the FinFET transistors include:

- Lower leakage currents caused by a fully depleted channel region
- Reduced short-channel effects
- More transistors/unit area due to 3D layout
- Less variation effects from dopant fluctuation
- Lower Line Edge Roughness (LER) variation
- Improved performance margins
- Lower retention voltage in SRAMs



Intel's 22nm Tri-Gate technology showing a wider performance advantage at lower VDD

Source: Mark Bohr, Intel. May 2011.

Negative consequences of using FinFET devices are:

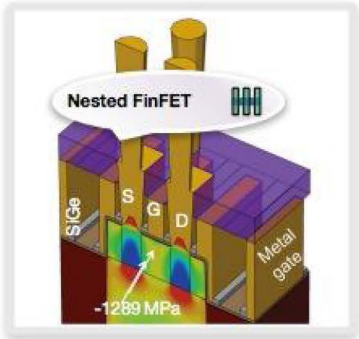
- Quantized channel widths, fewer choices compared to planar CMOS
- More complex SPICE models, longer simulation run times
- More complex extraction rules and longer extraction run times
- Body-biasing techniques lose their effectiveness
- Additional Restricted Design Rules (RDR)
- New Layout Proximity Effects (LPE)
- Reliability concerns, Negative-Bias Temperature Instability (NBTI) and Positive-Bias Temperature Instability (PBTI)

Scalable Solution for Fast Heterogeneous Integration

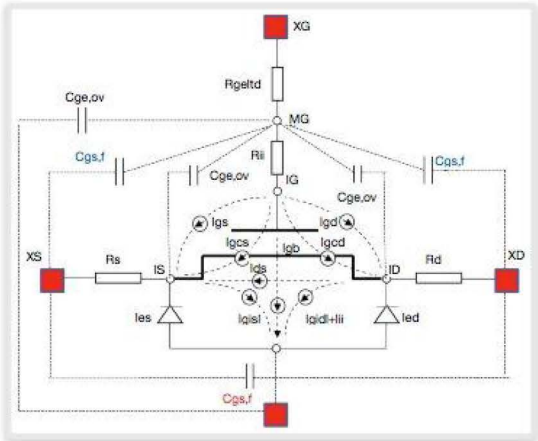
February 3, 2025

Will 50% of New High Performance Computing (HPC) Chip Designs be Multi-Die in 2025?

January 28, 2025



Stress simulation of FinFETs



Parasitics model of the FinFET

With the increased number of layout rules for FinFET devices you want to use a rule-driven layout flow, instead of the old sequential flow of: Schematic design, Layout design, batch rule check, iterate until correct.

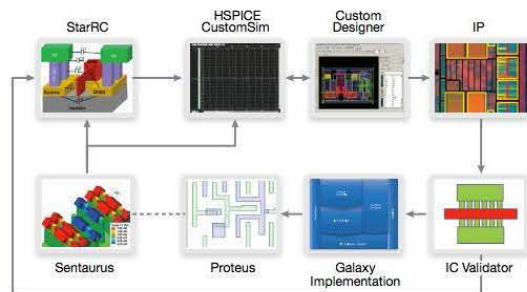
EDA Tool Flow

Synopsys has seven EDA tools used to implement FinFET-based IC designs:

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-
EDA Category
EDA Tool
-
TCAD modeling
Sentaurus
-
Parasitic extraction
StarRC
-
SPICE circuit simulation
HSPICE, CustomSim
-
IC schematic and layout editing
Custom Designer
-
DRC and LVS checking

IC Validator
Implementation (Logic Synthesis, P&R)
Galaxy
-
Mask synthesis
Proteus
-



Summary

Intel started using FinFET devices at the 22nm node in 2011 while other foundries have announcements for FinFETs at 14nm nodes coming up in 2013 and later. EDA tool flows have been updated to account for the new FinFET issues, so the big question that remains is silicon pricing and yield compared to planar technology.

Read the complete White Paper here after a brief registration process.

Related Reading

- FinFET Wiki
- GLOBALFOUNDRIES Announces 14nm Process
- Intel's finfets too complex and difficult?
- FinFET Standard Cells at DAC
- Industry Standard FinFET versus Intel Tri-Gate
- Intel Tri-Gate is in Trouble?
- Next Generation Transistors: a Tutorial from the Master
- Introduction to FinFET technology Part II
- Introduction to FinFET technology Part I

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EDA, FINFET, FINFETS, JAMIL KAWA, SEMICONDUCTORS, SYNOPSYS, TRI-GATE

Comments

30 Replies to “Designing with FinFETs”

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