

Abstract

FinFET devices are demonstrated with multiple fins (>2) at a 120nm pitch using e-beam lithography to address some key challenges of FinFETs for 32nm node technologies and beyond. Target V_t 's are achieved by proper halo design using 20nm fins. V_t scatter due to Fin width variation is greatly reduced with a reduced halo. When such a realistic fin pitch is used, S/D contact formation becomes a serious challenge due to poly-to-active overlay requirements and the need for raised S/D for series resistance reduction. A new FinFET design without S/D contact pads is thus proposed and a selective epitaxial process to merge individual fins is developed.

Introduction

Multi-gate MOSFETs such as the FinFET [1][2] and Tri-gate FET [3] are potential device candidates for the 32nm node and beyond. Primary concerns, however, include the formation of narrow and uniform fins while providing low series resistance from the extension and contact regions of the device, V_t control and V_t variation – which have been addressed by most previous FinFET work [4, 5]. Exacerbating this problem, these fins must be placed at a fine pitch to make efficient use of layout area. To date, FinFET research has not yet addressed ground rule issues for an actual technology. In particular, S/D contact formation has not yet been studied experimentally as previous demonstrations use large S/D landing pads for a simplified contact scheme, which is unsuitable for a realistic technology.

In this work, e-beam lithography is used to look ahead and study these issues for realistic fin dimensions and pitch characteristic of 32nm node expectations. Critical process issues are examined, including spacer formation, raised S/D (RSD) by selective Si epitaxy, and silicidation, and solutions to these integration challenges are demonstrated. A S/D contact scheme is proposed in which individual fins without large S/D landing pads can be later merged by selective epitaxy. The Fin-only array design makes it easier to adopt new advanced lithography methods. The resulting tradeoff between increased parasitic capacitance and reduced parasitic resistance is studied.

Device Fabrication

Figure 1 lists key process steps used in the FinFET fabrication sequence. SOI wafers are first thinned down to 75nm with a 25nm hard mask dielectric. Fins of 20nm width and 120nm pitch are defined using e-beam lithography and reactive ion etch (RIE). FinFETs with and without large S/D contact pads are fabricated. Precise proximity correction ensures that there is no fattening of the fins at the intersection of fin and the S/D pad as shown in Fig. 2. The gate oxide and poly-Si gate are formed after fin definition. To improve gate-level lithography, the poly-Si gate is planarized using CMP as shown in Fig. 3. Extension and optional halo implants are performed after gate patterning. Spacers are successfully formed only along the gate sidewall (Fig. 2) to allow for RSD growth on the sides of the fins, which can become difficult in future technologies when active and poly pitches are small. After spacer formation, RSD is formed only on the fin sidewall by selective epitaxy. Two different silicide thickness are investigated to optimize for device performance.

Device results

Multiple-fin FinFETs with pitch as small as 120nm are demonstrated. Fig 4 shows typical NFET and PFET I-V characteristics for $L=30$ nm. Excellent subthreshold slope and DIBL (Fig. 5) is achieved with 20nm wide fins. Halo-doped channel devices show a strong V_t dependence on fin width (Fig. 6) due to channel charge. With reduced halo dose, the channel dopant concentration is lower, and both fin width dependence and V_t scatter are reduced. As the number of fins is increased, V_t scatter reduces (Fig. 7), likely due to averaging of fin characteristics. Silicidation of a FinFET must be done carefully as too thick a silicide can fully consume the fin, which reduces silicon-to-silicide contact area and greatly increases contact resistance. Drive current could thus be degraded with a thicker silicide (Fig. 8) – a problem that becomes especially pronounced when the fin width is small (Fig. 9). An optimized silicide thickness can thus minimize Ron dependence on the fin width (Fig 9).

Multiple-Fin FinFET Design

Most previously reported FinFETs use S/D landing pads to connect an array of narrow fins in parallel at two ends. This is unsuitable for an actual FinFET technology, however, as the use of S/D landing pads inevitably increases gate contacted pitch (Fig. 10) due to overlay requirements. This is undesirable because the layout efficiency of a FinFET is thus severely degraded over that of a conventional planar FET. The use of S/D landing pads also complicates spacer etching in the small space between the FinFET gate and landing pad, as shown in Fig. 2. Elimination of S/D landing pads simultaneously solves both problems, but requires that parallel fins be strapped together (Fig. 11) by local interconnect [5] or, especially when the fin pitch is realistically small, Si epitaxy (Fig. 12). Such a design makes it possible to adopt new advanced lithography methods such as alternating phase shift and self assembly for fin formation. The merged fin approach, however, results in a tradeoff between parasitic resistance and capacitance, as studied by 3D simulation (20nm fins at 120nm pitch) in Figs. 13&14. Leaving a hard mask on top of the fin eliminates RSD vertical epi growth, which adds parasitic capacitance (Fig. 13). Series resistance is optimized with a 30nm or more RSD (Fig.14). Local interconnect results in significant parasitic capacitance (Fig. 15), such that merging of fins (50nm epi growth on each side of the fin in Fig. 12) is preferred.

Conclusion

The first experimental demonstration of FinFETs with fin pitch as small as 120nm is presented. The elimination of S/D contact pads is necessary for introduction of the FinFET into future technologies for layout efficiency, process integration, and parasitic capacitance. New spacer and RSD processes are developed to merge fins using Si epi for the new proposed design.

References

- [1] X. Huang, *et al.*, *IEDM*, 1999, p. 67.
- [2] J. Kedzierski, *et al.*, *IEDM*, 2001, p. 437.
- [3] R. Chau, *et al.*, *SSDM*, 2002.
- [4] K. G. Anil, *et al.*, *VLSI Tech. Symp.* 2005, p.198
- [5] Y. X. Liu, *et al.*, *IEDM*, 2003, p. 986
- [6] J. A. Choi, *et al.*, *IEDM*, 2004, p. 647

- (1) FIN formation using e-beam lith
- (2) Gate deposition, CMP and Pattern
- (3) Extension/Halo implant
- (4) Spacer formation
- (5) Raised Source/Drain epitaxy
- (5) Source/Drain implant & RTA
- (6) Salicide formation
- (7) Standard CMOS MOL process

Figure 1: FINFET process flow used in this work.

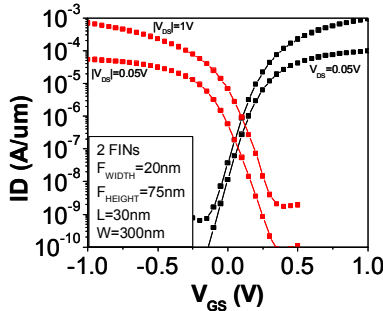


Figure 4: NFET and PFET Id-Vg characteristics. Data is collected after silicide formation.

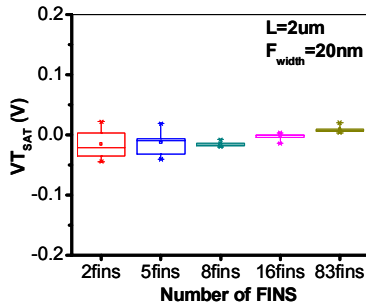


Figure 7: Increasing the number of fins reduces Vt scatter – likely due to averaging.

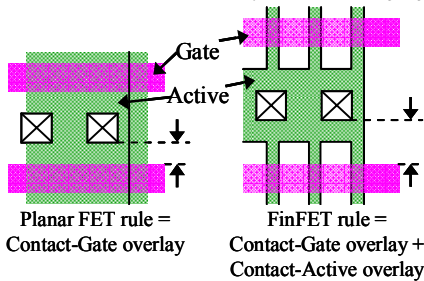


Figure 10: In a FinFET design with S/D landing pads, the S/D contact-to-gate spacing ground rule must be increased over that of planar FETs, which increases contacted gate pitch.

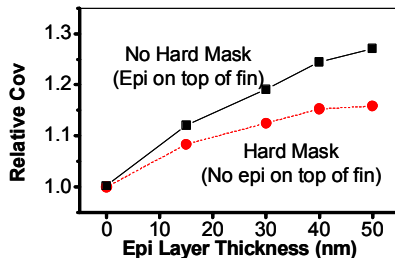


Figure 13: Use of a hard mask on top of the fin to eliminate vertical RSD epi growth reduces the added parasitic capacitance.

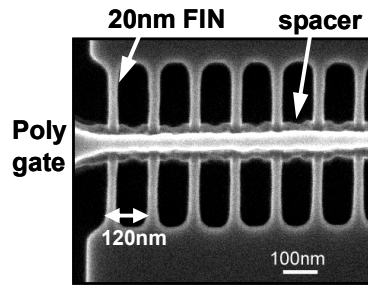


Figure 2: SEMs of Fins with a 120nm pitch obtained using e-beam, and spacers that are formed only along the gate of FINFETs.

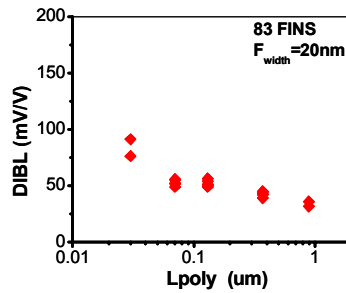


Figure 5: Excellent DIBL is achieved down to Lg=30nm.

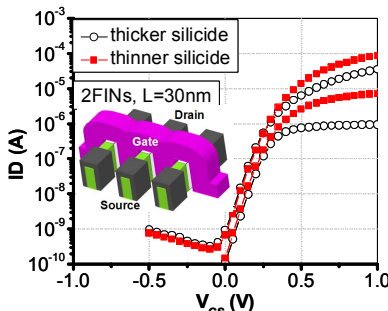


Figure 8: Drive current is greatly improved with a thinner silicide.

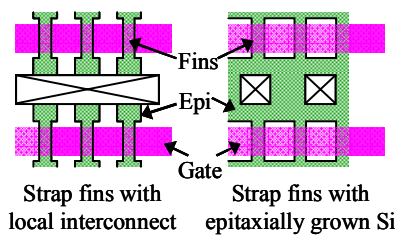


Figure 11: For a contact-to-gate space consistent with planar FETs, FinFET S/D's can be connected by metal (local interconnect) or merged by selective epitaxial silicon growth.

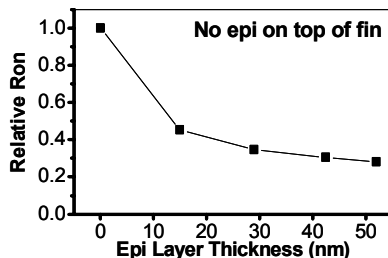


Figure 14: RSD epi growth of 30nm or more is preferred to sufficiently reduce series resistance.

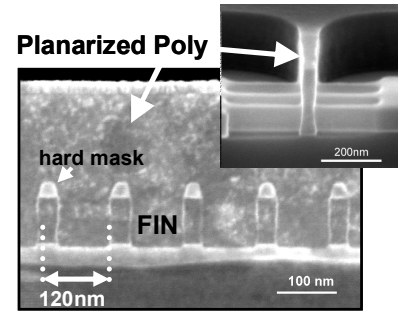


Figure 3: Poly Si gate is planarized using CMP to improve gate level lithography.

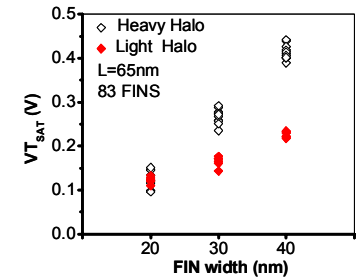


Figure 6: Vt as a function of fin width for halo-doped fins. Vt Fin width dependence and Vt scatter are reduced with a reduced halo.

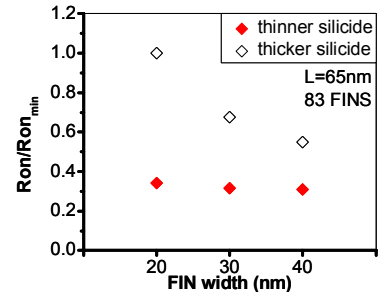


Figure 9: Ron (Vds=50mV, Vgs-Vt=0.8V) has a much weaker dependence on fin width than that with thicker silicide process.

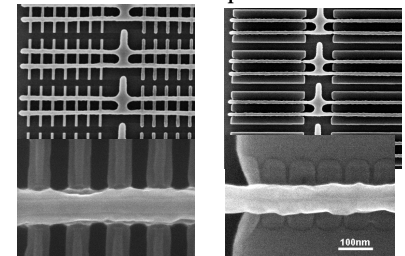


Figure 12: SEMs of selective RSD (a) 25nm is grown (b) 50nm epi is grown to merge the FINS.

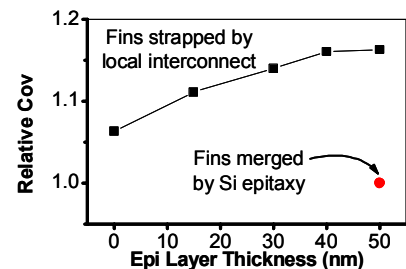


Figure 15: Using local interconnect as shown in Fig. 11 results in a capacitance penalty over the epi merged fin approach.