

Logic Detailed Structural Analysis of the Intel 22 nm Ivy Bridge Processor

May 2012

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Device Summary

Manufacturer	Intel
Part Number	i5-3550
Description	Quad-core i5 3550 3.3 GHz processor
Package Type	1155 LGA
Package Markings (top)	(Intel logo) (M) © 09 INTEL® CORE™ i5-3550 SR09A 3.30 GHZ MALAY L155B001 (e4) 2550
Package Markings (bottom)	001
Die Markings	IVB © (M) intel 2010
Die Size	19.6 mm x 8 mm = 157 mm ²
Die Thickness	480 µm
Number of Metal Levels	9
Number of Metal Gate Levels	1
Foundry	INTEL
Interconnect Level (Width / Pitch (µm))	
Metal Level - M1	0.06 / 0.09 (Measured (X-Section))
Metal Level - M2	0.06 / 0.08 (Measured (X-Section))
Metal Level - M3	0.07 / 0.10 (Measured (X-Section))
Metal Level - M4	0.07 / 0.11 (Measured (X-Section))
Metal Level - M5	0.17 / 0.10 (Measured (X-Section))
Metal Level - M6	0.24 / 0.14 (Measured (X-Section))
Metal Level - M7	0.21 / 0.36 (Measured (X-Section))
Metal Level - M8	0.23 / 0.36 (Measured (X-Section))
Metal Level - M9	7.85 / 13.85 (Measured (X-Section))
Metal Gate	0.30 / 0.09 (Measured (X-Section))
Process Type	CMOS (Copper)
Process Generation	22 nm
Feature Measured to Determine Process Generation	Gate Length (Logic, TEM)
Transistor Gate Length	30 nm
Cell Size	0.108 µm ²

Executive Summary

The Intel CORE i5-3550 processor is a quad-core device codenamed Ivy Bridge and fabricated using Intel's Tri-Gate transistor 22 nm process technology. A traditional 2-D planar MOS transistor is replaced with a gate that is wrapped around a thin three-dimensional silicon fin that rises up vertically from the silicon substrate. A thin high-k dielectric separates the silicon fin from the metal gate on each of the three sides of the fin – one on each side and one across the top - rather than just one on top, as is the case with the 2-D planar transistor. Control of current from the source side of the fin to its drain side is accomplished by the gate on each of the three sides of the fin; therefore Tri-Gate name was coined.

Intel 22 nm Tri-Gate process technology summary:

- 1st generation Tri-Gate™ process technology
 - Three-dimensional Tri-Gate transistor (FinFET-type)
 - Rounded silicon fins are 18 nm thick at foot, 7 nm thick at top and 38 nm high
 - “Structured layout” at fin level
 - All fins constrained to be parallel and have a restricted/fixed pitch of 60 nm
- 3rd generation high-k dielectric and metal gate
 - Hafnium oxide (2 nm thick) high-k gate dielectric with the bottom interface silicon oxide layer (0.6 nm)
 - Dual work function metal gates:
 - TiN/AlCO/TiAlN for PMOS with TaAl barrier and W body
 - AlTiCO/TiN for NMOS with TaAl barrier and W body
 - “Structured layout” at gate level
 - All gates constrained to be parallel and have a restricted/fixed pitch of 90 nm or 180 μm (in I/O regions)
- Gate last (replacement gate) integration
- 5th generation strained silicon engineering
 - Embedded graded SiGe for PMOS channel compressive strain
 - Embedded Si:C for NMOS channel tensile strain
 - Presence of low amount of carbon detected in the NMOS source/drain regions by EELS analysis
 - Raised source/drain regions for PMOS and NMOS transistors formed by selective epitaxial processes
- Front-End-Of-Line process features
 - Shallow N-wells in P-epi layer grown on P⁺ silicon substrate
 - SiCON sidewall spacers and nitride cap layer for NMOS and PMOS transistors
 - Tungsten-based metal 0 used for local interconnects and contacts
 - Trench type contacts have 25 nm width at bottom and 90 nm pitch or 180 μm (in I/O regions)

- Back-End-Of-Line process features
 - o Nine copper dual damascene metal levels
 - o Dense metal 0 to metal 2 lines with 90 nm pitch
 - o Thick non-damascene copper metal 9
 - o Low-k (SiOC) inter-metal dielectrics with SiCN copper-sealing/etch-stop layers for IMD 1 to IMD 7
 - o Self-aligned aluminum-based barrier is used to improve the copper-cap layer interface for the metal levels
 - o SiCN-based IMD 8
 - o Decoupling MIM capacitors formed between M8 and M9 levels are implemented using TiN plates and Hf-based capacitor dielectric
 - o Single layer silicon nitride passivation
- Flip-chip land grid array (FC-LGA) package with copper pillar bumping (CPB) technology

Embedded SiGe and Si:C regions are epitaxially grown in the cavities formed in the source/drain regions of respective PMOS and NMOS fins to provide compressive and tensile strain to the channel parts of the fins. Metal gates and trench contacts formed later may provide additional strain and improve performance of PMOS and NMOS transistors.

A thin SiO bottom interface layer is used between the fin and hafnium-based high-k gate dielectric to overcome channel mobility degradation. A TiN protective layer and TaAl barrier are then formed followed by the multi-layer TiN/AlCO/TiAlN work function (WF) metal stack deposition in both PMOS and NMOS gate trenches. This metal stack is left for PMOS gates but selectively removed from NMOS gates and replaced with AlTiCO/TiN layers. Both PMOS and NMOS gates are filled with tungsten, recessed, and capped with a thin TiW layer and a thicker SiN layer.

Intel enforces restricted design rules to create “structured” fin and gate layouts. This DFM technique of uniform, regular arrangement of silicon fins and metal gates improves yields of the advanced HKMG technology while using less advanced lithography. A double patterning process is used at the fin and gate levels to enable abrupt gate endcap regions. The minimum gate length and pitch are 30 nm and 90 nm, respectively. The silicon fin thickness and pitch are even more impressive: 18 nm (at foot) and 60 nm, respectively.

Two 6T STAM cell layouts are used. The 6T “thin layout” SRAM cell has an area of $0.108 \mu\text{m}^2$. The access NMOS transistor is done as a single-fin Tri-Gate transistor while the pull-down NMOS transistor is done as a double-fin Tri-Gate transistor. The pull-up PMOS transistor has a common gate with the pull-down transistor and is done as a single-fin Tri-Gate PMOS transistor. This 6T SRAM cell is used for L3 cache while a larger 6T SRAM cell ($0.128 \mu\text{m}^2$) is used in four cores, processor graphics and other regions of the die.

Process Summary

Level	Constituent Materials	Process
Substrate	Silicon	Lightly doped P-type epitaxial layer on heavily doped P-type substrate
Wells	Silicon	Multiple implants followed by annealing (not analyzed)
Fin and Isolation	Silicon and Oxide	Hard mask with 60 nm pitch likely formed using immersion litho with double patterning. Etch trench in Si, thermal oxidation, thick oxide fill, CMP. Recess etch to expose fin and form lateral shallow trench isolation; STI. Thermal oxidation to repair etch-induced damage and define silicon fin geometry (fin thinning and top rounding).
Sacrificial gate	Polysilicon	Grow thin oxide, deposit polysilicon. Pattern and etch polysilicon gates running perpendicular to fins. Minimum gate pitch of 90 nm (likely immersion litho and double patterning)
Sidewall spacer (SWS) and source/drain (S/D) implant	SiOCN	Source/drain extension implant; deposit conformal SiCON; etch back to form SWS; possibly S/D implants and laser annealing
PMD, lower portion	Oxide	CVD oxide, CMP
NMOS source/drain (S/D)	Si:C	Pattern and expose NMOS S/D; wet-etch silicon cavity; Si:C selective epitaxial growth (in-situ doped or NMOS S/D implant)
PMOS source/drain (S/D)	SiGe	Pattern and expose PMOS S/D; wet-etch silicon cavity; SiGe selective epitaxial growth (in-situ doped or PMOS S/D implant), likely graded Ge concentration
PMD, upper portion	Oxide/SiN	CVD SiCN and oxide, CMP
Gate dielectric	Silicon oxide/hafnium oxide	Likely chemical oxide for bottom interface layer, ALD hafnium oxide, post deposition annealing
Top interface layer	TiN	ALD TiN
Barrier layer	TaAl	ALD TaAl
PMOS work function metal	TiN/AlCO/TiAlN	ALD TiN/AlCO/TiAlN, CVD W, CMP

<i>Level</i>	<i>Constituent Materials</i>	<i>Process</i>
NMOS work function metal	AlTiCO/TiN	ALD AlTiCO/TiN, CVD W, CMP
Recess and cap layers	W/TiW/SiN	Etch back W, ALD TiW, CVD SiN, CMP
Metal 0 contact	W with TiN/Ti liner	Dual damascene
IMD 0	SiCN/SiOC	CVD
Metal 1 to metal 8	Copper with Ta/TaN barrier	Dual damascene
IMD 1 to IMD 5	SiOCN/SiOC	CVD
IMD 6 to IMD 7	SiCN/SiOC	CVD
IMD 8	SiCN/SiCN	CVD
Metal 9	Copper with Ti barrier	Electroplating
Passivation	SiN	CVD

1.0 Package and Die

1.1 Packaging



Figure 1.1.1: Package, top view.

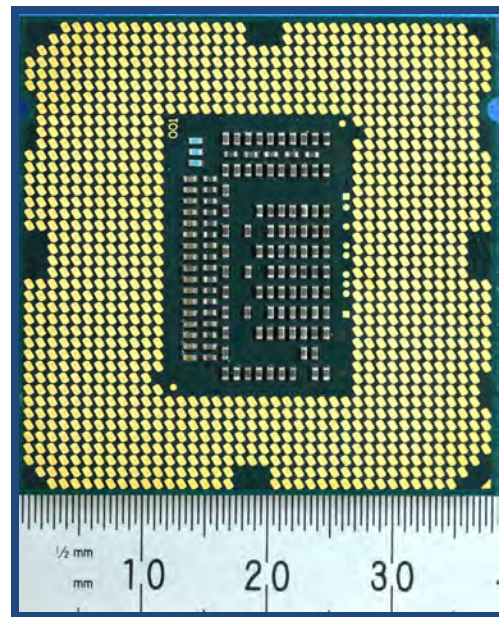
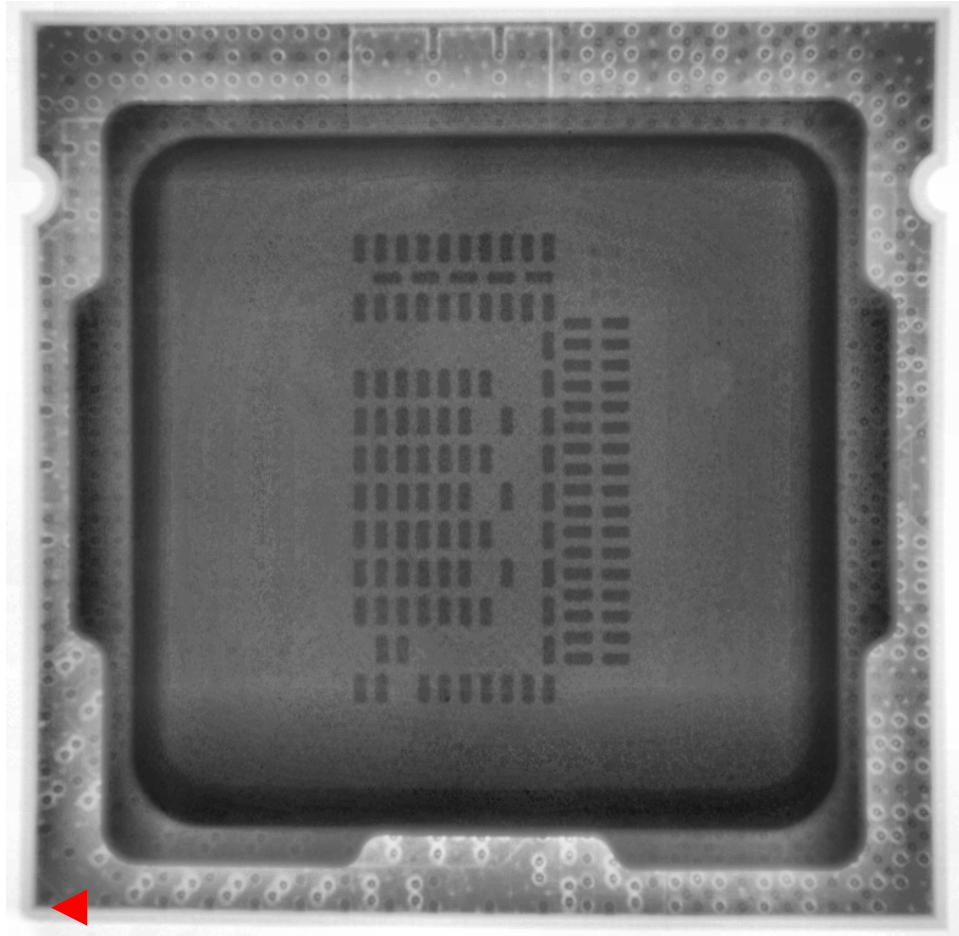


Figure 1.1.2: Package, bottom view.

Feature	Dimension	Unit
Package width	37	mm
Package height	37	mm
Land pitch	0.9	mm

Comments

- Flip-chip land grid array (FC-LGA) package;
- Packaged in Malaysia;
- Integrated heat-spreader (IHS).



Pin 1 Indicator

Figure 1.1.3: Package, X-ray image.

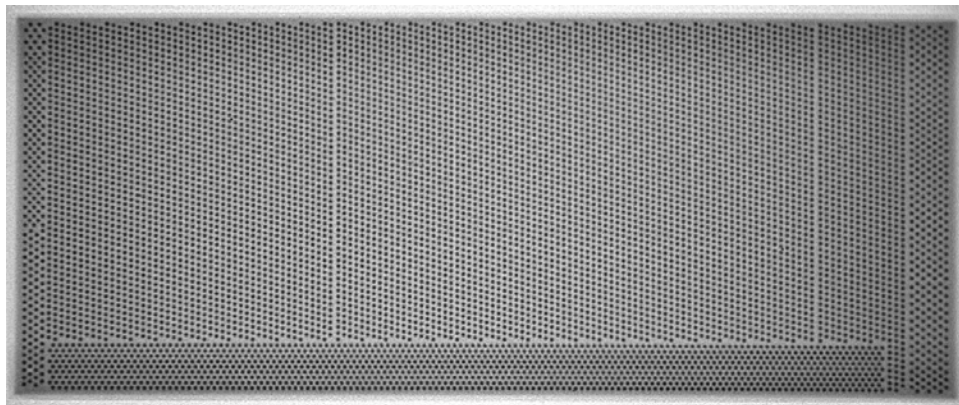


**Figure 1.1.4: Partially deprocessed package
(heat-spreader and package substrate removed), X-ray image.**

Comments

- Flip-chip packaging
- Single die in the package

1.2 Die

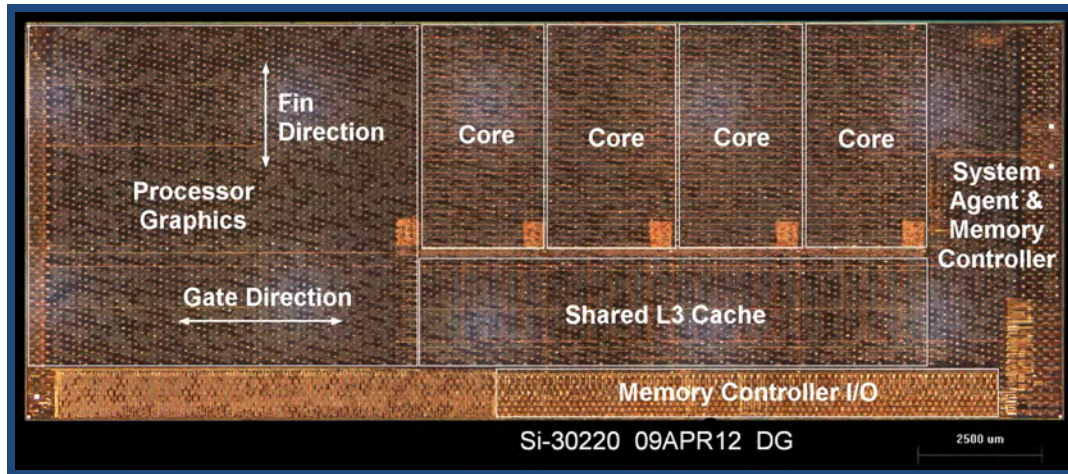


Figure 1.2.1: Die photograph.

Feature	Dimension	Unit
Die width	19.6	mm
Die height	8.0	mm
Die area	157	mm ²
Die thickness	0.48	mm



Figure 1.2.2: Die markings.

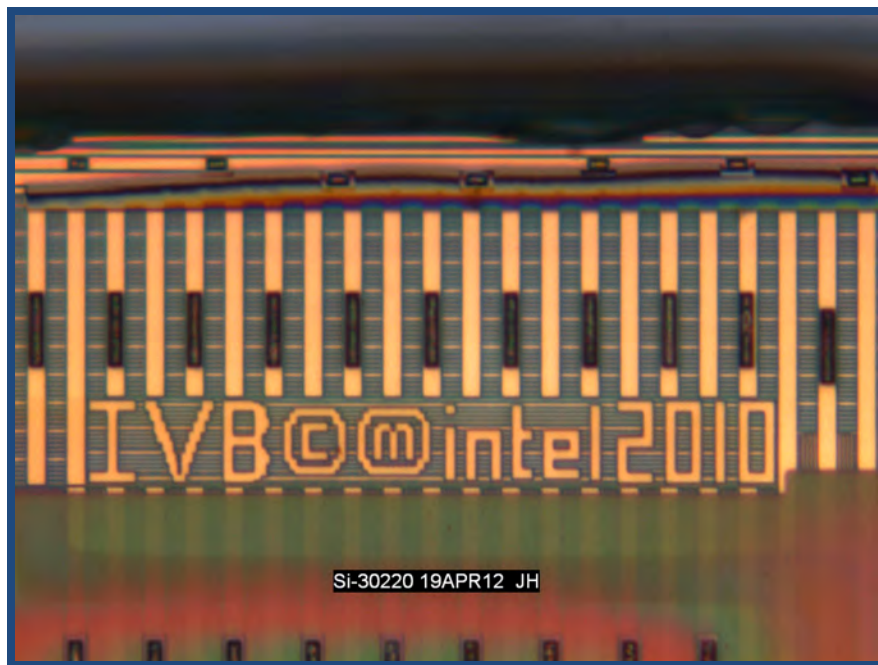


Figure 1.2.3: Die markings (after removal of top metal level).

Comments

- Die markings: IVB.© (M) intel 2010.

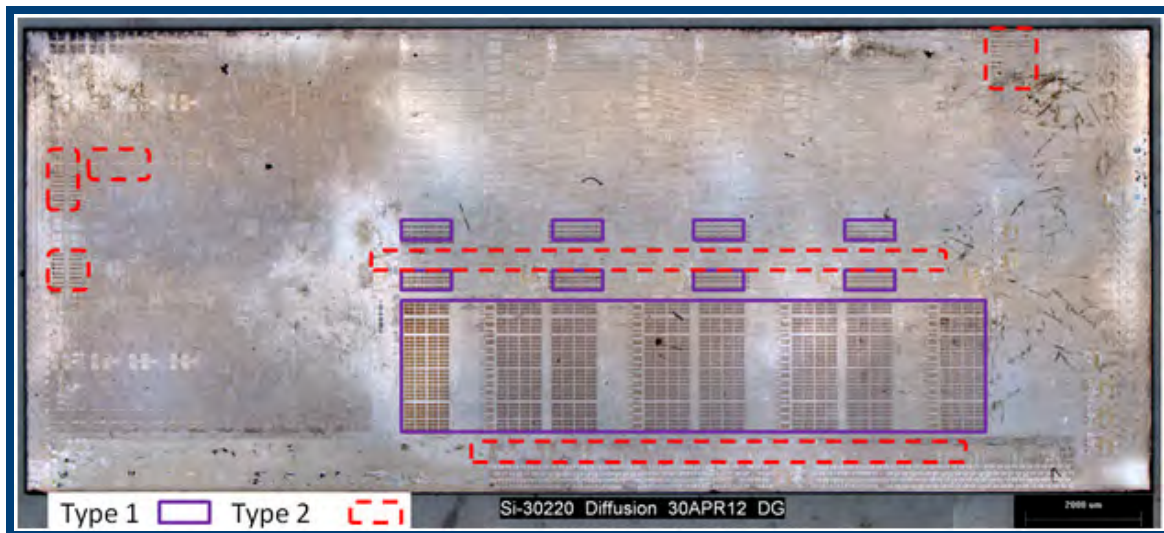


Figure 1.2.4: Die floor plan with SRAM blocks (after delayering to substrate level).

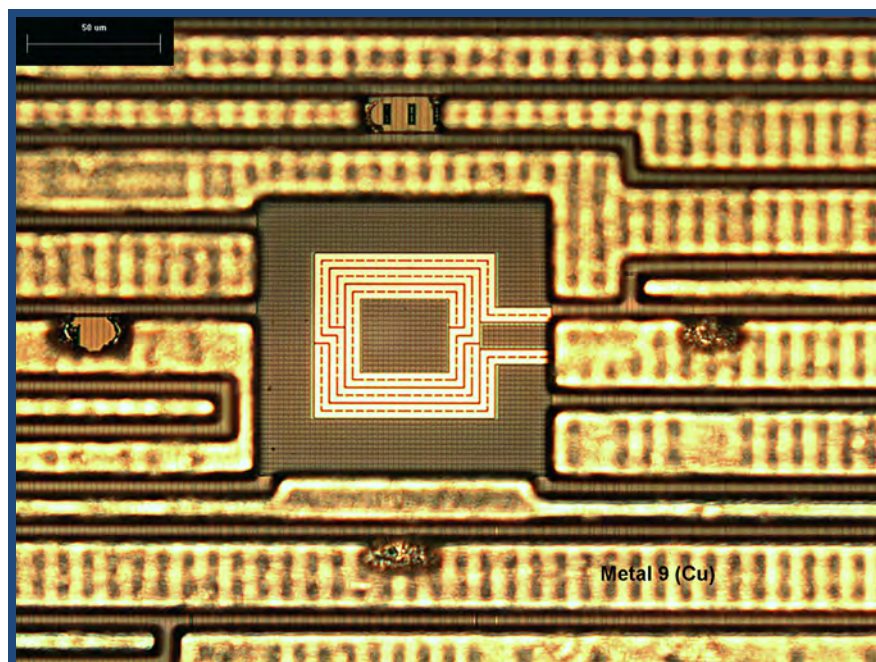


Figure 1.2.5: Inductor, high magnification optical image.

Comments

- Quad-core architecture;
- Four identical processor cores;
- 6 MBytes of shared L3 cache;
- Two types of SRAM cell found in the die;
 - o 6T SRAM cell of Type 1 has the cell area of $0.108 \mu\text{m}^2$ and used in shared L3 cache and 8 arrays located in processor cores;
 - o 6T SRAM cell of Type 2 has the cell area of $0.128 \mu\text{m}^2$ and used in processor graphics, cores and other locations;
- Memory controller I/O located at the die bottom;
- There are a few inductors in the die. Together with decoupling capacitors (implemented between M8 and M9 levels), they are likely used as low pass filters.

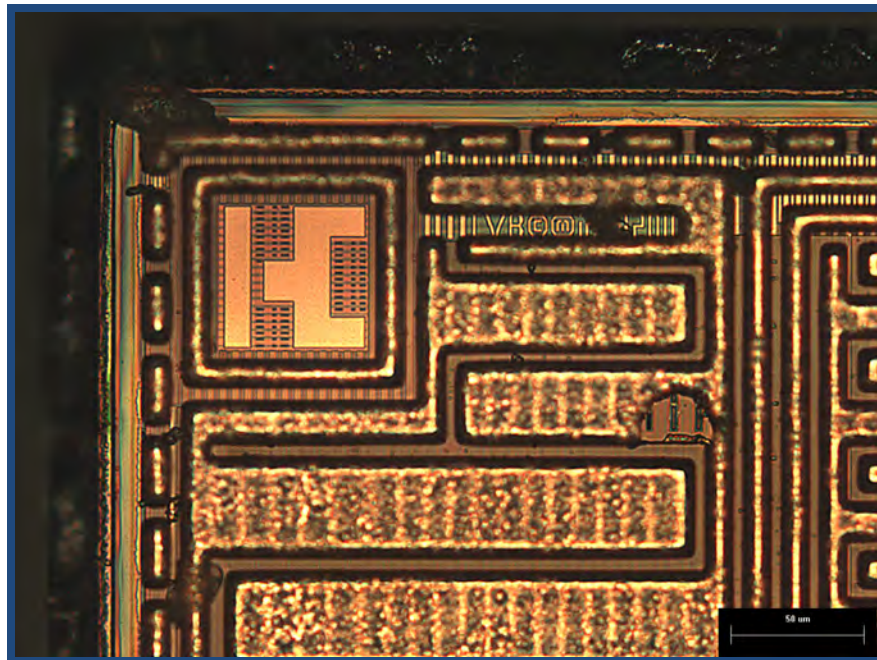


Figure 1.2.6: Top-left die corner.

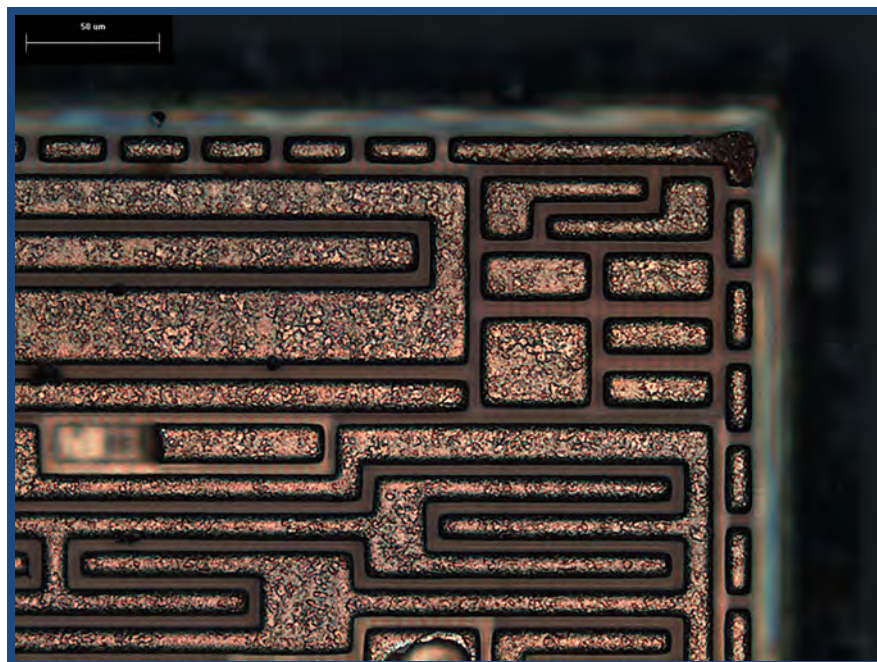


Figure 1.2.7: Top-right die corner.

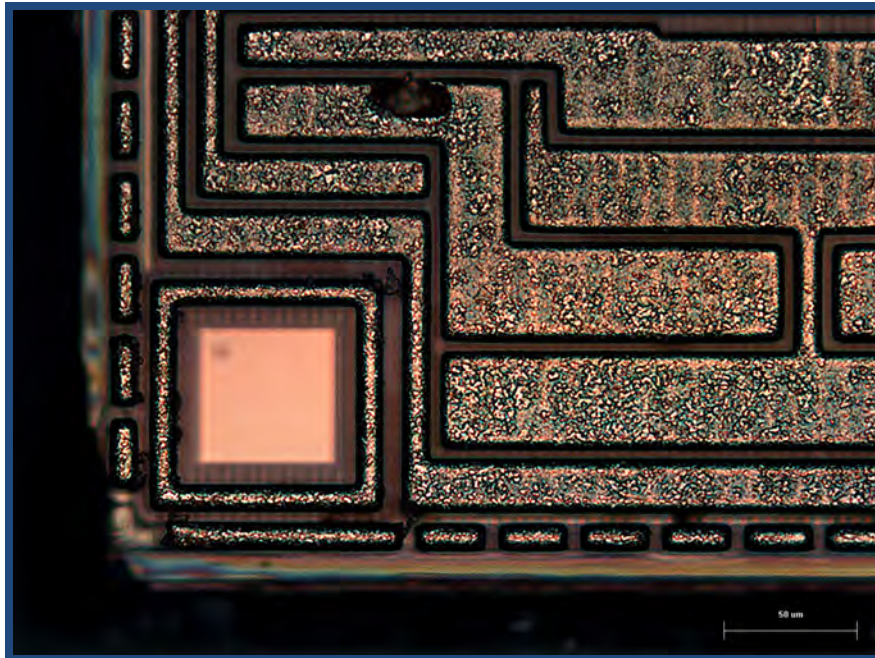


Figure 1.2.8: Bottom-left die corner.

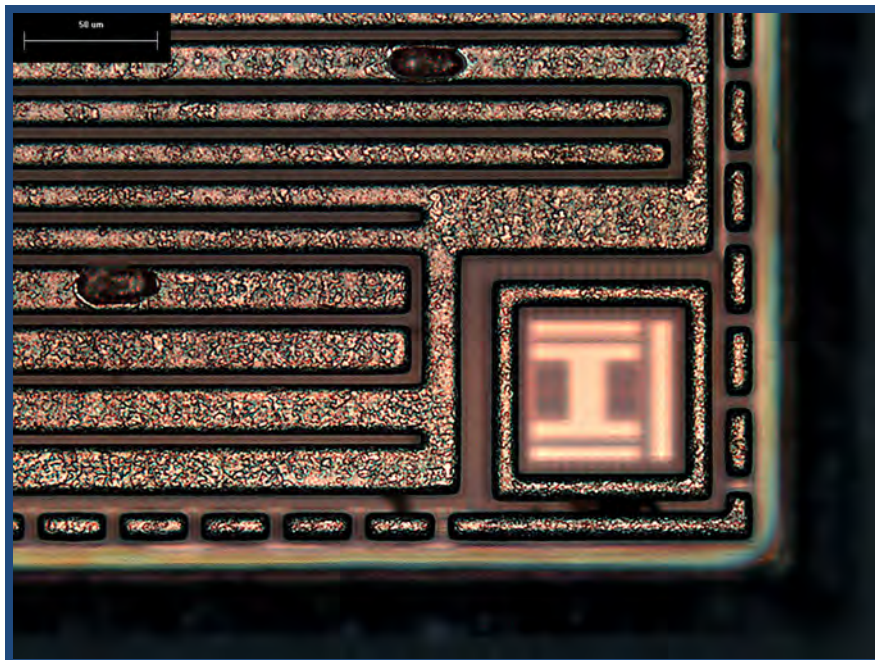


Figure 1.2.9: Bottom-right die corner.

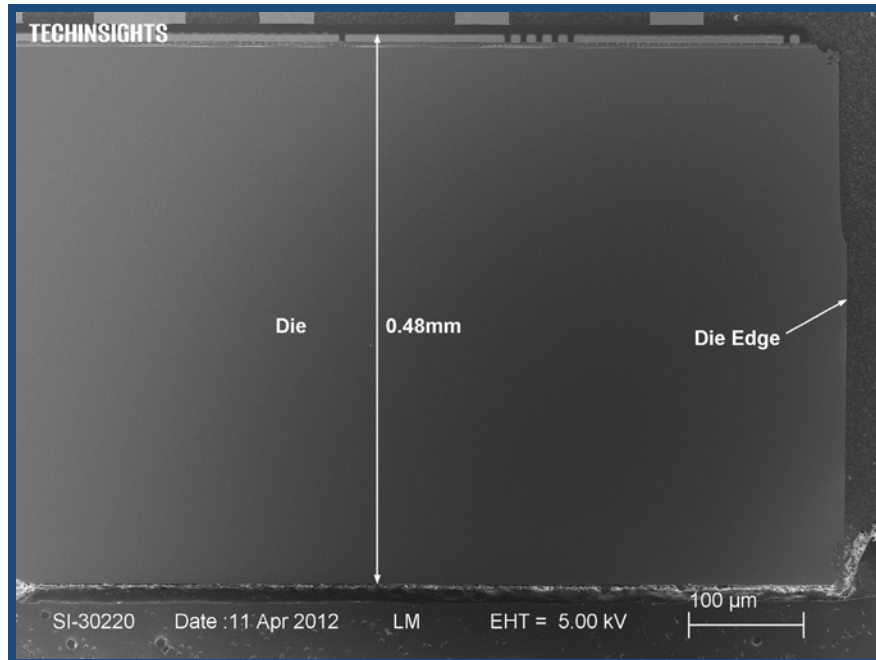


Figure 1.2.10: Die thickness, SEM cross-section.

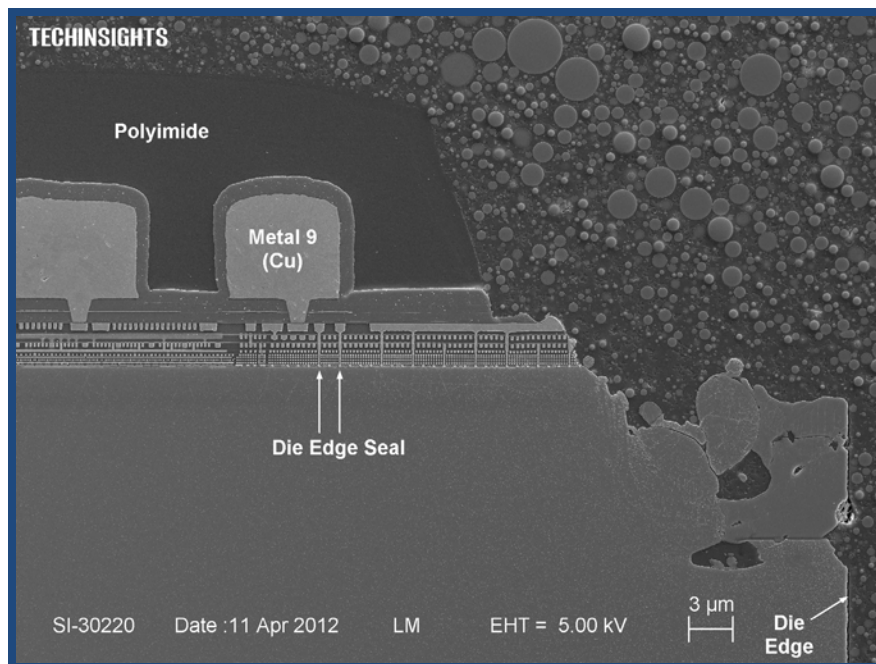


Figure 1.2.11: Die edge, SEM cross-section.

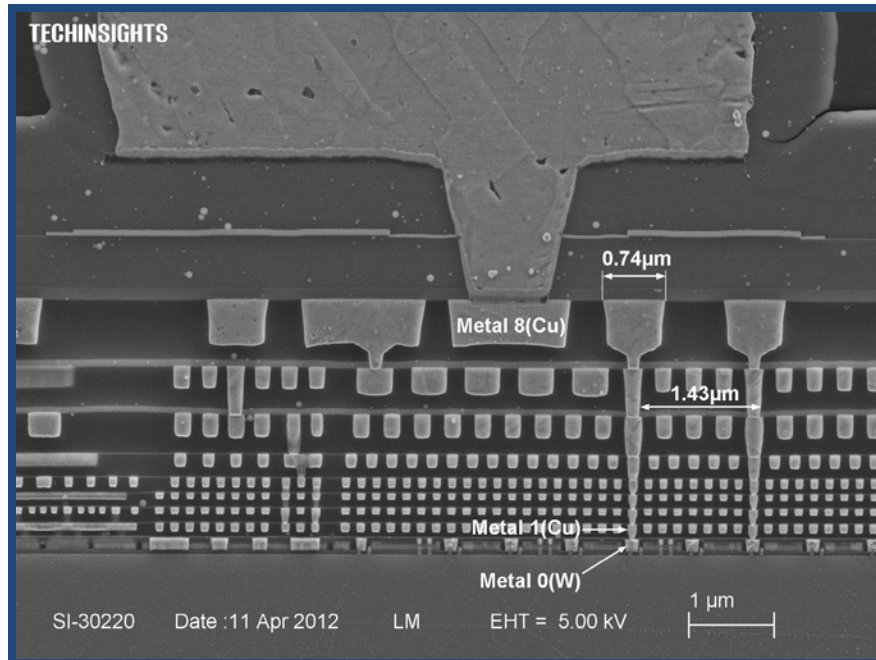


Figure 1.2.12: Die edge seal, SEM cross-section.

Feature	Dimension	Unit
Die edge seal pitch	1.43	µm
Copper metal 8 width	0.74	µm

Comments

- Double die edge seal consists of silicon fin regions protruding from silicon substrate and strapped by W-based metal 0 and Cu-based metal 1 to metal 8 stack running around the die.
- Die singulated as two-step process with deep laser cut on front side of die.

1.3 Bump Pads

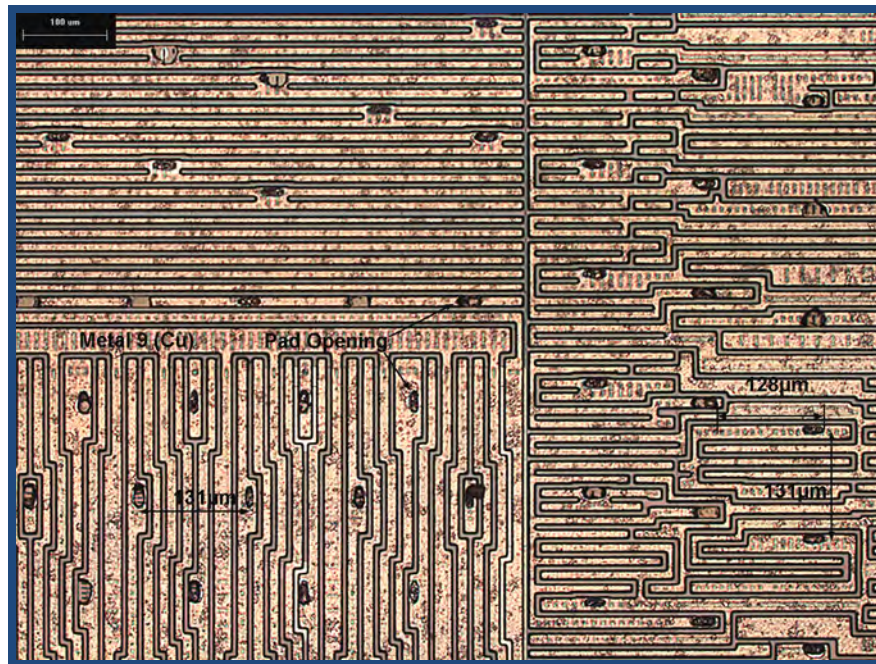


Figure 1.3.1: Metal 9 lines with bump pad openings, low magnification optical image.

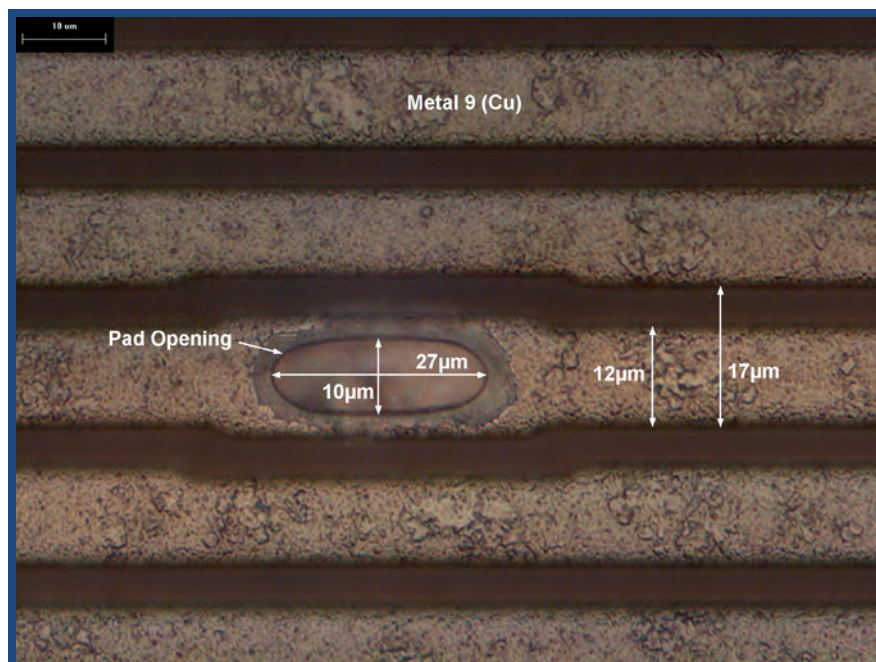


Figure 1.3.2: Metal 9 line with a minimum size bump pad opening, high magnification optical image.

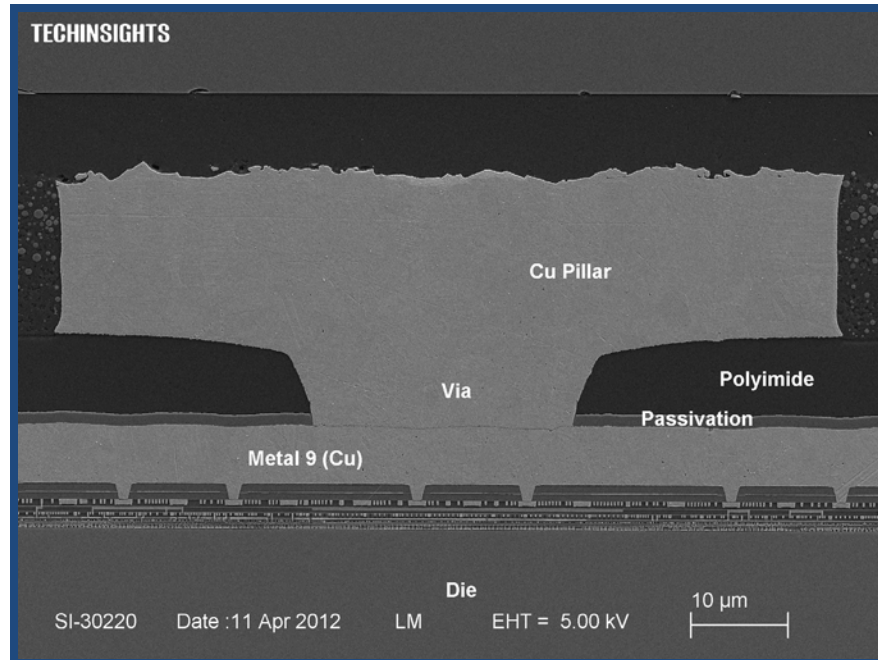


Figure 1.3.3: Copper pillar bump, SEM cross-section.

Feature	Dimension	Unit
Minimum observed pad opening width	10	μm
Minimum observed pad opening length	27	μm
Minimum observed pad opening pitch (vertical)	131	μm
Minimum observed pad opening pitch (horizontal)	128	μm
Minimum observed metal 9 width	12	μm
Minimum observed metal 9 space	5	μm
Minimum observed metal 9 pitch	17	μm
Polymide die coat thickness	15	μm

Comments

- Copper pillar bumping (CPB) technology;
- Copper pillars are connected to metal 9 pads and bus lines through pad openings.

2.0 Process

The Intel Ivy Bridge i5-3550 quad-core processor die is fabricated using the industry-leading 22 nm process technology, featuring Tri-Gate transistors formed on a bulk epitaxial silicon substrate, high-k hafnium oxide gate dielectric, dual work function metal gates, fifth generation strained silicon technology, tungsten metal 0 local routing and bar type contacts, nine copper interconnect levels, low-k inter-metal dielectrics, and double patterning process used at the transistor gate level. The fabrication process is described in detail in the following sections, beginning with the substrate and ending with the passivation. The minimum sized L3 cache SRAM cell and relaxed 6T cell structures and related process features are presented in Section 3.0. Critical vertical and horizontal dimensions are summarized in Section 4.0.

Overview:

- P-type bulk silicon substrate
 - Lightly doped epitaxial layer (~2.6 μm thick) on highly doped substrate
- Shallow trench isolation (STI) with minimum pitch of 60 nm
- Three-dimensional Tri-Gate transistors used as PMOS and NMOS transistors for core logic, SRAM arrays, and I/O regions
- Tri-Gate transistor technology
 - Innovative 3-D transistor structure comprises metal gate wrapped around transistor's channel, which is implemented in a silicon fin
 - Monocrystalline silicon fins are 18 nm thick at foot, 7 nm thick at top and 37 nm tall
 - Fin pitch of 60 nm
 - "Structured layout" at fin level
 - All fins constrained to be parallel
 - Double patterning used at fin level to enable abrupt fin endcap regions
 - The first lithography step patterns are a series of parallel continuous lines
 - The second masking step is used to define the length of the lines
 - Restricted/fixed fin pitch of 60 nm
- High-k metal gate (HKMG) technology
 - Hafnium oxide high-k gate dielectric
 - Thin SiO_x bottom interface layer to overcome channel mobility degradation
 - TiN top interface layer
 - Replacement dual band edge work function metal gates
 - TiN/AlCO/TiALN with a TaAl barrier used as PMOS WF metal
 - AlTiCO/TiN with a TaAl barrier used as NMOS WF metal

- ❑ W used as a gate filling material for both PMOS and NMOS gates
 - ❑ Polysilicon sacrificial transistor gates
- o Minimum observed gate length: 30 nm
- Fifth generation strained silicon technology
 - o Embedded graded SiGe technology used to enhance PMOS performance
 - o Embedded Si:C regions formed in recessed source/drain parts of silicon fin by selective epitaxial growth are used for NMOS mobility enhancement
- “Structured layout” at metal gate level
 - o All metal gate lines constrained to be parallel
 - o Double patterning used at the metal gate level to enable abrupt gate endcap regions
 - o Restricted/fixed gate pitch
 - ❑ Contacted gate pitch observed in L3 cache: 90 nm
 - ❑ Contacted gate pitch observed in processor core: 90 nm
 - ❑ Contacted gate pitch observed in I/O block: 180 nm
- Pre-metal dielectric, PMD
 - o SiN contact etch stop layer
 - o Undoped oxide 1, CMP planarized
 - o Undoped oxide 2, CMP planarized
- Tungsten dual damascene metal 0 used for local interconnects and contacts
- Nine copper-based interconnect levels
 - o Dual damascene metal 1 to metal 8
 - o Thick non-damascene metal 9 for copper pillar bumping (CPB) technology
 - o Self-aligned aluminum-based barrier is used to improve the copper-cap layer interface for the metal levels
- Low-k (SiOC) inter-metal dielectrics with SiCN or SiON copper-sealing/etch-stop layers for IMD 1 to IMD 7
- SiCN-based IMD 8
- Single layer nitride passivation

2.1 Substrate

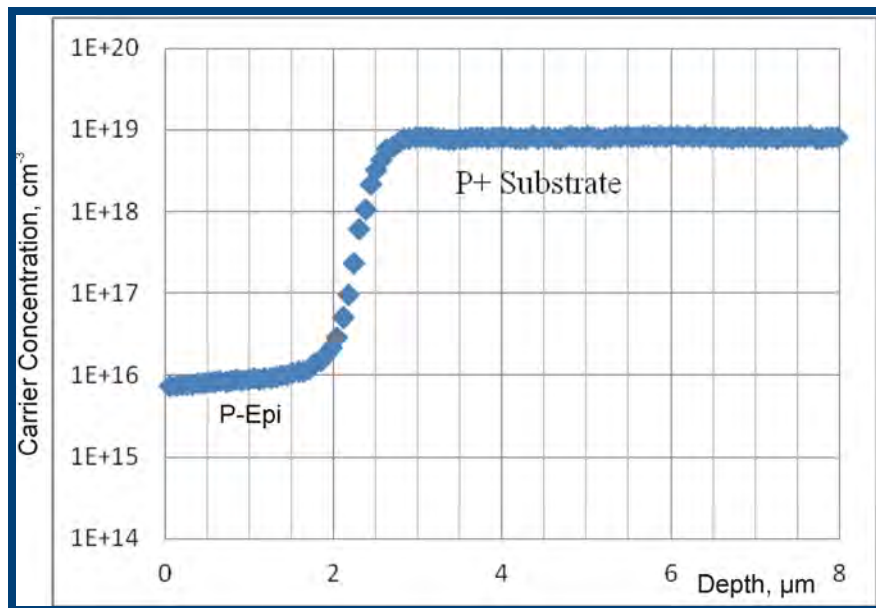


Figure 2.1.1: Carrier concentration profile of a P-type epitaxial layer on a P-type silicon substrate, spreading resistance analysis.

Feature	Depth (μm)	Carrier concentration (cm⁻³)
Si Substrate	-	8.2×10^{18}
Epitaxial layer	2.6	7.5×10^{15}
N-well	0.2	-

Table 2.1.1: Substrate doping profile summary.

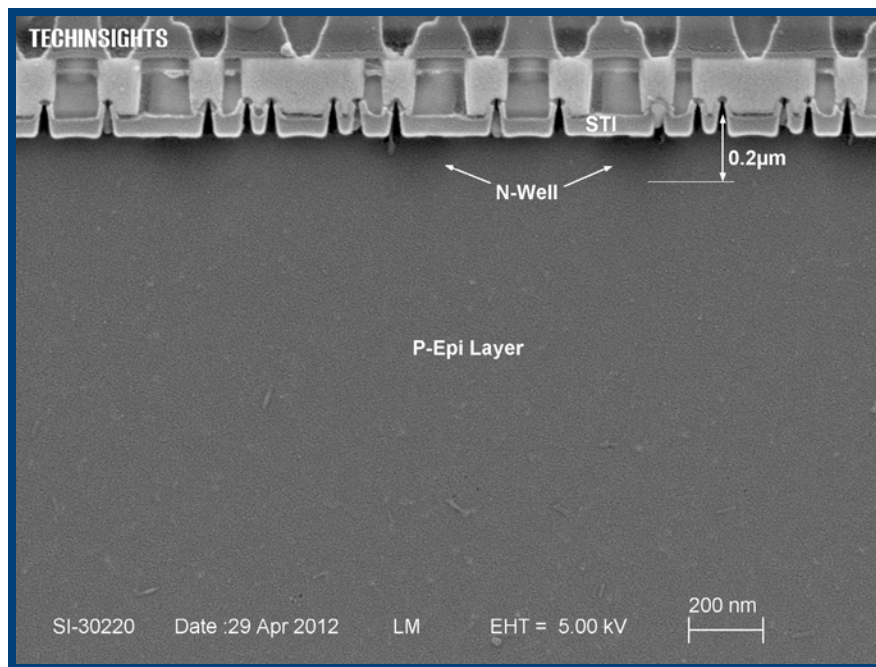


Figure 2.1.2: N-wells delineated by silicon etch staining, SEM cross-section, SRAM region.

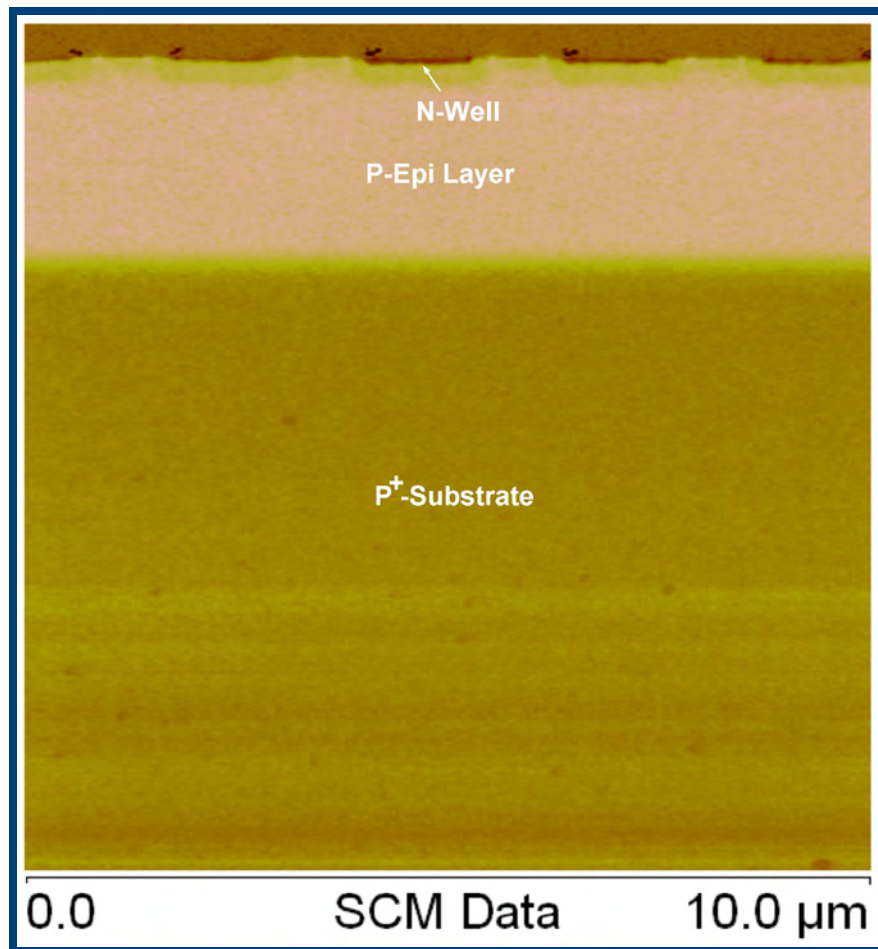


Figure 2.1.3: N-well in logic region, scanning capacitance microscopy (SCM) cross-section.

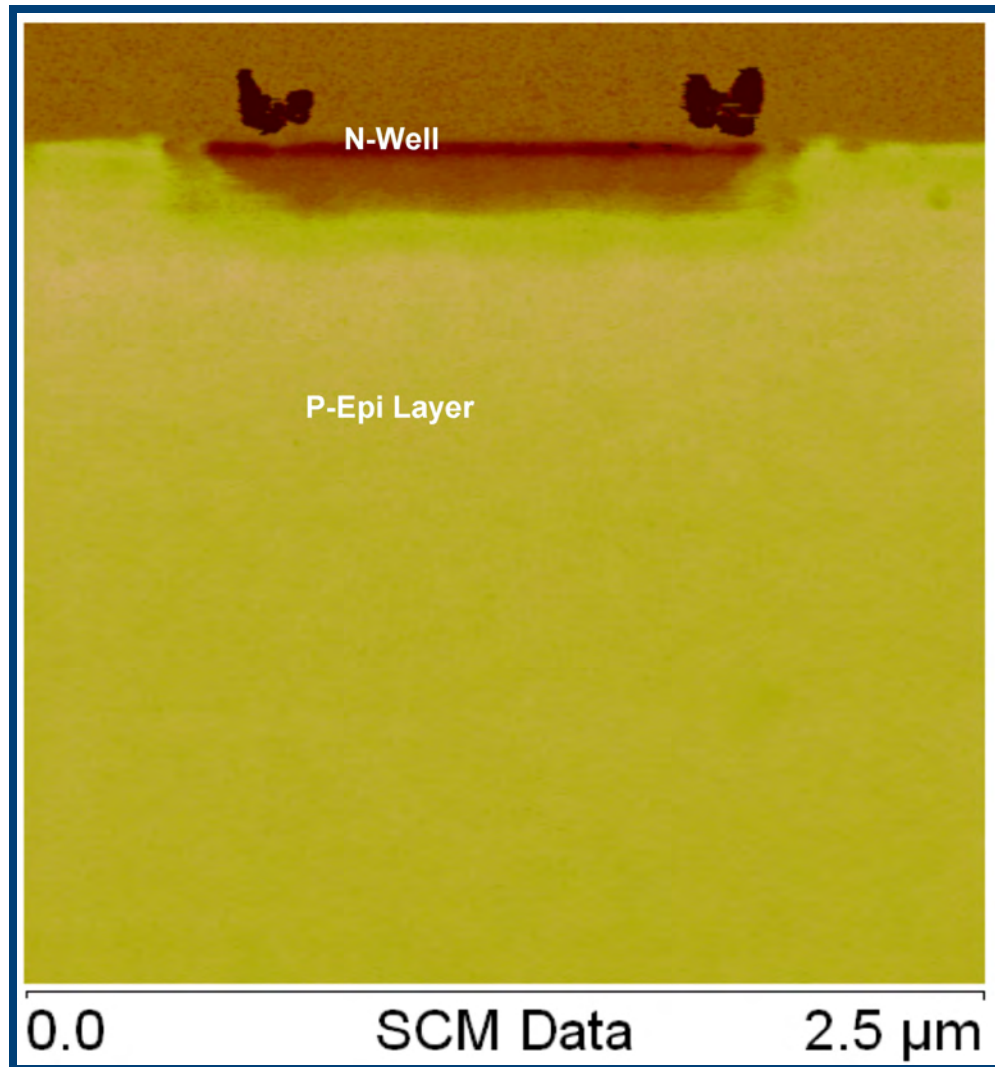


Figure 2.1.4: N-well, SCM cross-section.

Comments
• Highly doped P-type substrate; • Lightly doped P-type epitaxial layer, approximately 2.6 μm thick; • No N-well large enough for spreading resistance profiling.

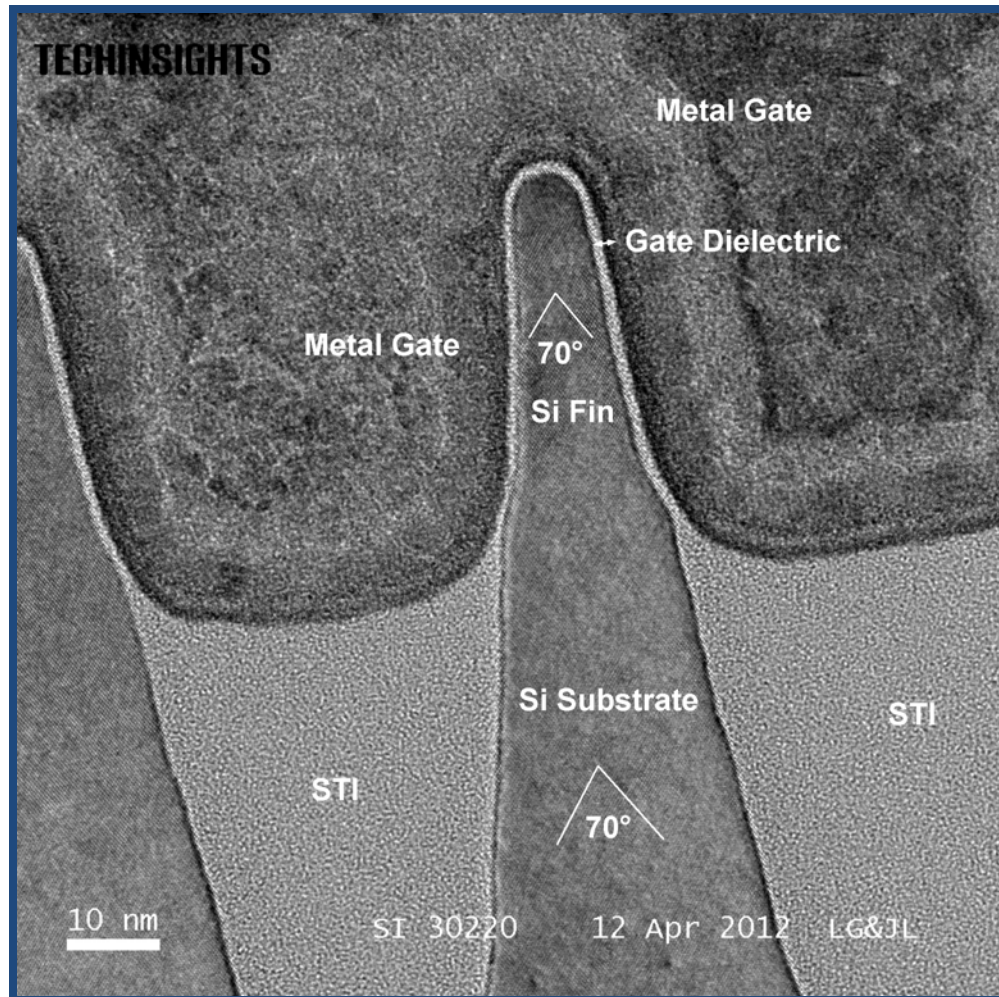


Figure 2.1.5: Silicon substrate with a silicon fin between STI regions, HRTEM lattice-fringe image.



Figure 2.1.6: Silicon fin of a PMOS transistor, HRTEM lattice-fringe image.

Feature	Dimension	Unit
Lattice fringe pitch (approximately)	3.14	Å

Comments

- Transistor channel (fin) along conventional <110> direction.

2.2 Fin and Isolation

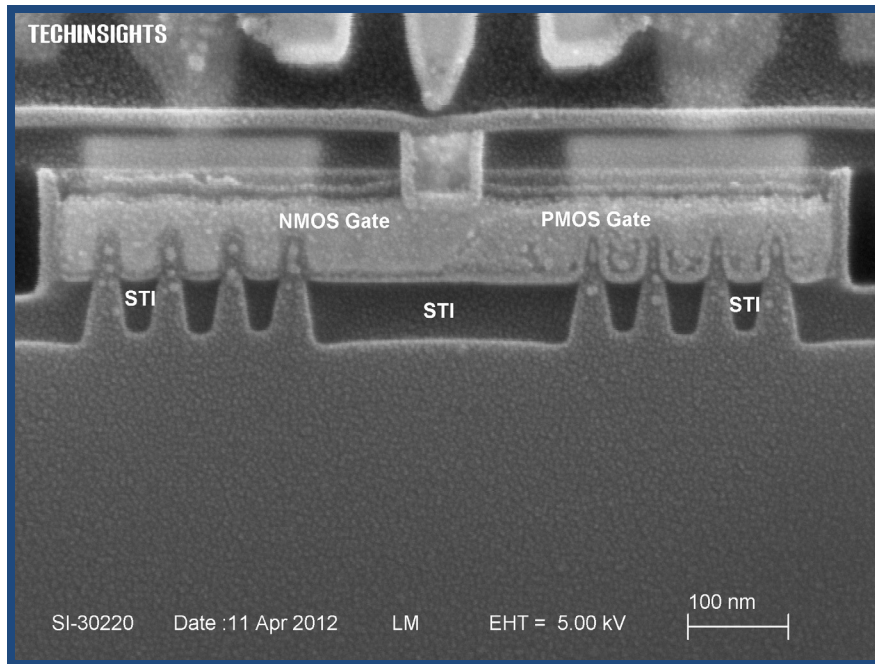


Figure 2.2.1: STI covered by a common gate, SEM cross-section, logic circuit.

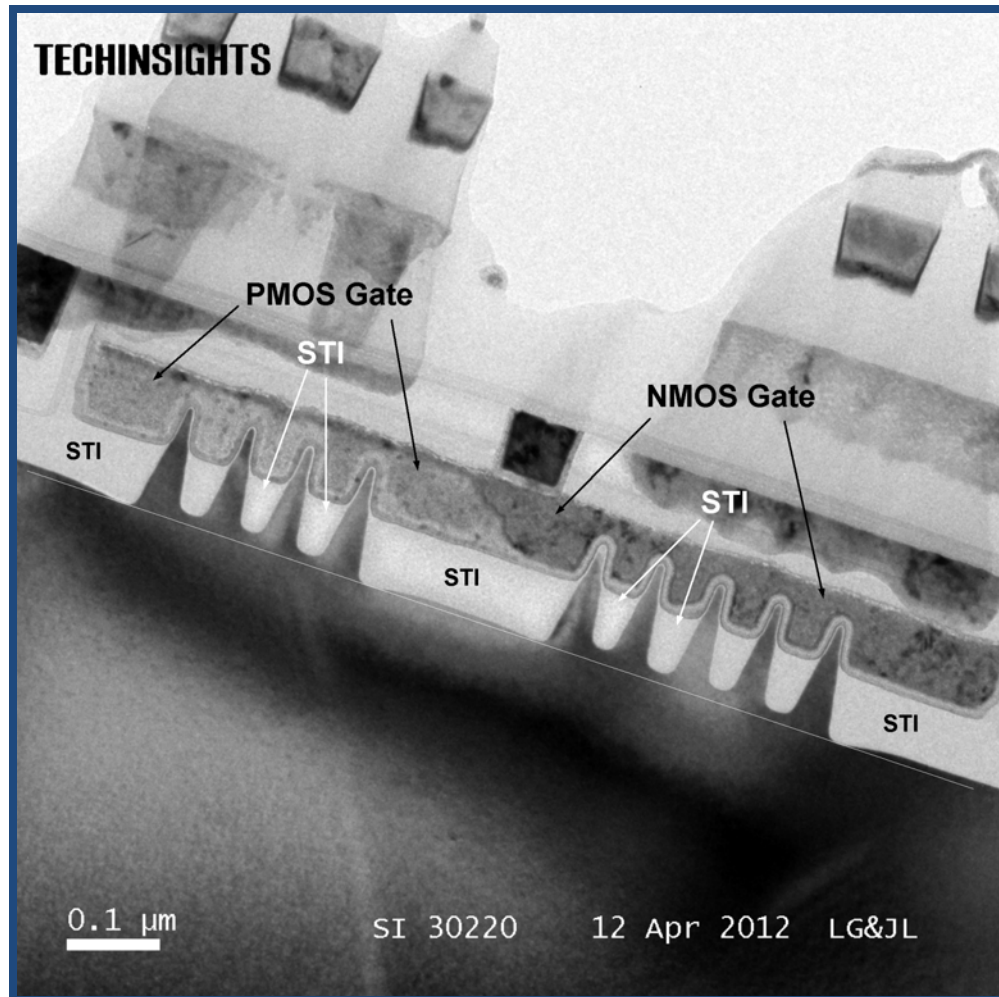


Figure 2.2.2: STI covered by a common gate, low magnification TEM cross-section, logic circuit.

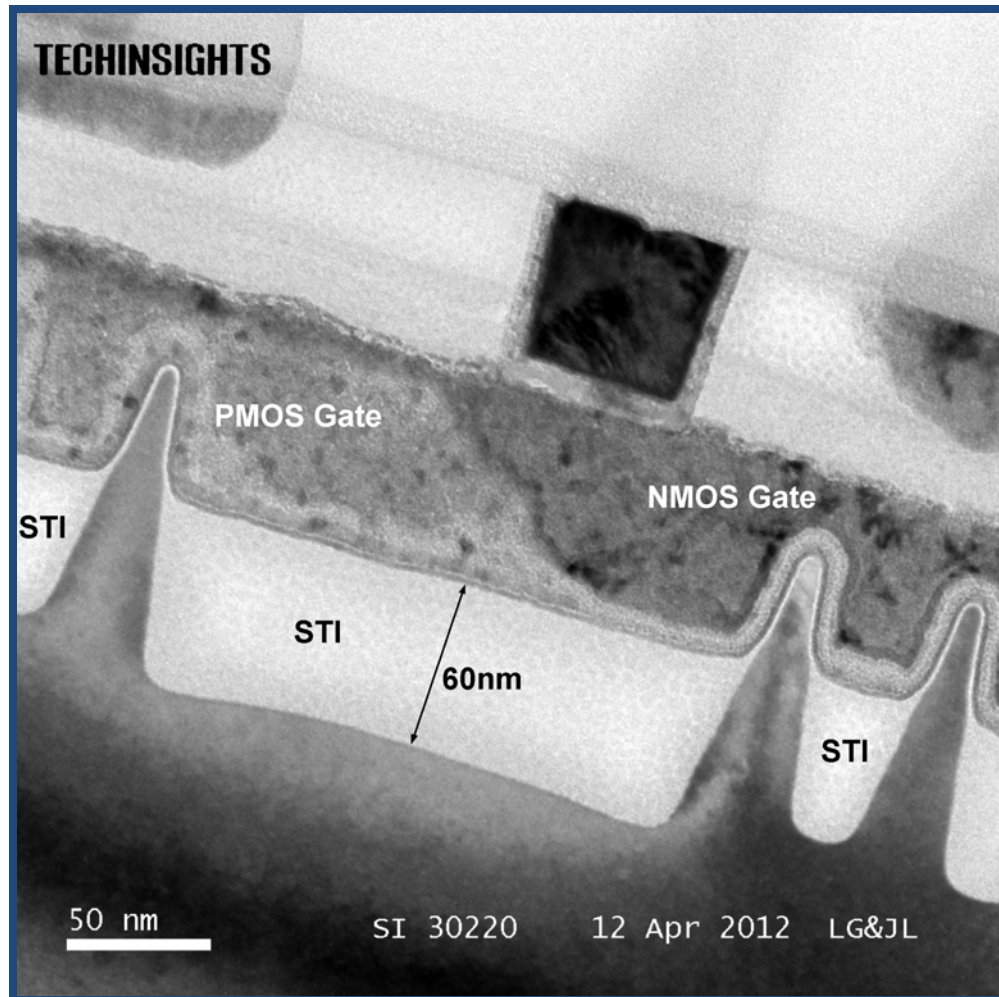


Figure 2.2.3: STI under the transition region between PMOS and NMOS gates, TEM cross-section along a common gate.

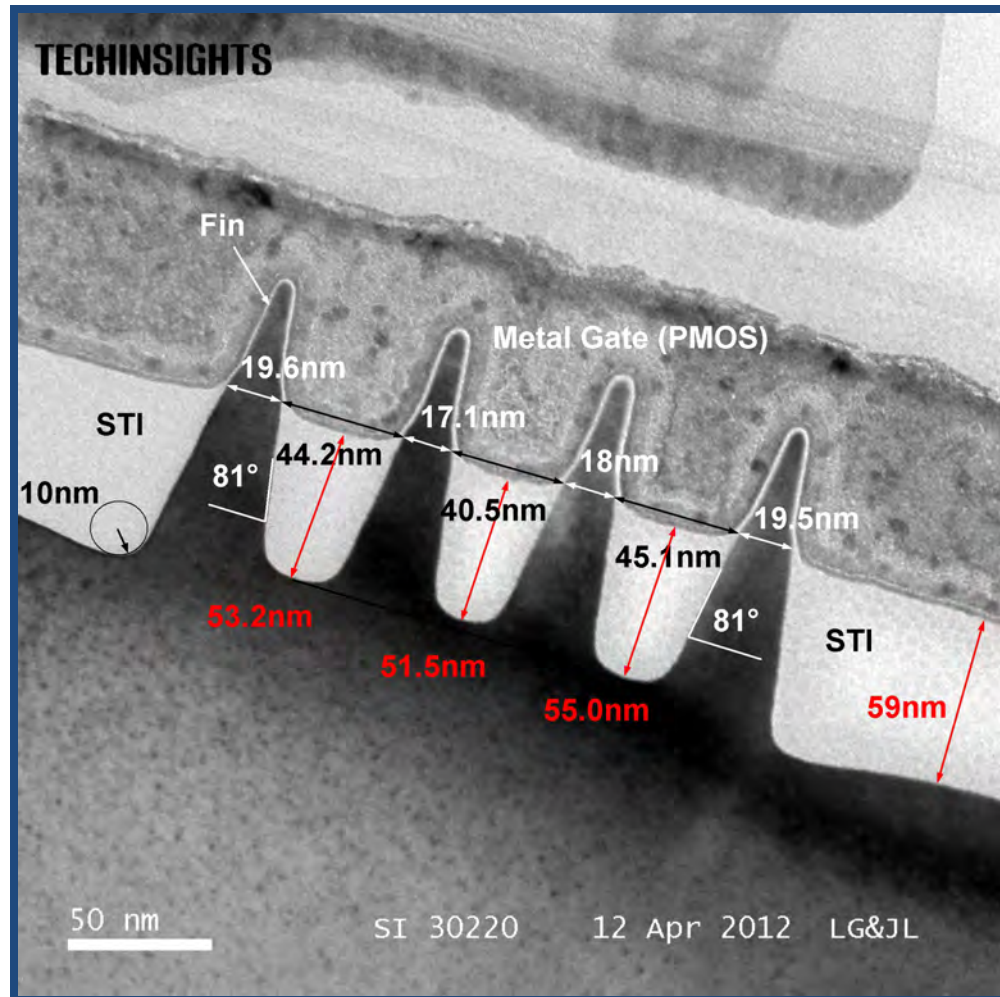


Figure 2.2.4: STI regions under PMOS metal gate, TEM cross-section.

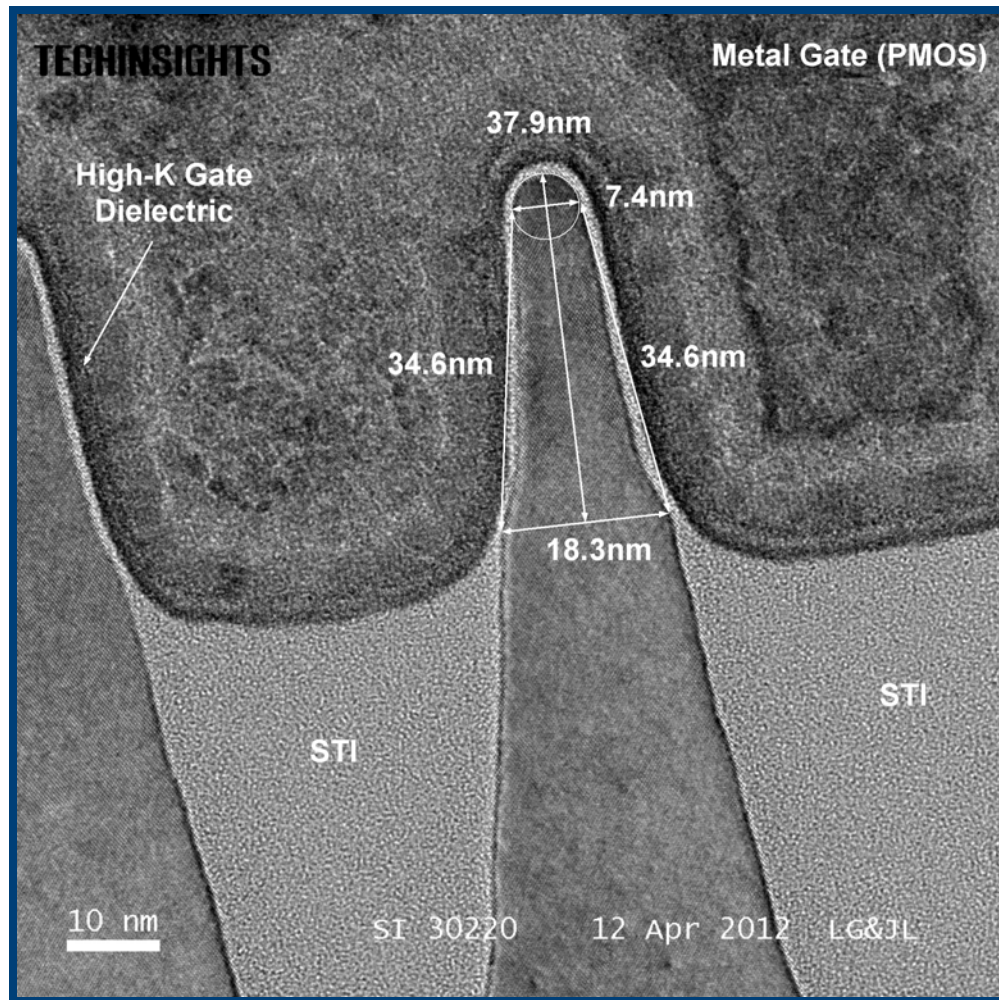


Figure 2.2.5: STI regions and silicon fin under PMOS metal gate, HRTEM lattice fringe image.

<i>Feature</i>	<i>Dimension</i>	<i>Unit</i>
PMOS fin height	38	nm
Fin width, bottom	18.3	nm
Fin width, top	7.4	nm
Fin top rounding radius	3.7	nm
Fin sidewall angle	84	grad
Fin pitch average	60	nm
Effective transistor channel width (sidewall + top + sidewall)	81	nm

Comments

- Tilted transition border in the cross-section along a common metal gate indicates that NMOS metal gates have been formed after formation of PMOS metal gates;
- Main process steps of fin formation;
 - o Hard mask deposition (likely silicon nitride with a pad oxide) and patterning. An immersion lithography with double patterning was likely used to achieve the 60 nm fin pitch;
 - o STI trench etch (~0.12 μm deep);
 - o Thermal oxidation and thick oxide fill;
 - o CMP planarization;
 - o Hard mask removal and recess etch (~0.07 μm deep) to expose fins and form lateral isolation (STI);
 - o Thermal oxidation to repair etch-induced damage and define silicon fin geometry (fin thinning and top rounding).

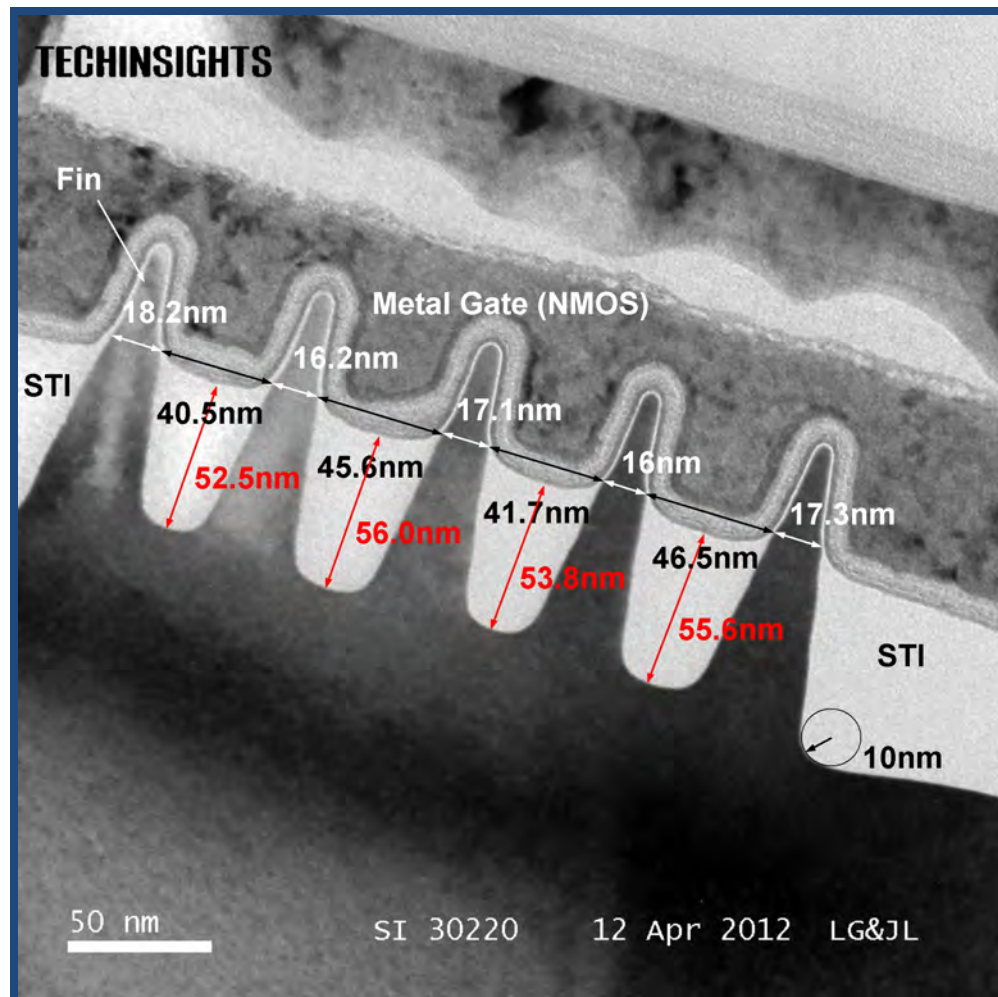


Figure 2.2.6: STI regions under NMOS metal gate, TEM cross-section.

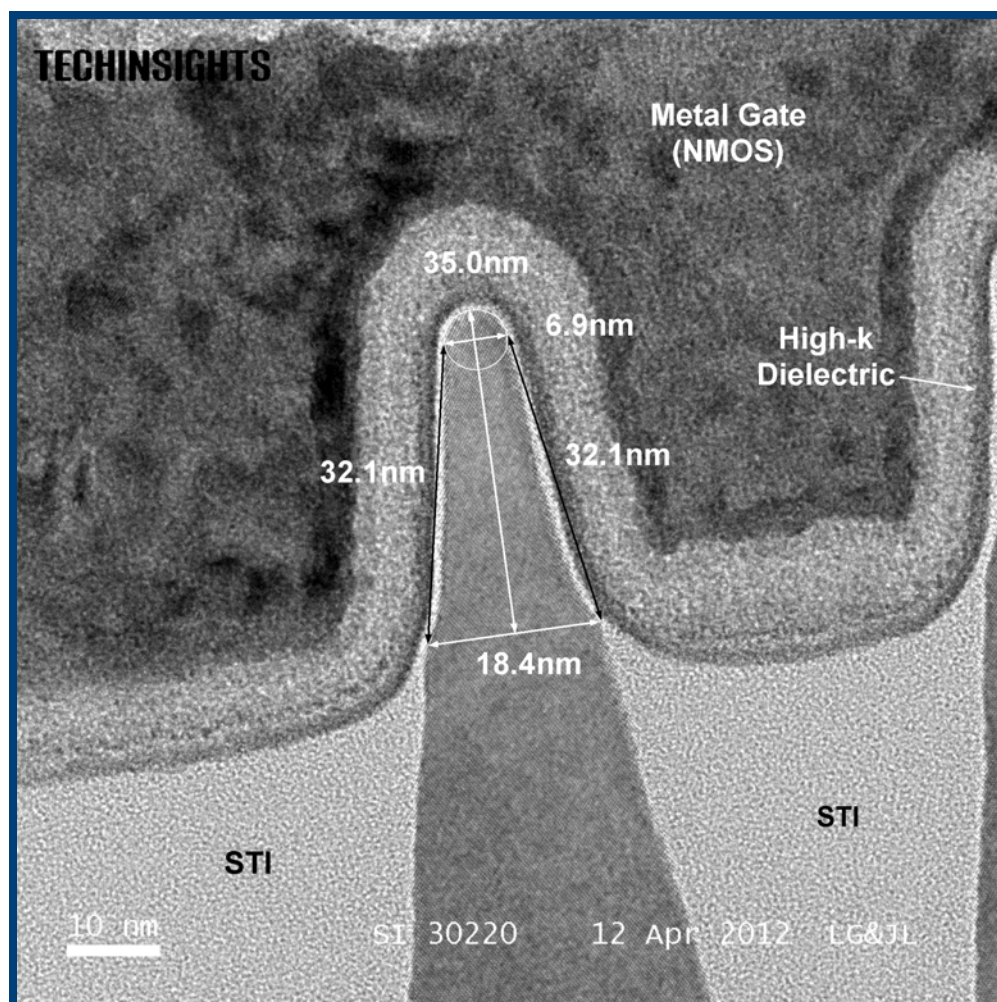


Figure 2.2.7: STI regions and silicon fin under NMOS metal gate with critical dimensions annotated, HRTEM lattice fringe image.

Feature	Dimension	Unit
NMOS silicon fin height	35	nm
Fin width, bottom	18.4	nm
Fin width, top	7	nm
Fin top rounding radius	3.5	nm
Fin sidewall angle	84	grad
Fin pitch	60	nm
Effective NMOS transistor channel width (sidewall + top + sidewall)	75	nm
Silicon fin pitch	60	nm

Comments

- Tilted transition border in the cross-section along a common metal gate indicates that NMOS metal gates have been formed after formation of PMOS metal gates;
- Silicon fin of NMOS transistor has in general the same geometry as that of PMOS transistor;
- Measured NMOS fin height is slightly smaller than that of PMOS transistor; this may be a result of statistical variation and measurement error.

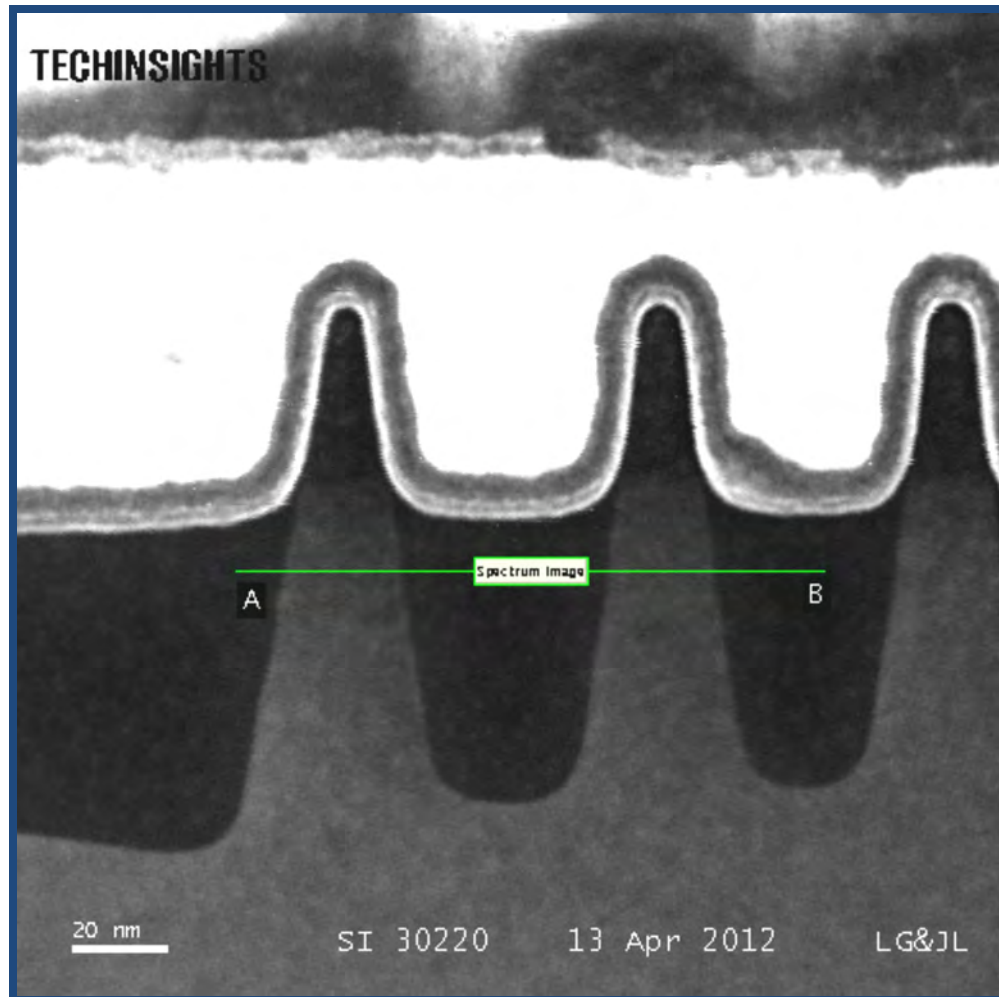


Figure 2.2.8: EELS horizontal line scan profile through STI regions under a metal gate, HAADF survey image.

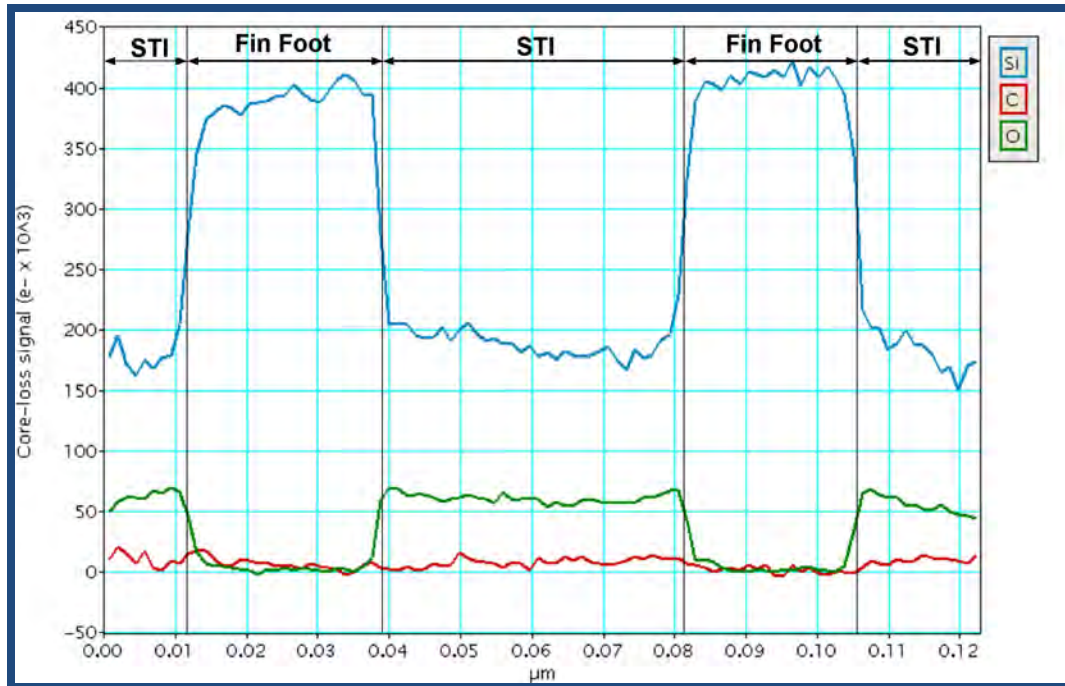


Figure 2.2.9: Element profiles of STI and fin foot regions, EELS line scan.

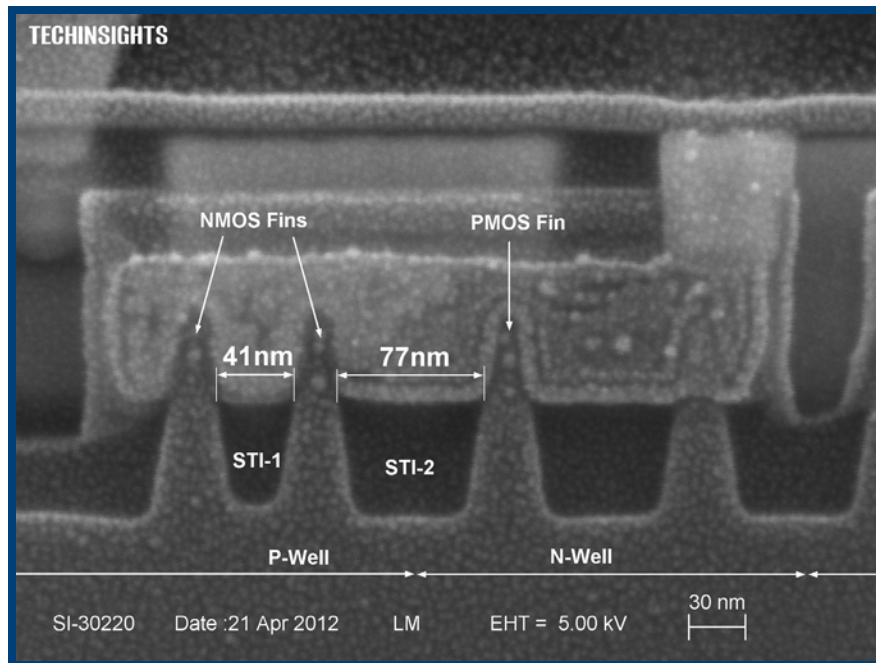


Figure 2.2.10: STI regions under common metal gate, SEM cross-section of SRAM in wordline direction.

<i>Feature</i>	<i>Dimension</i>	<i>Unit</i>
Wide STI depth (under gate)	60	nm
Minimum STI depth	51	nm
Minimum STI width	41	nm
Minimum fin-defining STI pitch	60	nm
STI and fin total depth	~110	nm
STI sidewall angle	81	degree
Bottom STI corner rounding radius	10	nm

Table 2.2.1: STI dimensions.

<i>Comments</i>
• Shallow trench isolation (STI) used to define silicon fins used in Tri-Gate transistors; • Aggressive scaling of STI and active area width likely using immersion lithography with double patterning; • A few nanometer difference between even and odd STI depths likely due to a double patterning process and etch loading effect; • Well rounded bottom STI corners; • No voids, seams and other defects in the filling oxide; • Edge of wider STI region is slightly deeper than narrow fin-defining STIs due to micro-loading effect (non-uniform etching induced by varied etch process loading due to variations of pattern size and density); • Minimum STI width is 41 nm for fin-defining STI used within the same well (i.e. P-well in Figure 2.2.10). • For the STI that is used between P- and N-wells, the minimum STI width is larger (77 nm in Figure 2.2.10) likely due to electrical requirements.

2.3 Tri-Gate High-k Metal Gate Transistors

2.3.1 Topographical Analysis of Logic Tri-Gate Transistors

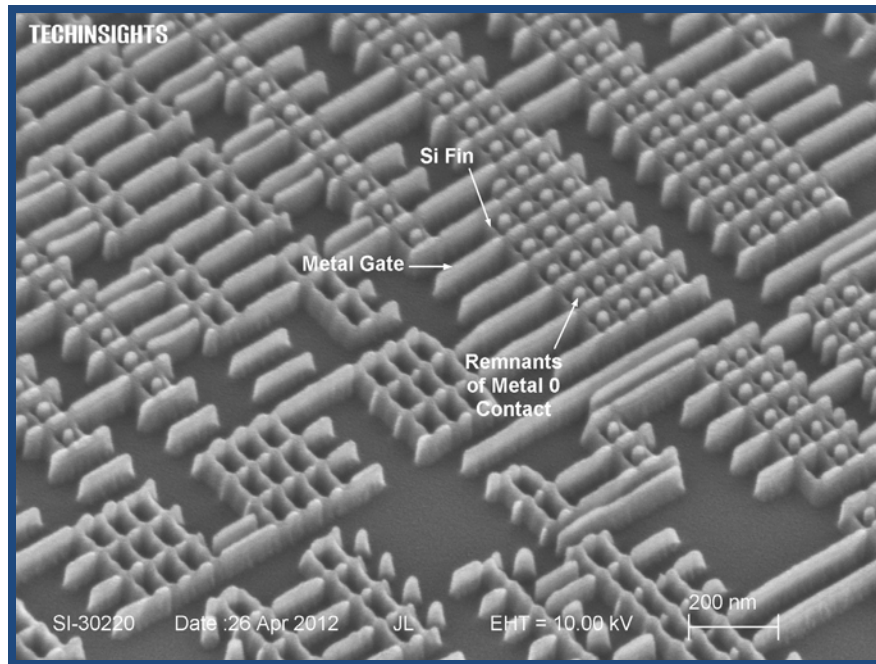


Figure 2.3.1.1: Logic Tri-Gate transistors delayed to metal gate level, SEM tilted view.

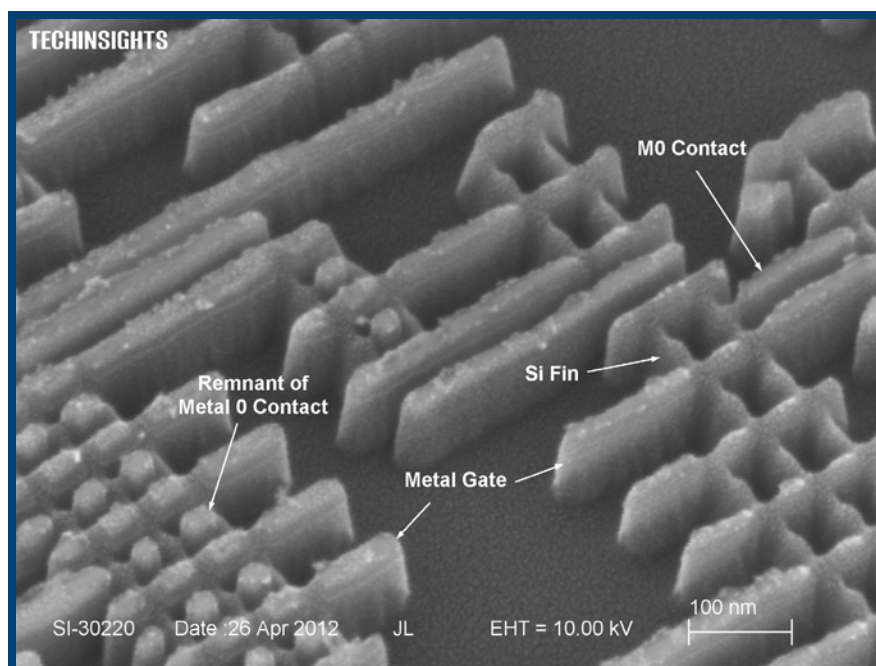


Figure 2.3.1.2: Tri-Gate transistors delayed to metal gate level, high magnification SEM tilted view.

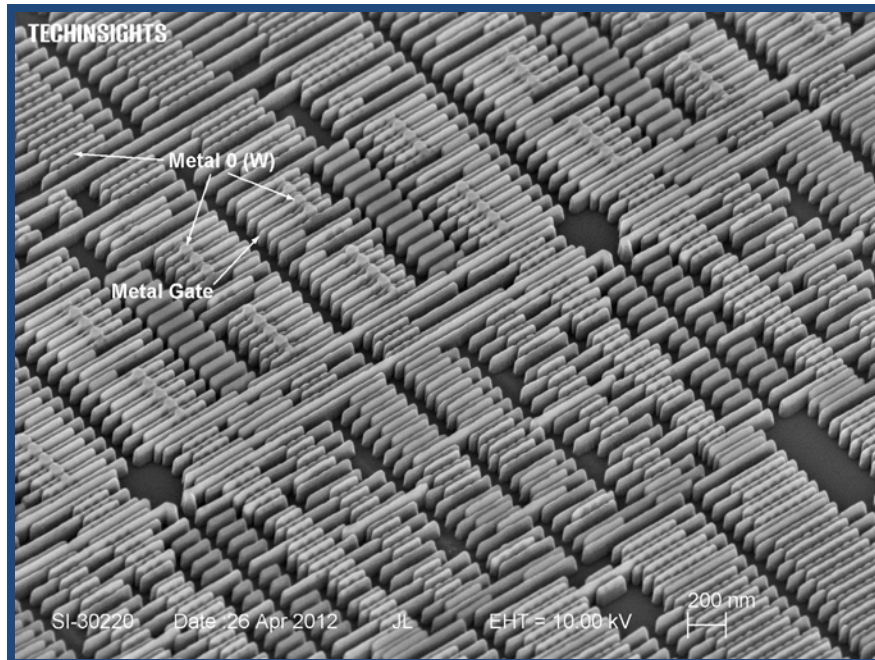


Figure 2.3.1.3: Logic Tri-Gate transistors delayed to metal 0 level, SEM tilted view.

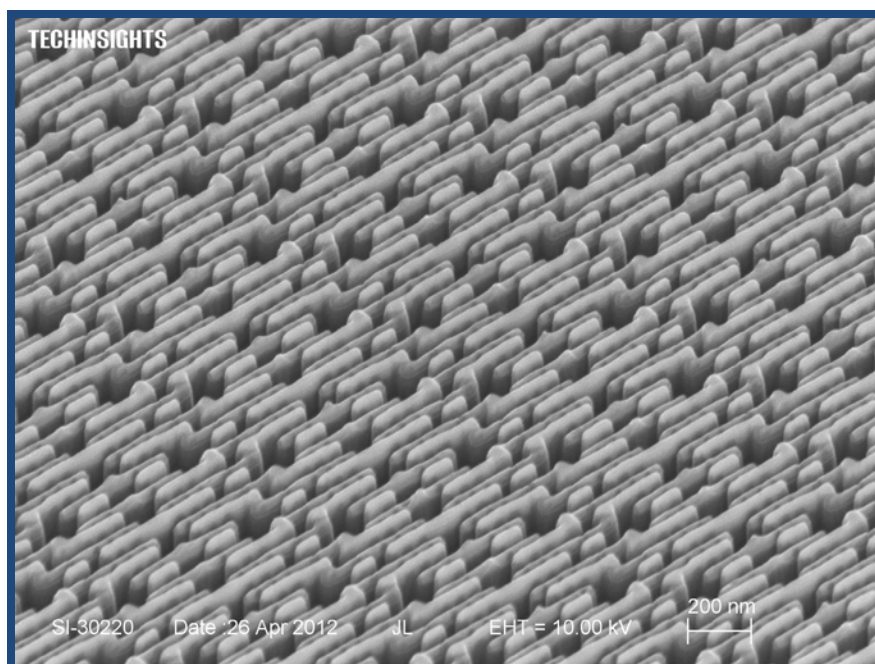


Figure 2.3.1.4: Tri-Gate transistors delayed to metal 0 level, SEM tilted view, SRAM area.

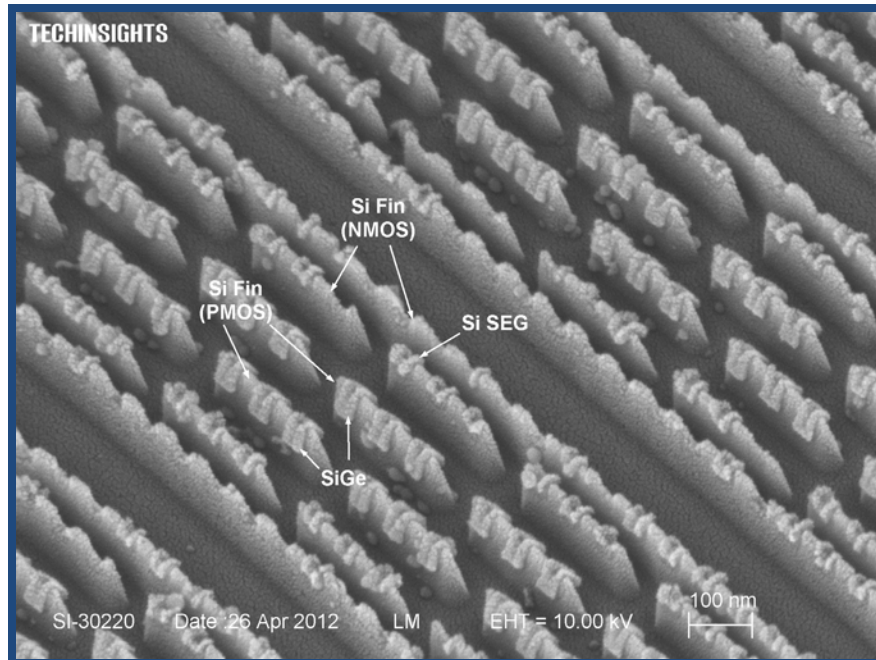


Figure 2.3.1.5: Tri-Gate transistors delayed to Si fin level, SEM tilted view, SRAM area.

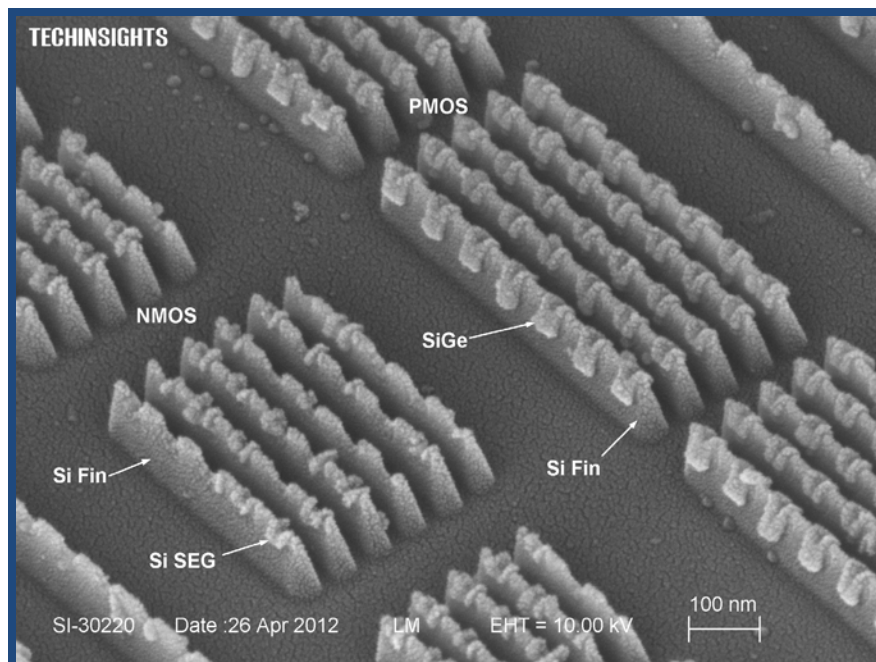


Figure 2.3.1.6: Logic Tri-Gate transistors delayed to Si fin level, SEM tilted view.

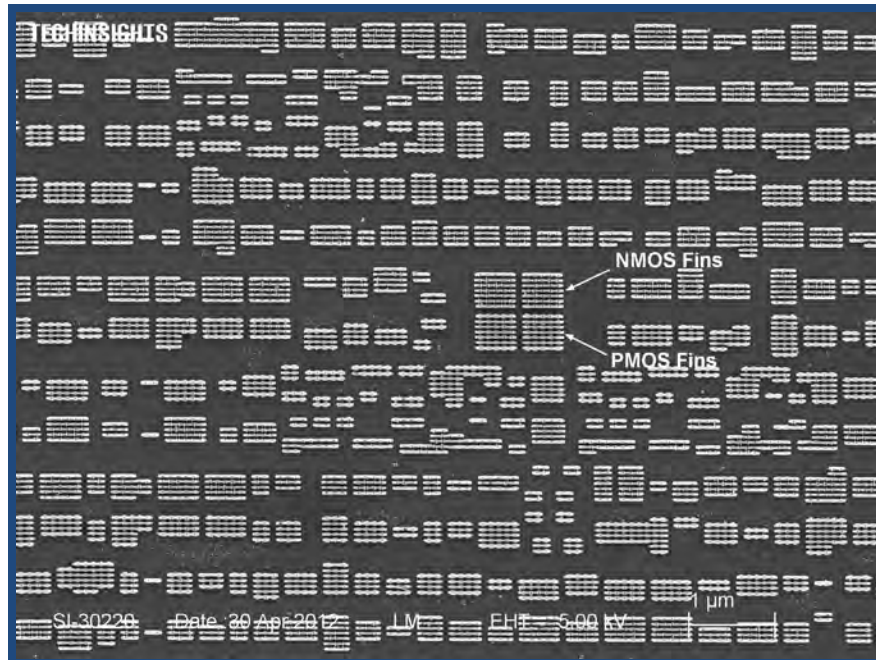


Figure 2.3.1.7: Logic NMOS and PMOS Tri-Gate transistors delayed to fin level, low magnification SEM topographical view.

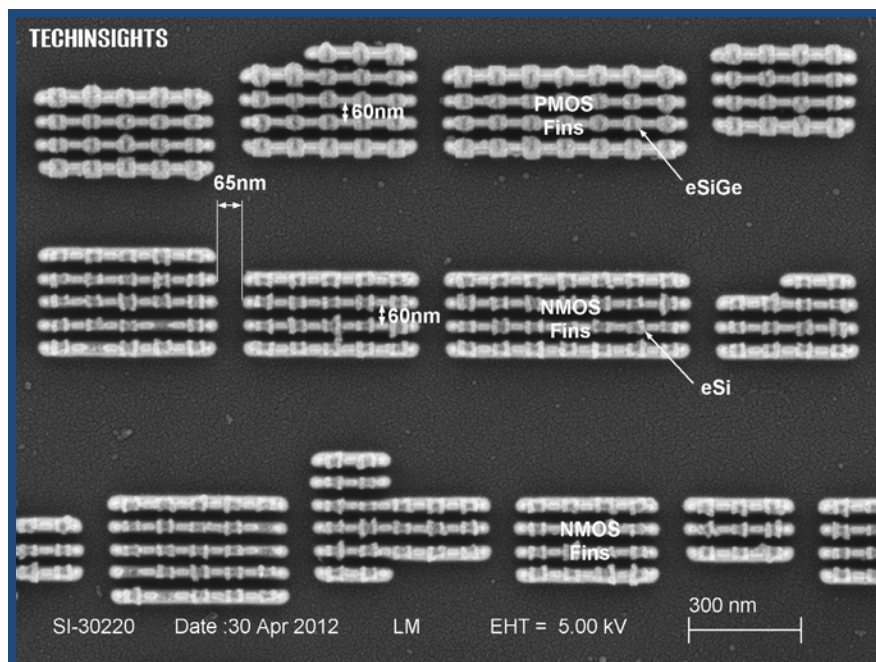


Figure 2.3.1.8: NMOS and PMOS Tri-Gate transistors at fin level, SEM topographical view.

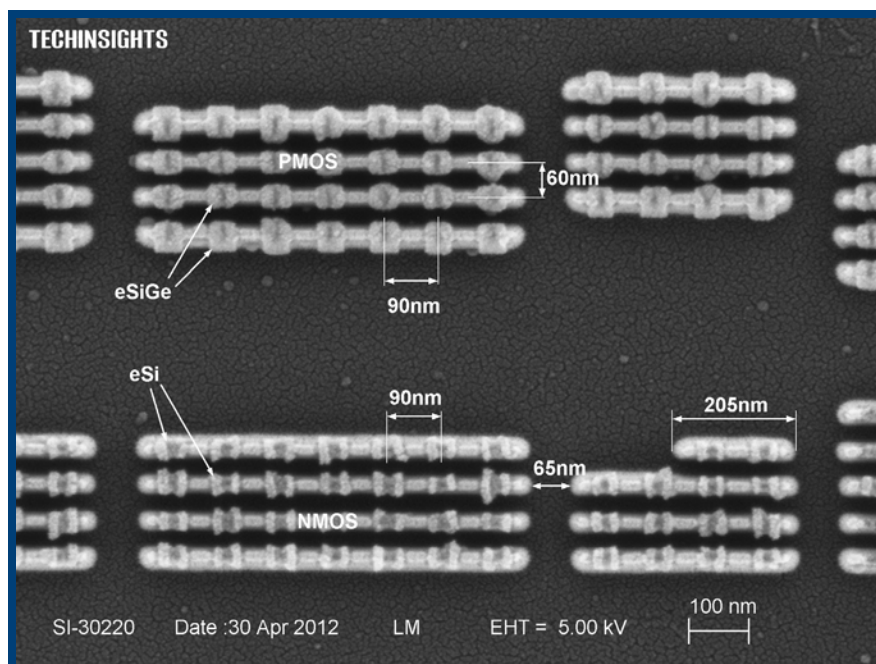


Figure 2.3.1.9: NMOS and PMOS fins with fin and contact pitches annotated, high magnification SEM topographical view.

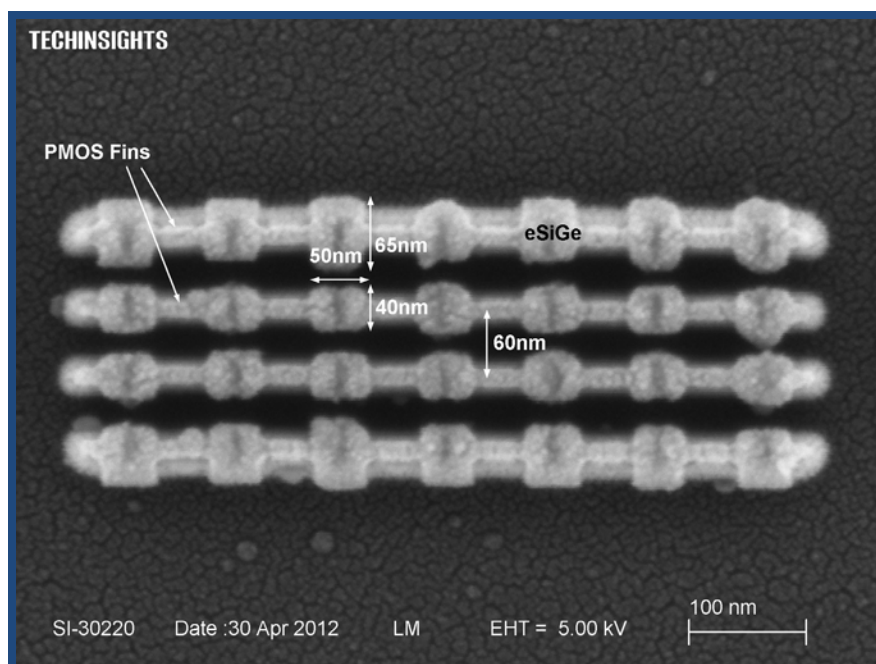


Figure 2.3.1.10: PMOS fins with eSiGe dimensions and fin pitch annotated, high magnification SEM topographical view.

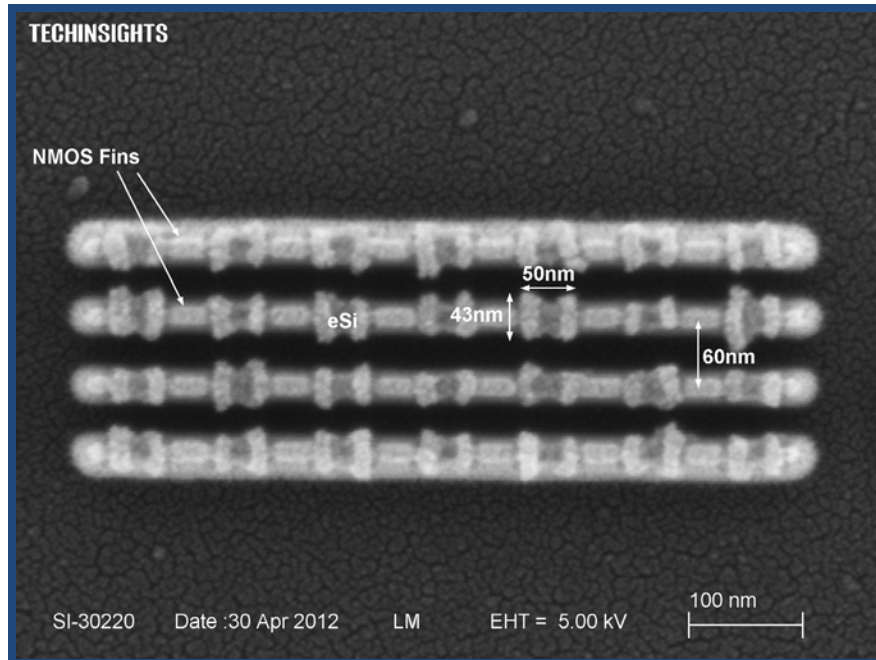


Figure 2.3.1.11: NMOS fins with eSi dimensions and fin pitch annotated, high magnification SEM topographical view.

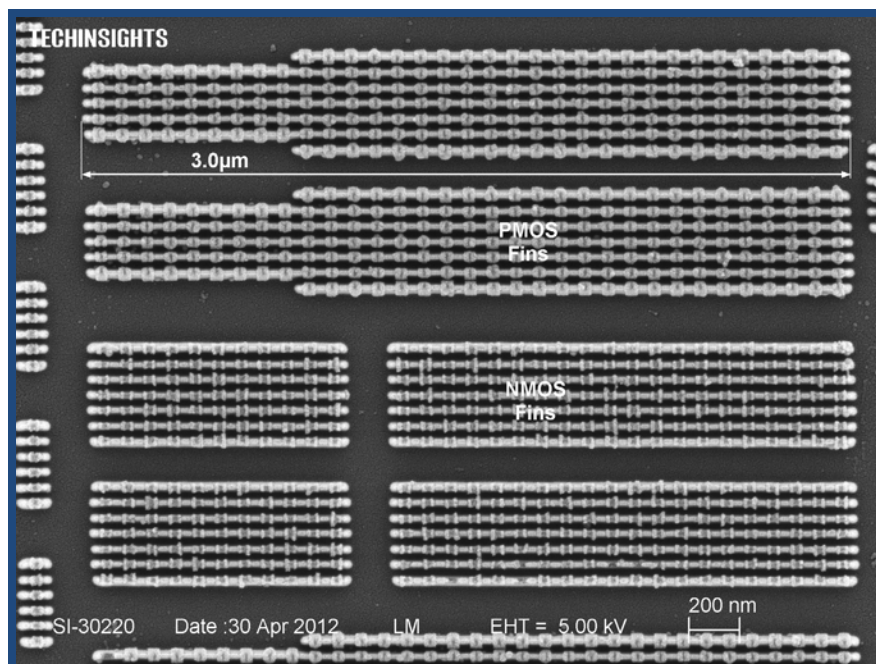


Figure 2.3.1.12: Long NMOS and PMOS fins, low magnification SEM topographical view.

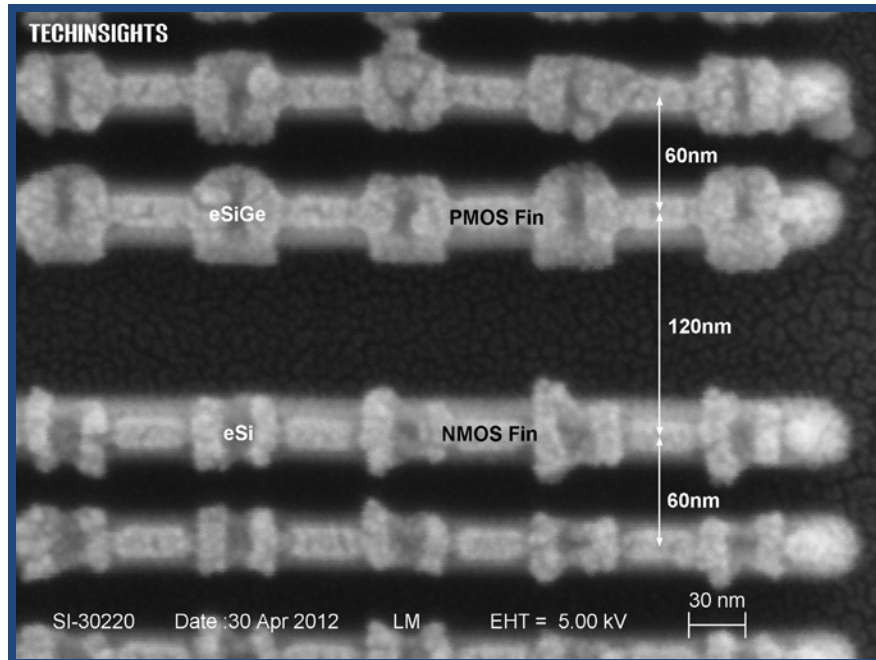


Figure 2.3.1.13: NMOS and PMOS fins at minimum 120 nm distance to each other, high magnification SEM topographical view.

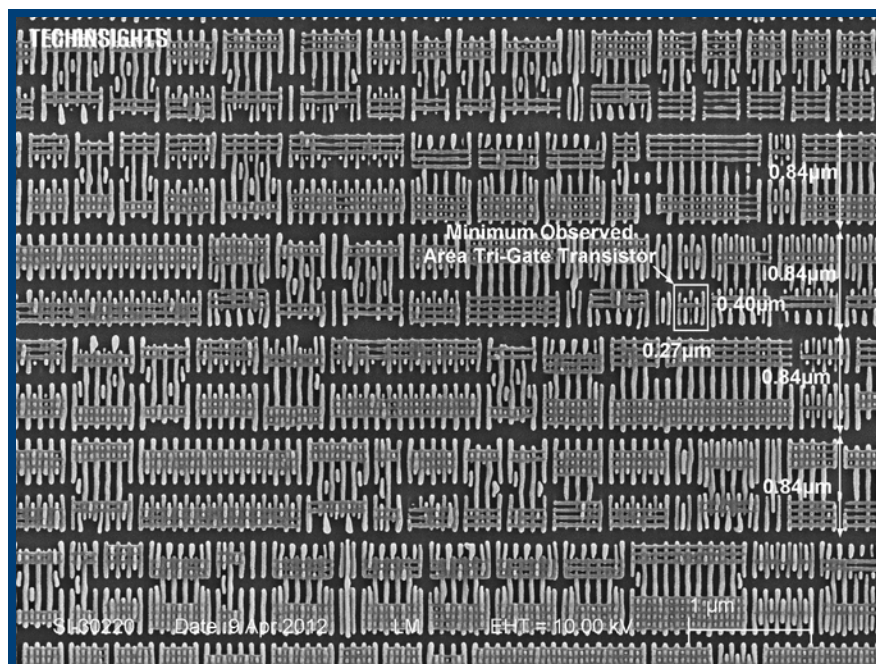


Figure 2.3.1.14: Standard cells delayed to gate level, with minimum observed Tri-Gate transistor annotated, SEM topographical image.

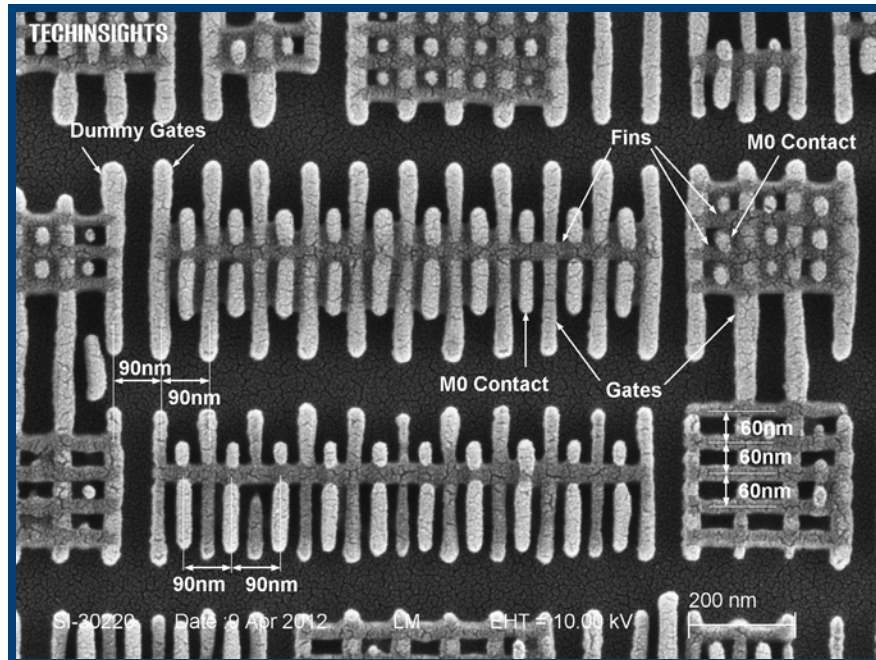


Figure 2.3.1.15: Logic Tri-Gate transistors at gate level with fin, gate and contact pitches annotated, SEM topographical image.

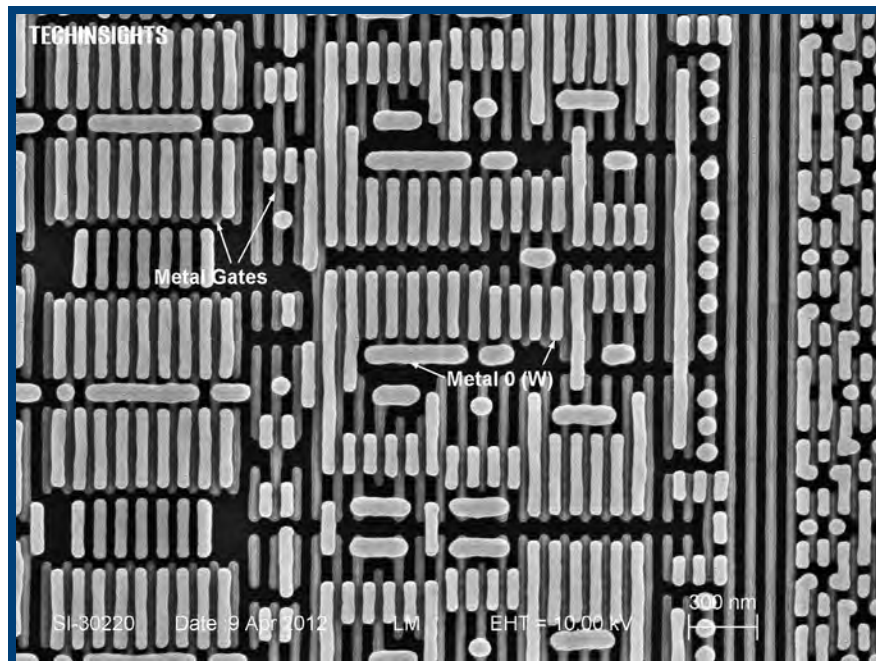


Figure 2.3.1.16: Tri-Gate transistors at metal 0 level, SEM topographical image.

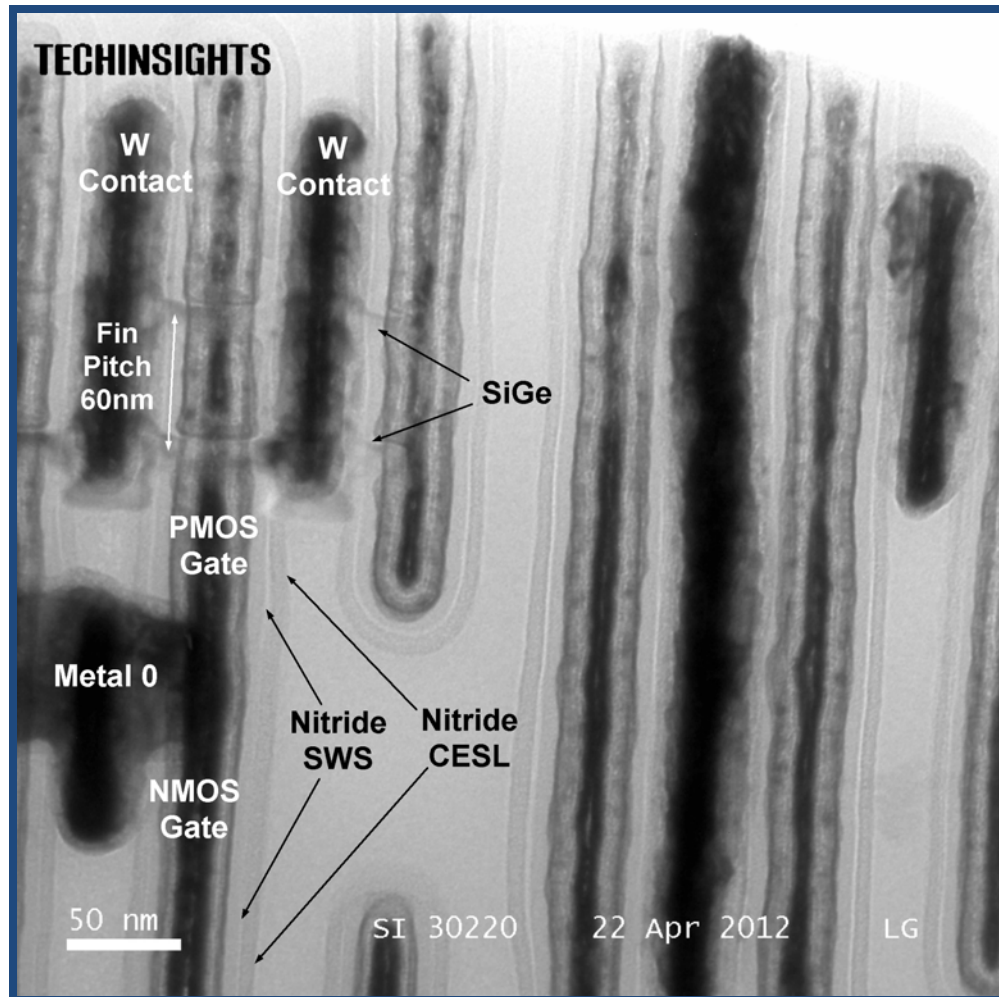


Figure 2.3.1.17: PMOS and NMOS tri-gate transistors near a transition region, higher magnification TEM plan view image.

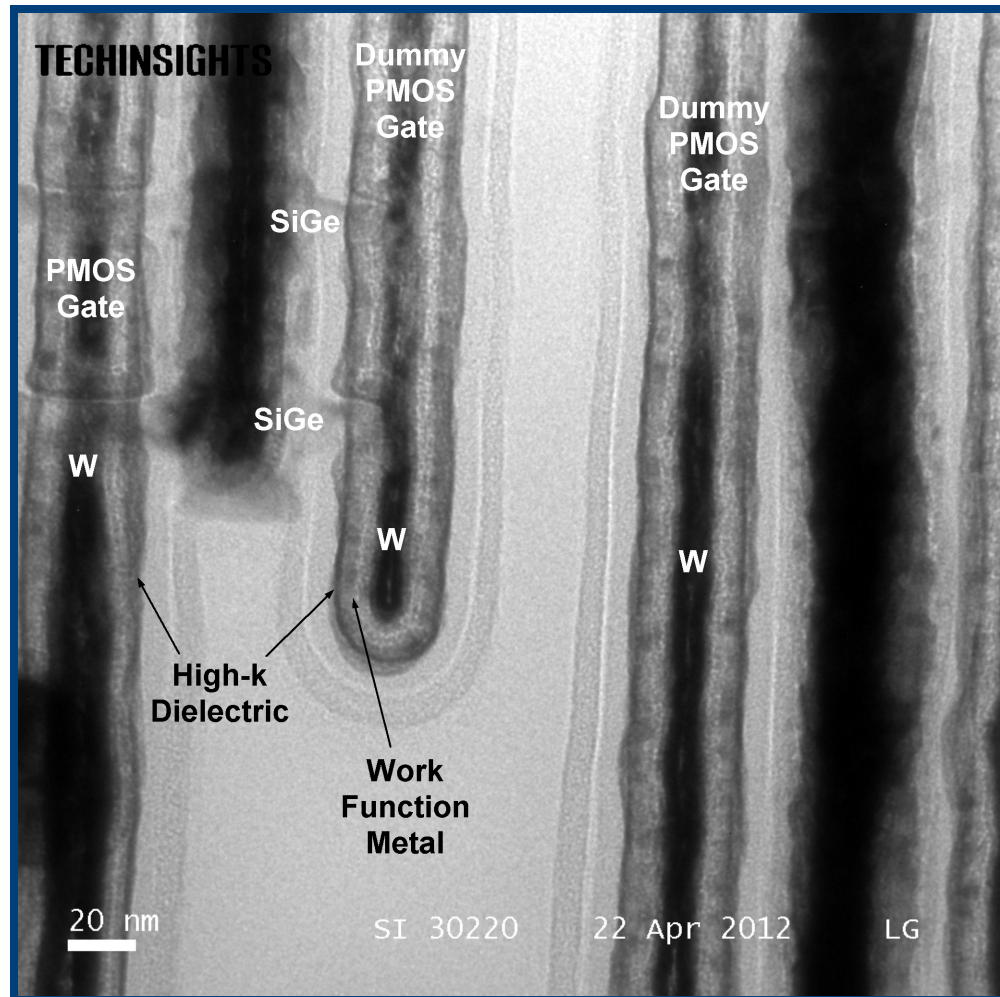


Figure 2.3.1.18: PMOS gate with high-k gate dielectric and SiGe source/drain regions, high magnification TEM plan view image.

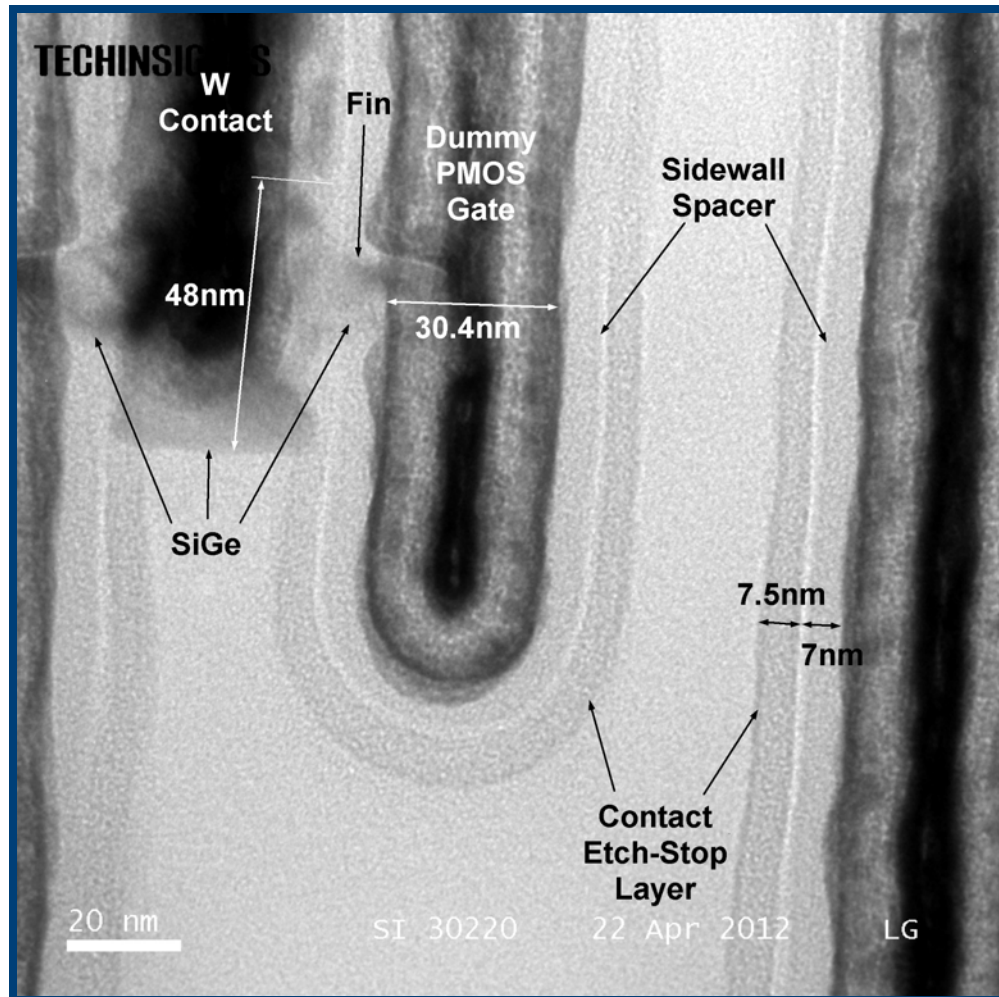


Figure 2.3.1.19: Detailed structure of PMOS transistor, high magnification TEM plan view image.

<i>Feature</i>	<i>Dimension</i>	<i>Unit</i>
Standard cell height	0.84	μm
Minimum observed Tri-gate transistor length	0.27	μm
Minimum observed Tri-gate transistor width	0.40	μm
Minimum observed gate pitch	90	nm
Minimum observed fin pitch	60	nm
Minimum observed space between fins in the fin direction	65	nm
Minimum observed Tri-gate transistor area	0.108	μm ²
Minimum observed fin length	205	nm
Maximum observed fin length	3	μm
Embedded SiGe maximum width (across fin)	65	nm
Embedded SiGe minimum width (across fin)	40	nm
Embedded SiGe maximum length (along fin)	50	nm
Embedded SiGe minimum length (along fin)	50	nm
Embedded Si maximum width (across fin)	50	nm
Embedded Si minimum width (across fin)	40	nm
Embedded Si maximum length (along fin)	50	nm
Embedded Si minimum length (along fin)	50	nm

Comments

- PMOS and NMOS Tri-Gate transistors with a single silicon fin or multiple fins;
- Each Tri-gate transistor has a pair of dummy gates, one gate on each edge;
- Silicon fins have the same pitch of 60 nm;
- Minimum observed fin length of 205 nm;
- Minimum length fin carries two eSiGe (or eSi:C) source/drain regions;
- Minimum observed contacted metal gate pitch is 90 nm;
- Dummy gates used at both edges of logic transistors;
- There are dummy metal 0 and metal gate patterns;
- Single Tri-Gate transistor has a minimum observed size of 0.108 μm^2 , which is the same area occupied by a six-transistor SRAM cell (see Section 3). The reason is that the even a minimum size Tri-Gate transistor has and a 270 nm long dummy gate on each side, and non-shared contacts. In contrast, SRAM cell has no dummy gates (since their function is performed by the gates from neighbor cells), and SRAM cell contacts are shared with the neighbor cells.

2.3.2 Cross-Sectional Analysis of Tri-Gate PMOS Transistors

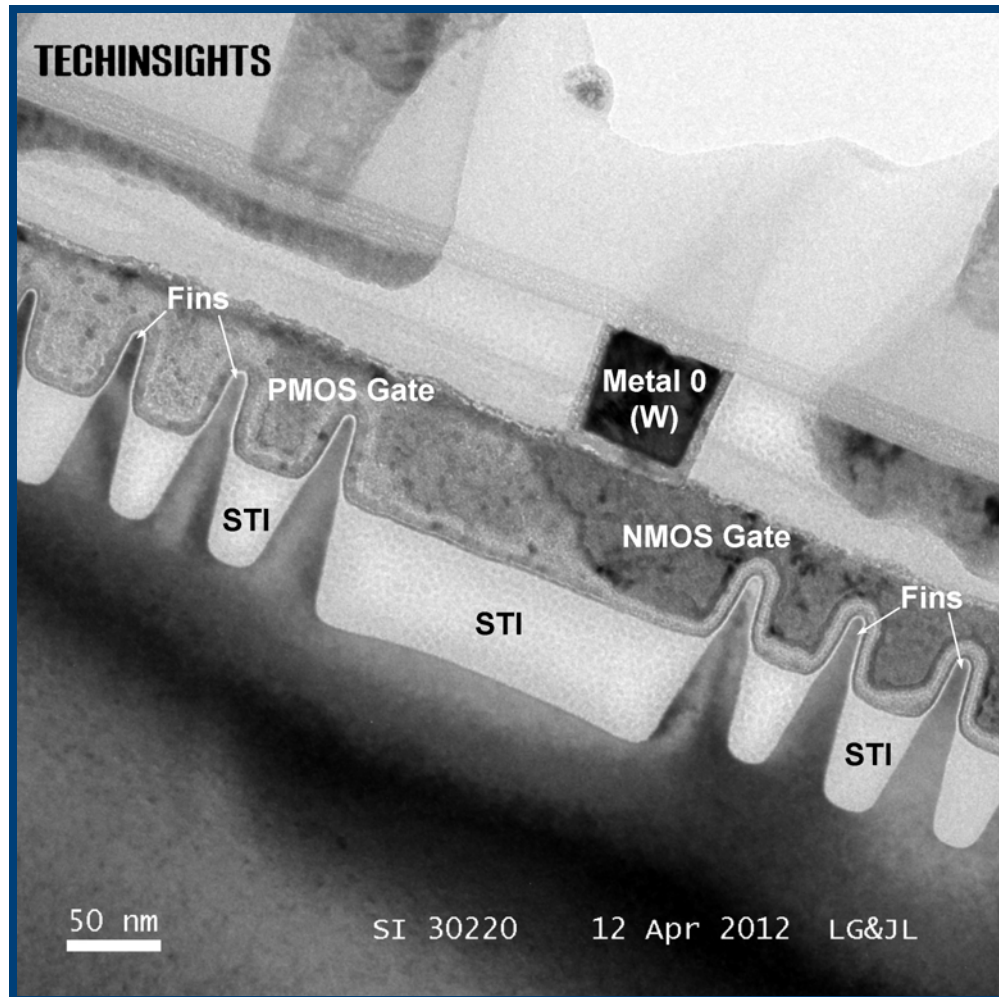


Figure 2.3.2.1: PMOS and NMOS logic transistors sectioned along a common gate in gate width direction, TEM cross-section.

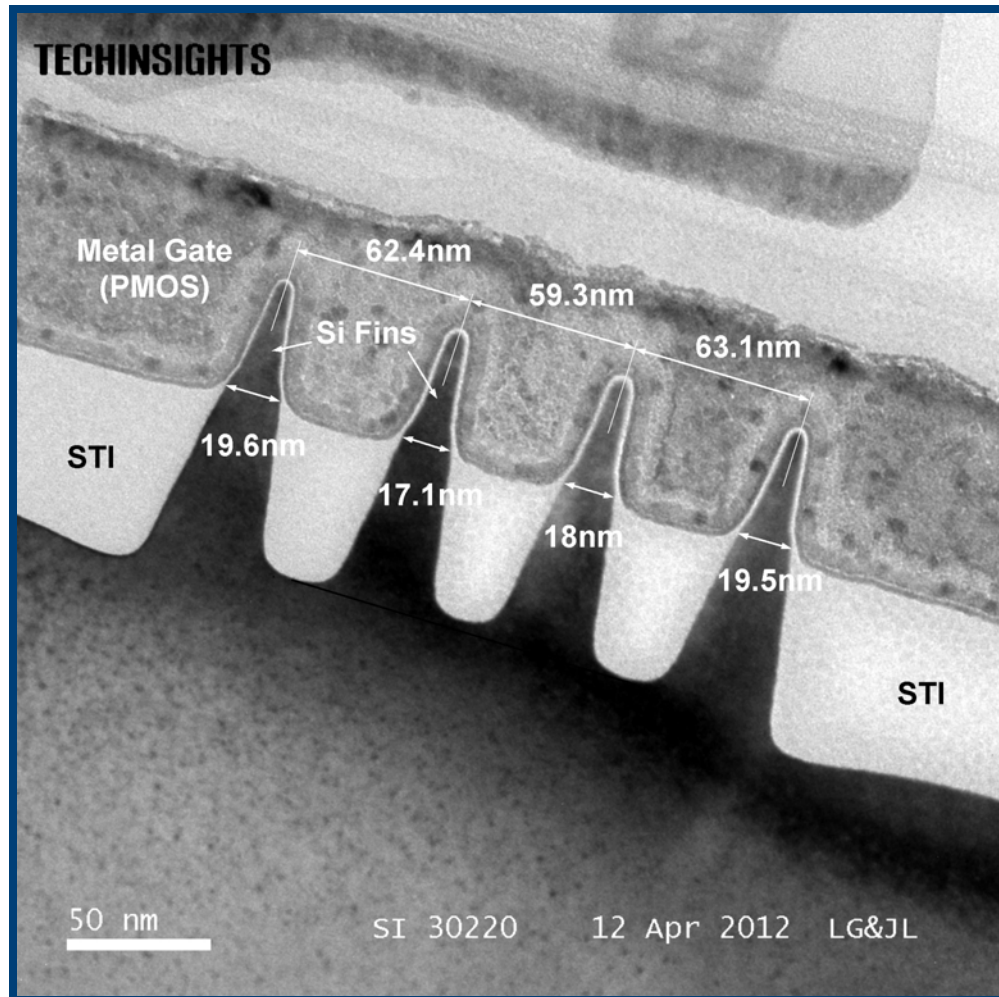


Figure 2.3.2.2: Logic PMOS transistor sectioned along a PMOS gate and across silicon fins, TEM cross-section with fin widths and pitches annotated.

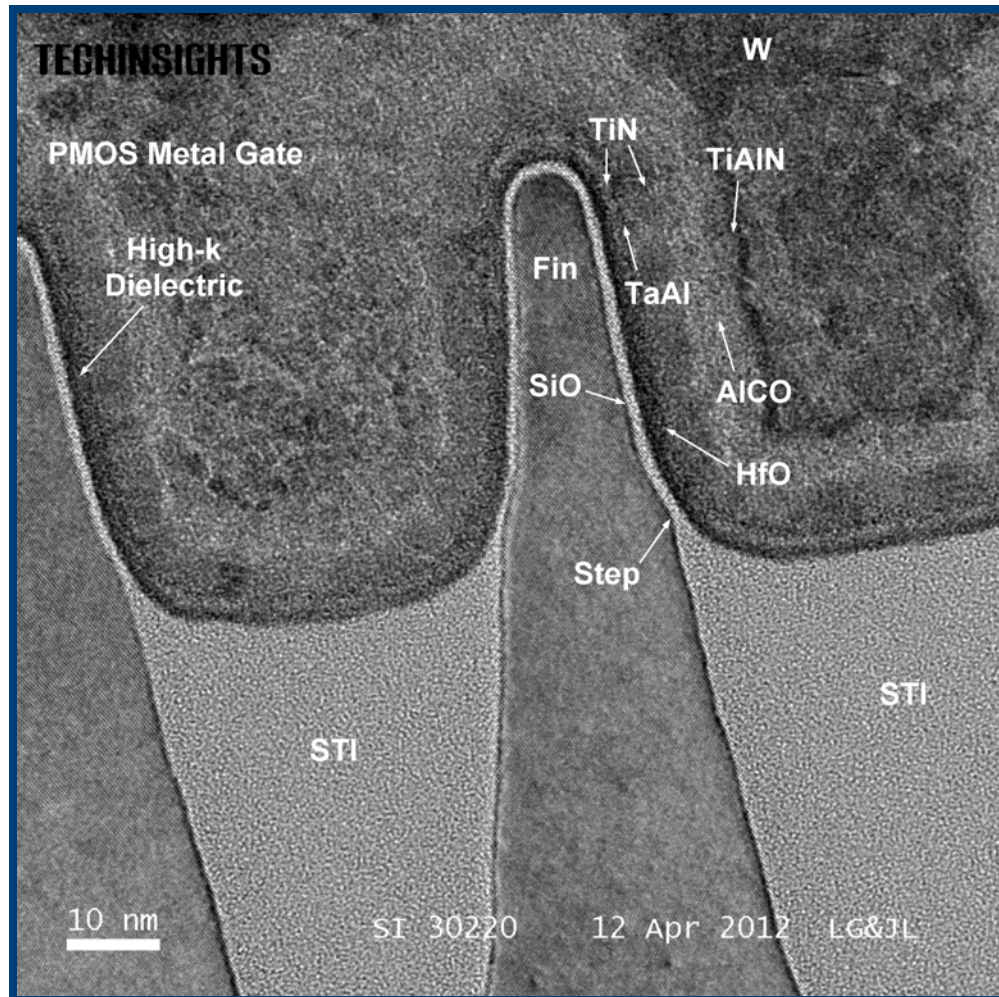


Figure 2.3.2.3: PMOS metal gate layers, HRTEM image.



Figure 2.3.2.4: Middle part of the PMOS transistor fin with gate dielectric and metal gate layers, HRTEM image.

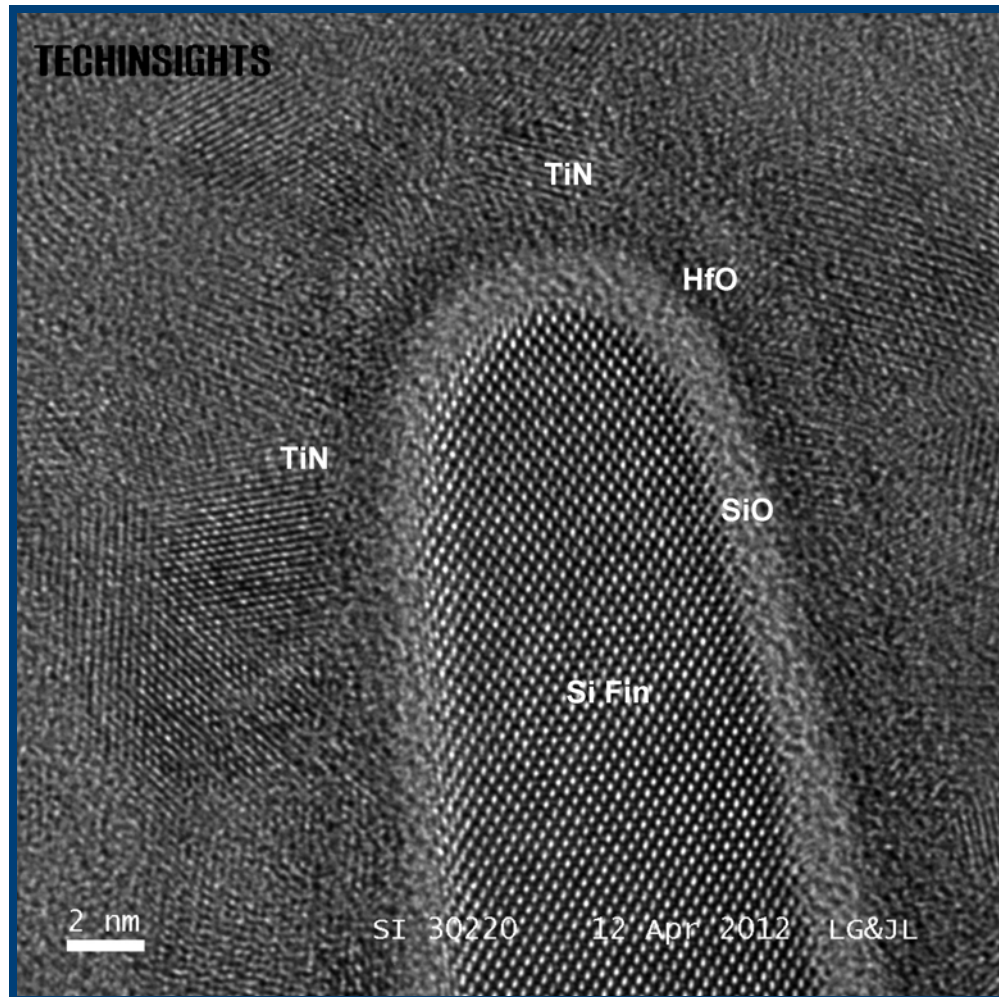


Figure 2.3.2.5: Upper part of the PMOS transistor fin with gate dielectric and metal gate layers, HRTEM image.

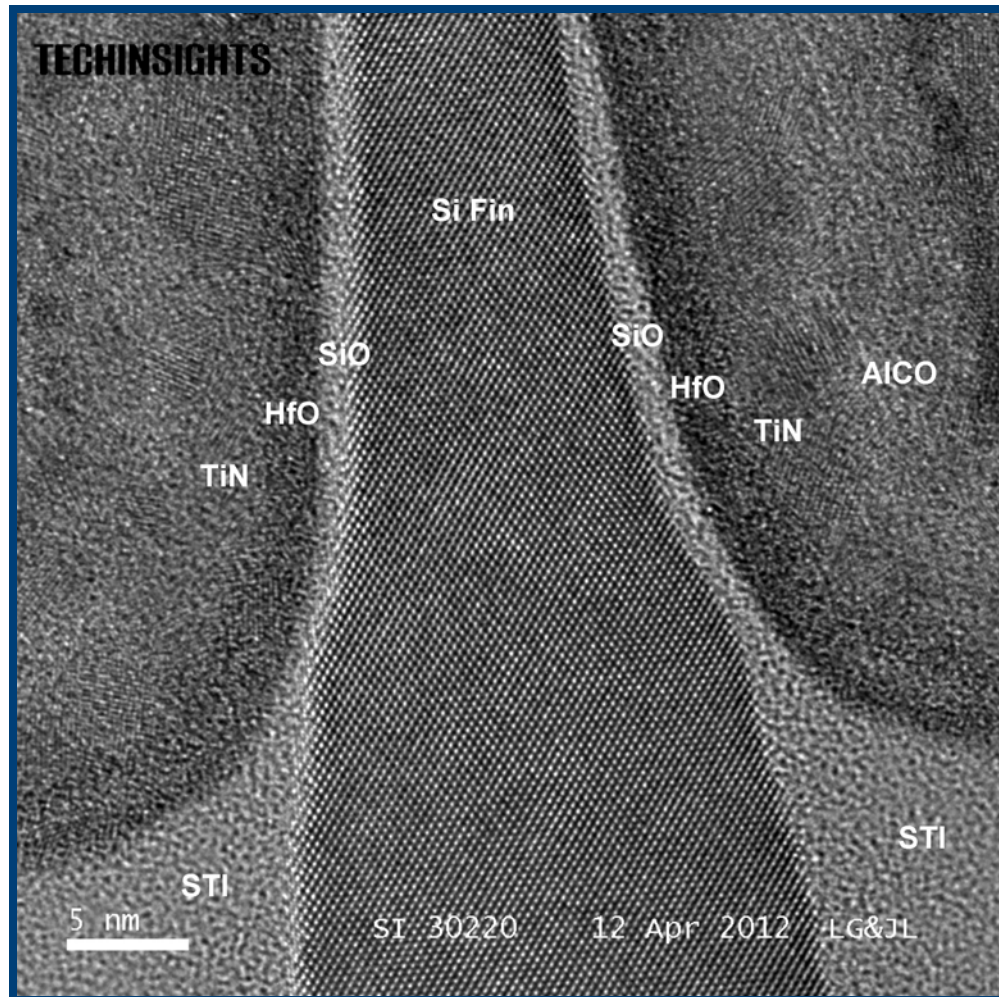


Figure 2.3.2.6: Lower part of the PMOS transistor fin with gate dielectric and metal gate layers, HRTEM image.

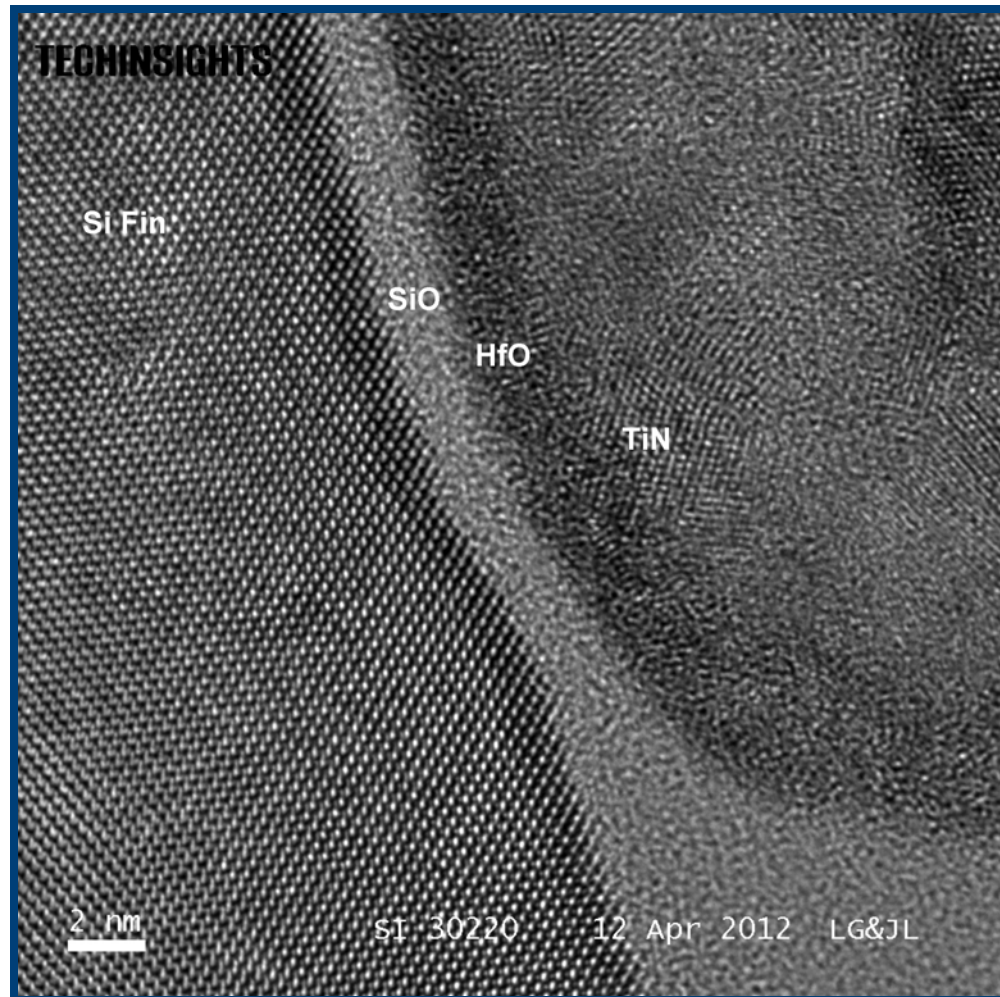


Figure 2.3.2.7: Metal gate and high-k dielectric layers at the bottom of PMOS transistor fin, HRTEM image.



Figure 2.3.2.8: PMOS transistor, TEM cross-section along metal gate with EDS sites annotated.

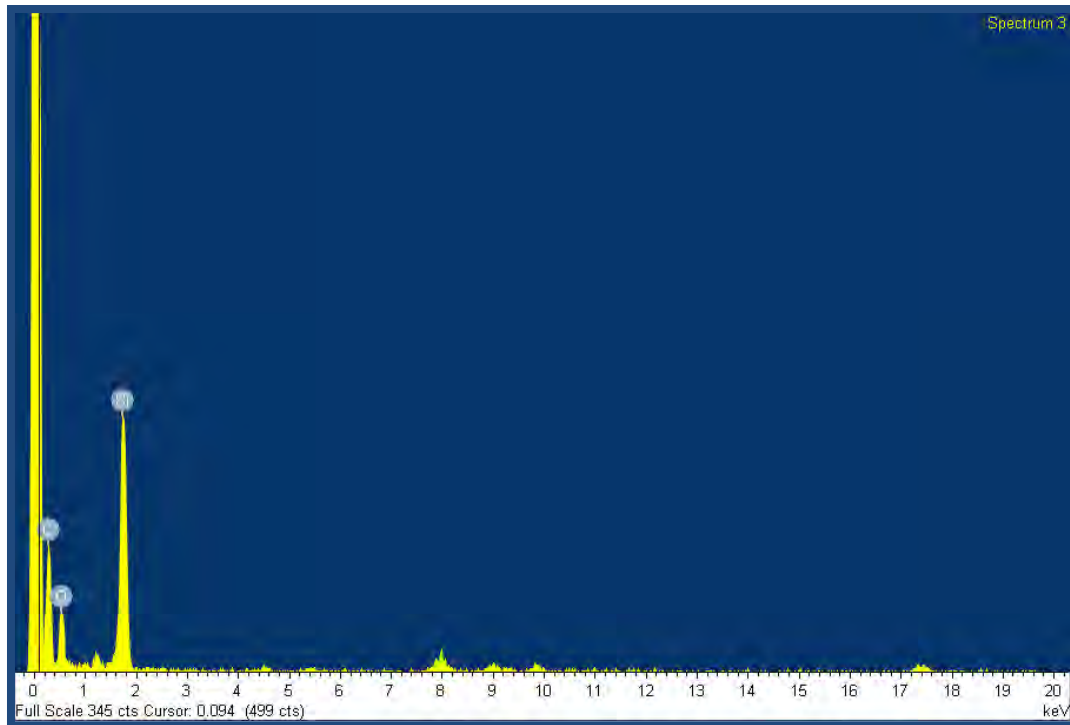


Figure 2.3.2.9: TEM EDS spectrum of SiO bottom interface layer, site 3.

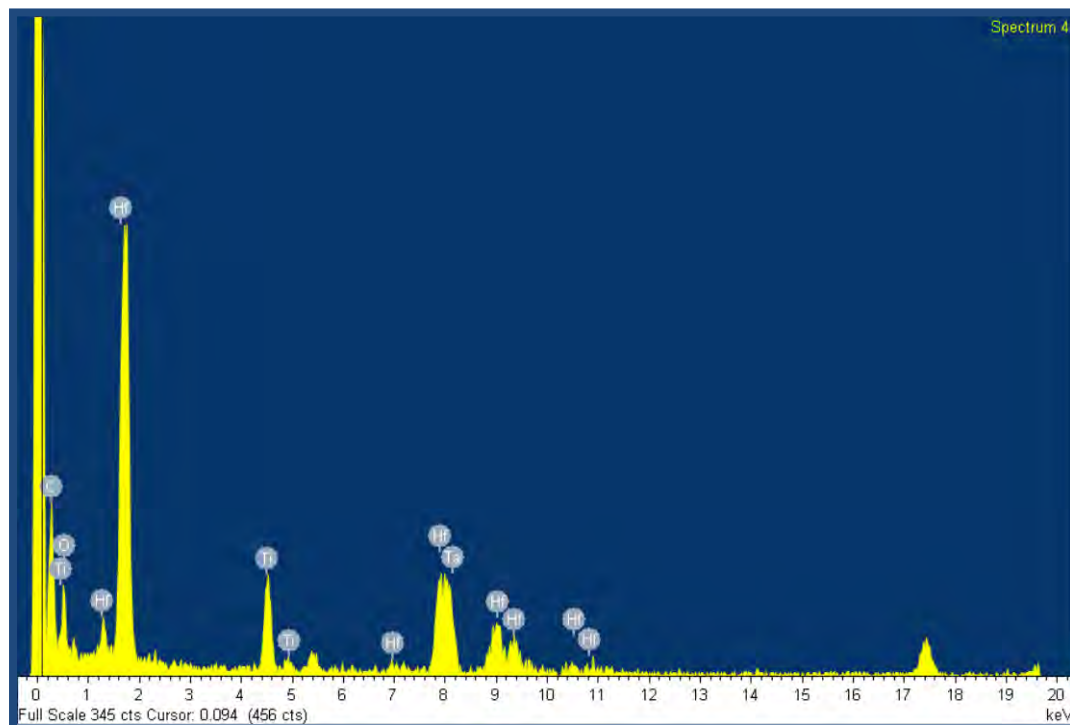


Figure 2.3.2.10: TEM EDS spectrum of HfO high-k gate dielectric, site 4.

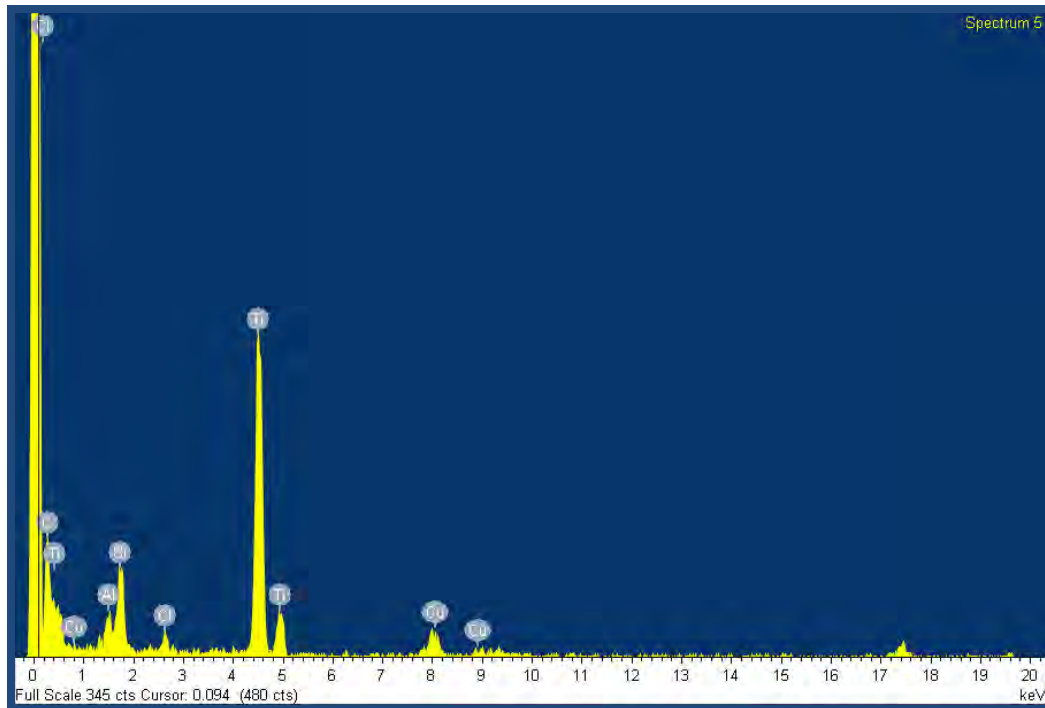


Figure 2.3.2.11: TEM EDS spectrum of metal gate, TiN-AlCO site 5. Copper peaks are artifacts.

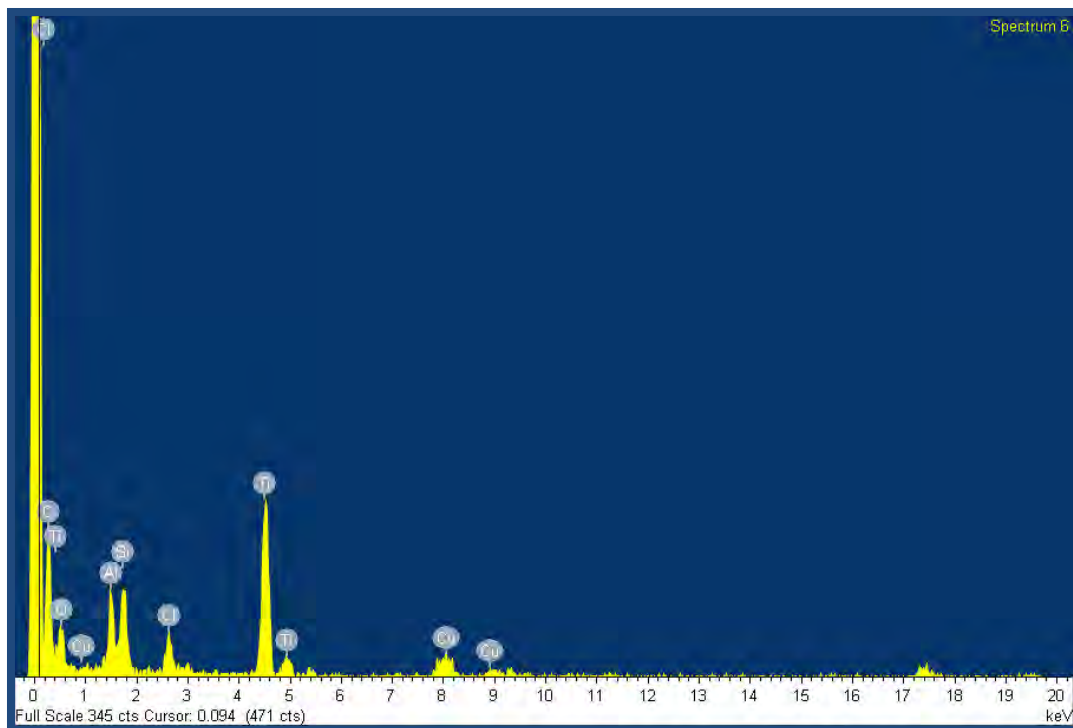


Figure 2.3.2.12: TEM EDS spectrum of metal gate, AlCO-TiAlN site 6.

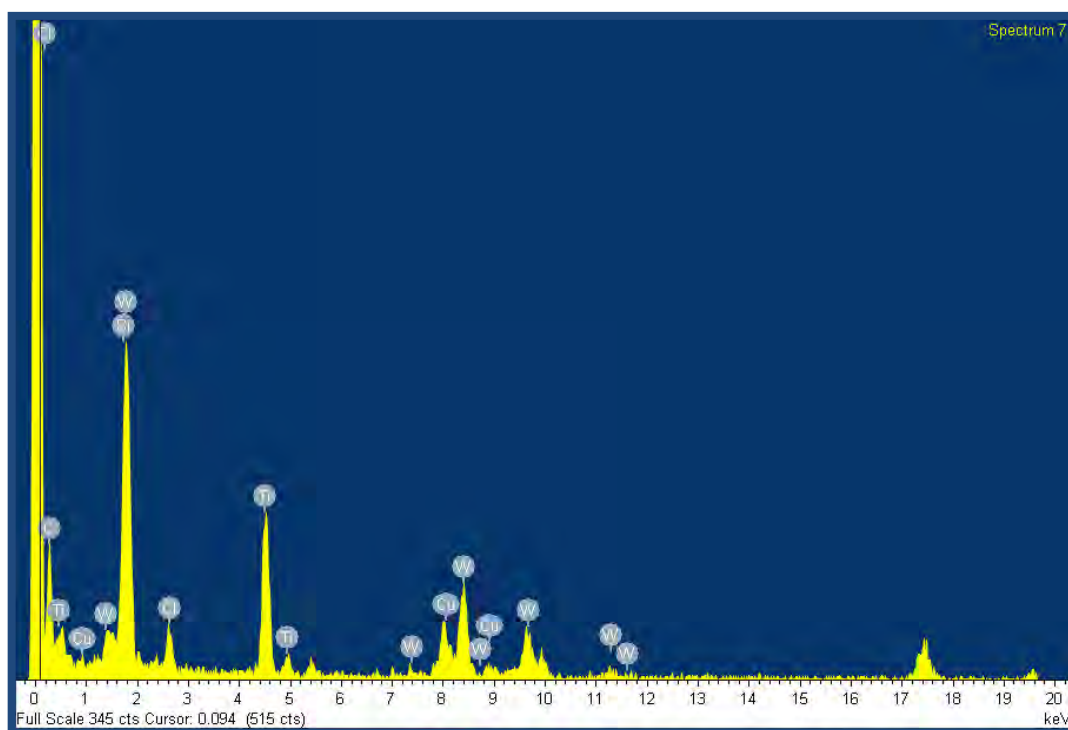


Figure 2.3.2.13: TEM EDS spectrum of metal gate, TiAlN-W site 7. Copper peaks are artifacts.

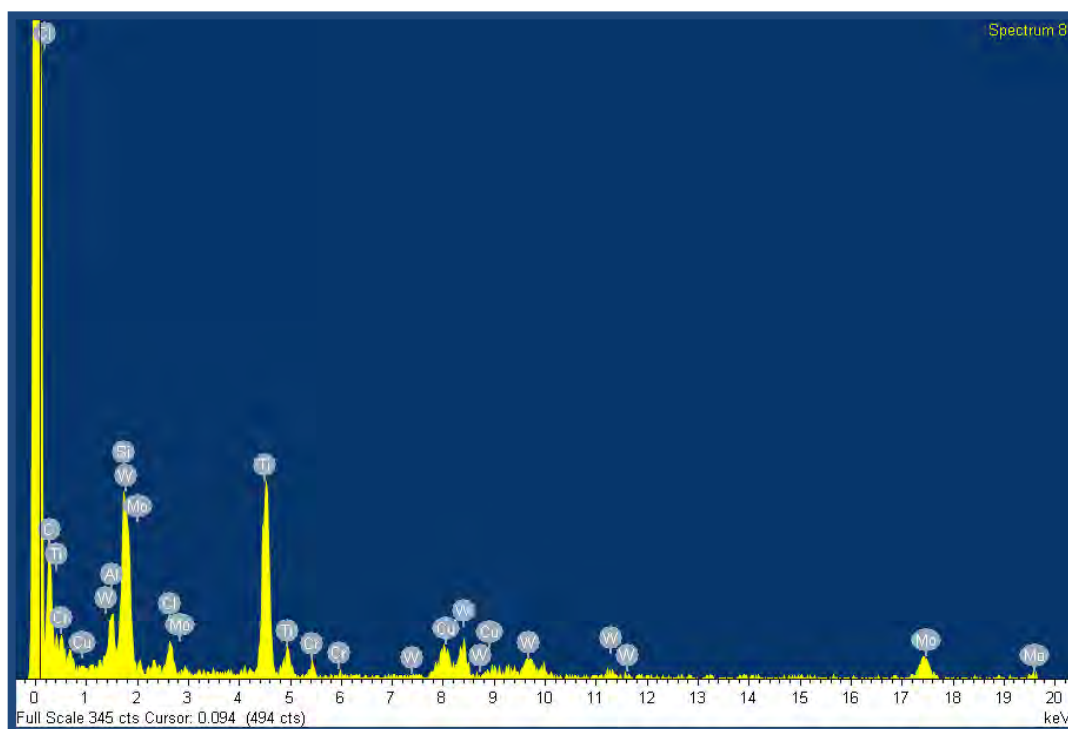


Figure 2.3.2.14: TEM EDS spectrum of metal gate, TiAlN-W site 8.

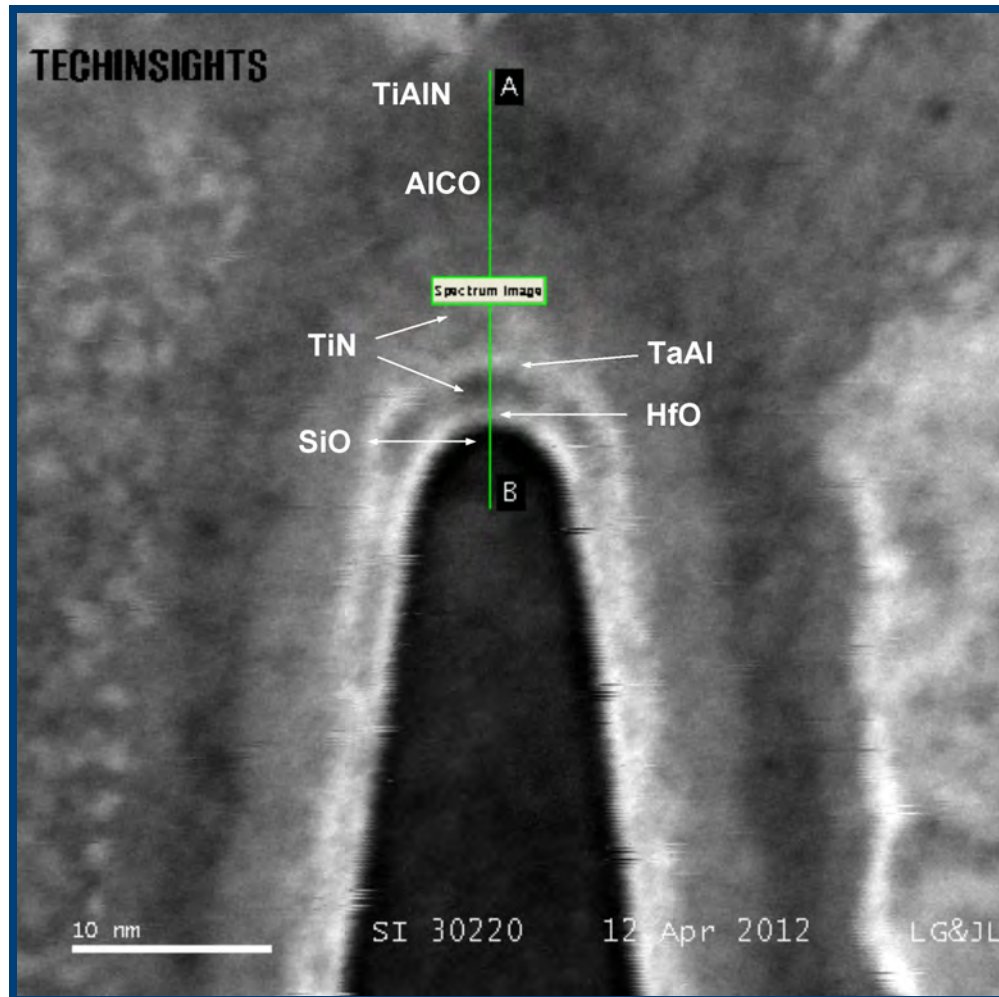


Figure 2.3.2.15: EELS vertical line scan through a PMOS gate, HAADF survey image.

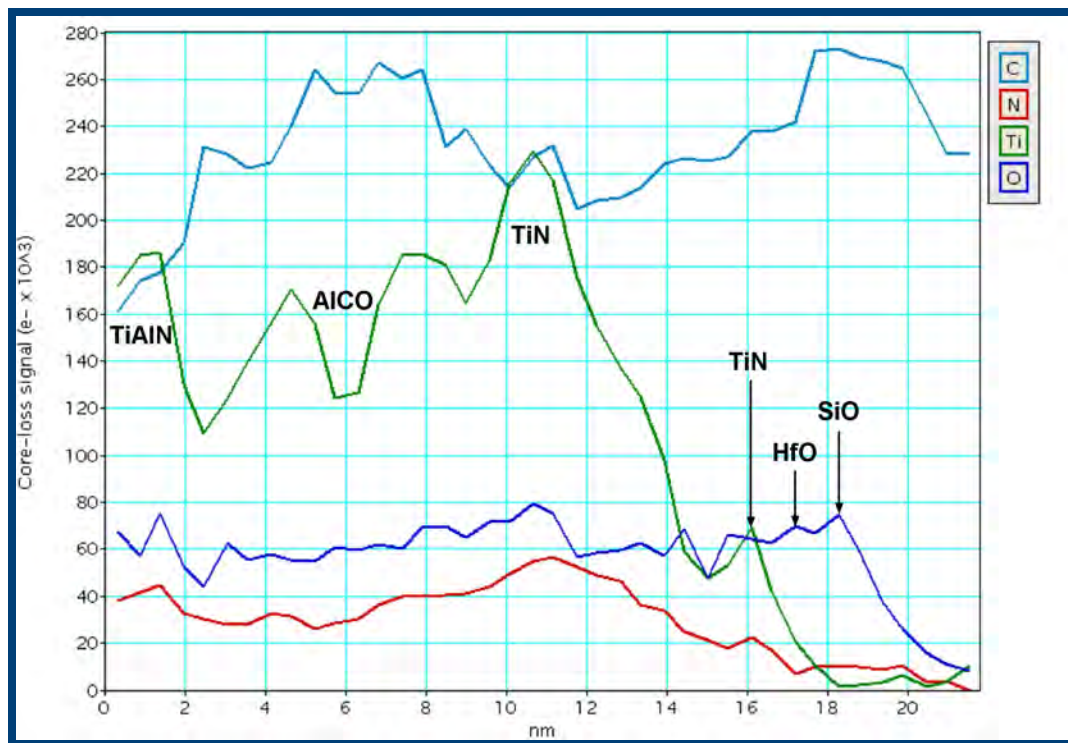


Figure 2.3.2.16: Element profiles of the PMOS gate and gate dielectric, EELS vertical line scan.

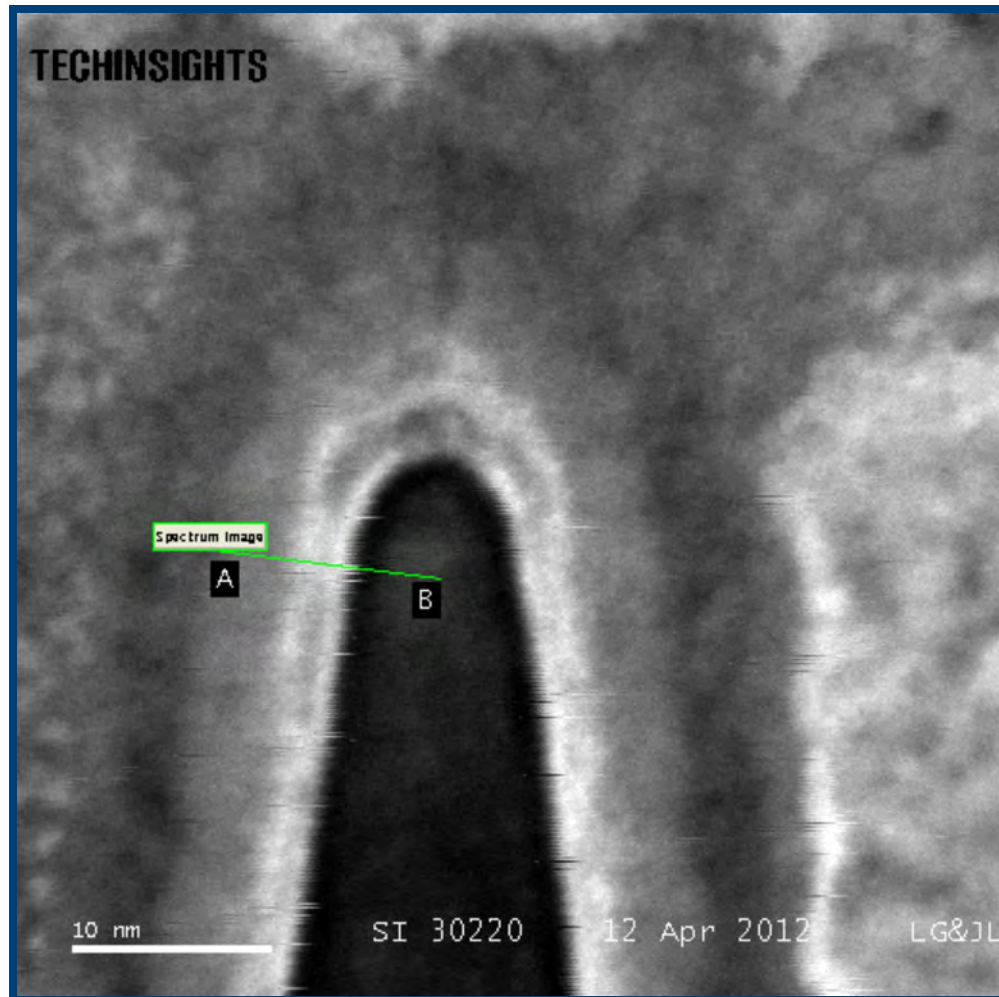


Figure 2.3.2.17: EELS horizontal line scan through a PMOS gate , HAADF survey image.

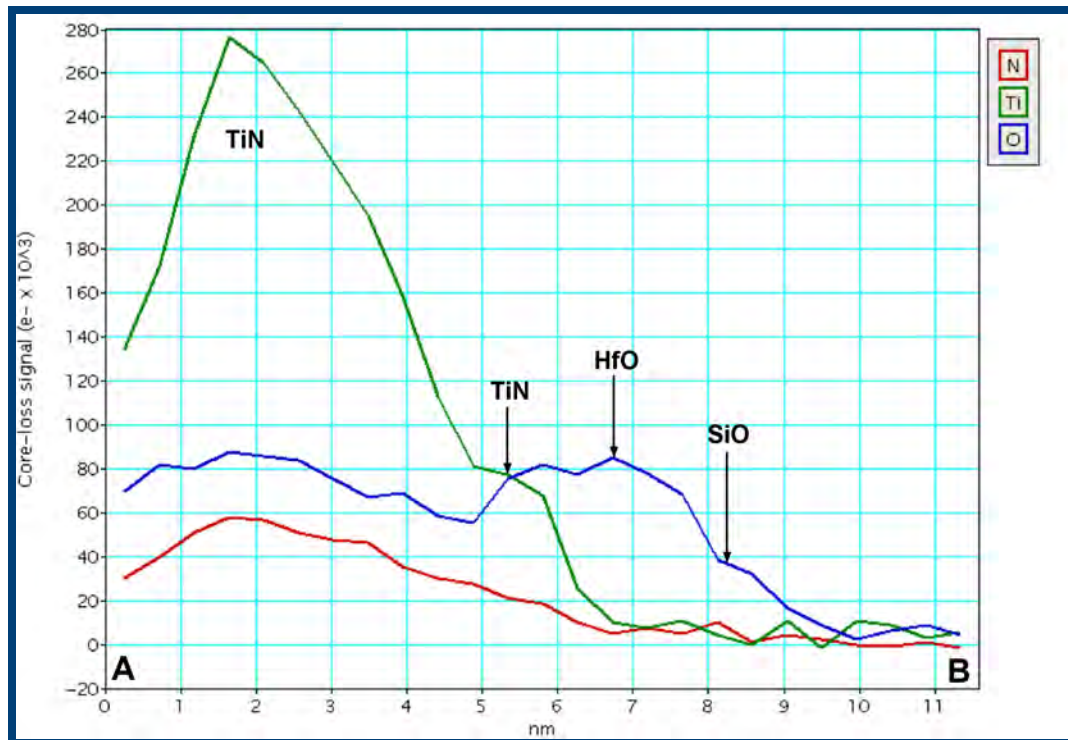


Figure 2.3.2.18: Element profiles of the PMOS gate and gate dielectric, EELS horizontal line scan.