Feature	Dimension	Unit
PMOS gate stack thickness	18	nm
TiN layer above HfO	1	nm
TaAl barrier	1	nm
TiN work function metal	4	nm
AlCO layer	3.5	nm
TiAlN layer	2.5	nm
W gate fill	6	nm

Comments

- Three dimensional FinFET-type transistors (Intel Tri-Gate transistors) with silicon fin and replacement dual work function metal gates and high-k gate dielectric;
- High-k dielectric HfO with bottom interface SiO layer used as a gate dielectric stack;
- Multi-layer replacement metal gate used for PMOS transistor;
  - Thin TiN layer above HfO;
  - Thin TaAl barrier layer;
  - Relatively thick TiN work function metal;
  - Two layers of AlCO and TiAlN;
  - Relatively thick W layer used as a gate filling metal;
  - Thin TiW gate capping layer.

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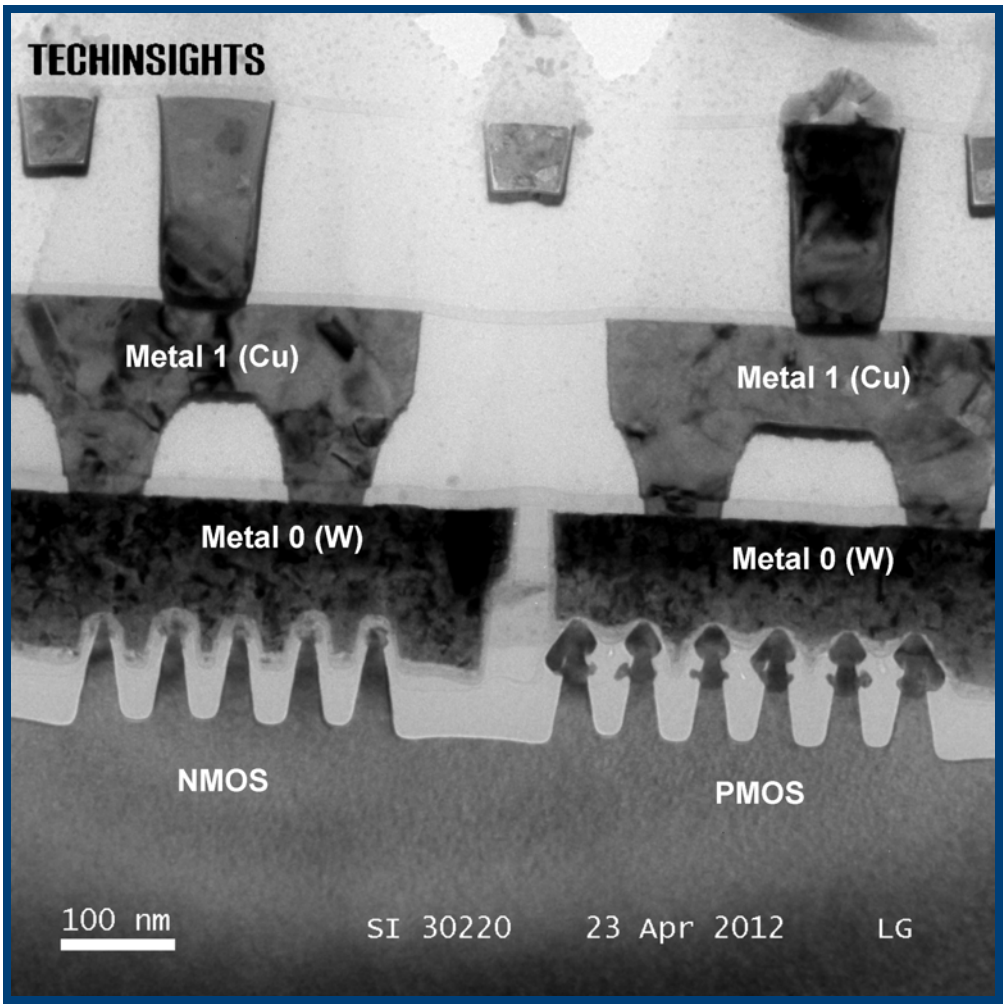


Figure 2.3.2.19: Contacts to source/drain regions of PMOS and NMOS transistors, low magnification TEM section across silicon fins.

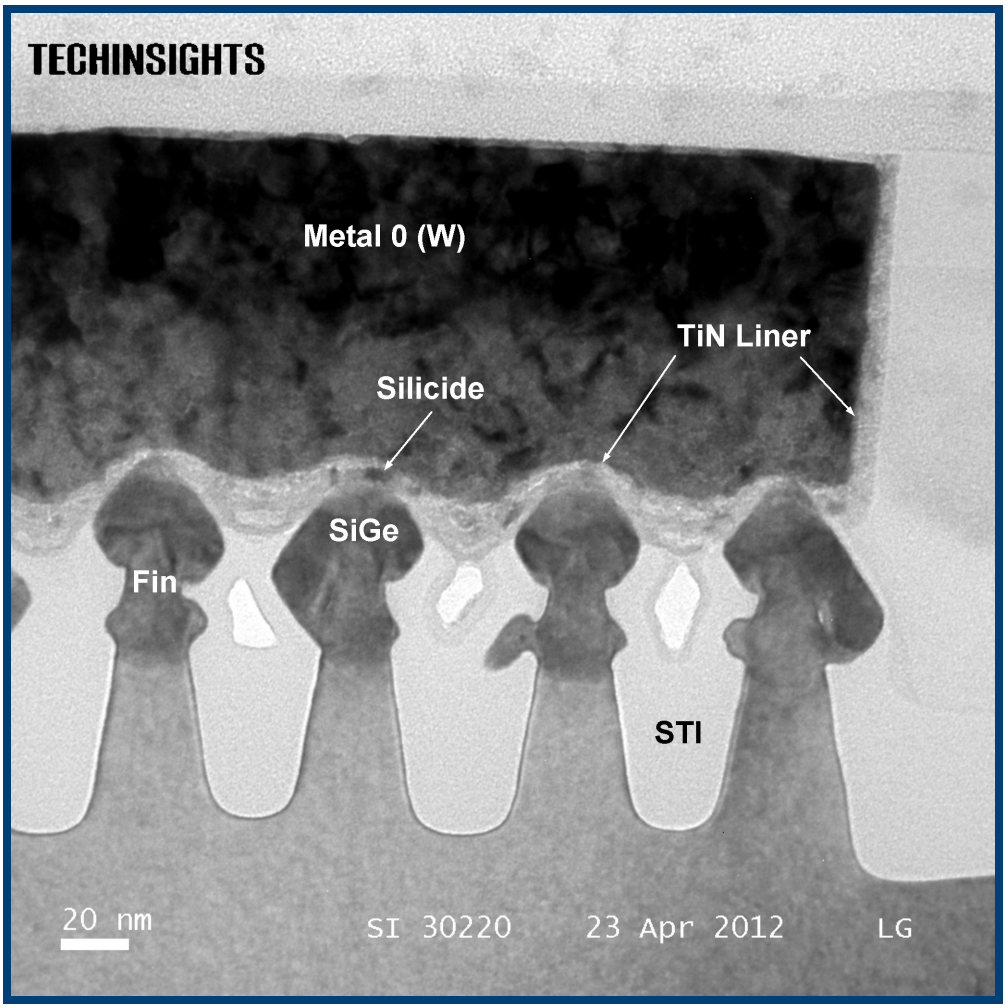


Figure 2.3.2.20: Metal 0 contact to source/drain regions of PMOS transistor, TEM section across fins.

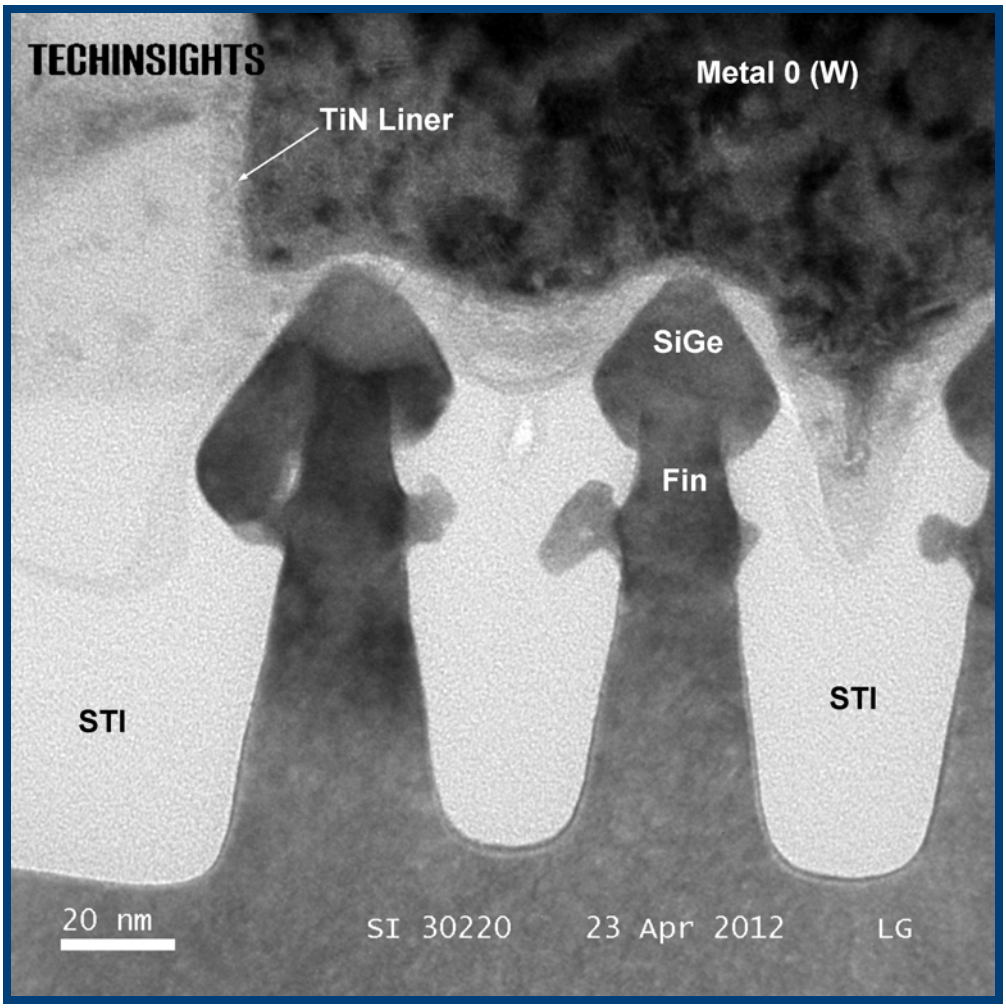


Figure 2.3.2.21: Embedded SiGe in the source/drain of PMOS transistor, high magnification TEM section.

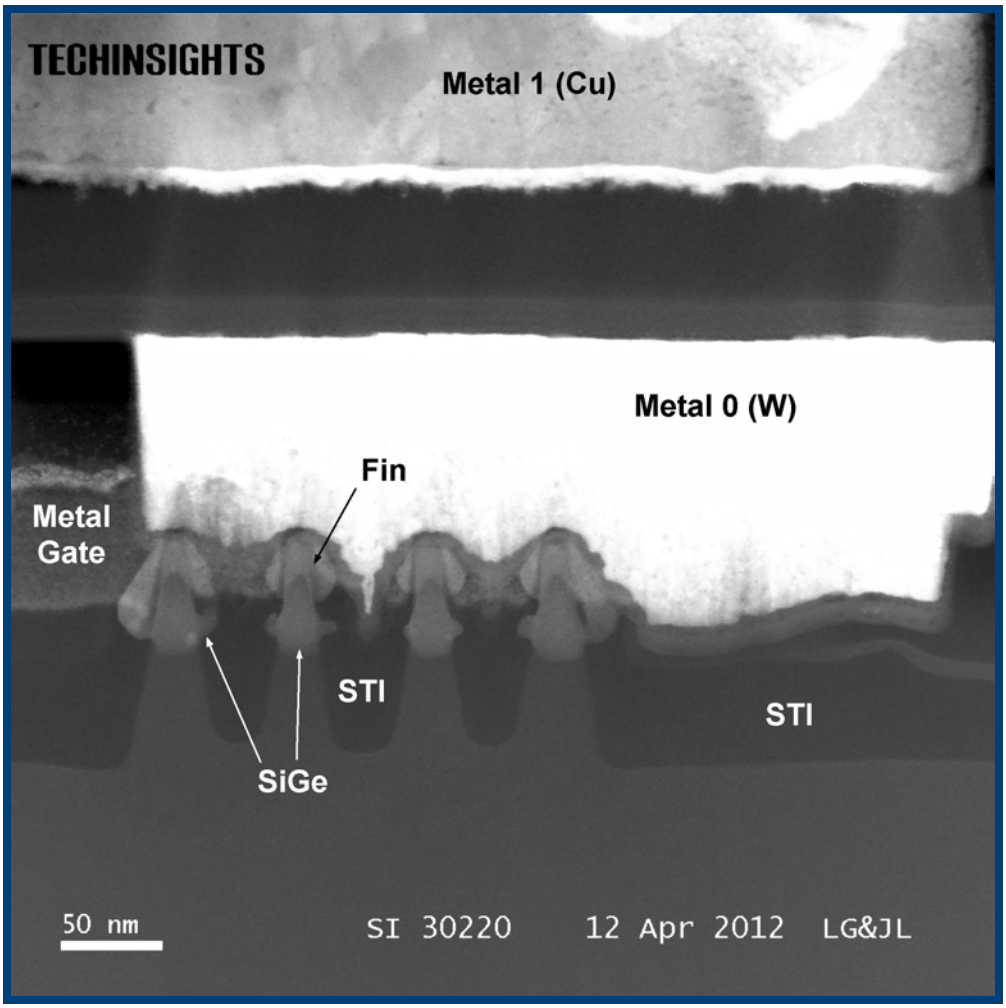


Figure 2.3.2.22: Metal 0 contact to source/drain regions of a PMOS transistor, HAADF section across silicon fins.

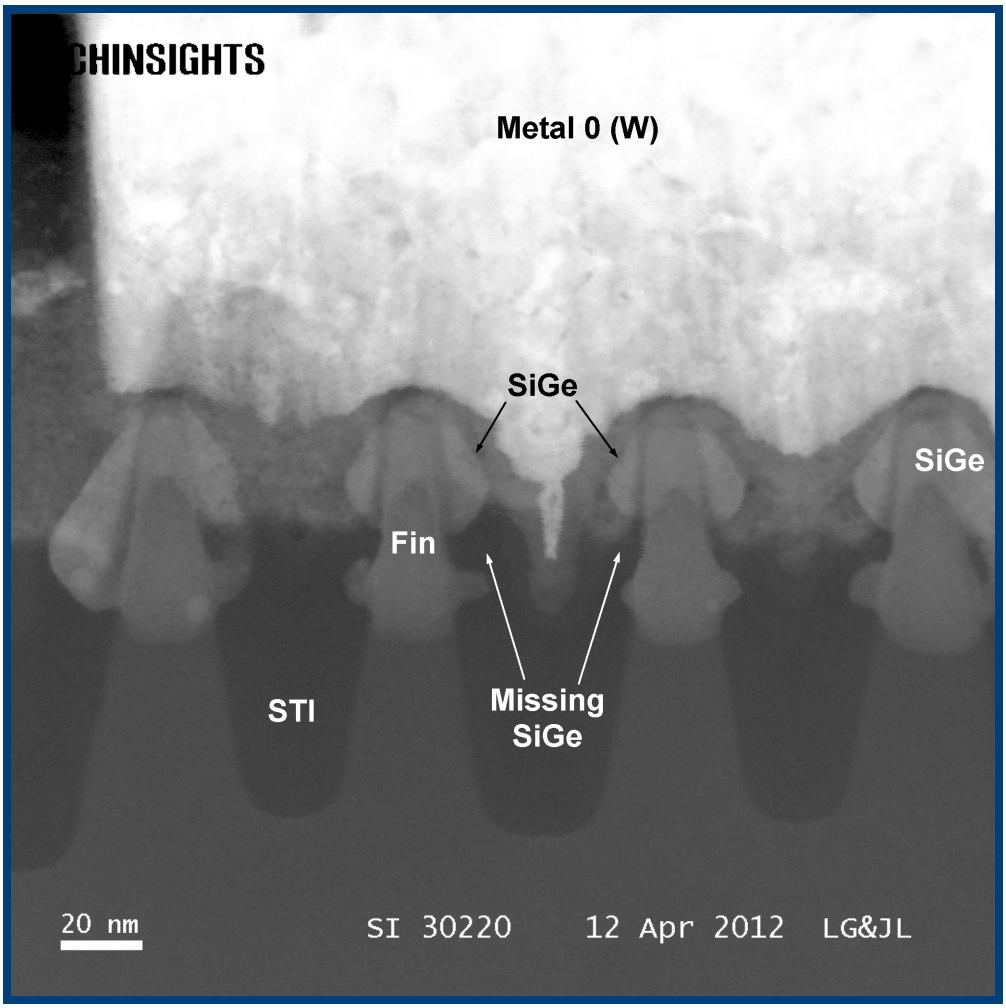


Figure 2.3.2.23: Source/drain regions of the PMOS transistor, higher magnification HAADF cross-section.

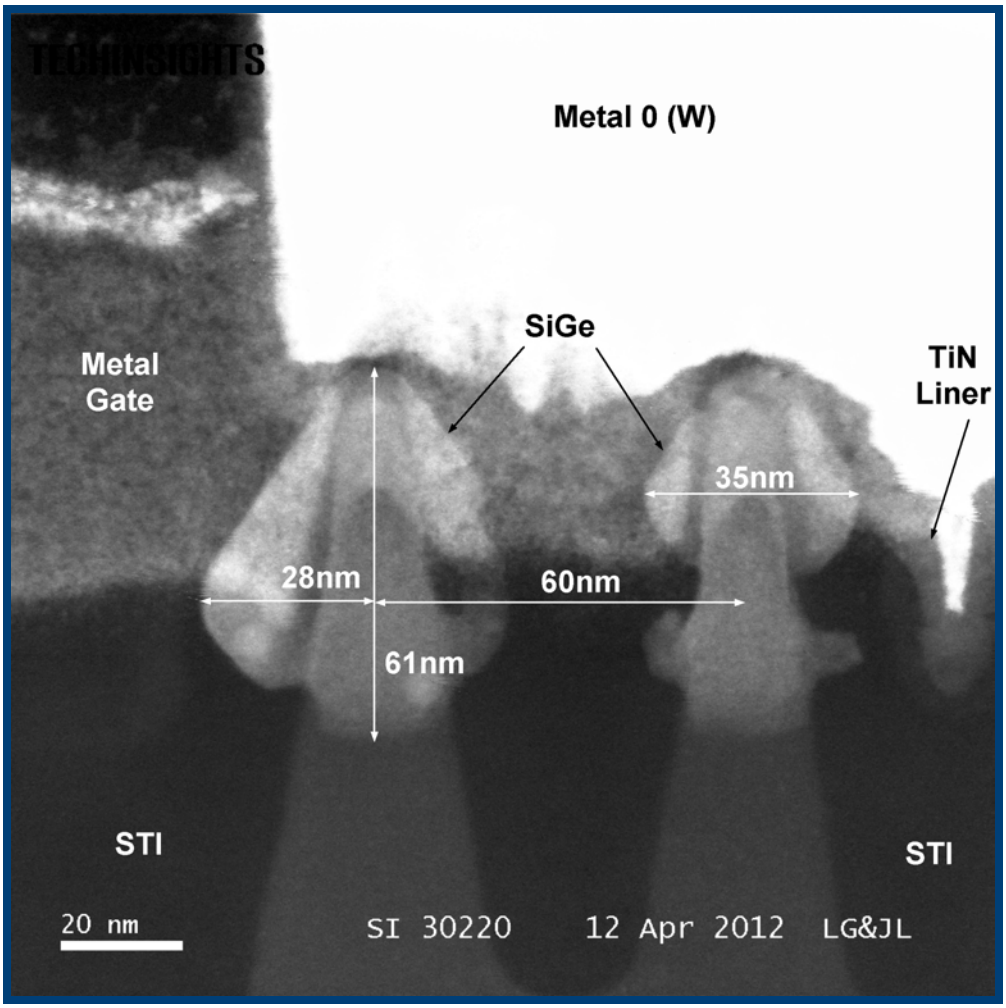


Figure 2.3.2.24: SiGe in the source/drain of PMOS transistor showing width direction, high magnification HAADF cross-section.

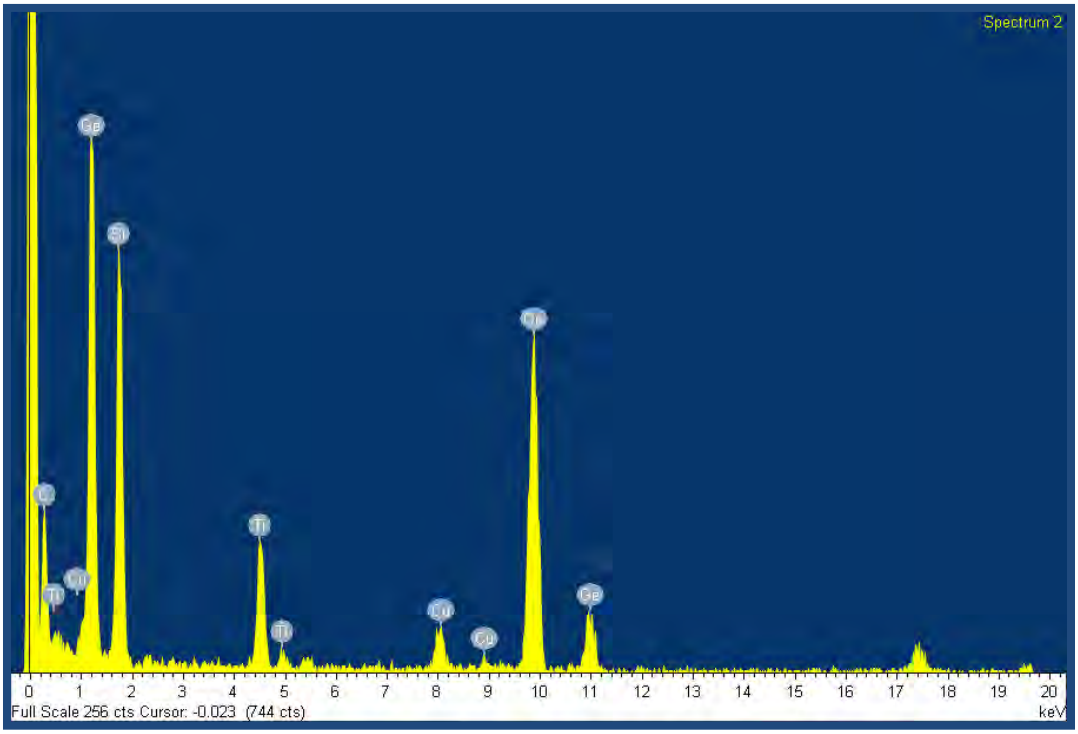


Figure 2.3.2.25: TEM EDS spectrum of a SiGe PMOS source/drain region. Copper peaks are artifacts.

Comments
• Source/drain regions of PMOS transistors have been anisotropically etched to form recess in the PMOS fin; • SiGe selective epitaxial process has been used to fill the source/drain cavity; embedded SiGe (eSiGe) regions standing a few nm above the fin; • eSiGe regions formed to provide compressive stress to PMOS channel (fin) to increase hole mobility and improve PMOS performance; • "Missing" sidewall eSiGe portions have been observed in the inner fins of PMOS transistor.

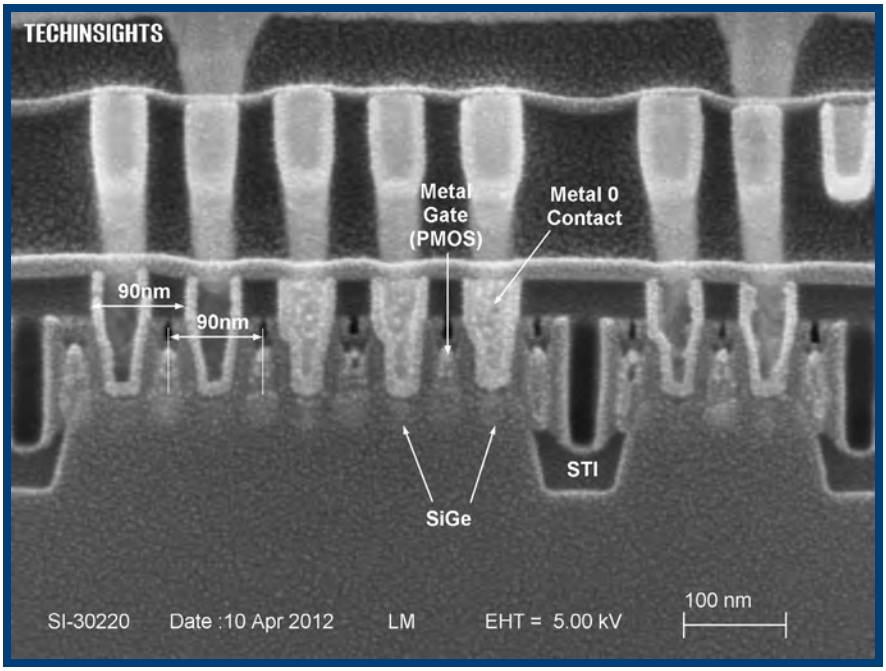


Figure 2.3.2.26: Logic PMOS transistors, SEM cross-section in gate length direction, along silicon fin and transistor channel

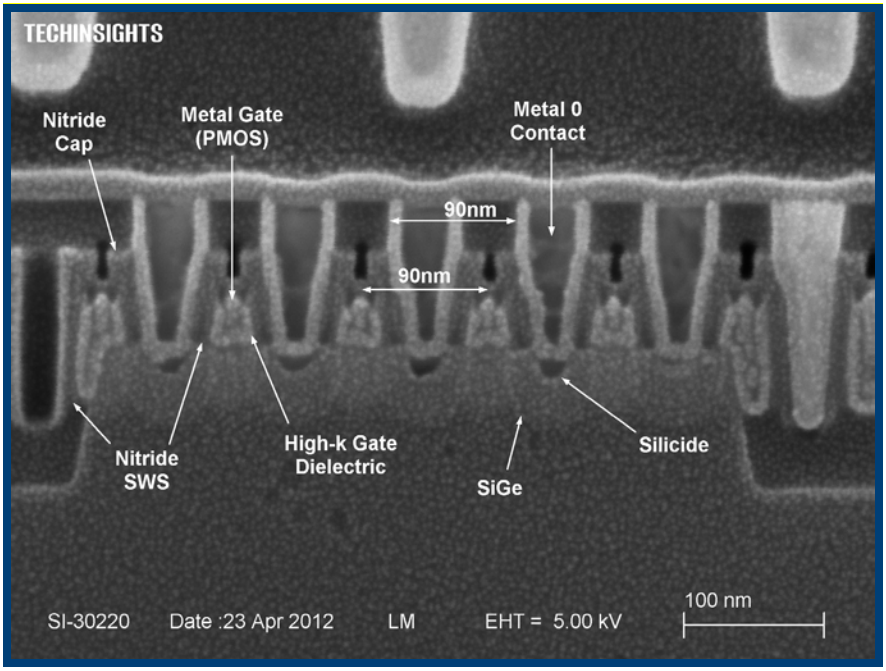


Figure 2.3.2.27: PMOS transistors, SEM cross-section in gate length direction, glass etch.

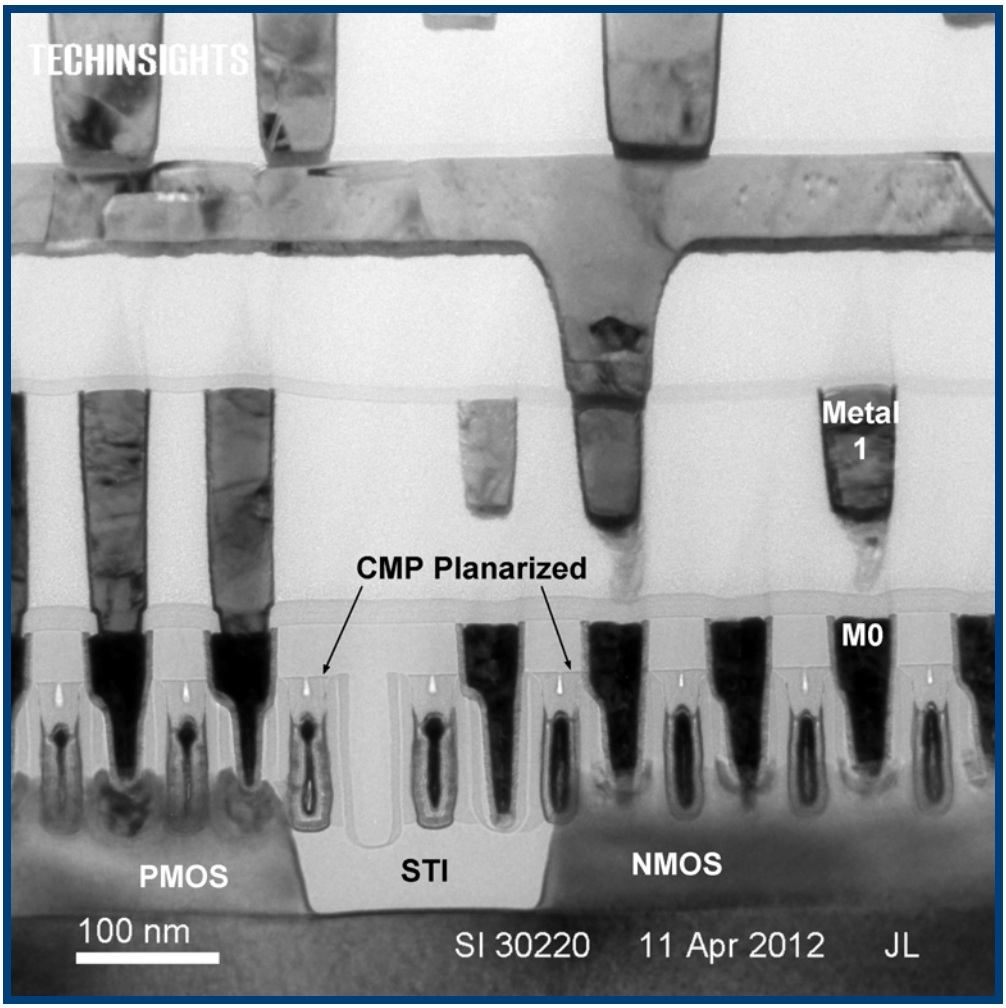


Figure 2.3.2.28: Logic PMOS and NMOS transistors cross-sectioned along silicon fins and transistor channels, low magnification TEM image.

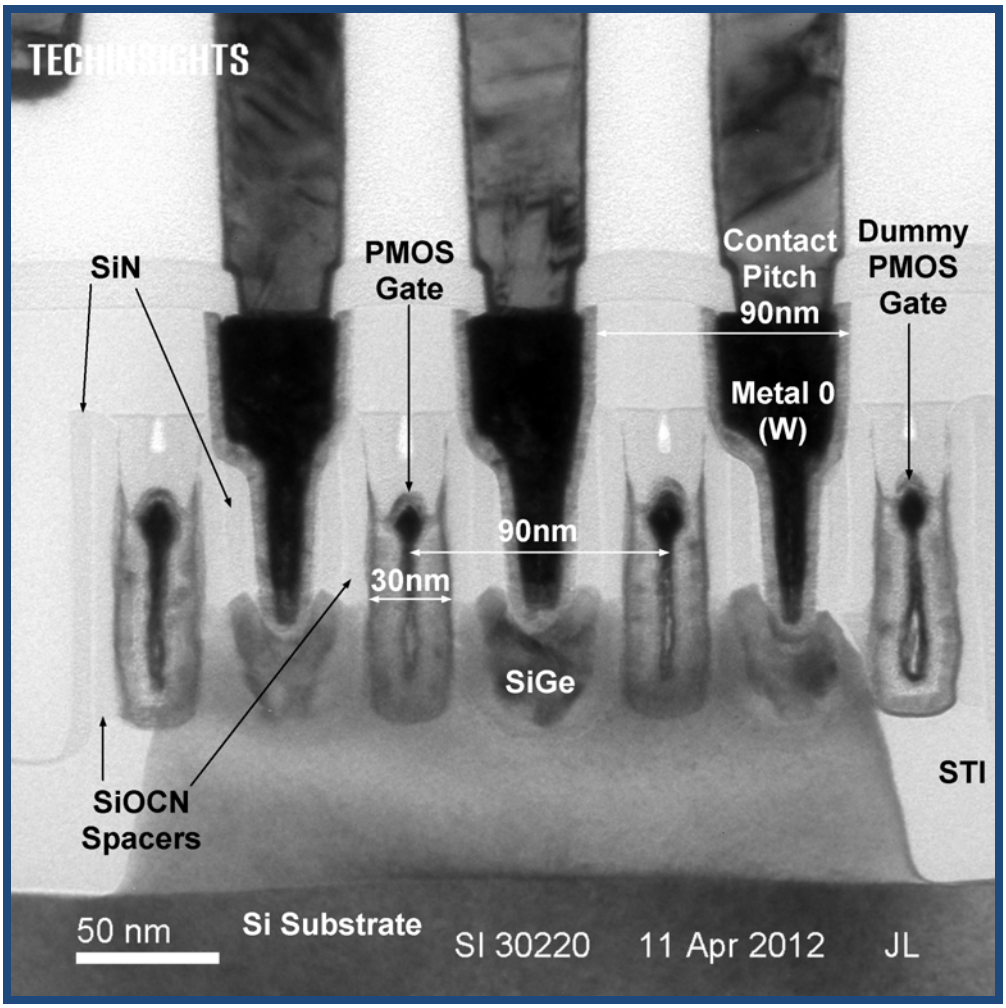


Figure 2.3.2.29: Minimum contacted gate pitch PMOS transistors, TEM cross-section along transistor channel and across metal gates.

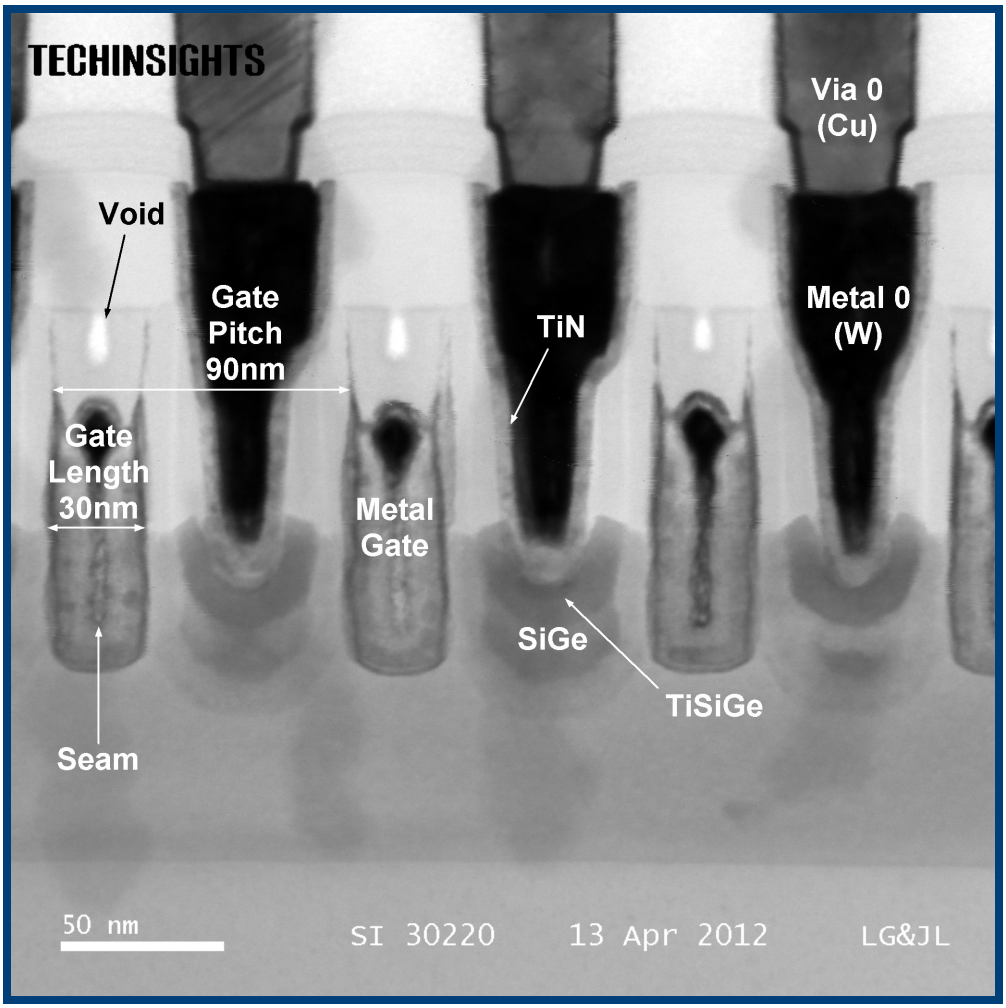


Figure 2.3.2.30: Minimum pitch/gate length PMOS transistors with contacts to SiGe source/drain regions, TEM cross-section.

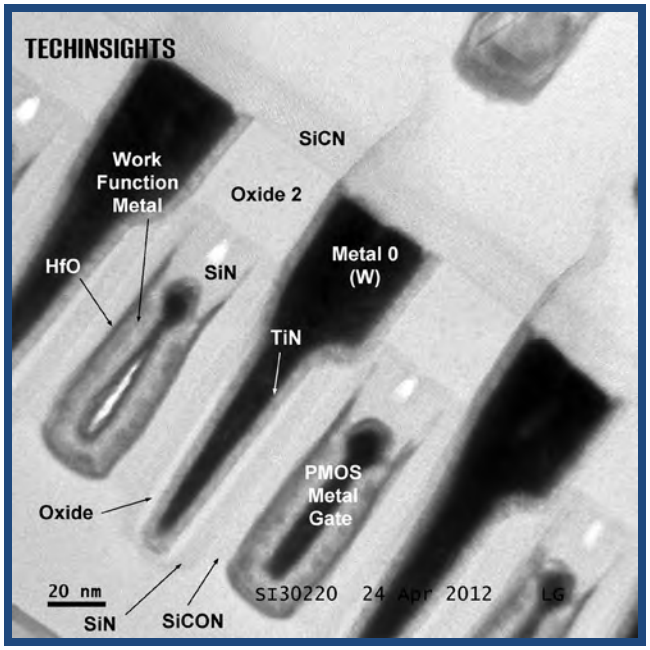


Figure 2.3.2.31: Dummy PMOS metal gate, unfiltered EFTEM image.

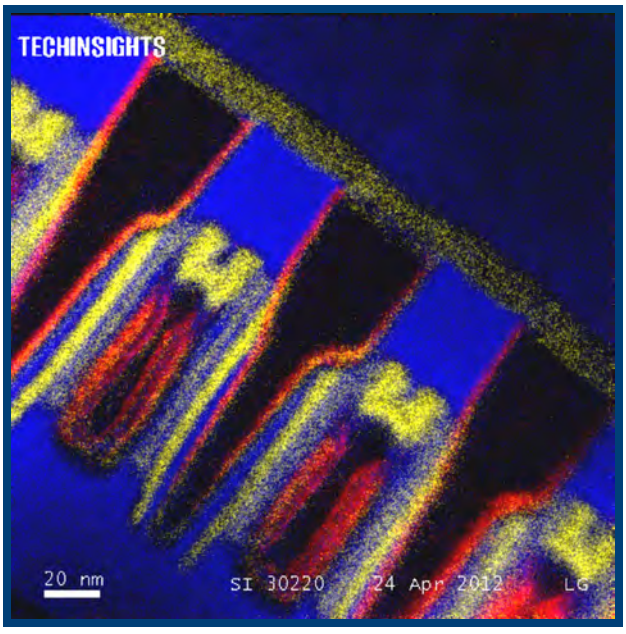


Figure 2.3.2.32: Dummy PMOS metal gate, false color EFTEM image showing Ti (red), N (yellow) and O (blue)

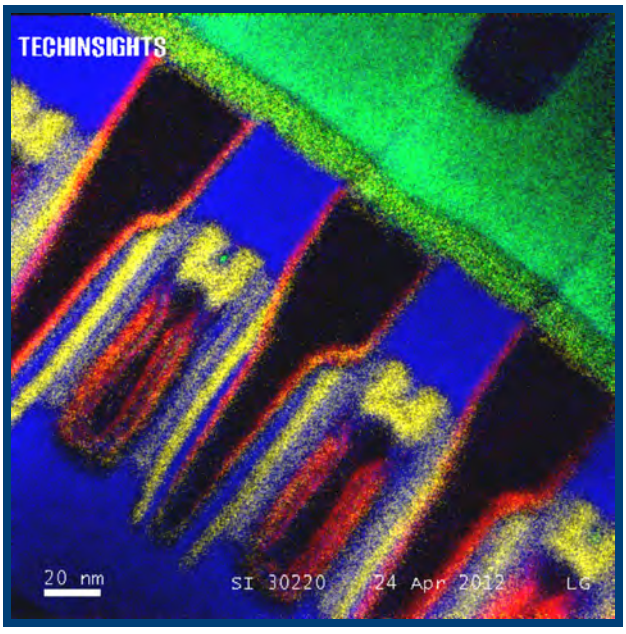


Figure 2.3.2.33: Dummy PMOS metal gate, false color EFTEM image showing Ti (red), N (yellow), O (blue), and C (green).

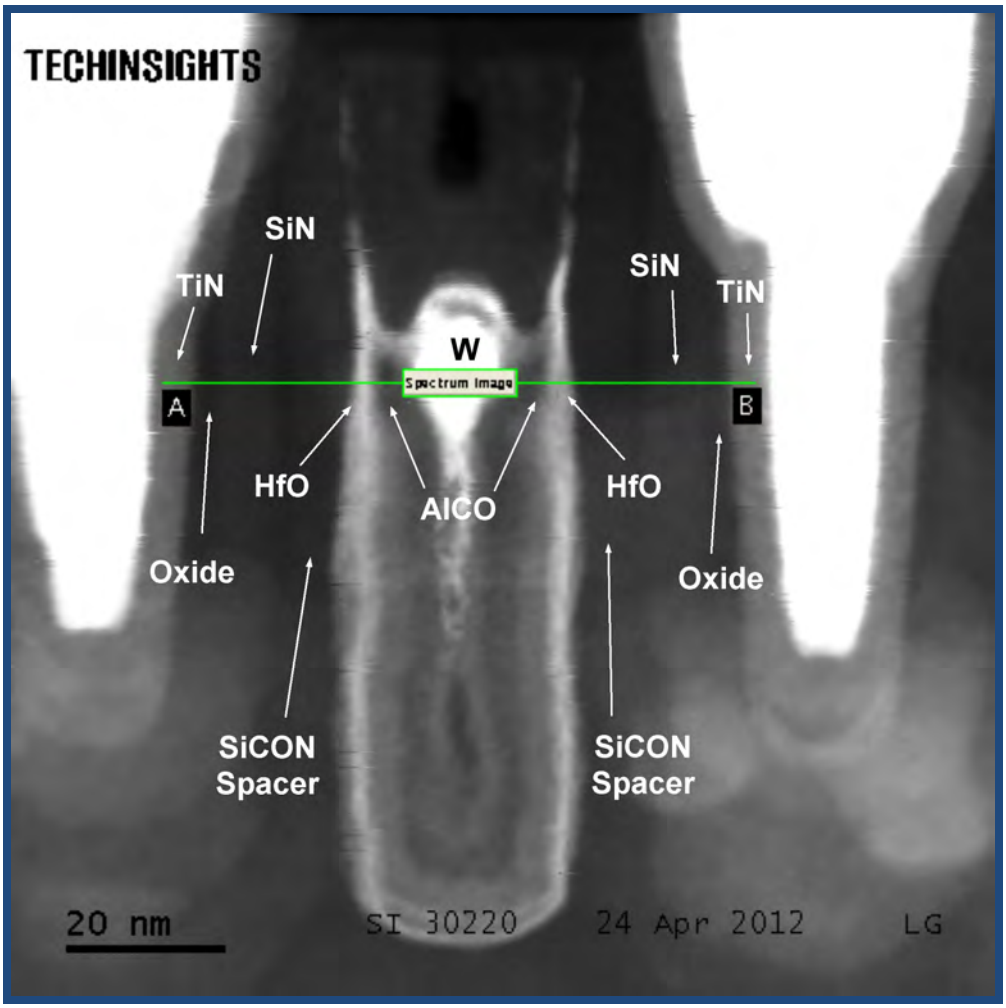


Figure 2.3.2.36: EELS line scan through a PMOS gate between source/drain contacts, HAADF survey image.

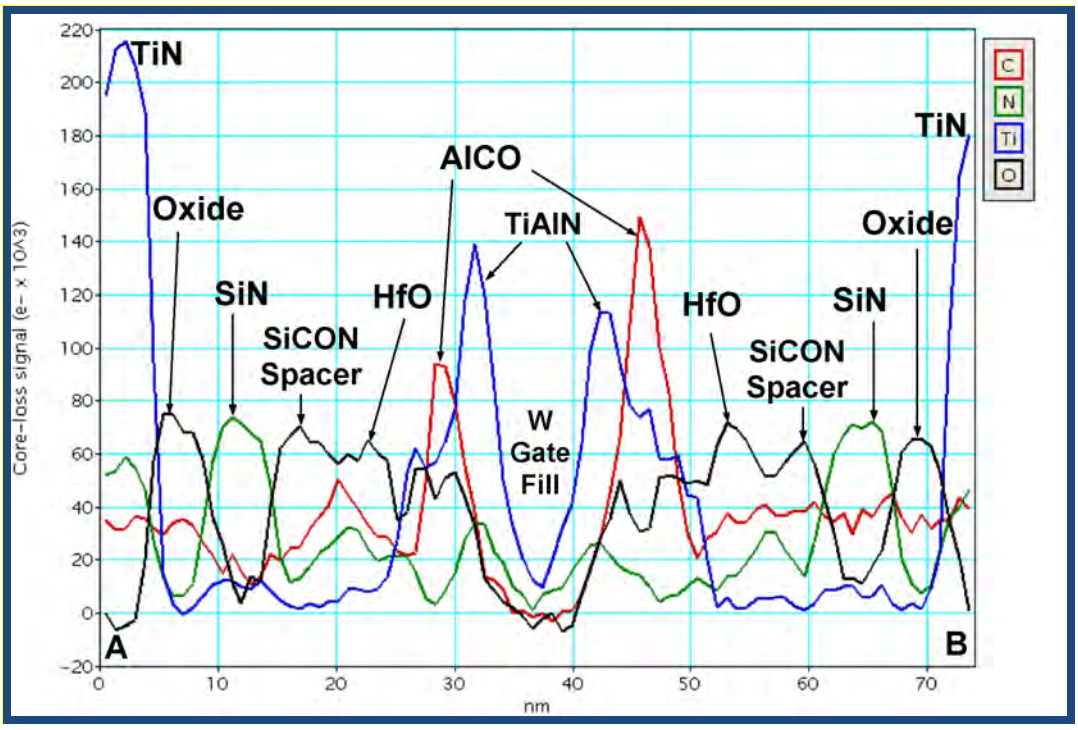


Figure 2.3.2.37: Element profiles of the PMOS gate and dielectric layers, EELS line scan between source/drain contacts.

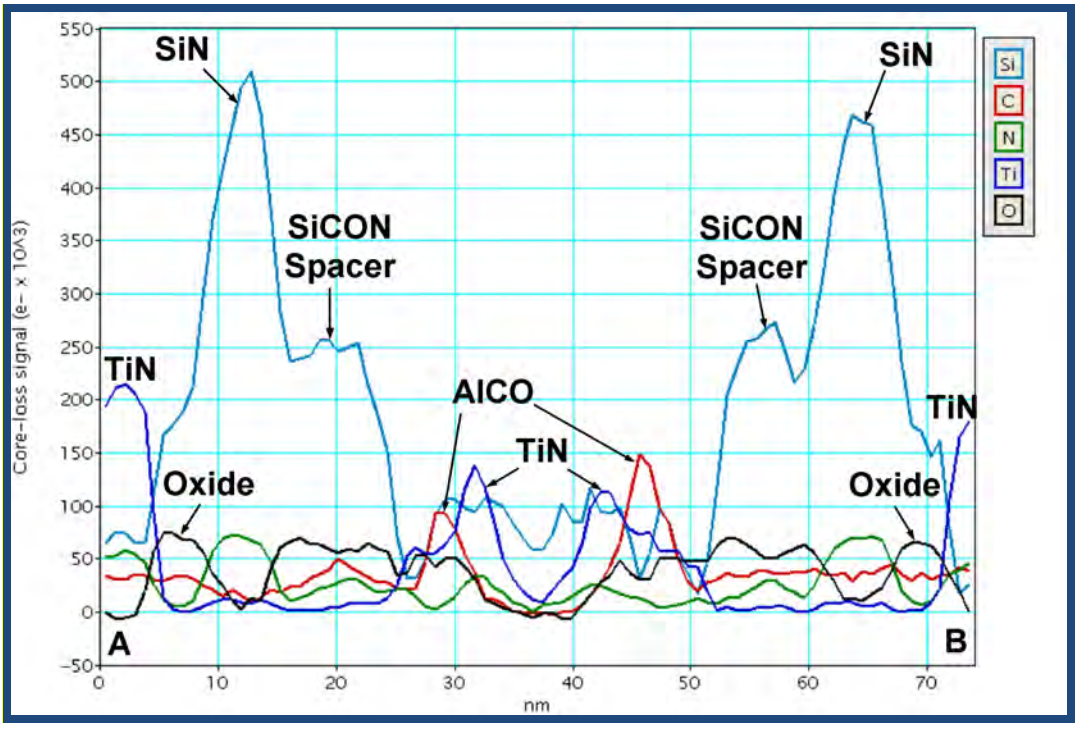


Figure 2.3.2.38: Element profiles (including Si) of the PMOS gate and dielectric layers, EELS line scan between source/drain contacts.

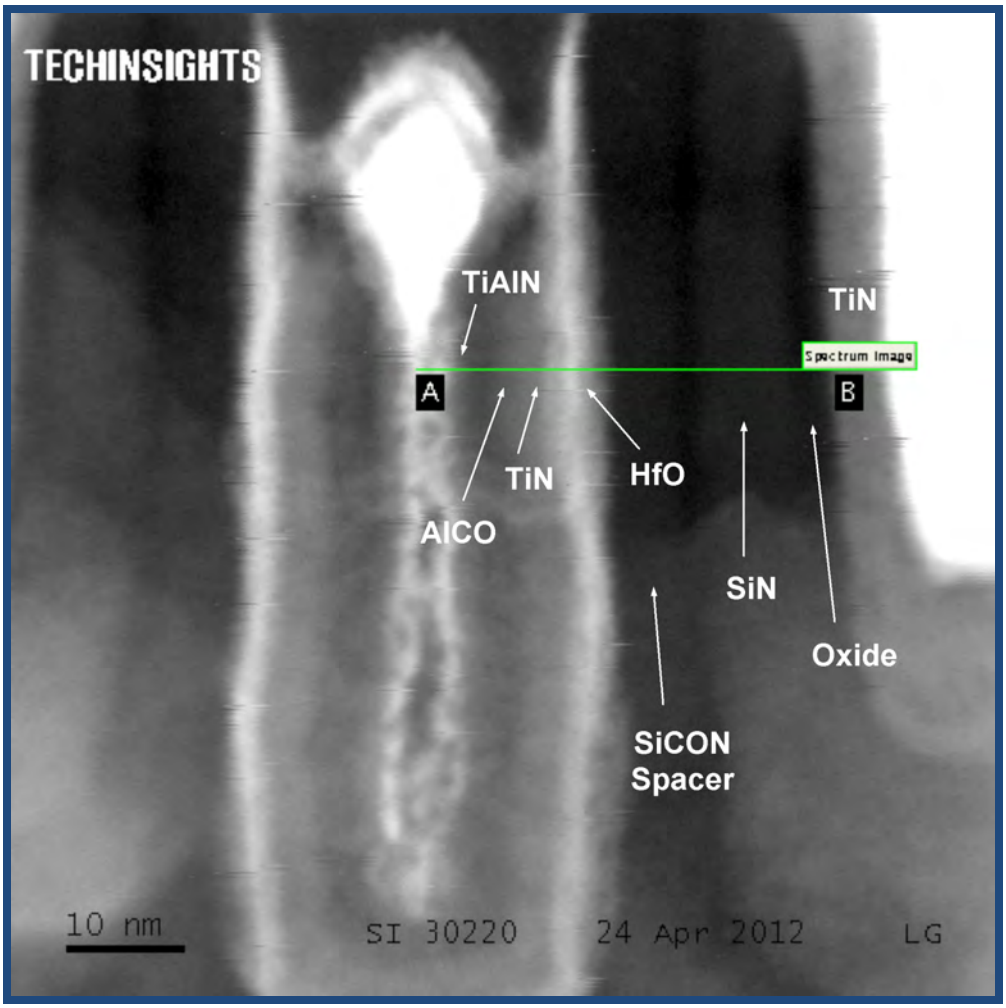


Figure 2.3.2.39: EELS line scan through the PMOS gate right side, HAADF survey image.

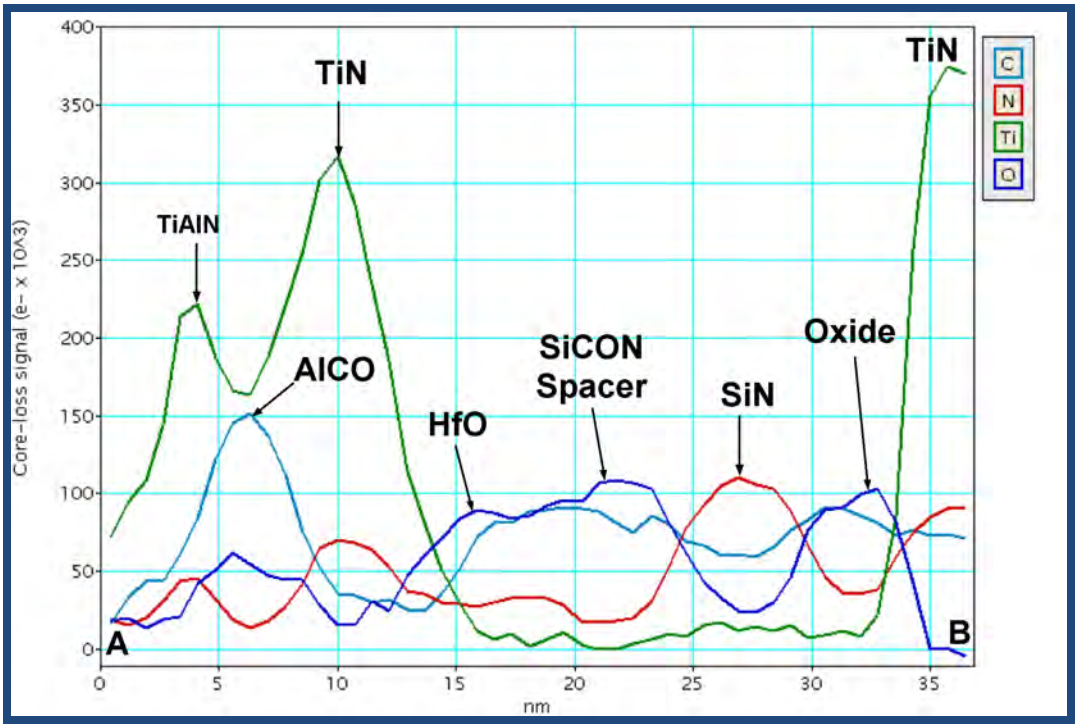


Figure 2.3.2.40: Element profiles of the PMOS gate and dielectric layers, EELS line scan.

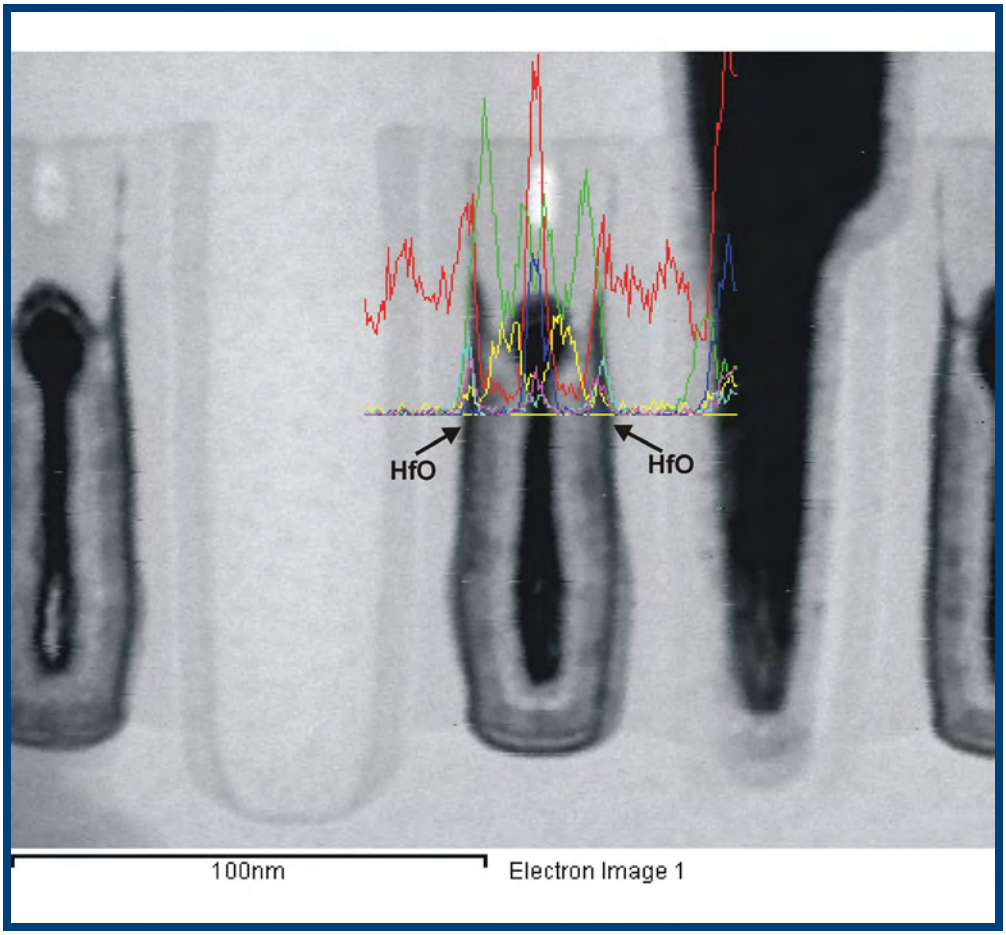


Figure 2.3.2.41: TEM EDS line scan through a PMOS metal gate with element profiles overlaid.

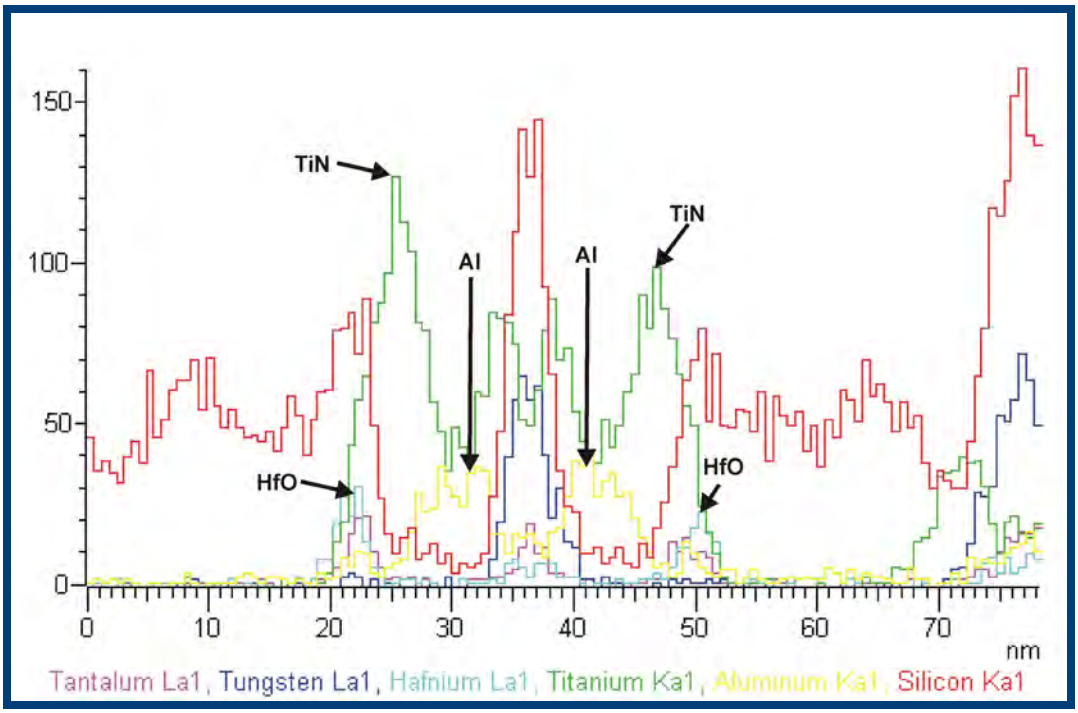


Figure 2.3.2.42: Element profiles of PMOS metal gate, TEM EDS line scan.

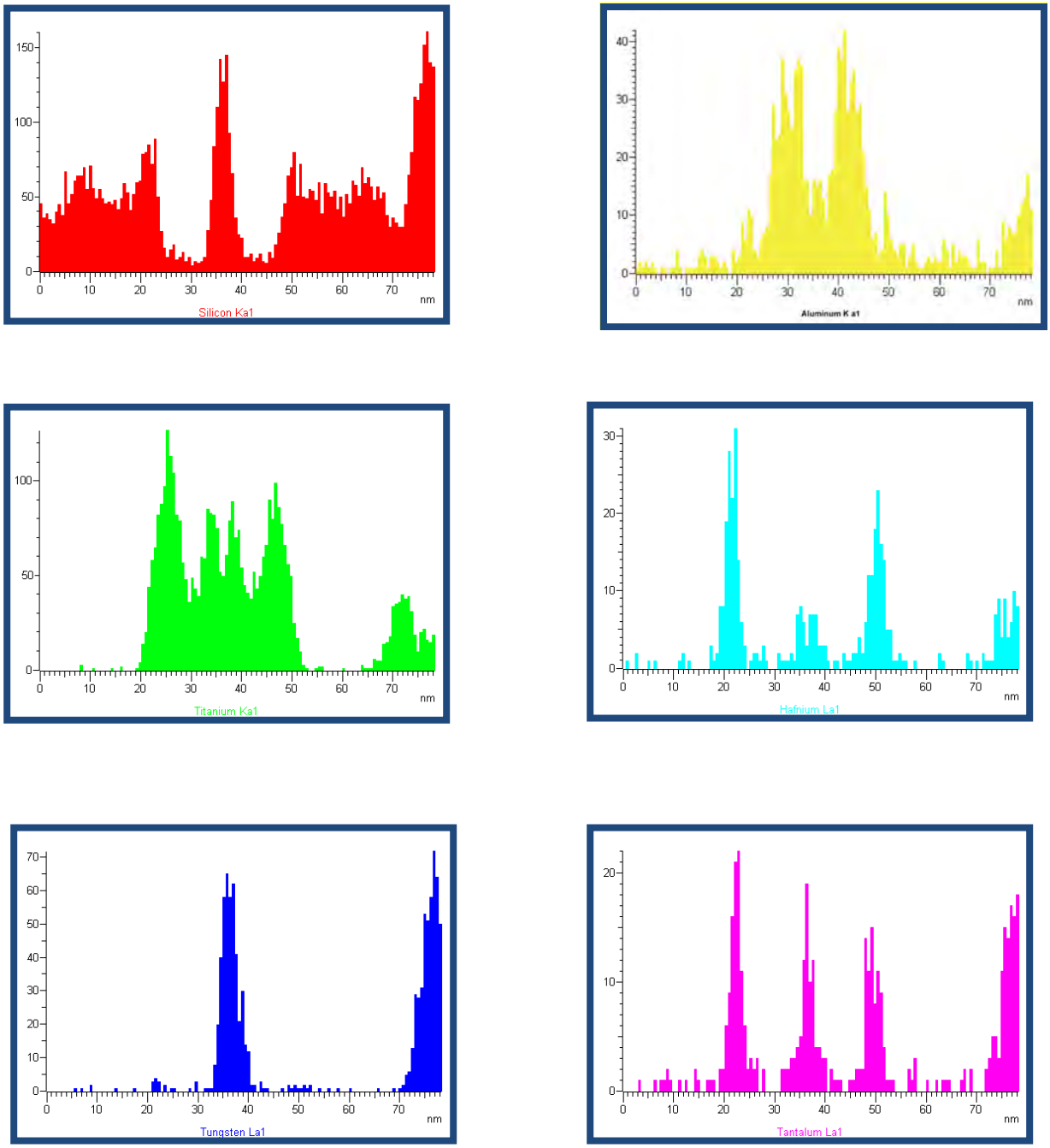


Figure 2.3.2.43: Separate element profiles of the PMOS metal gate, TEM EDS line scan.



Figure 2.3.2.44: PMOS transistor with contacts to SiGe source/drain regions and TEM EDS sites annotated.

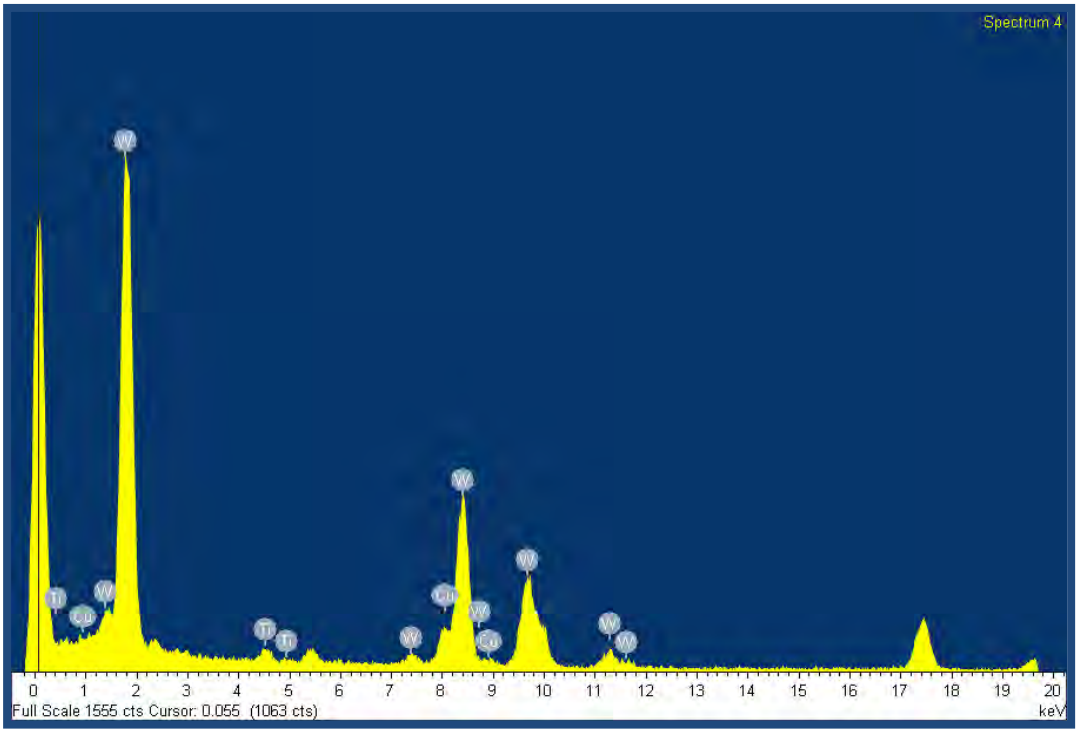


Figure 2.3.2.45: TEM EDS spectrum of PMOS metal gate (W), site 4.

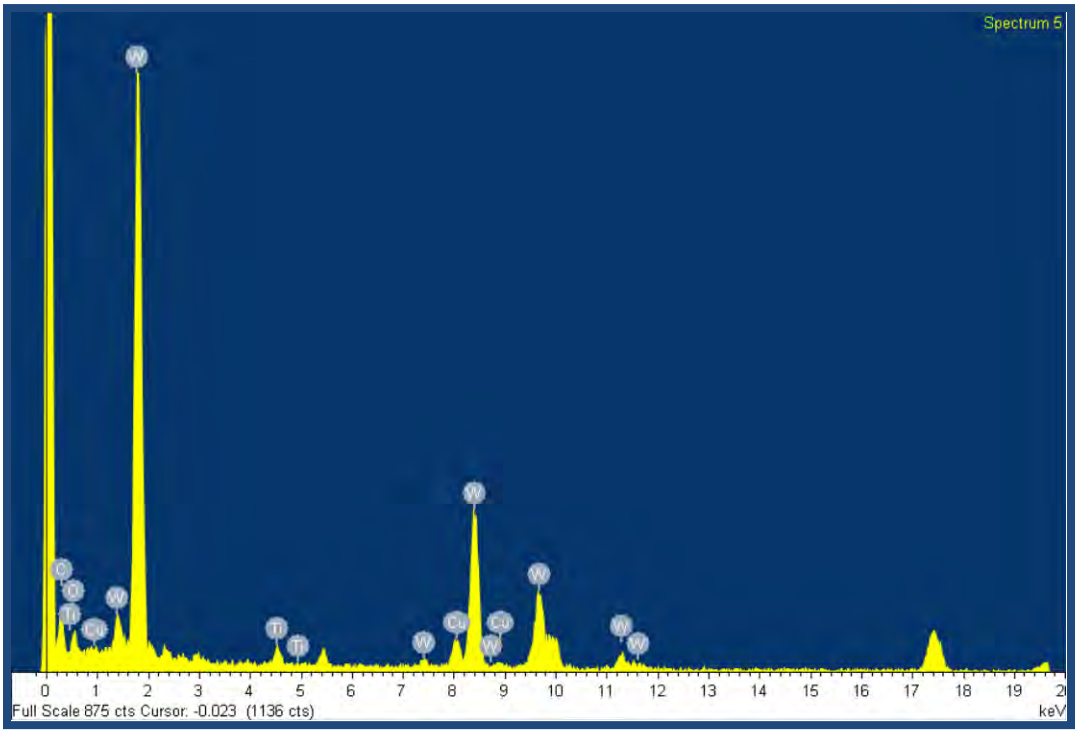


Figure 2.3.2.46: TEM EDS spectrum of TiW cap layer, site 5.

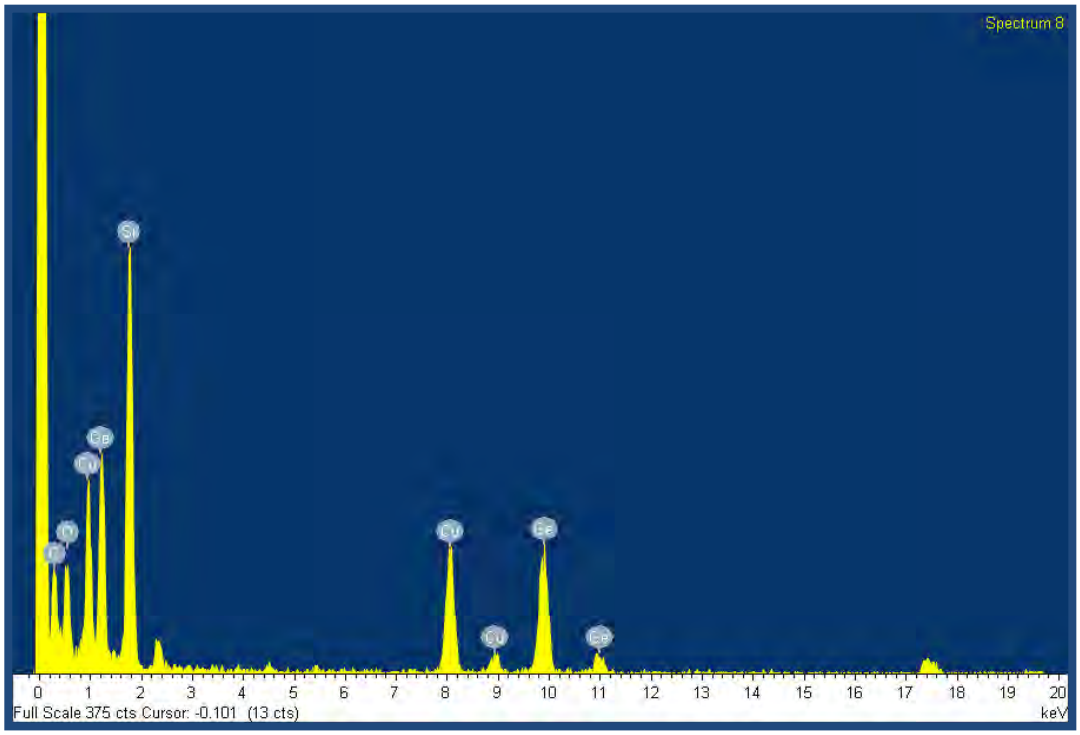


Figure 2.3.2.47: TEM EDS spectrum of PMOS SiGe region, site 8.

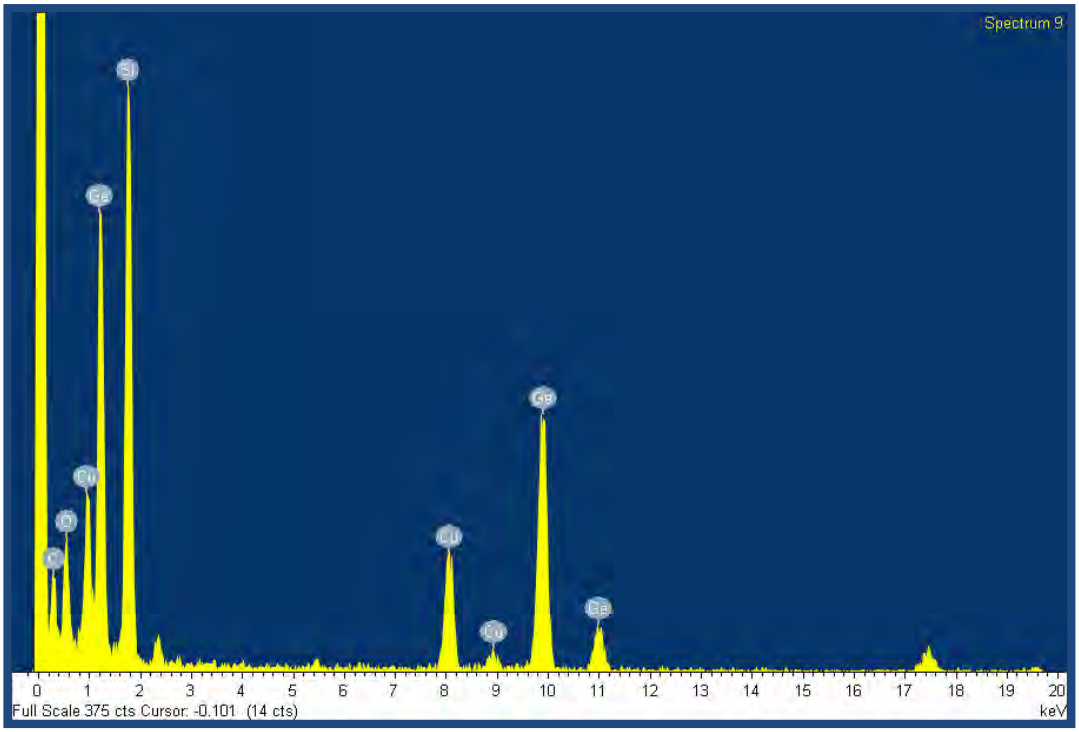


Figure 2.3.2.48: TEM EDS spectrum of SiGe region, site 9.

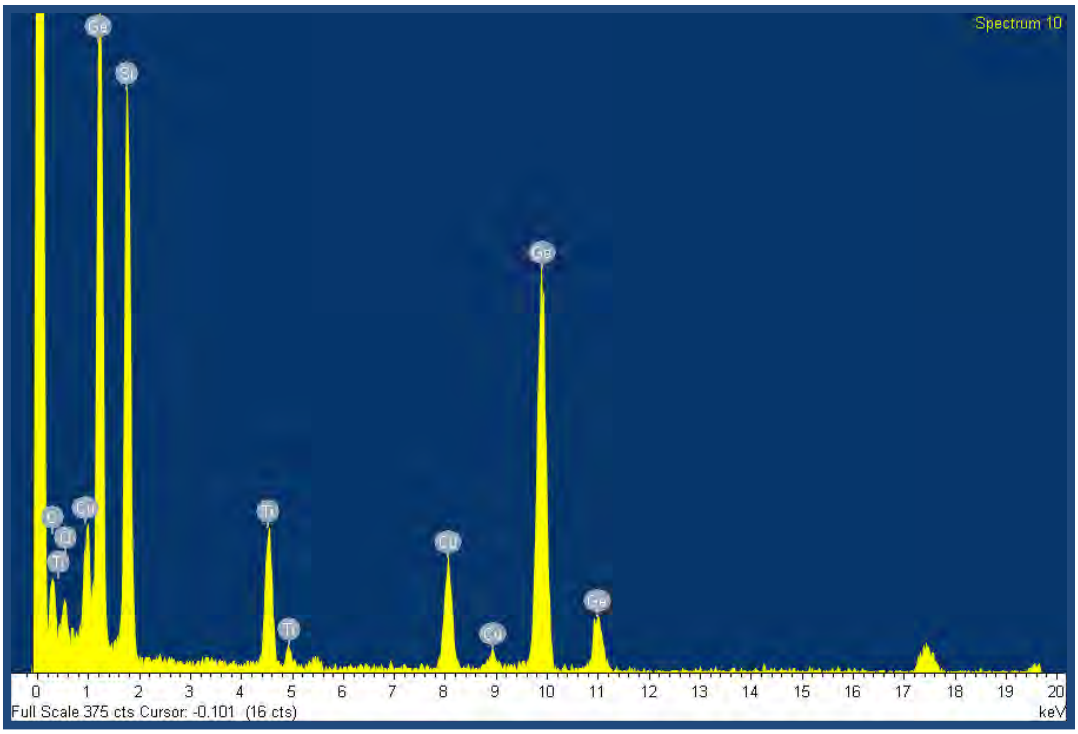


Figure 2.3.2.49: TEM EDS spectrum of TiSiGe interface layer, site 10.

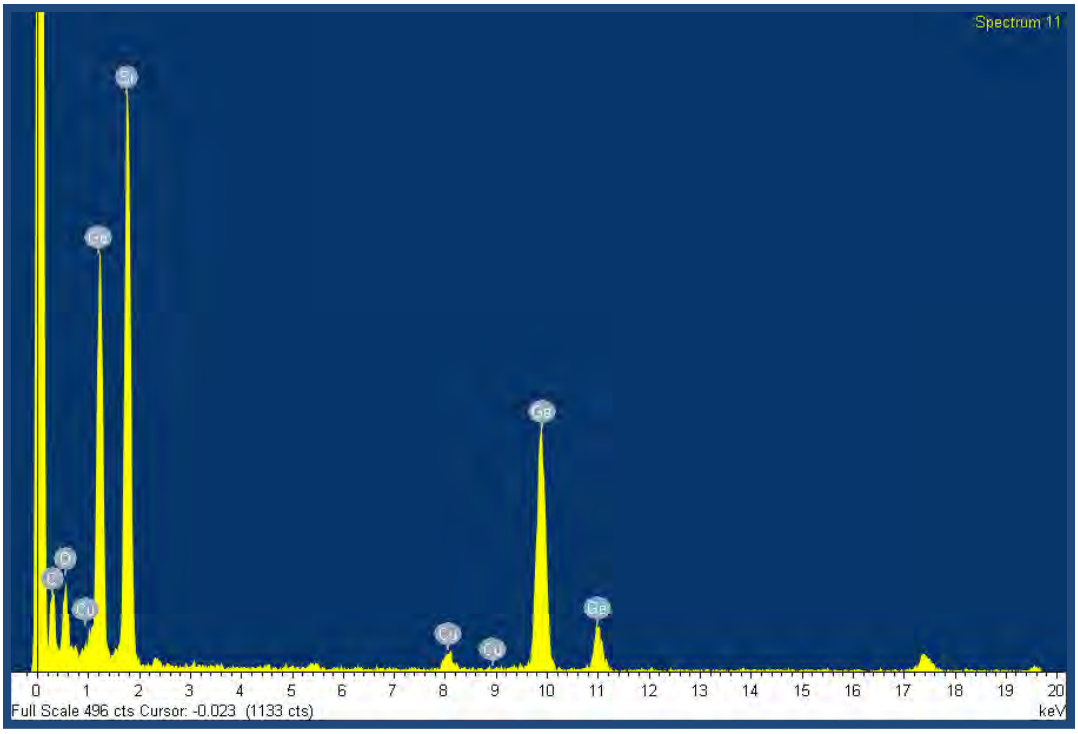


Figure 2.3.2.50: TEM EDS spectrum of PMOS SiGe region, site 11.

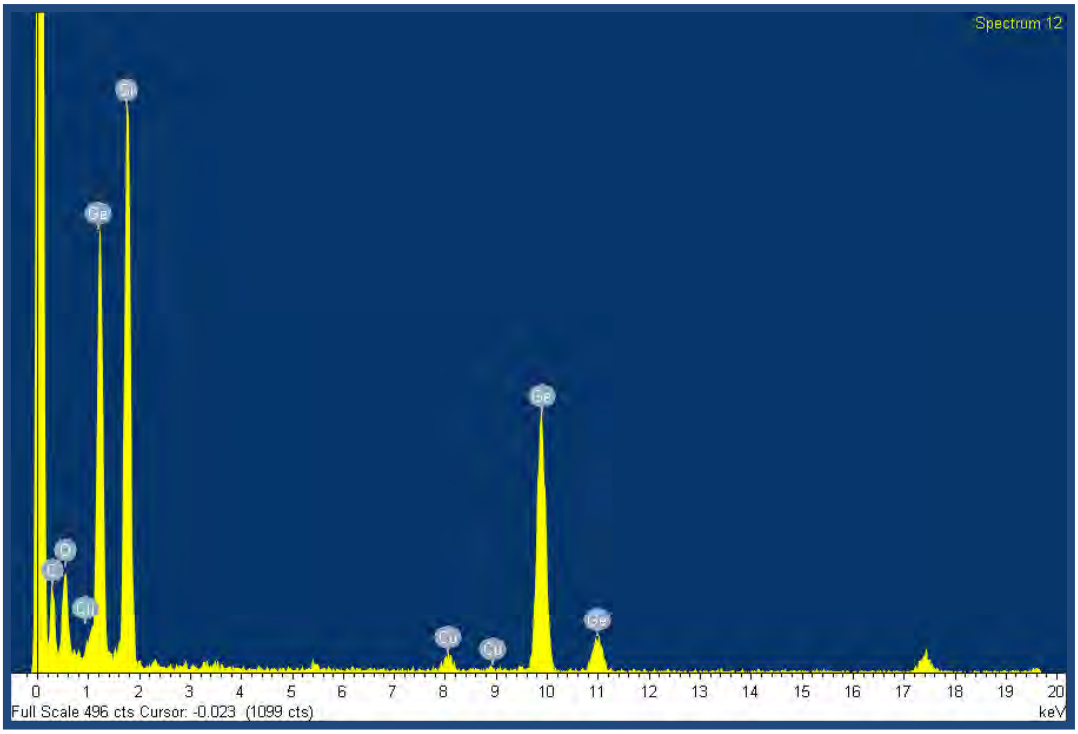


Figure 2.3.2.51: TEM EDS spectrum of PMOS SiGe region, site 12.

Comments
• A thin TiSiGe layer may have been formed at the interface between the SiGe region and a thin Ti adhesion layer on the outer surface of the TiN liner of metal 0 contact.

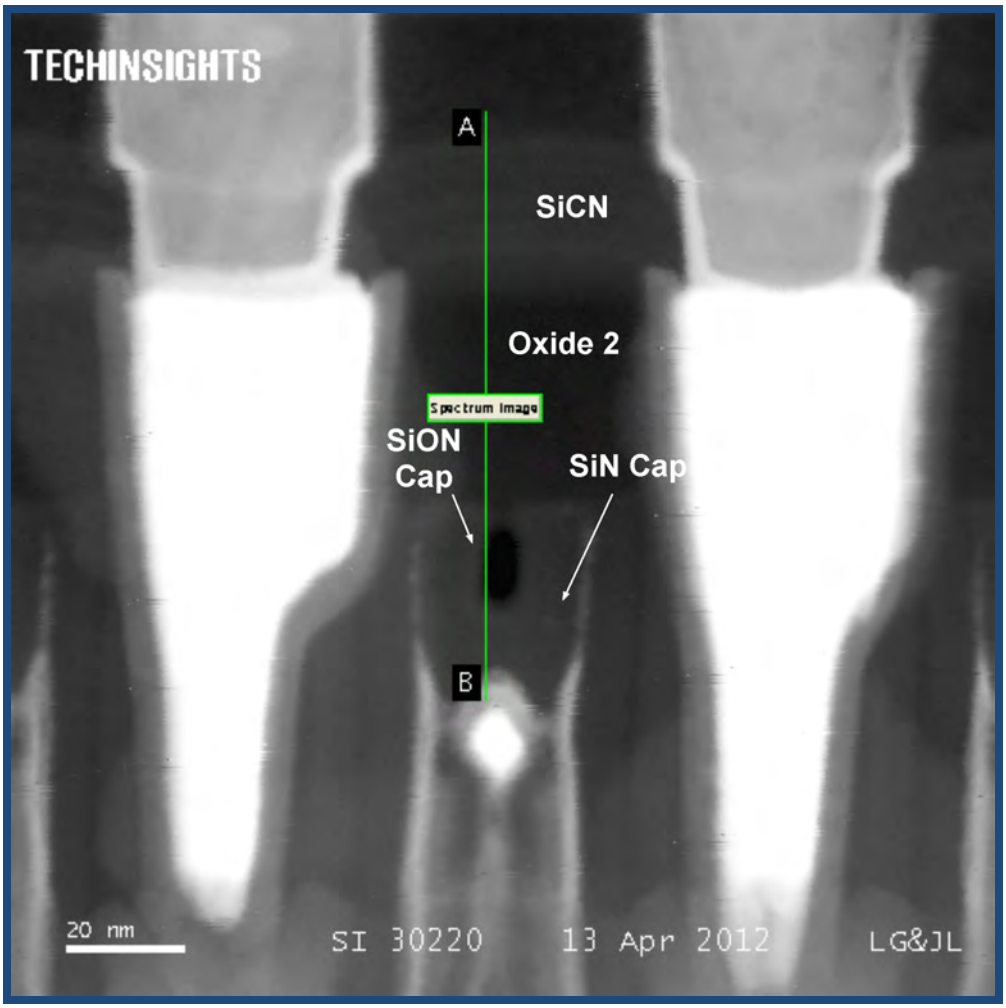


Figure 2.3.2.52: EELS line scan through dielectric layers over a PMOS metal gate, HAADF survey image.

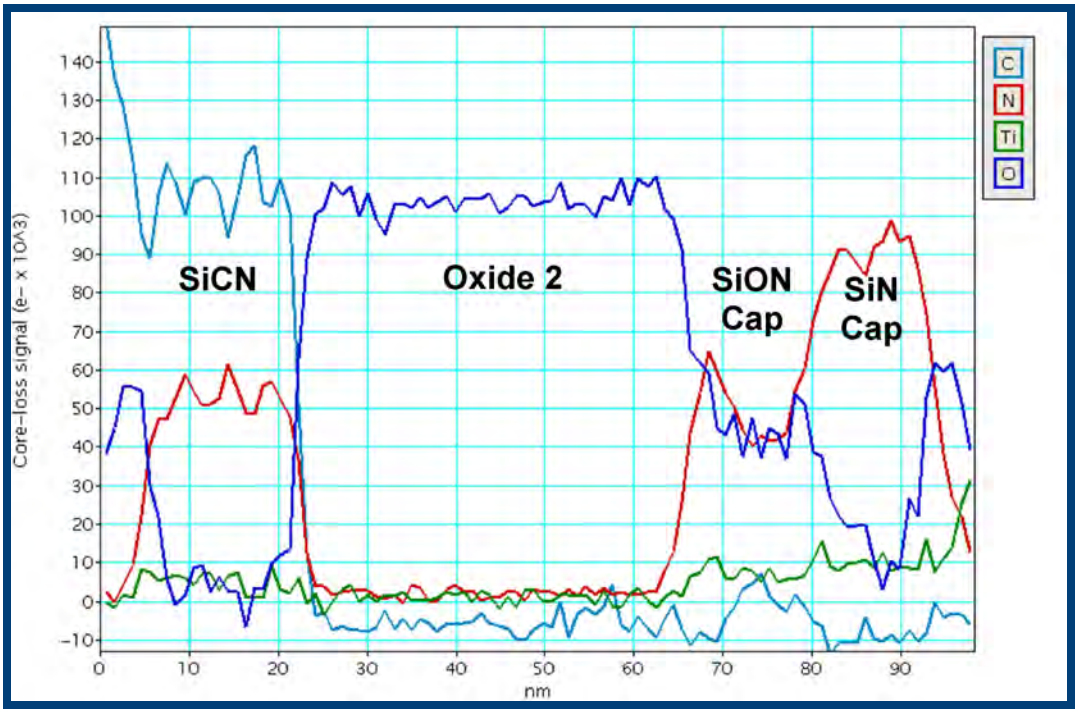


Figure 2.3.2.53: Element profiles of dielectric layers over the PMOS metal gate, EELS line scan.

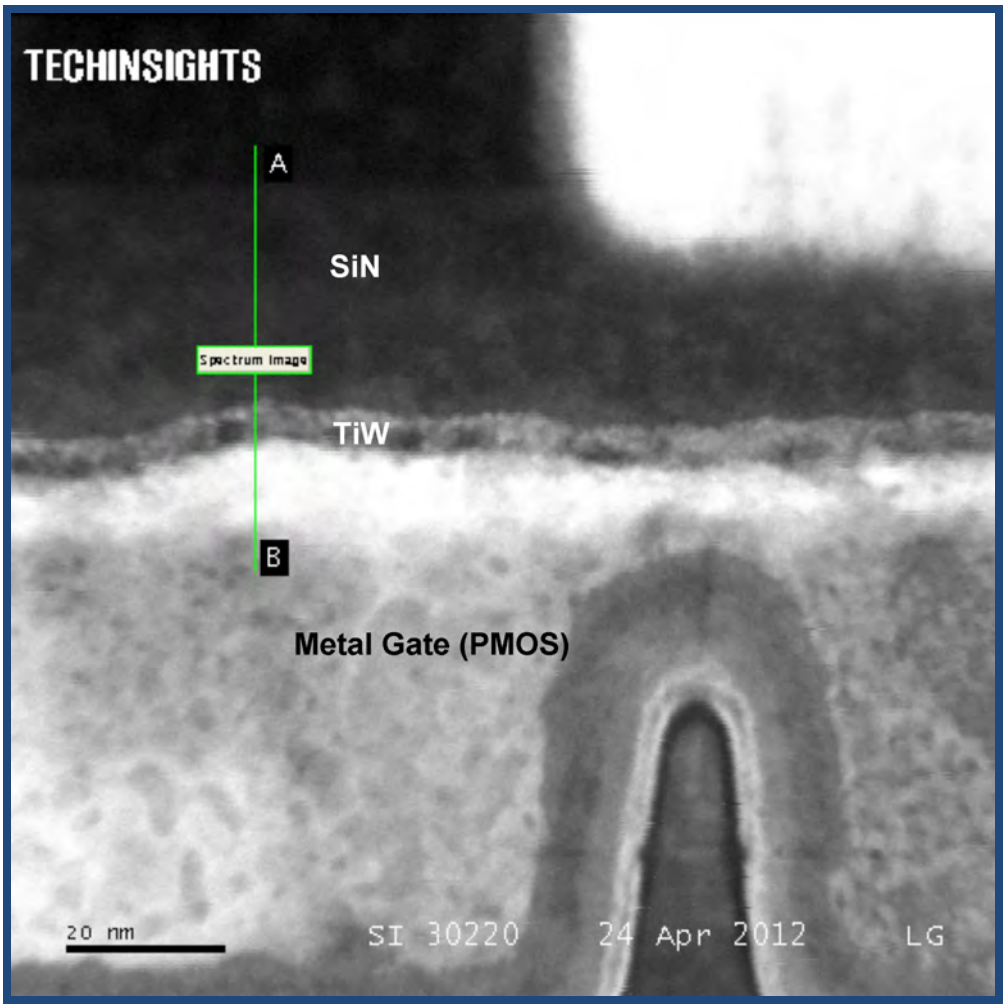


Figure 2.3.2.54: EELS vertical line scan through cap layer, HAADF survey image.

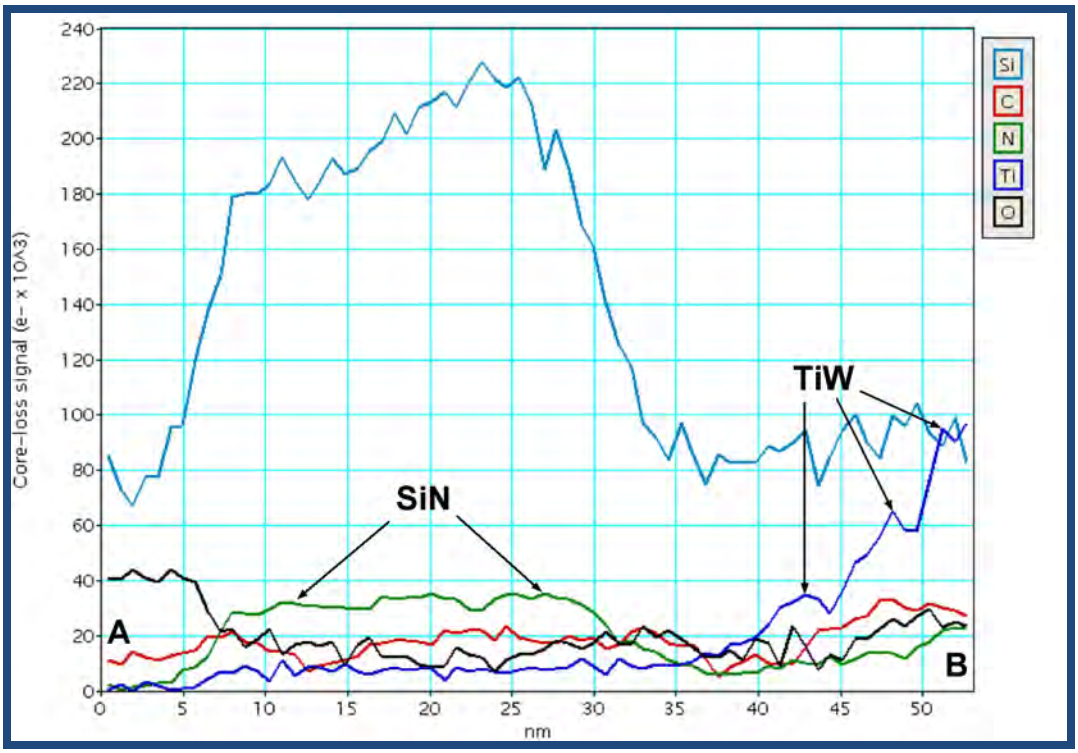


Figure 2.3.2.55: Element profiles of the SiN and cap layers, EELS line scan.

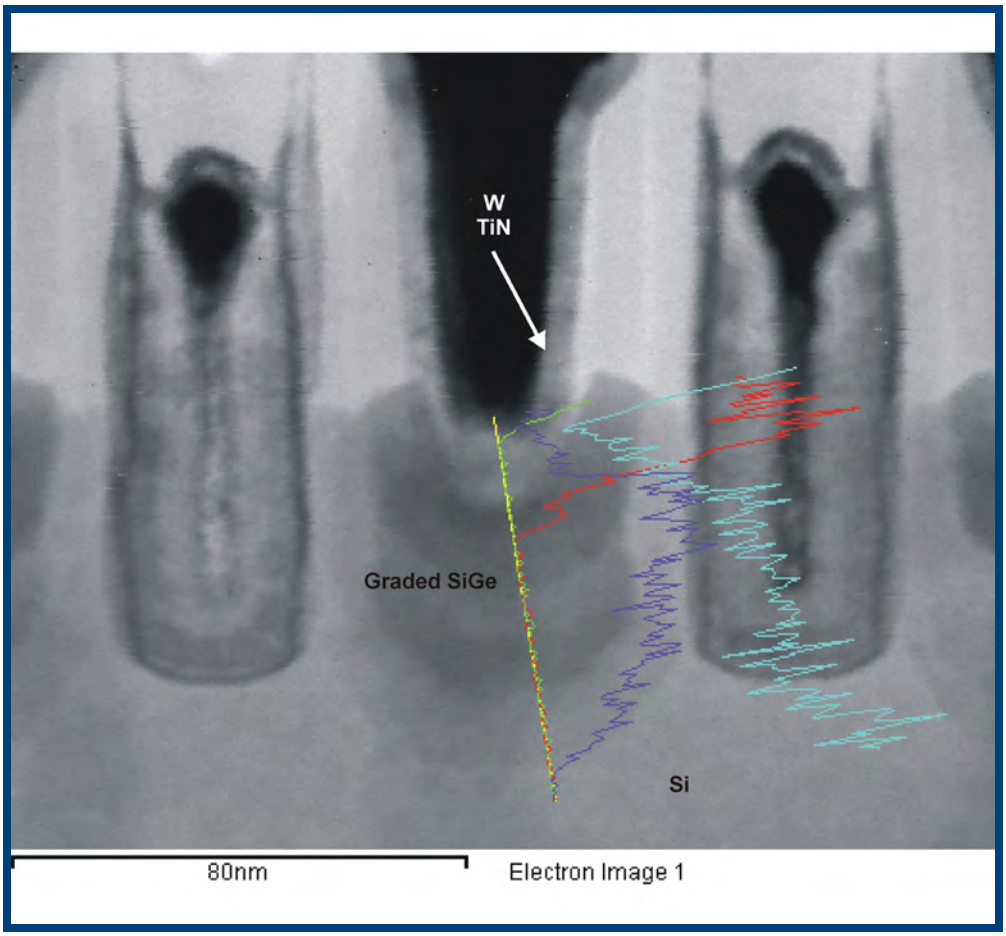


Figure 2.3.2.56: PMOS transistor with a contact to SiGe source/region, and TEM EDS linescan and element profiles overlayed.

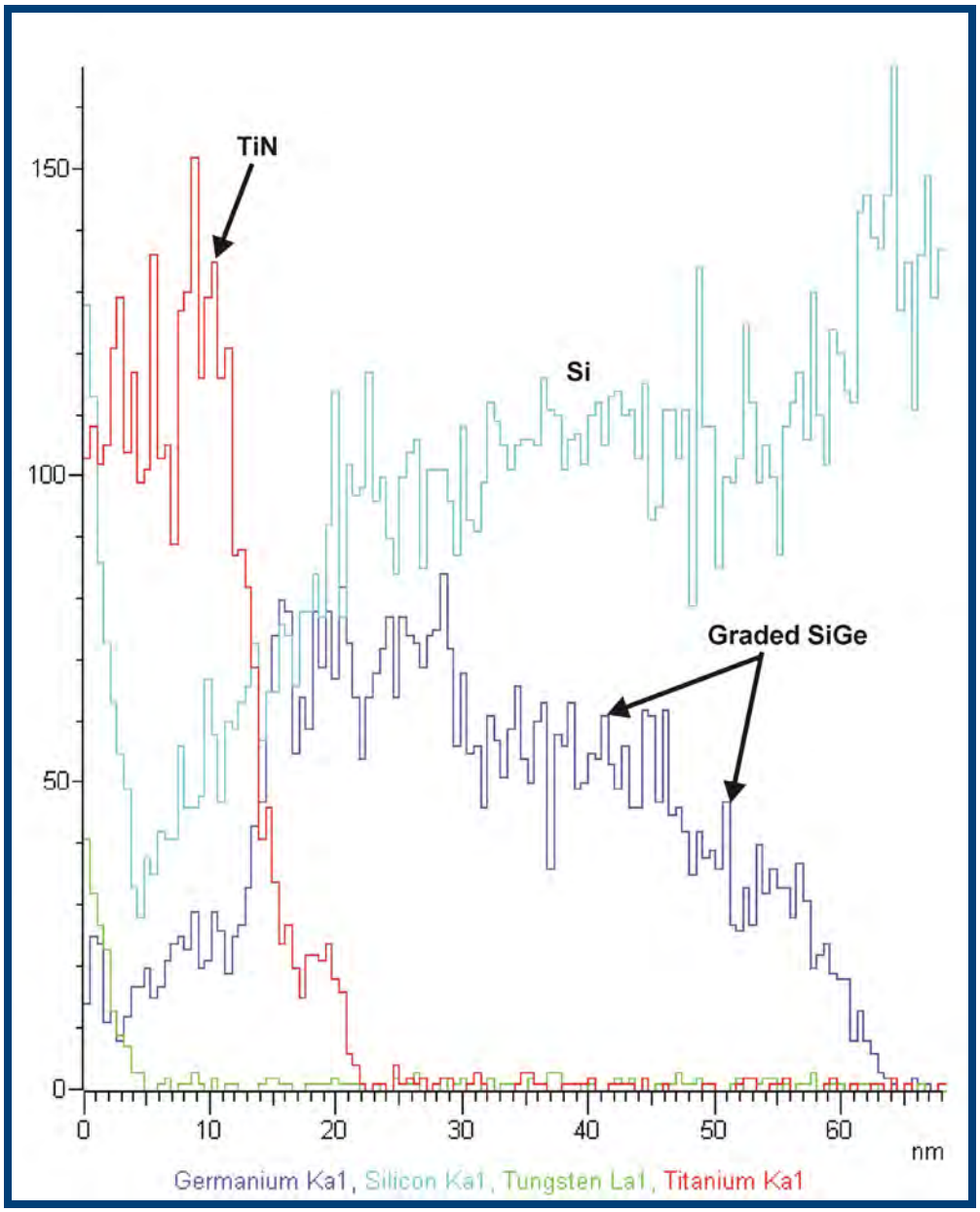


Figure 2.3.2.57: TEM EDS element profiles through the SiGe source/drain region of the PMOS transistor.

2.3.3 Cross-Sectional Analysis of Tri-Gate NMOS Transistors

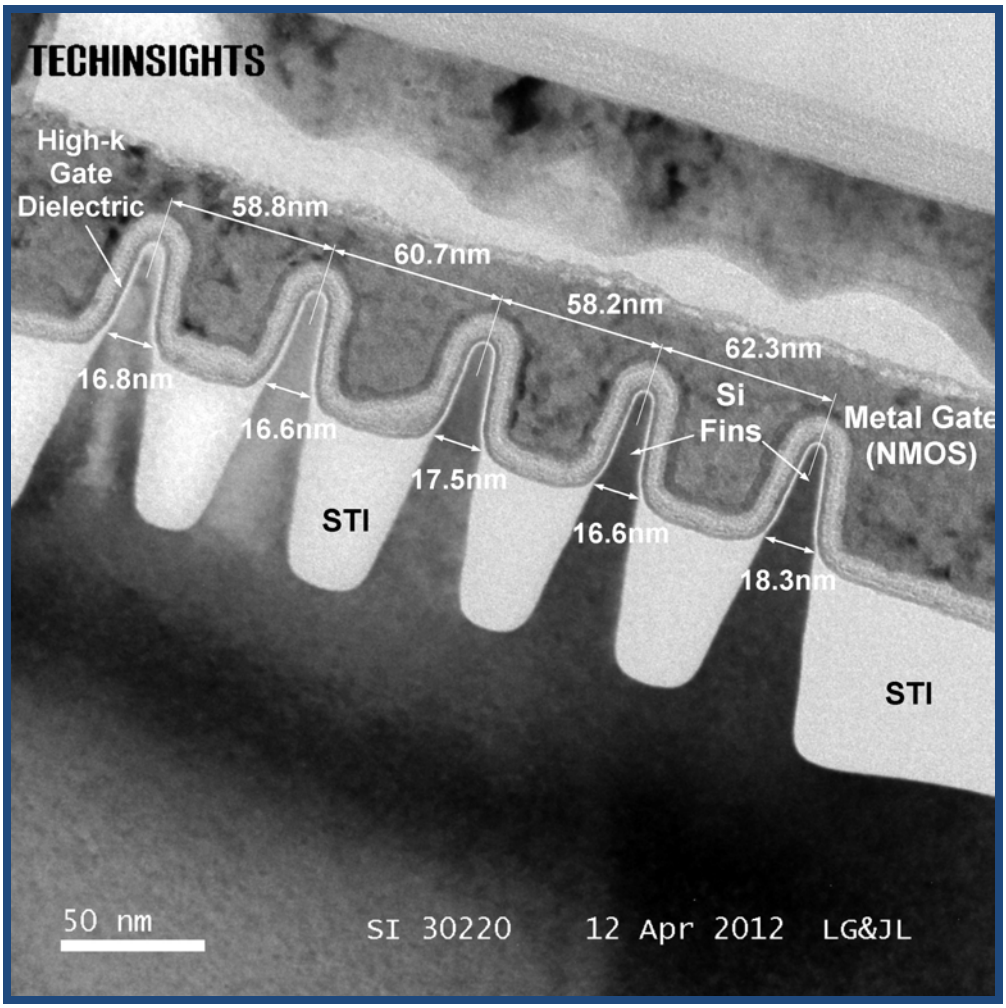


Figure 2.3.3.1: Logic NMOS transistor sectioned across silicon fins and along the NMOS gate, TEM cross-section with fin widths and pitches annotated.

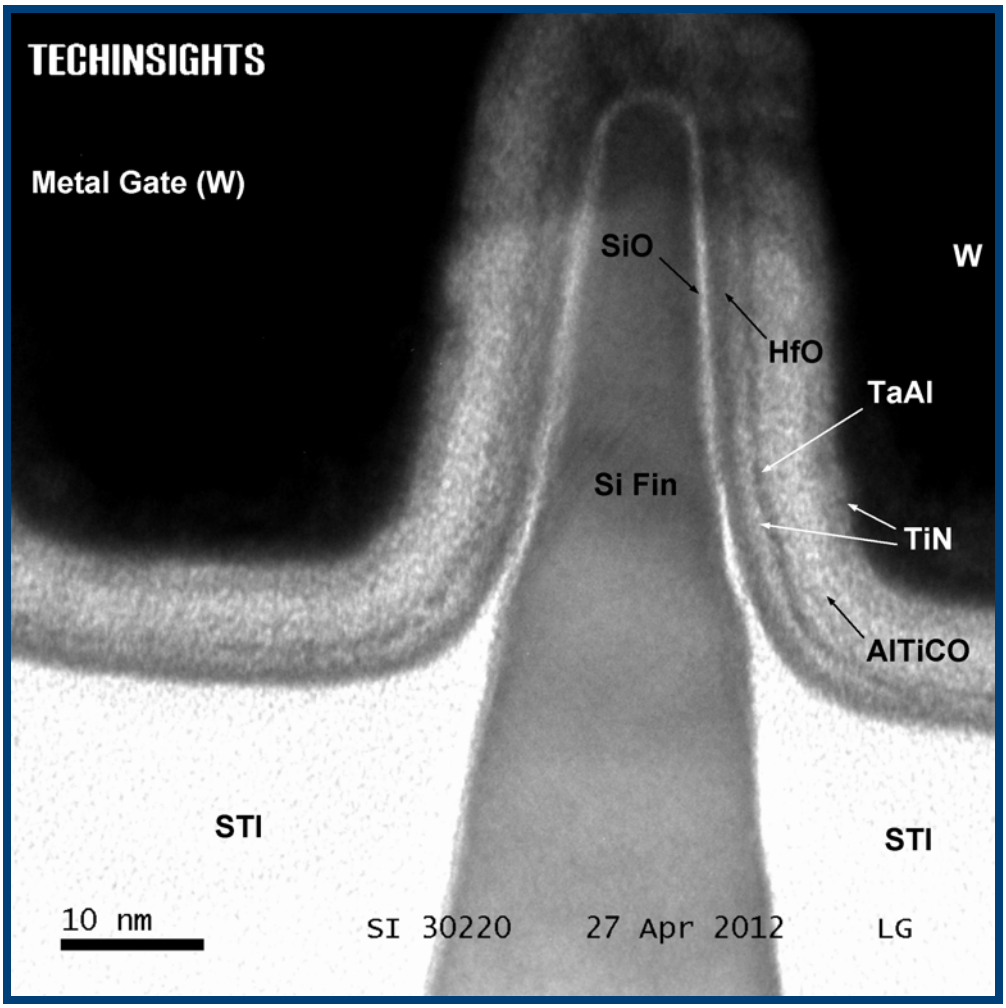


Figure 2.3.3.2: Silicon fin of a logic NMOS transistor with gate layers annotated, HRTEM image.

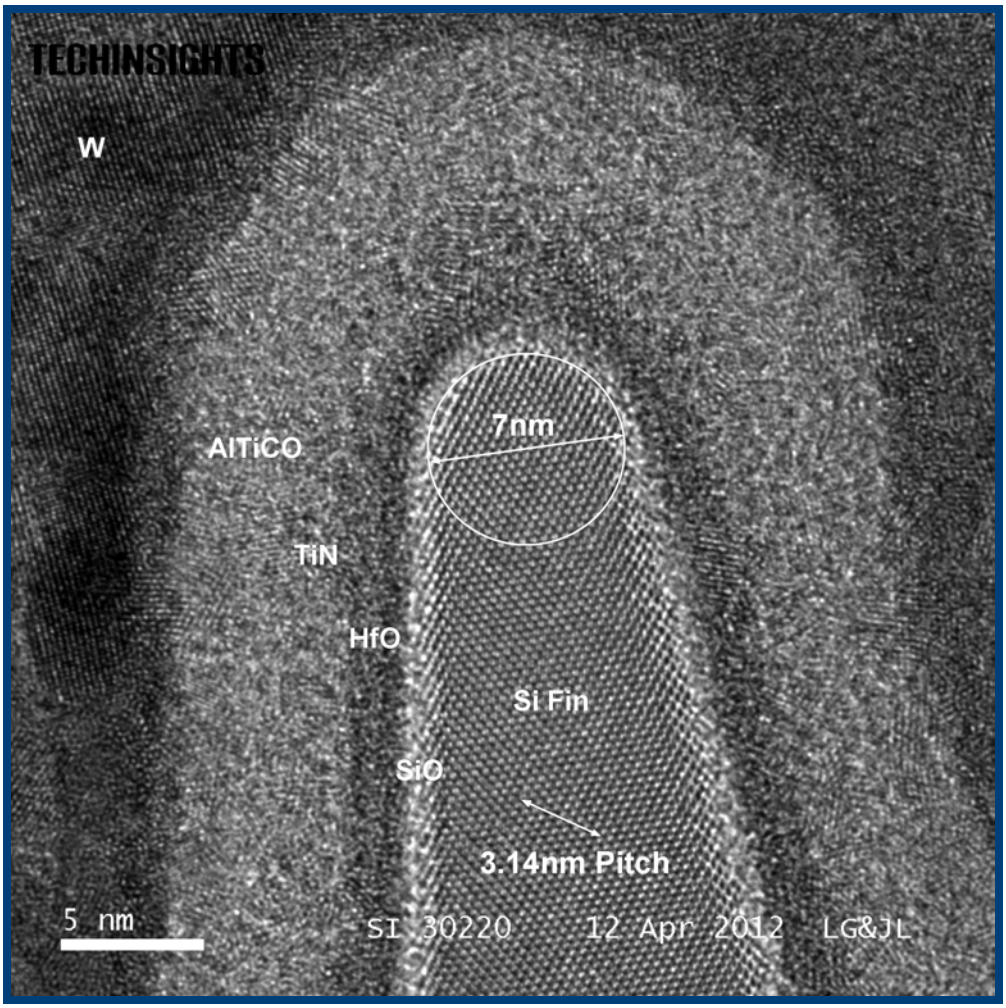


Figure 2.3.3.3: Middle part of the NMOS transistor fin with gate dielectric and metal gate layers, HRTEM image.

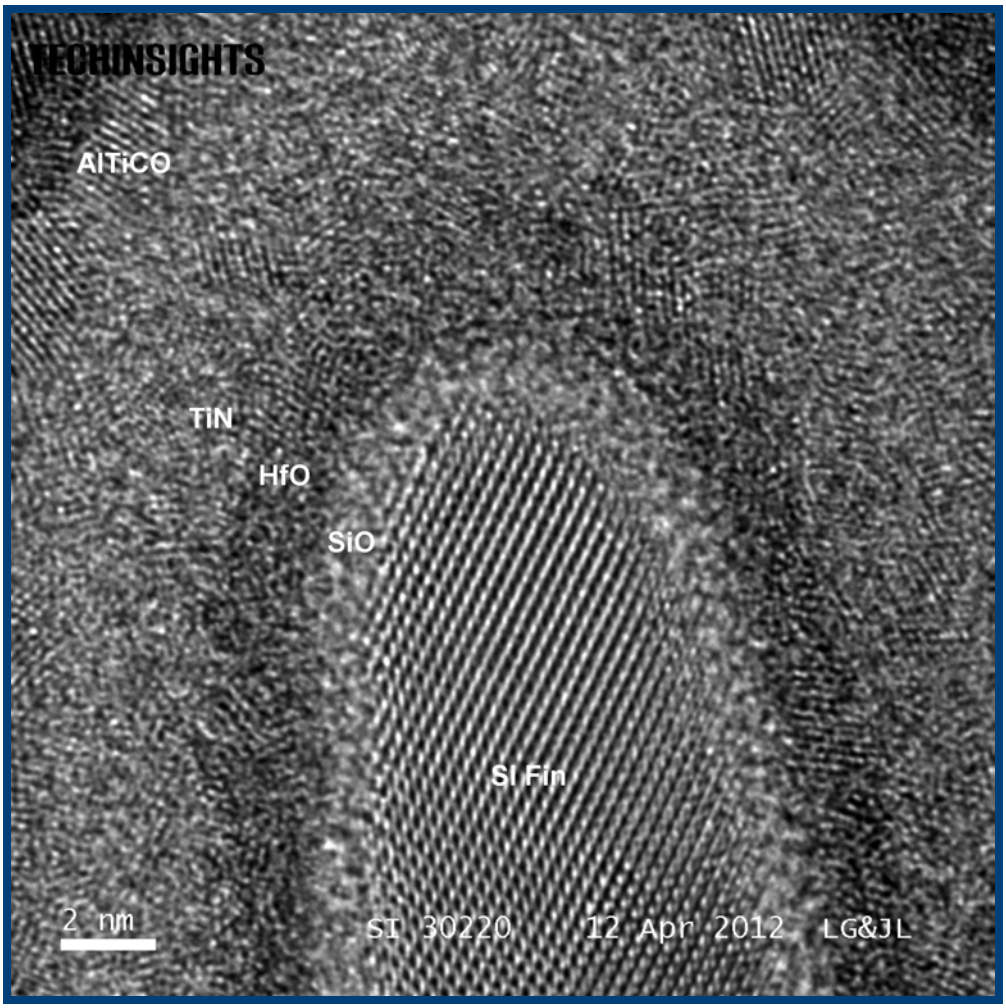


Figure 2.3.3.4: Upper part of the NMOS transistor fin with gate dielectric and metal gate layers, HRTEM image.

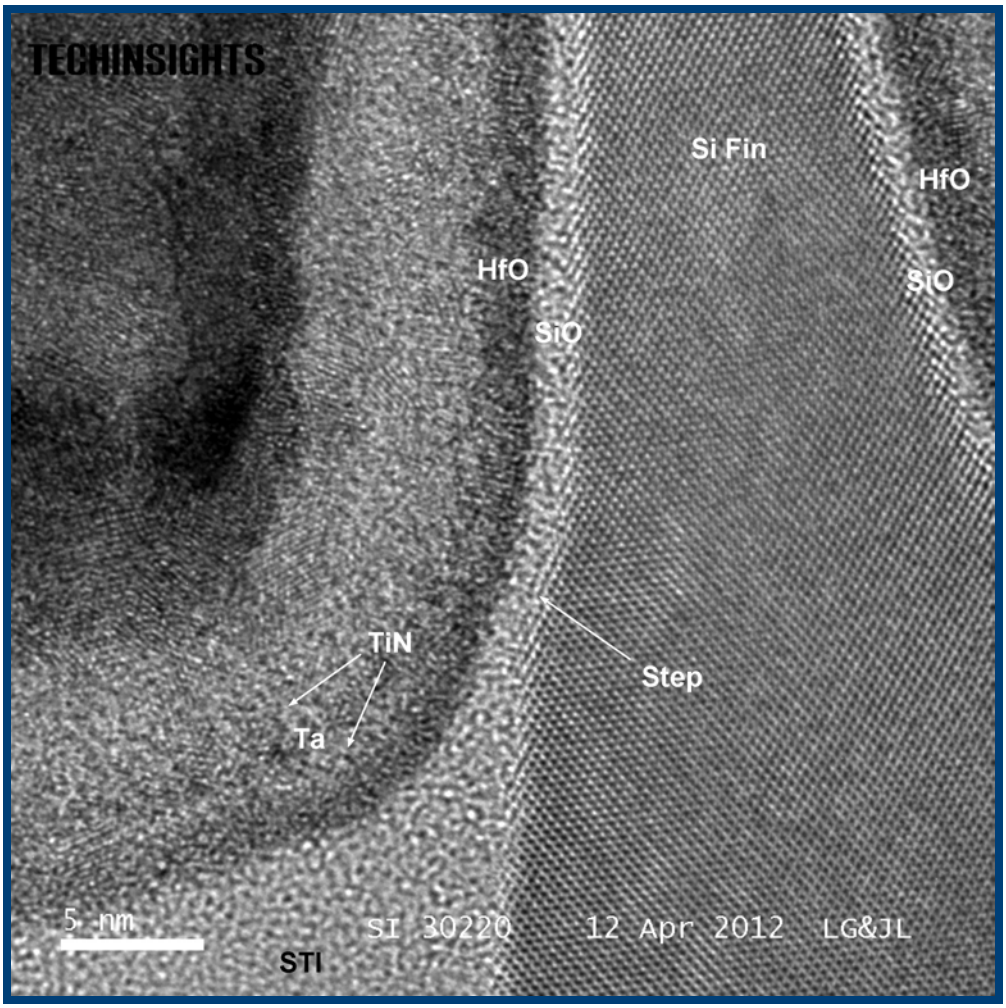


Figure 2.3.3.5: Metal gate and high-k dielectric layers at the bottom of NMOS transistor fin, HRTEM image.

Feature	Dimension	Unit
NMOS gate dielectric thickness	2.6	nm
SiO thickness	0.7	nm
HfO thickness	1.9	nm

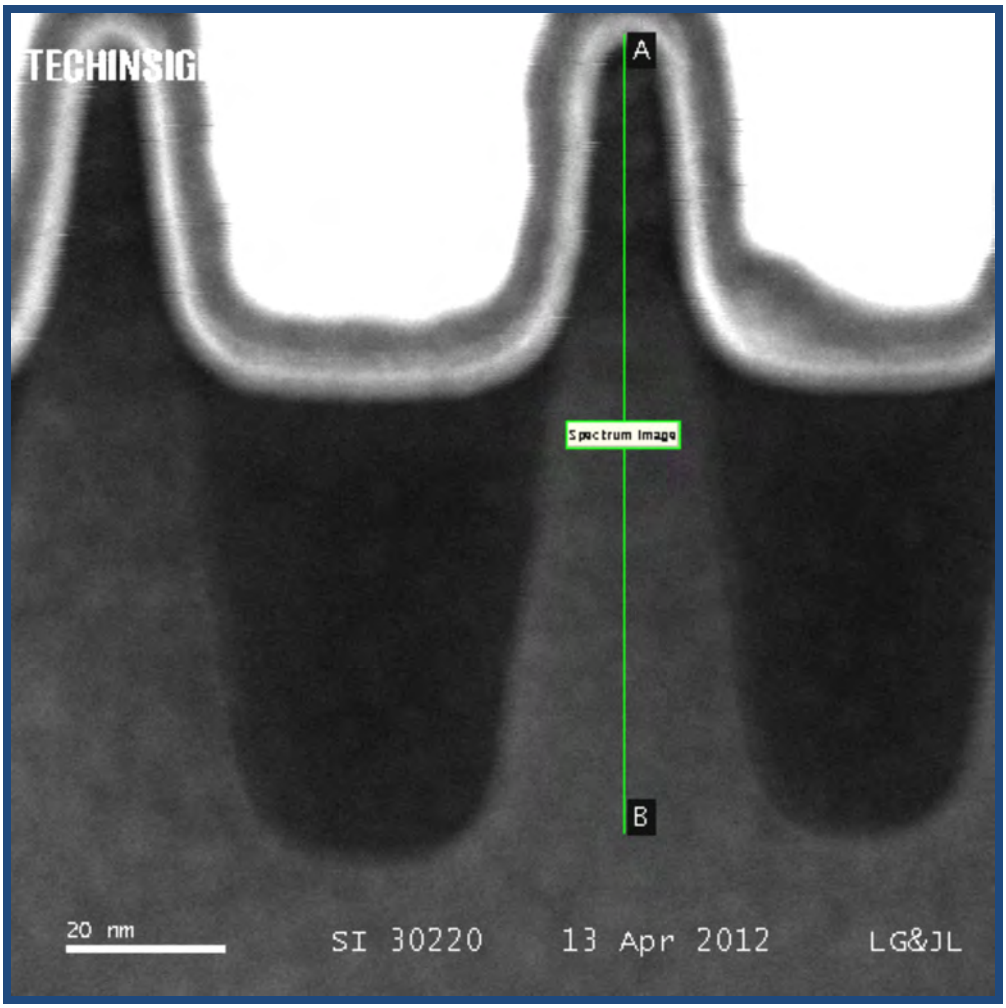


Figure 2.3.3.6: EELS vertical line scan through a silicon fin under an NMOS gate, HAADF survey image.

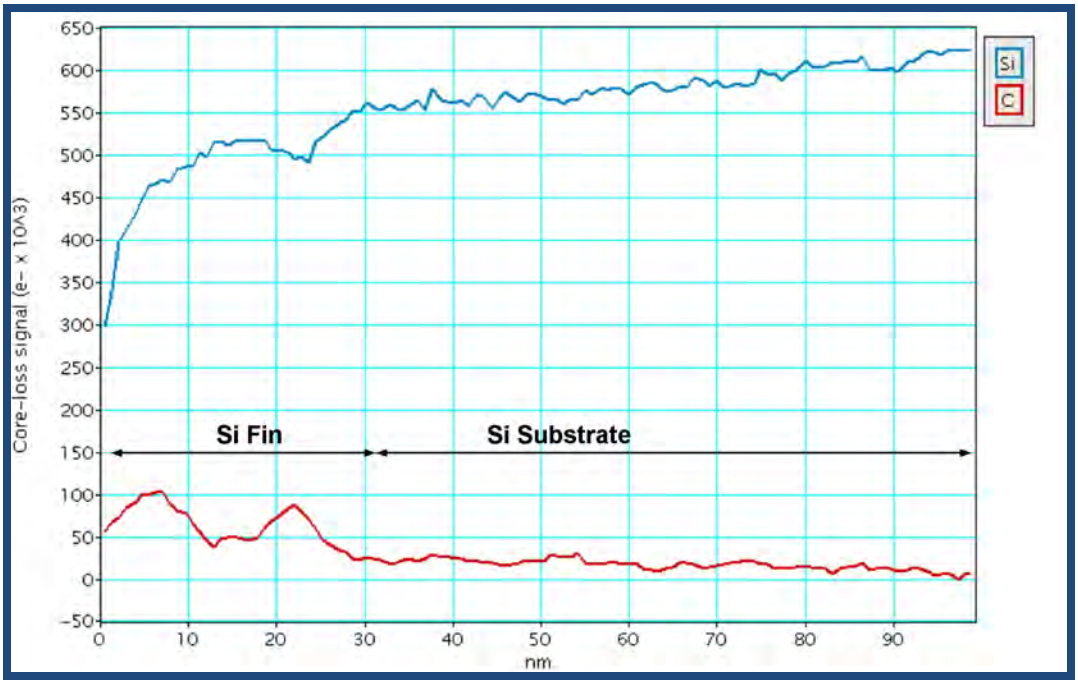


Figure 2.3.3.7: Element profiles of the fin and fin foot regions, EELS line scan.

Comments
• EELS line scan analysis of NMOS fin indicates carbon signal at Si fin level that likely originates from the embedded carbon-doped (eSi:C) source/drain region located in the sample further after the fin. The eSi:C regions have been formed in the source/drain recesses by a selective silicon epitaxial growth, SEG with in-situ carbon incorporated into the Si lattice. The eSi:C regions are likely used to provide tensile strain to the transistor channel located in the Si fin between the Si:C source/drain regions to improve performance of NMOS transistor

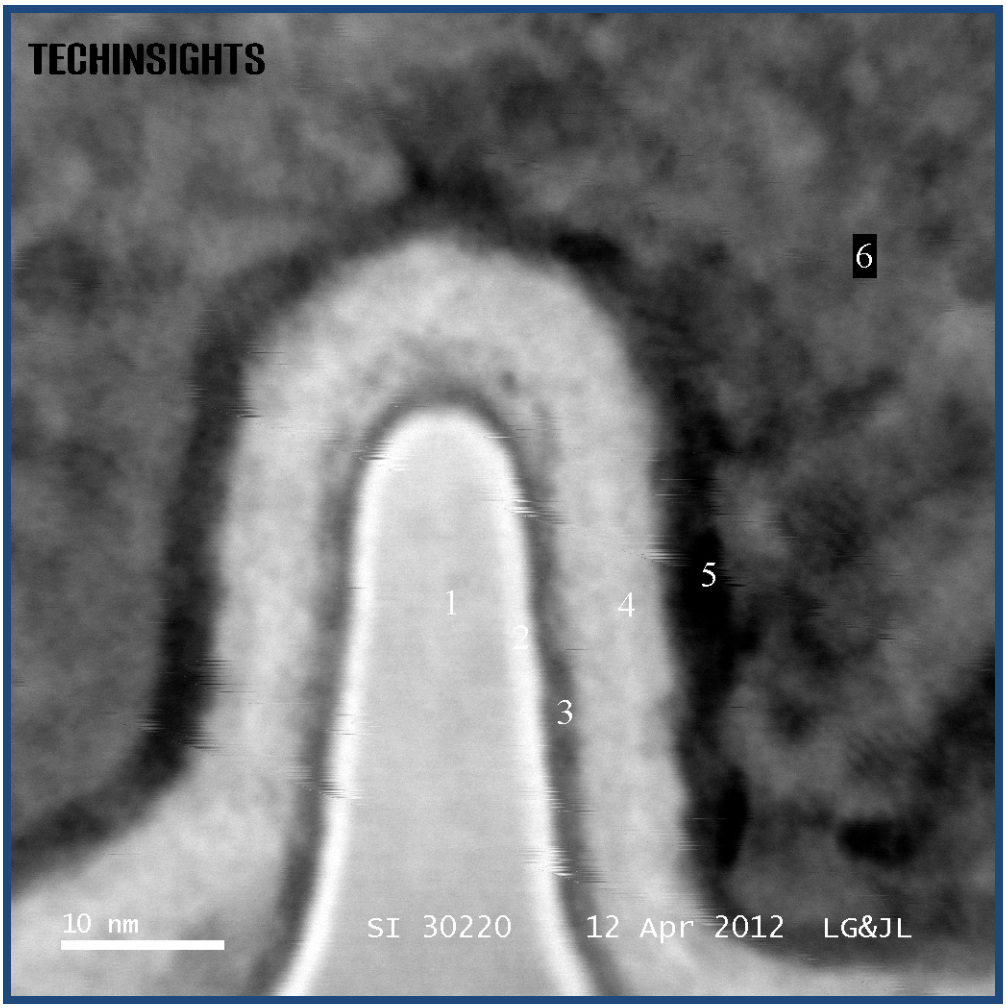


Figure 2.3.3.8: NMOS transistor, TEM cross-section along metal gate with EDS sites annotated.

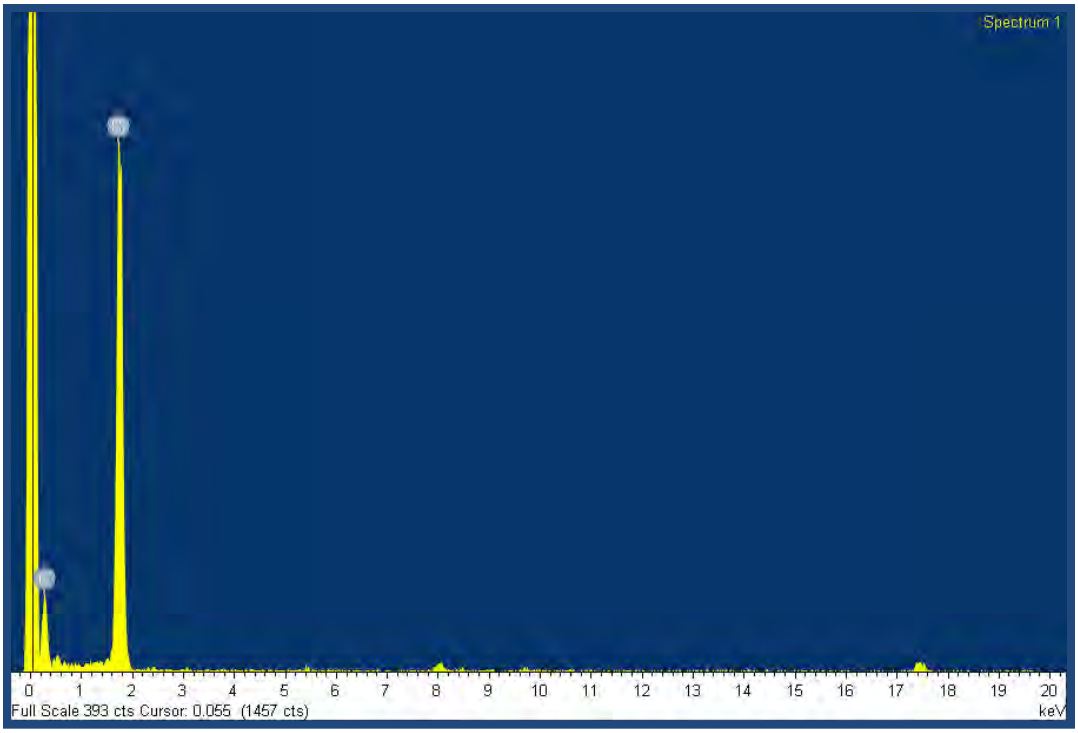


Figure 2.3.3.9: TEM EDS spectrum of silicon fin, site 1.

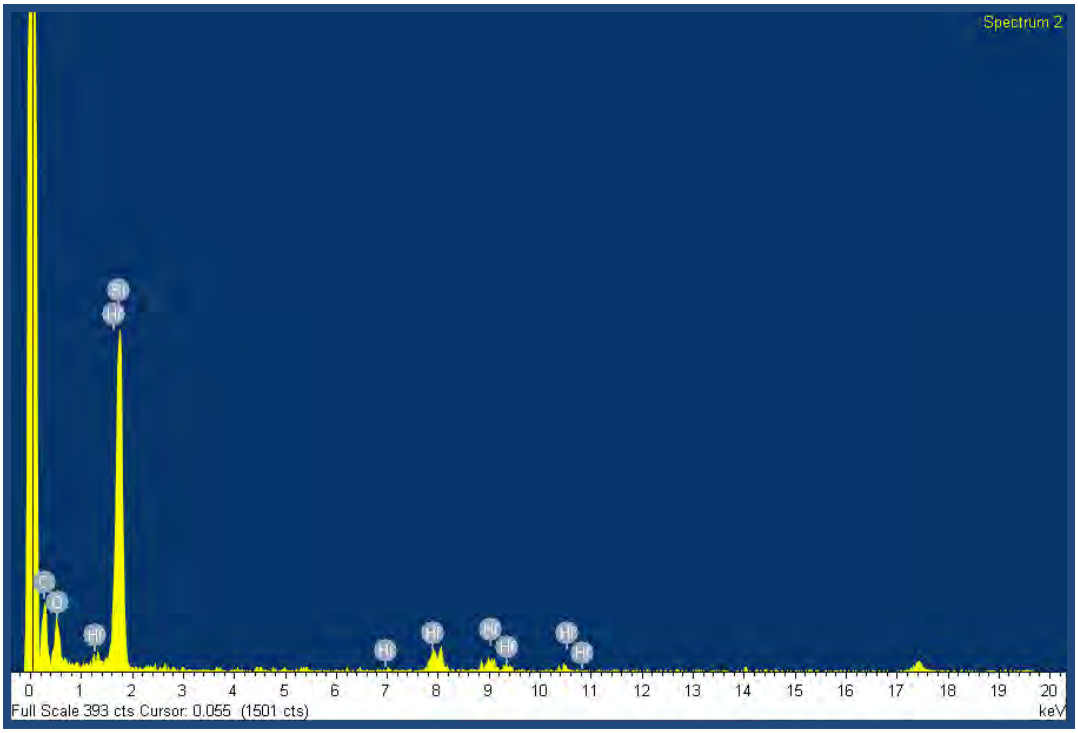


Figure 2.3.3.10: TEM EDS spectrum of HfO and SiO gate dielectric, site 2.

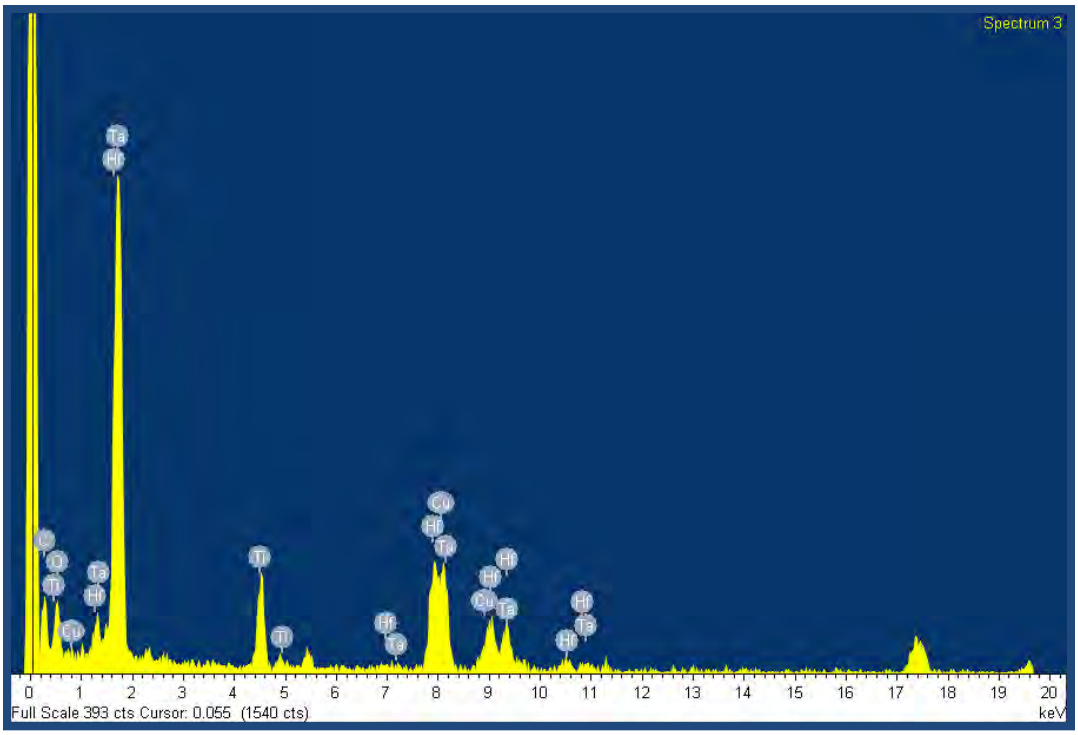


Figure 2.3.3.11: TEM EDS spectrum of high-k gate dielectric TaAl and TiN layers, site 3.

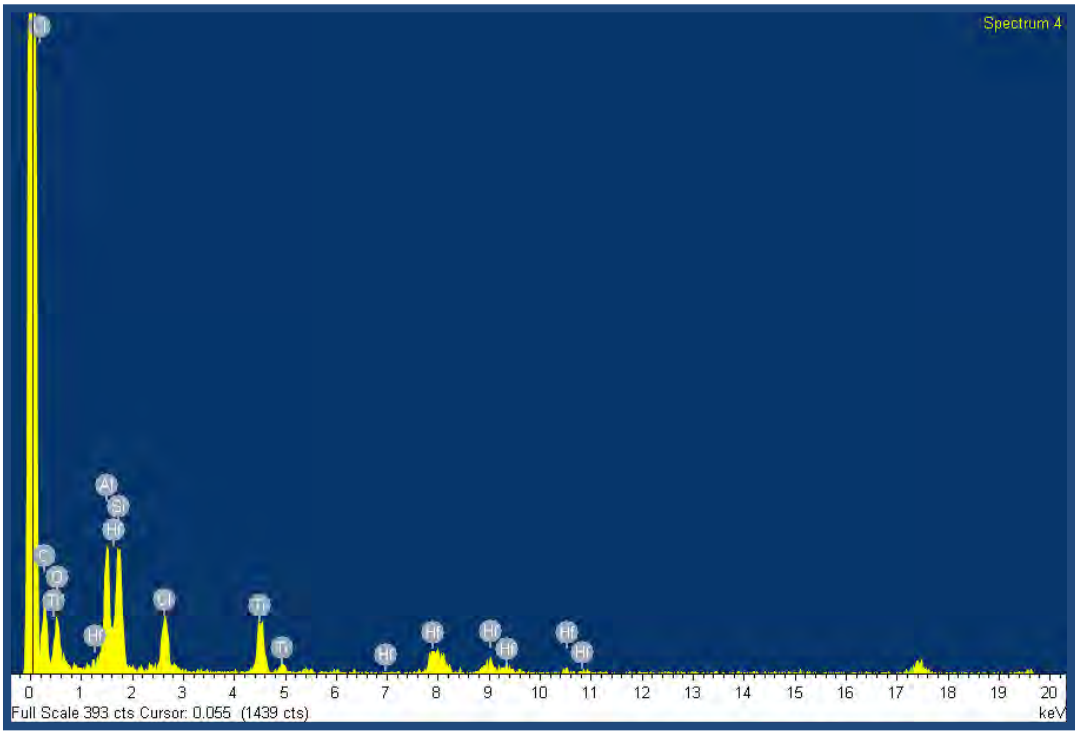


Figure 2.3.3.12: TEM EDS spectrum of metal gate AlTiCO layer, site 4.

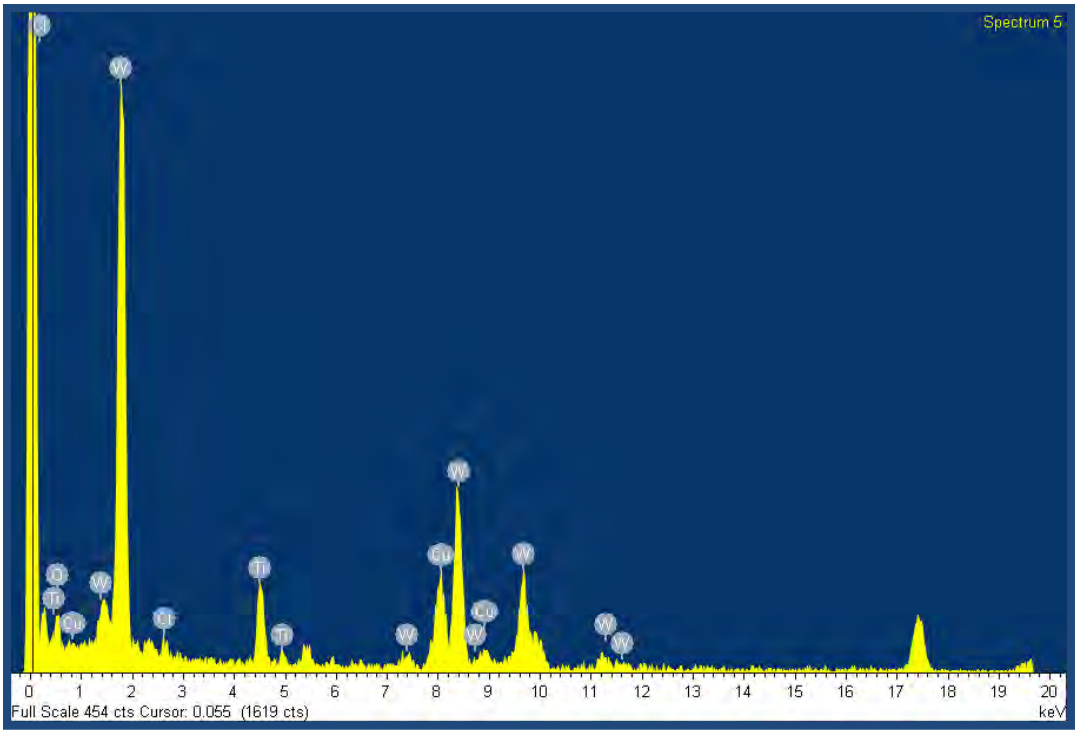


Figure 2.3.3.13: TEM EDS spectrum of metal gate TiN and W layers, site 5. Copper peaks are artifacts.

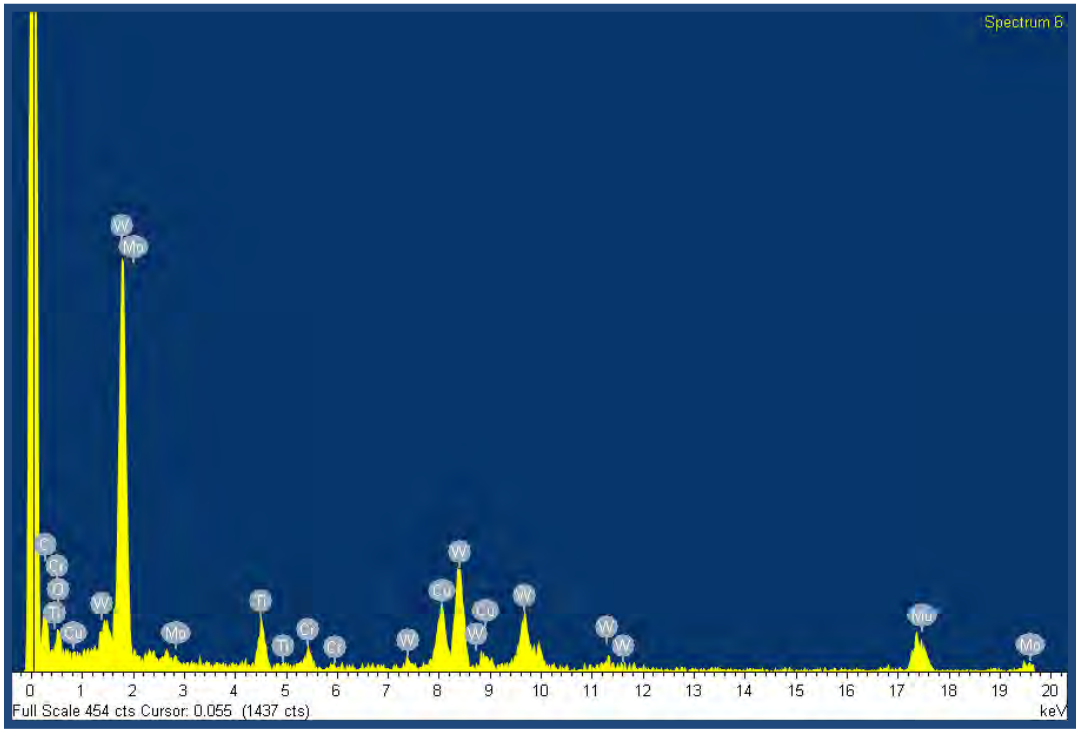


Figure 2.3.3.14: TEM EDS spectrum of metal gate W fill layer, site 6.

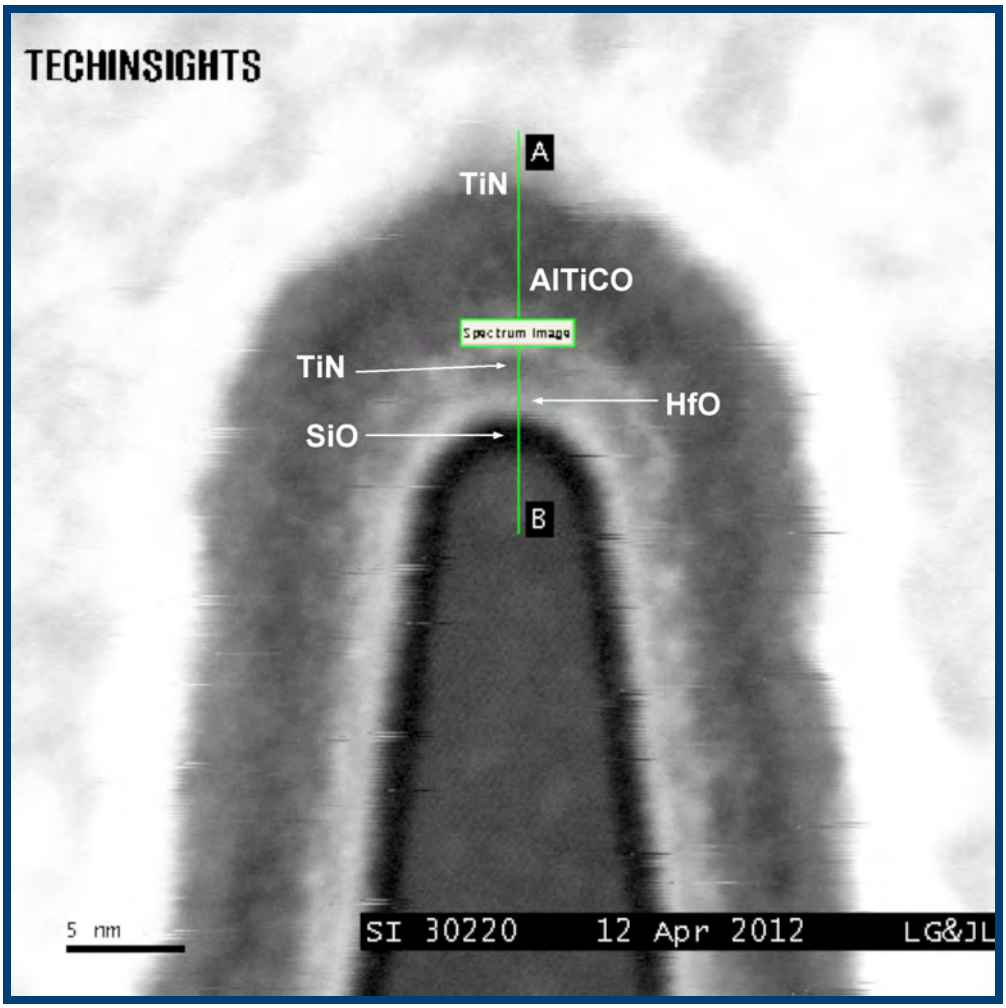


Figure 2.3.3.15: EELS vertical line scan through an NMOS gate, HAADF survey image.

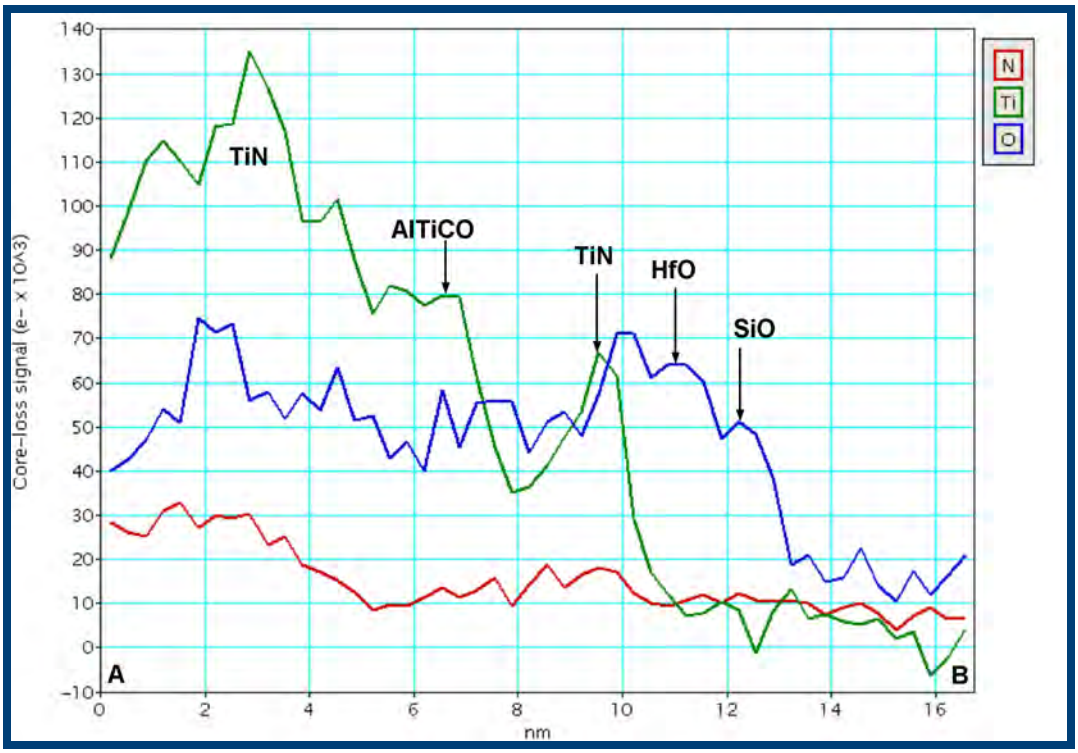


Figure 2.3.3.16: Element profiles of the NMOS gate and high-k gate dielectric, EELS vertical line scan.

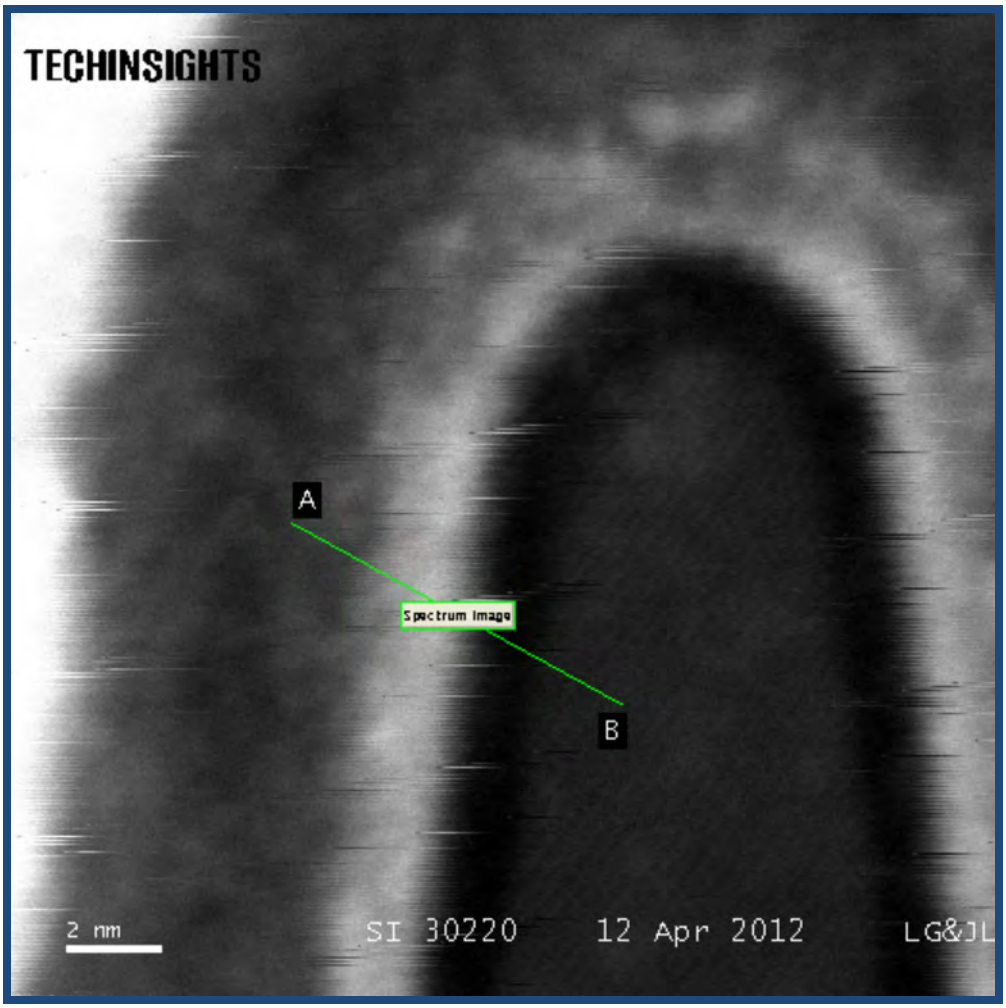


Figure 2.3.3.17: EELS horizontal line scan through an NMOS gate, HAADF survey image.

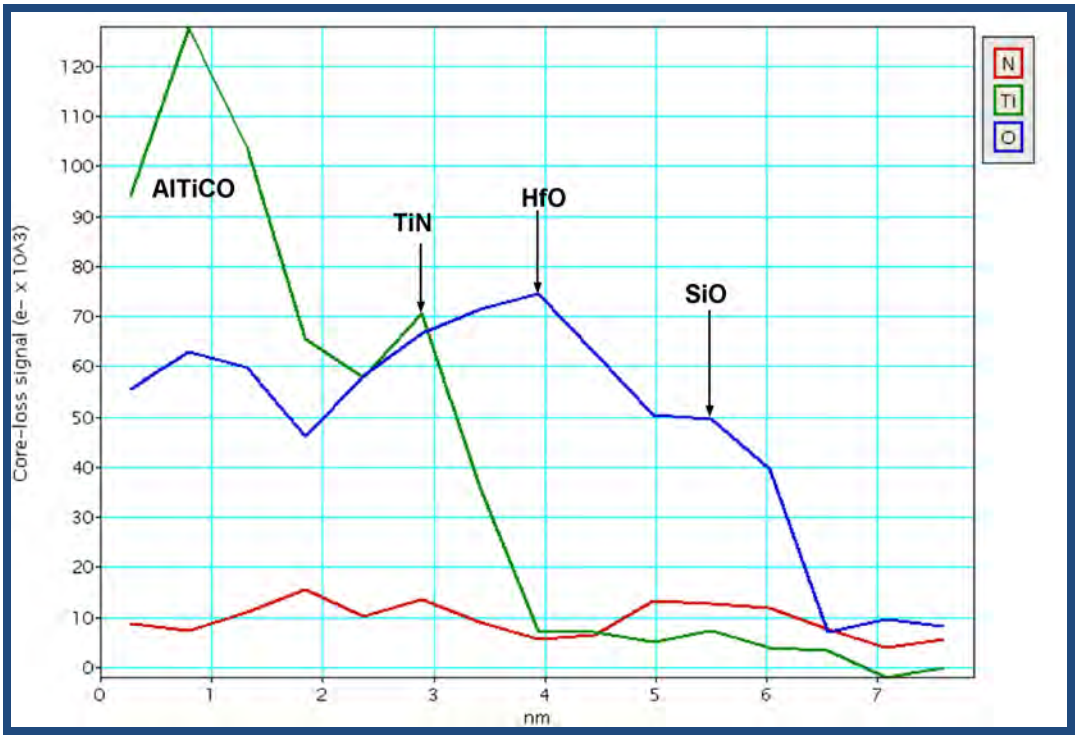


Figure 2.3.3.18: Element profiles of the NMOS gate and high-k gate dielectric, EELS horizontal line scan.

Feature	Dimension	Unit
NMOS gate stack thickness	13.5	nm
TiN layer above HfO	1	nm
TaAl barrier	1	nm
AlTiCO work function metal	2.9	nm
TiN layer	2.6	nm
W gate fill	6	nm

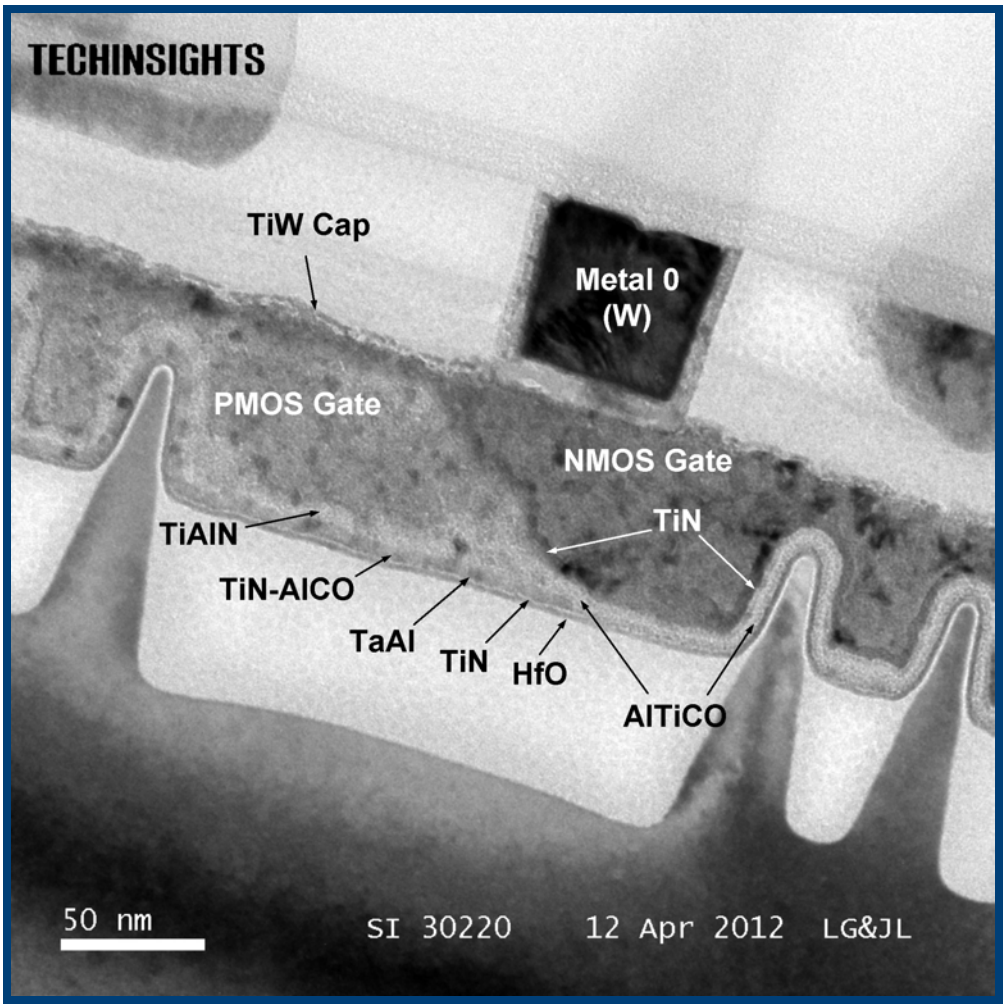


Figure 2.3.3.19: Transition between PMOS and NMOS metal gate layers, TEM cross-section along a common gate.

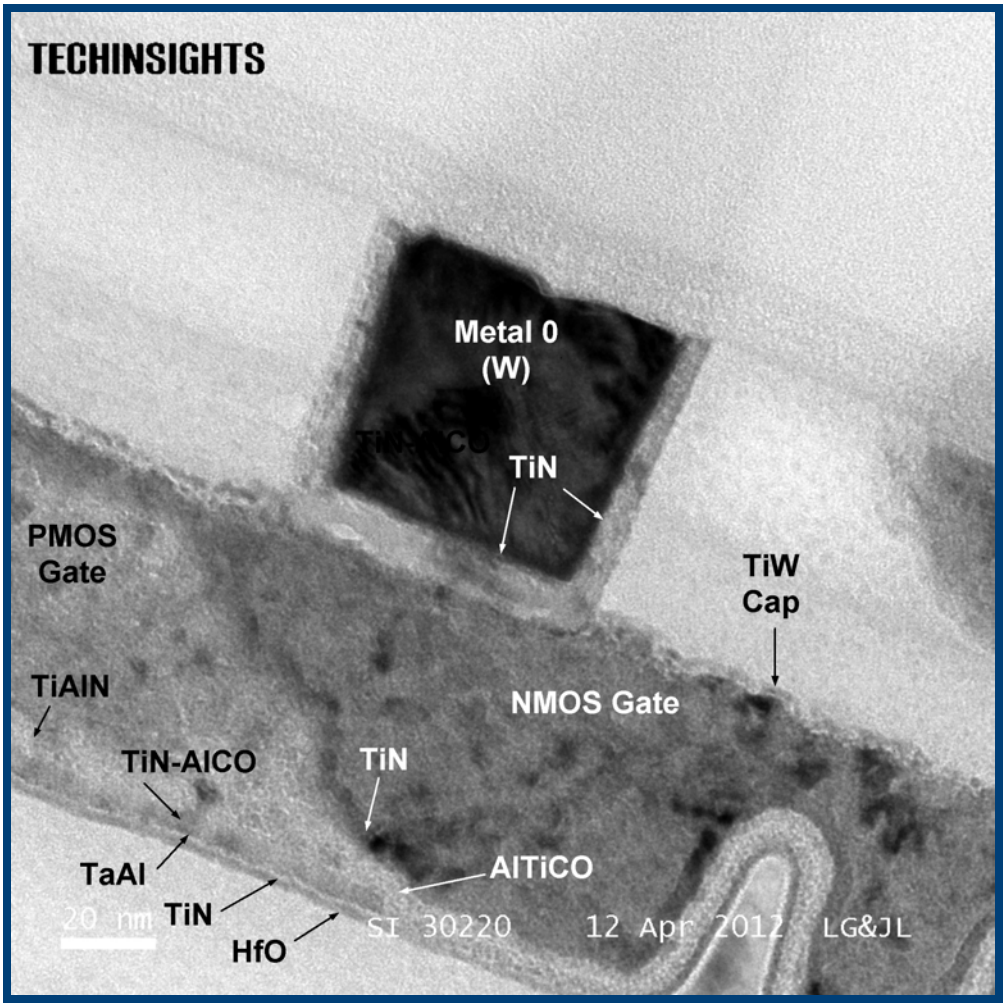


Figure 2.3.3.20: Transition between metal gate layers of PMOS and NMOS transistors, high magnification TEM cross-section along a common gate.

Comments

- Three dimensional Intel Tri-Gate transistors with silicon fin, replacement metal gate and high-k gate dielectric have been used as NMOS transistors;
- High-k dielectric HfO with bottom interface SiO layer used as the NMOS gate dielectric stack; the same gate dielectric used for PMOS transistors;
- Multi-layer replacement metal gate used for NMOS transistor:
  - Thin TiN layer above HfO;
  - Thin TaAl barrier layer;
  - The AlTiCO and TiN used as work function metal;
  - Relatively thick W layer used as a gate filling metal;
  - Thin TiW gate capping layer;
  - The bottom part of the dielectric/gate stack (SiO/HfO/TiN/TaAl) and W gate fill seem to be the same for NMOS and PMOS gates.

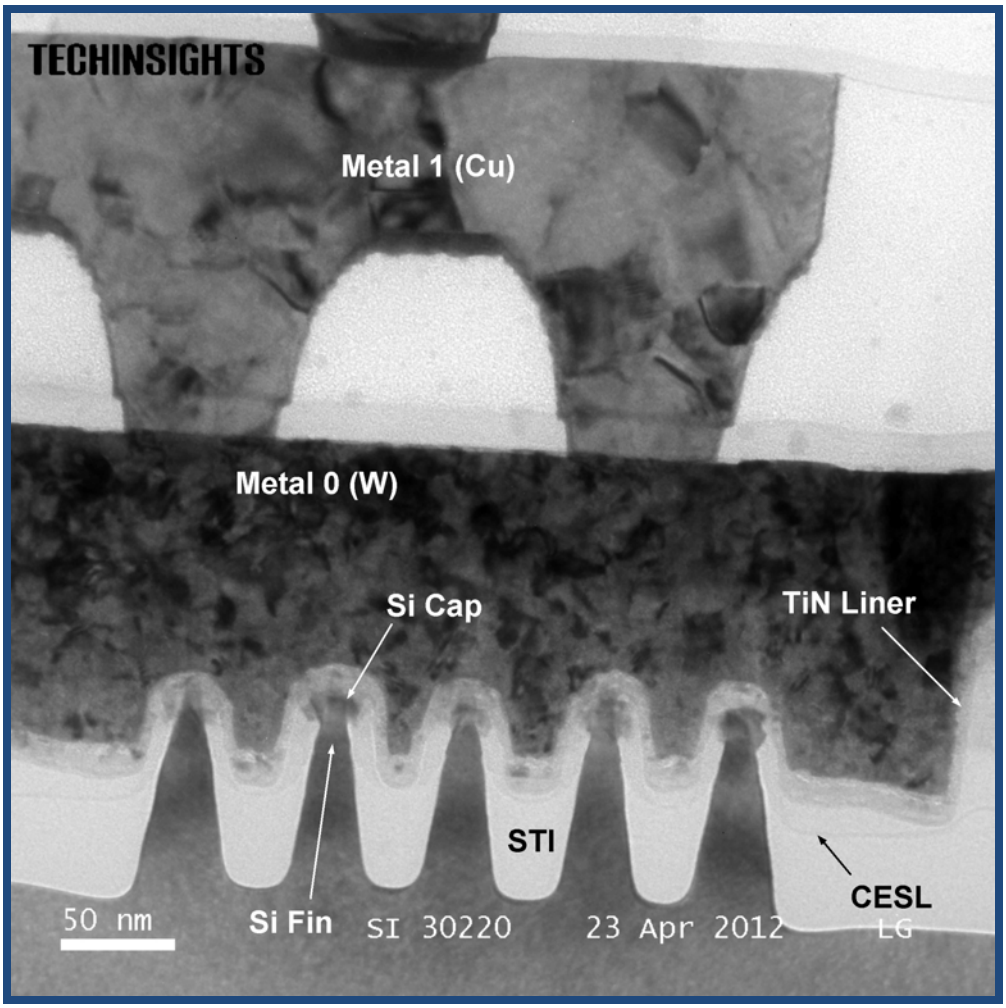


Figure 2.3.3.21: Metal 0 contact to source/drain regions of an NMOS transistor, TEM section across fins.

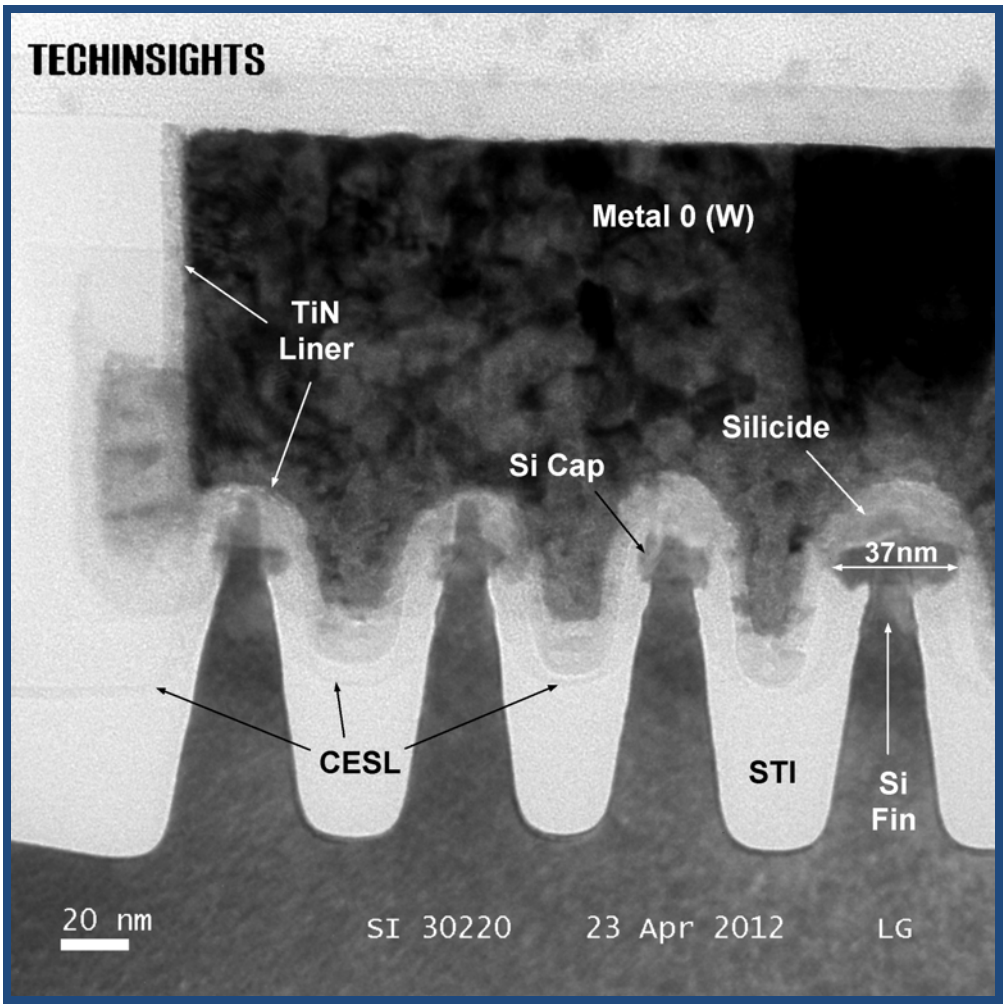


Figure 2.3.3.22: Source/drain silicon caps of NMOS transistor, high magnification TEM cross-section.

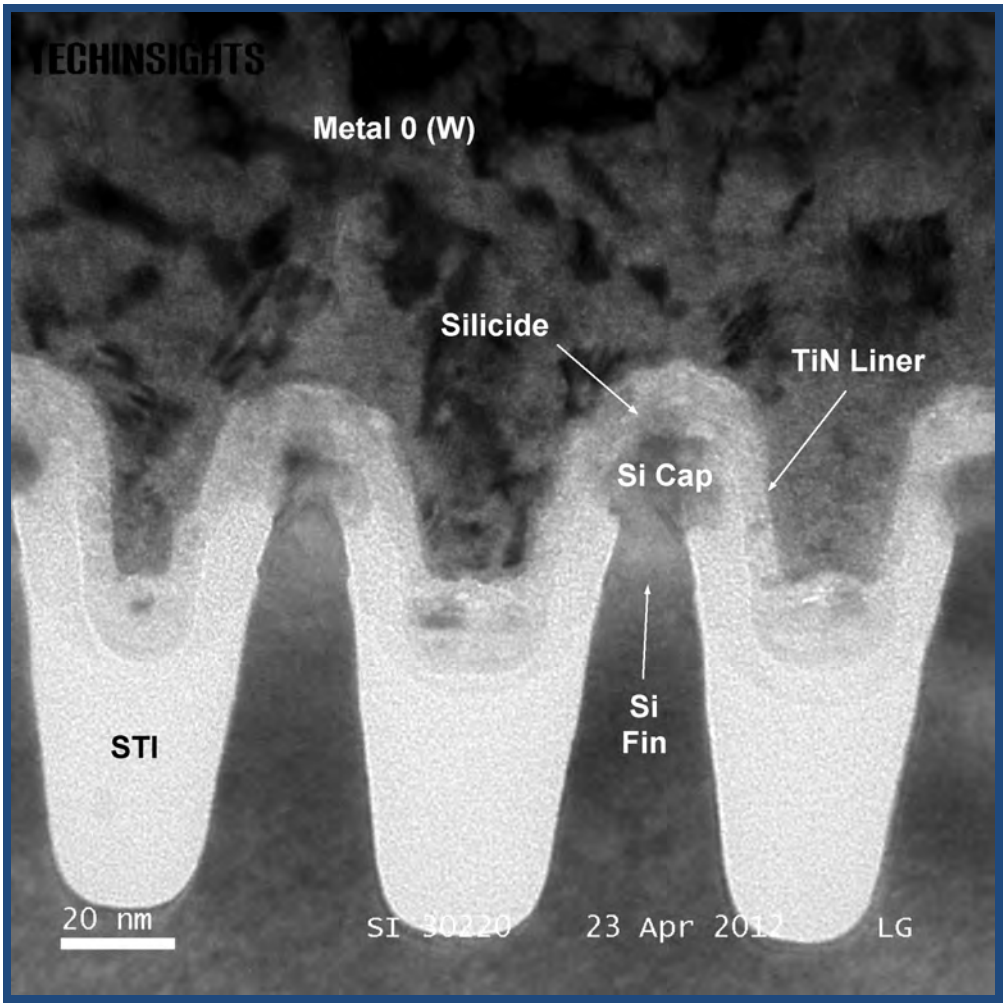


Figure 2.3.3.23: Silicon caps in the source/drain regions of NMOS transistor, high magnification TEM cross-section.

Comments
• Source/drain regions of NMOS transistors have been anisotropically etched to form recess in the NMOS fin; • Embedded Si islands, likely in situ doped with C have been grown by selective epitaxial growth, SEG in the source/drain recesses; embedded Si region standing a few nm above the NMOS fin; • Compared to well “diamond-shaped”embedded SiGe regions, the embedded Si island has a more rounded shape.

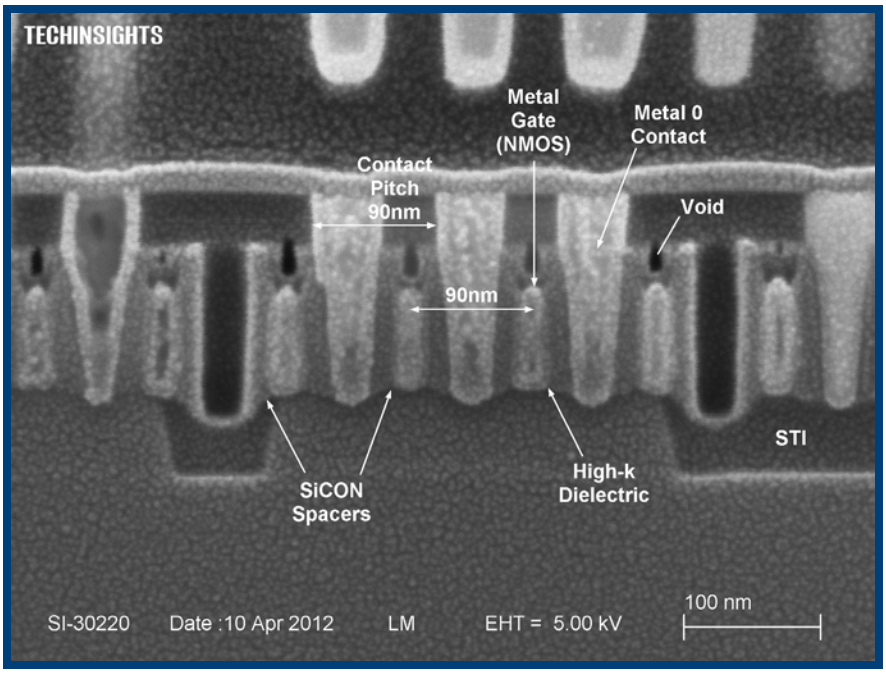


Figure 2.3.3.24: Logic NMOS transistors, SEM cross-section along transistor channel and showing 90 nm contacted gate pitch.

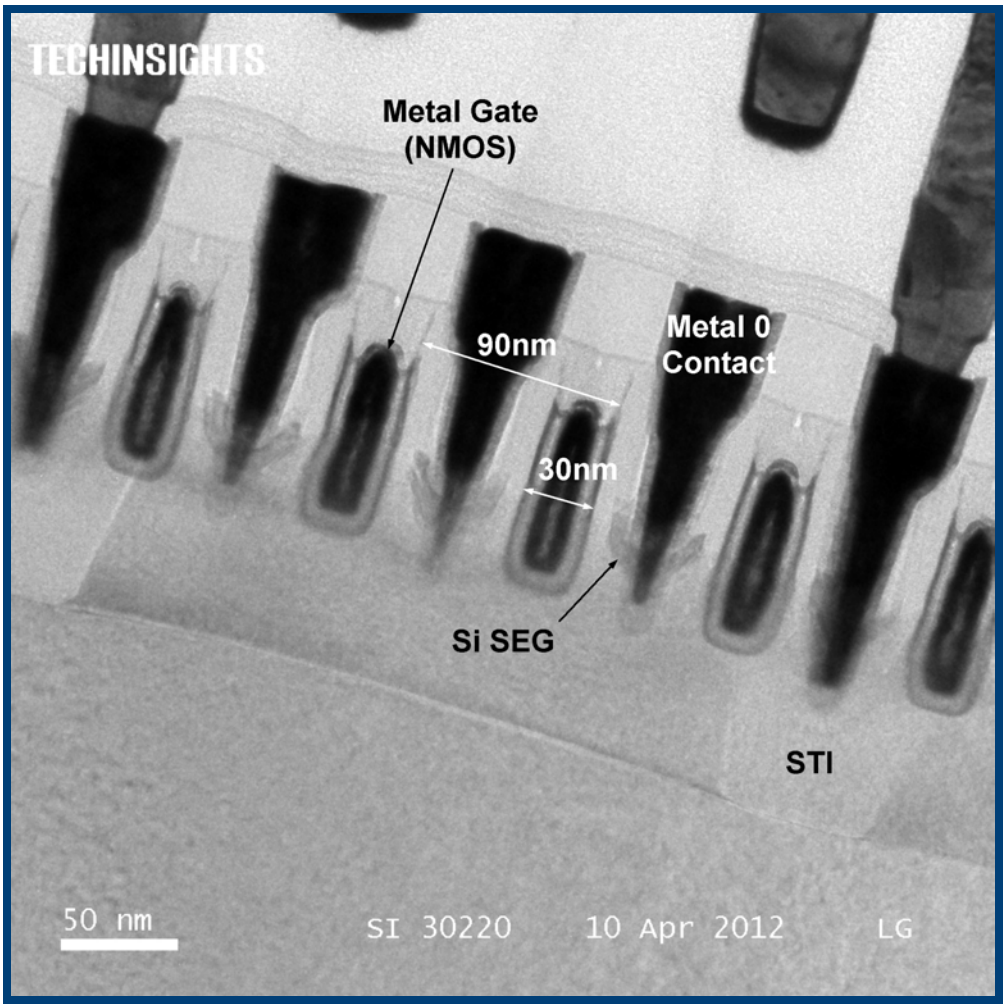


Figure 2.3.3.25: Logic NMOS transistors, TEM cross-section along silicon fin showing 30 nm metal gate length.

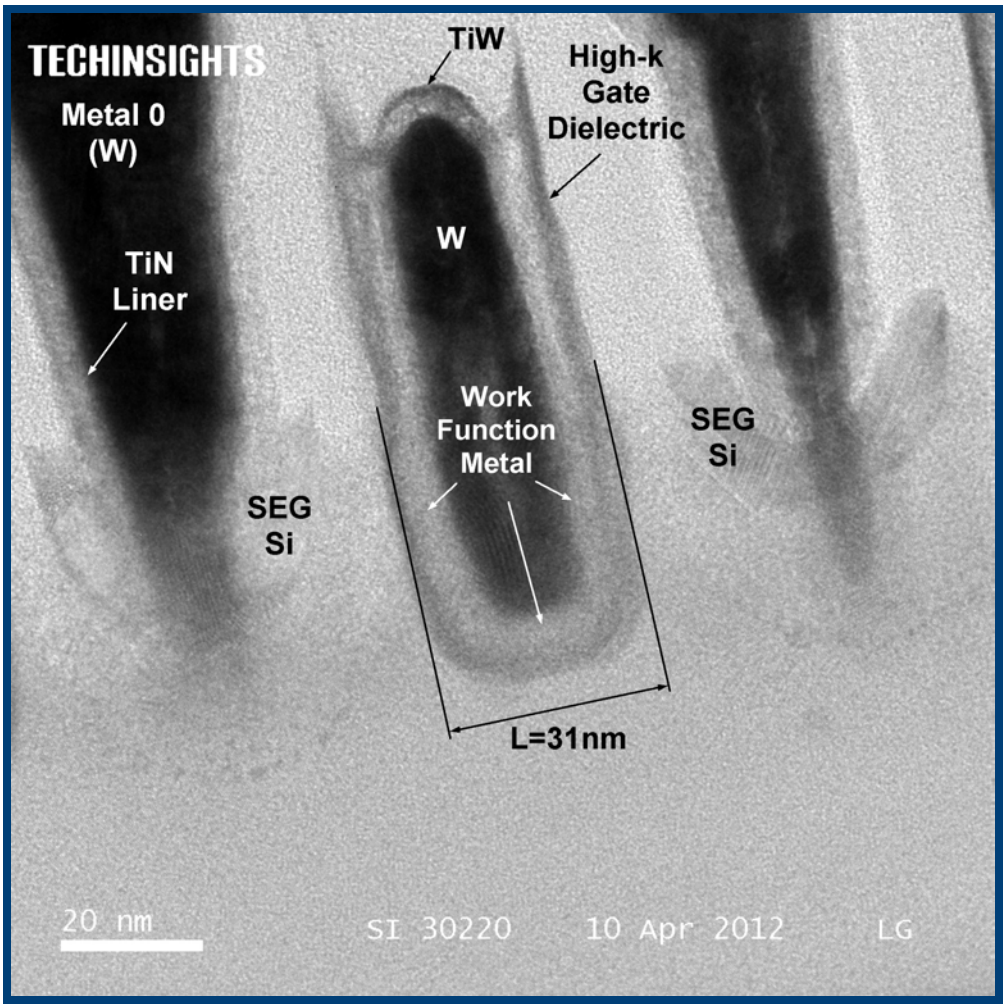


Figure 2.3.3.26: NMOS metal gate with source/drain contacts, high magnification TEM cross-section.

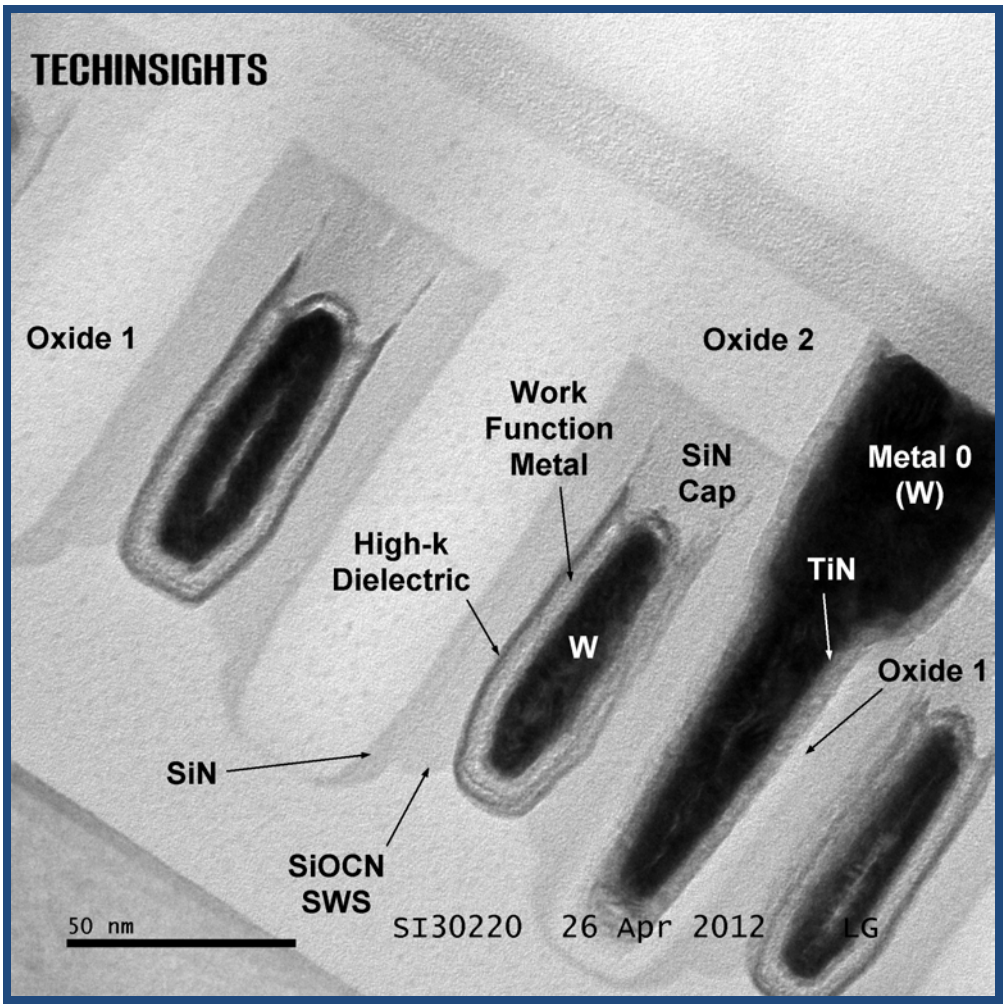


Figure 2.3.3.27: Dummy NMOS metal gate, unfiltered EFTEM image.

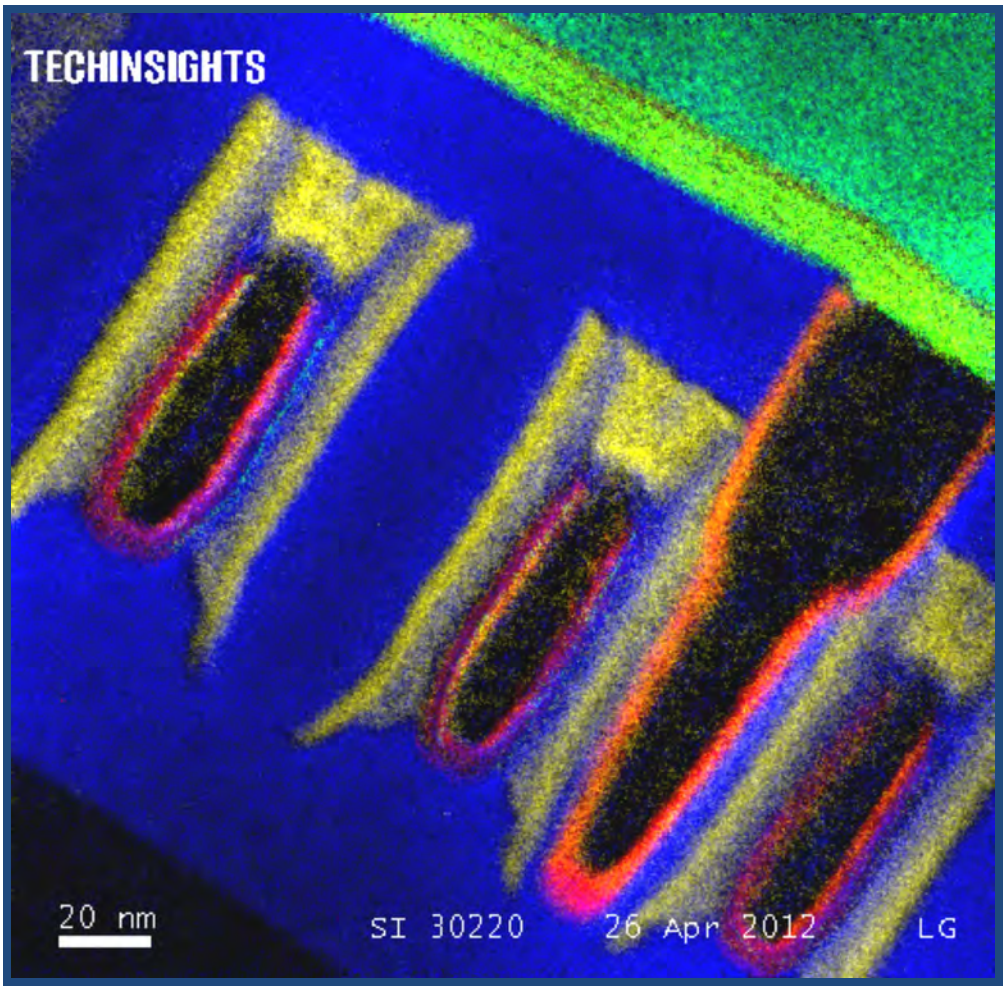


Figure 2.3.3.28: Dummy NMOS metal gate, false color EFTEM image showing Ti (red), N (yellow), (blue), and C (green).

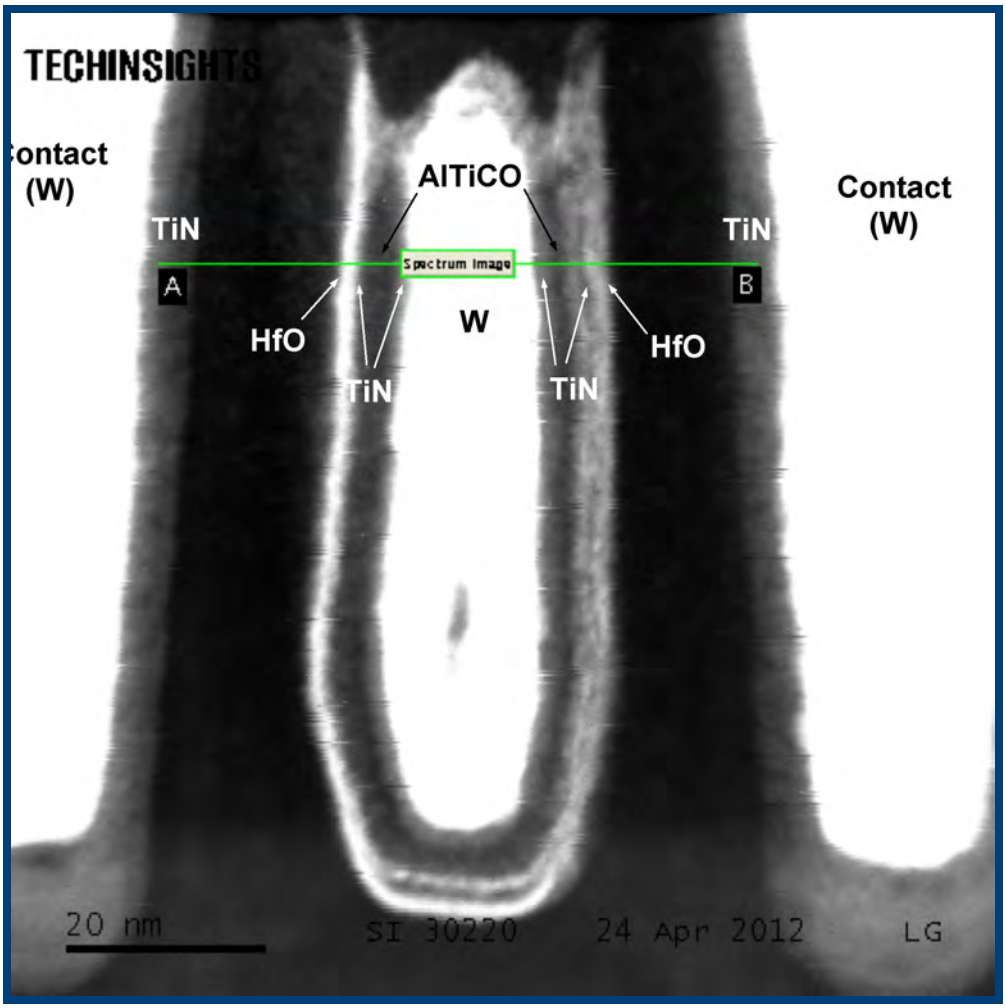


Figure 2.3.3.29: EELS line scan through an NMOS gate between source/drain contacts, HAADF survey image.

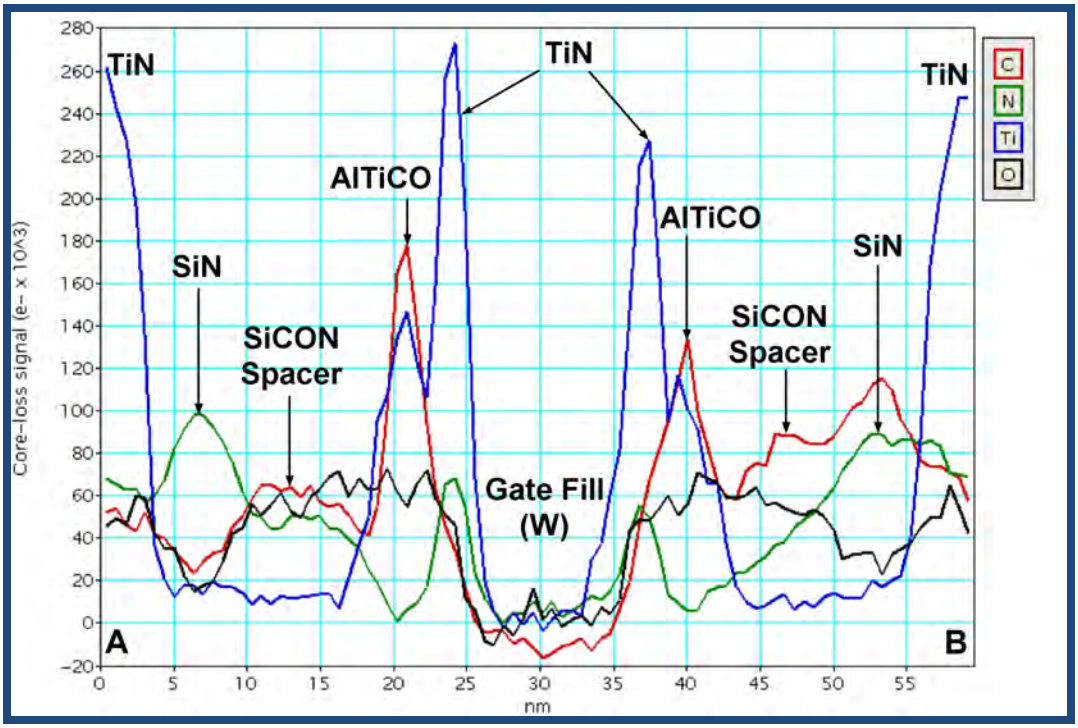


Figure 2.3.3.30: Element profiles of the NMOS gate and dielectric layers, EELS line scan between source/drain contacts.

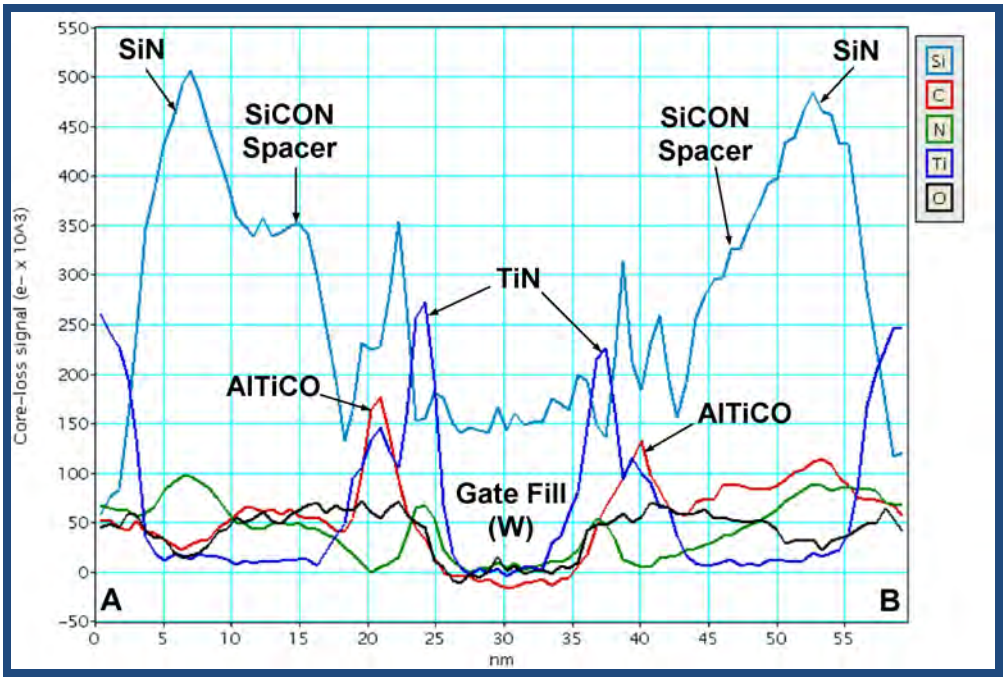


Figure 2.3.3.31: Element profiles (including Si) of the MOS gate and dielectric layers, EELS line scan between source/drain contacts.

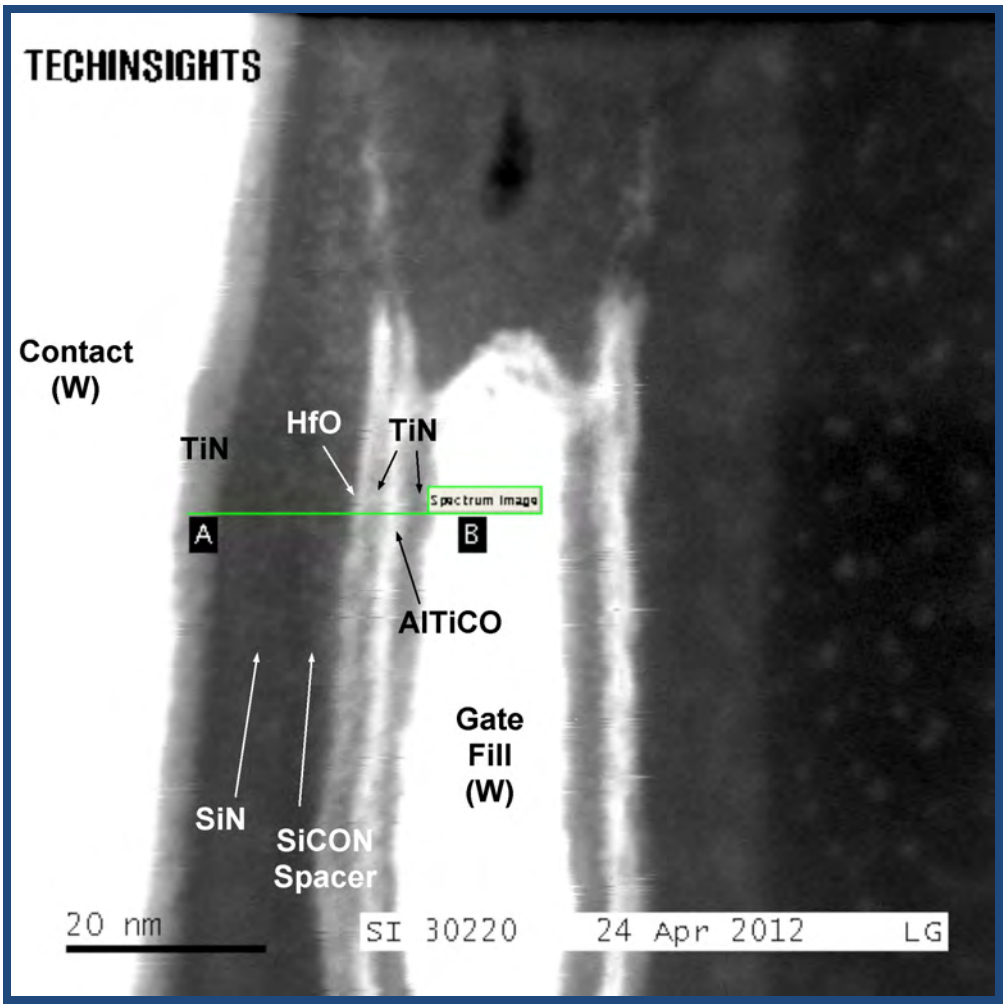


Figure 2.3.3.32: EELS line scan through the NMOS gate left side, HAADF survey image.

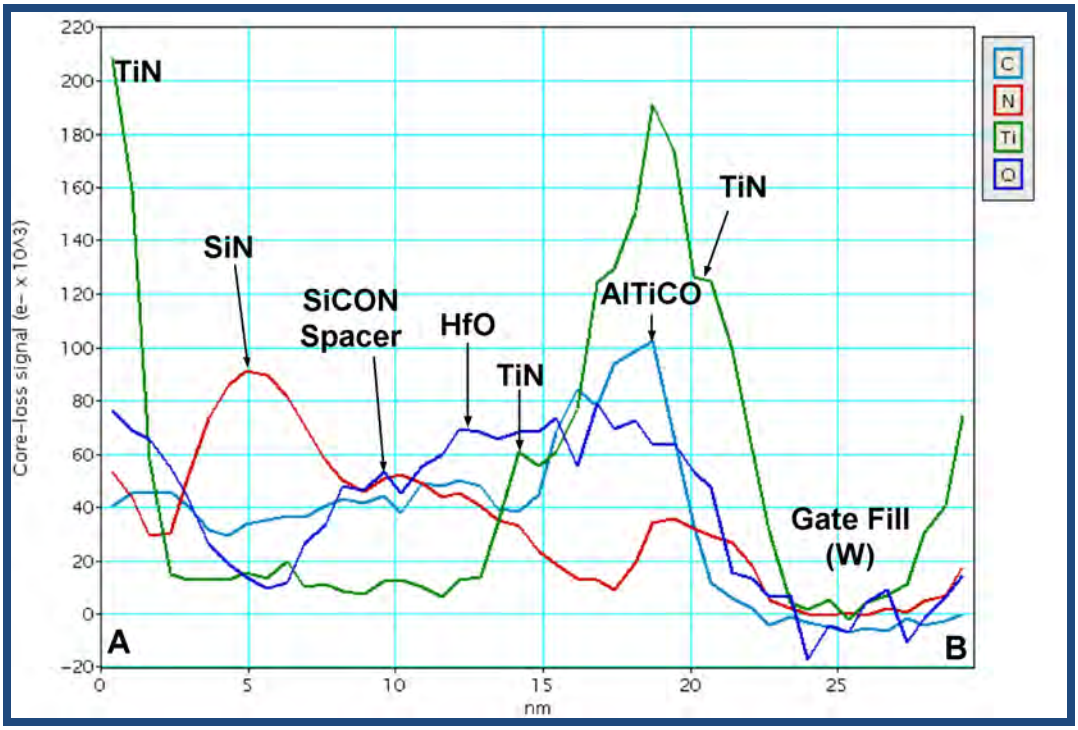


Figure 2.3.3.33: Element profiles of the NMOS gate and dielectric layers, EELS line scan.

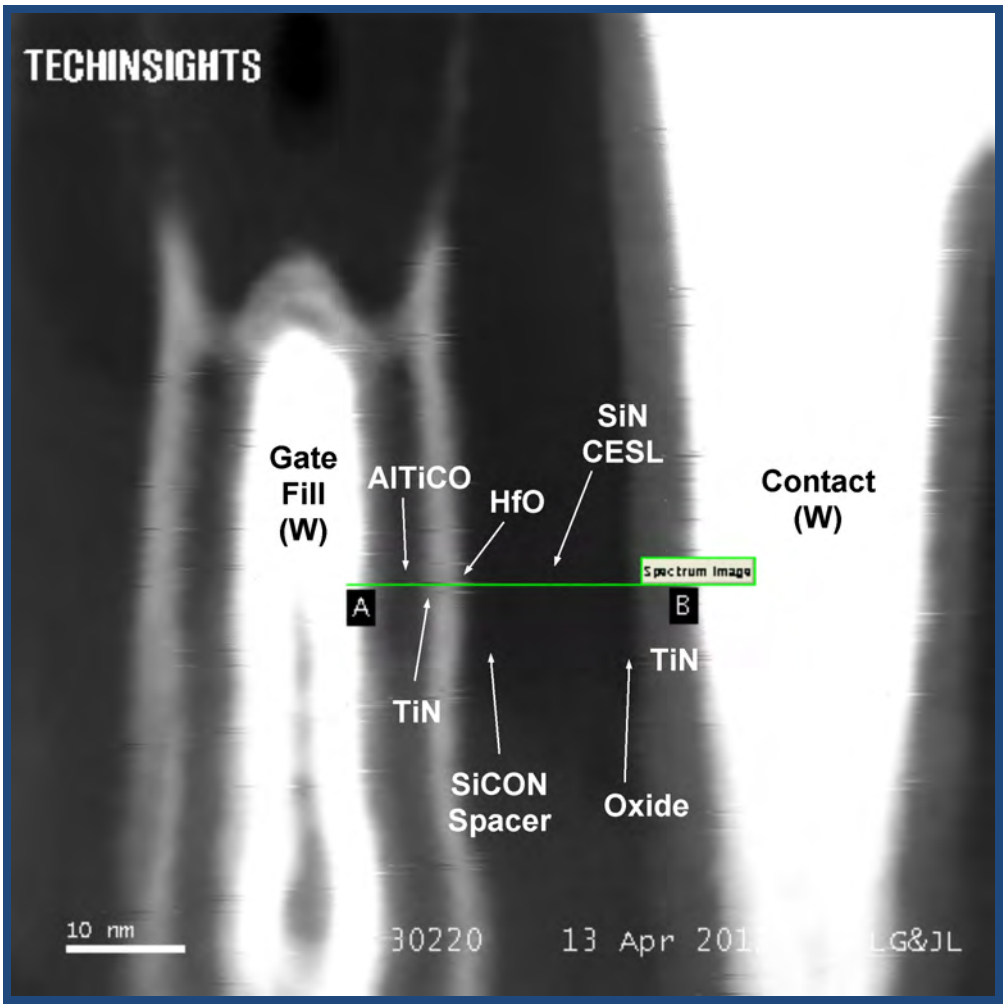


Figure 2.3.3.34: EELS horizontal line scan through an NMOS gate, spacer and contact, HAADF survey image.

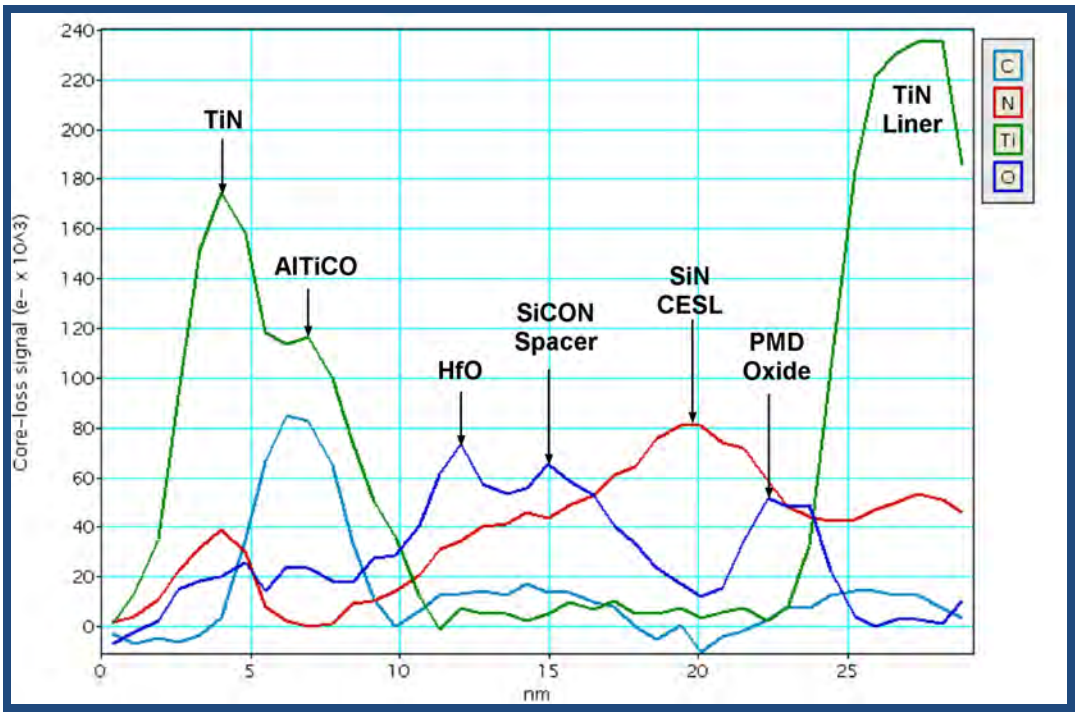


Figure 2.3.3.35: Element profiles of the NMOS gate, high-k gate dielectric, spacer and contact EELS line scan.

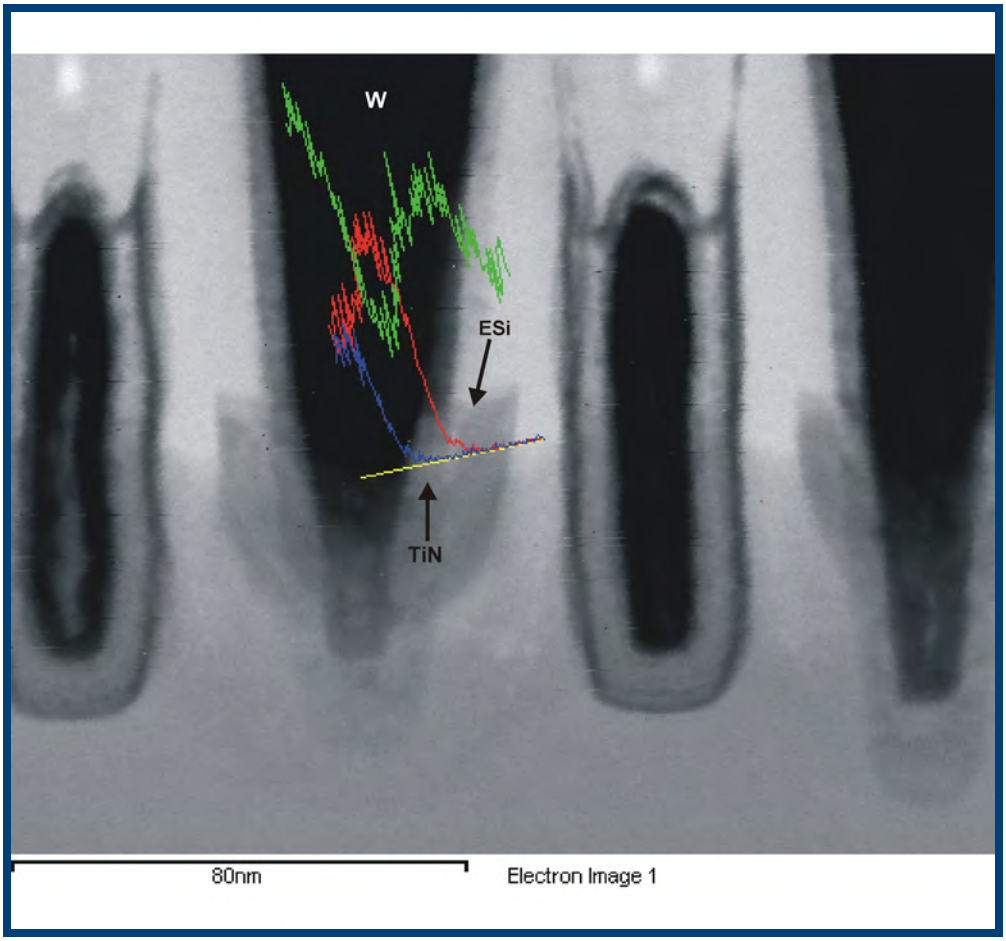


Figure 2.3.3.36: TEM EDS line scan through source/drain region of NMOS transistor, with element profiles overlaid.

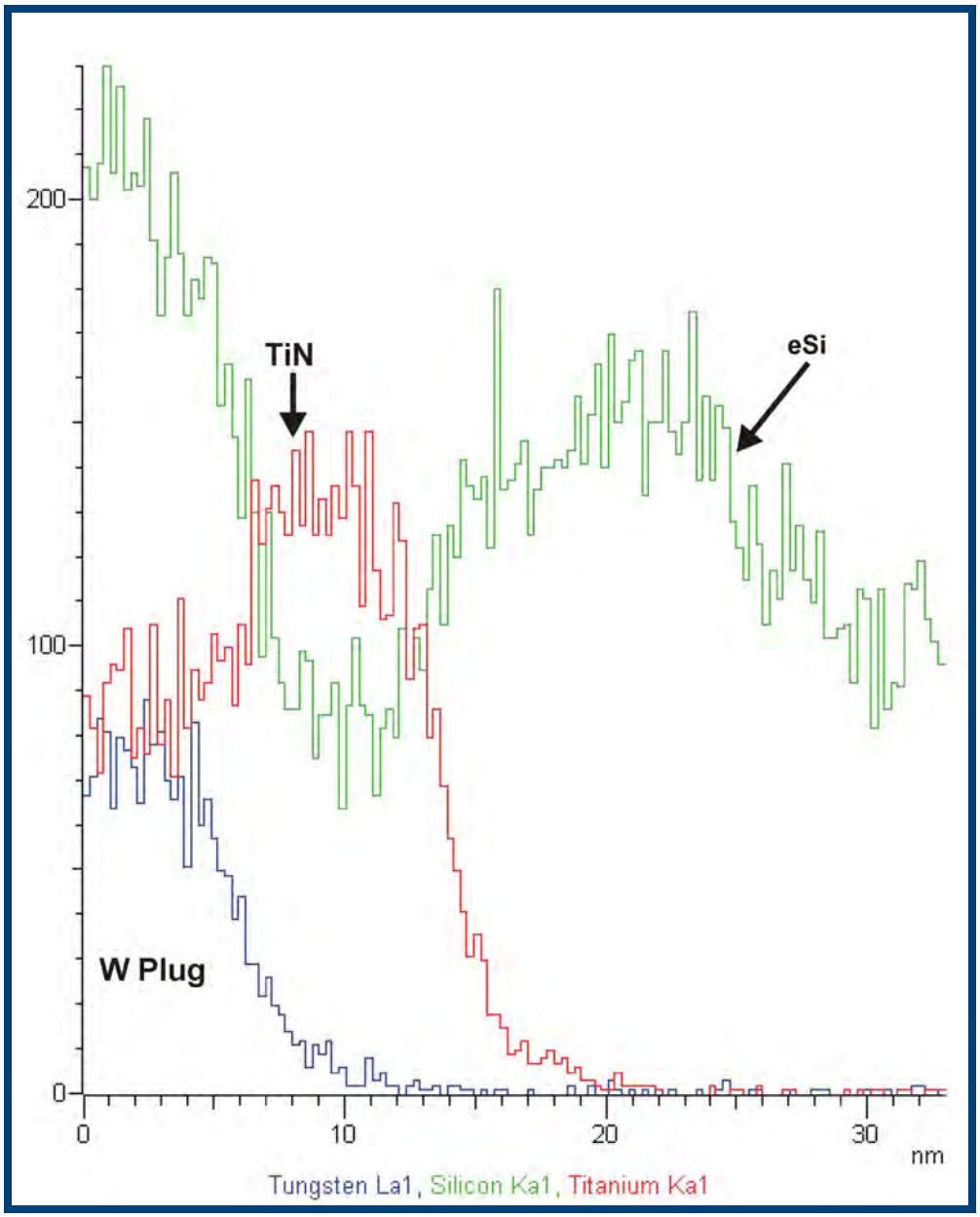


Figure 2.3.3.37: Element profiles through the NMOS source/drain contact region, TEM EDS line scan.

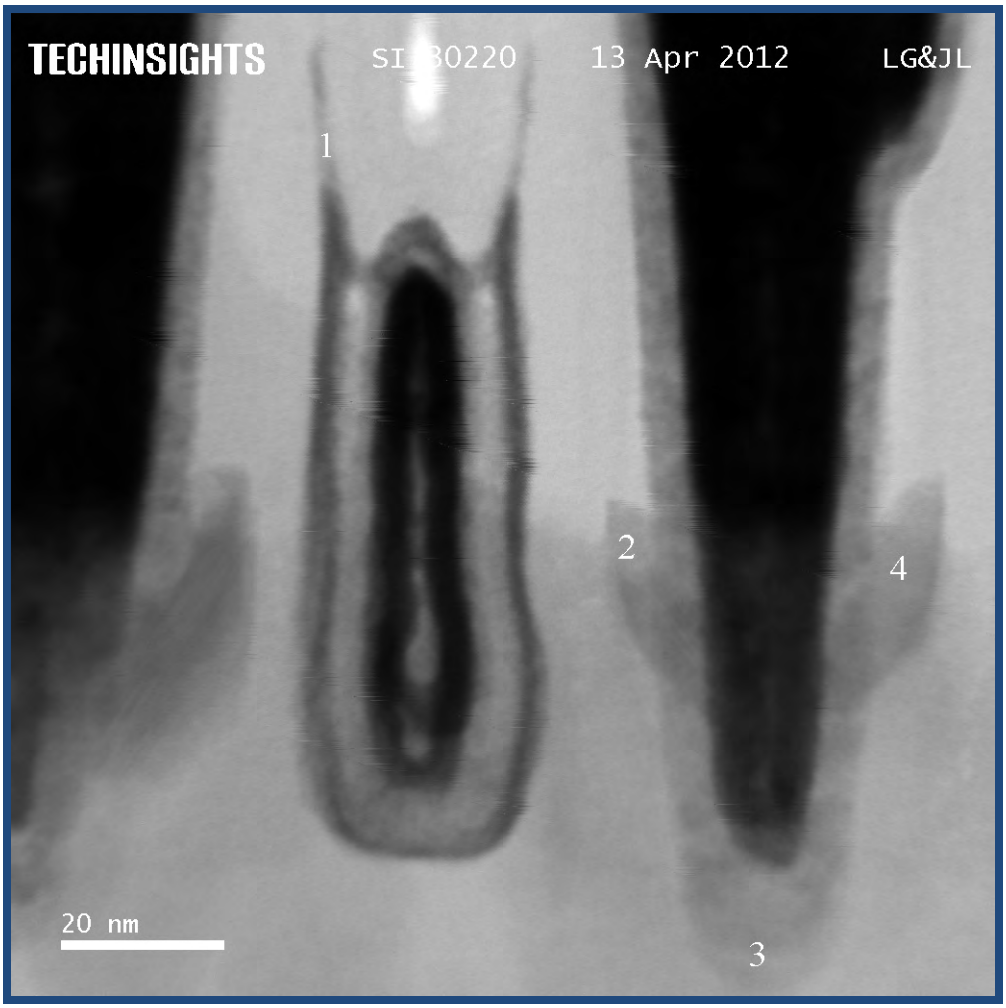


Figure 2.3.3.38: Source/drain region of NMOS transistor with TEM EDS sites annotated.

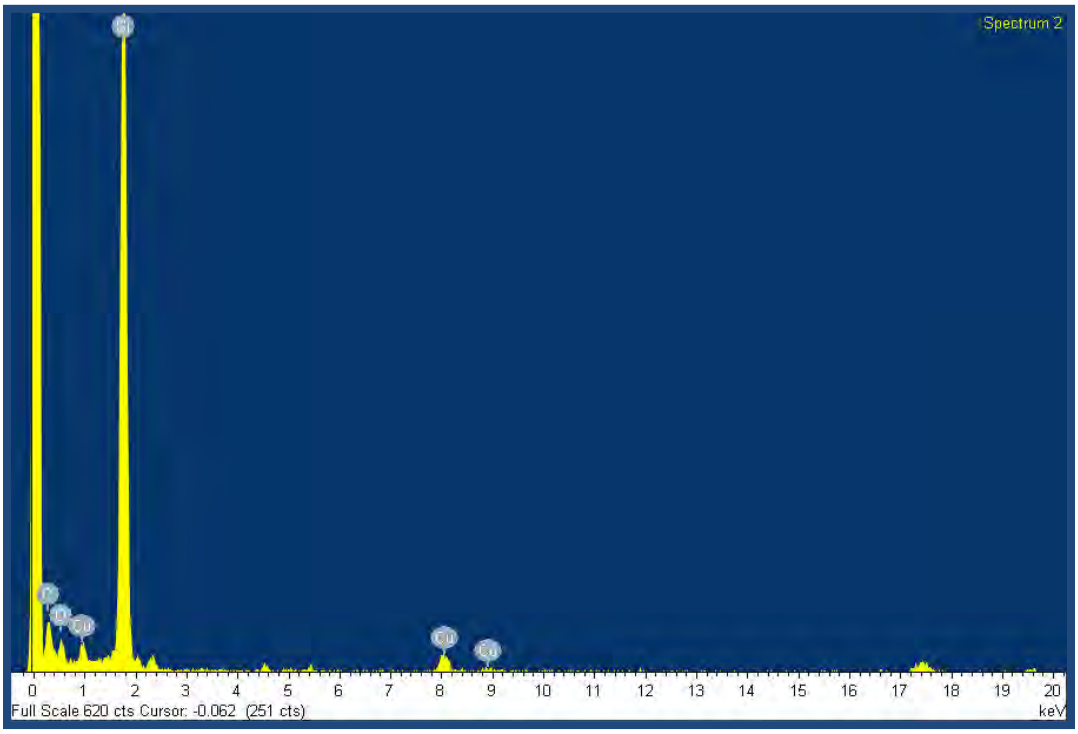


Figure 2.3.3.39: TEM EDS spectrum of source/drain silicon cap, site 2.

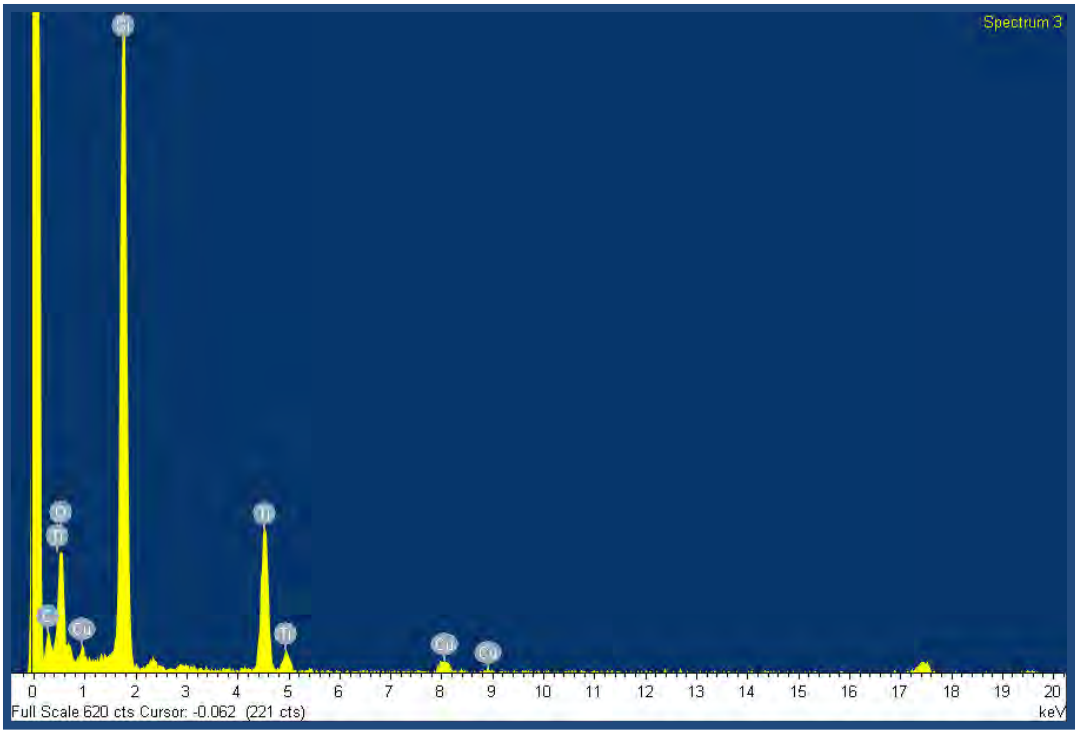


Figure 2.3.3.40: TEM EDS spectrum of TiN source/drain contact tip, site 3.

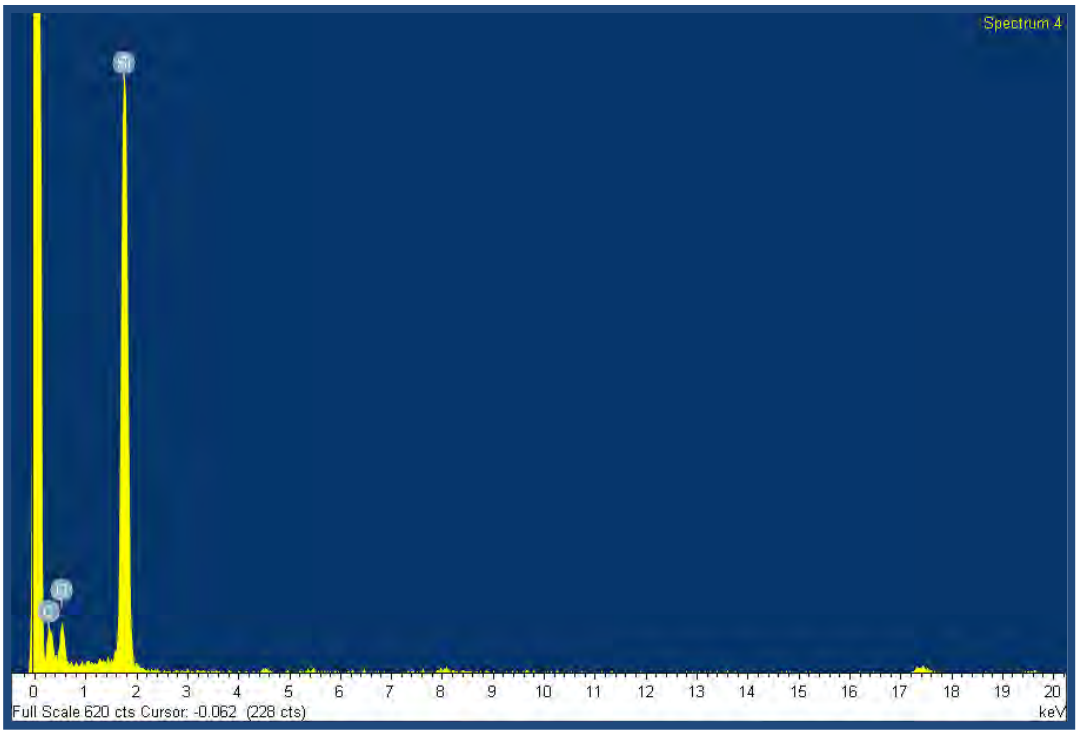


Figure 2.3.3.41: TEM EDS spectrum of source/drain silicon cap, site 4.

Comments
• A thin TiSi layer may have been formed at the interface between the eSi:C region and a thin Ti adhesion layer on the outer surface of the TiN liner of metal 0 contact.

Comments

- Tri-Gate transistors with silicon fin, replacement dual work function metal gate and high-k gate dielectric have been used;
- Main process steps of Tri-Gate transistor gates formation;
  - Grow a thin silicon oxide layer on silicon fins;
  - Deposit sacrificial poly gate layer, pattern and etch. A double patterning with immersion lithography was likely used to achieve the 30 nm transistor gate lengths;
  - Deposit SiOCN layer and etch back to form low-k sidewall spacers, SWS likely by a combination of dry and wet processes;
  - Likely ion implantations for source/drain extensions (PMOS and NMOS);
  - Deposit an oxide layer and CMP to planarize the surface;
  - Open NMOS source/drain regions, etch a recess and grow embedded N-type doped Si:C regions by selective epitaxial growth, SEG to provide tensile strain to NMOS channel;
  - Protect NMOS and open PMOS source/drain regions, etch a recess and grow embedded P-type doped SiGe regions to provide compressive strain to PMOS channel;
  - Deposit a SiN etch-stop layer, oxide 1 layer and CMP to planarize surface and expose sacrificial poly gates;
  - Remove sacrificial poly gates from both PMOS and NMOS transistors;
  - Grow thin silicon oxide layer on silicon fins of both PMOS and NMOS transistors;
  - Deposit hafnium oxide layer likely by atomic layer deposition (ALD) for both PMOS and NMOS gates;
  - Deposit TiN barrier layer to protect hafnium oxide during metal gate processing for both PMOS and NMOS gates;
  - Deposit thin TaAl barrier layer likely by ALD for both PMOS and NMOS gates;
  - Deposit the PMOS work function metal layers TiN/AlCO/TiAlN for both PMOS and NMOS gates;
  - Deposit W to fill both PMOS and NMOS gates;
  - CMP to remove the excess gate layers;
  - Protect PMOS areas and remove the PMOS gate fill and work function metals from NMOS gates ;
  - Deposit the NMOS work function metal layers AlTiCO/TiN;
  - Deposit W to fill NMOS gates;
  - CMP to remove the excess gate layers;
  - Etch back the gate layers to form recess over the PMOS and NMOS gates;
  - Deposit a TiW cap layer;
  - Deposit an oxy-nitride and nitride cap layers likely by low temperature CVD to remain in the thermal budget of high-k dielectric and metal gate;
  - CMP planarization.

2.3.4 Topographical and Cross-Sectional Analysis of Input/Output Transistors

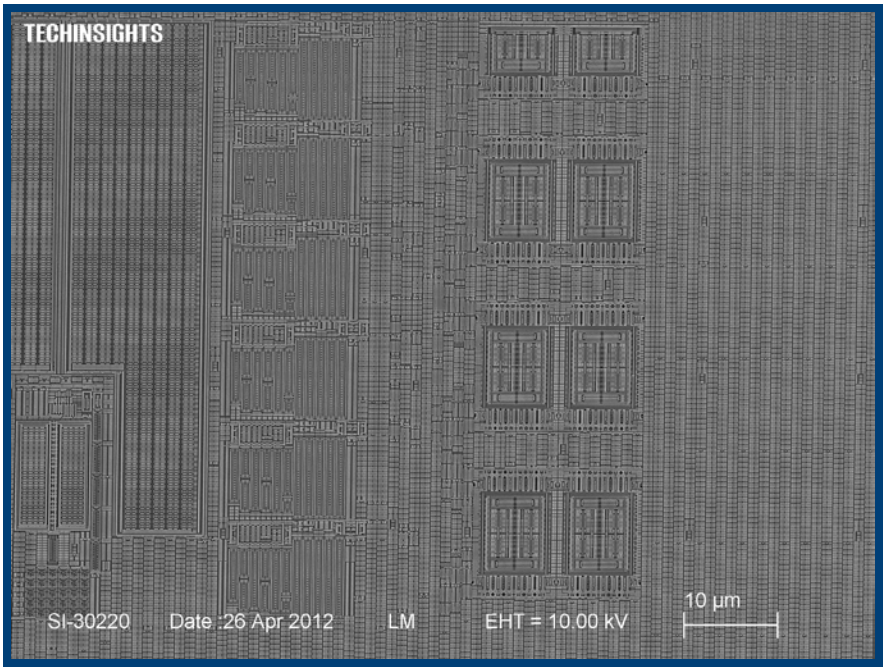


Figure 2.3.4.1: Input/output transistors at metal 0/metal gate level, low magnification SEM topographical image.

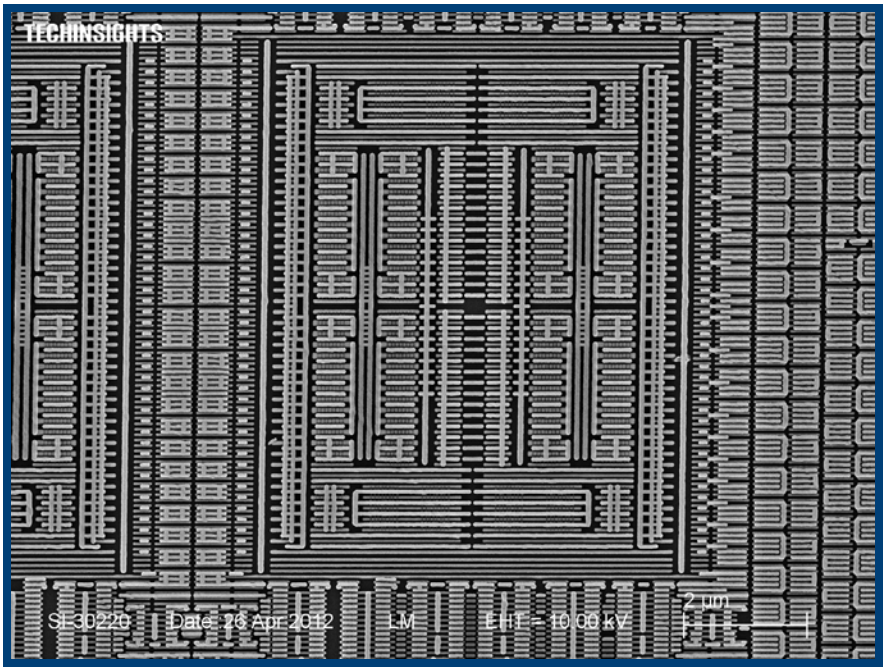


Figure 2.3.4.2: Input/output transistor at metal 0/metal gate level, SEM topographical image.

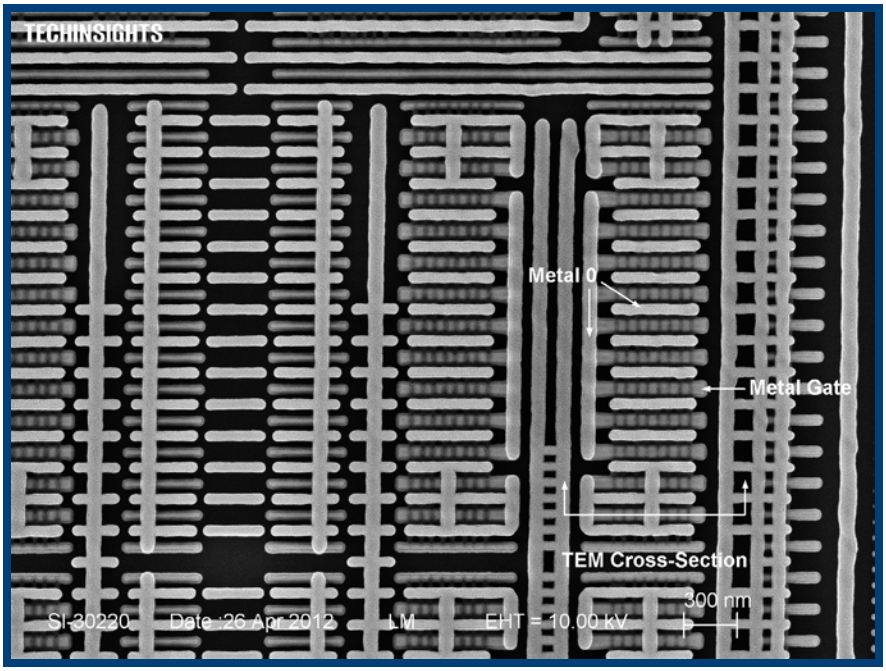


Figure 2.3.4.3: Input/output transistor with the location of TEM cross-section annotated, high magnification SEM topographical image.

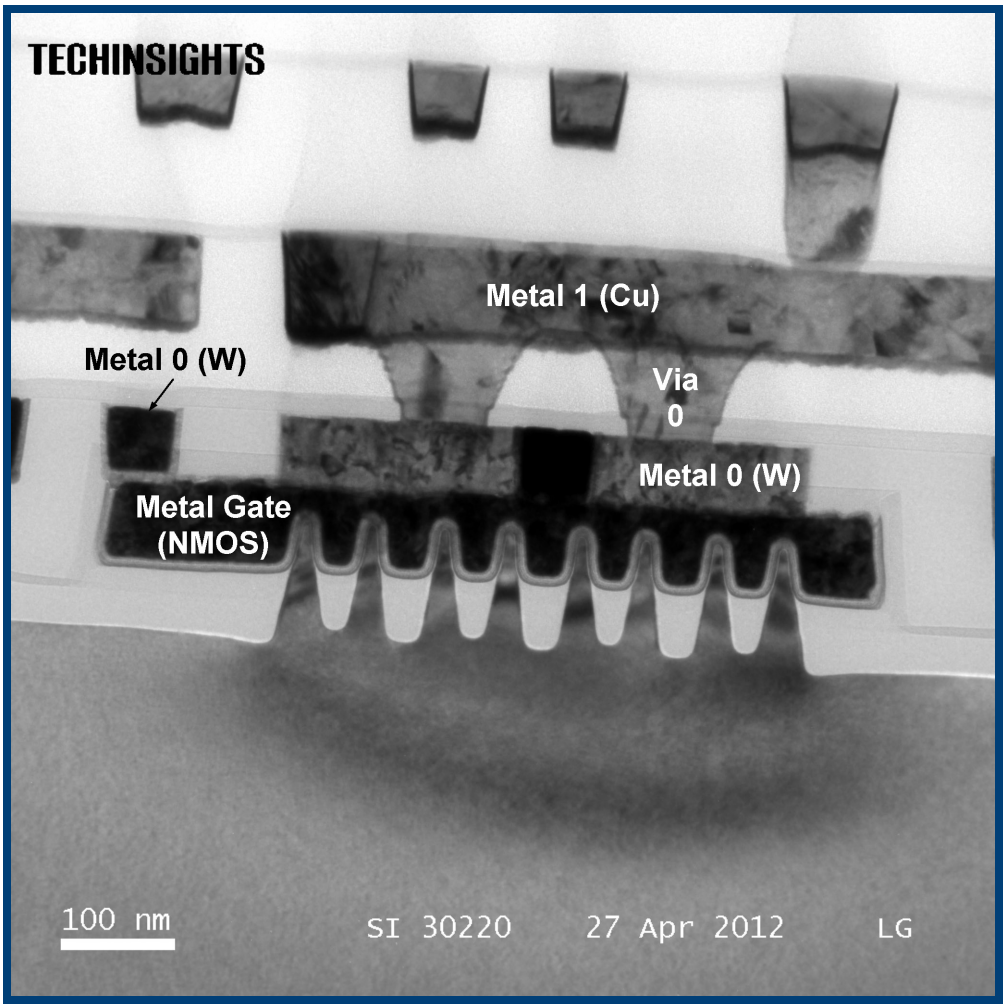


Figure 2.3.4.4: Input/output NMOS transistor, low magnification TEM cross-section along the gate.

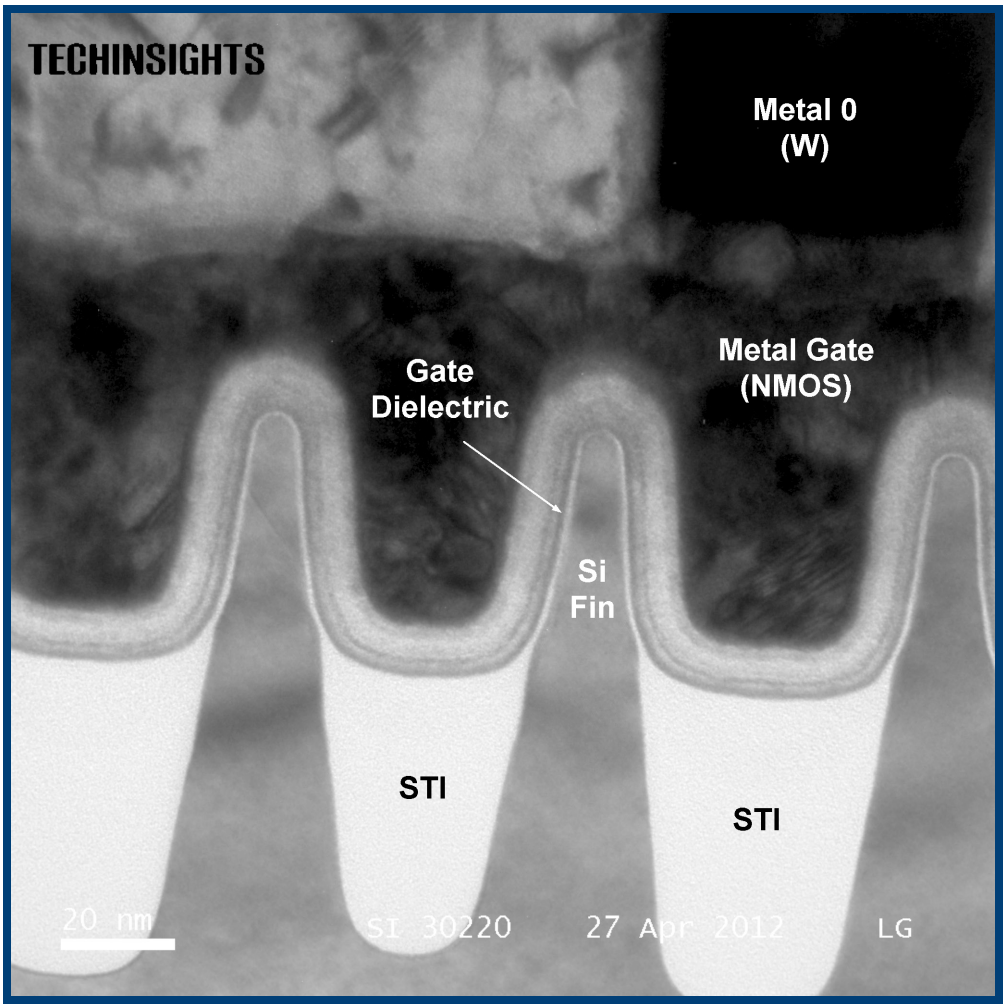


Figure 2.3.4.5: I/O NMOS transistor, TEM cross-section along the gate.

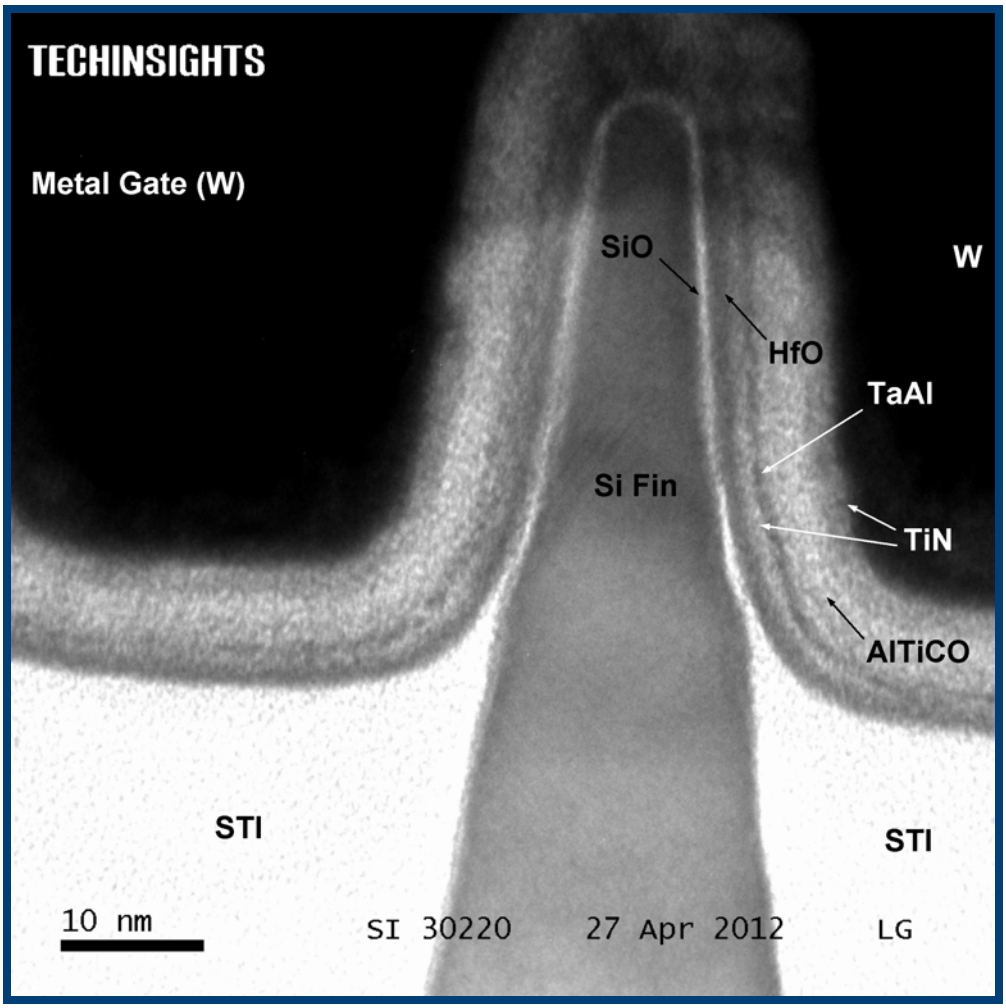


Figure 2.3.4.6: Gate dielectric and metal gate layers of the I/O NMOS transistor, high magnification TEM cross-section.

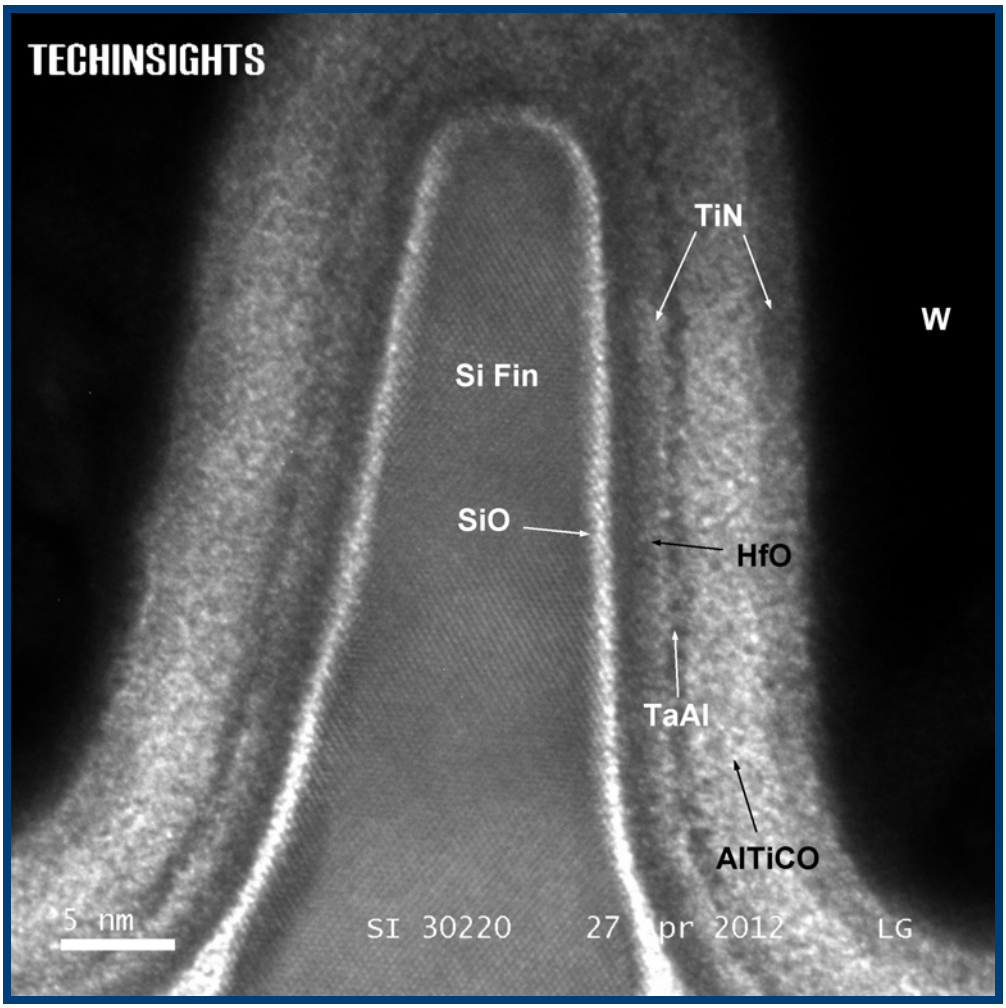


Figure 2.3.4.7: Gate dielectric of the I/O NMOS transistor, HRTEM image.

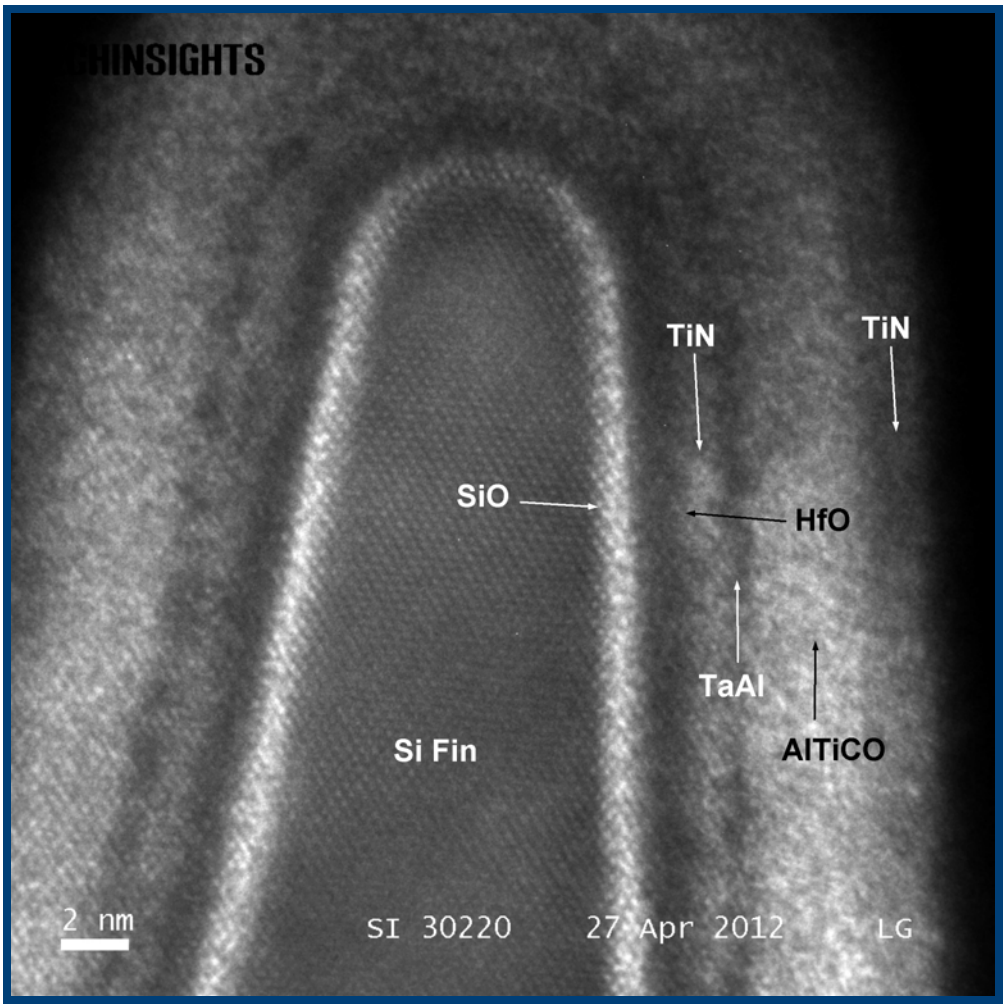


Figure 2.3.4.8: I/O gate dielectric of NMOS transistor, HRTEM image.

Feature	Dimension	Unit
I/O transistor gate pitch	180	nm
I/O transistor contact pitch	180	nm
I/O transistor fin pitch	60	nm
I/O NMOS gate dielectric thickness	2.6	nm
SiO thickness	0.7	nm
HfO thickness	1.9	
I/O NMOS gate stack thickness	13.5	nm
TiN layer above HfO	1	nm
TaAl barrier	1	nm
AlTiCO work function metal	2.9	nm
TiN layer	2.6	nm
W gate fill	6	nm

Comments

- I/O transistors have the structure similar to logic Tri-Gate transistors, with silicon fin, replacement metal gate and high-k gate dielectric of the same critical dimensions;
- I/O NMOS transistors use the same metal gate stack and same HfO and SiO layers as the NMOS logic transistors;
- I/O NMOS transistor has metal gate and metal 0 contact pitch two times larger than those of logic NMOS transistor;
  - I/O metal gate pitch of 180 nm;
  - I/O metal 0 contact pitch of 180 nm.

2.4 Pre-Metal Dielectric (PMD) and Contacts

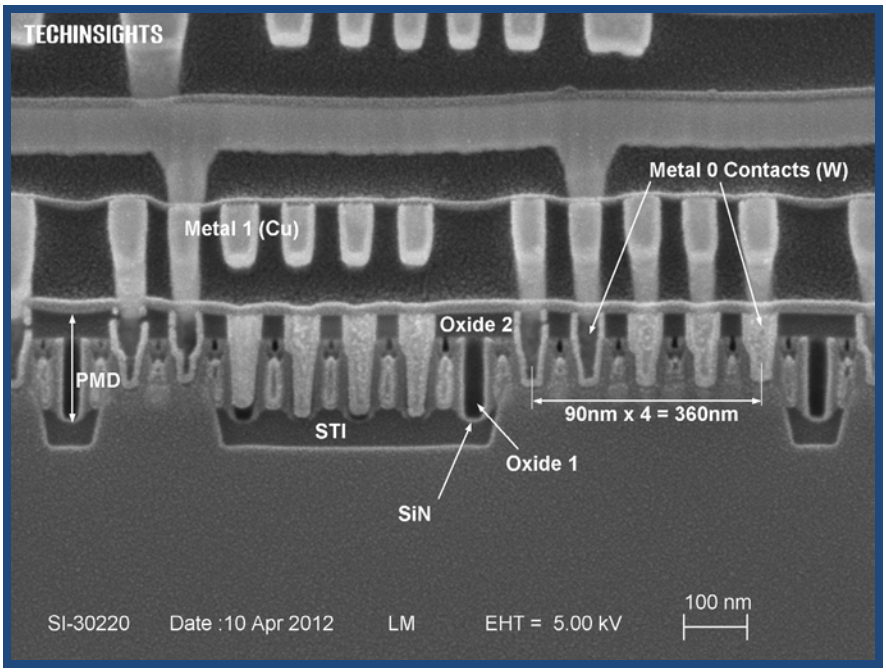


Figure 2.4.1: PMD over PMOS transistors, SEM cross-section.

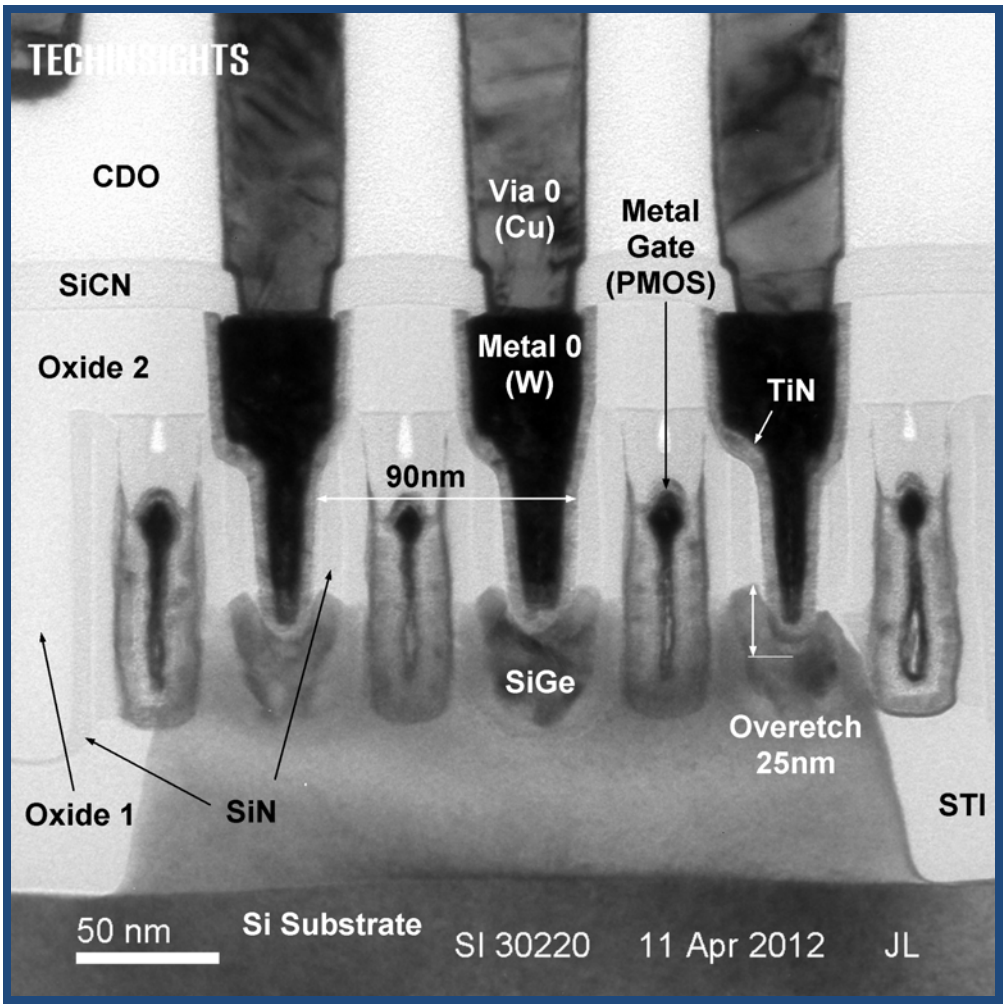


Figure 2.4.2: PMD layers and contacts of PMOS transistors, TEM cross-section.

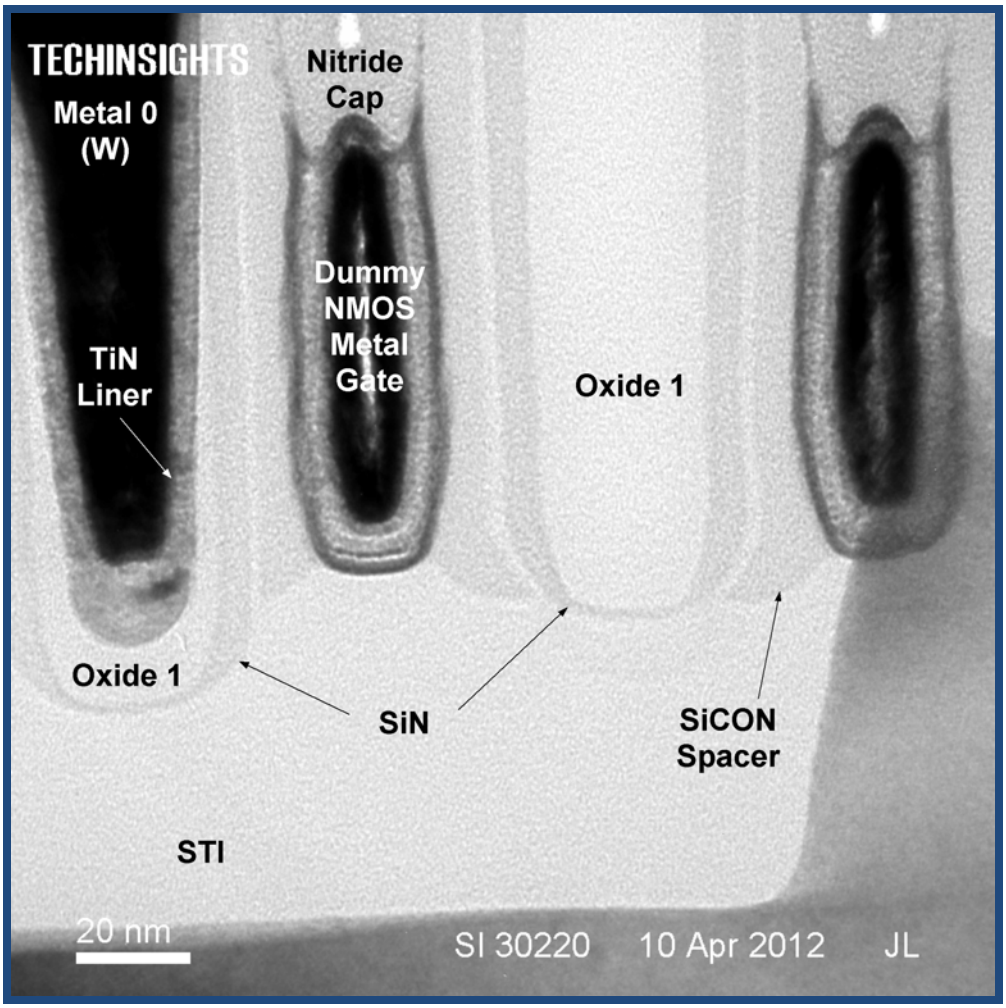


Figure 2.4.3: PMD layers and a source/drain contact to STI, high magnification TEM cross-section.

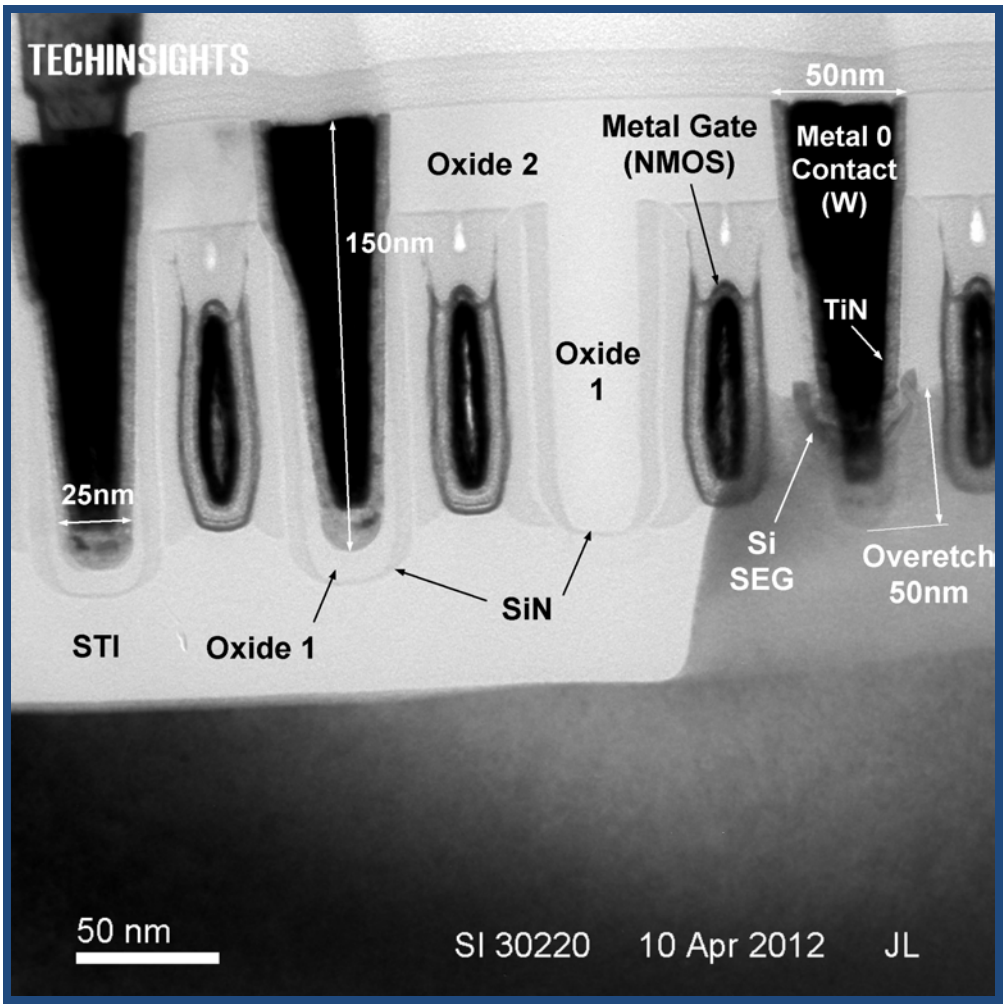


Figure 2.4.4: Bottom PMD layers and bottom part of metal 0 contact on STI, high magnification TEM cross-section.

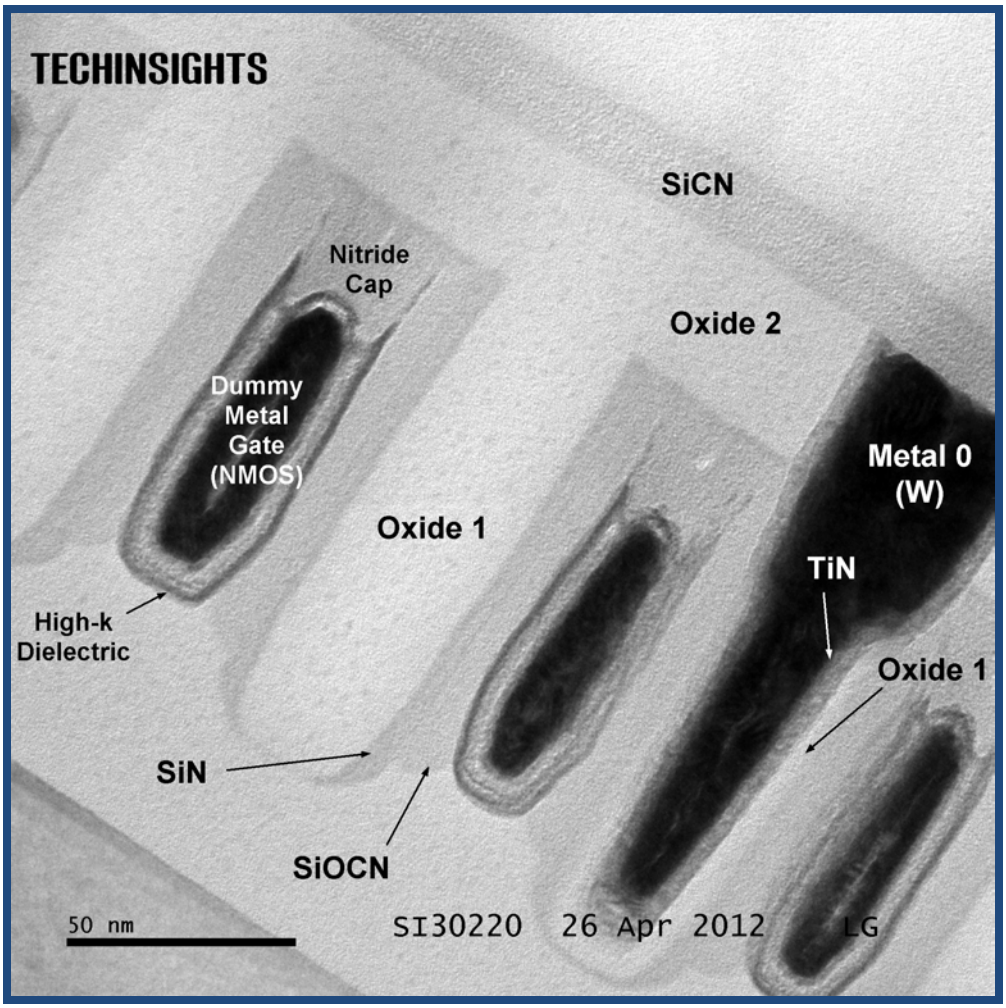


Figure 2.4.5: PMD layers, unfiltered EFTEM image.

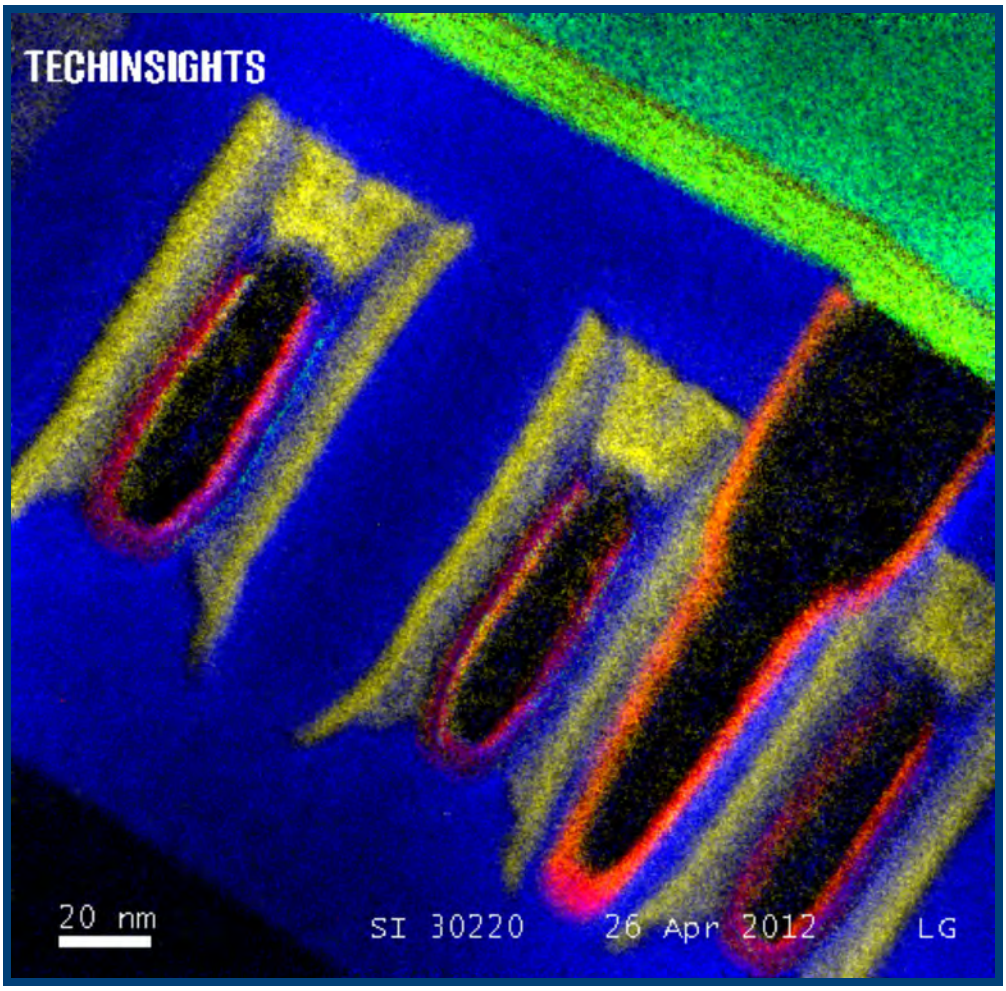


Figure 2.4.6: PMD layers in the vicinity of NMOS metal gate, false color EFTEM image showing Ti (red), N (yellow), O (blue), and C (green).

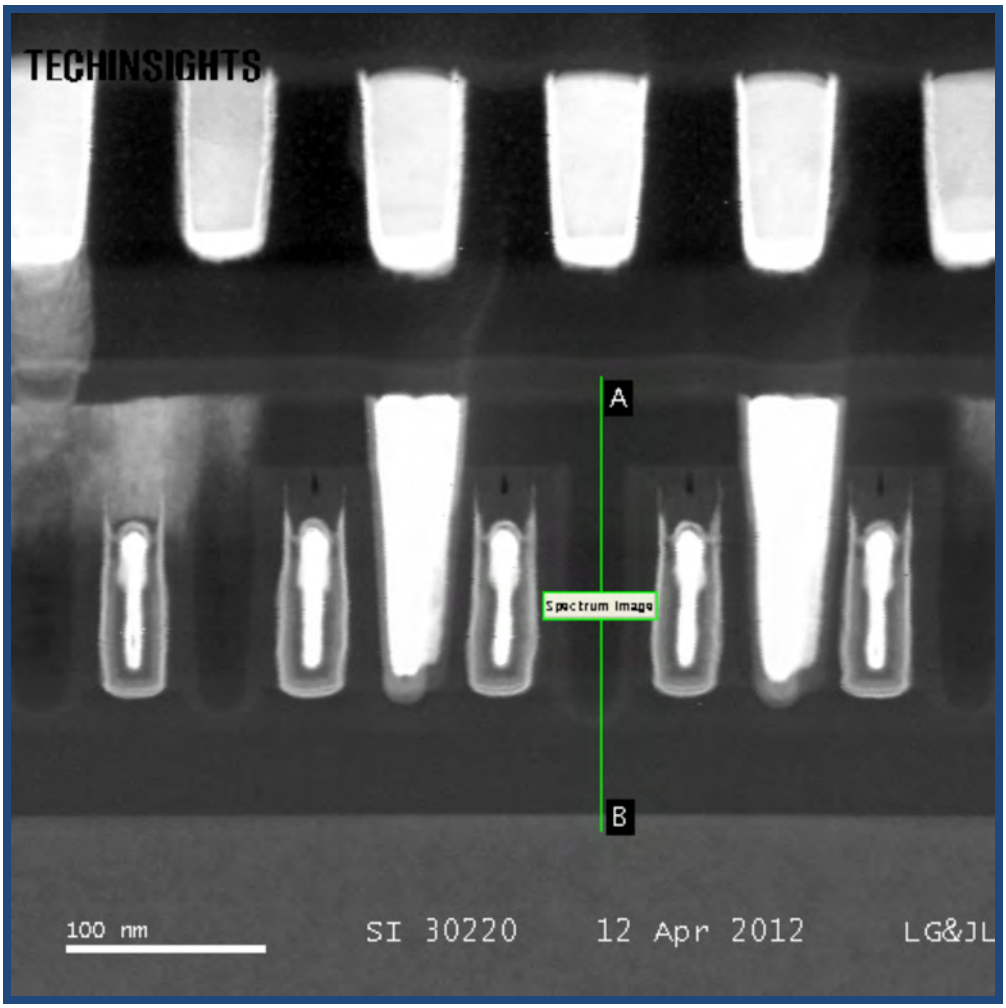


Figure 2.4.7: EELS vertical line scan through the PMD layers and STI, HAADF survey image.

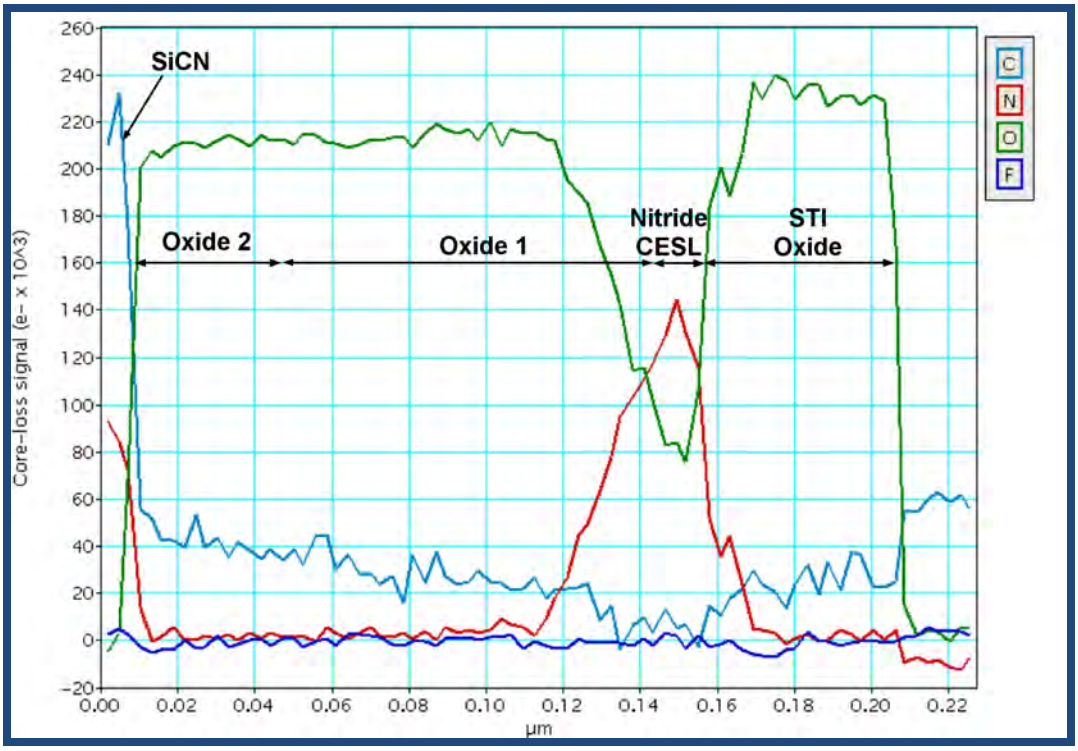


Figure 2.4.8: Element profiles of the lower PMD layers and STI, EELS vertical line scan.

Feature	Dimension	Unit
PMD maximum thickness	160	nm
SiN contact etch-stop layer, CESL	8	nm
Oxide 1 (CMP planarized)	115	nm
Oxide 2	37	nm

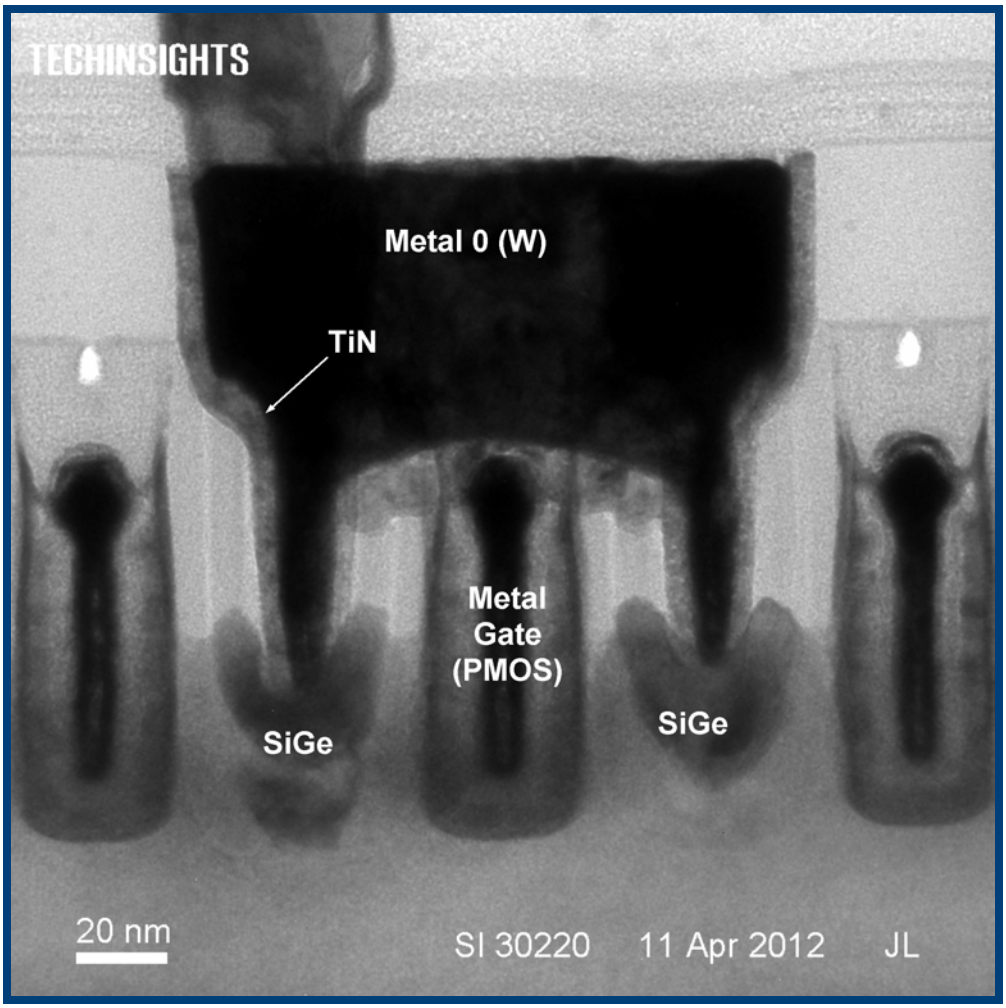


Figure 2.4.9: Contact to PMOS metal gate and to SiGe regions, TEM cross-section across the gate.

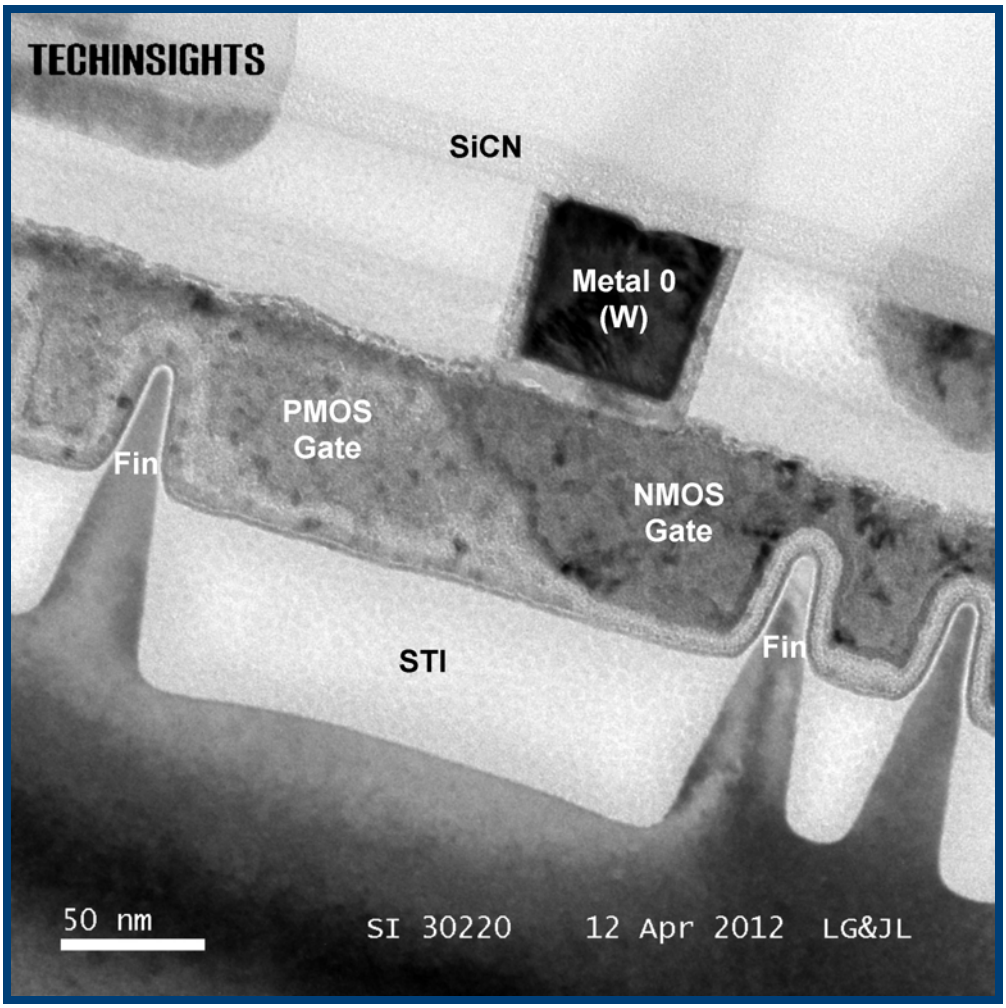


Figure 2.4.10: Contact to common metal gate of NMOS and PMOS transistors, TEM cross-section along the gate.

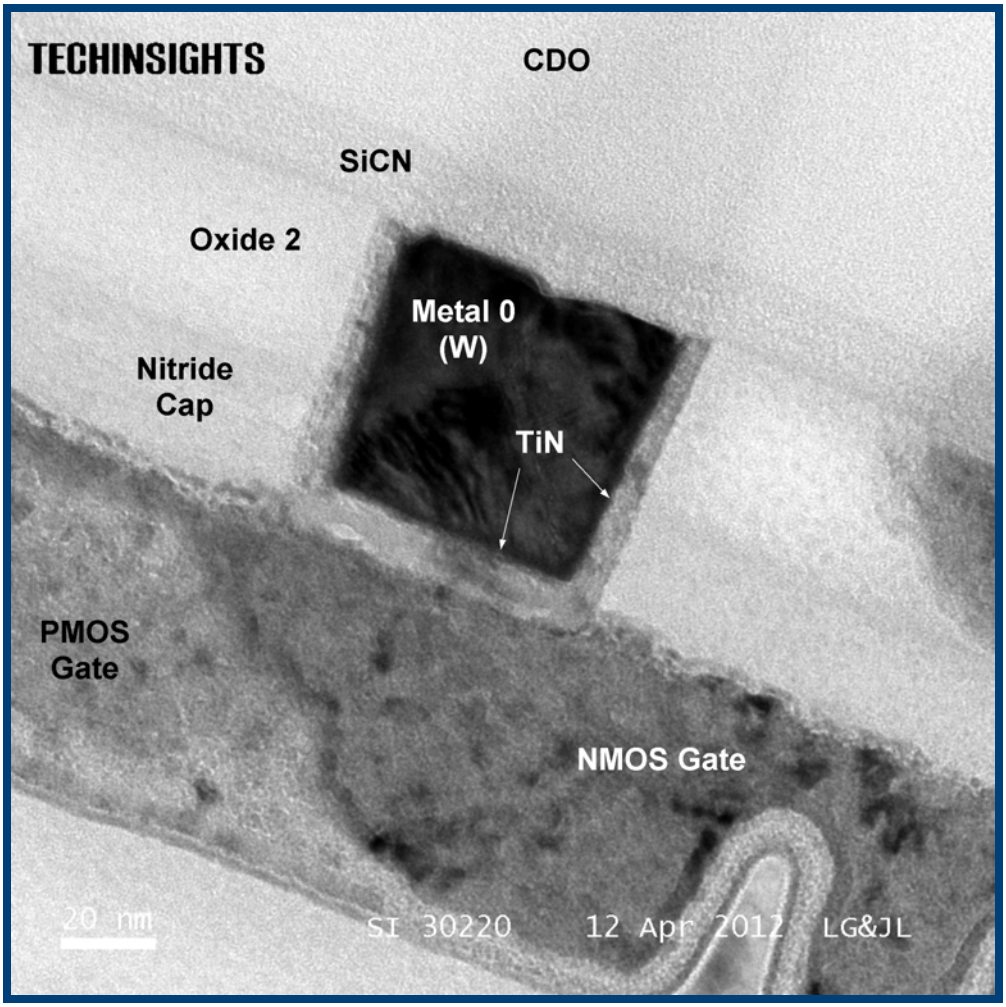


Figure 2.4.11: Contact to common metal gate, high magnification TEM cross-section along the gate.

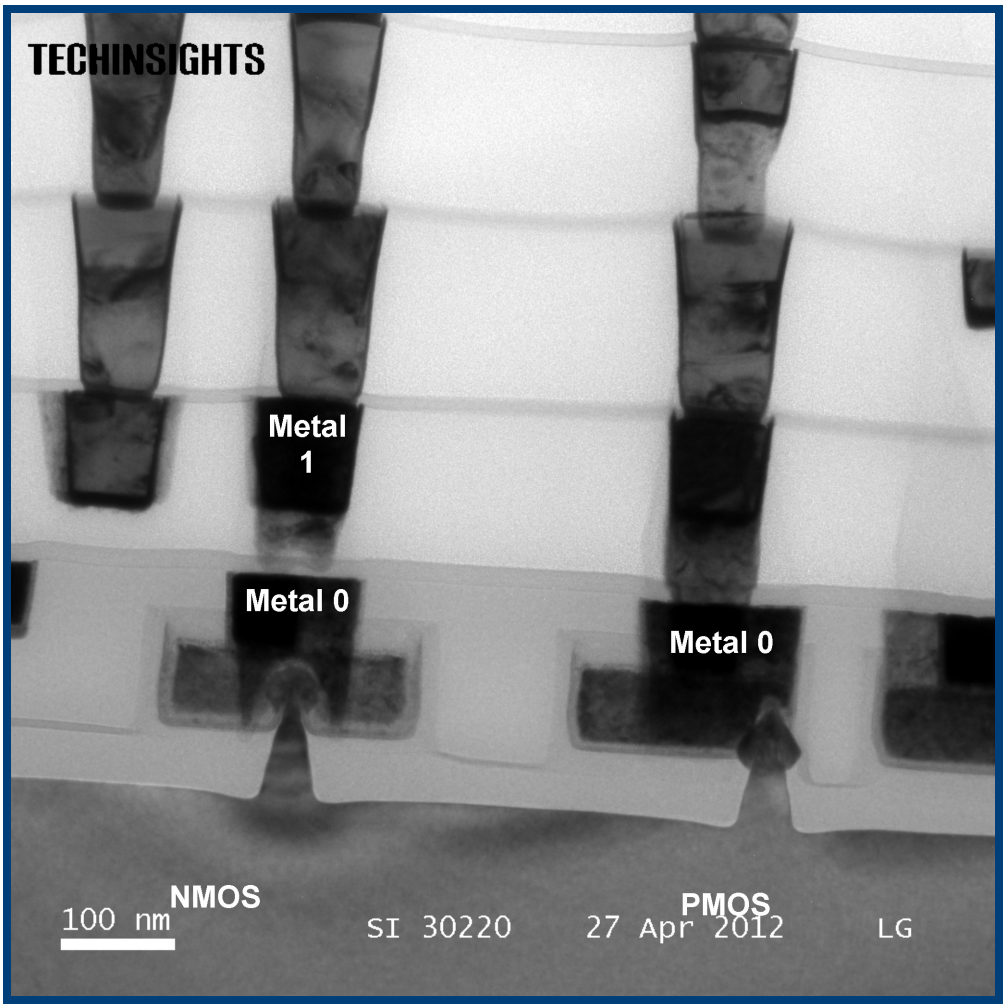


Figure 2.4.12: Contacts to source/drain regions of single-fin NMOS and PMOS transistors, low magnification TEM cross-section along the contact.

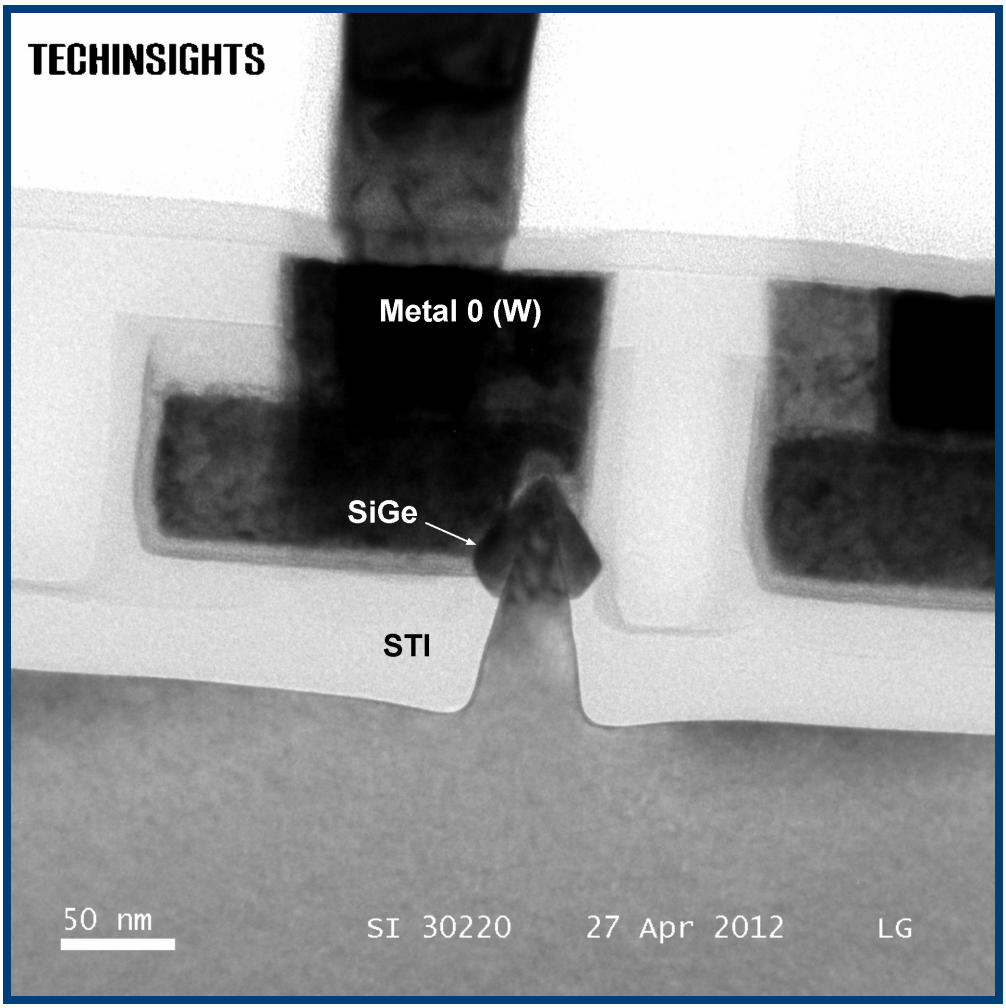


Figure 2.4.13: Contact to source/drain SiGe region of PMOS transistor, TEM cross-section.

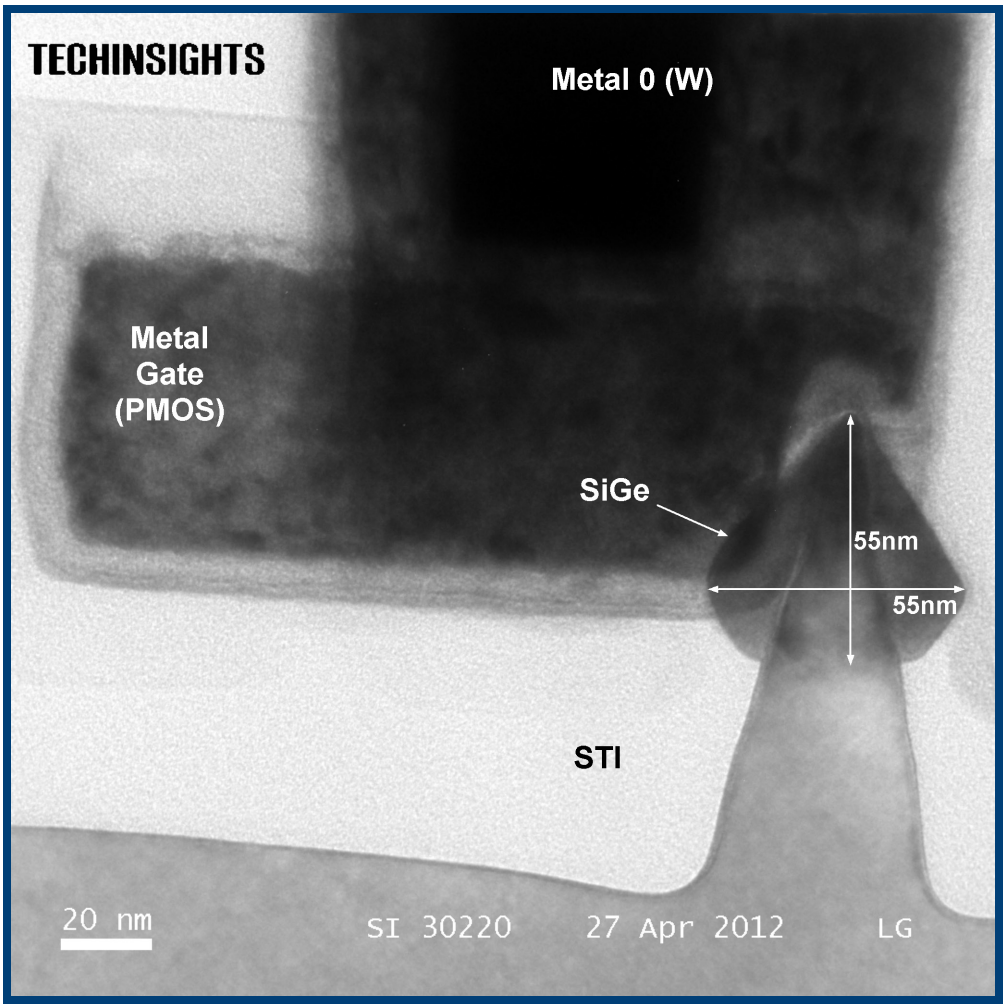


Figure 2.4.14: Contact to source/drain SiGe region of PMOS transistor, high magnification TEM cross-section.