

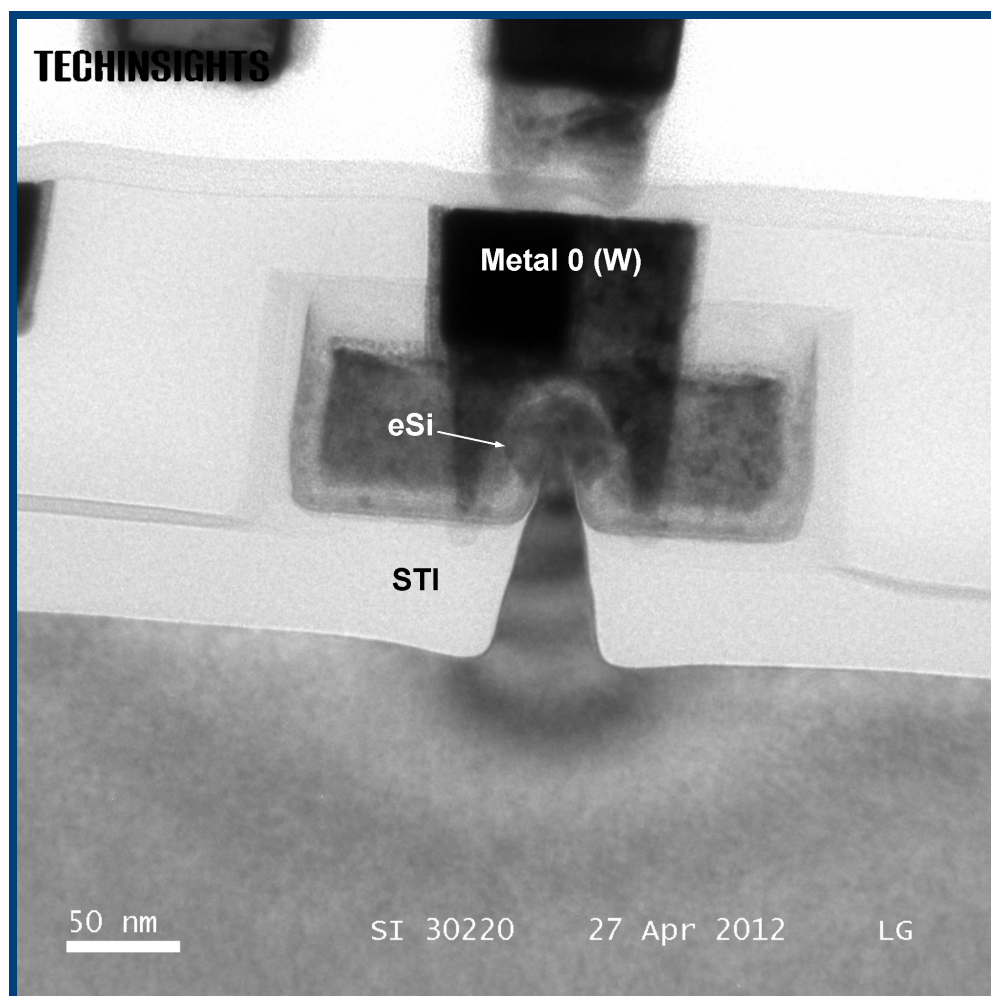


Figure 2.4.15: Contact to source/drain eSi region of NMOS transistor, TEM cross-section.

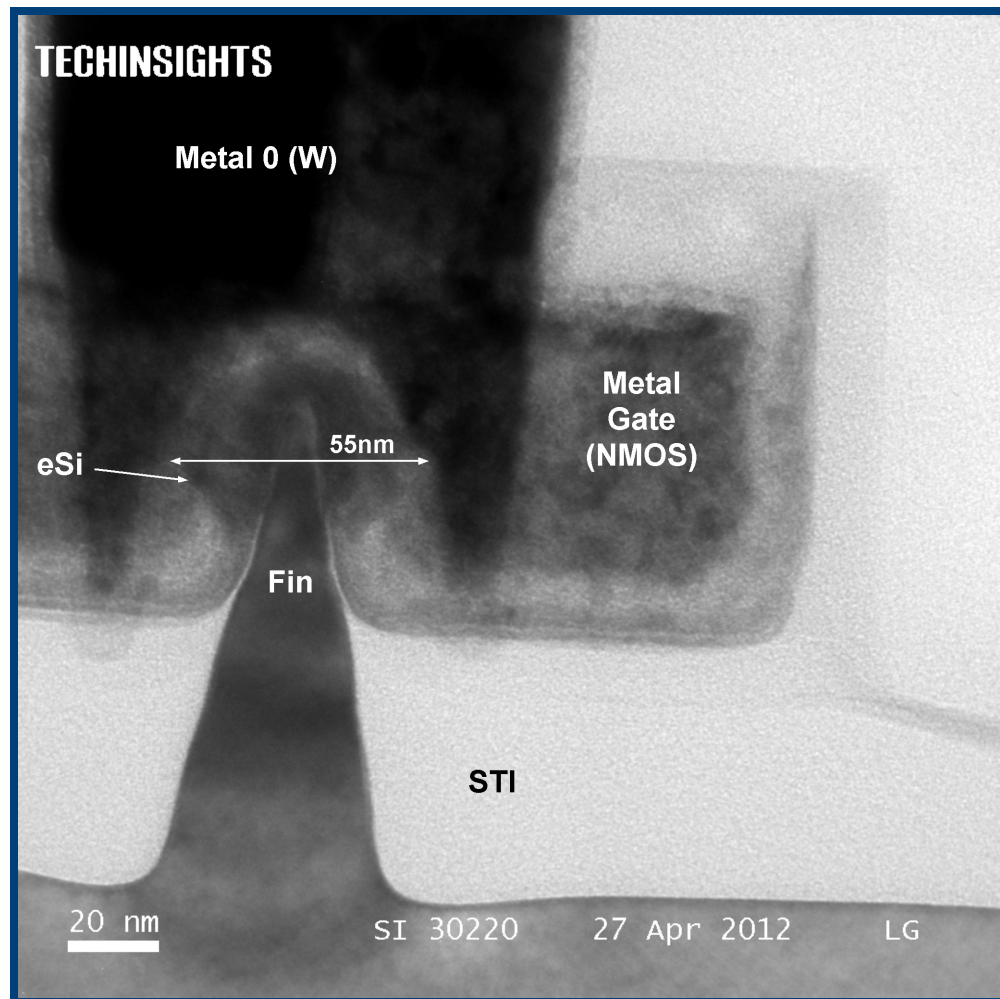


Figure 2.4.16: Contact to source/drain eSiGe region of NMOS transistor, high magnification TEM cross-section.

<i>Feature</i>	<i>Dimension</i>	<i>Unit</i>
Minimum observed Metal 0 contact width at top	50	nm
Metal 0 contact width at bottom	25	nm
Minimum metal 0 contact pitch	90	nm
Metal 0 contact overall depth	150	nm
Metal 0 contact recess into SiGe	25	nm
Metal 0 contact recess into Si SEG	50	nm

Comments

- Multi-layer pre-metal dielectric, PMD:
 - a conformal SiN contact etch stop layer, CESL;
 - an oxide 1 planarized by CMP;
 - an oxide 2 layer over NMOS and PMOS transistors;
- Dual damascene, tungsten-filled metal 0 with a TiN liner is used for local interconnects and for contacts;
- Metal 0 contact to PMOS source/drain region is formed on an elevated SiGe island grown in the fin recess; PMOS contact overetch is smaller compared to that of NMOS contact overetch;
- Metal 0 contact to NMOS source/drain region is formed on an elevated Si island likely grown by selective epitaxial growth in the fin recess.

2.5 Metallization

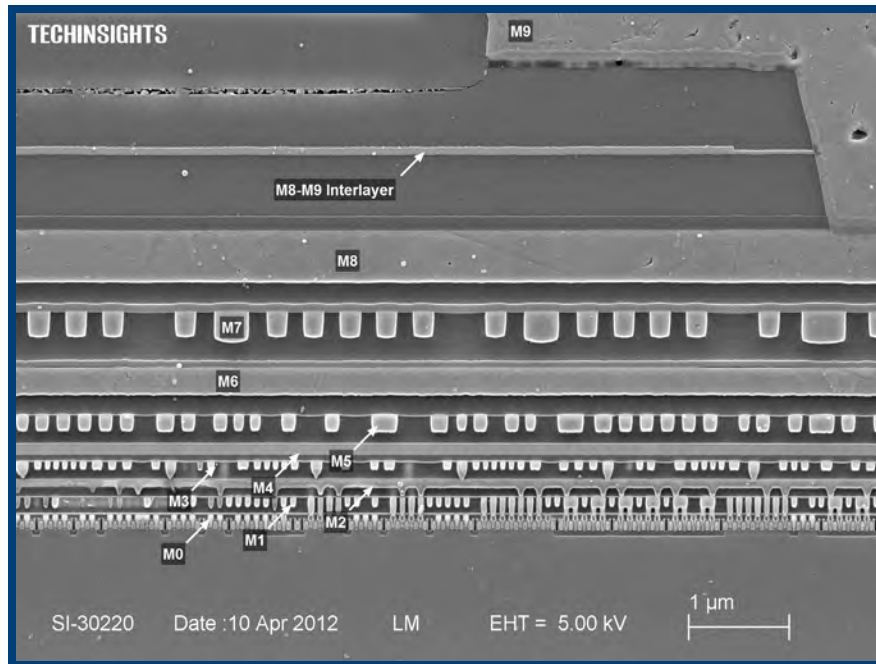


Figure 2.5.1: General interconnect structure, SEM cross-section.

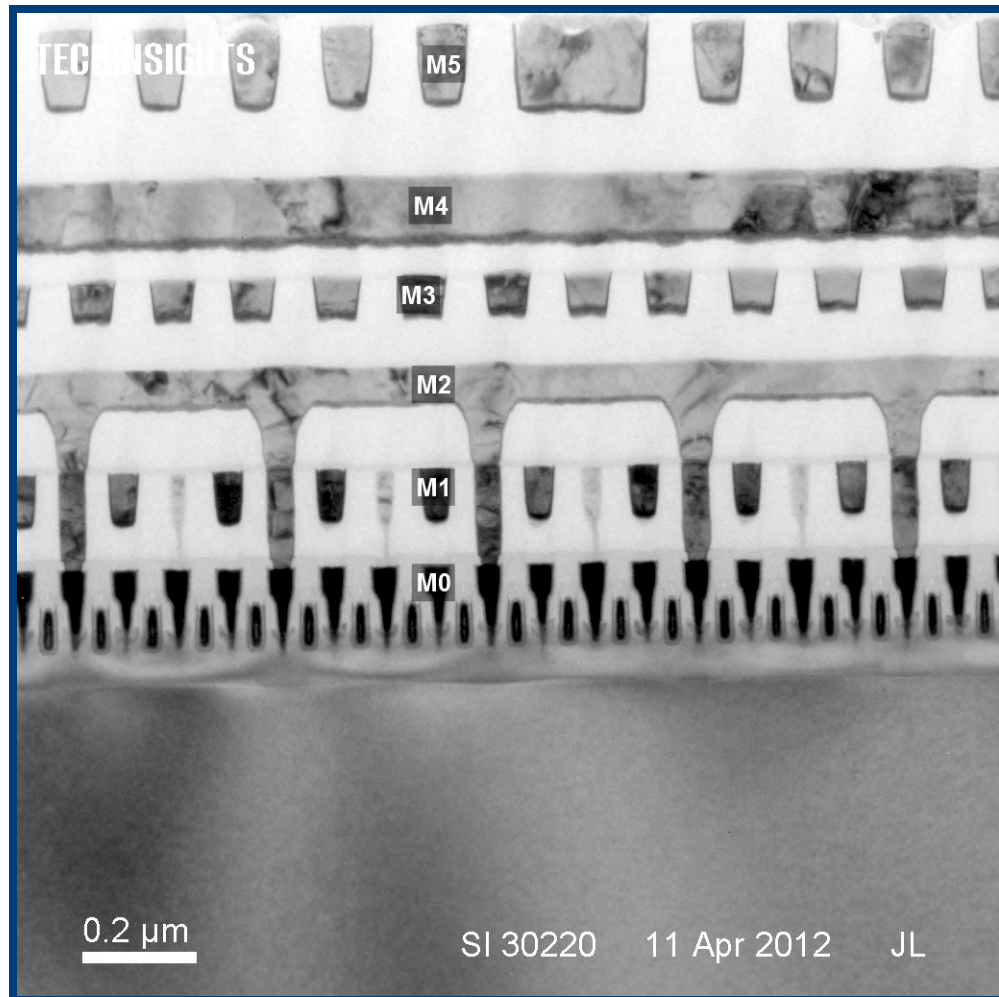


Figure 2.5.2: Metal 0 to metal 5 overview; TEM cross-section.

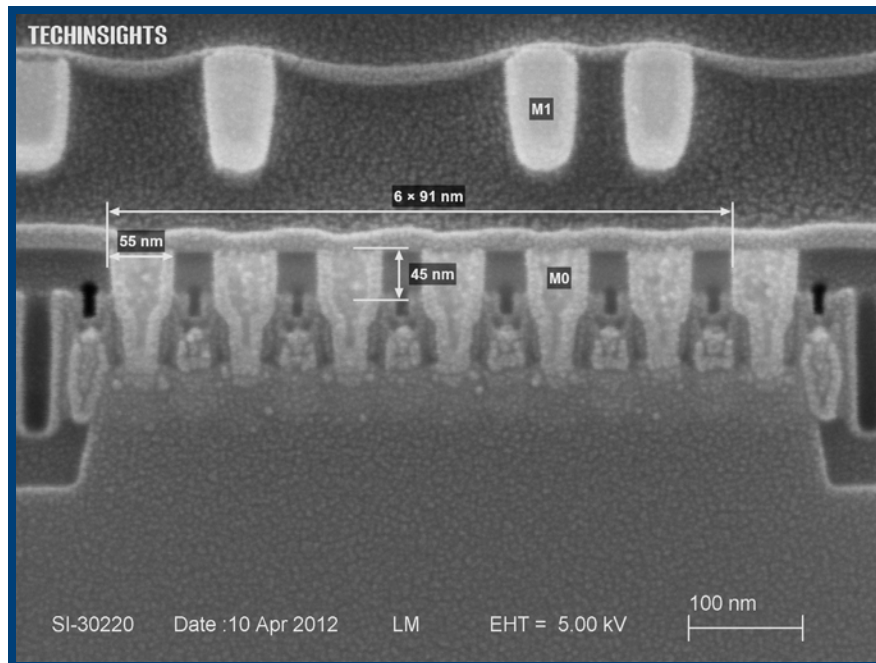


Figure 2.5.3: Metal 0; SEM cross-section.

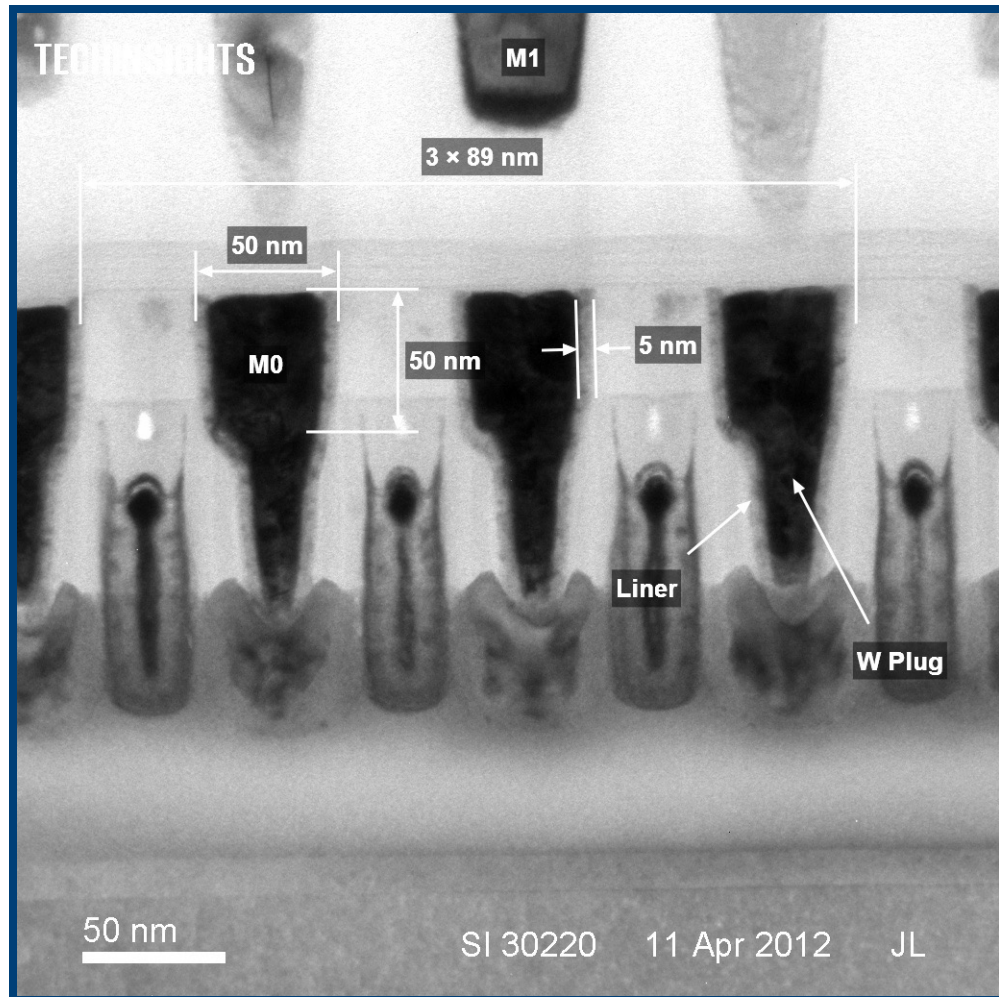


Figure 2.5.4: Metal 0; TEM cross-section.

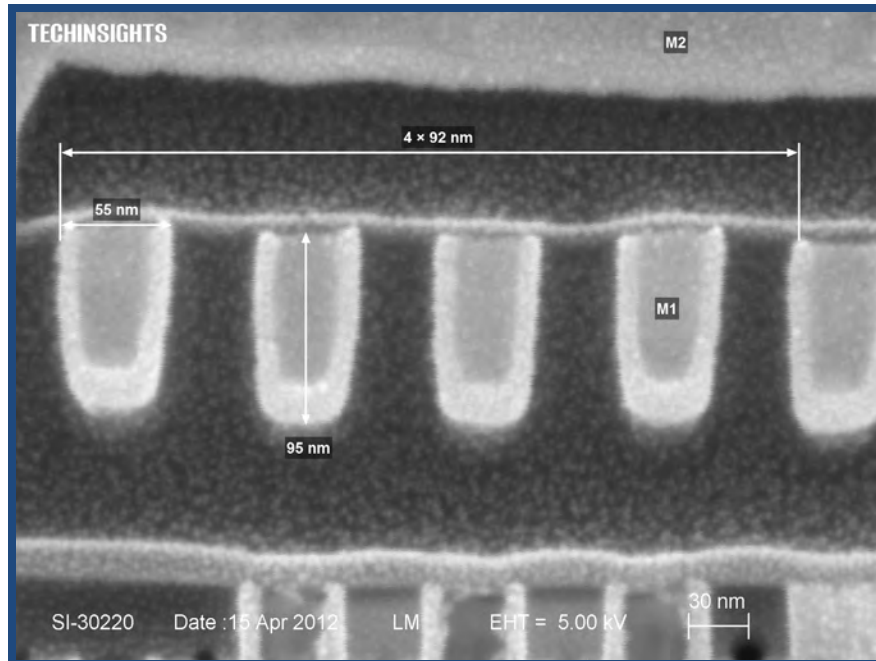


Figure 2.5.5: Metal 1; SEM cross-section.

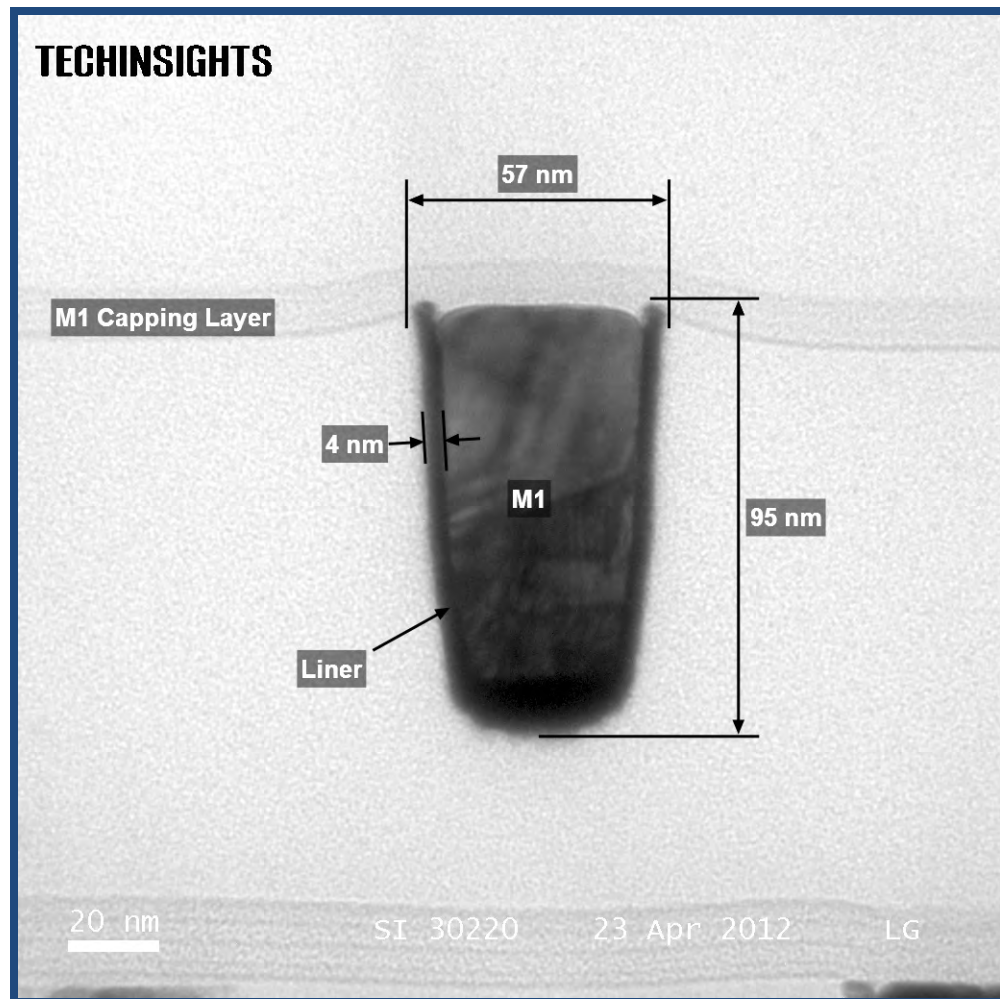


Figure 2.5.6: Metal 1; TEM cross-section.

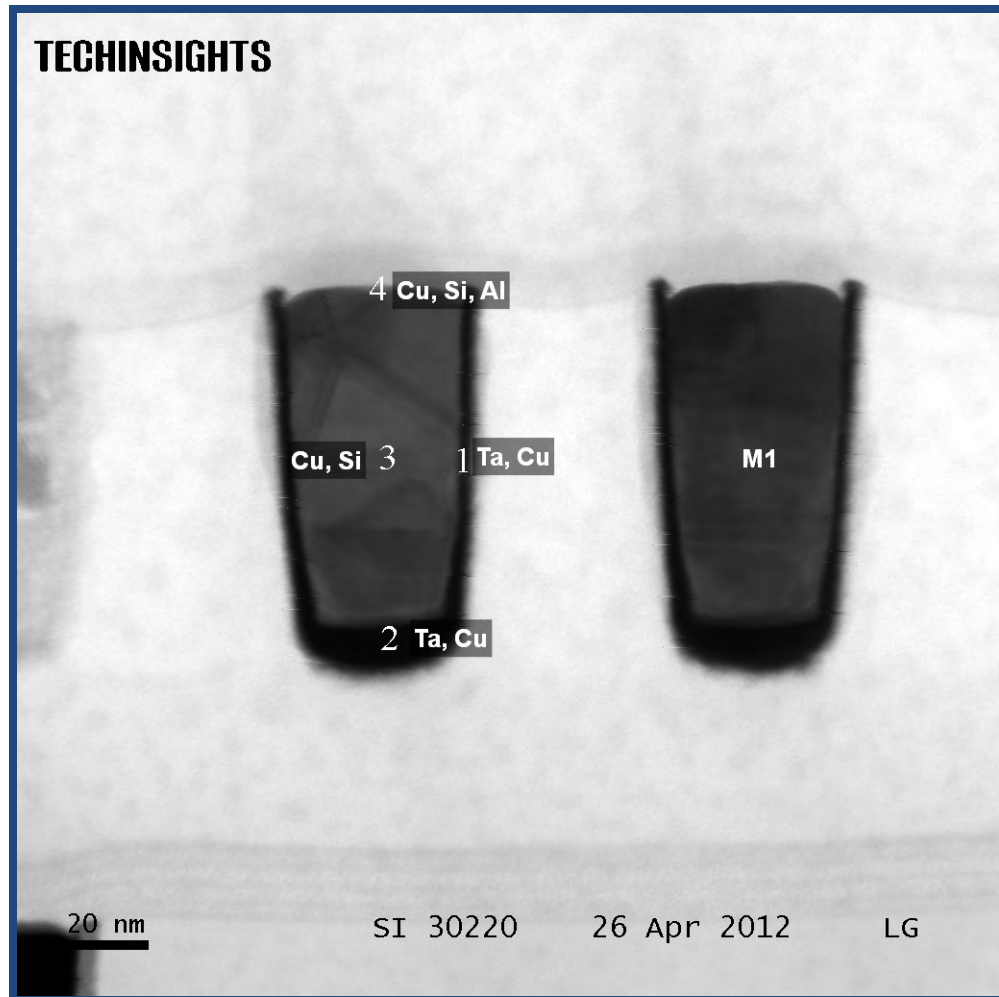


Figure 2.5.7: EDX analysis results for metal 1; TEM cross-section.

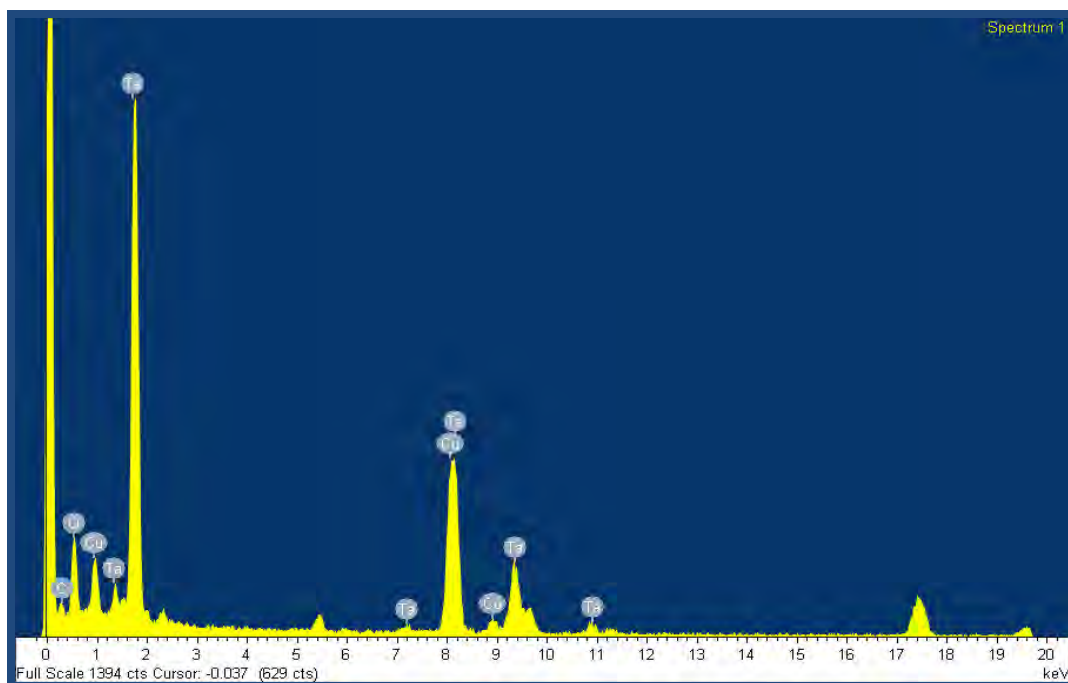


Figure 2.5.8: EDX spectrum of Ta-based barrier at position 1 of Figure 2.5.7.

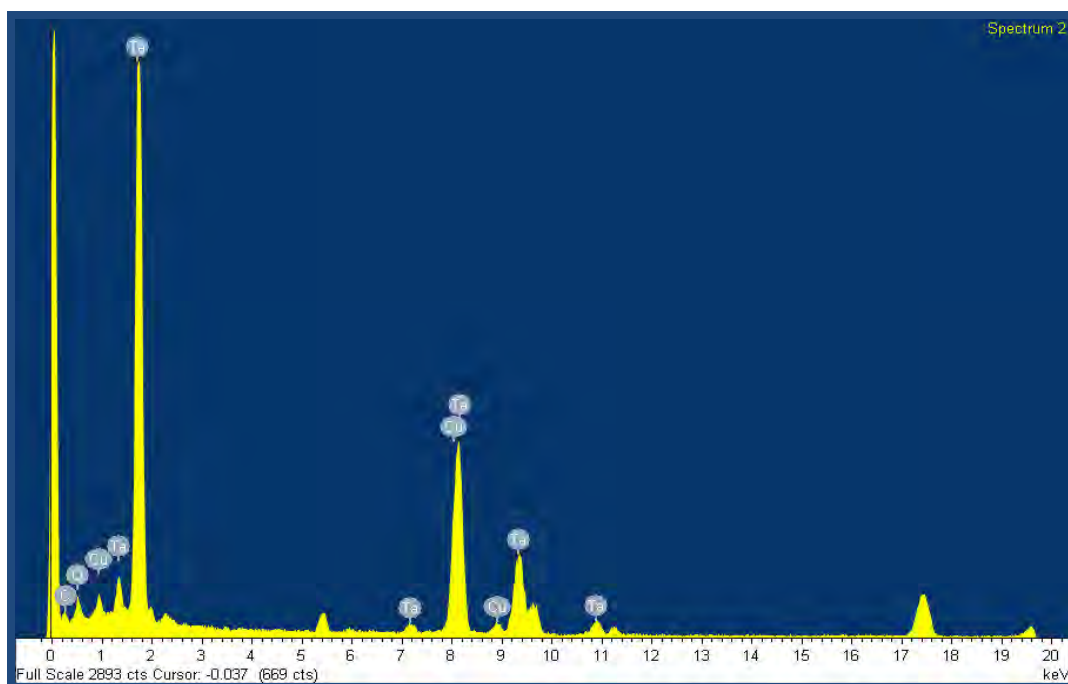


Figure 2.5.9: EDX spectrum of Ta-based barrier at position 2 of Figure 2.5.7.

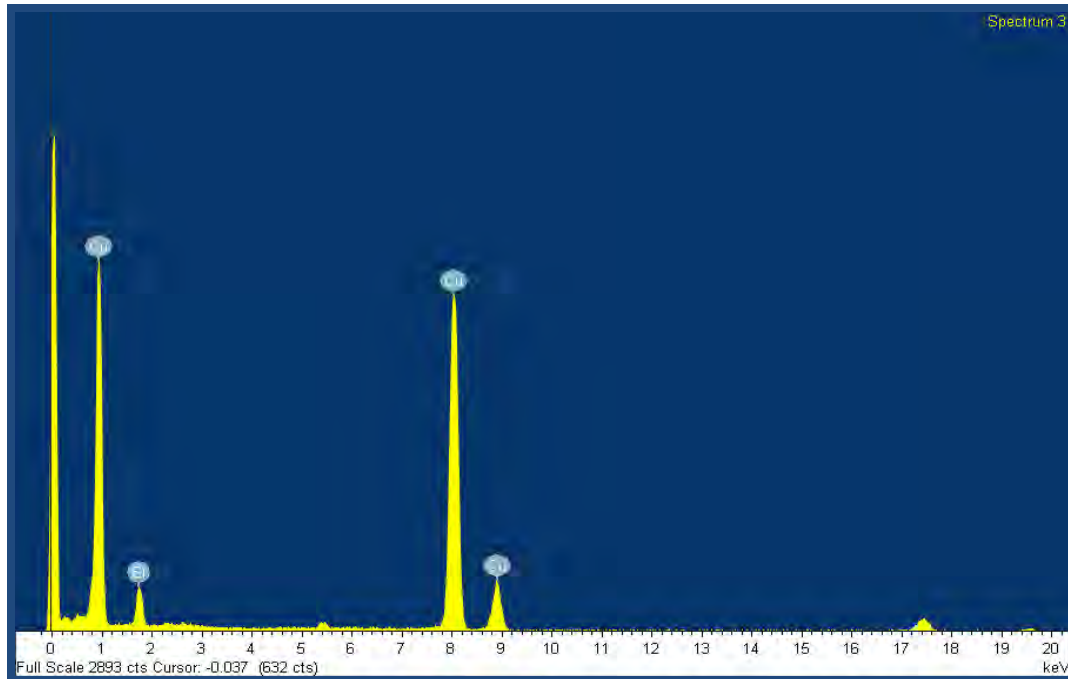


Figure 2.5.10: EDX spectrum of Cu body at position 3 of Figure 2.5.7.

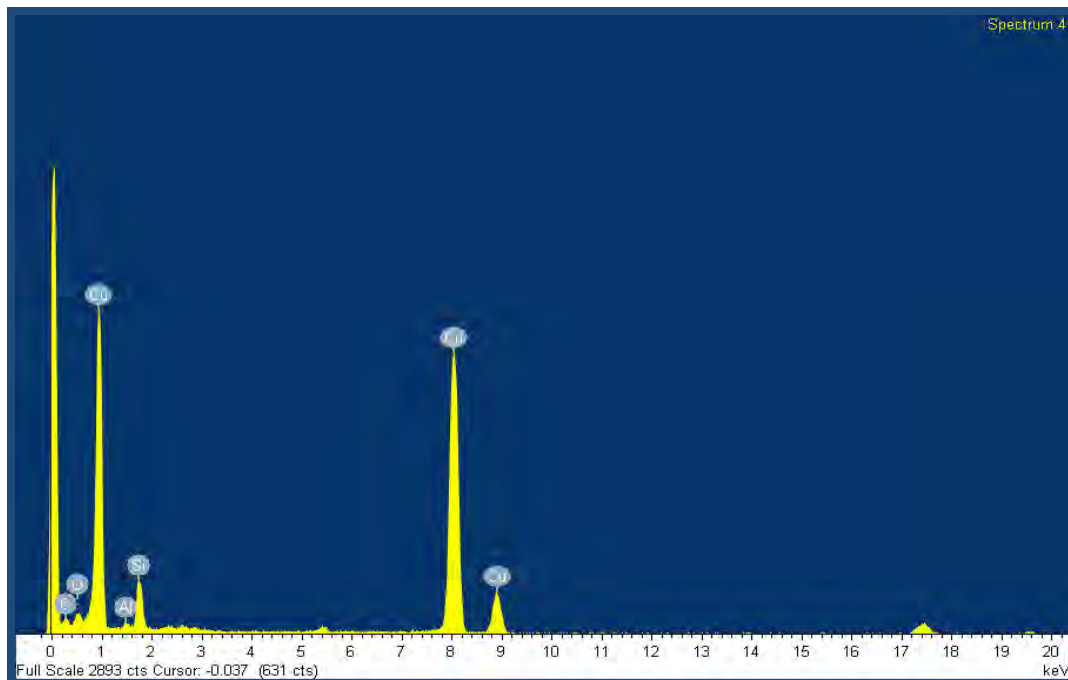


Figure 2.5.11: EDX spectrum of upper surface of Cu line at position 4 of Figure 2.5.7.

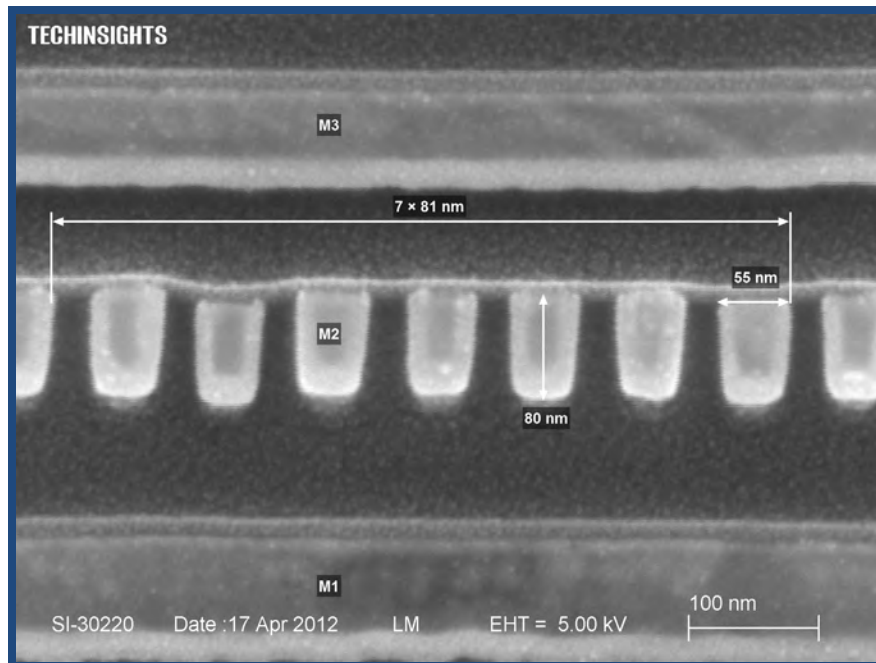


Figure 2.5.12: Metal 2; SEM cross-section.

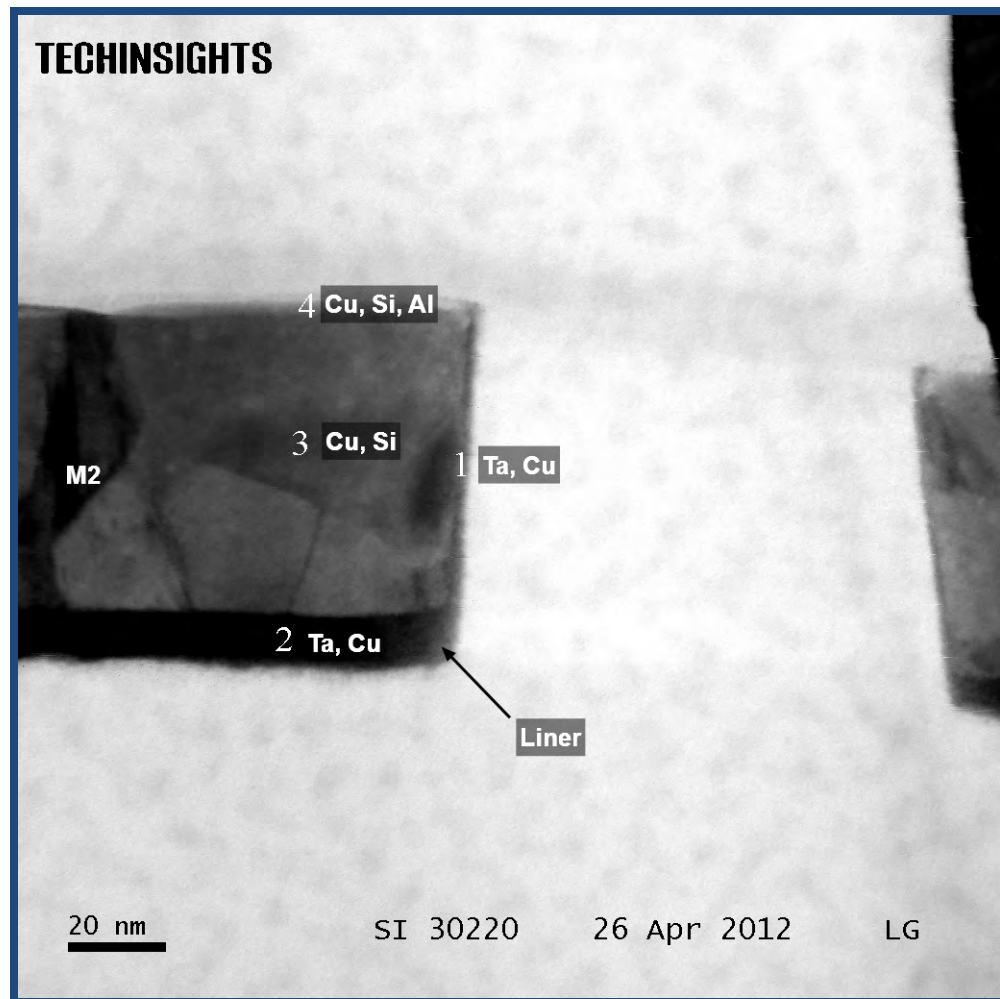


Figure 2.5.13: EDX analysis results for metal 2; TEM cross-section.

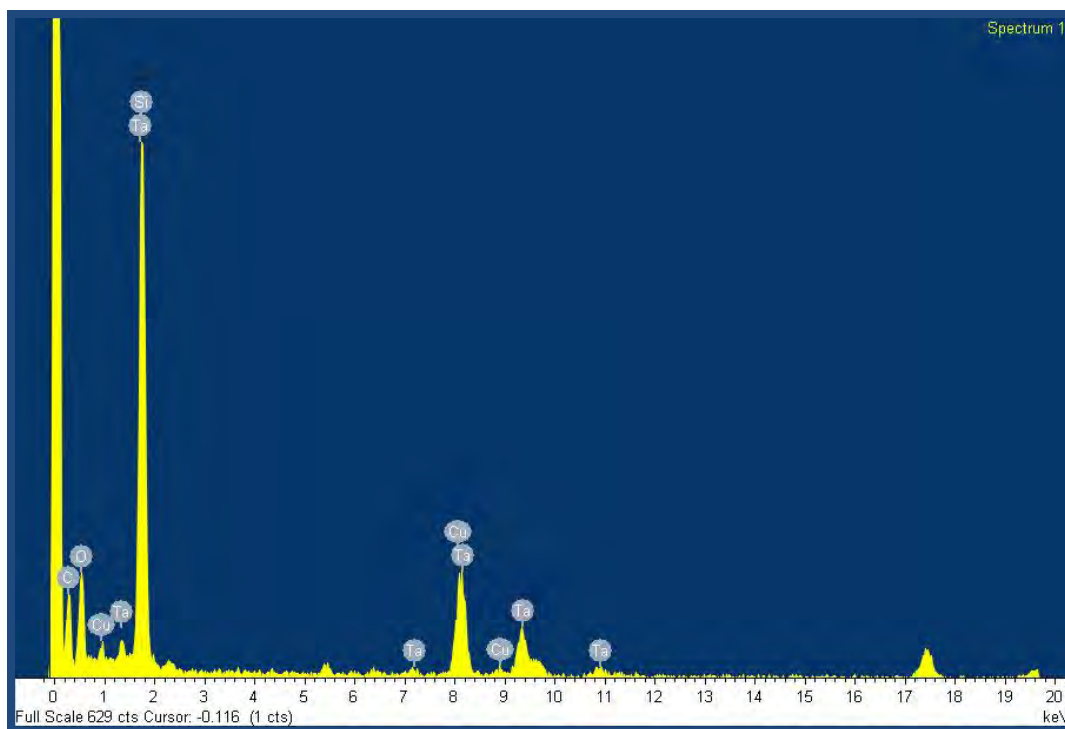


Figure 2.5.14: EDX spectrum of Ta-based barrier at position 1 of Figure 2.5.13.

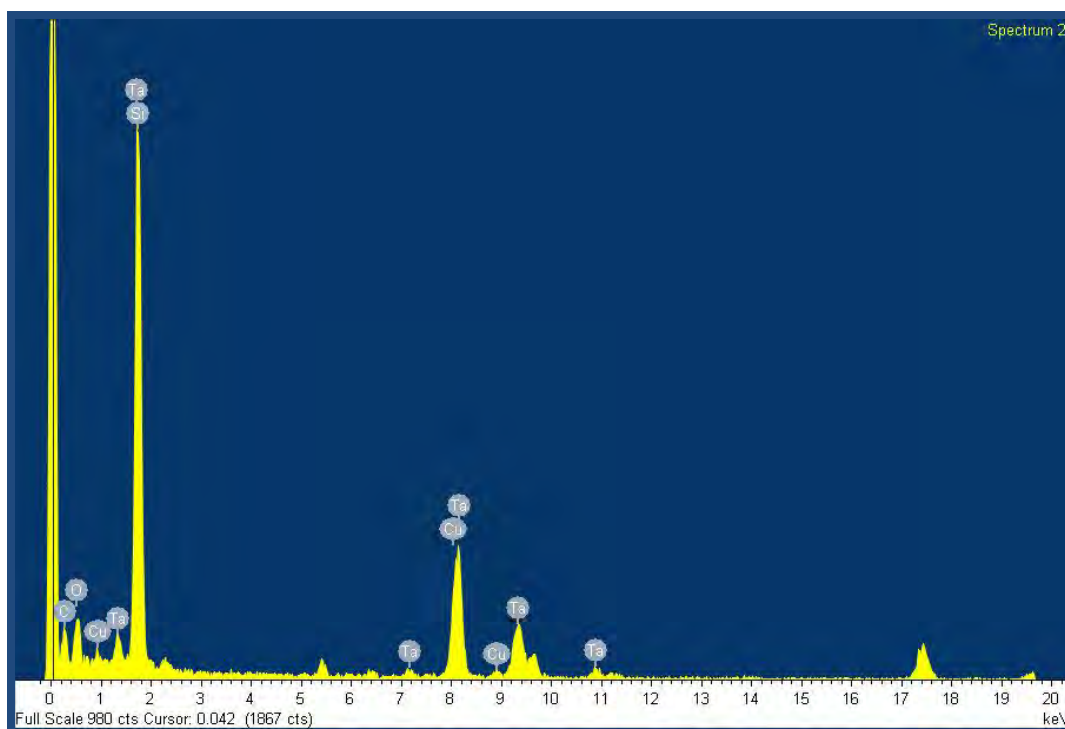


Figure 2.5.15: EDX spectrum of Ta-based barrier at position 2 of Figure 2.5.13.

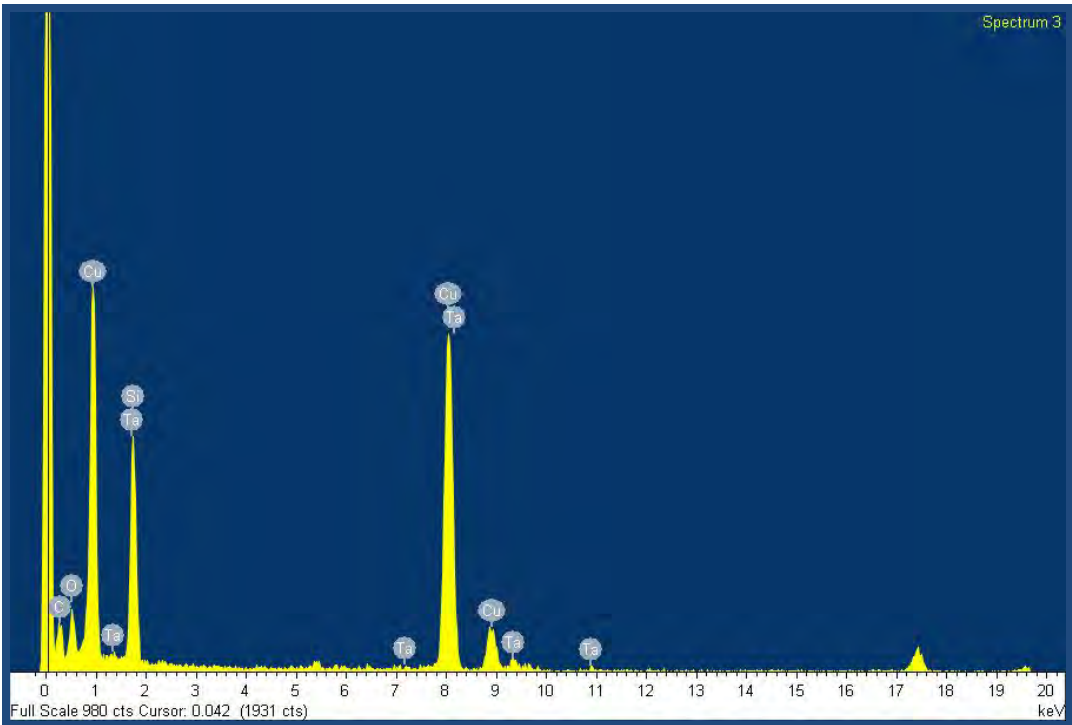


Figure 2.5.16: EDX spectrum of Cu body at position 3 of Figure 2.5.13.

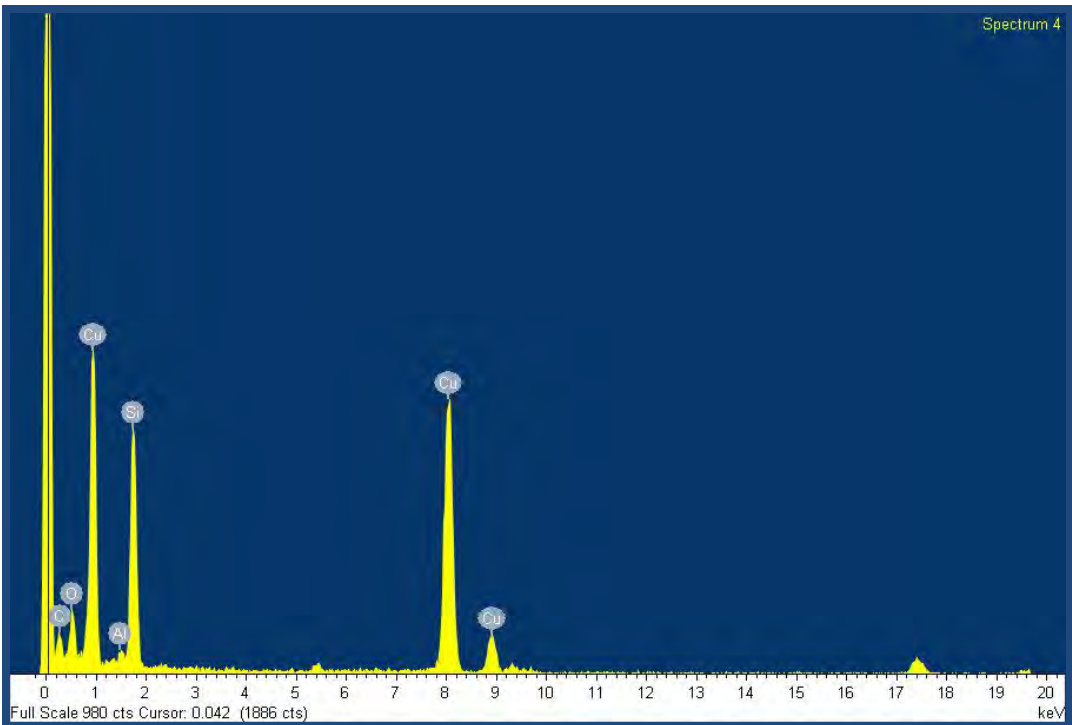


Figure 2.5.17: EDX spectrum of upper surface of Cu line at position 4 of Figure 2.5.13.

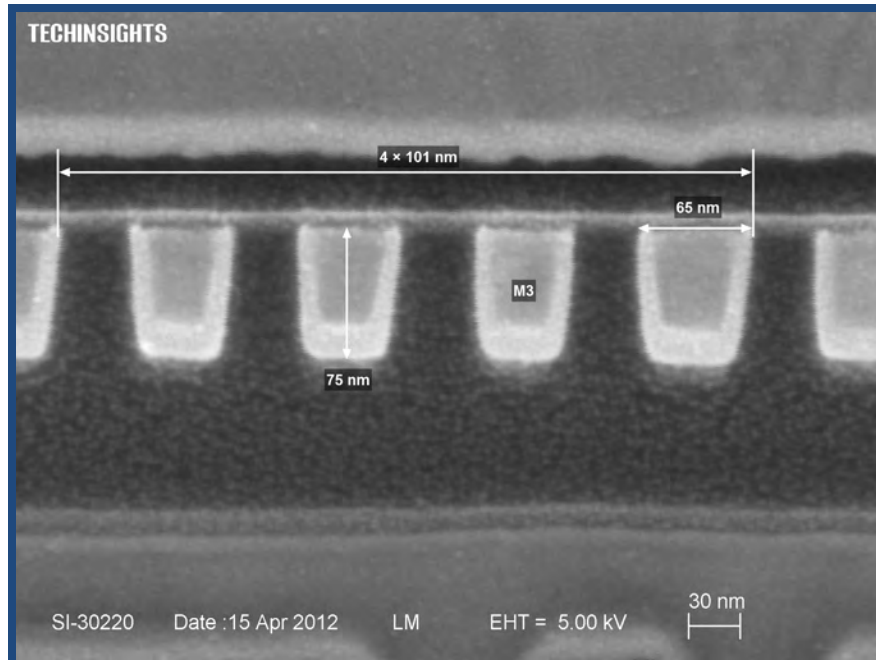


Figure 2.5.18: Metal 3; SEM cross-section.

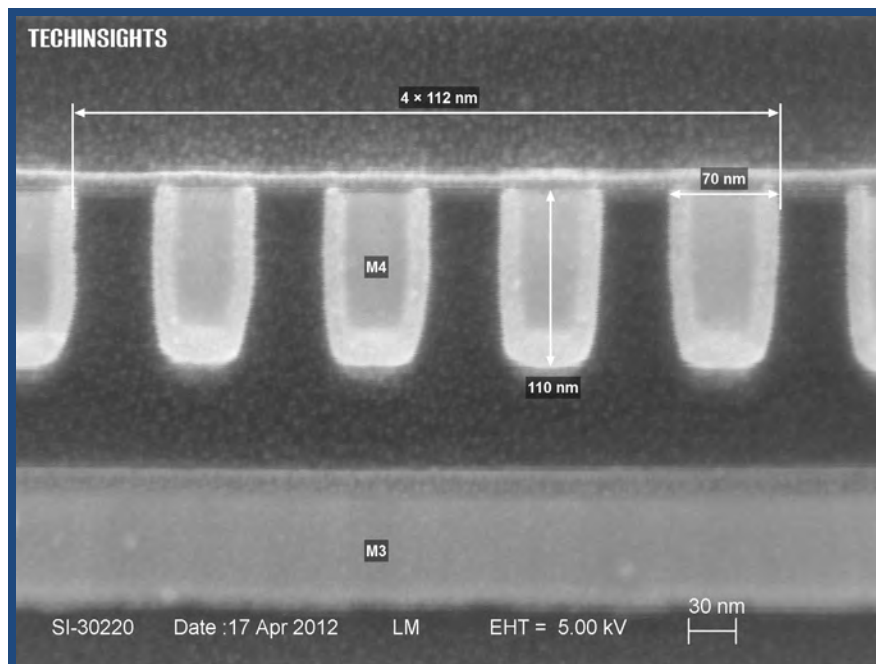


Figure 2.5.19: Metal 4; SEM cross-section.

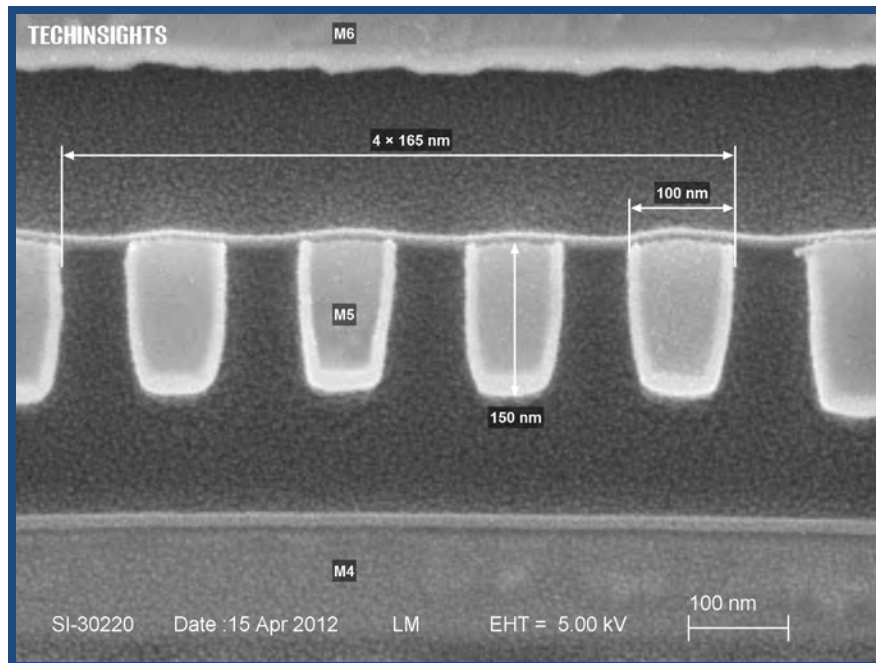


Figure 2.5.20: Metal 5; SEM cross-section.

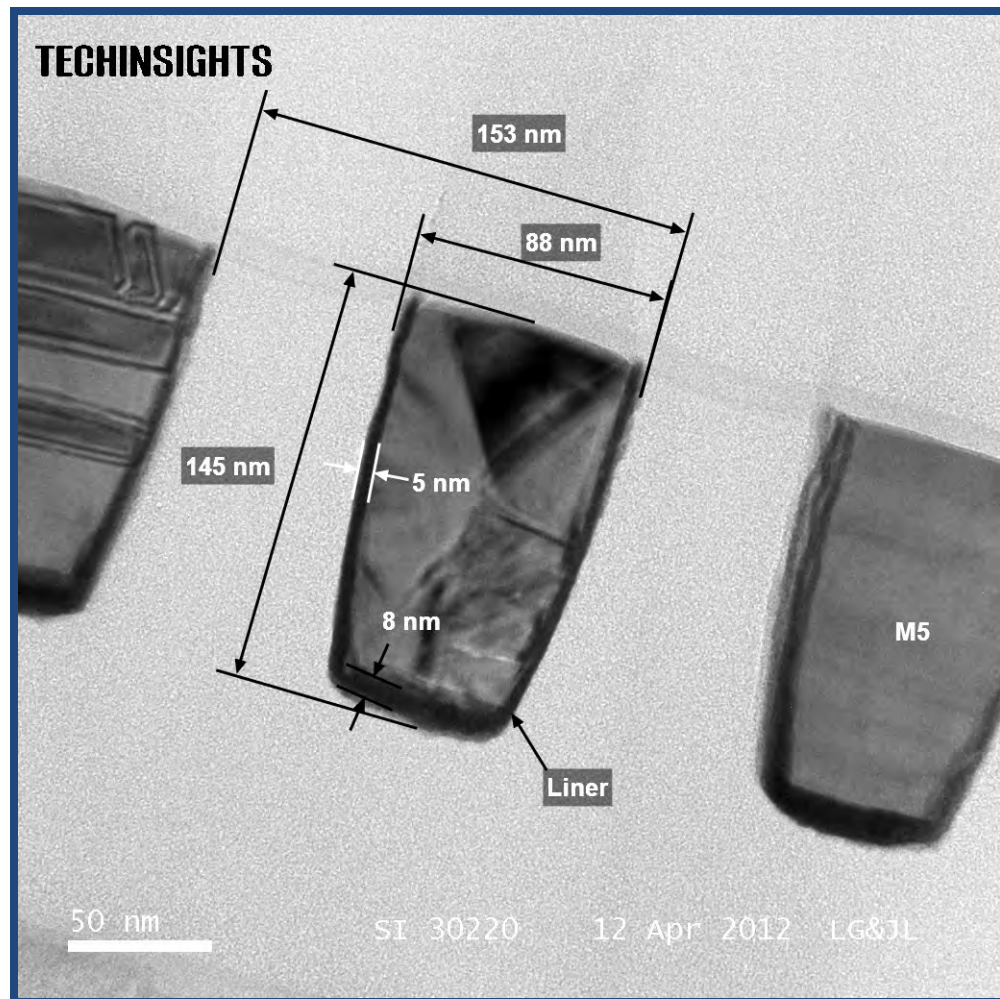


Figure 2.5.21: Metal 5; TEM cross-section.

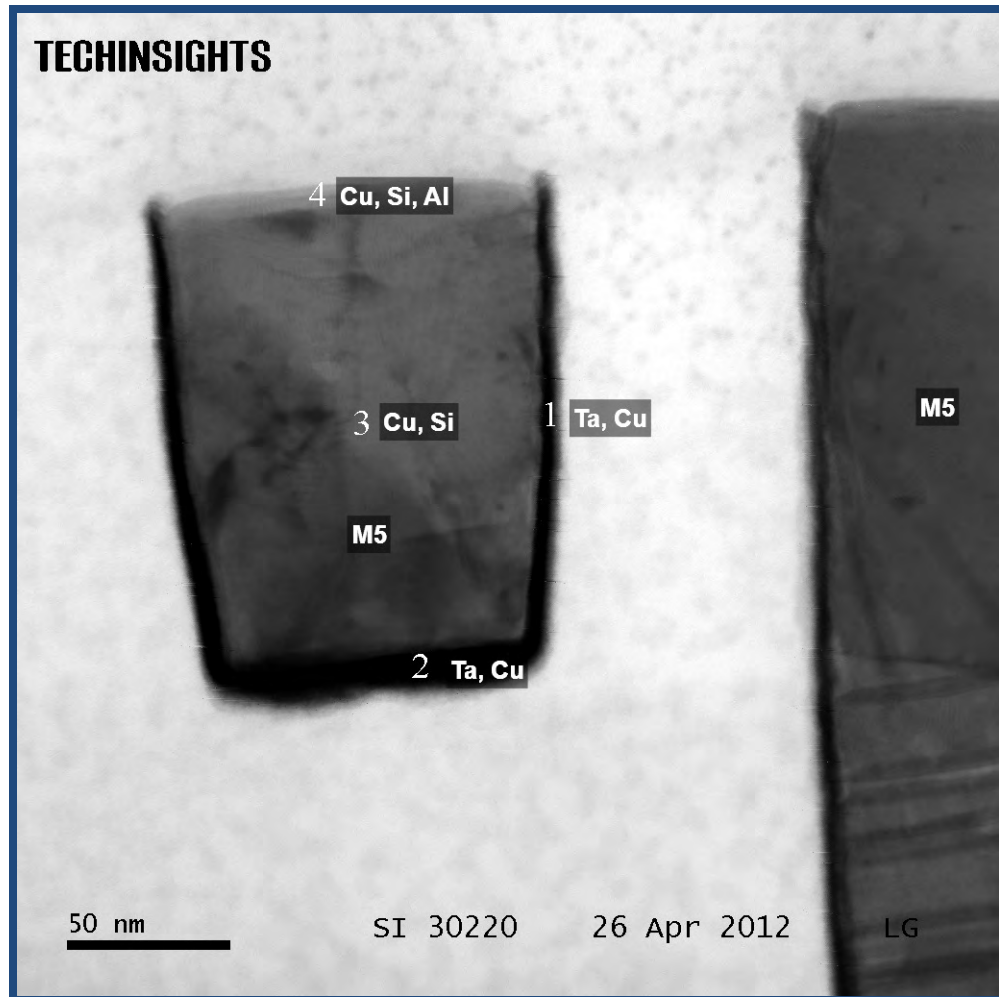


Figure 2.5.22: EDX analysis results for metal 5; TEM cross-section.

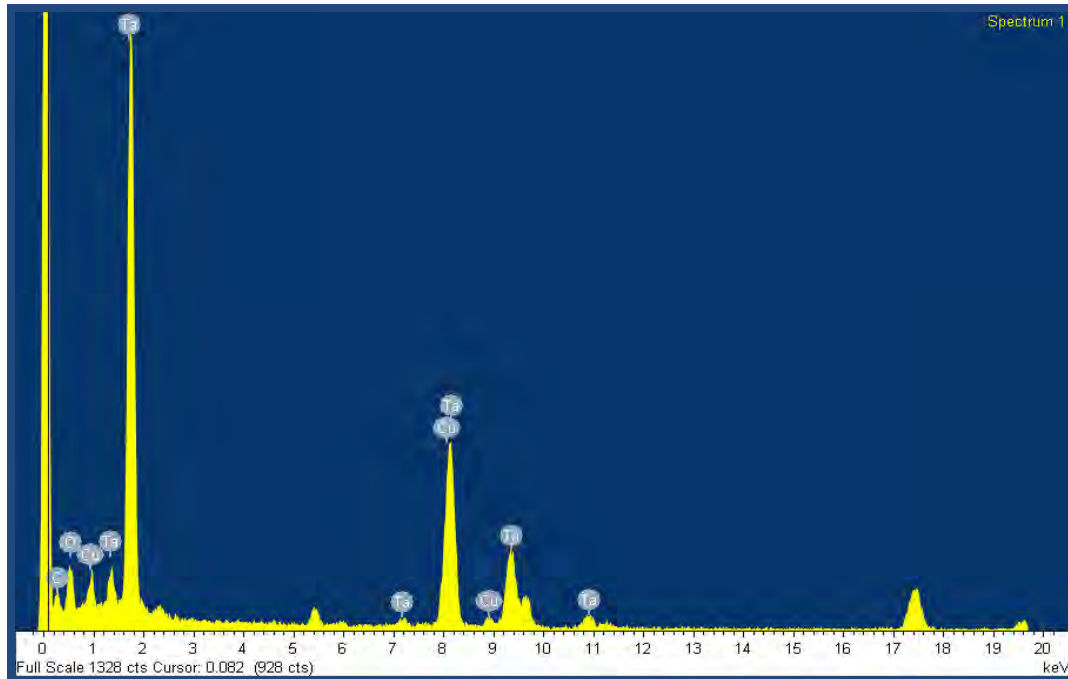


Figure 2.5.23: EDX spectrum of Ta-based barrier at position 1 of Figure 2.5.22.

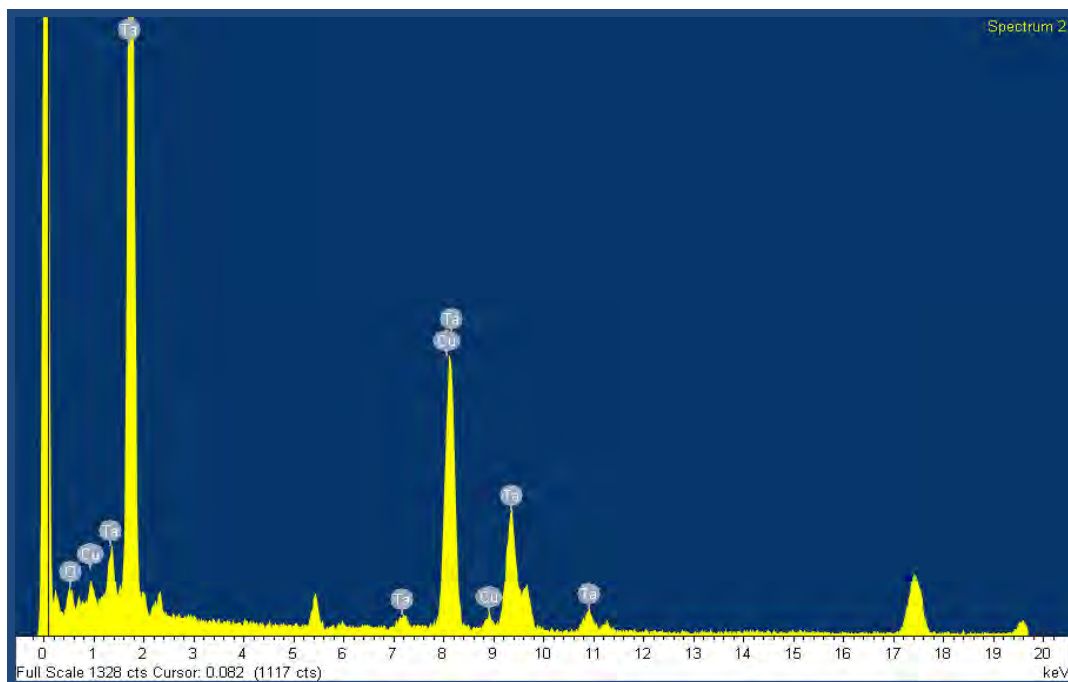


Figure 2.5.24: EDX spectrum of Ta-based barrier at position 2 of Figure 2.5.22.

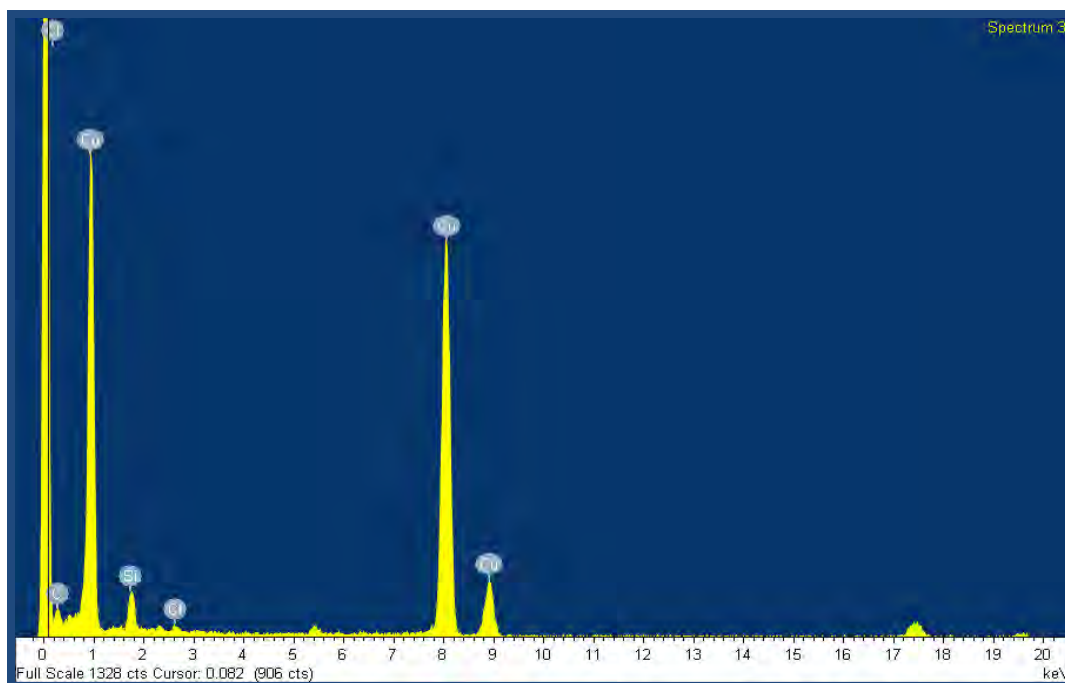


Figure 2.5.25: EDX spectrum of Cu body at position 3 of Figure 2.5.22.

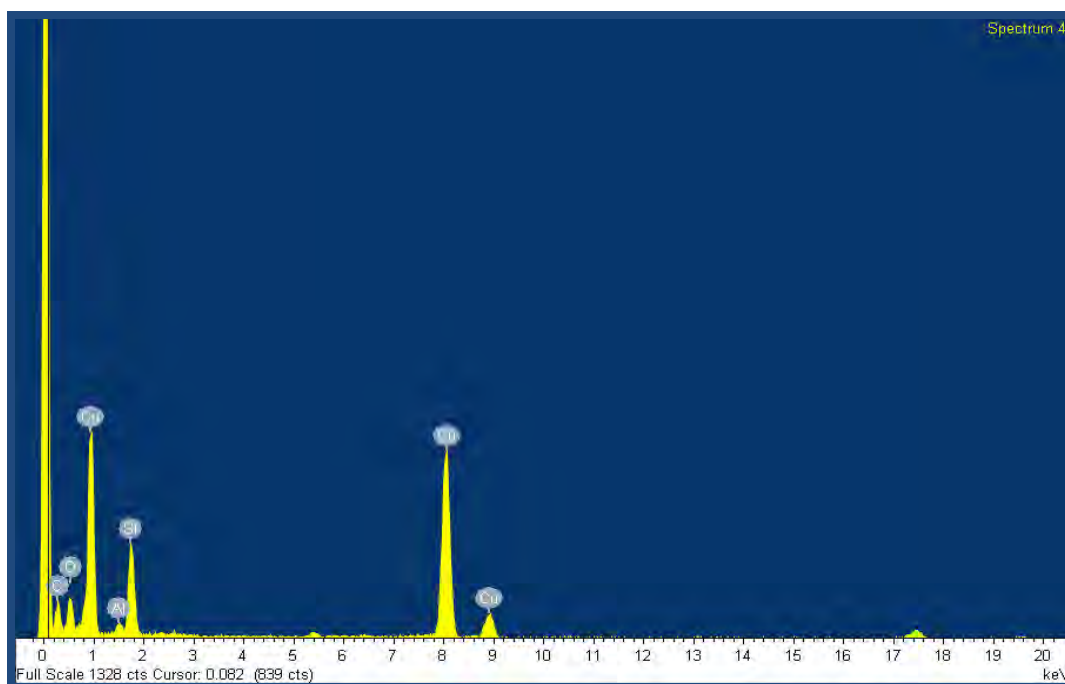


Figure 2.5.26: EDX spectrum of top surface of Cu line at position 4 of Figure 2.5.22.

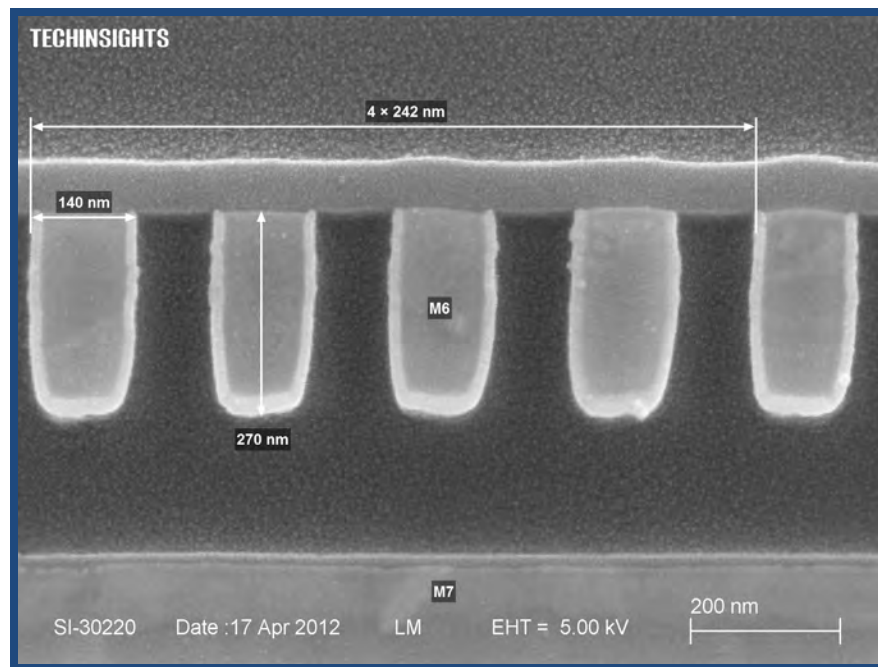


Figure 2.5.27: Metal 6; SEM cross-section.

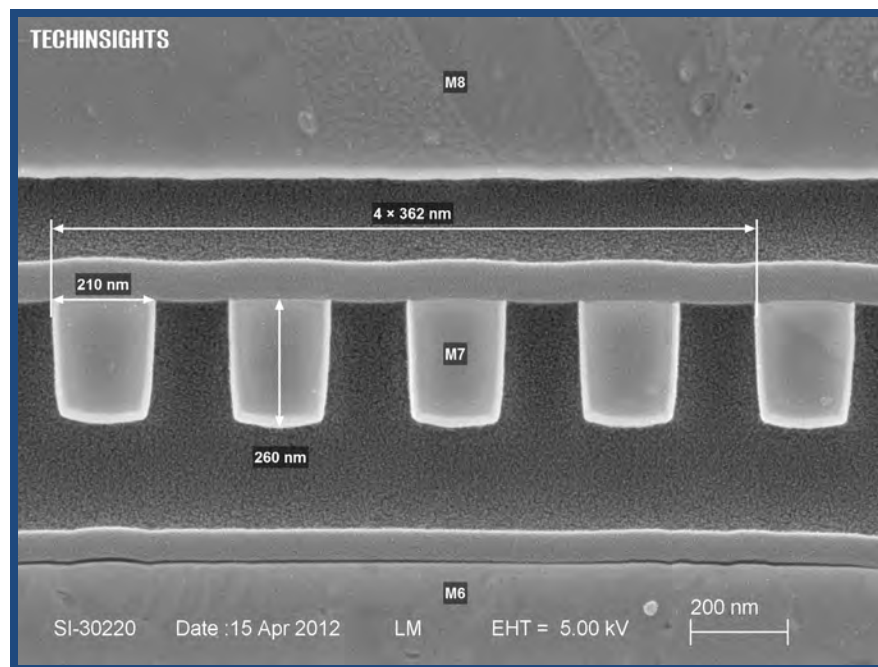


Figure 2.5.28: Metal 7; SEM cross-section.

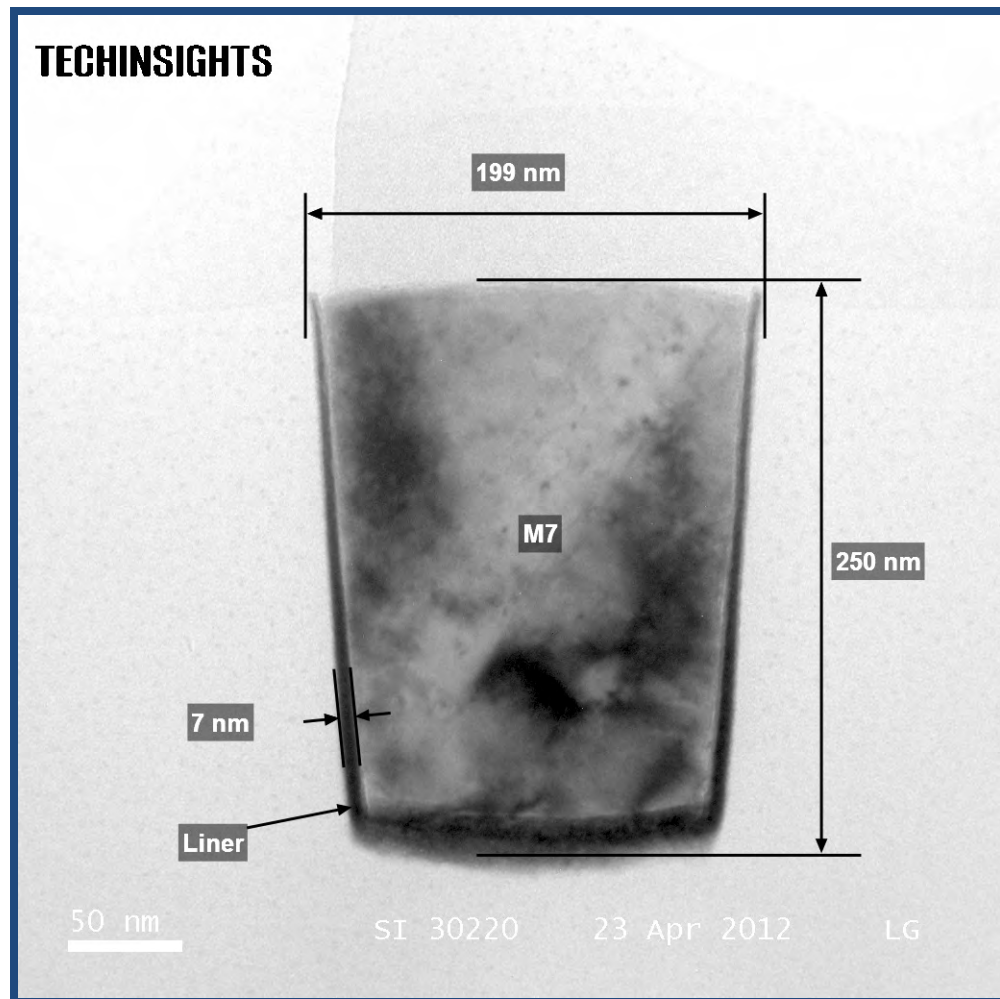


Figure 2.5.29: Metal 7; SEM cross-section.

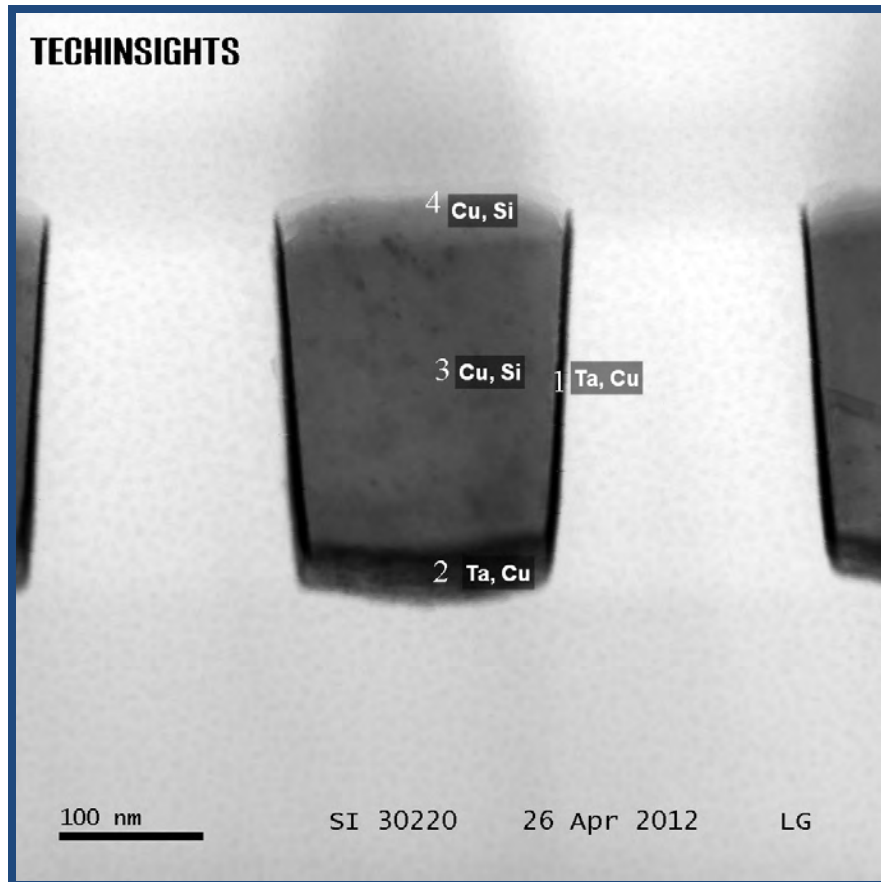


Figure 2.5.30: EDX results for metal 7; TEM cross-section.

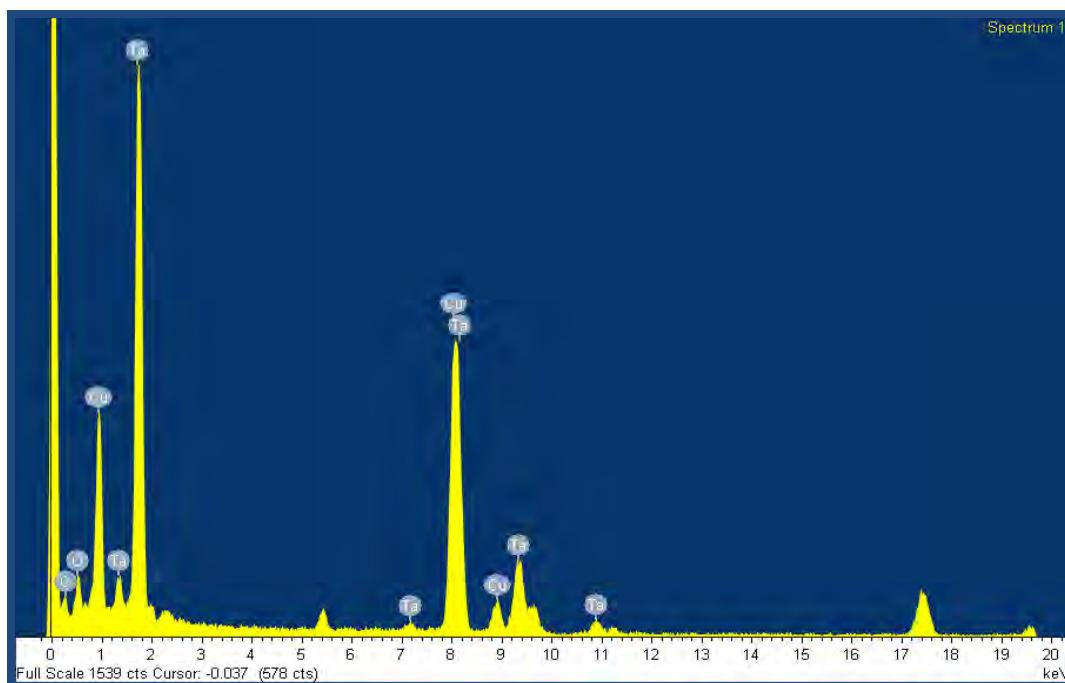


Figure 2.5.31: EDX spectrum of Ta-based barrier at position 1 of Figure 2.5.30.

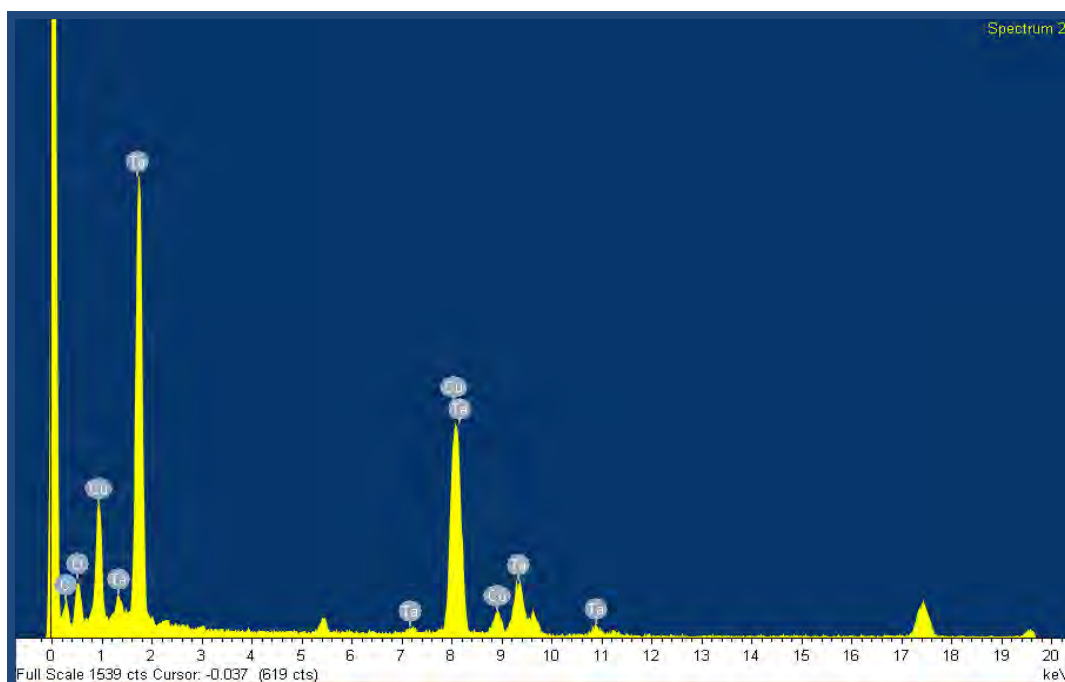


Figure 2.5.32: EDX spectrum of Ta-based barrier at position 2 of Figure 2.5.30.

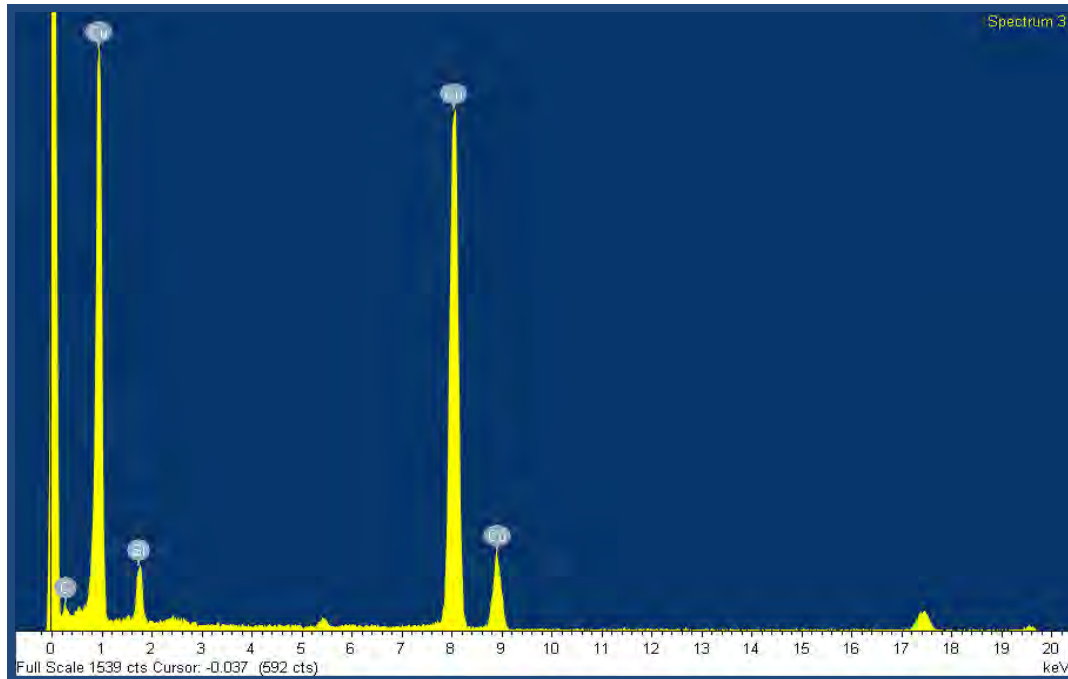


Figure 2.5.33: EDX spectrum of Cu body at position 3 of Figure 2.5.30.

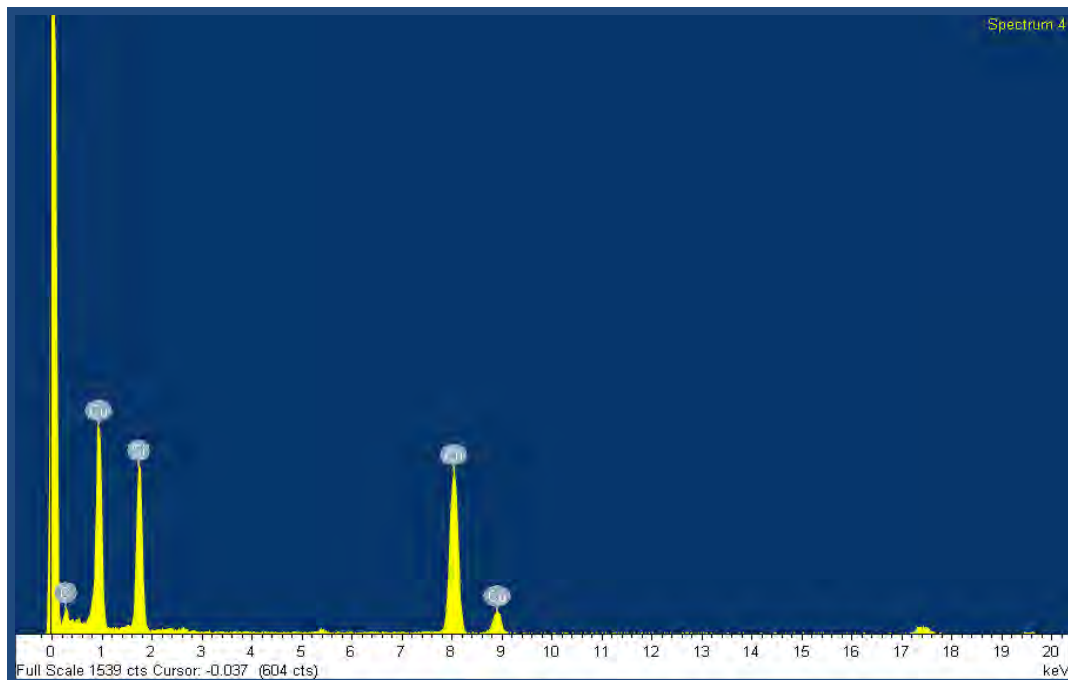


Figure 2.5.34: EDX spectrum of upper surface of Cu line at position 4 of Figure 2.5.30.

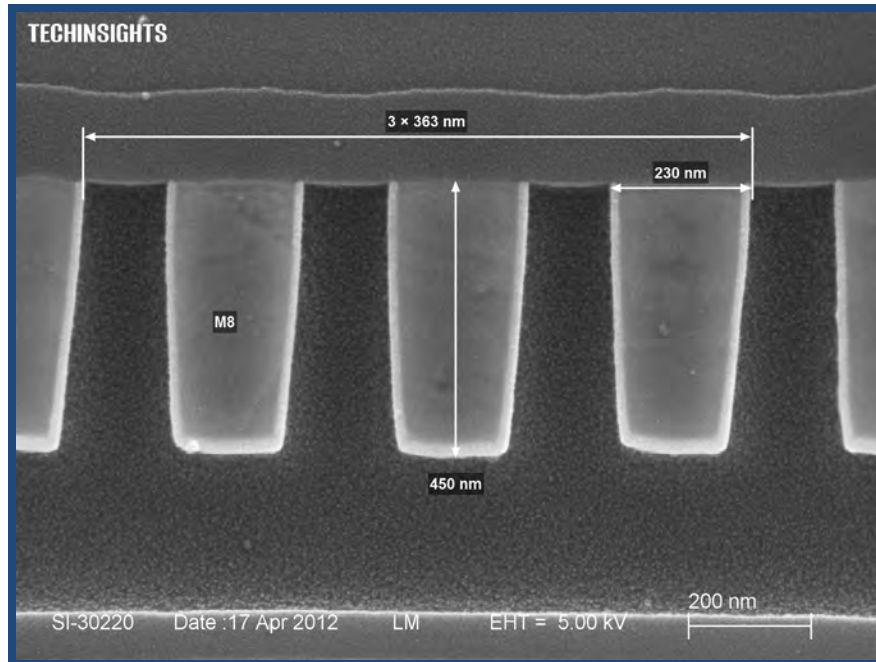


Figure 2.5.35: Metal 8; SEM cross-section.

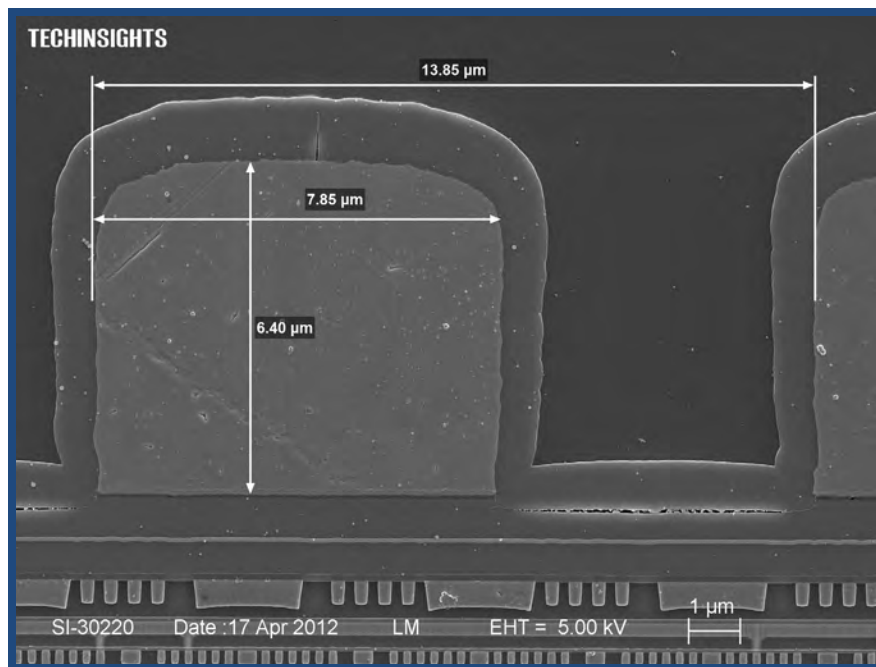


Figure 2.5.36: Metal 9; SEM cross-section.

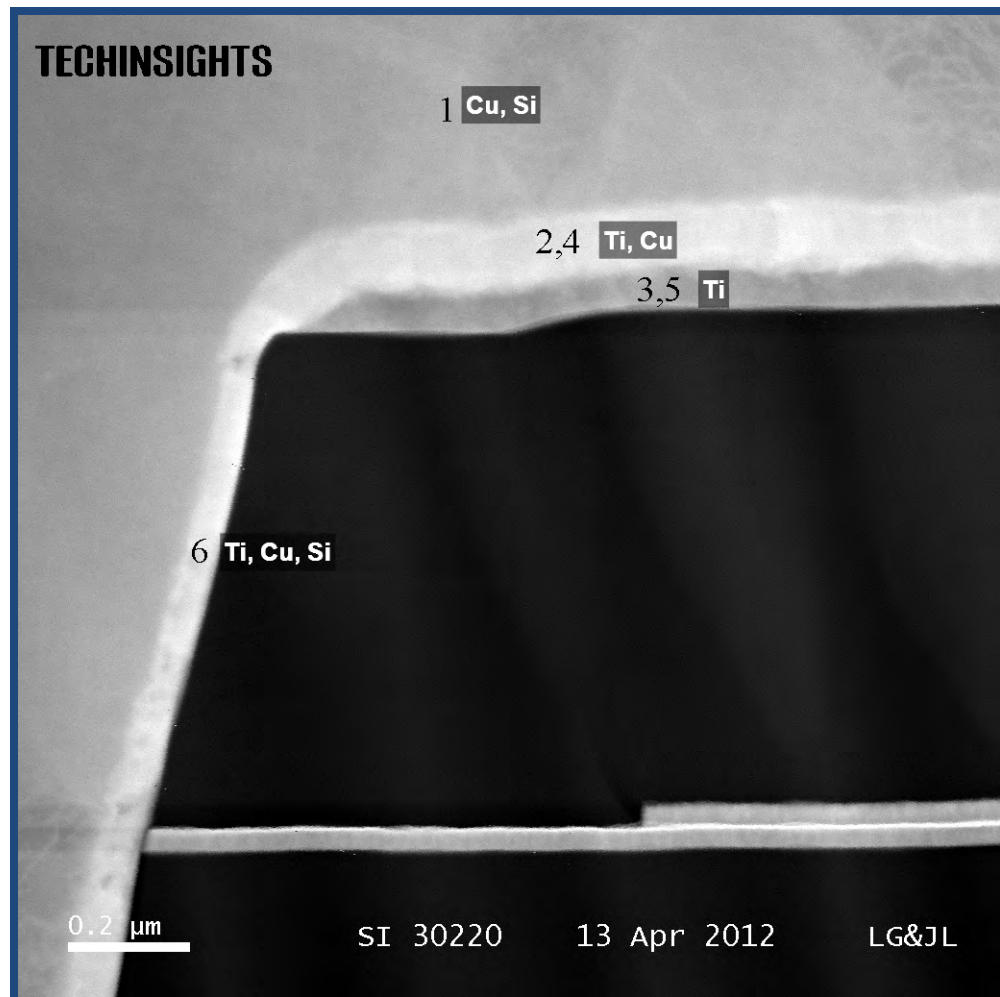


Figure 2.5.37: EDX analysis results for metal 9; HAADF TEM cross-section.

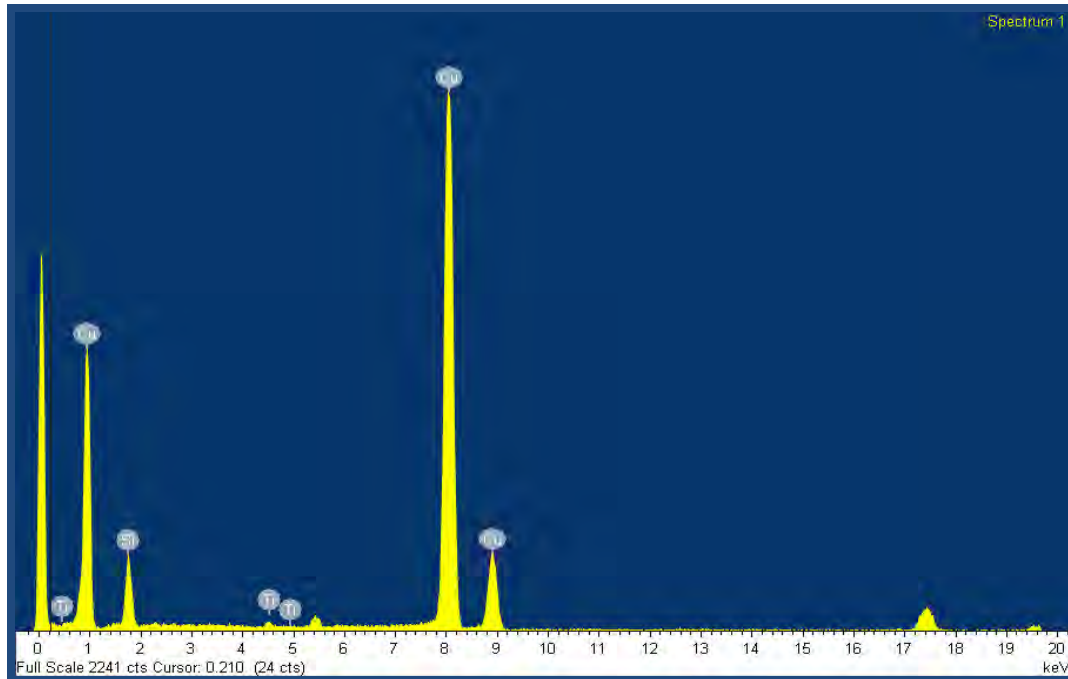


Figure 2.5.38: EDX spectrum of Si doped Cu at position 1 of Figure 2.5.37.

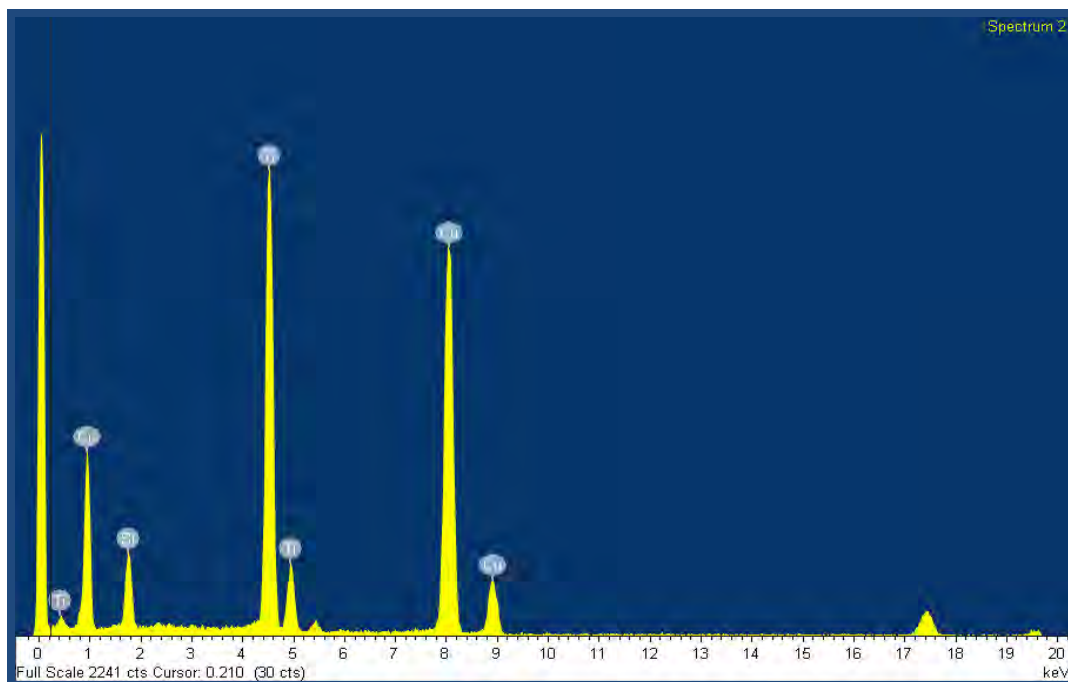


Figure 2.5.39: EDX spectrum of Ti-Cu layer at position 2 of Figure 2.5.37.

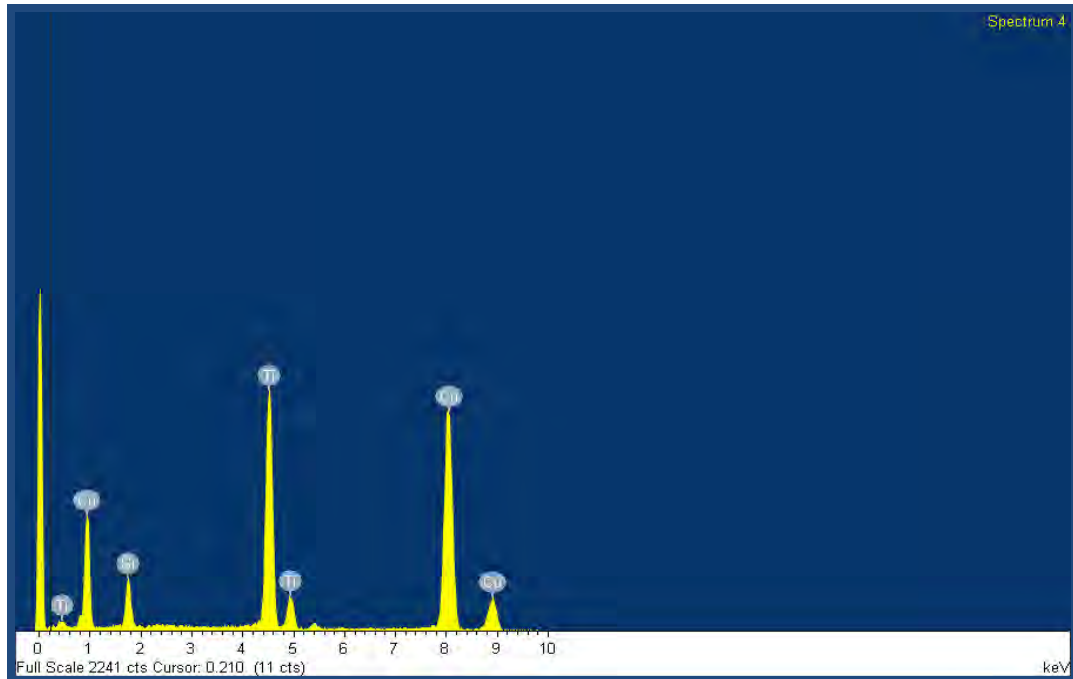


Figure 2.5.40: EDX spectrum of Ti-Cu layer at position 4 of Figure 2.5.37.

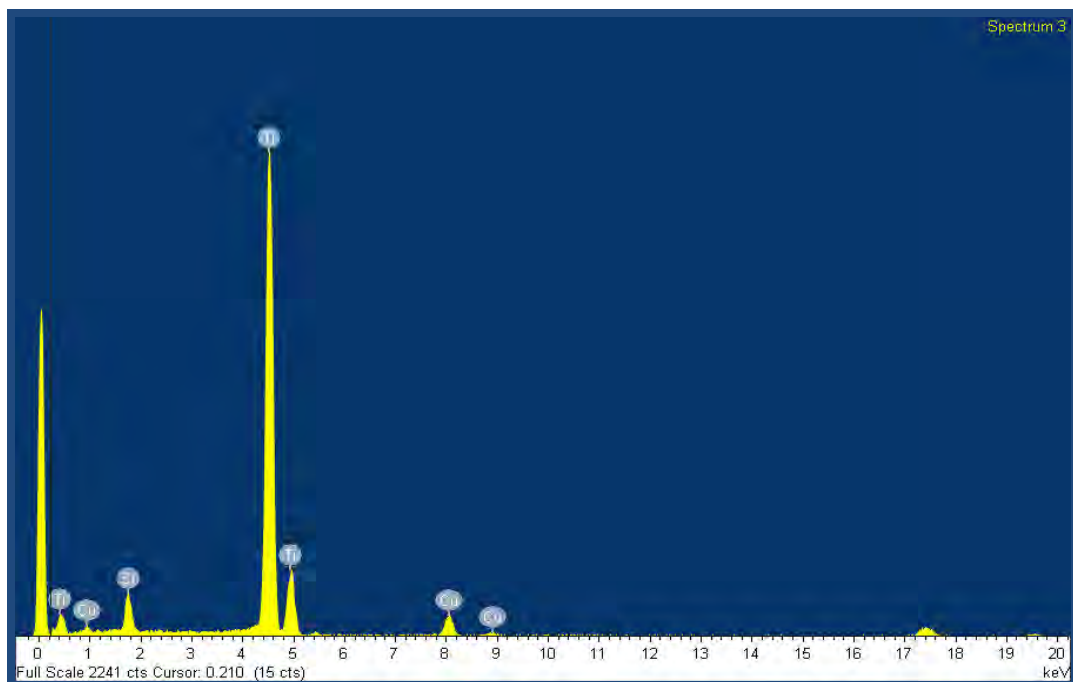


Figure 2.5.41: EDX spectrum of Ti layer at position 3 of Figure 2.5.37.

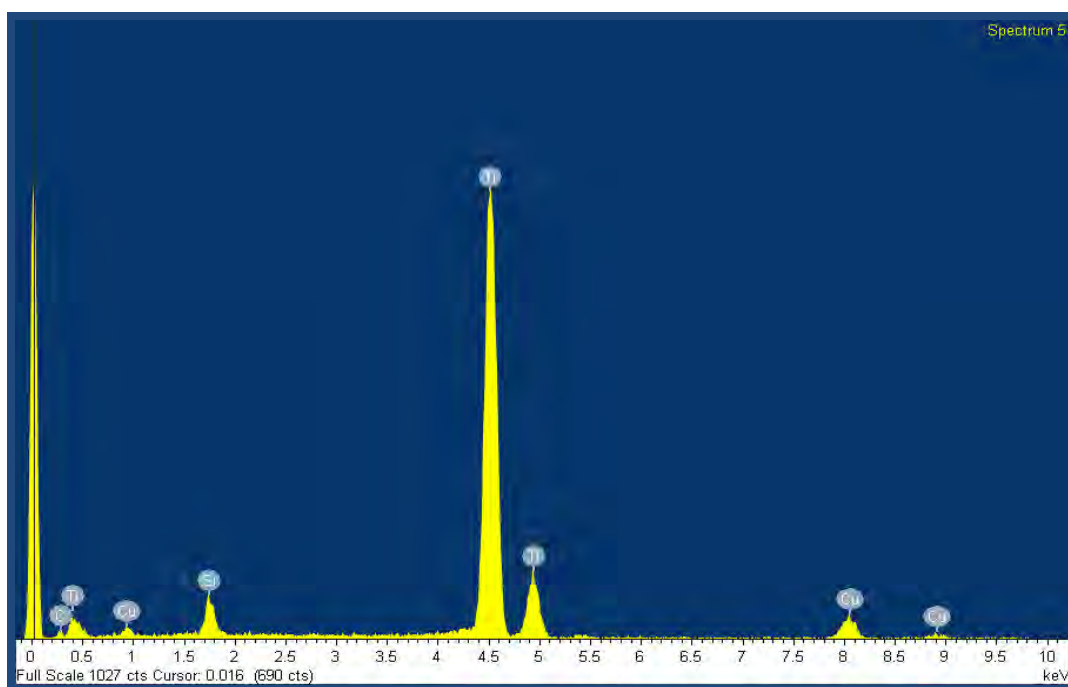


Figure 2.5.42: EDX spectrum Ti layer at position 5 of Figure 2.5.37.

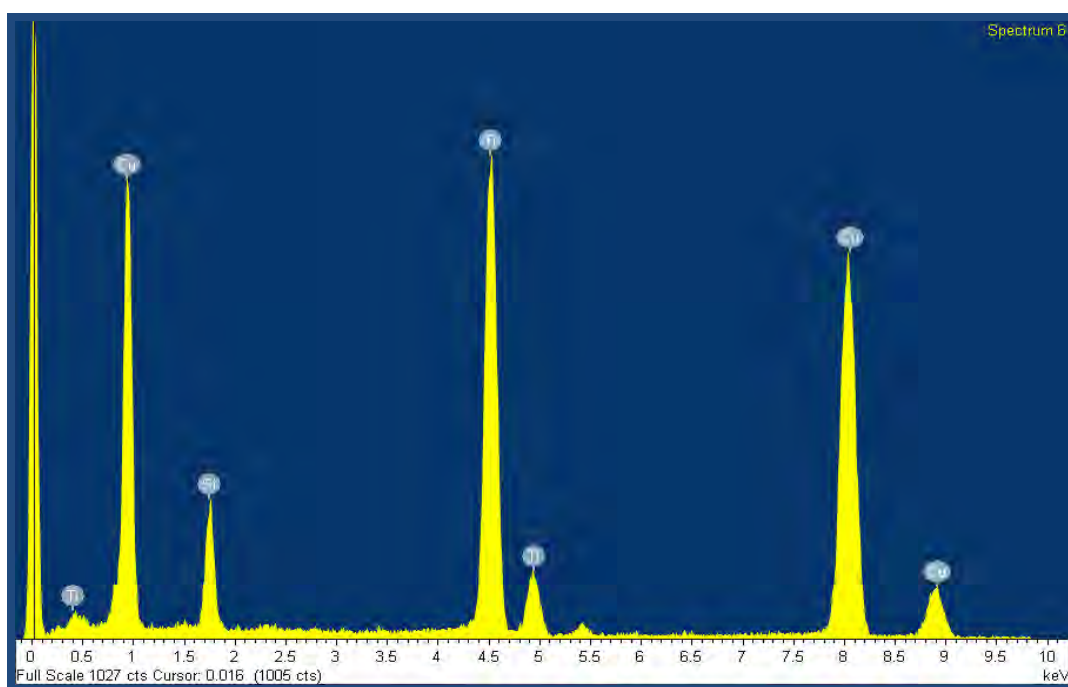


Figure 2.5.43: EDX spectrum of Ti-Cu layer at position 6 of Figure 2.5.37.

Feature	Pitch	Width	THK
Metal 0	90 nm	50 nm	50 nm
Metal 1	92 nm	55 nm	95 nm
Metal 2	81 nm	55 nm	80 nm
Metal 3	101 nm	65 nm	75 nm
Metal 4	112 nm	70 nm	110 nm
Metal 5	165 nm	100 nm	150 nm
Metal 6	242 nm	140 nm	270 nm
Metal 7	362 nm	210 nm	260 nm
Metal 8	363 nm	230 nm	450 nm
Metal 9	13.85 μm	7.85 μm	6.40 μm

Table 2.5.1: Metallization dimensions determined by SEM cross-section.

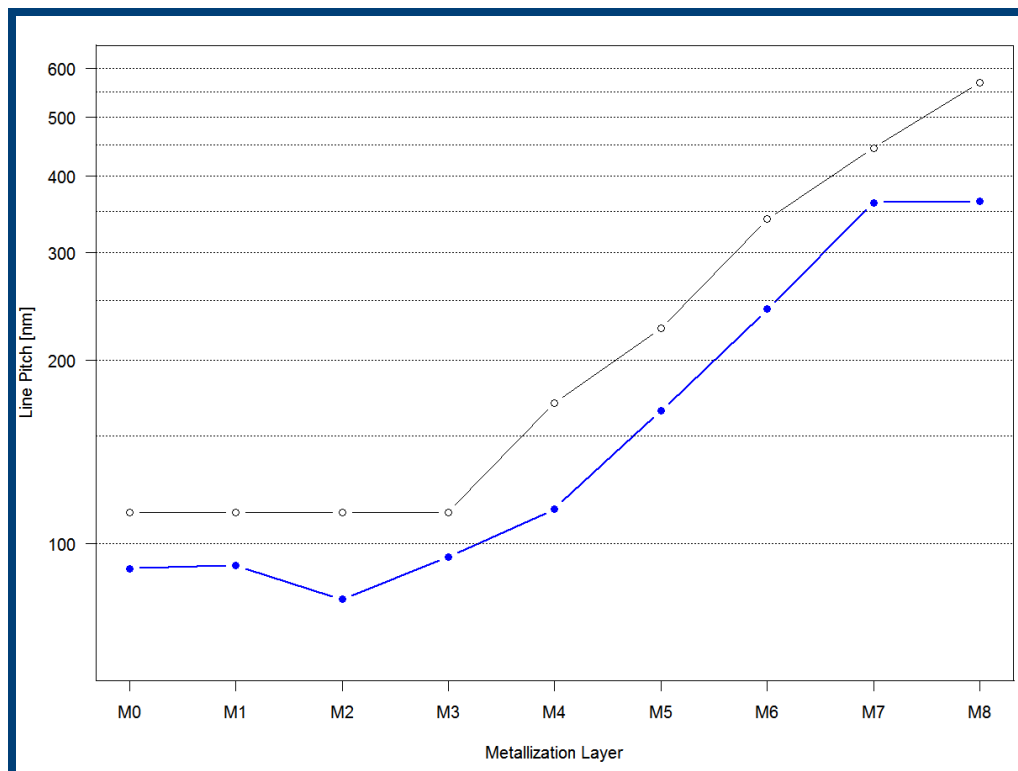


Figure 2.5.44: The pitches for metal 0 to metal 8 for the Intel 22 nm (blue) and 32 nm processor.

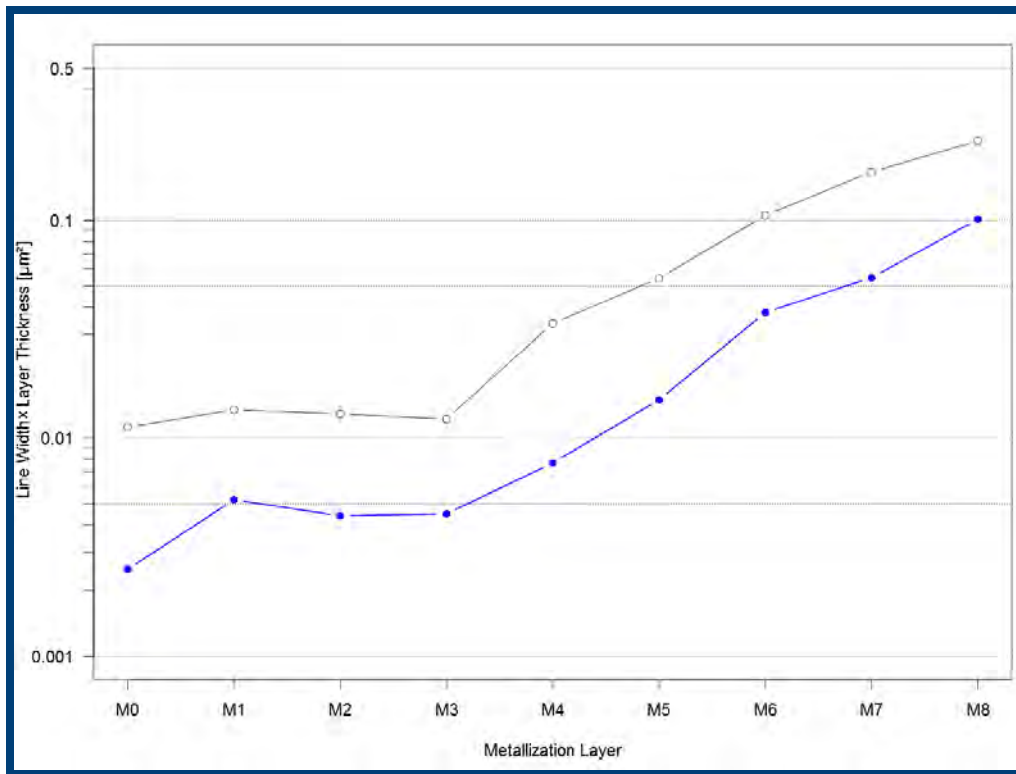


Figure 2.5.45: The cross-sectional areas for metal 0 to metal 8 for the Intel 22 nm (blue) and 32 nm processor.

Comments

- One tungsten and nine copper-based metallization levels;
- Tungsten dual damascene M0 local interconnect;
- M2 pitch is the smallest metal pitch;
- Confirmed Ta/TaN barrier for M1, M2, M5, M7, and concluded for M3, M4, M6, and M8;
- Ti liner for M9.
- TEM EDX reveals silicon doped copper for M1, M2, M5, M6, M7, and M9. The estimated silicon amount would be in the lower single percentage range, but neither it can be yet confirmed that silicon is present in the copper not that this is an artifact of the materials analysis.
- Aluminum is found at the copper-dielectric capping layer for M1, M2, and M5 which is most likely used to reduce electromigration.
- Likely a self aligned barrier process with metal organic vapour deposition (MOCVD) is used to form xxxx at the copper-cap interface;
- An additional metal inter-layer is found between M8 and M9, which is likely used as decoupling capacitors;
- Non-damascene copper-based metal 9 is likely formed by masked plating.



Figure 2.5.46: Metal 8/9 interlayer.

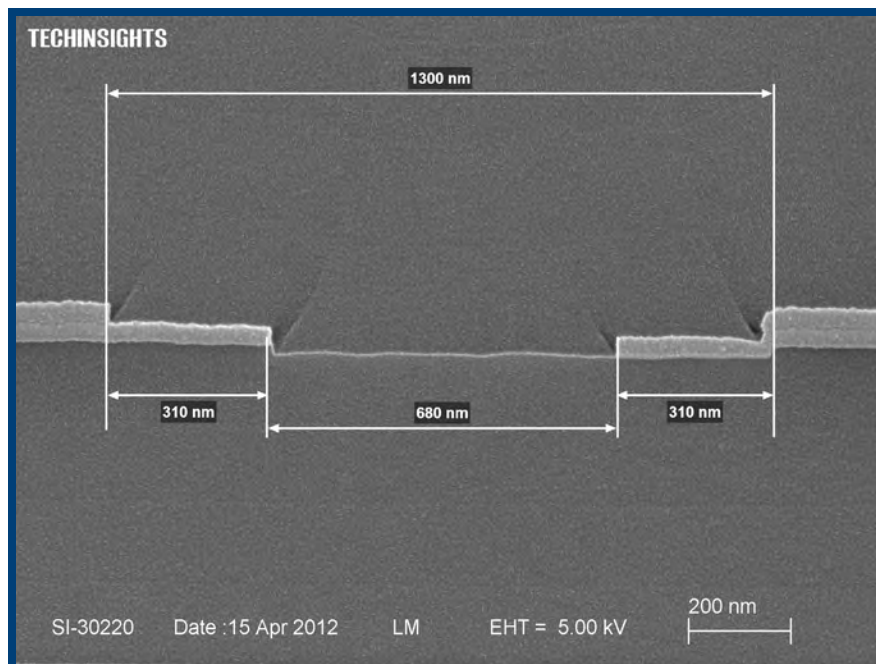


Figure 2.5.47: Metal 8/9 interlayer; SEM cross-section.

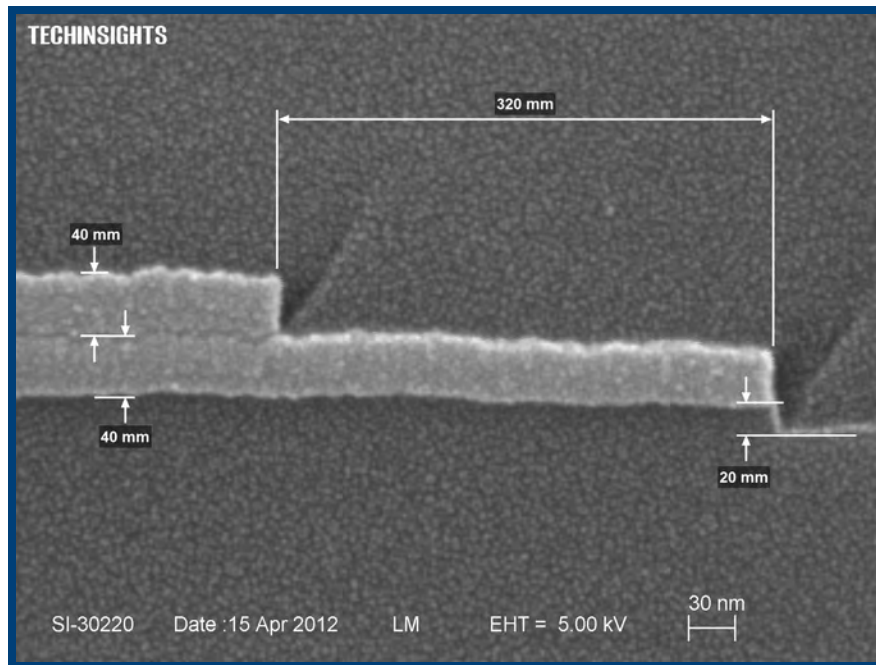


Figure 2.5.48: Metal 8/9 interlayer; SEM cross-section.

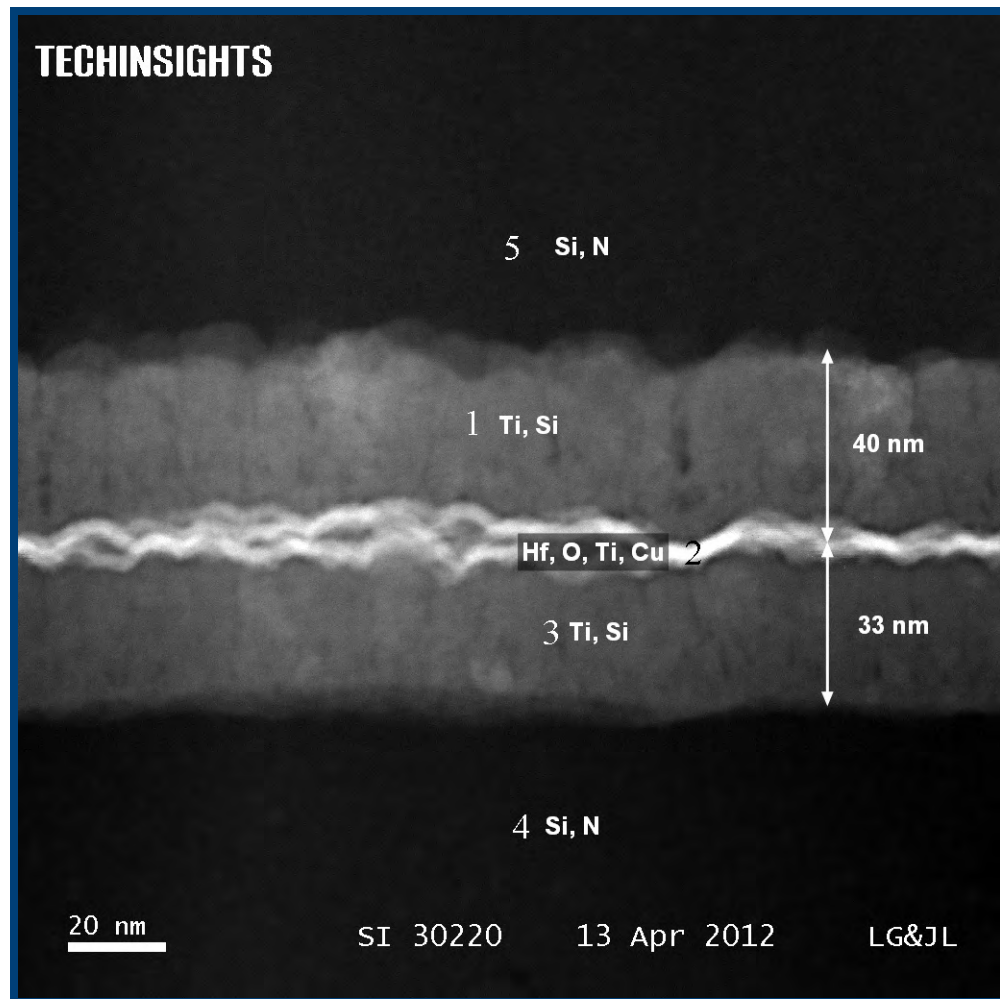


Figure 2.5.49: EDX analysis results for metal 8/9 interlayer; HAADF TEM cross-section.

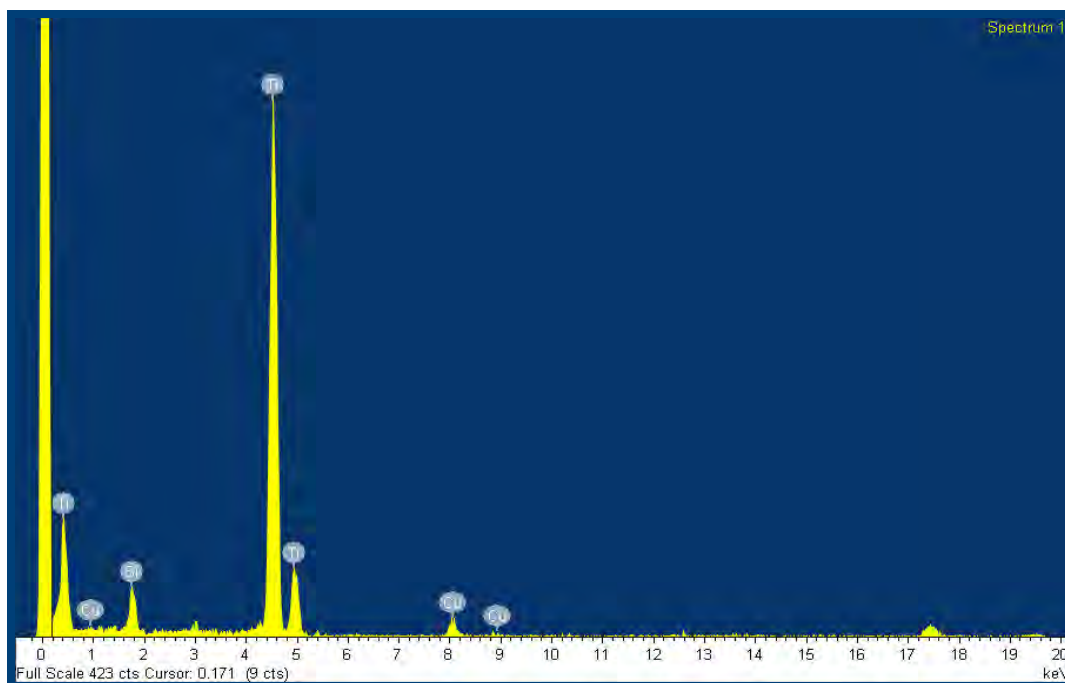


Figure 2.5.50: EDX spectrum of upper TiN layer at position 1 of Figure 2.5.49.

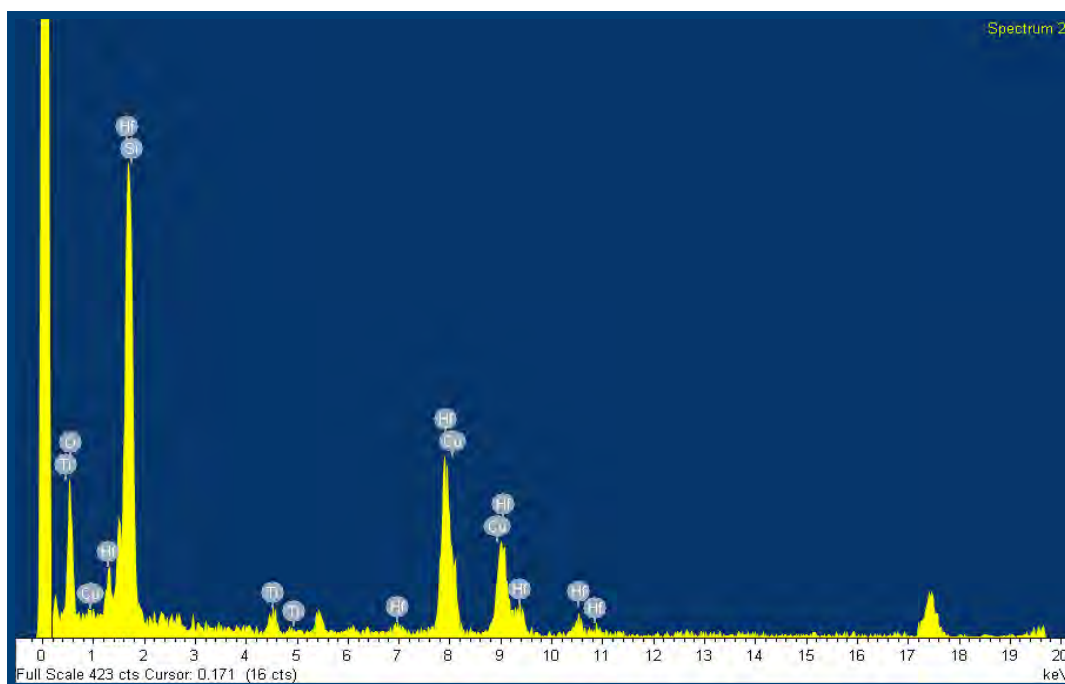


Figure 2.5.51: EDX spectrum of HfO at position 2 of Figure 2.5.49.

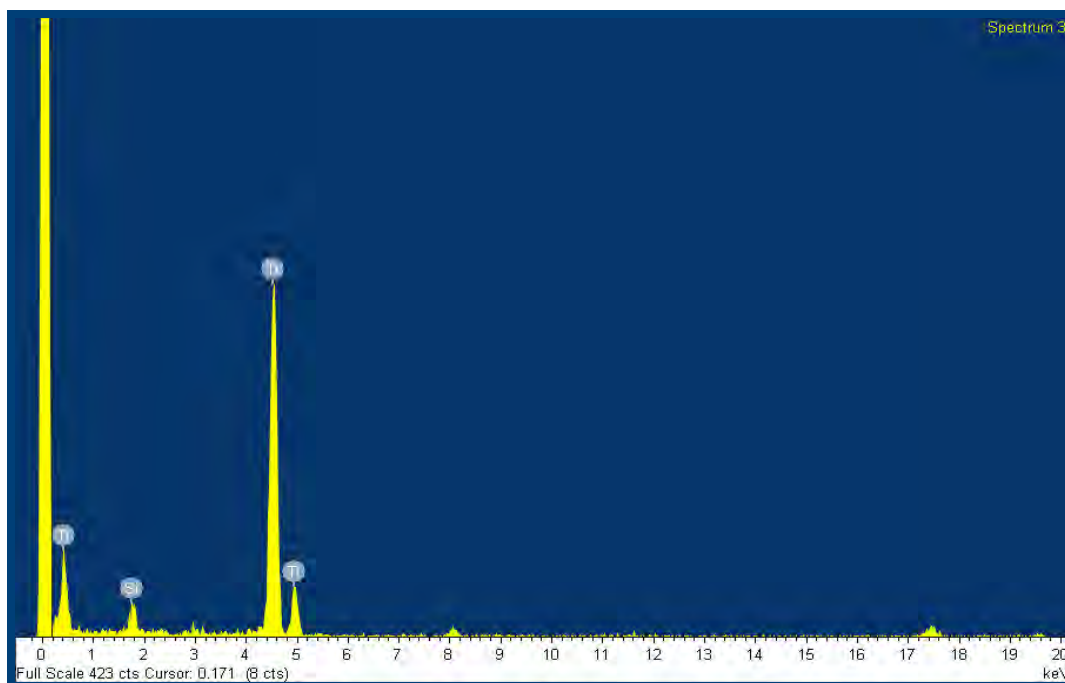


Figure 2.5.52: EDX spectrum of lower TiN layer at position 3 of Figure 2.5.49.

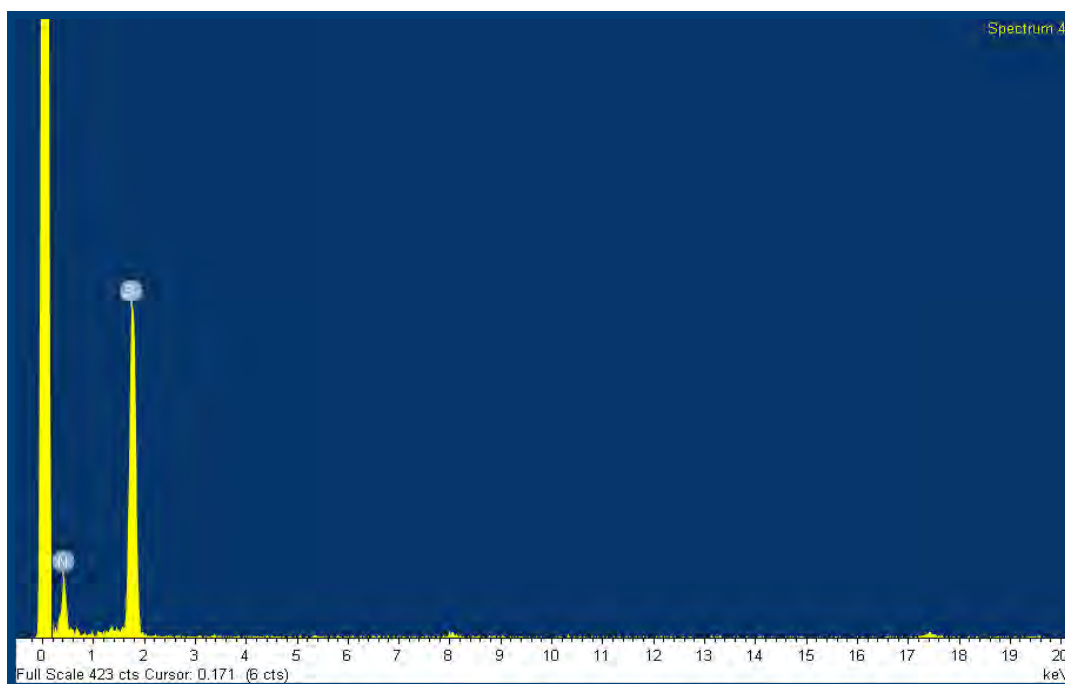


Figure 2.5.53: EDX spectrum of SiCN at position 4 of Figure 2.5.49.

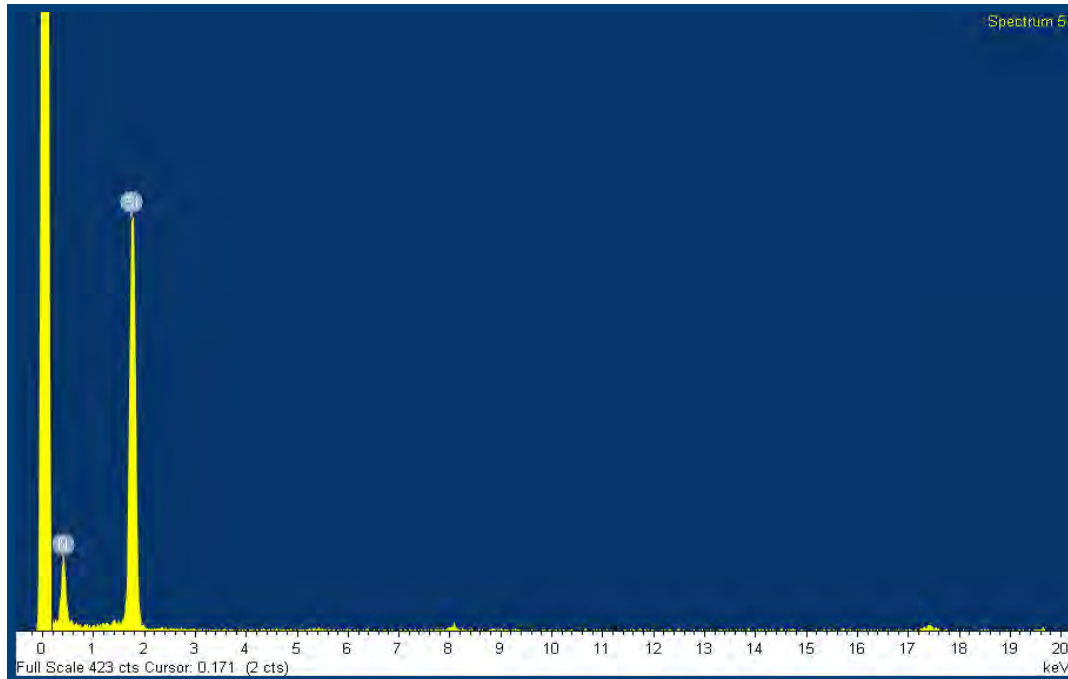


Figure 2.5.54: EDX spectrum of SiCN at position 5 of Figure 2.5.49.

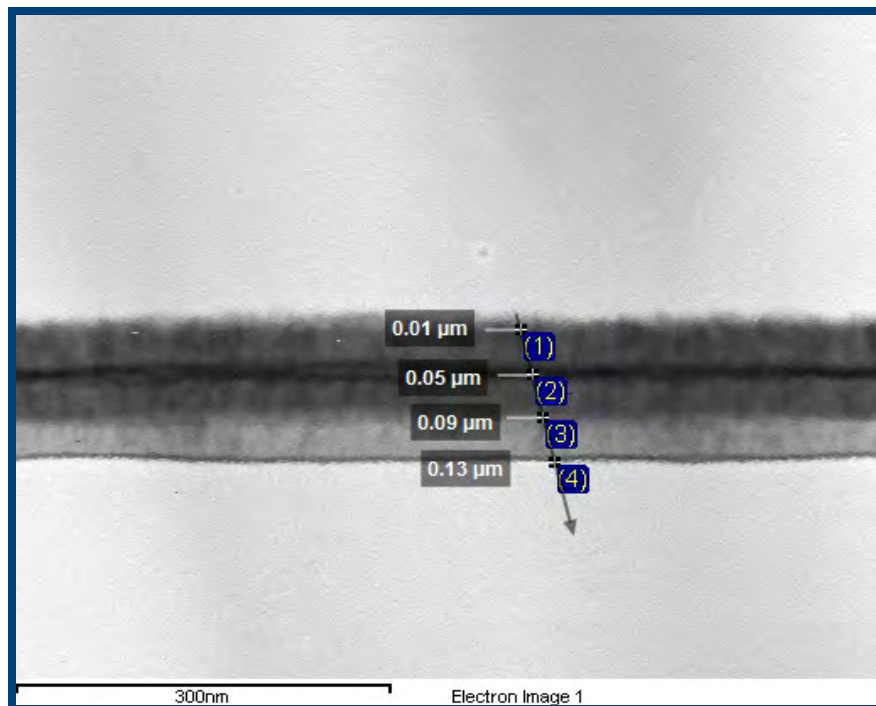


Figure 2.5.55: Location of the EDX point-ID scan through the M8/9 metal inter-layer.

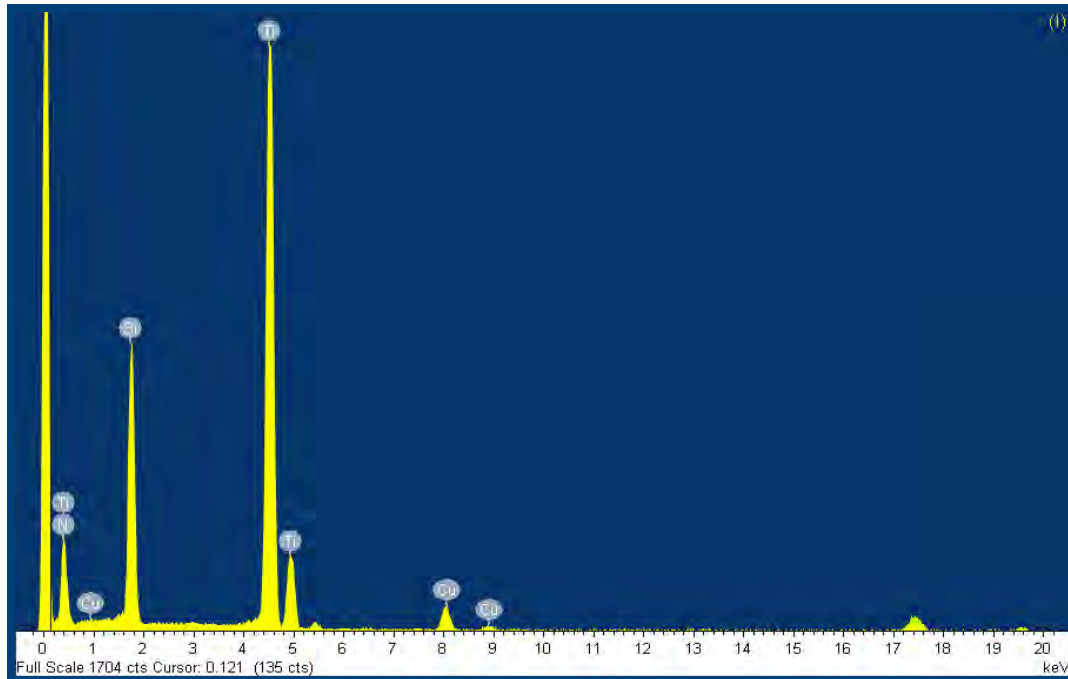


Figure 2.5.56: EDX spectrum of TiN layer at position 1 of Figure 2.5.55.

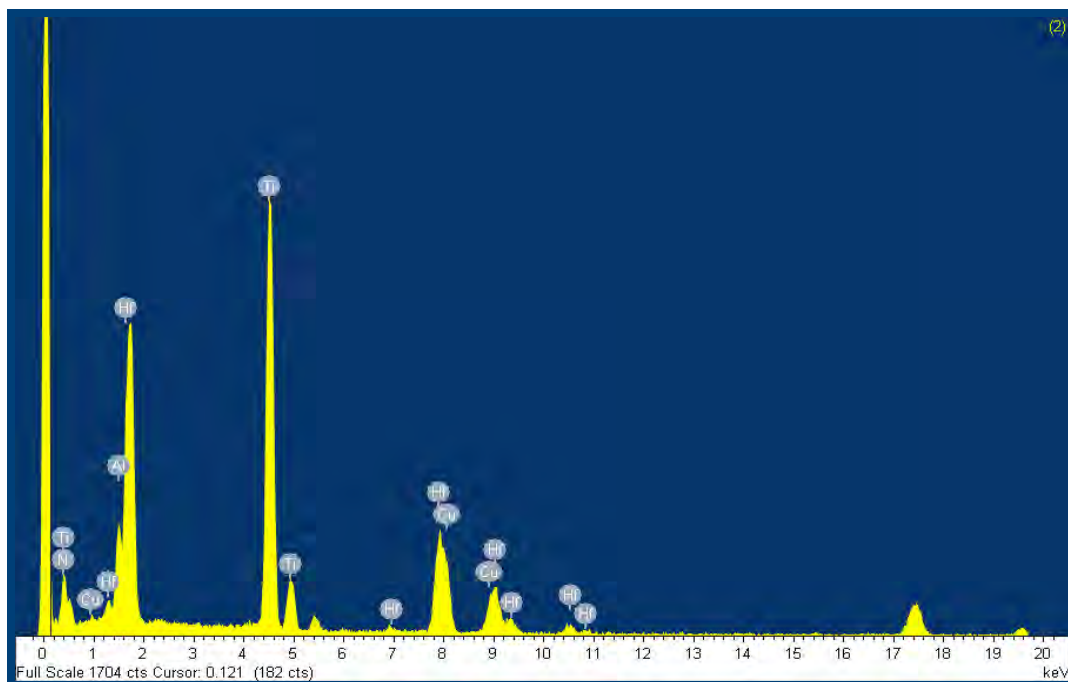


Figure 2.5.57: EDX spectrum of HfO layer at position 2 of Figure 2.5.55.

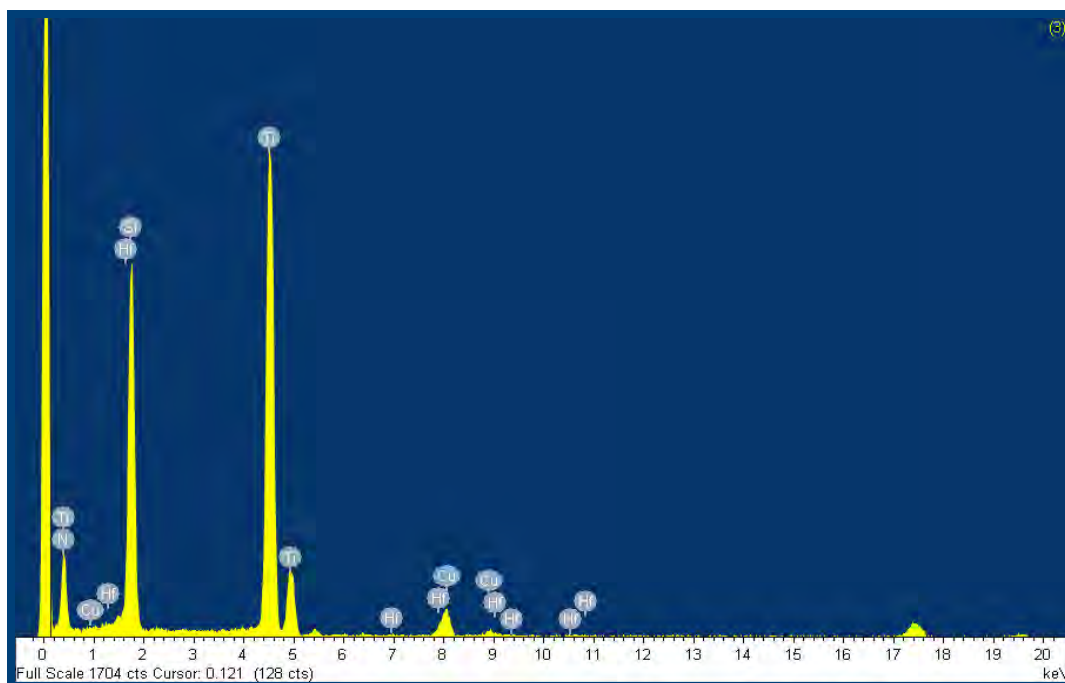


Figure 2.5.58: EDX spectrum at position 3 of Figure 2.5.55.

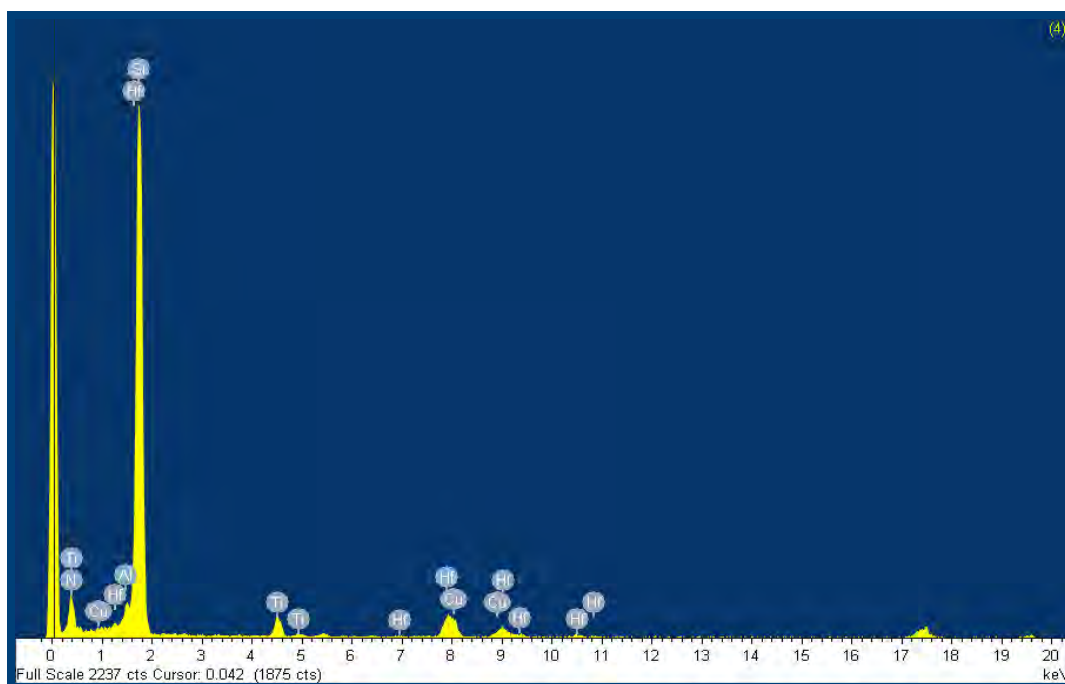


Figure 2.5.59: EDX spectrum of SiCN at position 4 of Figure 2.5.55.

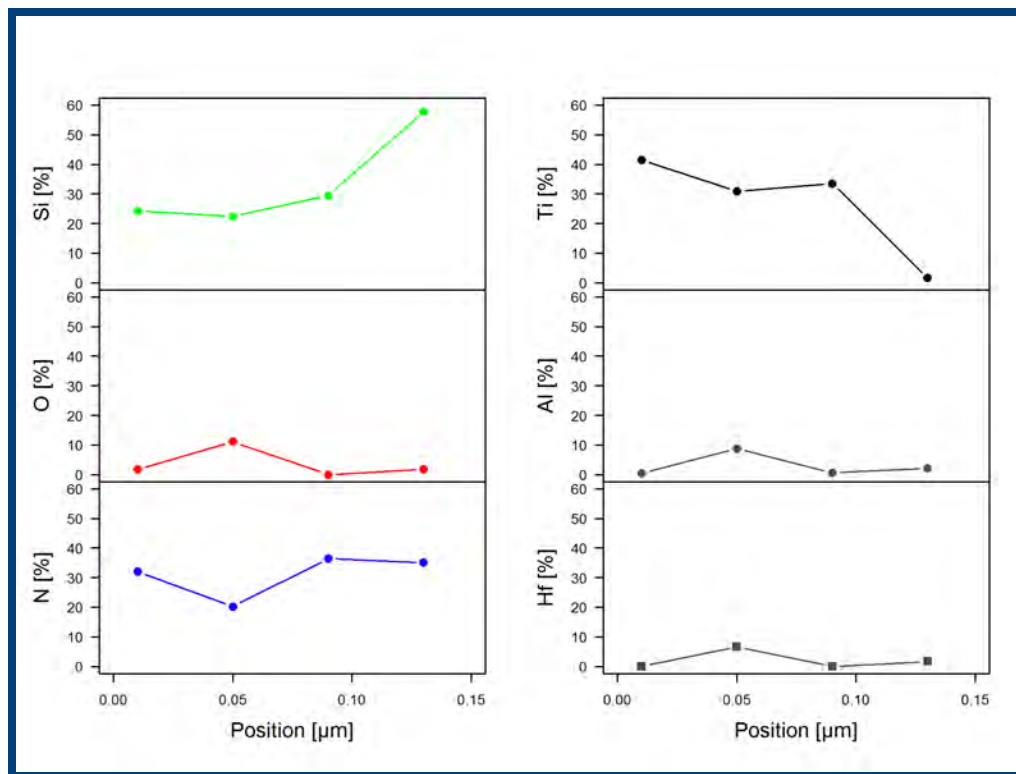


Figure 2.5.60: The results of the EDX point-ID scan through the M8/9 metal inter-layer. The intensities are normalized to 100 % for the shown elements.

Comments

- The top and bottom plates of the M8/9 metal inter-layer contain TiN;
- The dielectric contains aluminum and hafnium;
- With these results it cannot be distinguished if the titanium signal found in the dielectric comes from the dielectric itself or if it comes from the TiN;
- From the analysis by SEM and TEM cross-sections it is concluded that the M8/9 metal interlayer is electrically connected to via 8 and functions as decoupling capacitors.

2.6 Inter-Metal Dielectrics (IMD) and Vias

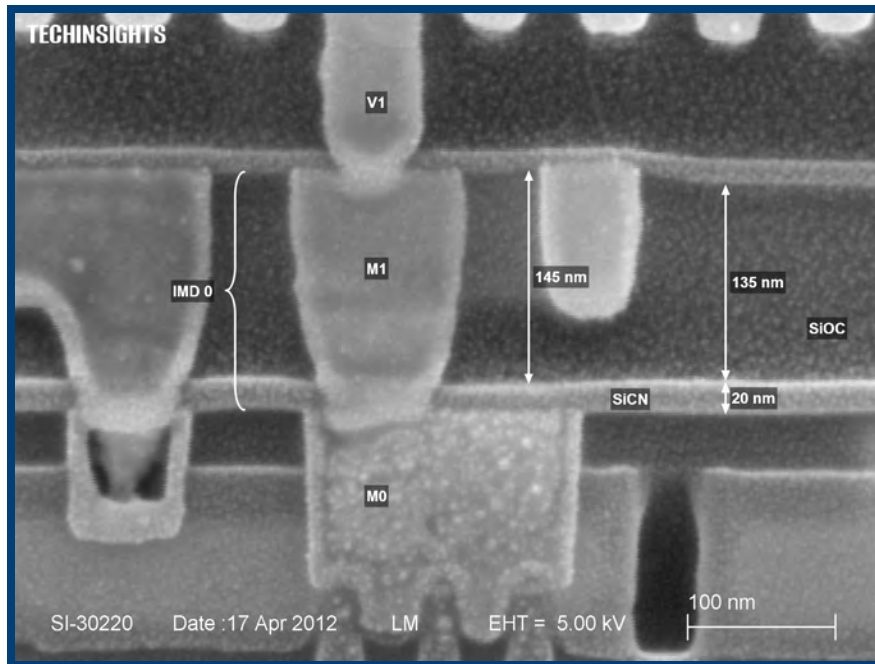


Figure 2.6.1: IMD 0; SEM cross-section.

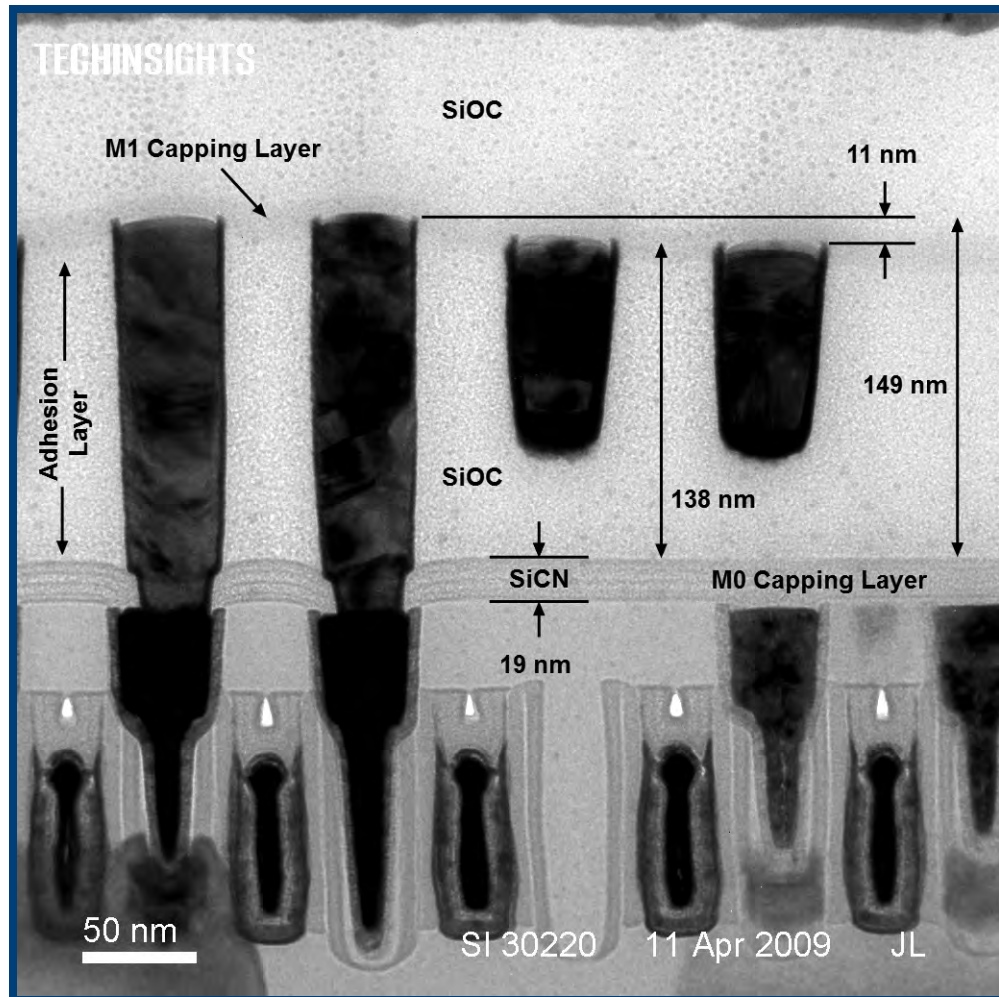


Figure 2.6.2: IMD 0; TEM cross-section.

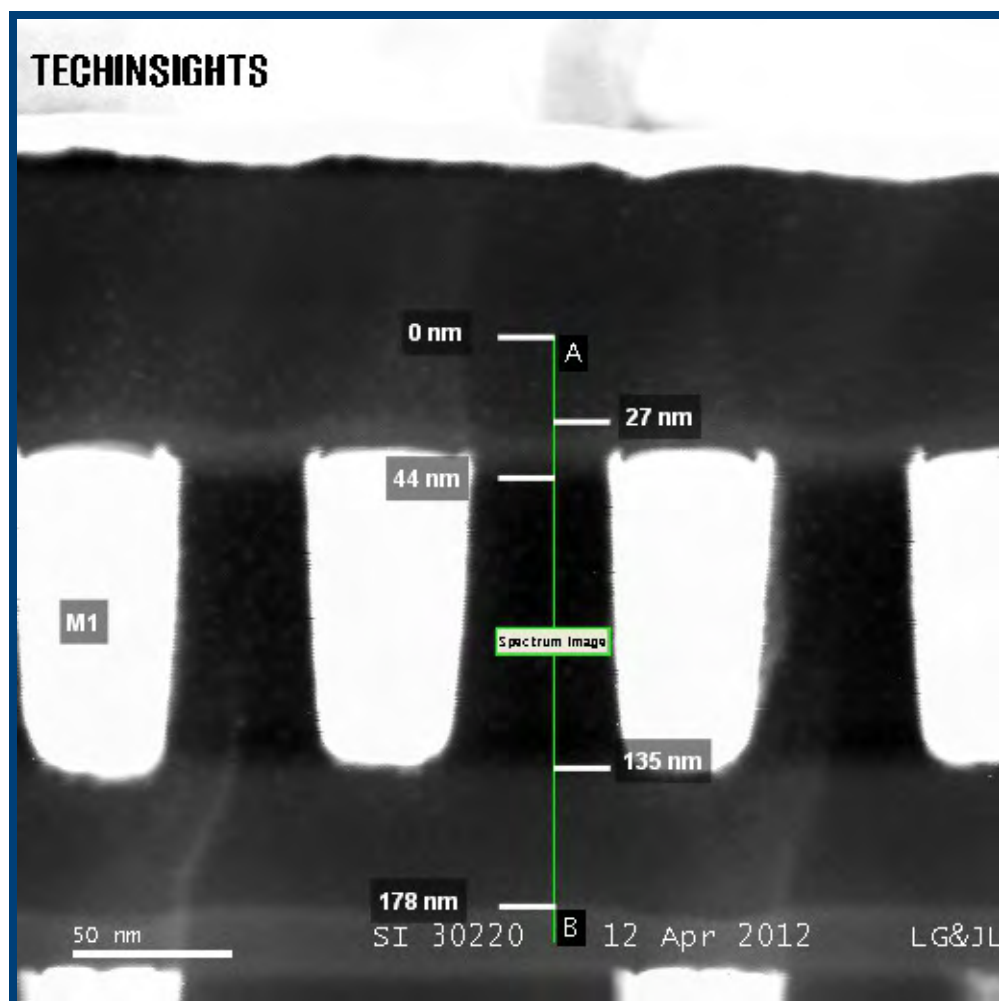


Figure 2.6.3: Location of the EELS line scan through IMD 0.

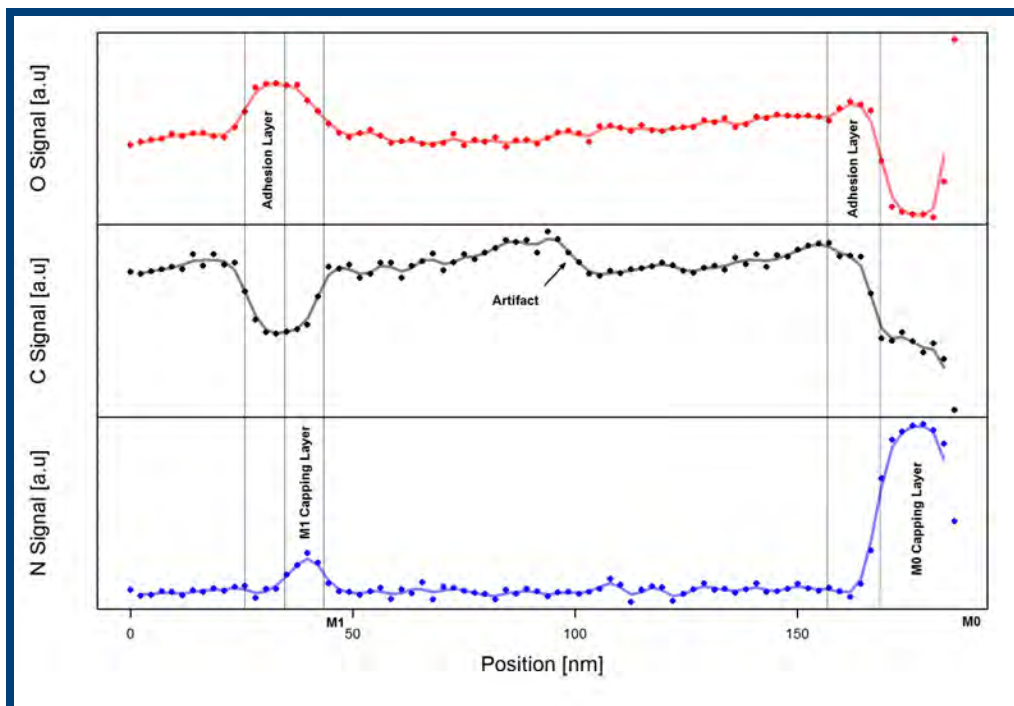


Figure 2.6.4: Results of the EELS line scan shown in Figure 2.6.3.

Comments

- The capping layer on top of M0 is SiCN (positions > 160 nm in Figure 2.6.4);
- On top of the M0 capping layer (approx. 155 – 165 nm) the oxygen signal increases and the carbon decreases indicating an oxide adhesion layer on top of M0;
- In the carbon-doped oxide (approx. 145 – 155 nm) a step profile is found which is concluded to be an artifact of the TEM sample thickness;
- Once the M1 capping layer starts (approx. 45 – 35 nm) the nitrogen signal increases, but not as strong as for the M0 capping layer, and carbon and oxygen are still present. Hence the M1 capping layer is a SiOCN layer;
- On top of the M1 SiOCN capping layer (25 – 35 nm) the oxygen signal remains high and the carbon signal remains low indicating an oxide adhesion layer on top of M1 capping layer.

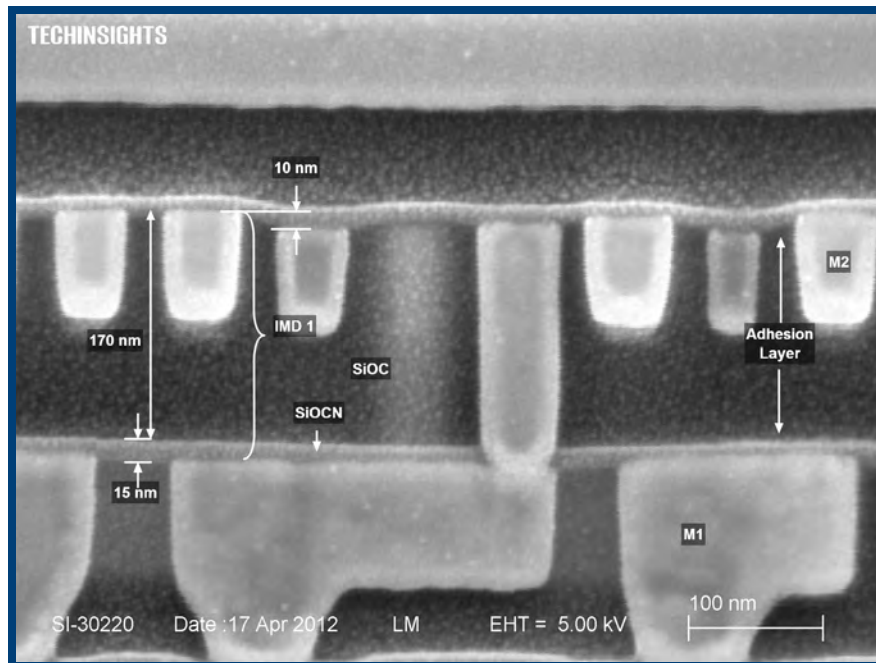


Figure 2.6.5: IMD 1; SEM cross-section.

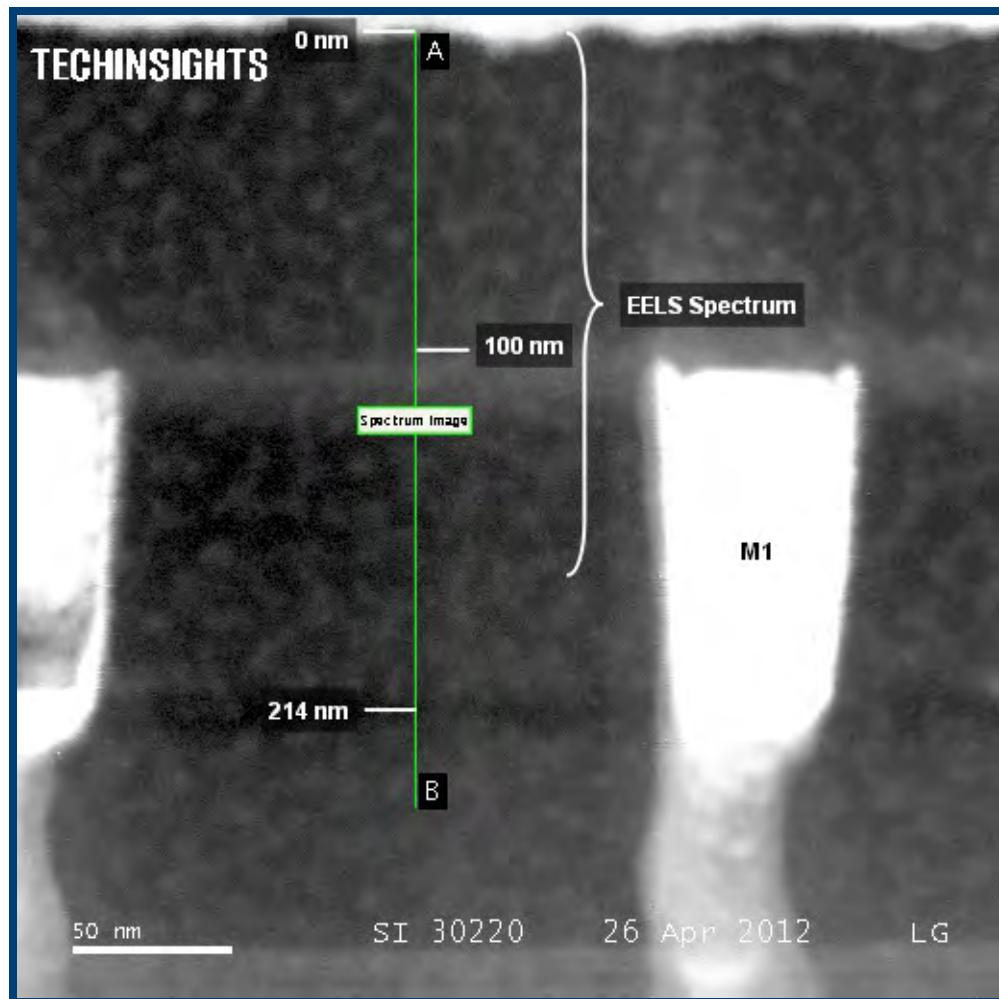


Figure 2.6.6: Location of the EELS line scan through the M1 capping layer.

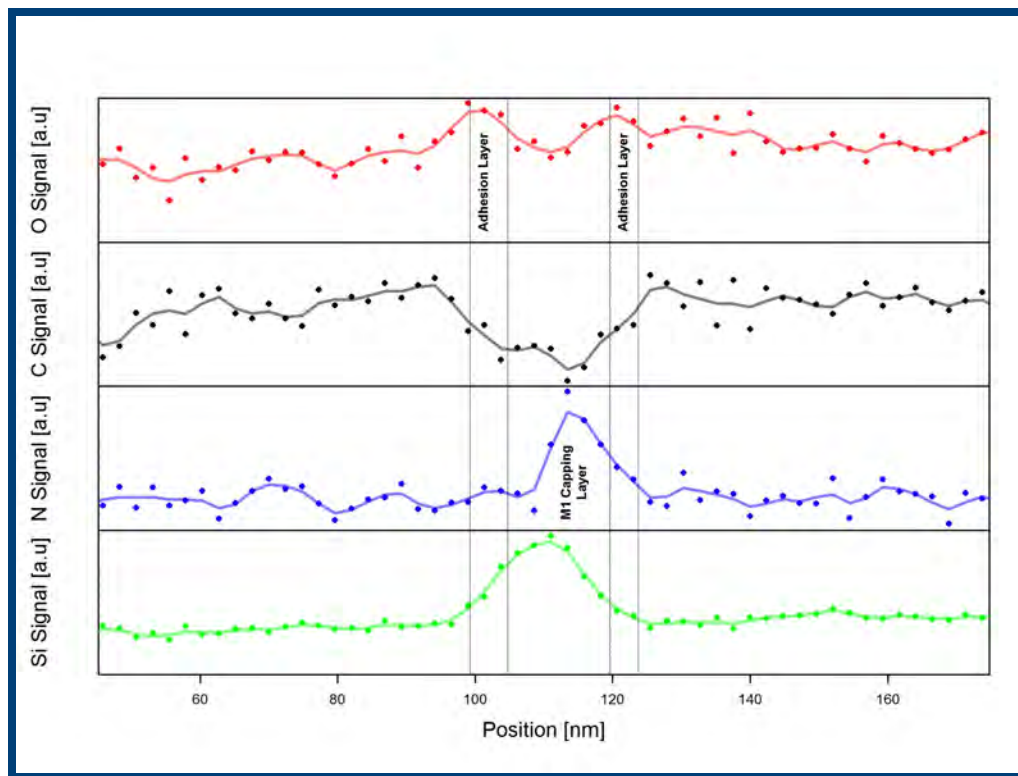


Figure 2.6.7: The results of the EELS line scan through the M1 capping layer shown in Figure 2.6.6.

Comments

- The EELS line scan through the M1 capping layer is a SiOCN capping layer;
- Despite weak EELS signals it can be concluded that the EEELS data indicate the presence of an adhesion or densified oxide layer under the M1 capping layer and an adhesion on top of the M1 capping layer.

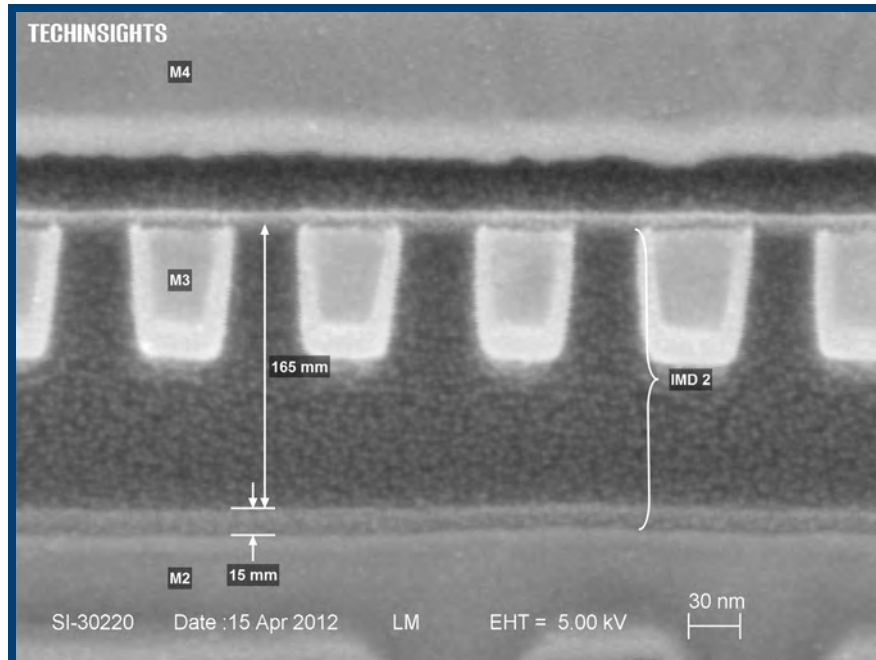


Figure 2.6.8: IMD 2; SEM cross-section.

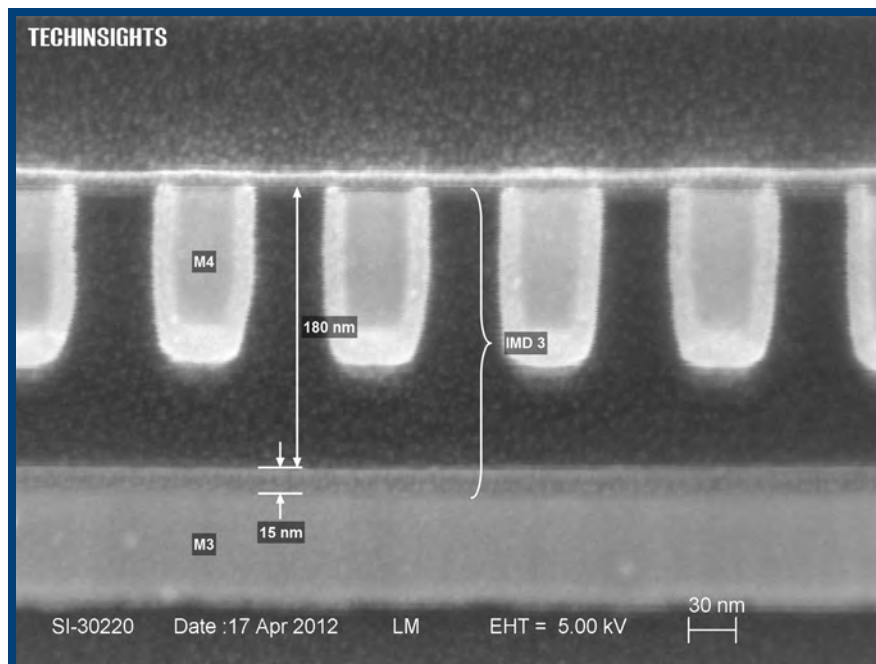


Figure 2.6.9: IMD 3; SEM cross-section.

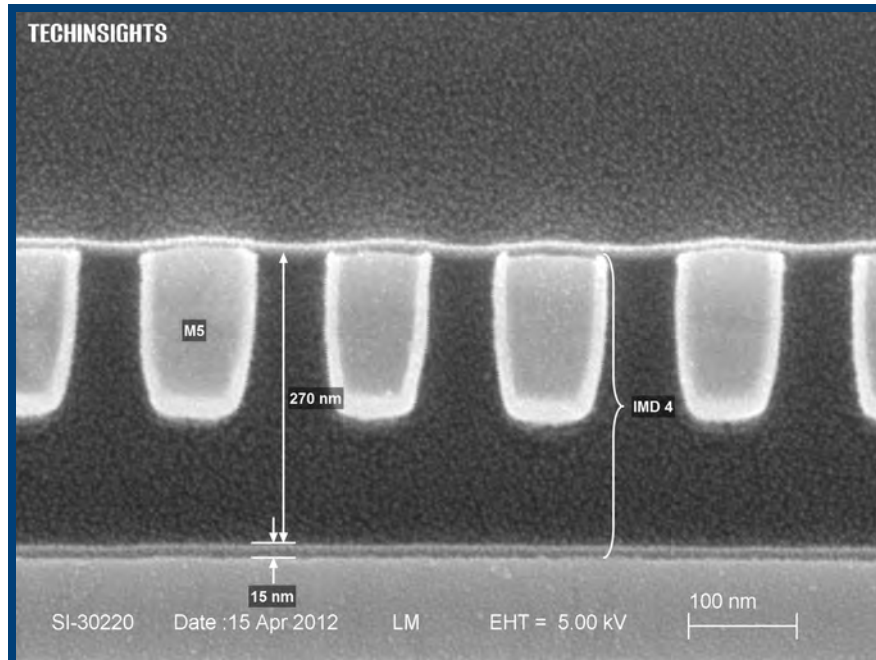


Figure 2.6.7: IMD 4; SEM cross-section.

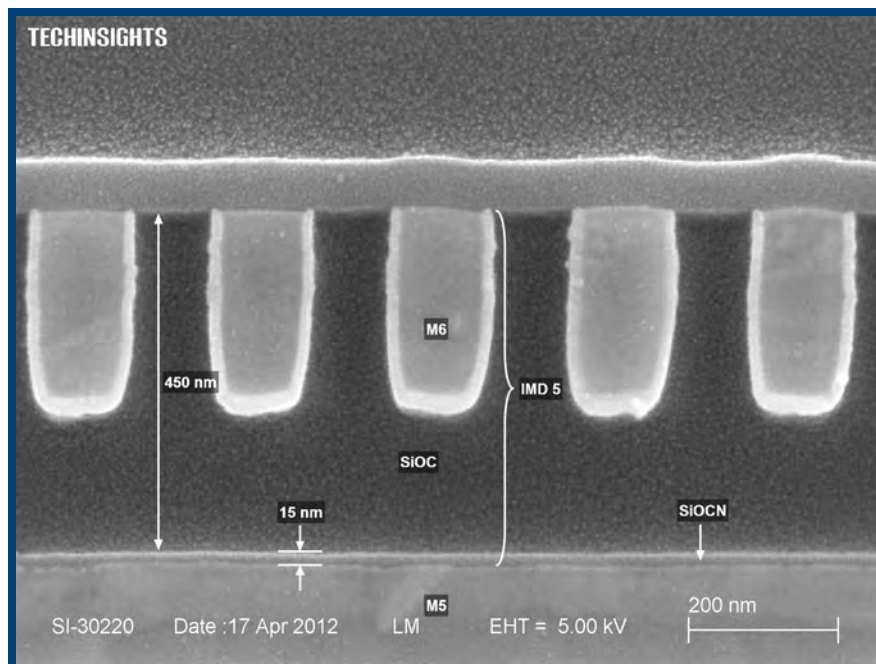


Figure 2.6.8: IMD 5; SEM cross-section.

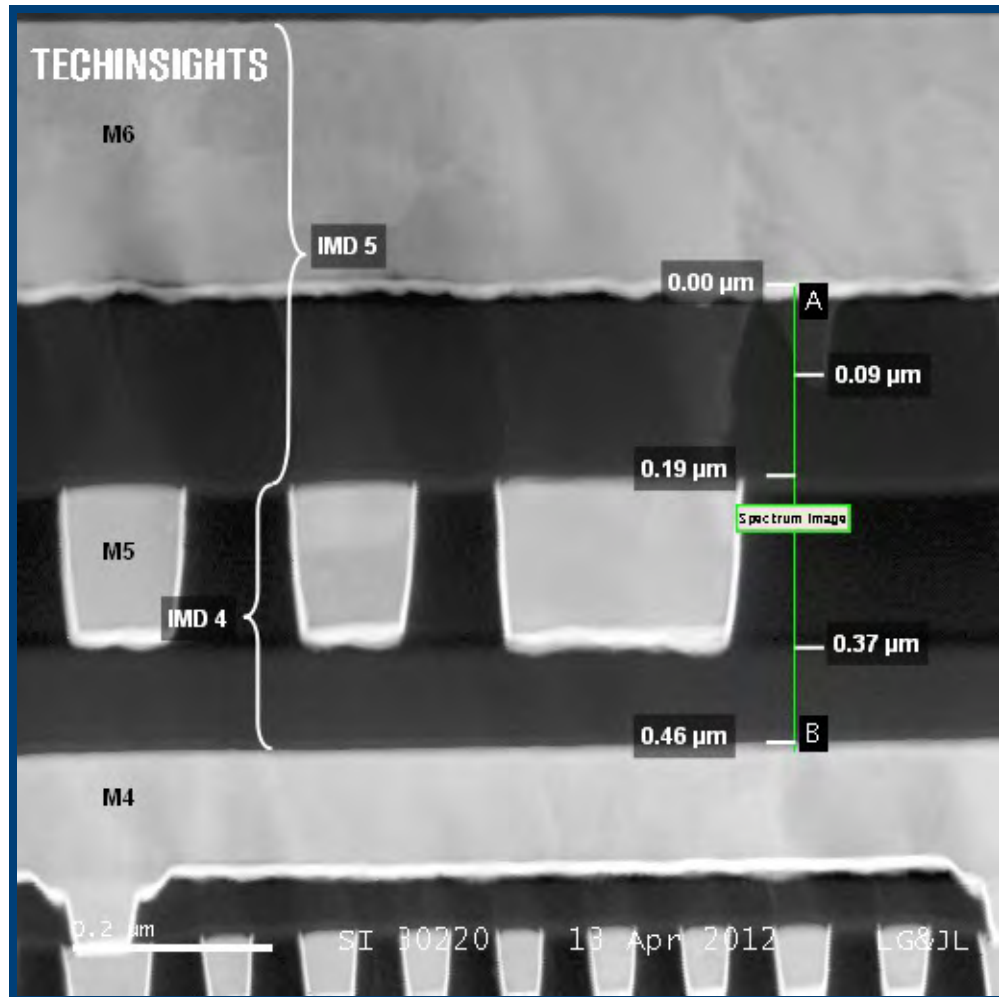


Figure 2.6.9: Location of the EELS line scan through IMD 4 and portions of IMD 5.

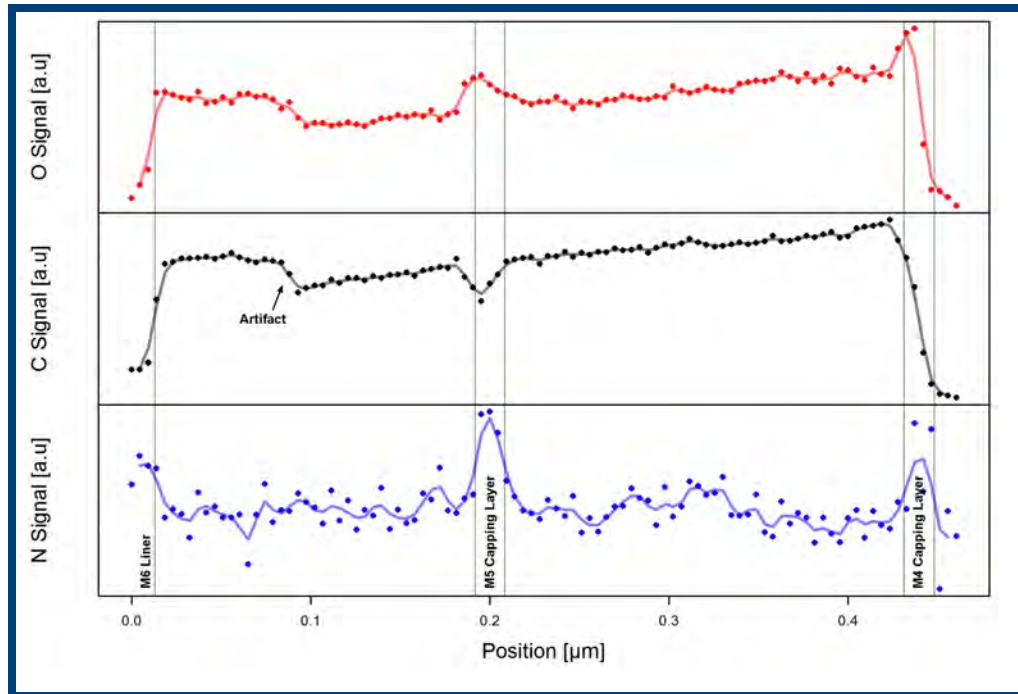


Figure 2.6.10: The results of the EELS line scan shown in Figure 72.

Comments

- The asymmetric oxygen signal profile may indicate low carbon adhesion / densified layer underneath and an adhesion layer on top of the M5 capping layer;
- The M5 capping layer is SiOCN;
- The IMD 5 SiOC dielectric shows a substructure in the oxygen and the carbon EELS signal which is concluded to be an artifact of the TEM sample thickness.

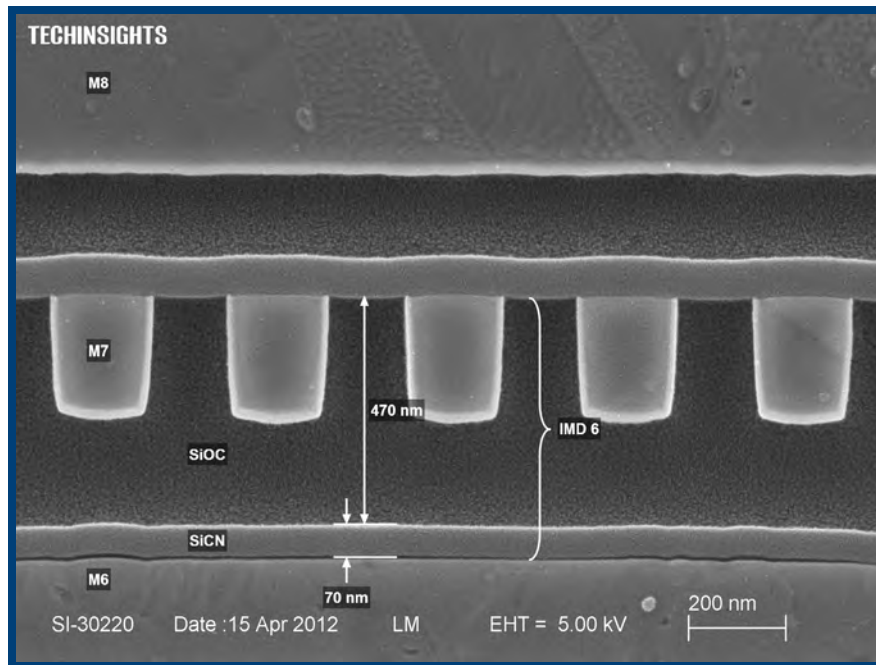


Figure 2.6.11: IMD 6; SEM cross-section.

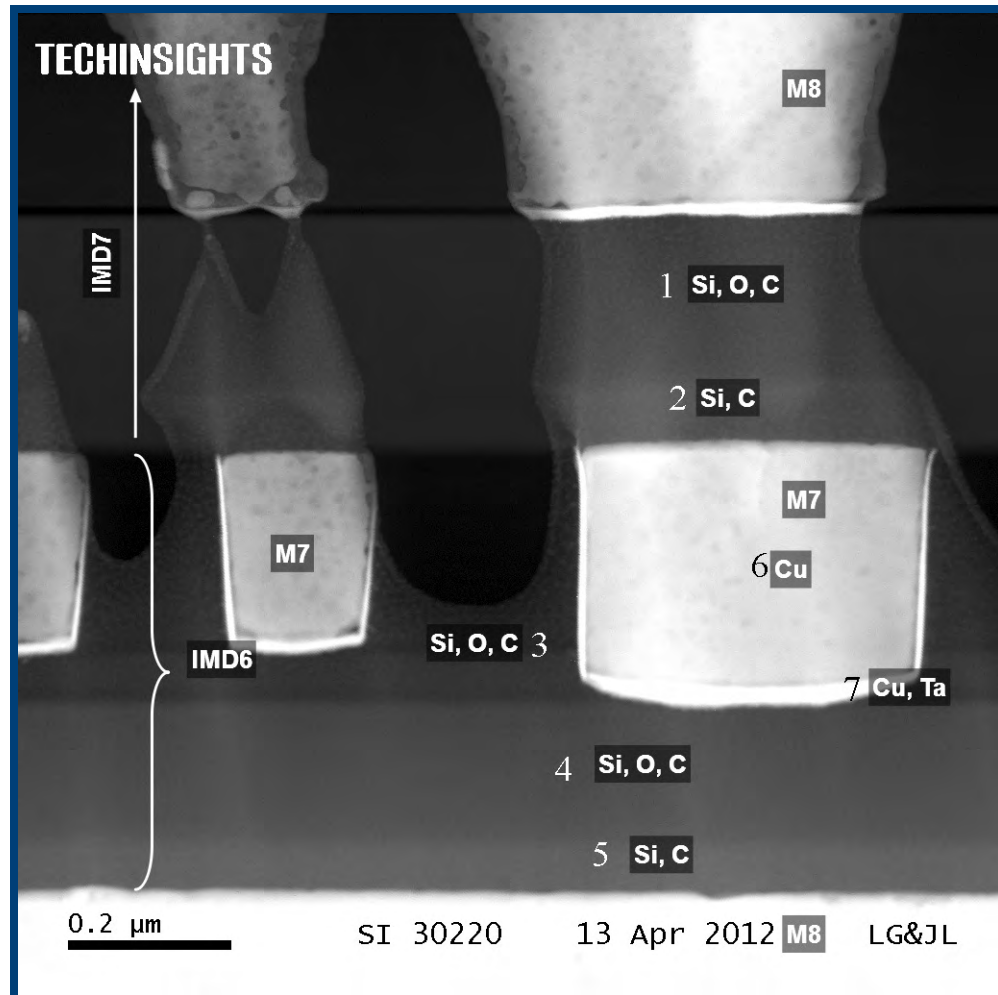


Figure 2.6.12: EDX analysis results for inter-metal dielectric 6, the lower portion of inter-metal dielectric 7, and metal 7; HAADF TEM cross-section.

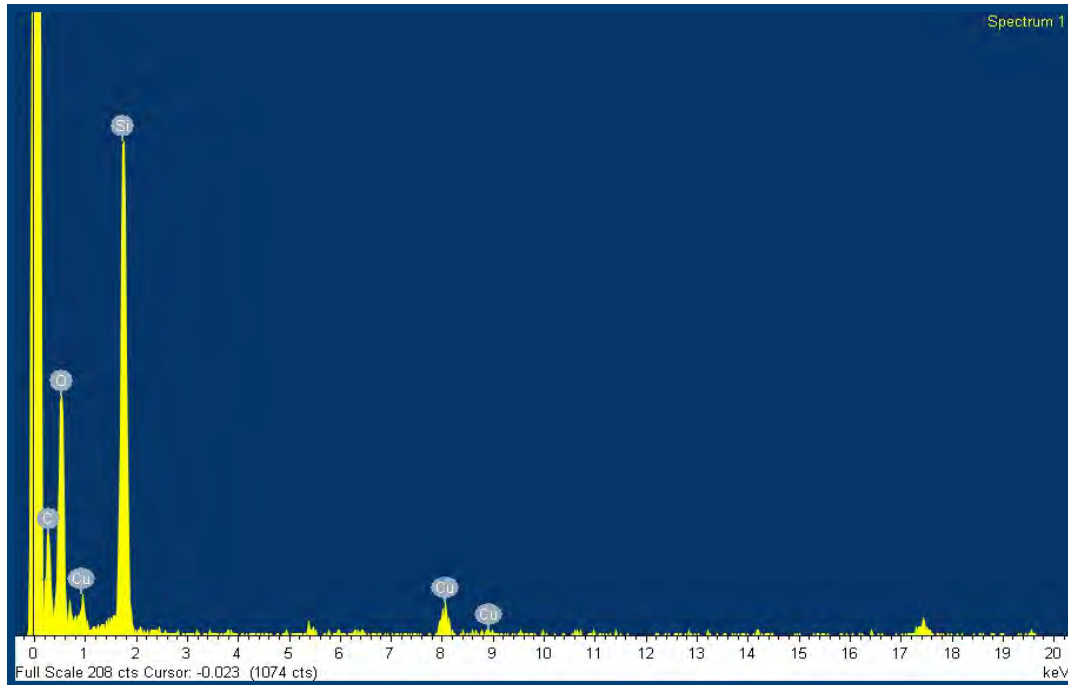


Figure 2.6.13: EDX spectrum of SiOC layer at position 1 of Figure 2.6.12.

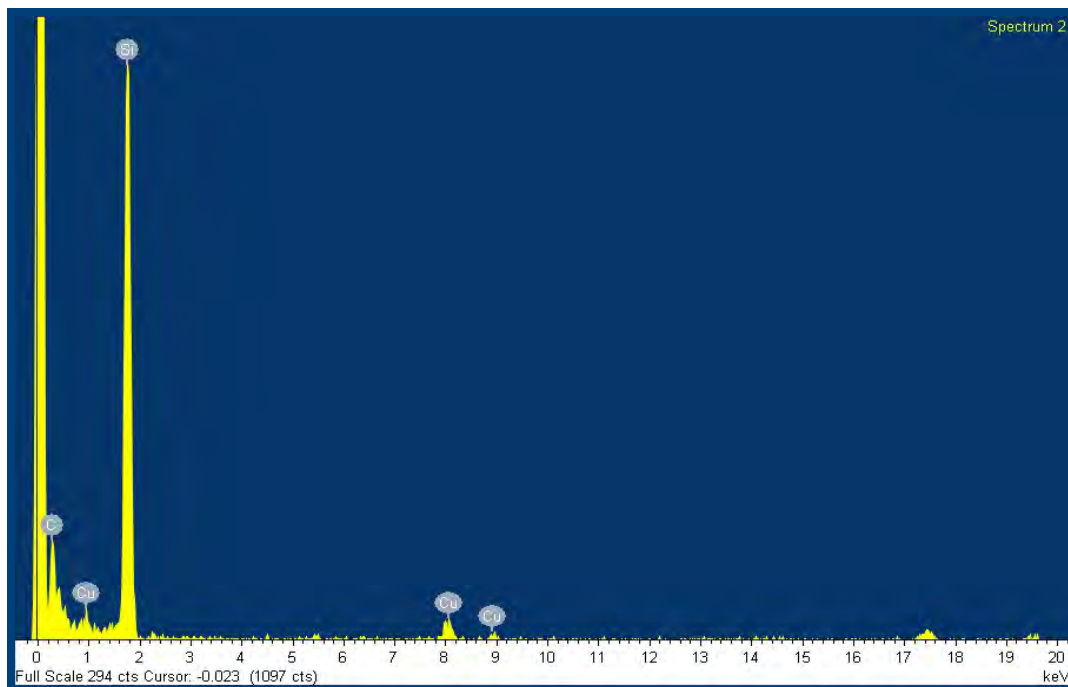


Figure 2.6.14: EDX spectrum of SiCN layer at position 2 of Figure 2.6.12.

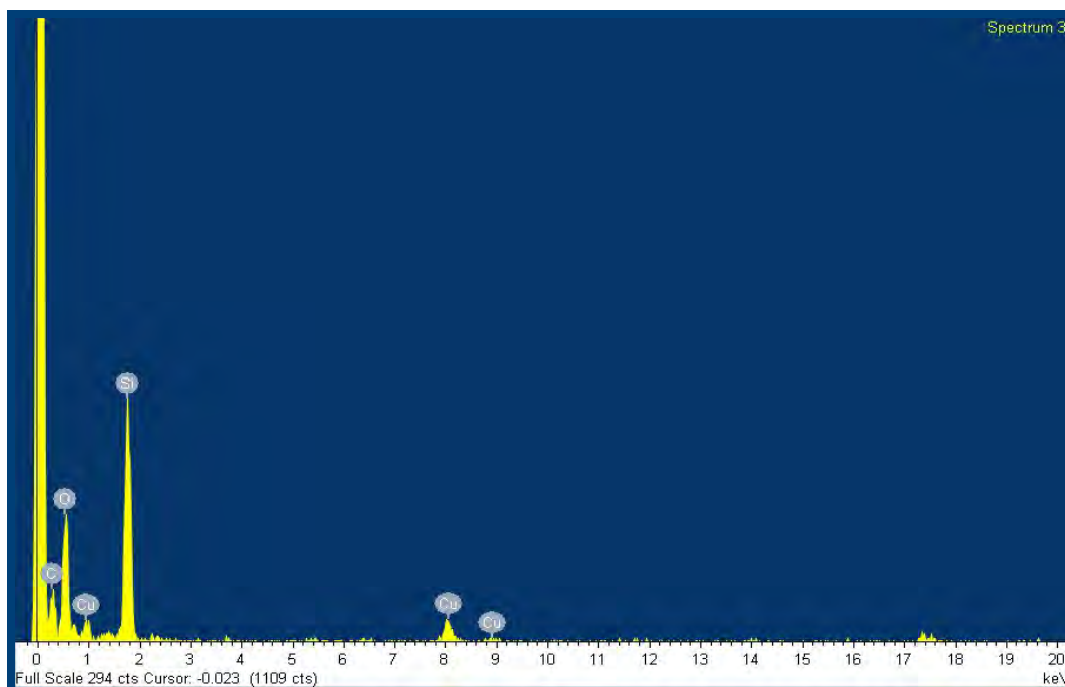


Figure 2.6.15: EDX spectrum at position 3 of Figure 2.6.12.

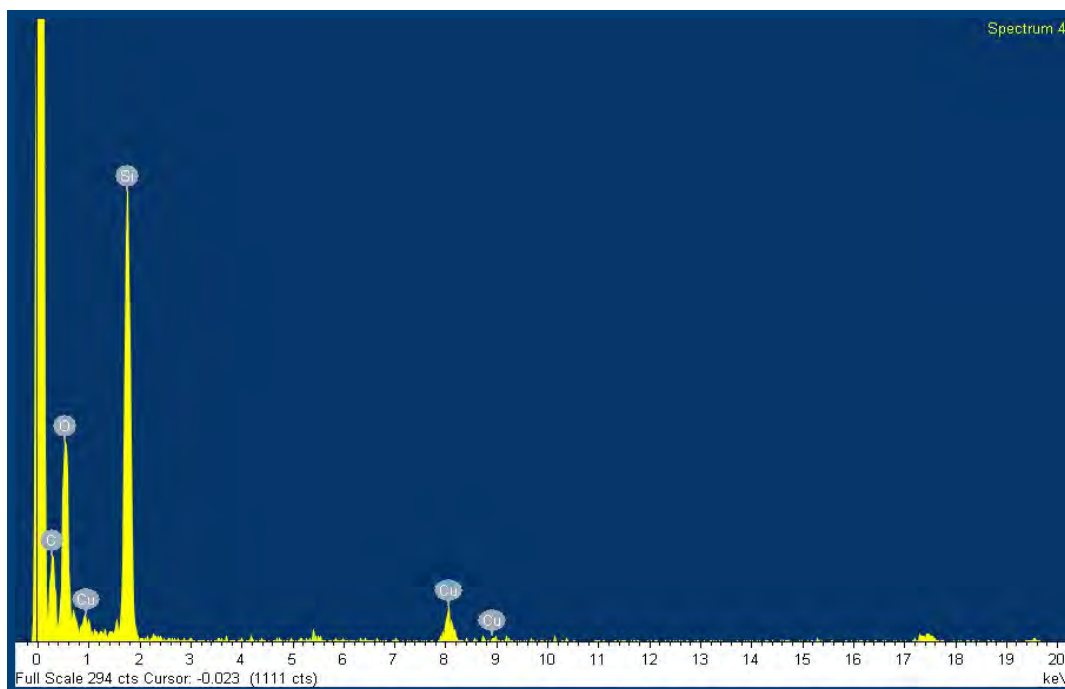


Figure 2.6.16: EDX spectrum at position 4 of Figure 2.6.12.

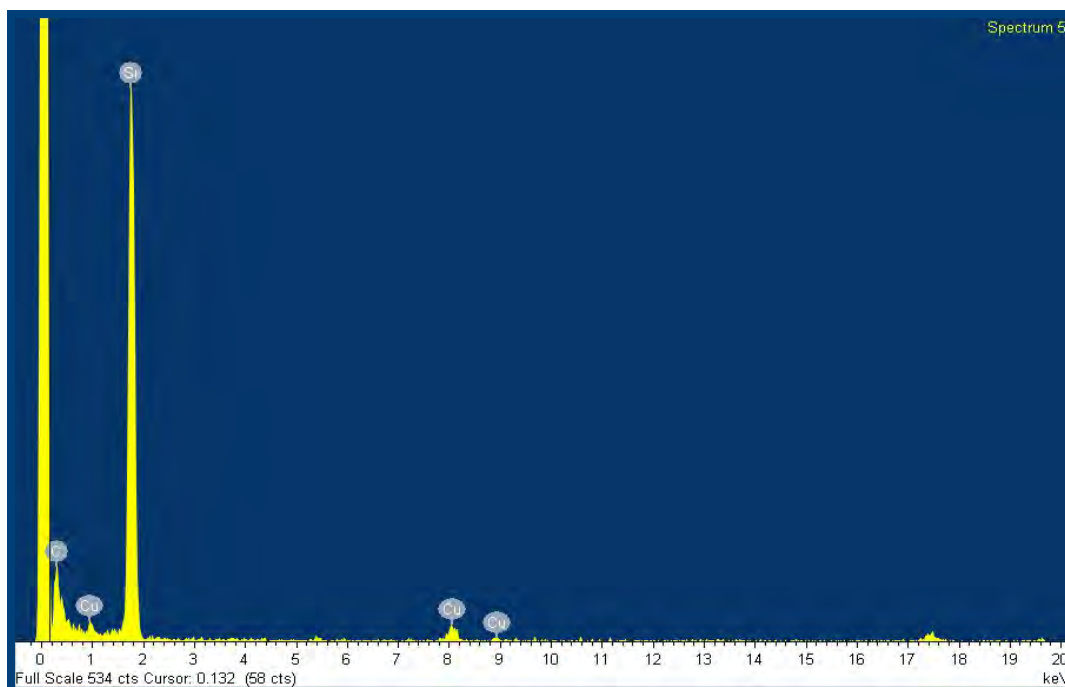


Figure 2.6.17: EDX spectrum at position 5 of Figure 2.6.12.

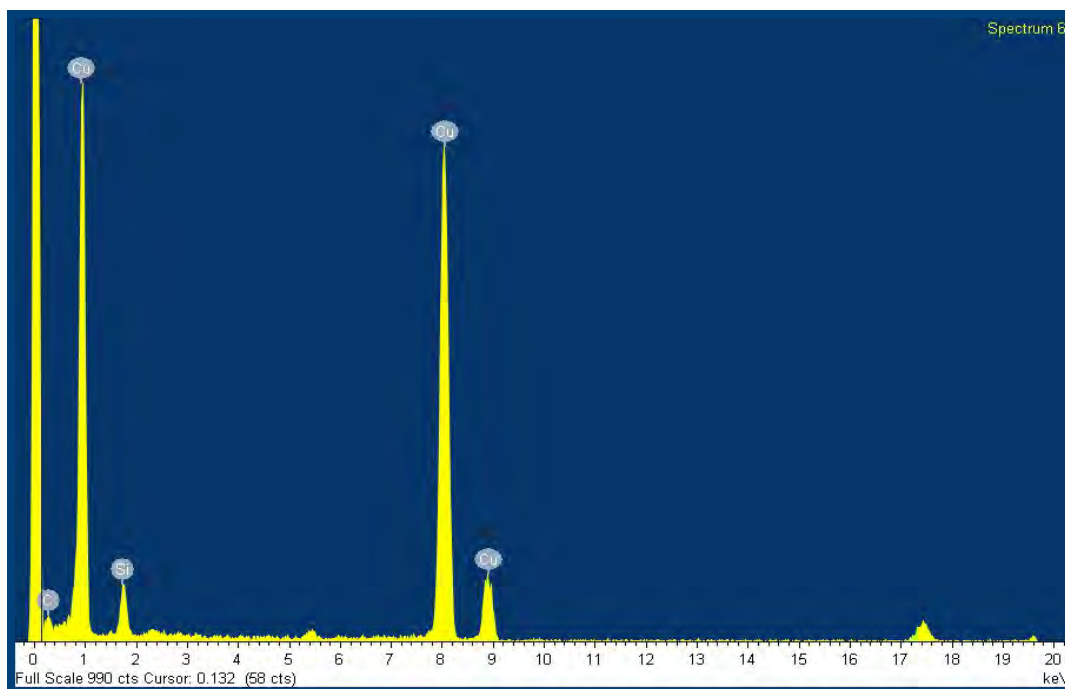


Figure 2.6.18: EDX spectrum at position 6 of Figure 2.6.12.

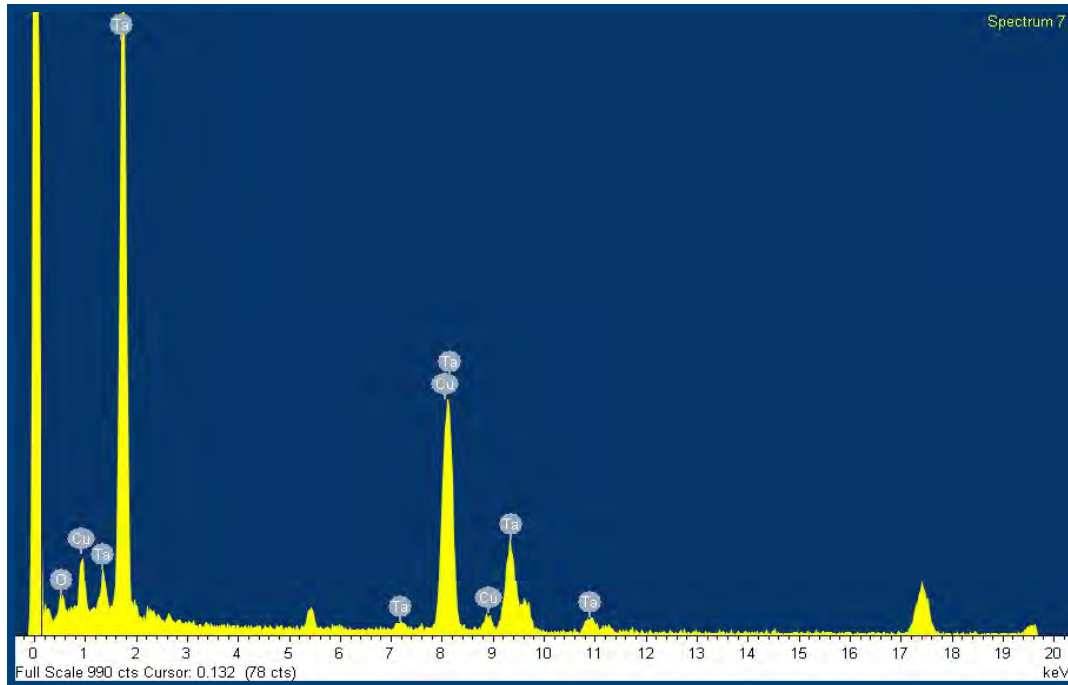


Figure 2.6.19: EDX spectrum at position 7 of Figure 2.6.12.

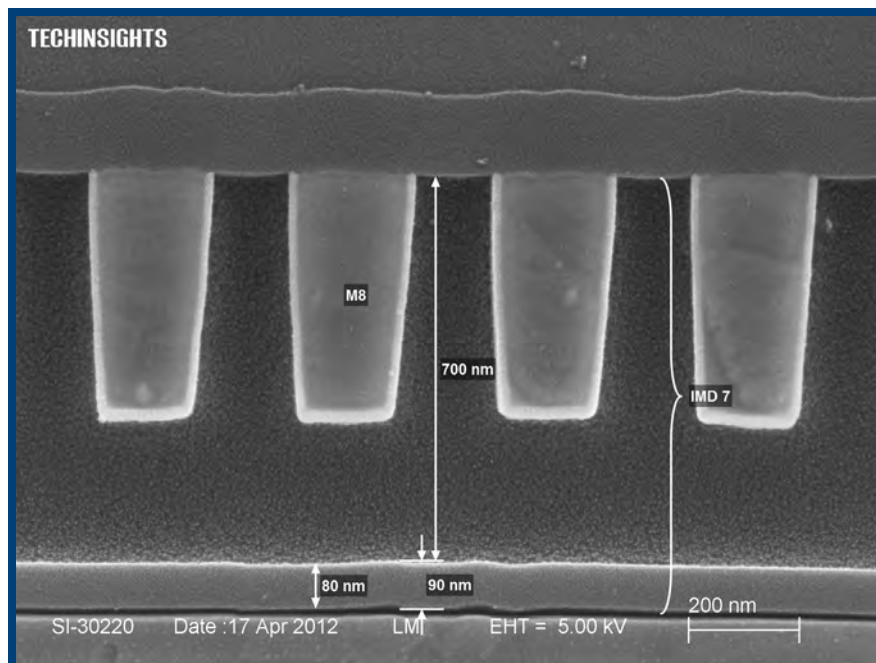


Figure 2.6.20: IMD 7; SEM cross-section.

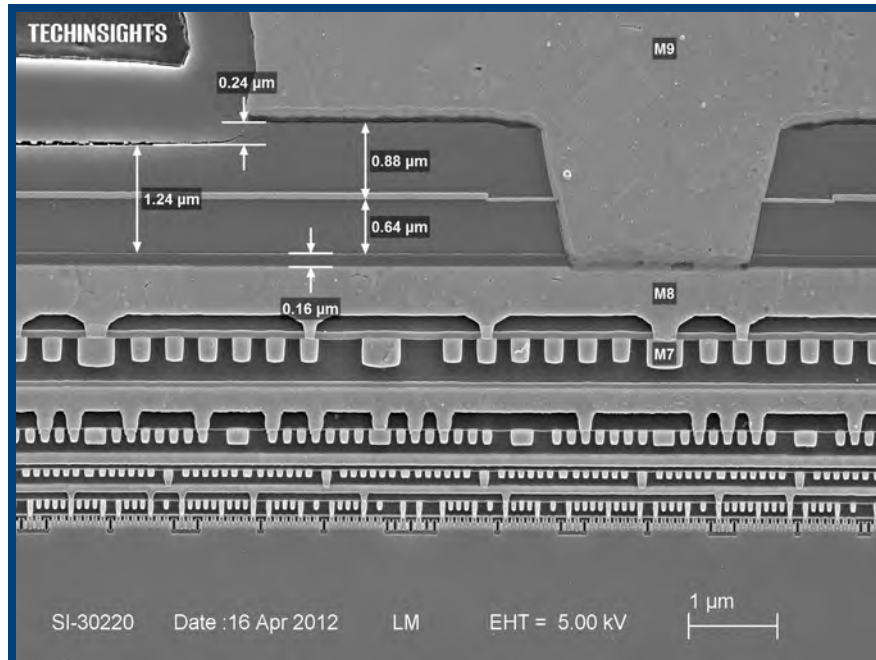


Figure 2.6.21: IMD 8; SEM cross-section.

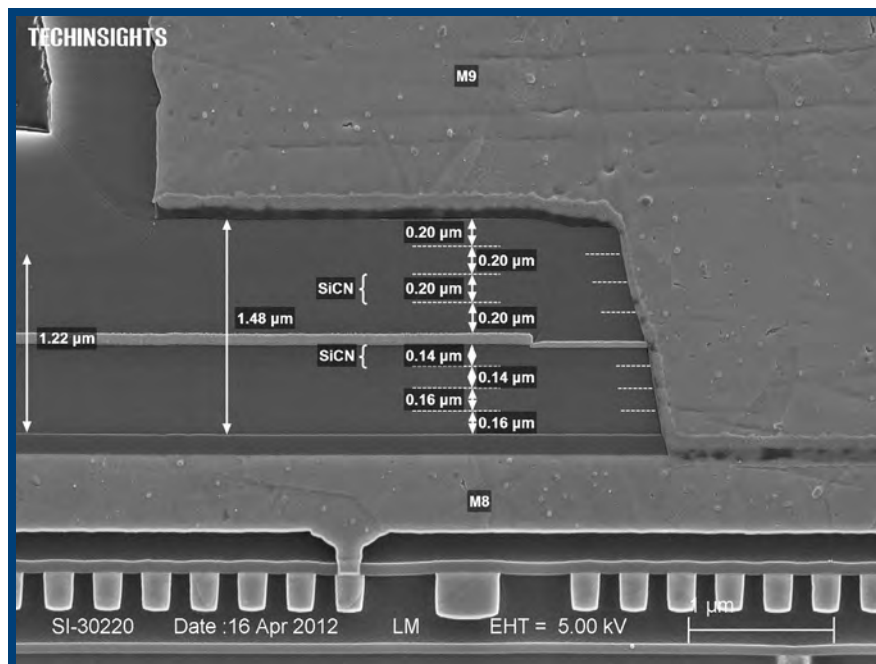


Figure 2.6.22: The substructure of IMD 8; SEM cross-section.

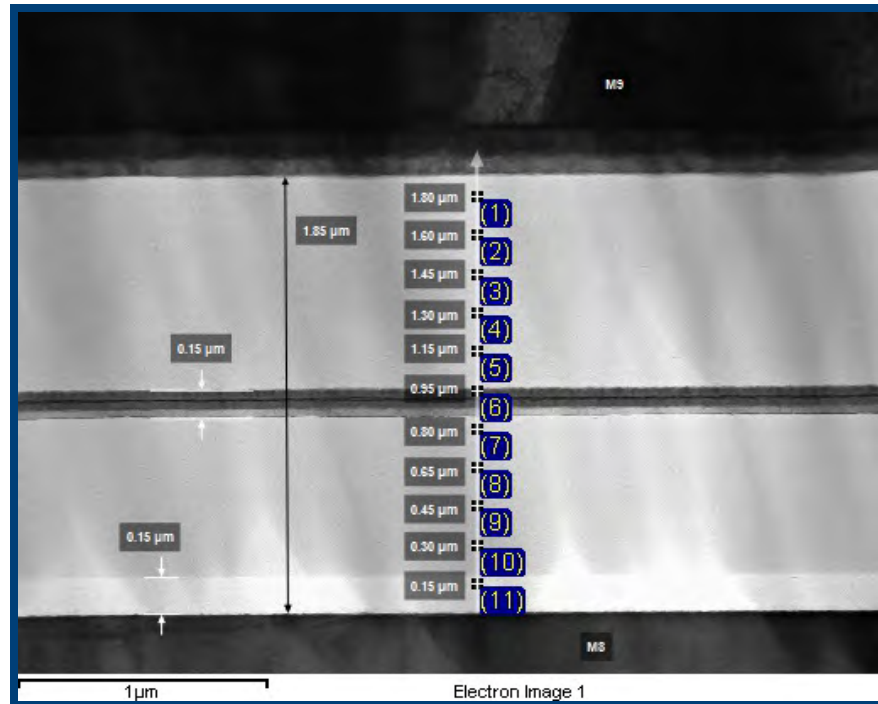


Figure 2.6.23: Location of the EDX point-ID scan through the IMD 8.

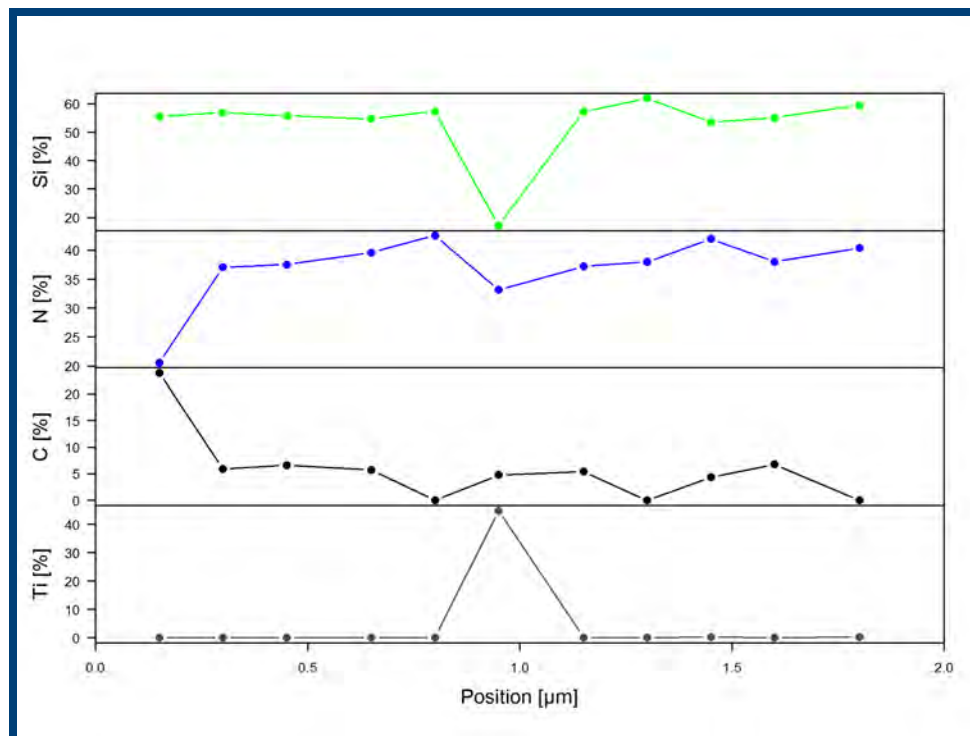


Figure 2.6.24: Results of the EDX point-ID scan through the IMD 8

Comments
- The M8 capping layer is SiCN; - It appears that the compositions of the IMD 8 sub-layers vary; - Two low/no-carbon layers are found in IMD 8; - IMD 8 shows so-called Novellus lines.

Feature	Cap Layer Material	Cap Layer THK	Dielectric Layer Material	Dielectric Layer THK
IMD 0	SiCN	20 nm	SiOC	135 nm
IMD 1	SiOCN	15 nm	SiOC	170 nm
IMD 2	(SiOCN)	15 nm	(SiOC)	165 nm
IMD 3	(SiOCN)	15 nm	(SiOC)	180 nm
IMD 4	(SiOCN)	15 nm	SiOC	270 nm
IMD 5	SiOCN	15 nm	SiOC	450 nm
IMD 6	SiCN	70 nm	(SiOC)	470 nm
IMD 7	SiCN	85 nm	(SiOC)	700 nm
IMD 8	SiCN	0.16 μ m	SiCN	1.54 μ m

Table 2.6.1: Inter-metal dielectric dimensions¹.

Comments
- No significant differences in the silicon oxide based dielectrics are found; - It is assumed that for IMD 0 to IMD 2 an extreme low-k and for IMD 3 to 7 a low-k material is used.

¹ Readings in brackets are conclusions. Missing metal capping layer materials can be safely assumed to be silicon nitride based.

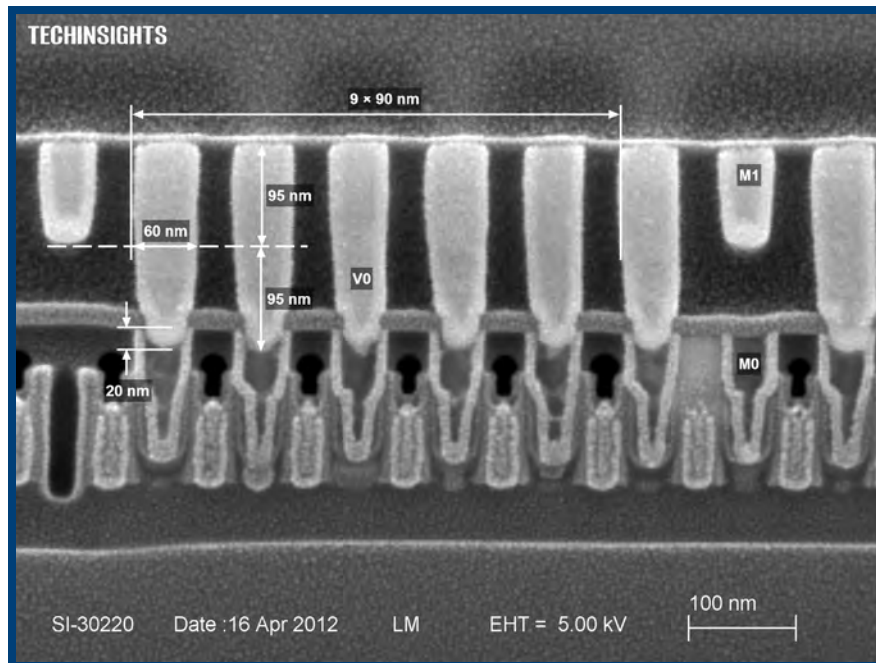


Figure 2.6.25: Dense via 0; SEM cross-section.

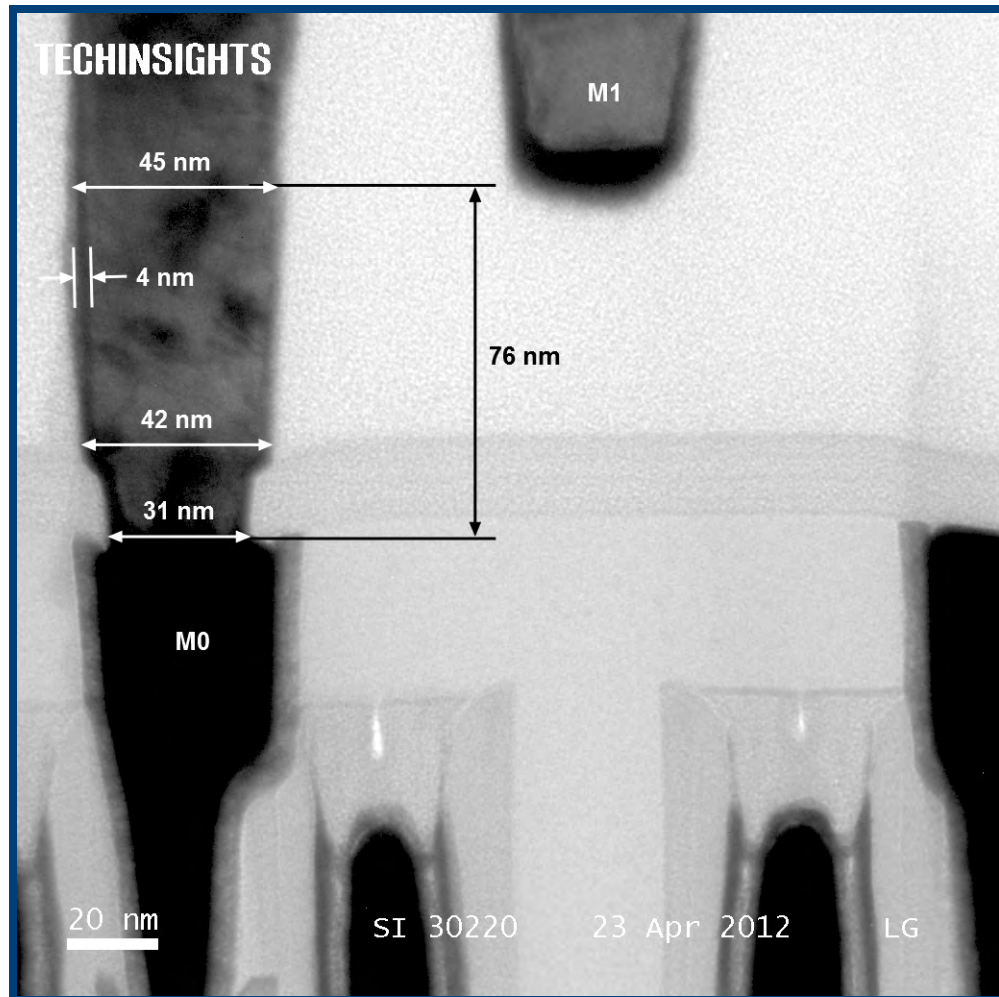


Figure 2.6.26: Isolated via 0; TEM cross-section.

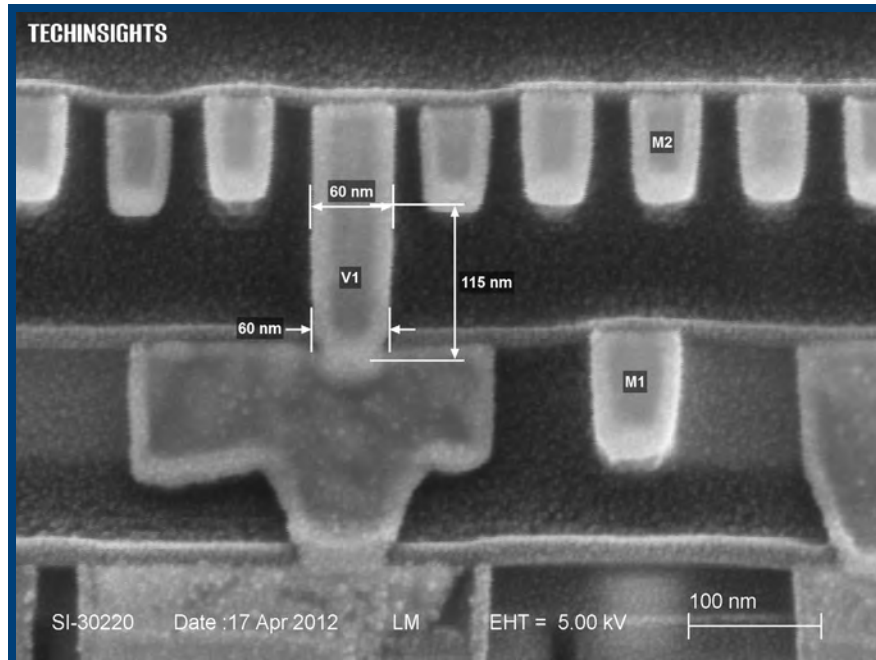


Figure 2.6.27: Via 1; SEM cross-section.

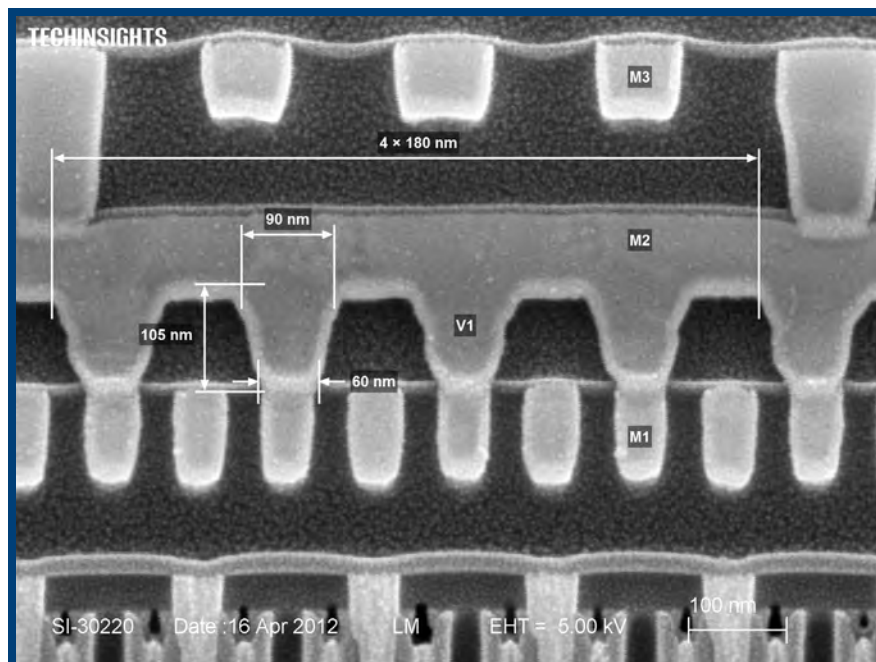


Figure 2.6.28: Via 1 chain; SEM cross-section.

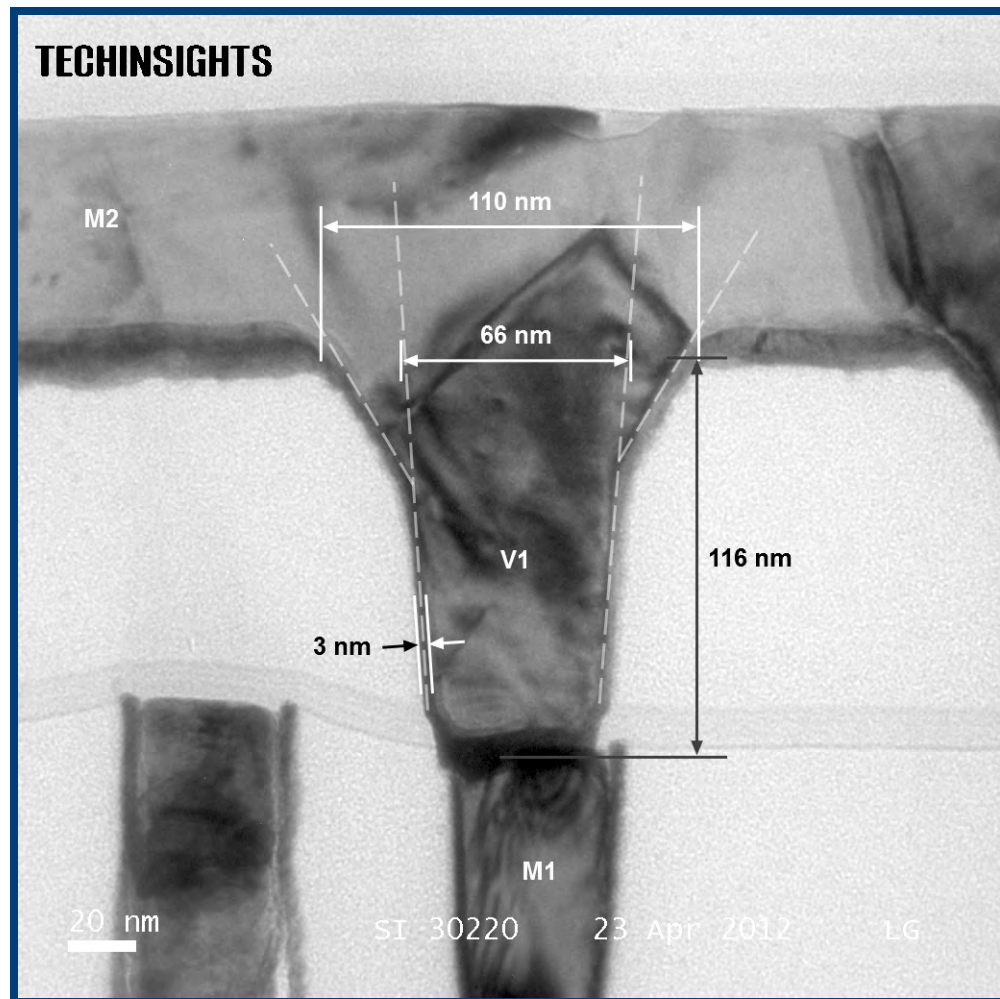


Figure 2.6.29: Isolated via 1; TEM cross-section.

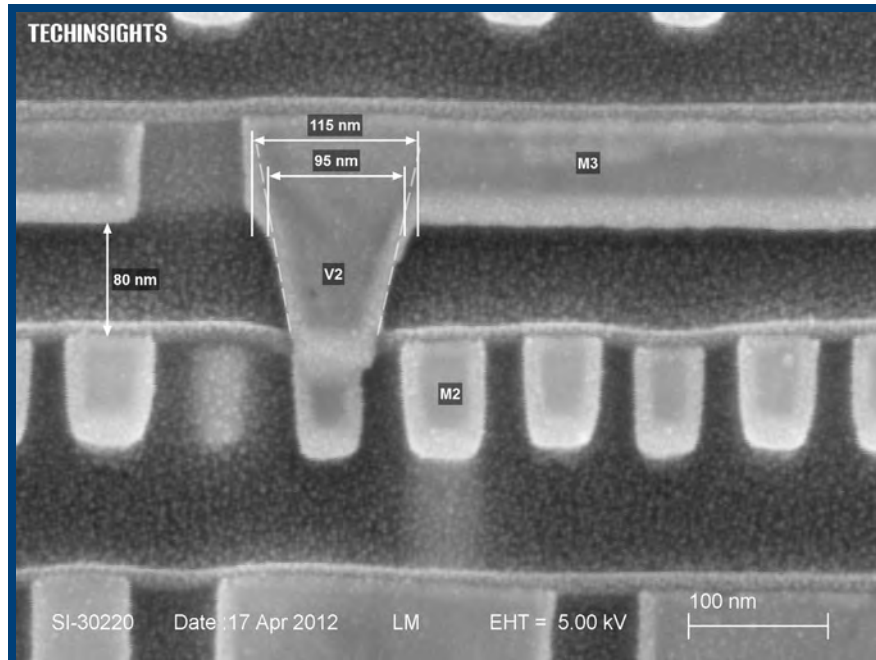


Figure 2.6.30: Via 2; SEM cross-section.

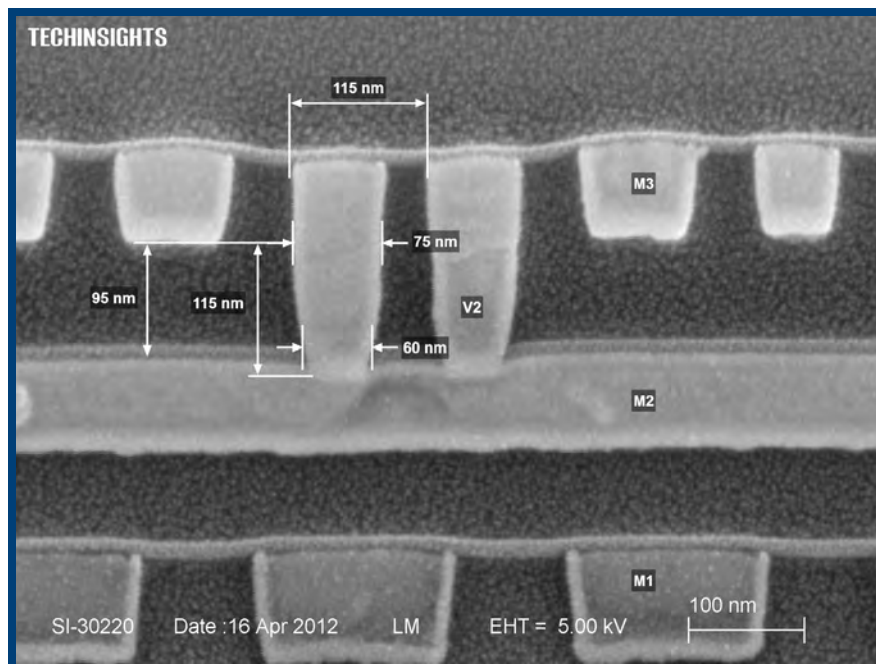


Figure 2.6.31: Via 2 pair; SEM cross-section.

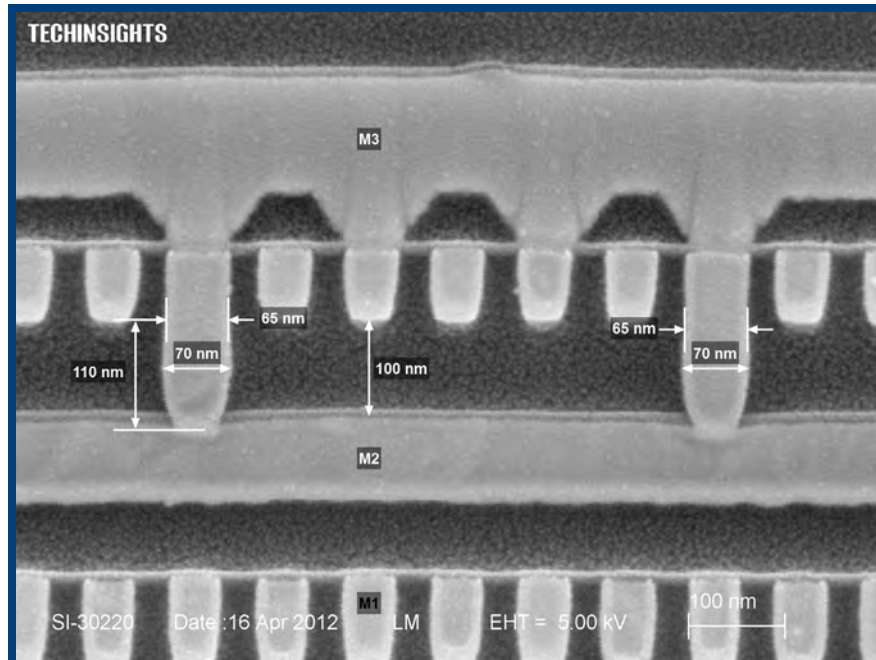


Figure 2.6.32: Barrel shaped via 2 due to over-etching; SEM cross-section.

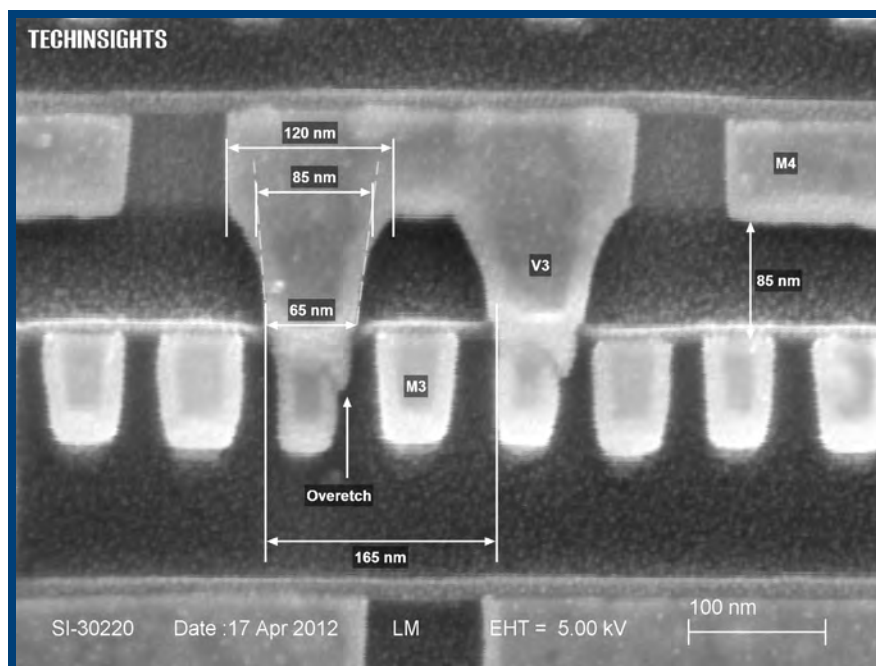


Figure 2.6.33: Via 3 pair; SEM cross-section.

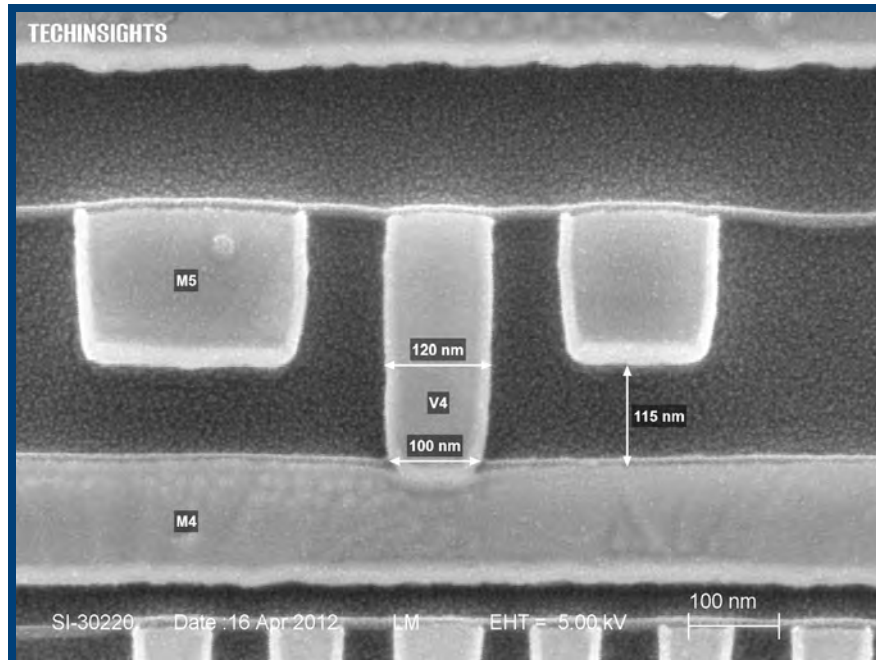


Figure 2.6.34: Isolated via 4; SEM cross-section.

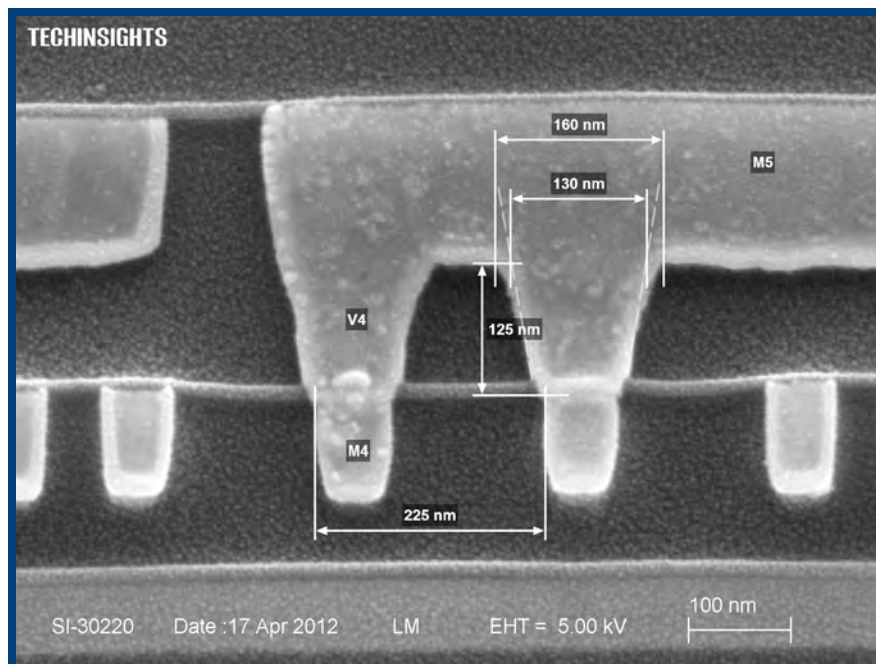


Figure 2.6.35: Via 4 pair; SEM cross-section.

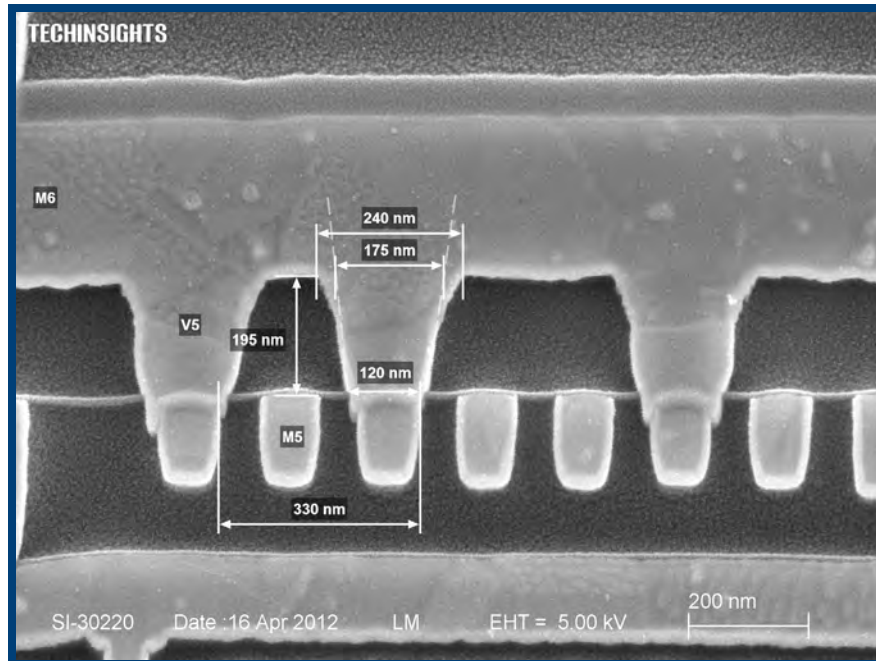


Figure 2.6.36: Via 5; SEM cross-section.

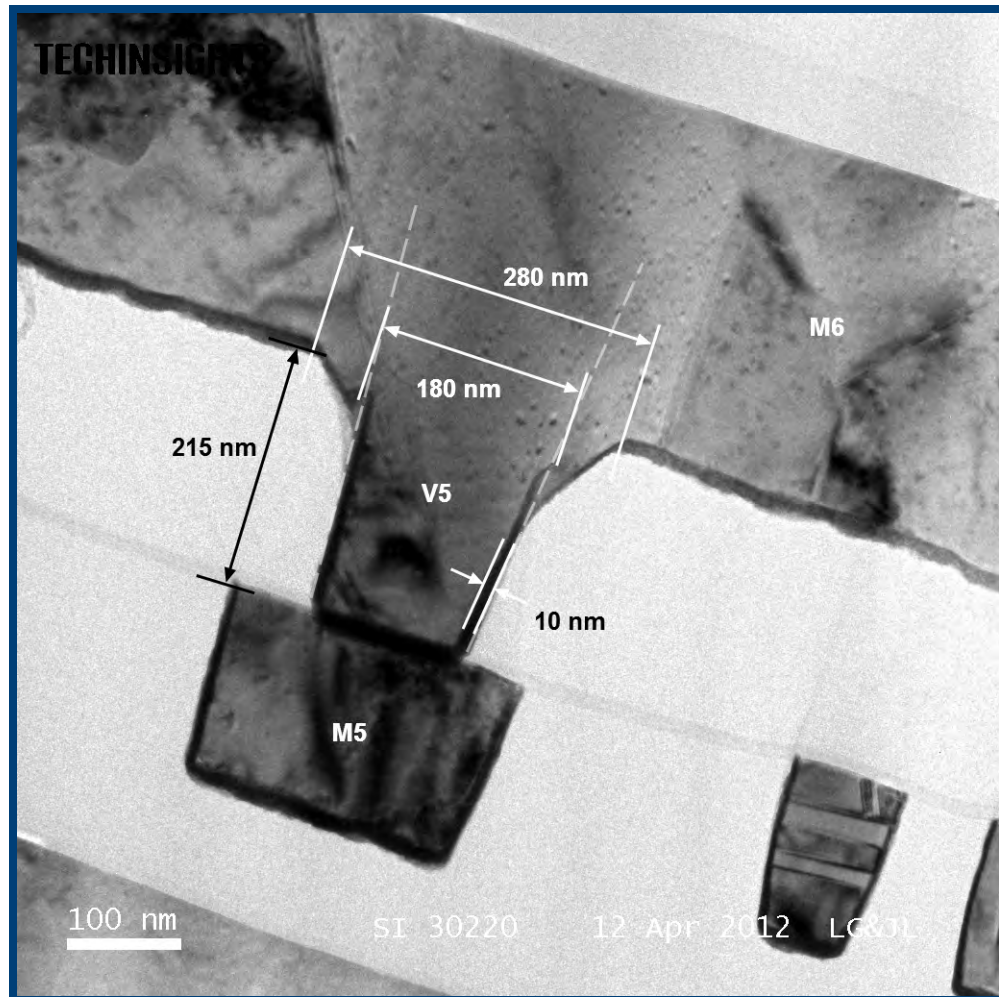


Figure 2.6.37: Isolated via 5; TEM cross-section.

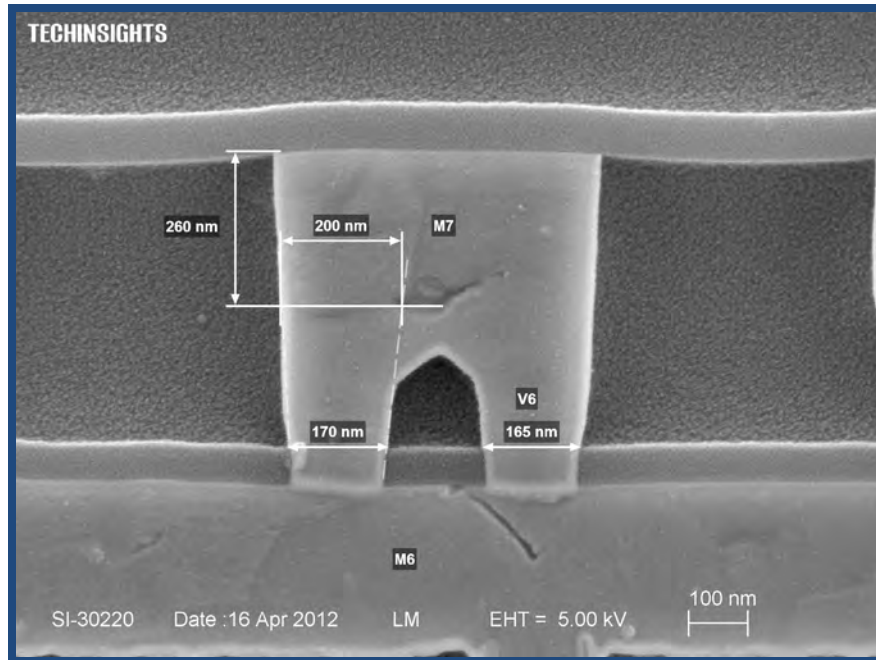


Figure 2.6.38: Via 6 pair; SEM cross-section.

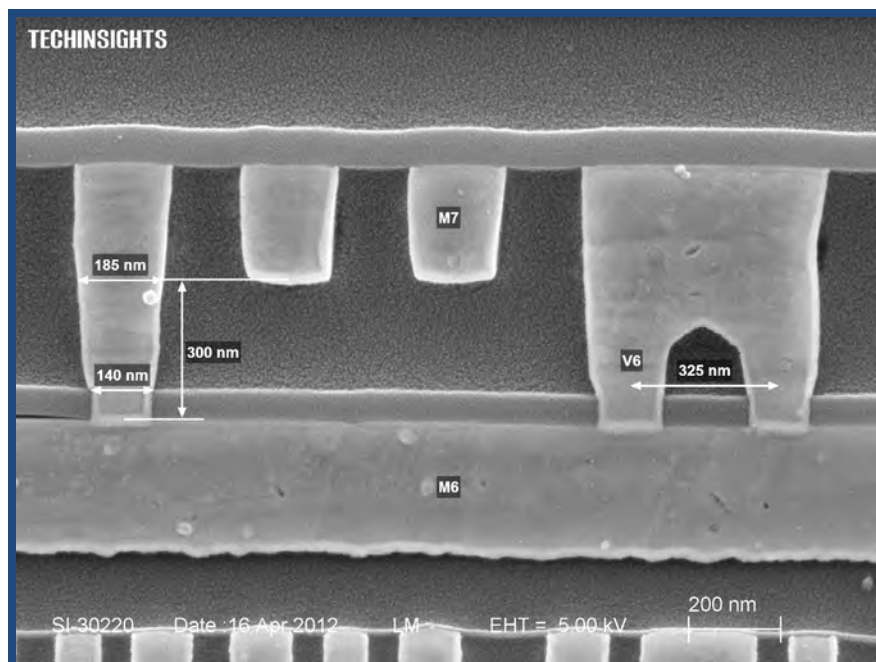


Figure 2.6.39: Isolated and pair of via 6; SEM cross-section.

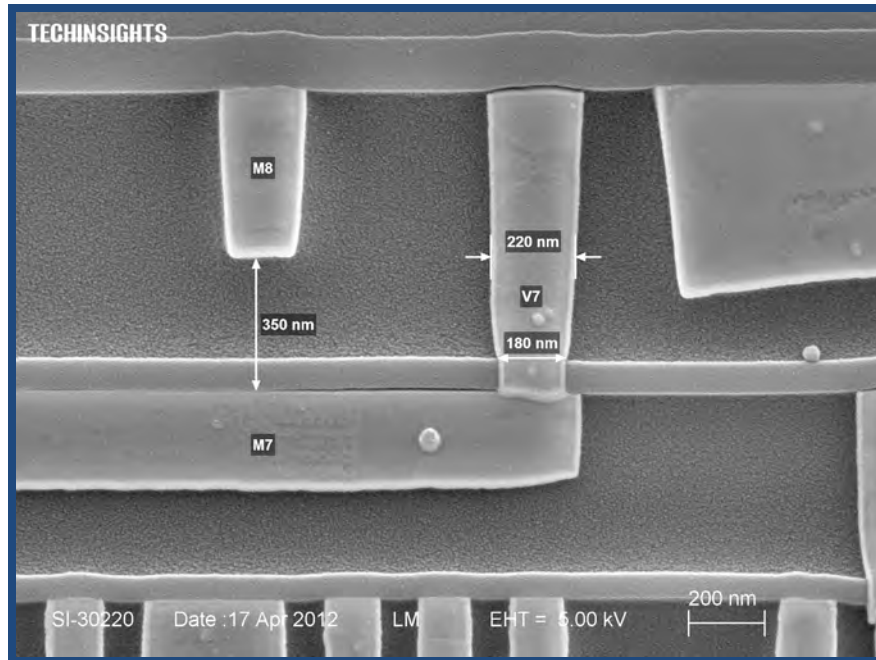


Figure 2.6.40: Isolated via 7; SEM cross-section.

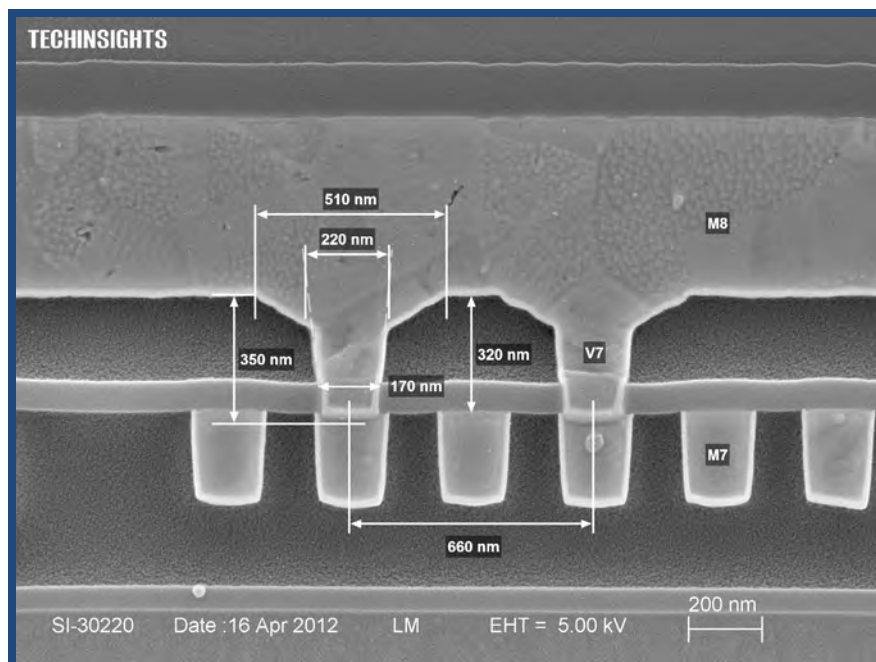


Figure 2.6.41: Via 7 pair; SEM cross-section.

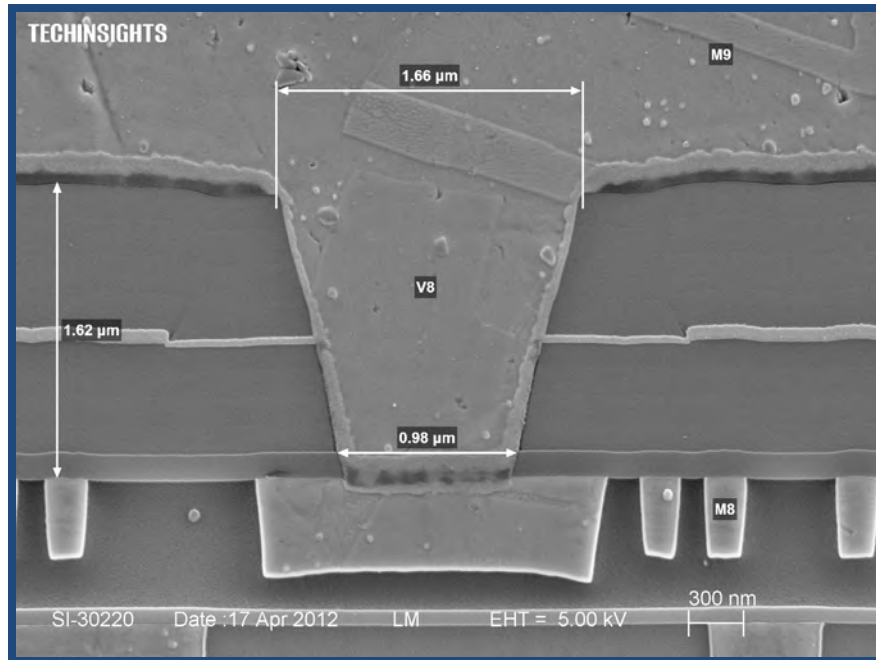


Figure 2.6.42: Via 8; SEM cross-section.

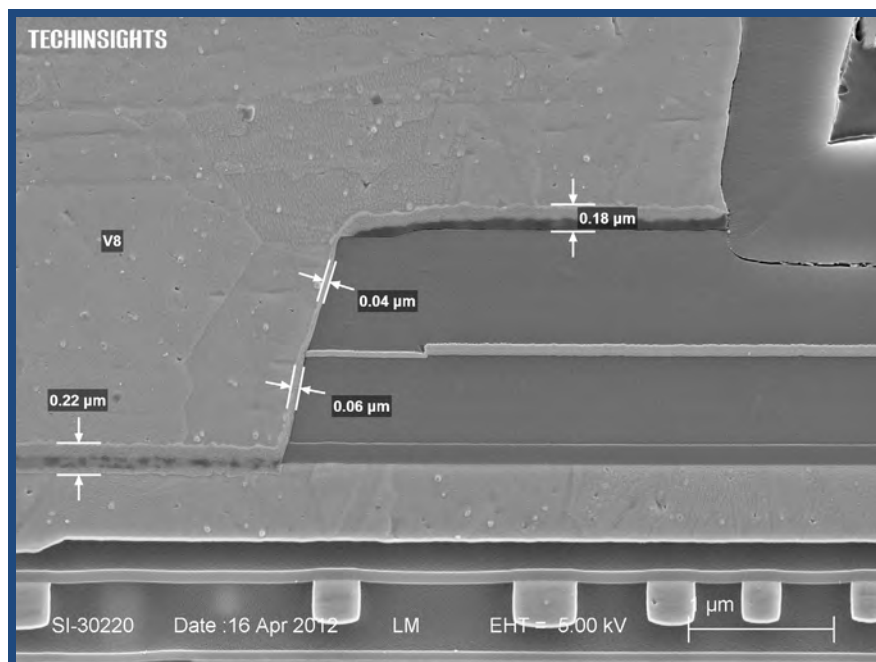


Figure 2.6.43: Via 8 side portion; SEM cross-section.

Feature	Pitch [nm]	Depth [nm]	Top CD [nm]	Bottom CD [nm]	Liner THK [nm]
VIA 0	90	95	45	42	4
VIA 1	180	115	66	60	3
VIA 2	115	(95)	(70)	(60)	—
VIA 3	165	85	(85)	(65)	—
VIA 4	225	115	120	100	—
VIA 5	330	195	(175)	120	10
VIA 6	325	300	185	140	—
VIA 7	660	350	220	180	—
VIA 8	—	1620	1660	980	50

Table 2.6.2: Via dimensions².

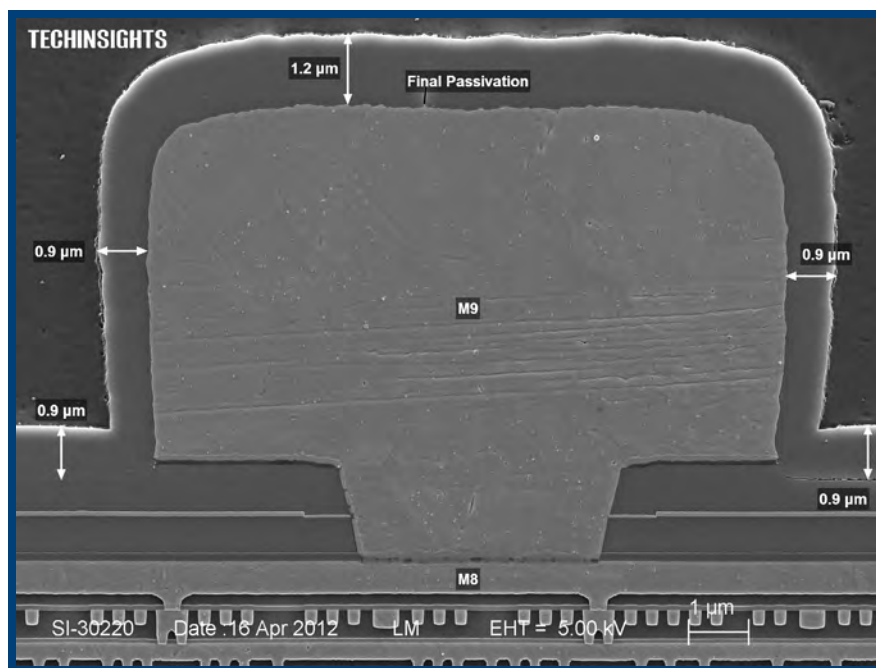


Figure 2.6.44: Final passivation overlying metal 9; SEM cross-section.

² Data given in brackets are estimates.

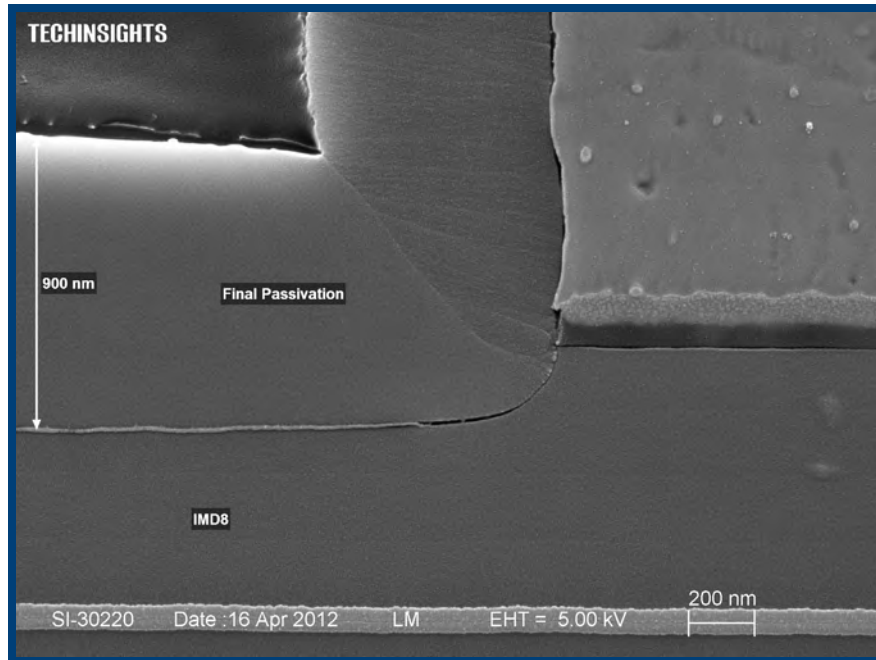


Figure 2.6.45: Final passivation corner coverage; SEM cross-section.

Comments

- 0.90 – 1.20 μm silicon nitride final passivation.

3.0 Layout and Structural Analysis of 6T SRAM Cell

3.1 Topographical Analysis of 6T SRAM Cell (Type 1)

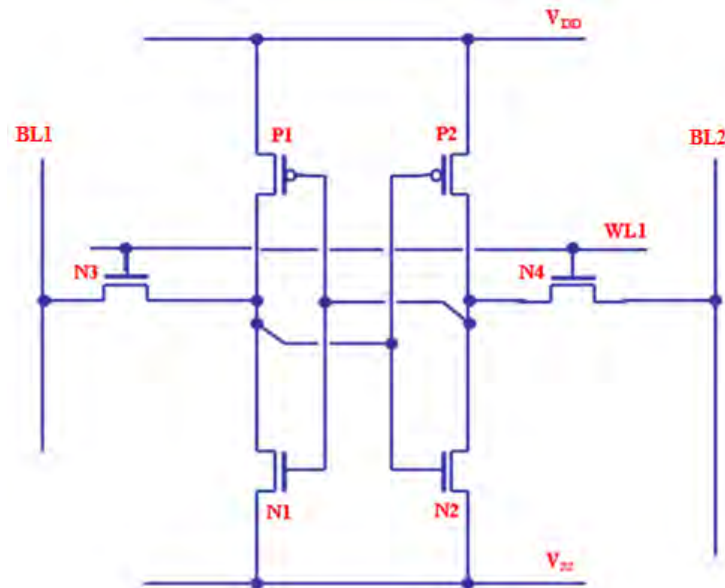


Figure 3.1.1: 6T SRAM cell schematic.

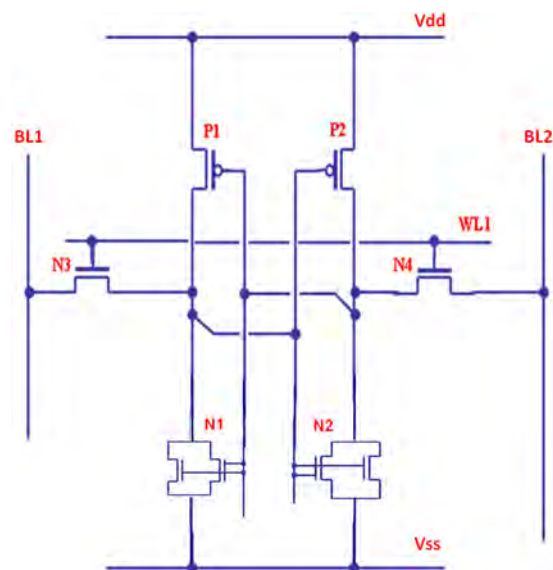


Figure 3.1.2: 6T SRAM cell schematic with pull-down transistors consisting of two transistors connected in parallel.



Figure 3.1.3: Die de-layered to diffusion. The approximate location of SRAMs is marked.

Comments

- Intel's IVY BRIDGE is using two 6T SRAM layouts but all pull down transistors have either two or three transistors in parallel;
- Both embedded memories in this 22 nm device have 6T SRAM cell configuration;
- The smaller cell size (Type 1) is more prevalent and is used as the L3 Cache employing 2-NMOS pull-down transistors in parallel;
- The Type-2 SRAM has bigger cell area employing 3-NMOS pull down transistors in parallel;
- P1 and P2 are PMOS "Pull-up transistors";
- N1 and N2 are NMOS "Pull-down transistors";
- N3 and N4 are NMOS "Access transistors".

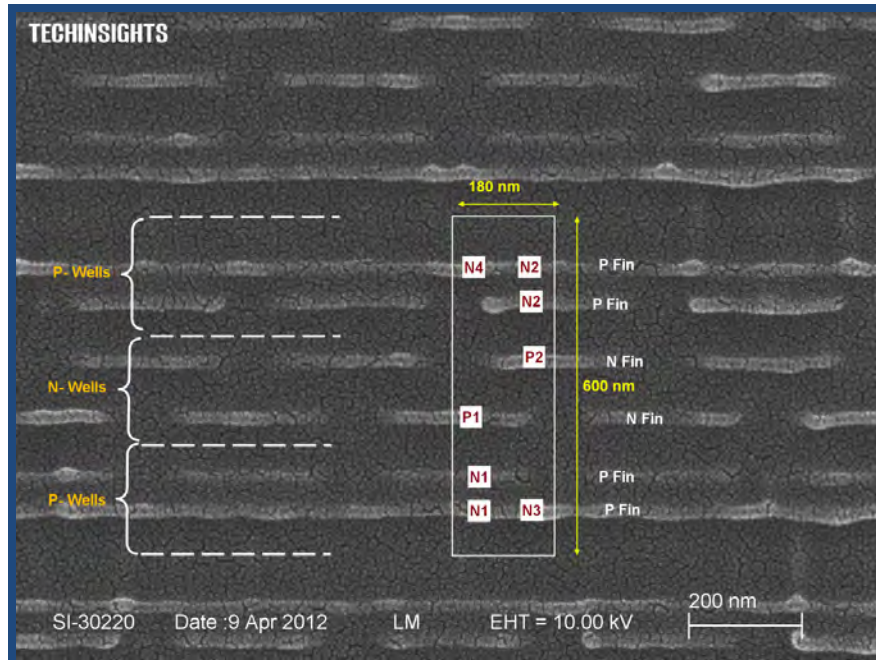


Figure 3.1.4: Topographical SEM image of 6T SRAM array (Type-1), de-layered to diffusion.

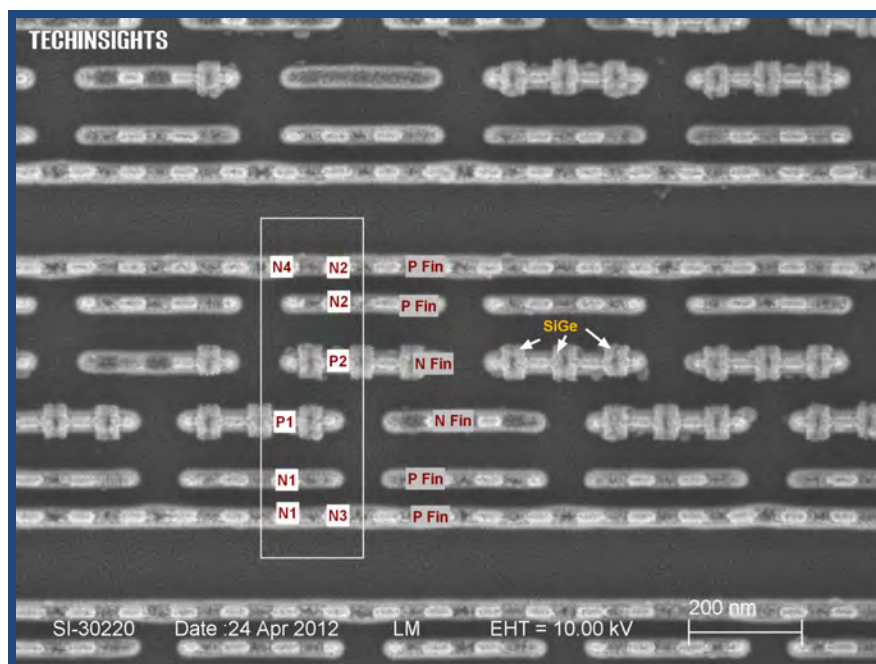


Figure 3.1.5: Topographical SEM image of the 6T SRAM array (Type 1) at the diffusion level with metal gates removed.

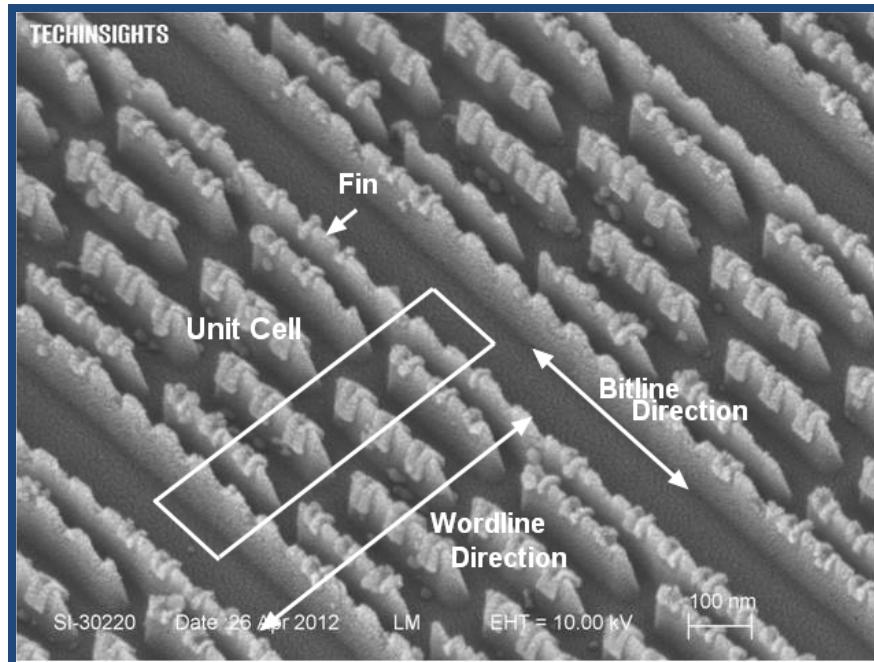


Figure 3.1.6: Topographical tilted-SEM image of the 6T SRAM array (Type 1) at the diffusion level with metal gates removed.

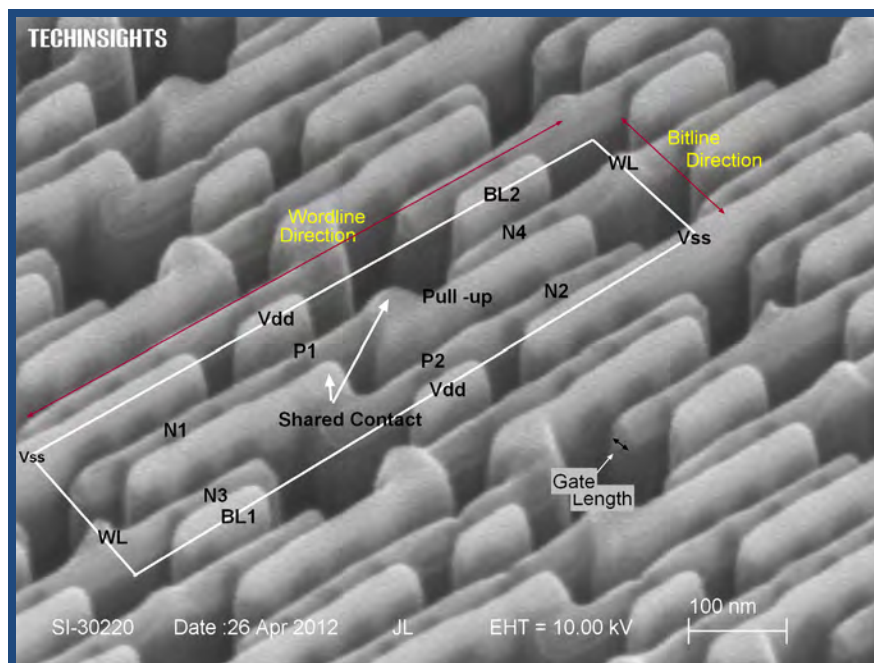


Figure 3.1.7: Topographical tilted-SEM image of the 6T SRAM array (Type 1) at the gate level.

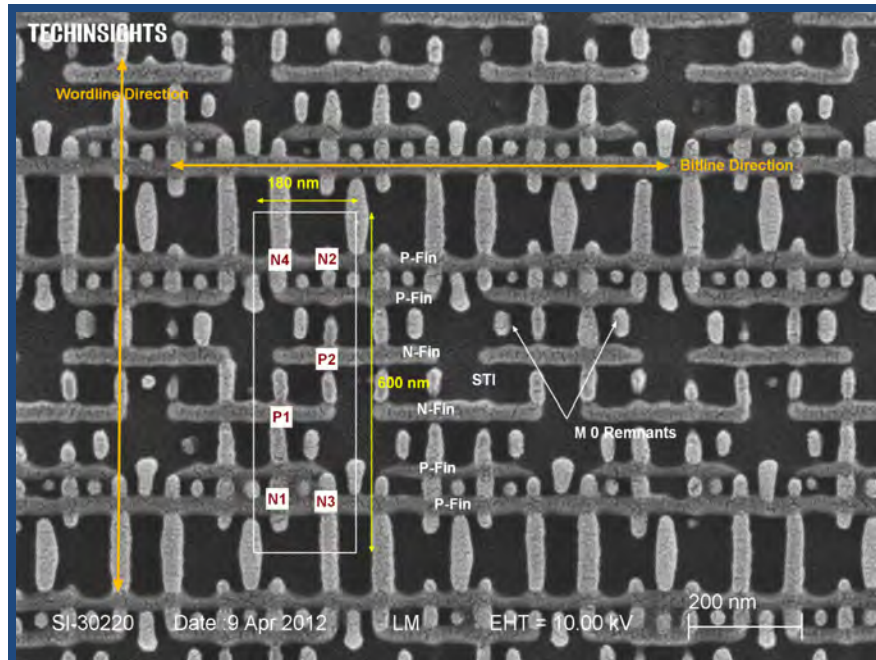


Figure 3.1.8: Topographical SEM image of 6T SRAM (Type 1) array de-layered to the level below gate level.

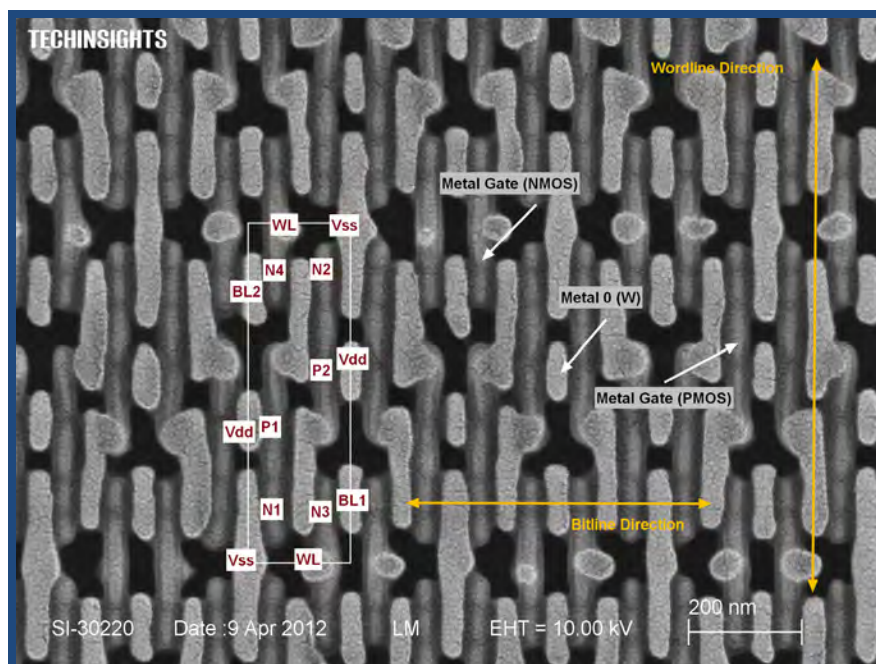


Figure 3.1.9: Topographical SEM image of 6T SRAM (Type 1) array at gate level and Metal 0.

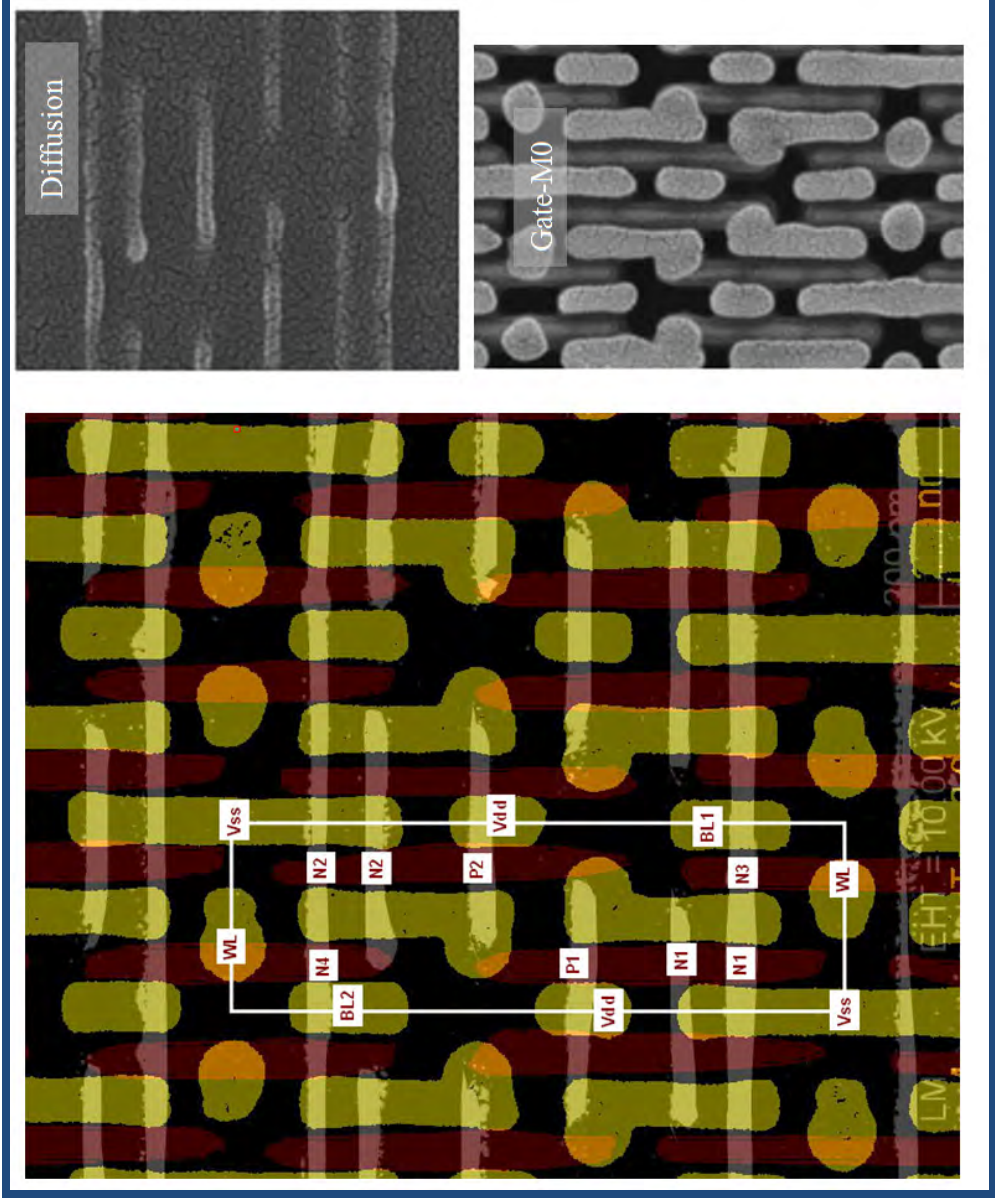


Figure 3.1.10: Superimposed topographical SEM image of 6T SRAM (Type 1) array of substrate and gate levels.

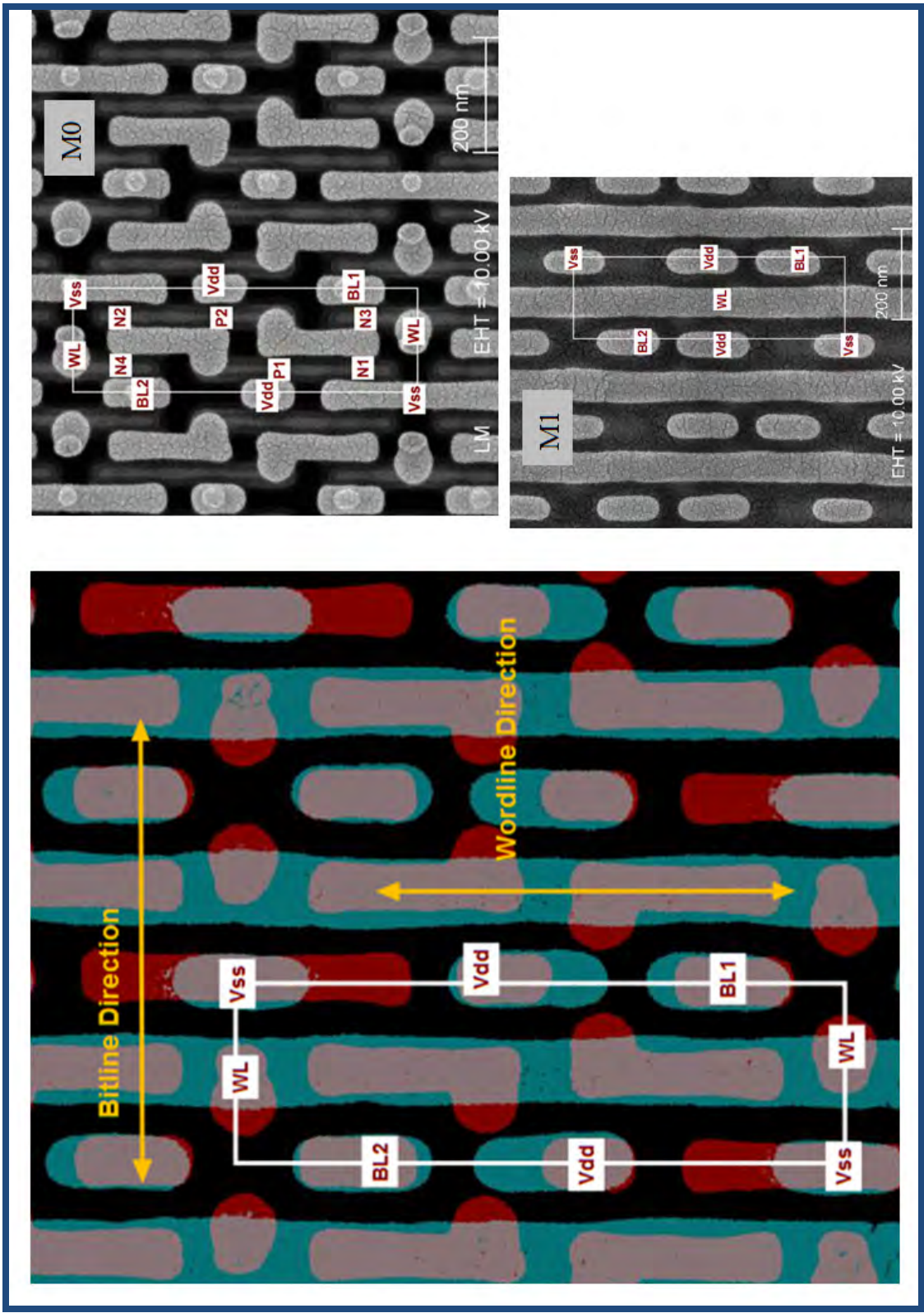


Figure 3.1.11: Superimposed topographical SEM image of 6T SRAM (Type 1) array of M0 and M1 levels.

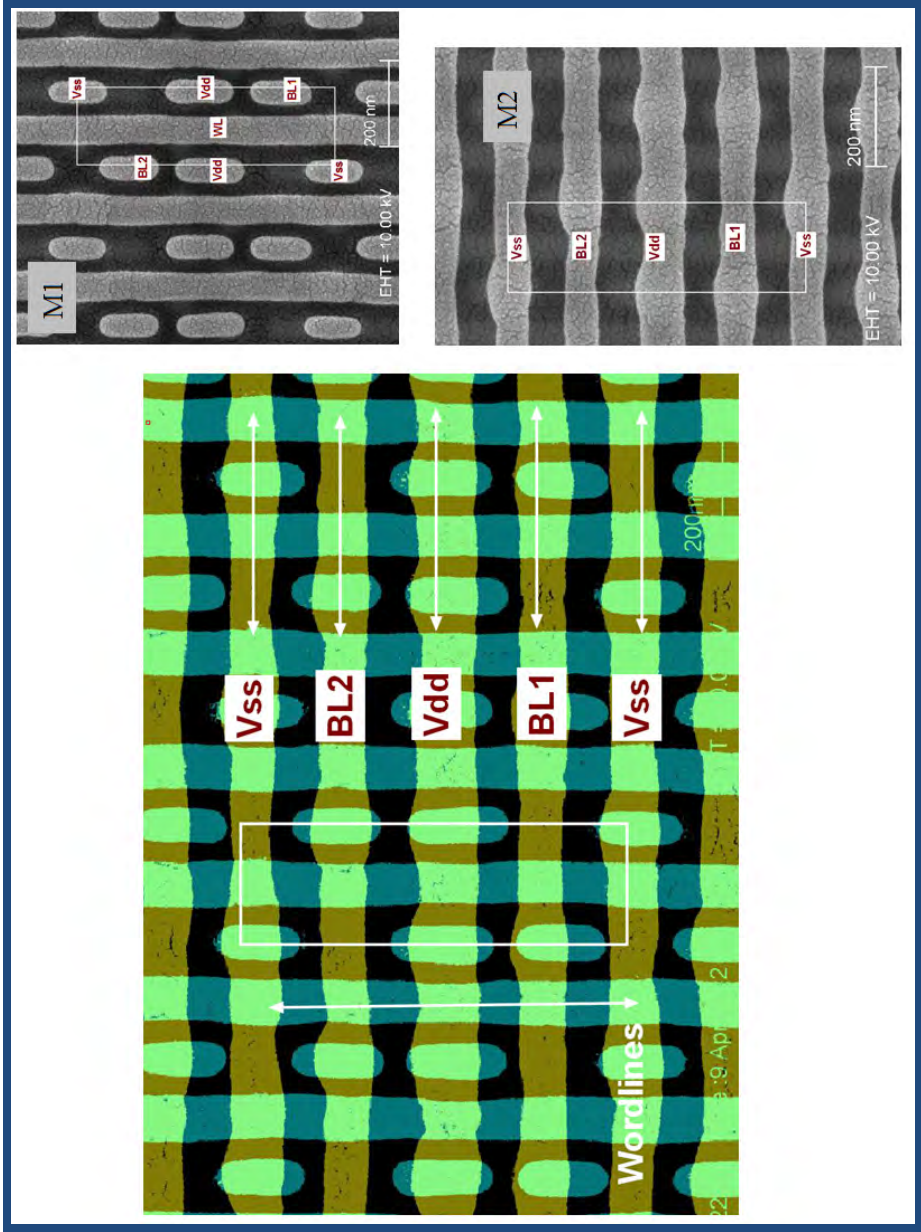


Figure 3.1.12: Superimposed topographical SEM image of 6T SRAM (Type 1) array of M1 and M2 levels.

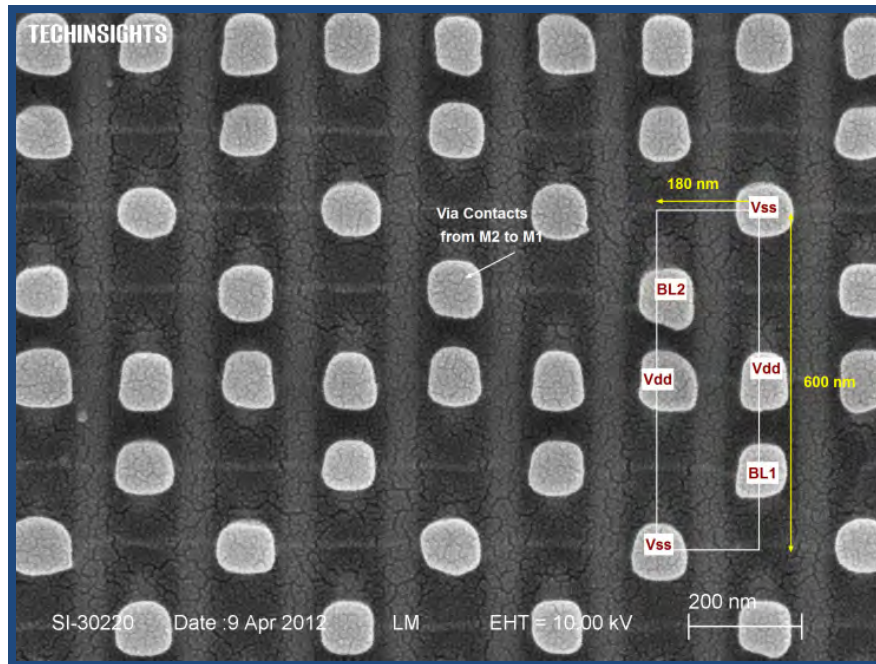


Figure 3.1.13: Topographical SEM image of 6T SRAM (Type 1) array at Via 1 level.

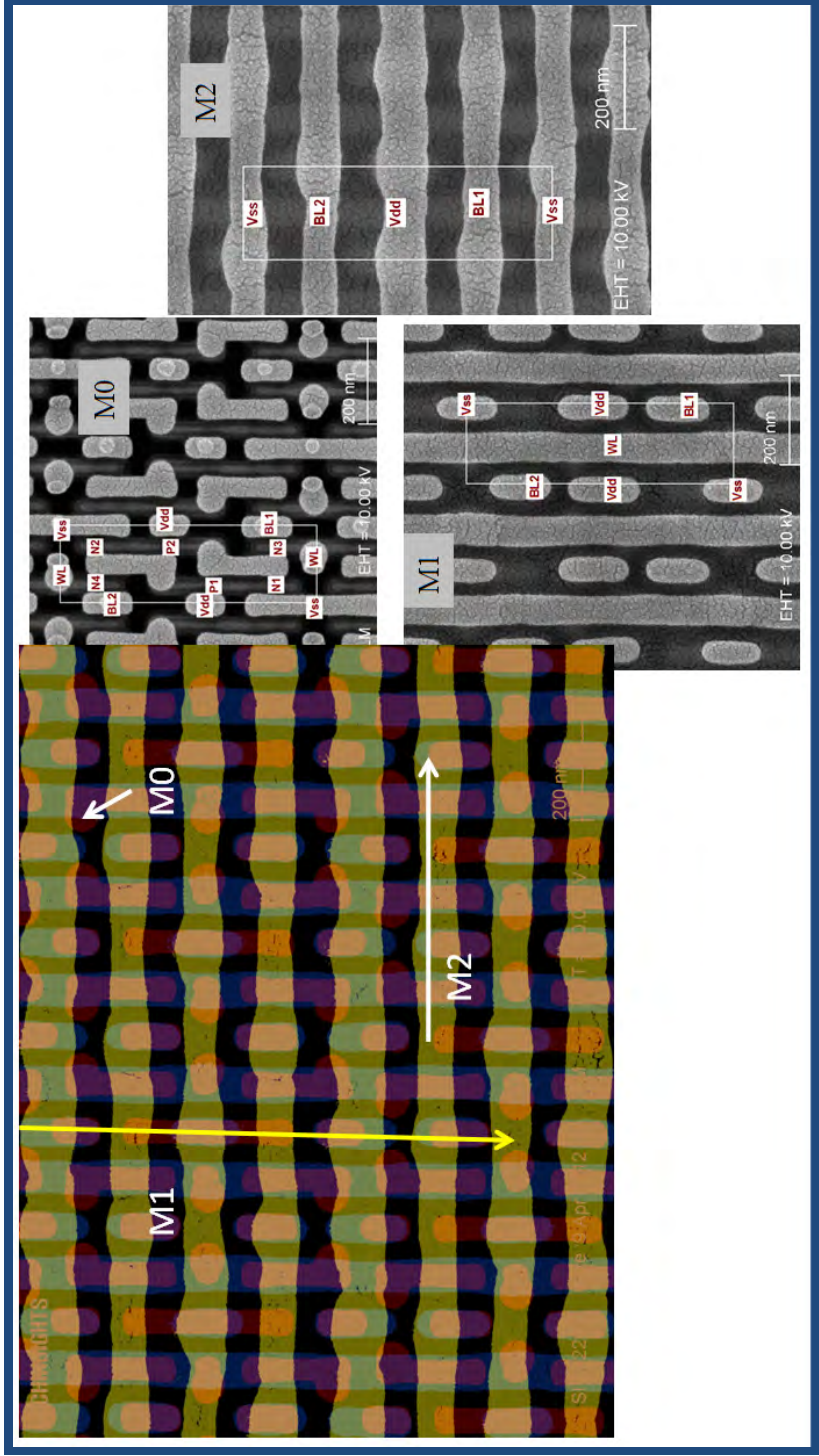


Figure 3.1.14: Superimposed topographical SEM image of 6T SRAM (Type 1) array of M0, M1 and M2 levels.

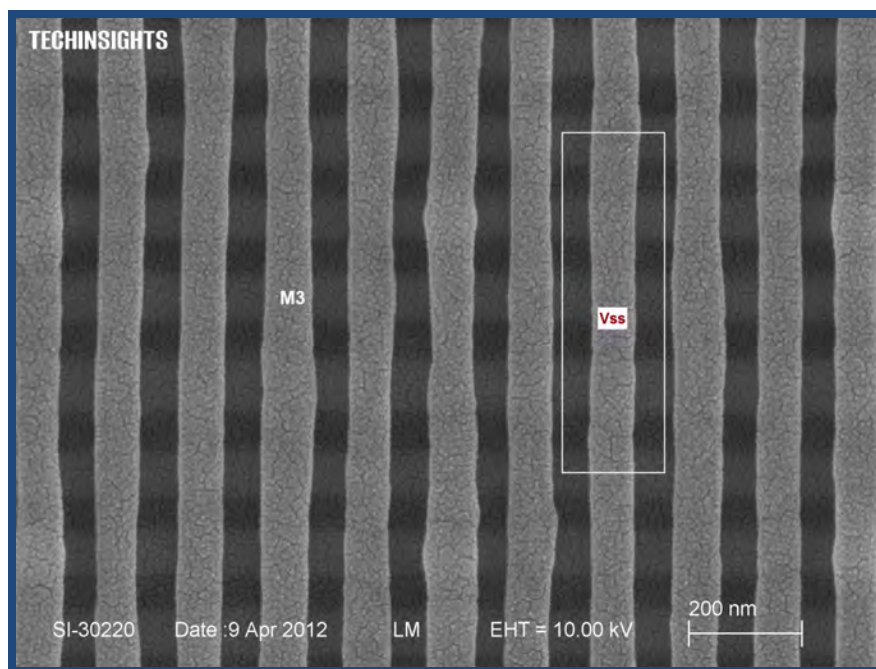


Figure 3.1.15: Topographical SEM image of 6T SRAM (Type 1) array at metal 3 level.

<i>Feature</i>	<i>Dimension</i>	<i>Unit</i>
6T SRAM cell height	0.60	μm
6T SRAM cell width	0.18	μm
6T SRAM cell area	0.108	μm^2

Table 3.1.1: 6T SRAM-Type1 cell size.

<i>Comments</i>
• “Thin Cell” layout, with cell aspect ratio of 3.3:1; • NMOS pull-down transistors use two silicon fins, therefore could be considered as two transistors connected in parallel; • Wordlines are implemented in metal 1; • Bitlines, Vdd and Vss are routed in metal 2; • The longer side of the cell is along wordlines; • Bitlines are parallel to the fins on the substrate; • Vdd and Vss lines are separated by bitlines at metal 2 level.

3.2 Plan View Analysis of the 6T SRAM Array-type 2

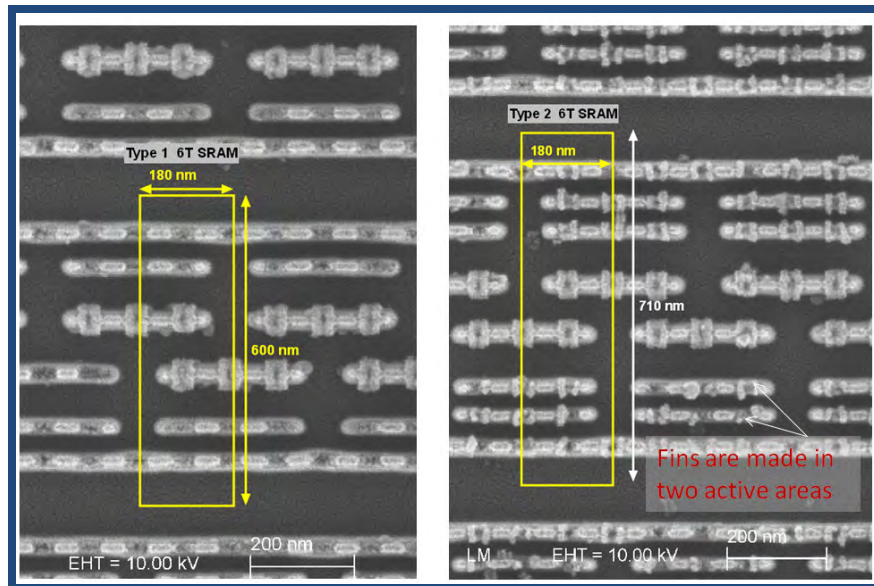


Figure 3.2.1: Topographical SEM images of the 6T SRAM cells (Type 1 left and Type 2 right) at the diffusion level.

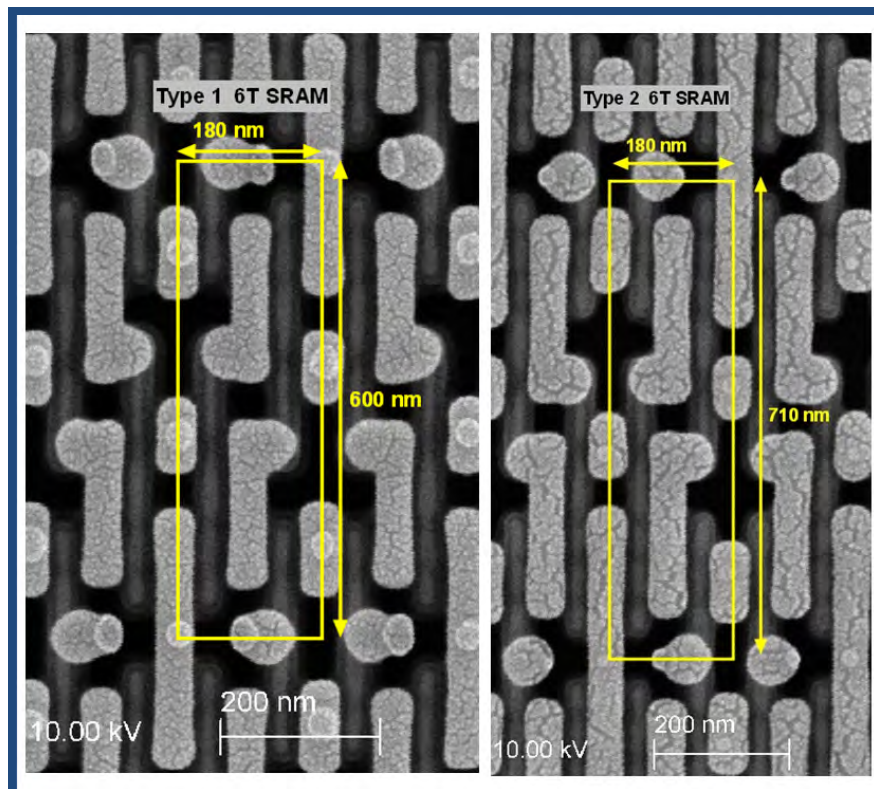


Figure 3.2.2: Topographical SEM images of the 6T-SRAM array (Type 1 and Type 2) at M0 level.

Comments

- Topographical image of Type 2 embedded memory at M0 level confirms the 6T-cell configuration;
- Plan view image at diffusion level puts in evidence that the pull down transistors of Type 2 SRAM are consisting of multiple fins.
- The Type 2 SRAM cell area is $0.128 \mu\text{m}^2$
- The width of Type 2 SRAM cell in bitline direction is the same as Type 1 SRAM cell but the overall cell area is about 15% larger.
- Bigger cell size, with multiple pull-down transistors in parallel suggests that Type 2 SRAM was most likely optimized for speed (L1 or L2 cache).

3.3 Cross-sectional Analysis of 6T SRAM Type 1 Cell in Bitline Direction

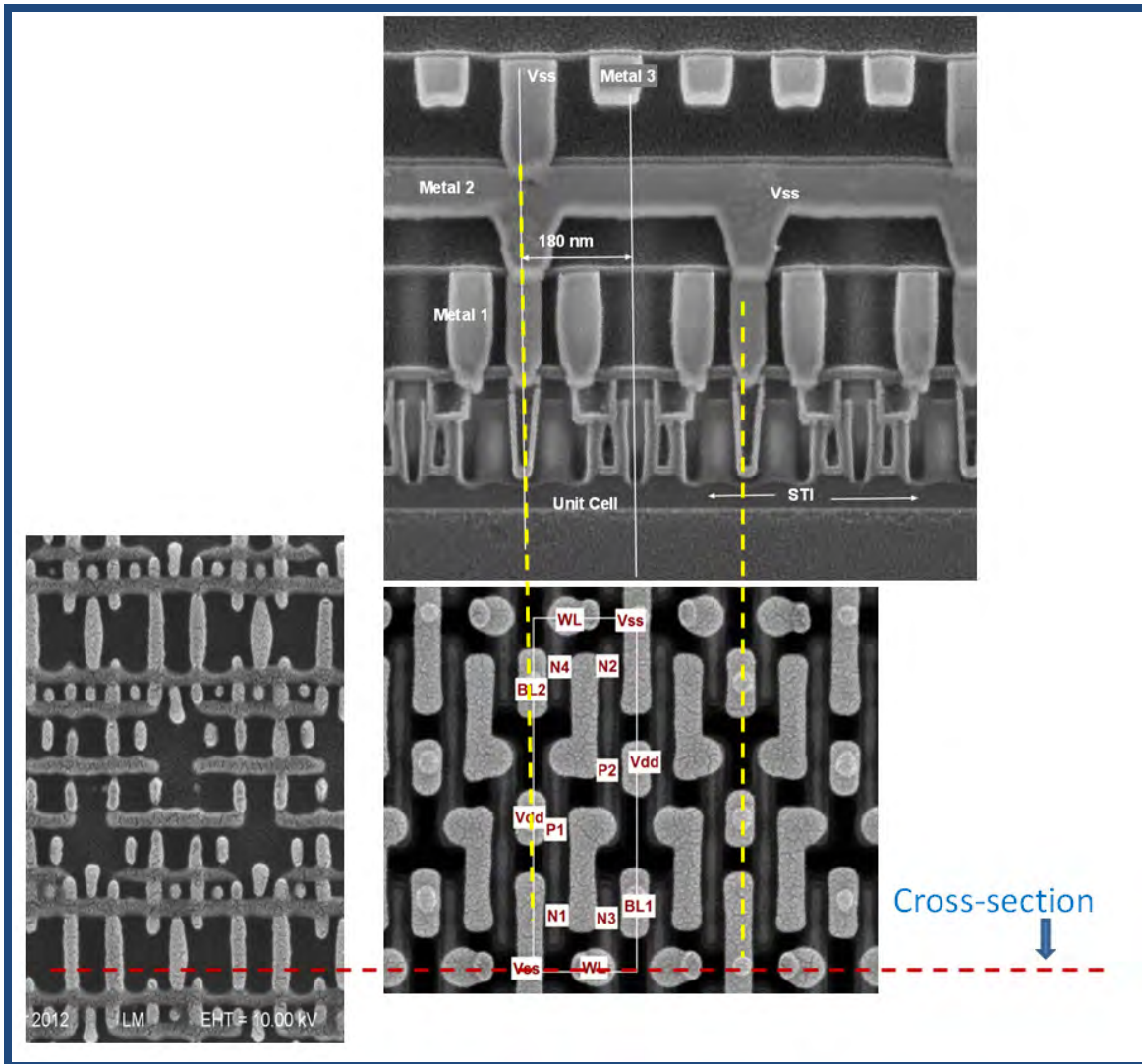


Figure 3.3.1: SEM cross-section of the SRAM cell in the BL direction through Vss contacts.

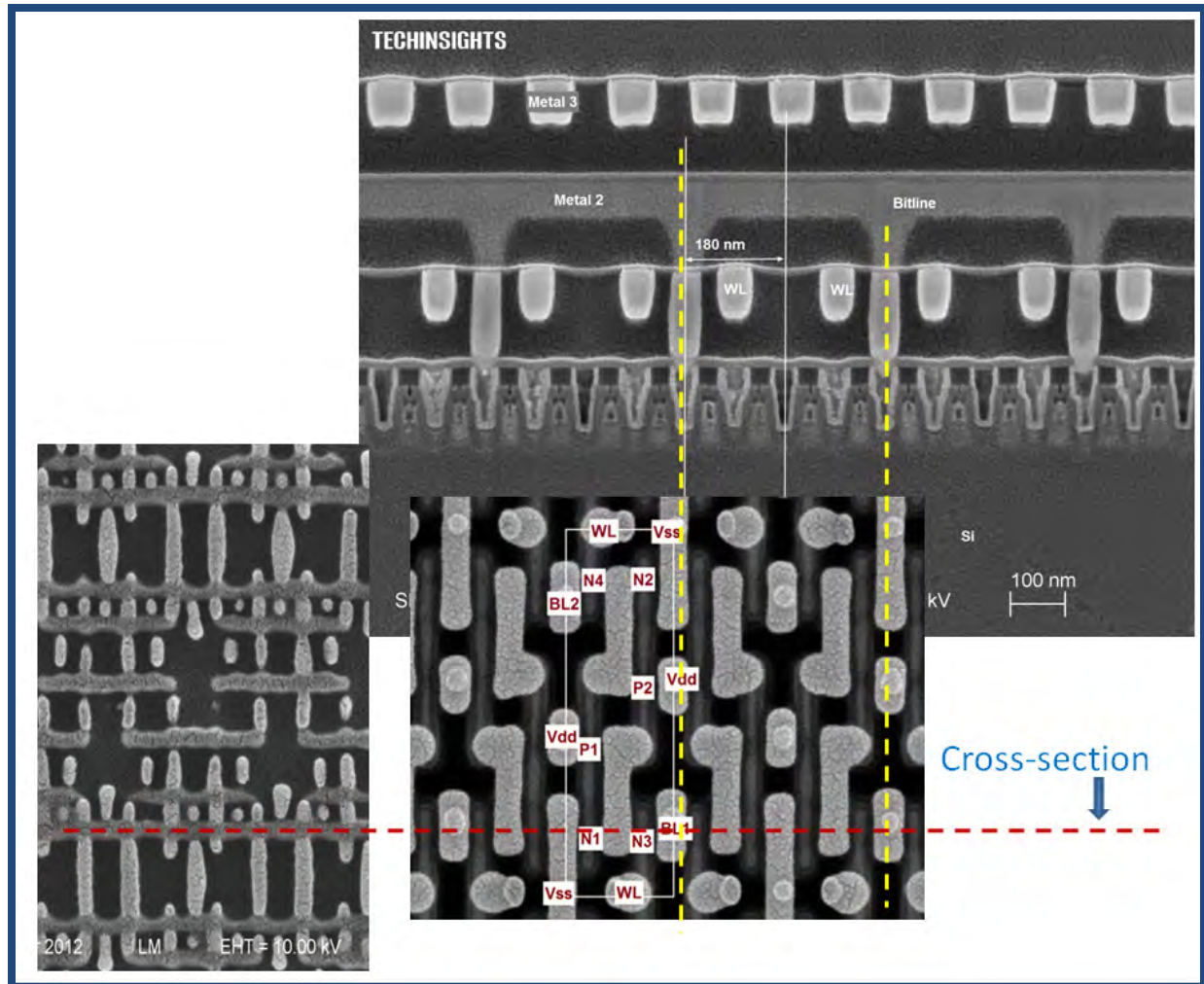


Figure 3.3.2: SEM cross-section of the SRAM array in the BL direction through BL contacts.

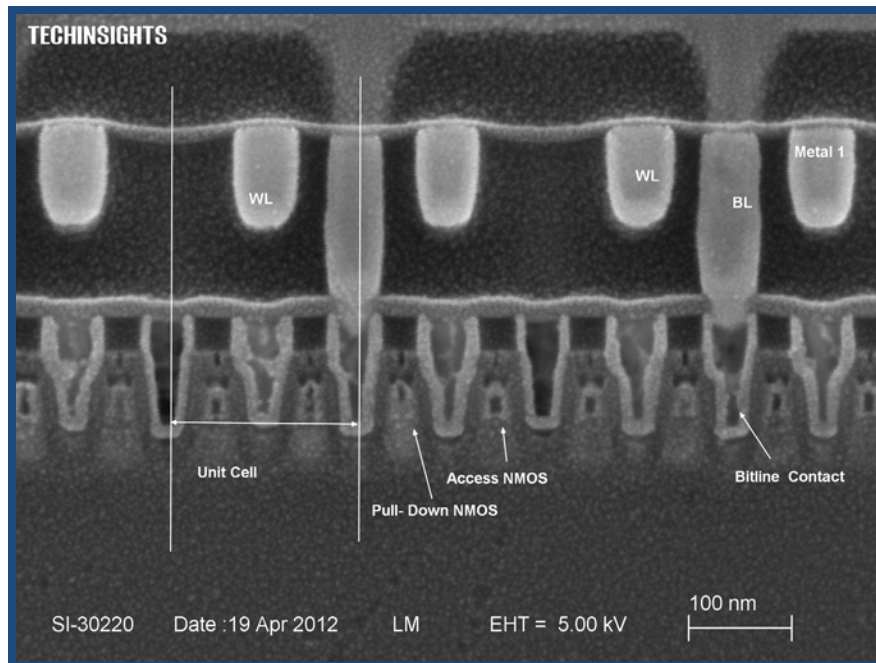


Figure 3.3.3: SEM cross-section of the SRAM array in the BL direction through BL contacts (Type 1 6T SRAM, high magnification).

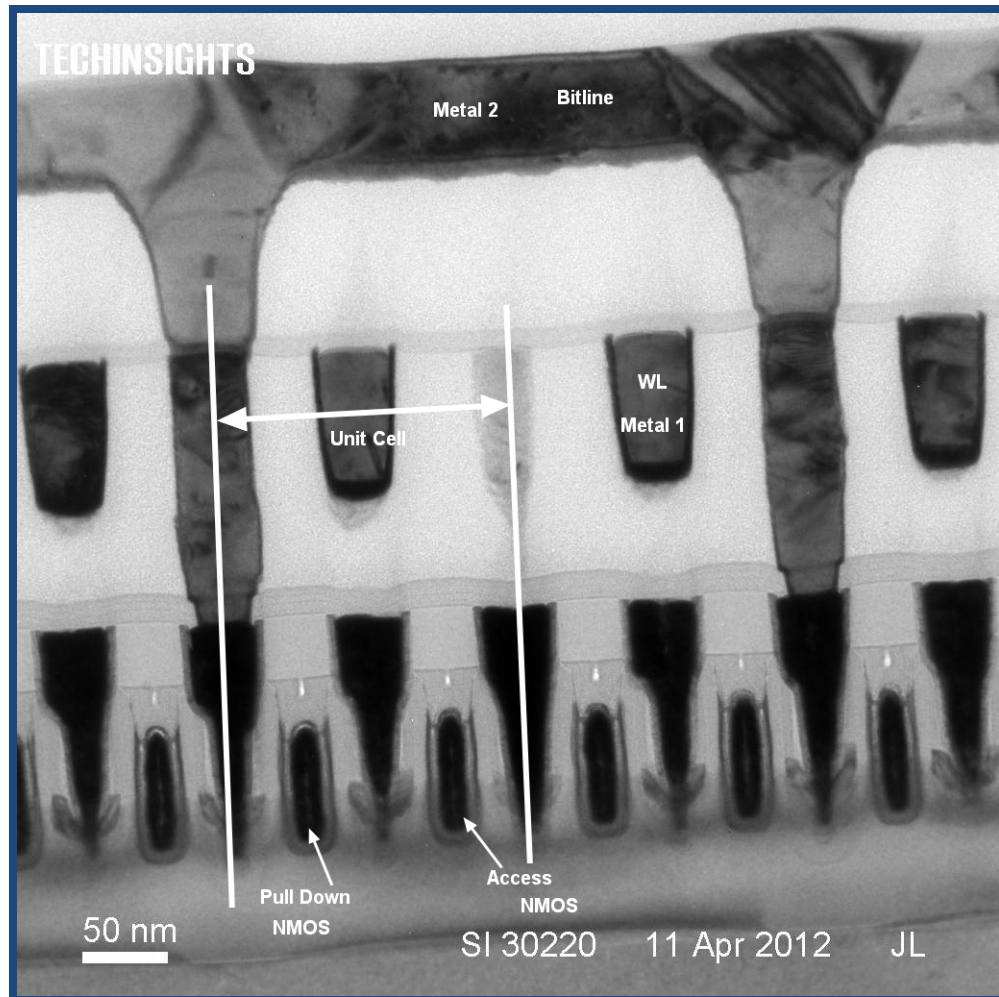


Figure 3.3.4: Cross-section of the SRAM array in the BL direction through BL contacts (TEM).

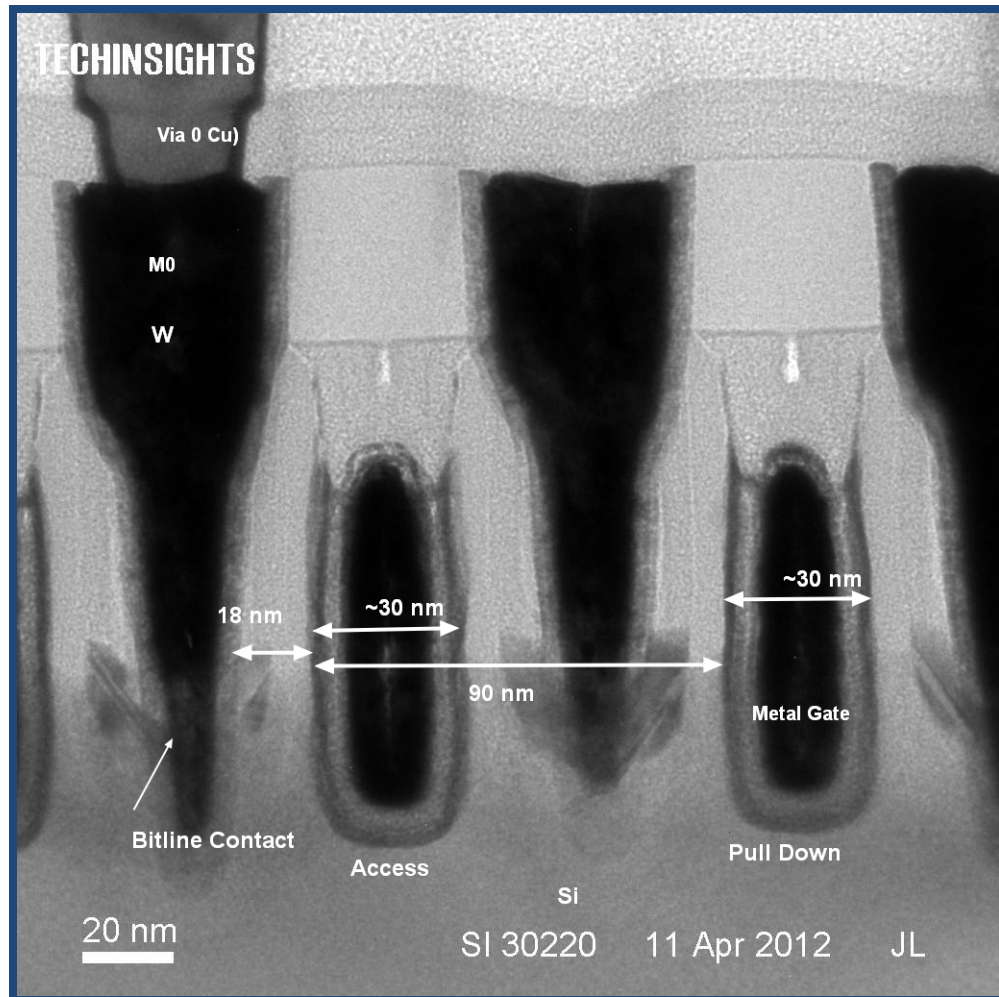


Figure 3.3.5: Cross-section of the SRAM array in the BL direction through BL contacts (high magnification TEM).

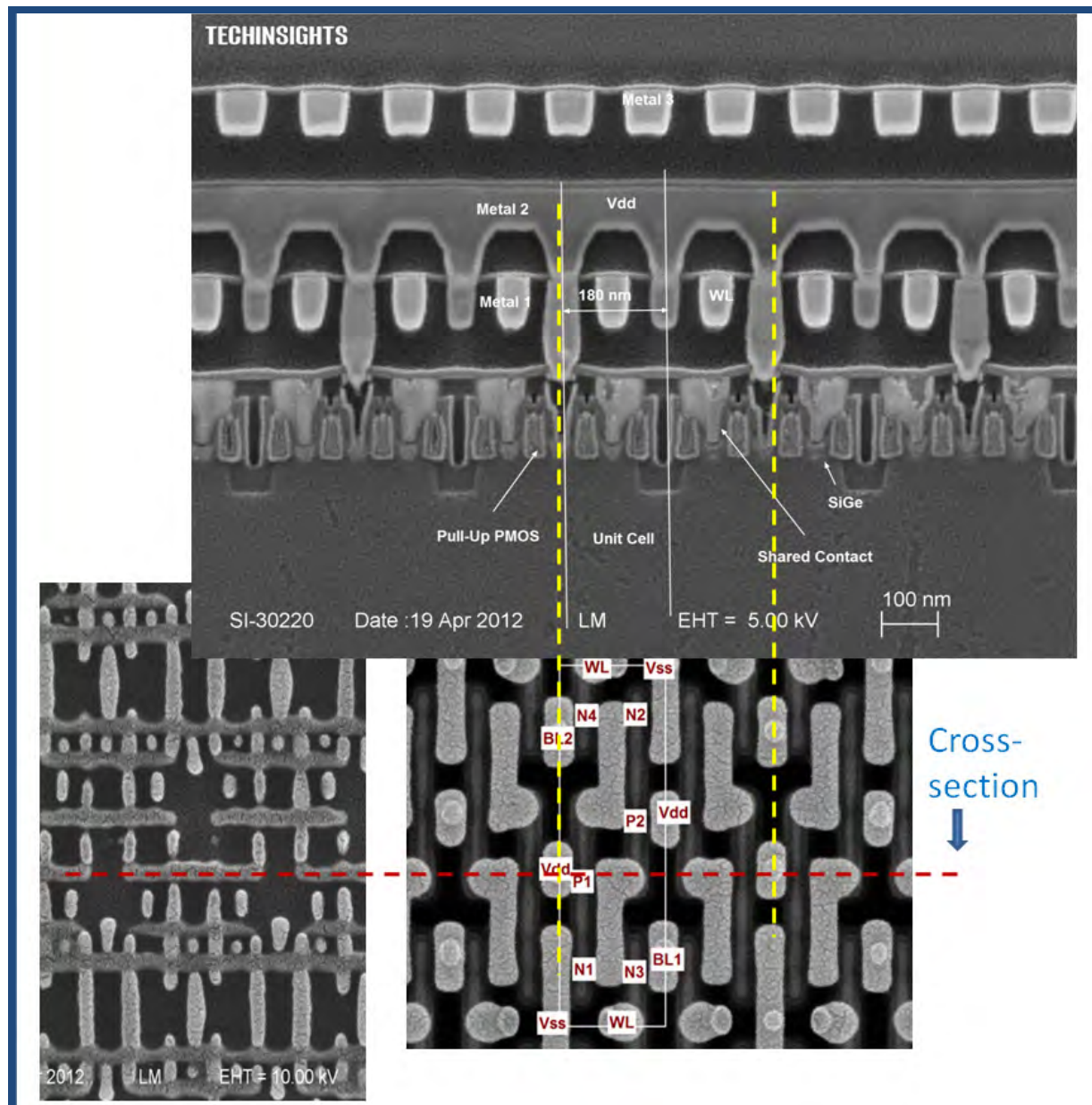


Figure 3.3.6: Cross-section of the Type 1 6T SRAM array in the BL direction through Vdd contacts (SEM).

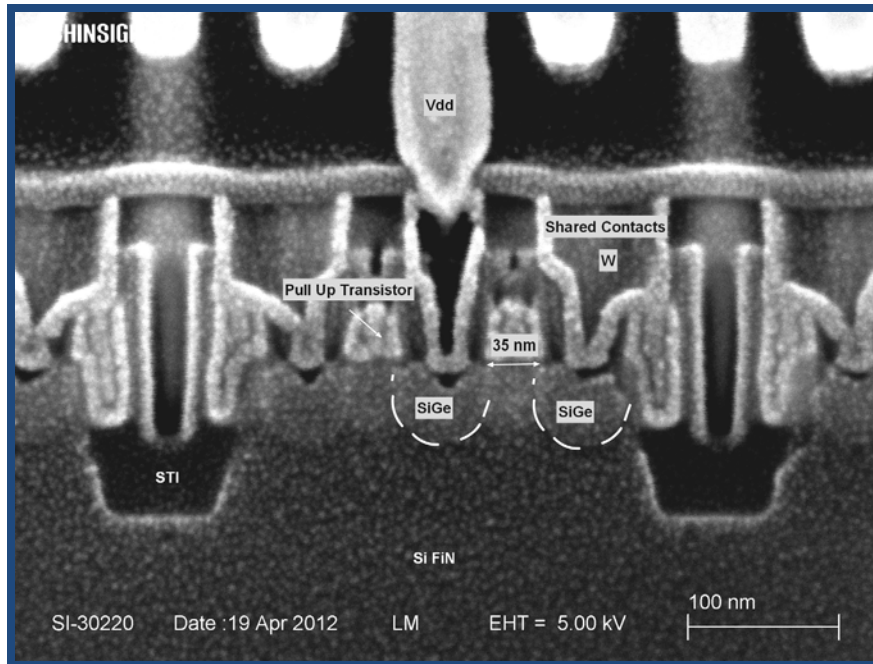


Figure 3.3.7: Cross-section of the SRAM array in the BL direction through Vdd contacts (high magnification SEM).

Feature	Dimension	Unit
SRAM cell width	180	nm
NMOS pull-down and access transistor gate length	32	nm
PMOS Pull-up gate length	35	nm

Table 3.3.1: SRAM transistor gate lengths.

Comments

- SEM cross-section of the SRAM array in bitline (BL) direction through BL contacts and Vdd contacts show that contacts are landing on epitaxial Si island and SiGe island formed on Si fins.
- The gate length of 'access' and 'pull down' transistors is about 30 nm.
- Pull-up transistor has a gate length of 35 nm, SEM cross-section).
- Vss line implemented at metal 2 and metal 3 level and makes contact to metal 2 and to metal 0.
- Vdd line implemented at metal 2 and makes contact to pull-up PMOS transistors.
- One side of the shared contact plug is in contact with raised SiGe region of the PMOS transistor while another side provides a contact to the metal gate of another PMOS pull-up transistor.

3.4 Cross-sectional Analysis of 6T SRAM Type 1 Cell in WordLine Direction

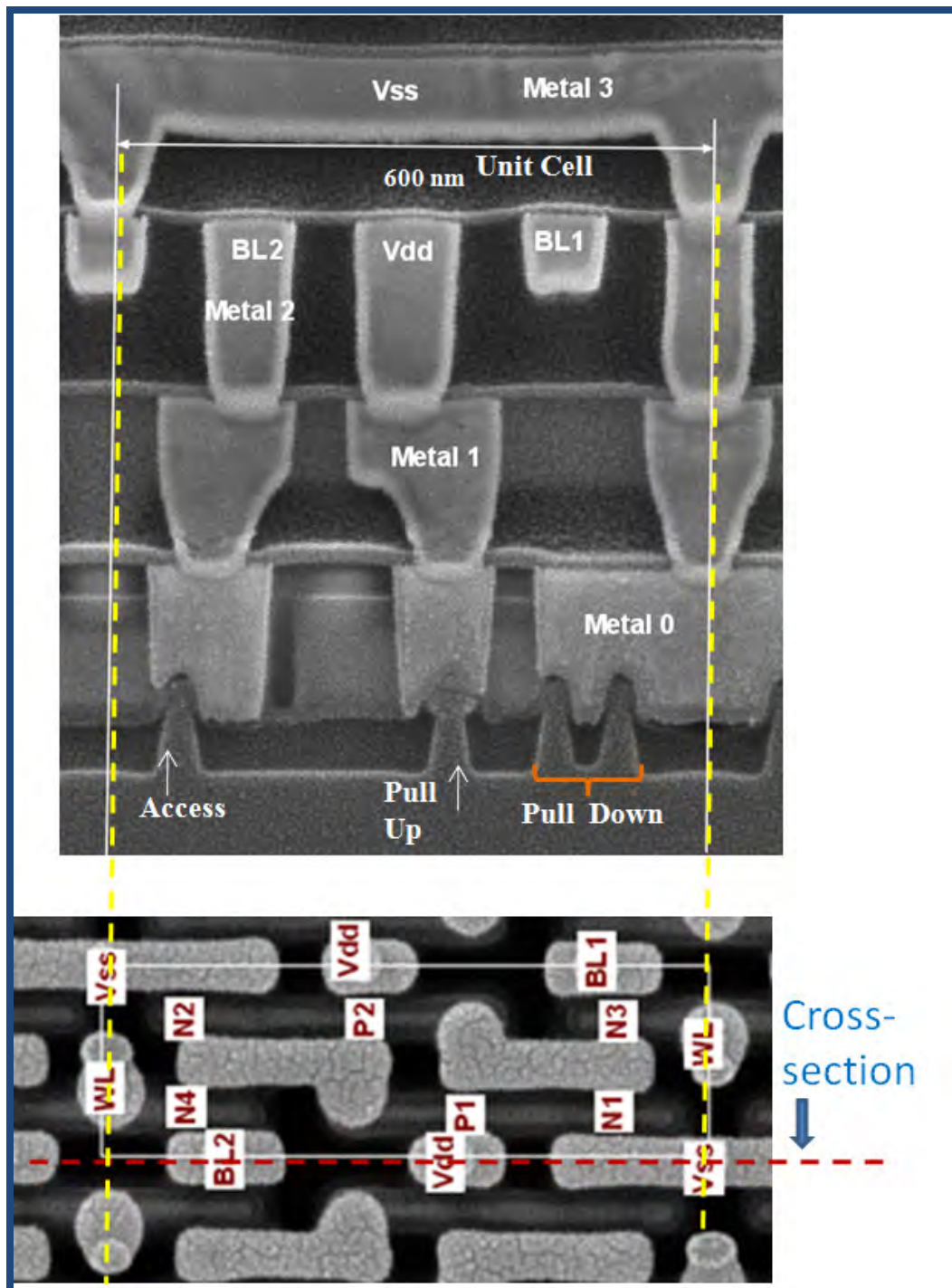


Figure 3.4.1: Cross-section of the SRAM array in the wordline (WL) direction through Vss contacts (SEM).

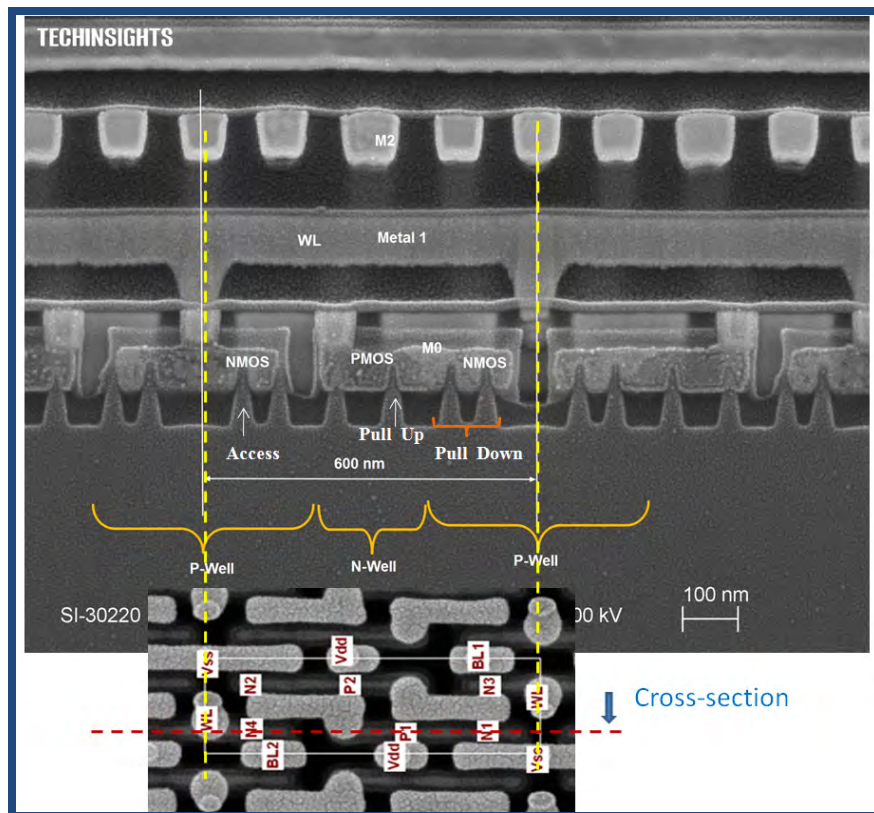


Figure 3.4.2: Cross-section of the SRAM array in the wordline direction through WL contacts (SEM).

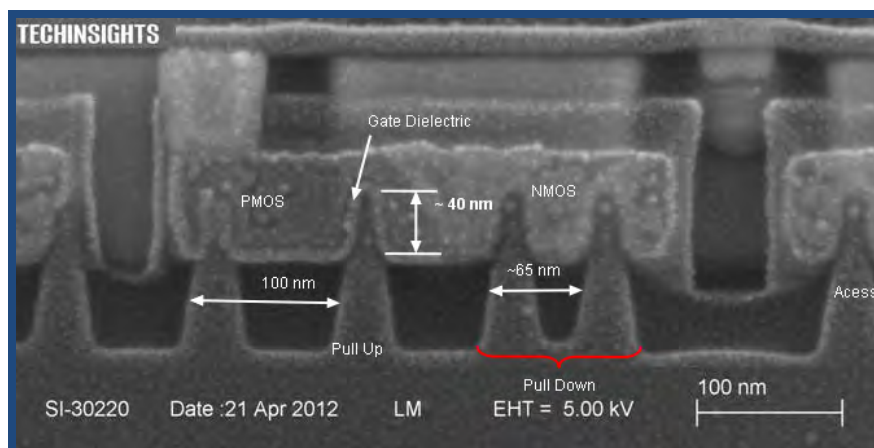


Figure 3.4.3: Cross-section of an SRAM cell along a common gate in the wordline direction (high magnification SEM).

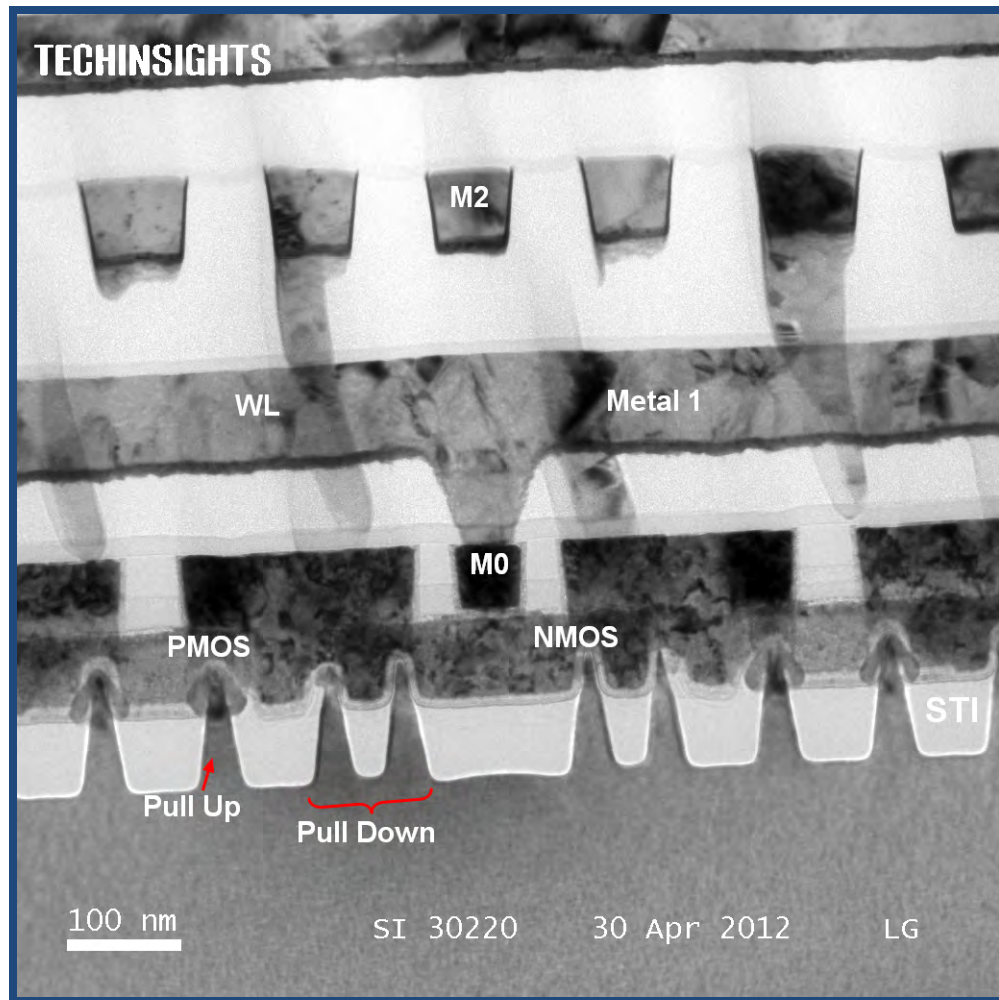


Figure 3.4.4: Cross-section of an SRAM cell along a common gate in the wordline direction (TEM).

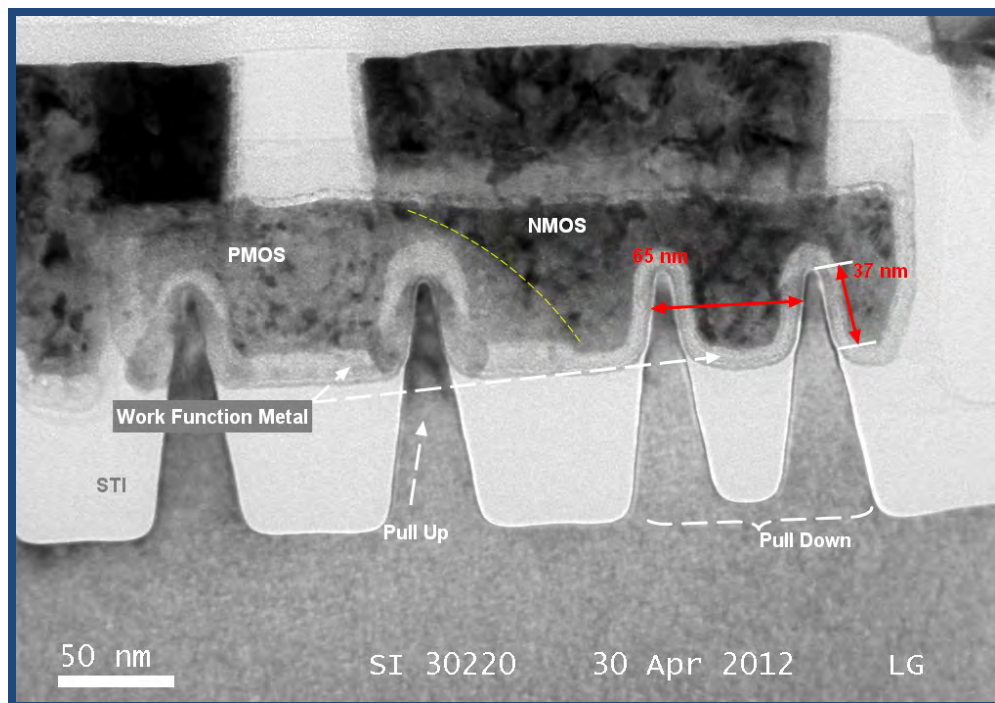


Figure 3.4.5: Cross-section of an SRAM cell along a common gate in the wordline direction (high magnification TEM).

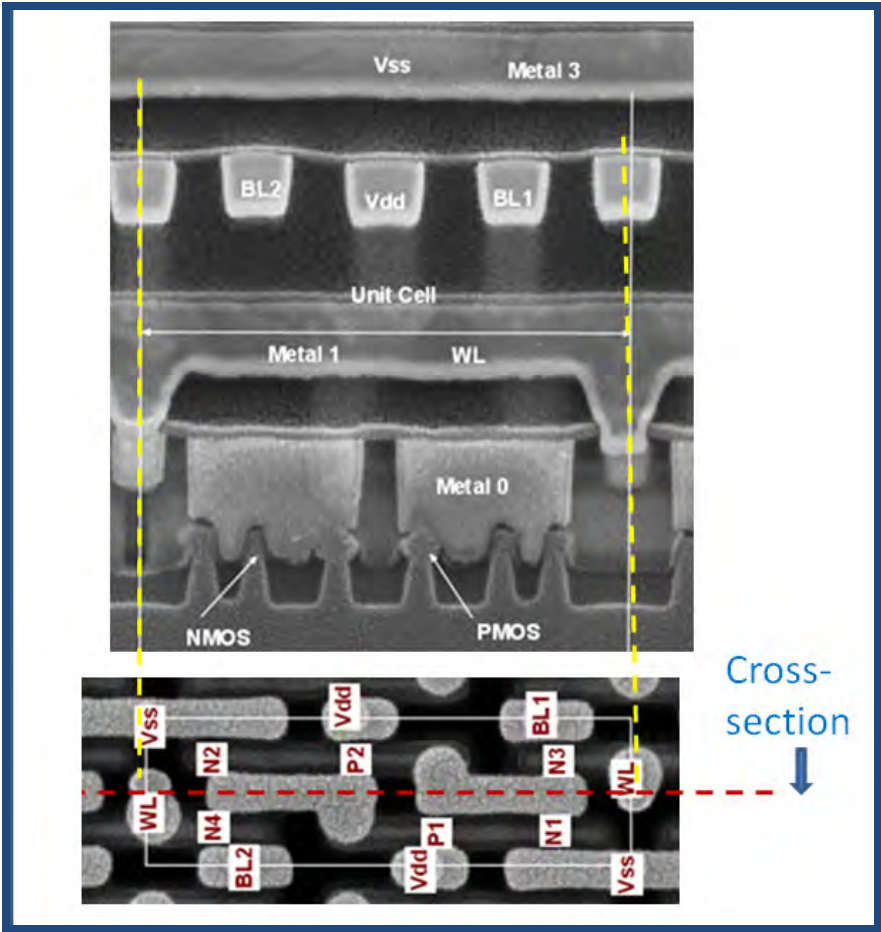


Figure 3.4.6: Cross-section of the SRAM array in the wordline direction through M0 cross-couples (SEM).

Feature	Dimension	Unit
SRAM cell height	0.60	µm
NMOS pull-down gate width	~0.16 (0.08 × 2)	µm
NMOS access gate width	~0.08	µm
PMOS pull-up gate width	~0.08	µm

Table 3.4.1: SRAM transistor gate widths.

Comments
- Type 1 6T SRAM pull-down NMOS transistors use two fins so their gate width is doubled compared to access and pull-up transistors; - In the SEM cross-section through the wordline contacts, a transition from PMOS to NMOS is seen in the common metal gate.

3.5 Overview of Intel's 6T SRAM memory

In this section, the evolution 6T SRAM cells in the last four generations of Intel processor is discussed briefly. These four generations (65 nm, 45 nm, 32 nm and 22 nm) all use 193 nm lithography and all use SiGe for mobility enhancement in PMOS transistors. The 65 nm node was almost identical to 90 nm node which also had SiGe for PMOS transistors.

Usually, the square root of SRAM cell-area scales linearly with gate length so this is also compared for the devices. The normalized cell area, which is the cell area divided by the square of gate length gives a rough indication of the design efficiency and the usage of the die floor space. Generally, a lower number suggests a better design. Similarly, the ratio of transistor width to length gives a rough estimation of stability in terms of signal to noise ratio (SNR)³. The embedded memory may be designed for speed or for low power and the design rules can vary but usually the width is larger than the length of the transistor.

In advanced technology nodes, the degradation of read and write stability at low operating voltages is a challenge. In planar CMOS SRAM design, device dimensions like gate width and gate length (W/L) of the pull down (PD), access (AC) and pull up (PU) are carefully designed to have optimum cell stability. Usually, the PD devices have the largest W/L ratio and are chosen to have stronger drive currents than AC devices. In most cases, the widths of pull down transistors are greater than the widths of access transistors. The current ratio of I_{PD}/I_{AC} reflecting geometric device dimension is known as beta ratio. Therefore, the ratio W/L of different devices is also compared.

As technology continues to be scaled, gate length and gate pitch have significant lithographic restrictions. One of the dire consequences is requiring uniform patterning. This may result in SRAM cells with identical gate-length and gate width, which could have an impact on pull-down and access transistor currents. By using Trigate FinFET structures this problem of equal width can be partially solved; depending on the requirement, a transistor with multiple fins may be used to increase the widths and at the same time have similar gate lengths and heights^{4, 5}.

³ FinFETs and other Multi-gate transistors, by Jean Pierre Colinge; Springer Publications.

⁴ Method and Apparatus for Improving Stability of a 6T CMOS SRAM cell;
(Intel patent US7445980)

⁵ Unity Beta Ratio Tri-gate Transistor SRAM (Intel Patent US7825437)

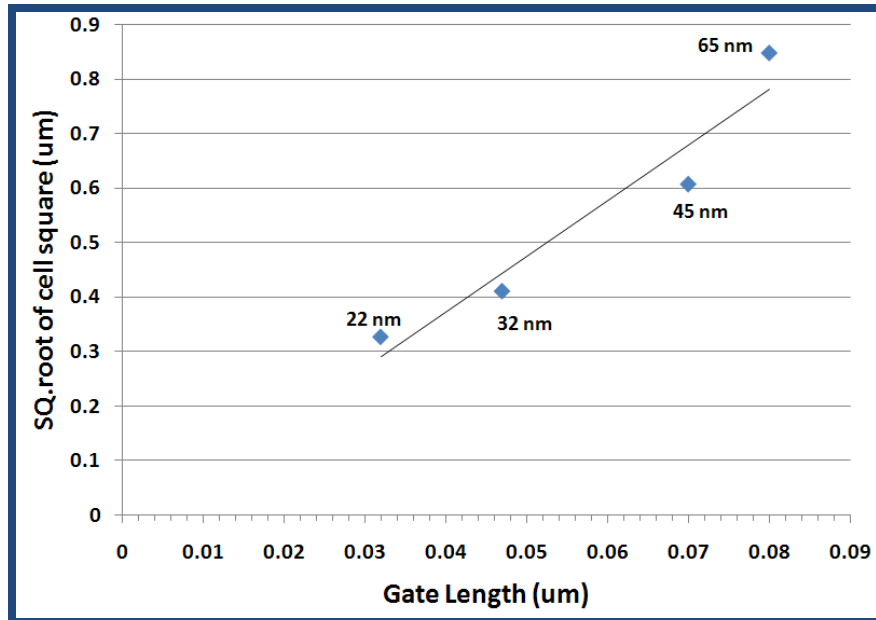


Figure 3.5.1: Square root of cell area as a function of gate length for four generations of Intel processors.

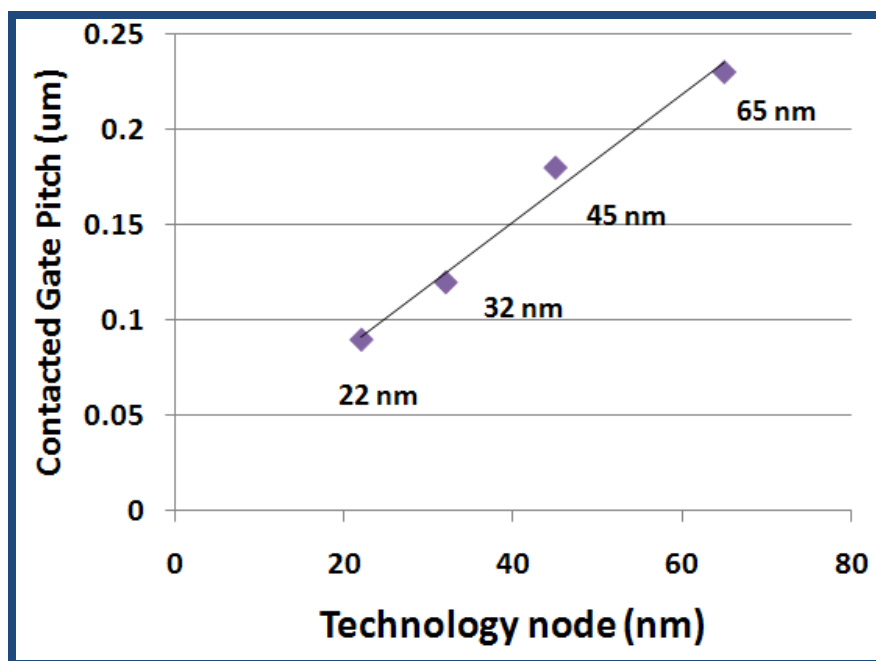


Figure 3.5.2: Contacted gate pitch as a function of technology node for four generations of Intel processors.

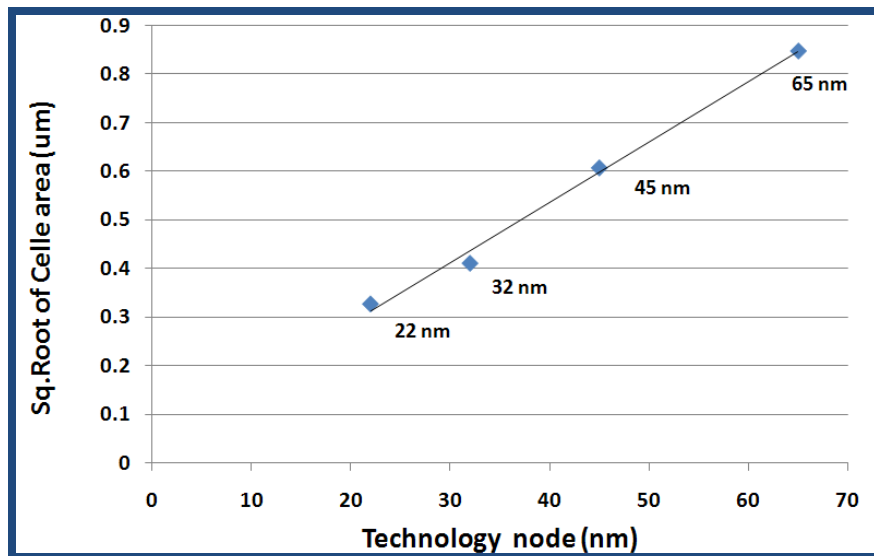


Figure 3.5.3: Square root of cell area as a function of technology node for four generations of Intel processors.

Node	65 nm	45 nm	32 nm	22 nm
Lithography	193 nm dry	193 nm dry	193 nm immersion + double patterning	193 nm immersion + double patterning
Process	SiGe for PMOS; Poly gates; W contact; M1 in Cu	SiGe for PMOS; Metal gates; W contact; M1 in Cu	SiGe PMOS; eSi NMOS; Metal gates, M0 level in Cu; W contact; M1 in Cu	Tri-gate transistor; SiGe PMOS; eSi NMOS; Metal gates, M0 level in W; W contact; M1 in Cu
Vss	Metal 2	Metal 2 & 3	Metal 2	Metal 2
Vdd	Metal 2	Metal 1 & 2 same dir.	Metal 2	Metal 2
BL	Metal 2	Metal 2	Metal 2	Metal 2
WL	Metal 3	Metal 3	Metal 1	Metal 1
Minimum NMOS Gate Length in SRAM (nm)	80	70	47	32
Contacted Gate pitch: NMOS_SRAM (nm)	230	180	120	90
Cell Dimenions	Length [Bitline dir.] (nm) Width [Wordline dir.] (nm) Cell Area (um^2)	Length [Bitline dir.] (nm) Width [Wordline dir.] (nm) Cell Area (um^2)	Length [Bitline dir.] (nm) Width [Wordline dir.] (nm) Cell Area (um^2)	Length [Bitline dir.] (nm) Width [Wordline dir.] (nm) Cell Area (um^2)
Cell Area	0.48 1.5 0.72	0.36 1.03 0.37	0.25 0.67 0.17	0.18 0.6 0.11
Normalized Cell Area (cell Area/ Gate length ²)	113	76	76	105
Transistor Channel Dimensions	Length (nm) Width (nm) W/L	Length (nm) Width (nm) W/L	Length (nm) Width (nm) W/L	Length (nm) Width (nm) W/L
NMOS Pull Down	80 230 2.9	74 130 1.8	47 90 1.9	32 160 5.0
PMOS Pull Up	60 110 1.8	70 70 1.0	47 58 1.2	35 80 2.3
NMOS Access	80 110 1.4	74 80 1.1	47 58 1.2	32 80 2.5

Table 3.5.1: Overview of Intel SRAM transistor's process.

Comments

- The cell area decreases about 0.7 times compared to previous technology node as expected from Moore's law;
- The contacted gate pitch decreases linearly with every technology node;
- For 45 nm node, the normalized cell area dropped by 25% compared to 65 nm node. The introduction of metal gates and high-k improved the drive current, reduced the leakage and improved the overall efficiency;
- However, the ratio of transistor width to length of 45 nm node was worse than that of 65 nm node;
- The 32 nm node introduced the metal 0 level and changed the wiring position of bitlines, wordlines, Vss and Vdd lines and improved slightly the W/L ratio;
- The SRAM in 22 nm node kept the same wiring configuration for BL, WL, Vdd and Vss, as in 32 nm node and also introduced the Tri-Gate (FinFET) structure, which made a dramatic improvement in W/L ratio;
- The pull down transistor's W/L is twice of that of access transistor;
- The good linearity of cell area vs. technology node and the contacted pitch vs. technology node are confirming that the device Ivy Bridge is indeed of 22 nm process node.

4.0 Critical Dimensions

<i>Layer</i>	<i>Vertical Dimension</i>	<i>Unit</i>
P-Epitaxial layer	2.6	μm
N-well	0.2	μm
Wide STI depth (under gate)	60	nm
Minimum STI depth (narrow STI under gate)	51.5	nm
STI sidewall angle	81	degree
Maximum observed silicon fin height, PMOS	38	nm
Minimum observed silicon fin height, NMOS	35	nm
Fin top rounding radius	3.7	nm
Fin sidewall angle	84	grad
PMOS gate dielectric thickness	2.6	nm
SiO thickness	0.6	nm
HfO thickness	2	nm
PMOS gate stack thickness	18	nm
TiN layer above HfO	1	nm
TaAl barrier	1	nm
TiN layer	4	nm
AlCO layer	3.5	nm
TiAlN layer	2.5	nm
W gate fill	6	nm
NMOS gate dielectric thickness	2.6	nm
SiO thickness	0.6	nm
HfO thickness	2	nm
NMOS gate stack thickness	13.5	nm
TiN layer above HfO	1	nm
TaAl barrier	1	nm
AlTiCO work function metal	2.9	nm
TiN layer	2.6	nm
W gate fill	6	nm
Maximum observed embedded SiGe height, PMOS	55	nm
Maximum observed embedded Si height, NMOS	45	nm
PMD maximum thickness	160	nm
SiN contact etch-stop layer, CESL	8	nm
Oxide 1 (CMP planarized)	115	nm
Oxide 2	37	nm
Metal 0 (W) contact overall depth	150	nm
Contact TiN liner thickness at sidewall	6	nm
Metal 0 thickness	50	nm
Metal 1 thickness	95	nm

<i>Layer</i>	<i>Vertical Dimension</i>	<i>Unit</i>
Metal 2 thickness	55	nm
Metal 3 thickness	65	nm
Metal 4 thickness	110	nm
Metal 5 thickness	150	nm
Metal 6 thickness	270	nm
Metal 7 thickness	260	nm
Metal 8 thickness	450	nm
Metal 9 thickness	6.40	μm
IMD 0 cap layer, SiCN	20	nm
IMD 0 dielectric layer, SiOC	135	nm
IMD 1 cap layer, SiOCN	15	nm
IMD 1 dielectric layer, SiOC	170	nm
IMD 2 cap layer, SiOCN	15	nm
IMD 2 dielectric layer, SiOC	165	nm
IMD 3 cap layer, SiOCN	15	nm
IMD 3 dielectric layer, SiOC	180	nm
IMD 4 cap layer, SiOCN	15	nm
IMD 4 dielectric layer, SiOC	270	nm
IMD 5 cap layer, SiOCN	15	nm
IMD 5 dielectric layer, SiOC	450	nm
IMD 6 cap layer, SiCN	70	nm
IMD 6 dielectric layer, SiOC	470	nm
IMD 7 cap layer, SiCN	85	nm
IMD 7 dielectric layer, SiOC	700	nm
IMD 8 cap layer, SiCN	160	nm
IMD 8 dielectric layer, SiCN	1.54	μm
Passivation layer, SiN	1.2	μm
Polyimide die coat thickness	15	μm
Die thickness	0.48	mm

Table 4.0.1: Critical vertical dimensions.

<i>Feature</i>	<i>Horizontal Dimension</i>	<i>Unit</i>
Minimum observed STI width	40	nm
Fin-defining STI pitch	60	nm
Minimum observed fin width, bottom	18.3	nm
Minimum observed fin width, top	6.9	nm
Effective PMOS transistor channel width (sidewall + top + sidewall)	80	nm
Silicon fin pitch	60	nm
Minimum observed fin length, core logic	205	nm
Minimum observed space between fins in the fin direction	65	nm
Maximum observed fin length	3.0	μm
Embedded SiGe maximum width (across fin)	65	nm
Embedded SiGe maximum length (along fin)	50	nm
Embedded Si maximum width (across fin)	50	nm
Embedded Si maximum length (along fin)	50	nm
Standard cell height	0.84	μm
Minimum observed gate pitch (core logic and SRAM)	90	nm
Maximum observed gate pitch (I/O region)	180	nm
Minimum observed Tri-Gate transistor length (core logic)	0.27	μm
Minimum observed Tri-Gate transistor width (core logic)	0.40	μm
Minimum observed Tri-Gate transistor area (core logic)	0.108	μm ²
Minimum observed metal 0 contact width at top	50	nm
Metal 0 contact width at bottom	25	nm
Minimum observed metal 0 contact pitch, core logic	90	nm
Maximum observed metal 0 contact pitch, I/O region	180	nm
Minimum observed metal 0 width	50	nm
Minimum observed metal 0 pitch	90	nm
Minimum observed metal 1 width	55	nm
Minimum observed metal 1 pitch	92	nm
Minimum observed metal 2 width	55	nm
Minimum observed metal 2 pitch	81	nm
Minimum observed metal 3 width	65	nm
Minimum observed metal 3 pitch	100	nm
Minimum observed metal 4 width	70	nm
Minimum observed metal 4 pitch	110	nm
Minimum observed metal 5 width	100	nm
Minimum observed metal 5 pitch	165	nm
Minimum observed metal 6 width	140	nm
Minimum observed metal 6 pitch	240	nm
Minimum observed metal 7 width	210	nm

<i>Feature</i>	<i>Horizontal Dimension</i>	<i>Unit</i>
Minimum observed metal 7 pitch	360	nm
Minimum observed metal 8 width	230	nm
Minimum observed metal 8 pitch	365	nm
Minimum observed metal 9 width	7.85	μm
Minimum observed metal 9 pitch	13.85	μm
Minimum observed via 0 width at bottom	42	nm
Minimum observed via 0 pitch	90	nm
Minimum observed via 1 width at bottom	60	nm
Minimum observed via 1 pitch	180	nm
Minimum observed via 2 width at bottom	60	nm
Minimum observed via 2 pitch	115	nm
Minimum observed via 3 width at bottom	65	nm
Minimum observed via 3 pitch	165	nm
Minimum observed via 4 width at bottom	100	nm
Minimum observed via 4 pitch	225	nm
Minimum observed via 5 width at bottom	120	nm
Minimum observed via 5 pitch	330	nm
Minimum observed via 6 width at bottom	140	nm
Minimum observed via 6 pitch	325	nm
Minimum observed via 7 width at bottom	180	nm
Minimum observed via 7 pitch	660	nm
Minimum observed via 8 width at bottom	0.98	μm
Minimum observed via 8 pitch	13.6	μm
6T SRAM-1 cell height	0.60	μm
6T SRAM-1 cell width	0.18	μm
6T SRAM-1 cell area	0.108	μm ²
Access NMOS Tri-Gate transistor gate length	32	nm
Pull-down NMOS Tri-Gate transistor gate length	32	nm
Pull-up PMOS Tri-Gate transistor gate length	~35	nm
Access NMOS Tri-Gate transistor gate width	80	nm
Pull-down NMOS Tri-Gate transistor gate width	160	nm
6T SRAM-2 cell height	0.71	μm
6T SRAM-2 cell width	0.18	μm
6T SRAM-2 cell area	0.128	μm ²
Minimum observed pad opening width	10	μm
Minimum observed pad opening length	27	μm
Minimum observed pad opening pitch	128	μm

<i>Feature</i>	<i>Horizontal Dimension</i>	<i>Unit</i>
Pull-up PMOS Tri-Gate transistor gate width	80	nm
Die width	19.6	mm
Die height	8.0	mm
Die area	157	mm ²

Table 4.0.2: Critical horizontal dimensions.

5.0 Major Findings

The Intel i5-CORE i5-3550 Ivy Bridge processor die is fabricated using 22 nm process with Tri-Gate transistors and 9 copper metal levels. Traditional planar MOS transistor is replaced with a multilayer metal gate that is wrapped around a thin three-dimensional silicon fin that rises up vertically from the silicon substrate. A 2.6 nm thick high-k HfO/SiO dielectric separates the silicon fin from the metal gate on each of the three sides of the fin. PMOS metal gate layers. A TiN protective layer and TaAl barrier are then formed followed by multi-layer TiN/AlCO/TiAlN work function (WF) metal stack deposition in both PMOS and NMOS gate trenches. This metal stack is left for PMOS gates but is selectively removed from NMOS gates and replaced with AlTiCO/TiN layers. Then both PMOS and NMOS gates are filled with tungsten.

Before metal gate formation, embedded SiGe and Si:C regions have been epitaxially grown in the cavities formed in the source/drain regions adjacent to sacrificial poly gates to provide compressive and tensile strain to the channel parts of the PMOS and NMOS fins.

Tungsten-based metal 0 is used for local interconnects and contacts. Lower two copper-based dual damascene metal levels with the 90 nm pitch use an ultra-low-k carbon-doped oxide and carbon-nitride for IMD levels while the upper copper metal levels use low-k oxide and SiCN for respective IMD levels. Aluminum was found at the copper-cap interface for the lower metal levels M1, M2, M5 (and assumed for M3, M4) likely to improve the electro-migration reliability. Thick non-damascene copper metal 9 is for copper pillar bumping (CPB) technology. Decoupling MIM capacitors have been formed between M8 and M9 levels; they use TiN plates and HfO capacitor dielectric.

Six-transistor SRAM-1 cell ($0.18 \times 0.60 = 0.108 \mu\text{m}^2$) arrays optimized for density and used in L3 cache while six-transistor SRAM-2 cell ($0.18 \times 0.71 = 0.128 \mu\text{m}^2$) arrays optimized for speed and used in processor graphics, four cores and other regions of the die. Both SRAM cells have a litho-friendly configuration, with the gates oriented in the same wordline direction. Access NMOS and pull-up PMOS transistors are single fin transistors while pull-down NMOS are double-fin devices in the SRAM-1 cell and triple-fin devices in the SRAM-1 cell. SRAM-1 cell area of $0.108 \mu\text{m}^2$ and contacted gate pitch of 90 nm indicate a 22 nm technology node.

5.1 Front-End-Of-Line (FEOL) Process Features

- 1st generation Tri-Gate process technology
 - Three-dimensional Tri-Gate transistor (FinFET-type)
 - Rounded silicon fins are 18 nm thick at foot, 7 nm thick at top and 38 nm high
 - “Structured layout” at fin level
 - All fins constrained to be parallel and have a restricted/fixed pitch of 60 nm
- 3rd generation high-k dielectric and metal gate
 - Hafnium oxide (2 nm thick) high-k gate dielectric with the bottom interface silicon oxide layer (0.6 nm)

- o Dual work function metal gates:
 - TiN/AlCO/TiAlN for PMOS with TaAl barrier and W body
 - AlTiCO/TiN for NMOS with TaAl barrier and W body
 - o “Structured layout” at gate level
 - o All gates constrained to be parallel and have a pitch of 90 nm
- Gate last (replacement gate) integration
- 5th generation strained silicon engineering
 - o Embedded SiGe for PMOS channel compressive strain
 - o Embedded Si:C for NMOS channel tensile strain
 - o Raised source/drain regions for PMOS and NMOS transistors formed by selective epitaxial processes
- Other FEOL features
 - o Shallow N-wells in P-epi layer grown on P+ silicon substrate
 - o SiCON sidewall spacers and nitride cap layer for NMOS and PMOS transistors
 - o Tungsten-based metal 0 used for local interconnects and contacts
 - o Trench type contacts have 25 nm width at bottom and 90 nm pitch

5.2 Back-End-Of-Line (BEOL) Process Features

- Metallization and Inter-metal Dielectrics
 - o Nine copper dual damascene metal levels
 - o Dense metal 0 to metal 2 lines with 90 nm pitch
 - o Self-aligned aluminum-based barrier is used to improve the copper-cap layer for the lower metal levels
 - o Thick non-damascene copper metal 9
 - o Low-k (SiOC) inter-metal dielectrics with SiCN copper-sealing/etch-stop layers for IMD 1 to IMD 7
 - o SiCN-based IMD 8
- Decoupling MIM capacitors formed between M8 and M9 levels are implemented using TiN plates and HfO capacitor dielectric
- Single layer nitride passivation
- Flip-chip land grid array (FC-LGA) package with copper pillar bumping (CPB) technology

5.3 SRAM (Type 1)

- Six-transistor SRAM cell: $0.18 \times 0.60 = 0.108 \mu\text{m}^2$
 - o Smallest SRAM cell optimized for density and used for L3 cache
 - o Double-fin pull-down NMOS Tri-Gate transistors
 - o Single-fin access NMOS and pull-up PMOS Tri-Gate transistors
 - o “Thin cell” layout with an aspect ratio of 3.3:1
 - o Litho-friendly unidirectional design of silicon fins

- o Litho-friendly unidirectional design of metal gates
- o Tungsten shared contacts for compact cell layout

5.4 SRAM (Type 2)

- Six-transistor SRAM cell: $0.18 \times 0.71 = 0.128 \mu\text{m}^2$
 - o SRAM cell likely optimized for speed and used in processor graphics, cores and other die regions
 - o Triple-fin pull-down NMOS Tri-Gate transistors
 - o Single-fin access NMOS and pull-up PMOS Tri-Gate transistors
 - o “Thin cell” layout with an aspect ratio of 4:1
 - o Litho-friendly unidirectional design of silicon fins
 - o Litho-friendly unidirectional design of metal gates
 - o Tungsten shared contacts for compact cell layout