

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

TAIWAN SEMICONDUCTOR MANUFACTURING COMPANY LTD.,

Petitioner,

v.

MARLIN SEMICONDUCTOR LTD.,

Patent Owner.

IPR2025-01054

U.S. Patent 9,337,193

**PETITION FOR *INTER PARTES* REVIEW OF
U.S. PATENT 9,337,193**

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EXHIBIT LIST

	Description
1001	U.S. Patent 9,337,193 to Chin-I Liao, et al. (“’193 patent”)
1002	File History of U.S. Patent 9,337,193 (“’193 File History”)
1003	Declaration of E. Fred Schubert, Ph.D. in Support of Petition for <i>Inter Partes</i> Review of U.S. Patent 9,337,193
1004	CV of E. Fred Schubert, Ph.D.
1005	U.S. Patent 10,535,735 to Glass, et al. (“Glass”)
1006	U.S. Patent 7,538,387 to Tsai (“Tsai”)
1007	U.S. Patent Publication 2011/0210404 to Su et al. (“Su”)
1008	U.S. Patent 8,399,931 to Liaw, et al. (“Liaw”)
1009	U.S. Patent 8,703,556 to Kelly, et al. (“Kelly”)
1010	U.S. Patent 8,598,003 to Murthy, et al (“Murthy”)
1011	RESERVED
1012	<i>FinFETs and Other Multi-Gate Transistors</i> (J.-P. Colinge ed., 2008) (excerpted)
1013	U.S. Patent 1,745,175 to Lilienfeld (“Lilienfeld”)
1014	<i>Semiconductor Manufacturing Technology</i> (M. Quirk, J. Serda, 1st ed., 2000) (“Quirk/Serda”)
1015	https://semiwiki.com/eda/synopsys/1709-designing-with-finfets/ by Payne
1016	<i>CMOS VLSI Design: A Circuits and Systems Perspective</i> (N. Weste and D. Harris, Third Edition, 2005) (“Weste”)
1017	U.S. Patent 6,413,802 to Hu, et al. (“Hu”)
1018	“Investigation of FinFET devices for 32nm technologies and beyond” to Shang, et al. (2006)
1019	File History of U.S. Patent 9,006,805 (“’805 File History”)
1020	U.S. Patent Publication 2013/0200470 to Liu, et al. (“Liu”)
1021	U.S. Patent 8,455,313 to Basker, et al (“Basker”)

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1022	<i>Microchip Fabrication</i> (P. Van Zant, 5th ed., 2004) (“Van Zant”)
1023	<i>Fundamentals of Semiconductor Fabrication</i> (G. May, S. Sze, 2011) (“May/Sze”)
1024	<i>Handbook of Physical Vapor Deposition (PVD) Processing</i> (D. Mattox, 2 nd Ed. 2010)
1025	Merriam-Webster, https://www.merriam-webster.com/dictionary/merge
1026	TechInsights, “Logic Detailed Structural Analysis of the Intel 22nm Ivy Bridge Processor” (May 2012)
1027	Merriam-Webster, https://www.merriam-webster.com/dictionary/cover
1028	“Highly tensile strained silicon–carbon alloys epitaxially grown into recessed source drain areas of NMOS devices” to M. Bauer, et al. (2006) (“Bauer”)
1029	Plummer, J., et al., “Silicon VLSI Technology: Fundamentals, Practice and Modeling” (Prentice Hall 2000) (“Plummer”)

I. Introduction

Taiwan Semiconductor Manufacturing Company Limited petitions for *inter partes* review of claims 1-11 of U.S. Patent 9,337,193 (“’193 patent”; TSMC-1001). The ’193 patent is directed to “non-planar semiconductor devices with epitaxial structures.” (TSMC-1001, 1:8-10.) FinFETs, a type of non-planar device, were known. The challenged claims recite basic components of prior art FinFET devices (fin-shaped structures, gate structure, source/drain epitaxial structures), a fact acknowledged by the original Patent Owner (“PO”). (§IV.C.) The purported novelty of the ’193 patent therefore lies in the inclusion of a “cap” surrounding the epitaxial region of the source/drain structures, where caps formed on adjacent epitaxial regions merge. However, the general concepts of including a cap and merging adjacent source/drain structures in FinFET devices was also known. (*See, e.g.*, TSMC-1012, 100; TSMC-1017, 2.) The challenged claims are unpatentable.

II. Grounds for Standing

Petitioner certifies the ’193 patent is available for IPR and it is not barred or estopped from requesting IPR.

III. Identification of Challenge

A. Prior Art

The ’193 patent, filed March 4, 2015, is a continuation of U.S. Patent 9,006,805 (“’805 patent”), filed August 7, 2013. Petitioner does not acquiesce the

'193 patent's claims are entitled to priority of the '805 patent. Regardless, each applied reference was filed or published before August 7, 2013.

1. **U.S. Patent 10,535,735 to Glass *et al.*** ("Glass"; TSMC-1005), filed June 29, 2012, is prior art under 35 U.S.C. §102(a)(2).
2. **U.S. Patent No. 7,538,387 to Tsai** ("Tsai"; TSMC-1006), issued May 26, 2009, is prior art under 35 U.S.C. §102(a)(1).
3. **U.S. Patent No. 8,703,556 to Kelly *et al.*** ("Kelly"; TSMC-1009), filed August 30, 2012, is prior art under 35 U.S.C. §102(a)(2).
4. **U.S. Patent No. 8,598,003 to Murthy¹ *et al.*** ("Murthy"; TSMC-1010), filed December 21, 2009, is prior art under 35 U.S.C. §102(a)(2).
5. **U.S. Patent No. 8,399,931 to Liaw *et al.*** ("Liaw"; TSMC-1008), issued March 19, 2013, is prior art under 35 U.S.C. §102(a)(1).
6. **U.S. Patent Publication 2011/0210404 to Su *et al.*** ("Su"; TSMC-1007), published September 1, 2011, is prior art under 35 U.S.C. §102(a)(1).

¹ The front page includes a misspelling of the first named inventor ("Murthty") which was corrected to "Murthy" in a Certificate of Correction.

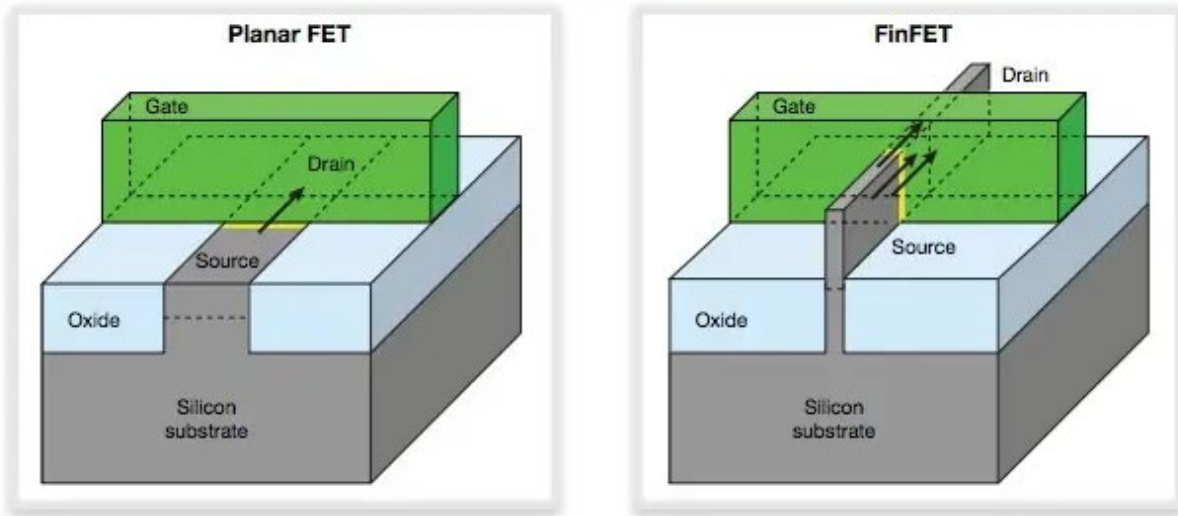
B. Grounds for Challenge

Ground	Challenged Claims	Statutory Basis	Prior Art
1	1-5, 7-9, 11	103	Glass
2	6	103	Glass, Tsai
3	1-10	103	Kelly, Murthy
4	11	103	Kelly, Murthy, Liaw
5	1, 7, 10	103	Su

IV. The '193 Patent

A. Technical Background

A semiconductor device, at its most basic, exploits the properties of semiconductor materials such as silicon. (See TSMC-1003, ¶¶42-53.) Many types of semiconductor devices exist including, e.g., metal-oxide-semiconductor (MOS) transistors (e.g., field effect transistors (FETs)), and memory devices. (TSMC-1029, 33-41.) MOSFETs appear in planar and non-planar arrangements. In a planar arrangement, illustrated below-left, the gate is formed on the top surface of a semiconductor substrate, and the source/drain are formed respectively within the substrate on opposite sides of the gate. (TSMC-1015, 1.) A conductive path, known as the channel, forms close to the top surface of the substrate underneath the gate between the source and drain regions.



One way to increase the effective volume of the channel is to implement a three-dimensional (3D) design, a non-planar transistor, such as a FinFET shown above-right. (TSMC-1015, 1.) In a FinFET (above-right), the gate wraps around a thin structure, called the fin, which extends vertically from the silicon substrate. The channel in a FinFET forms within the fin, with the electric current flowing between the source and the drain in 3D space, as indicated by the black arrows in the figure above. More specifically, the channel forms on the surfaces of the fin underneath the gate. As shown, the fin (and channel) is formed **above** the top surface of the substrate.

During the typical FinFET fabrication process, after fin formation, a gate is formed over the fin. (TSMC-1012, 50.) Subsequently, raised source/drain structures are grown using selective epitaxy. (TSMC-1012, 50.) With a selective epitaxially grown surface, faceting “is different for different surfaces” and

“determines the final shape of the source and drain region.” (TSMC-1012, 90.) For example, “[f]or (100) sidewall surfaces, a rectangular shaped fin is possible,” and for “(110) sidewall surface, the faceting will result in a diamond shaped surface.” (TSMC-1012, 90, Figure 2.37 (below).)

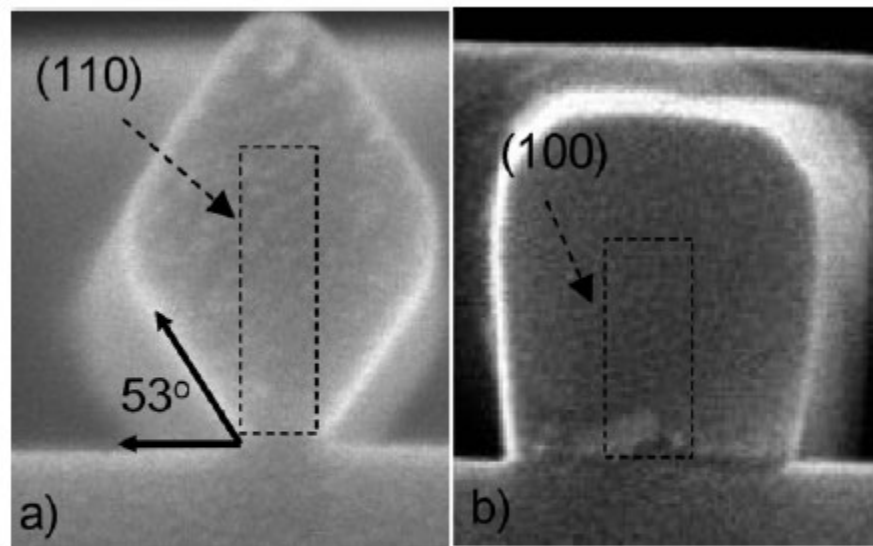


Fig. 2.37. Cross sectional SEM images on fins after epitaxial growth. a) (110) side wall surface result in diamond-shaped fin; b) (100) sidewall surface result in square-shaped fin.

It was well-known before the '193 patent that merging neighboring source/drain epitaxial layers, as shown below, increases the contact area between source/drain contacts and source/drain regions, thereby reducing the contact resistance and eliminating the need for source/drain pads (which severely degrade the layout efficiency of the FinFETs). (TSMC-1012, 100-101.) Thus, years before the '193 patent, merged source/drain structures were recognized as a desirable feature allowing for continued scaling of FinFET devices.

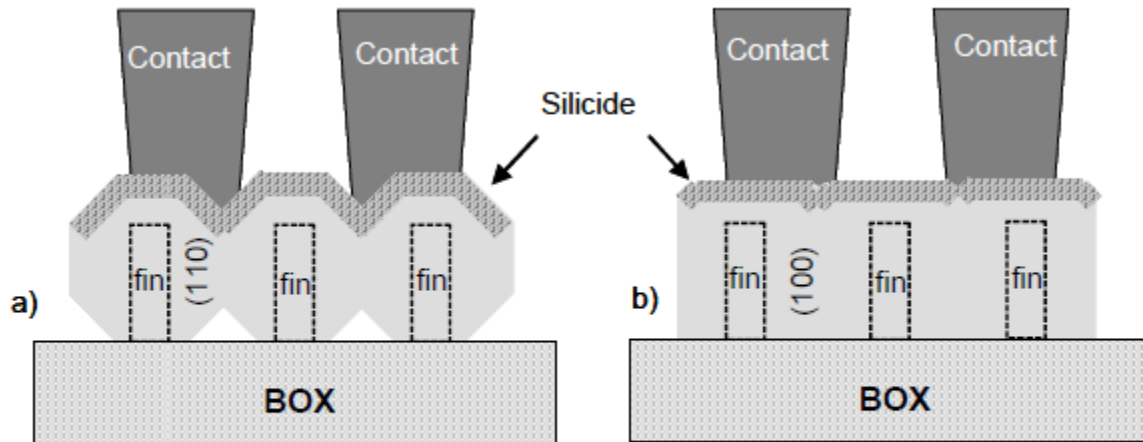


Fig. 2.45. Contact to merged fin: a) if the fin sidewall surface is (110), the contact lands on a wavy topography; b) if the fin sidewall surface is (100), the contact lands on a flat surface.

Colinge, Figure 2.45

B. '193 Patent Overview

The '193 patent's fabrication method follows the well-known process for forming FinFETs. (TSMC-1003, ¶¶45-49, 54; TSMC-1001, 2:53-3:20, 3:39-59.) For example, as shown in Figures 1-2 below, isolating structure 10 (e.g., shallow trench isolation (STI) structure) is formed on substrate 10 having a plurality of fin-shaped structures 12.

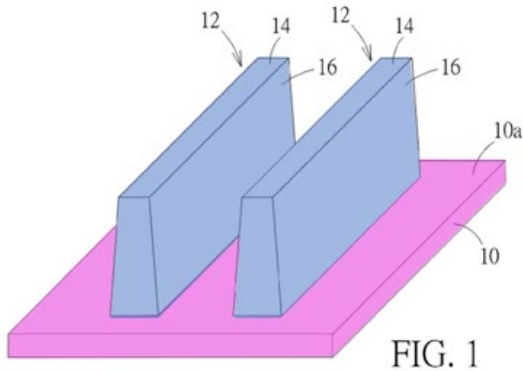


FIG. 1

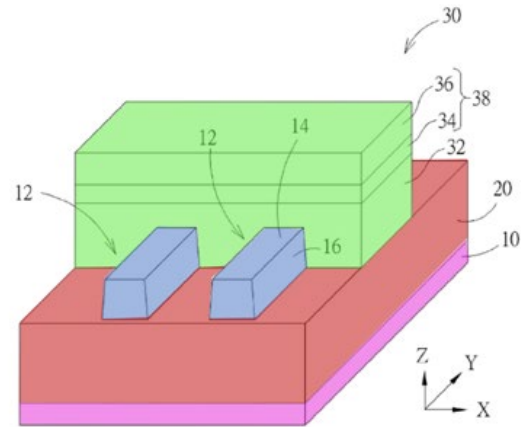


FIG. 2

'193 Patent, Figures 1² (left), 2 (right)

After formation of gate structure 30 (green) and spacer 40, fin-shaped structures 12 are etched to form recesses 60 (purple) located at least at one side of gate structure 30. (TSMC-1001, 4:53-55, 5:4-10, Figure 4 (below-left).) Epitaxial structures 66 (yellow) are then “formed in the corresponding recesses 60.” (TSMC-1001, 5:23-27, Figure 6 (below-right).)

² All shading and annotations in figures added, unless otherwise noted.

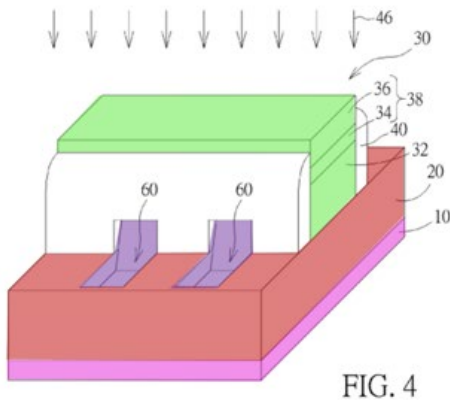


FIG. 4

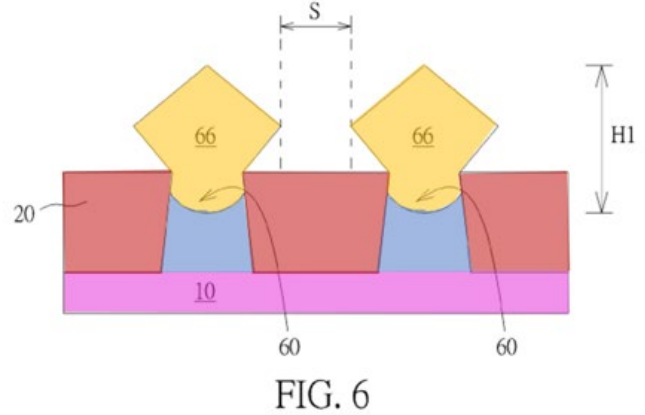


FIG. 6

'193 Patent, Figures 4 (left), 6 (right)

Silicon cap 68 (gray) is then “formed on the surface of each of the epitaxial structures 66.” (TSMC-1001, 5:64-6:1.) As shown in Figure 7 (below), two adjacent silicon caps 68 “merge together.” (TSMC-1001, 6:1-6.)

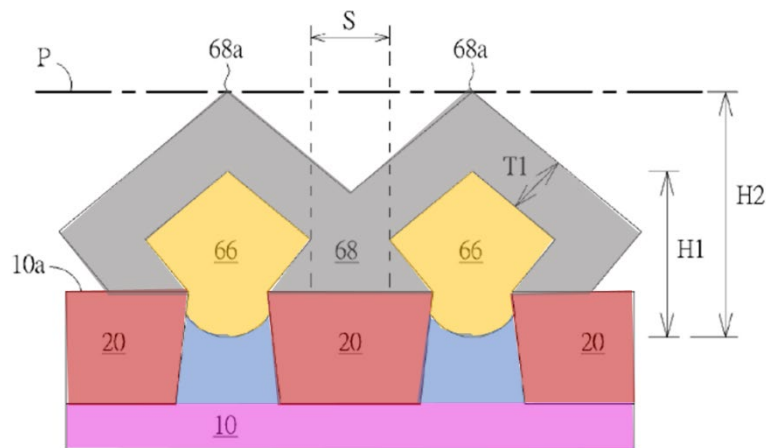


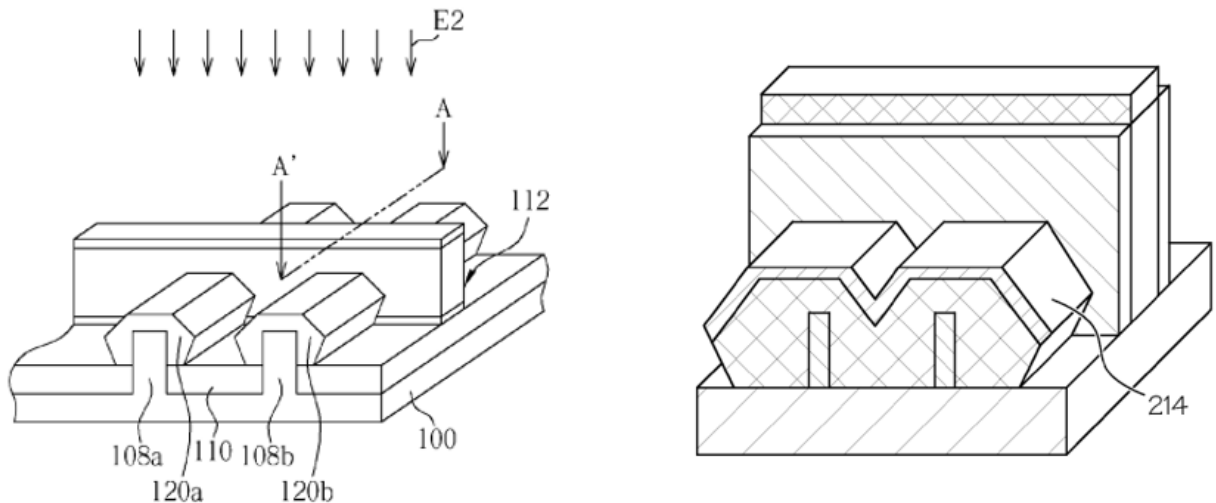
FIG. 7

'193 Patent, Figure 7

C. Prosecution History

Independent claim 1 shares a common preamble and limitations [1A]-[1C] with claim 1 of the parent '805 patent. The sole distinction between the claims is that the '193 patent claims “at least two adjacent caps are merged together” [1D], whereas the '805 patent claims a single cap layer “simultaneously surrounding the epitaxial structures.”

The Examiner, during the '805 patent's prosecution, rejected the claims as obvious over U.S. Publication 2013/0200470 to Liu et al. (“Liu”) combined with U.S. Patent 8,455,313 to Basker et al. (“Basker”), relying on Basker (below-right) as “disclos[ing] a silicon cap simultaneously surrounding the epitaxial structures.” (TSMC-1019, 59; TSMC-1021, Figure 7.)



Liu, Figure 7 (left); Basker, Figure 7 (right)

In response, Applicant acknowledged both references taught “at least two fin-shaped structures”, “gate structure”, and “at least two epitaxial structures” limitations. (TSMC-1019, 91-93.) Applicant, however, argued Basker failed to disclose a “silicon cap layer” because Basker’s “epitaxial silicon layer (214) is directly formed over the fin structures (208)” and “is used to merge the individual fin structures (208) together.” (TSMC-1019, 92.) Applicant further argued a POSITA “would not try to form or deposit another cap layer on the above-mentioned epitaxial layers [of Liu] because the cited references provide no hints about this.” (TSMC-1019, 93.) The Examiner subsequently allowed the ’805 patent claims. (TSMC-1019, 100-104; *see* TSMC-1003, ¶¶58-61.)

During the ’193 patent’s prosecution, Applicant filed a terminal disclaimer to overcome a double-patenting rejection and the Examiner allowed the claims. (TSMC-1002, 75.)

The purported novelty of the ’193 patent claims is therefore the inclusion of an additional layer (referred to as a “*cap*”) surrounding each source/drain epitaxial structure so caps of adjacent structures merge. (TSMC-1003, ¶¶62-63.) Use of a two-layer source/drain structure (epitaxial structure and an overlying cap) was well-known in the art.

D. Claim Construction

Petitioner does not believe any claims require construction to resolve the patentability disputes in this proceeding. *Vivid Techs., Inc. v. Am. Sci. & Eng’g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999).

E. Level of Ordinary Skill in the Art

A person having ordinary skill in the art (“POSITA”) would have had a master’s degree in electrical engineering, physics, chemistry, materials science, or related fields and three years of work experience in semiconductor manufacturing. (TSMC-1003, ¶39.) Additional relevant education could substitute for a portion of the professional experience, and significant work experience or training could substitute for less formal education. (*Id.*)

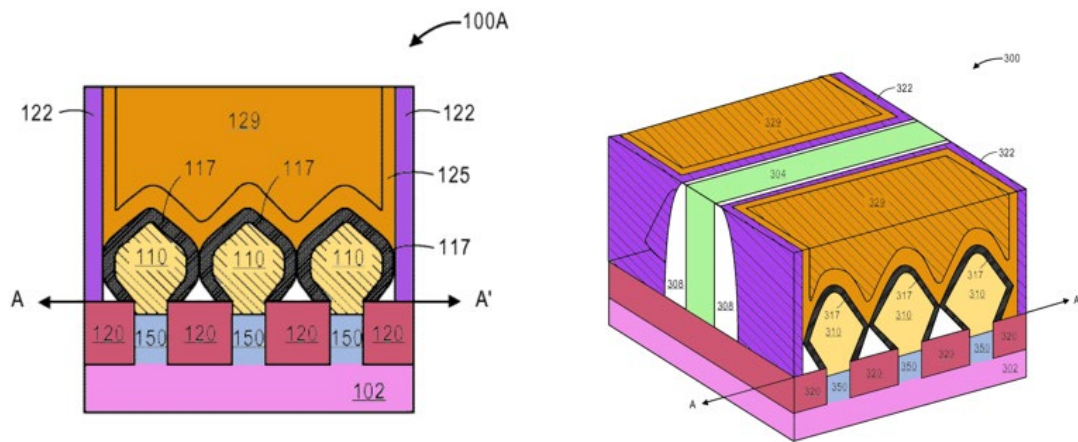
V. GROUND 1: Glass Renders Claims 1-5, 7-9, 11 Obvious.

A. Glass Overview

Glass discloses several embodiments of its technique for “minimiz[ing] the parasitic resistance associated with contacts.” (TSMC-1005, 1:11-17.) This Petition focuses on the embodiment of Glass’s Figures 1A and 3A-I (“Figure 1A/3A-I embodiment”). (TSMC-1005, 3:40-42 and 11:15-17 (relating Figure 1A to Figure 3), 6:61-65 (relating Figure 3A-3I structure to Figure 2 method).) The FinFET formed using Glass’s Figure 1A/3A-I embodiment includes “epitaxially grown source/drain layers 110 [yellow] ... on the top surface of fins 150, which have been

etched below the surface of STI regions 120.” (TSMC-1005, 3:58-61.)

Additionally, “a boron-doped germanium-tin alloy layer 117 [black] is disposed between source/drain layer 110 and a source/drain contact stack.” (TSMC-1005, 3:50-54, 9:8-10.)



Glass, Figures 1A (left), 3I (right)

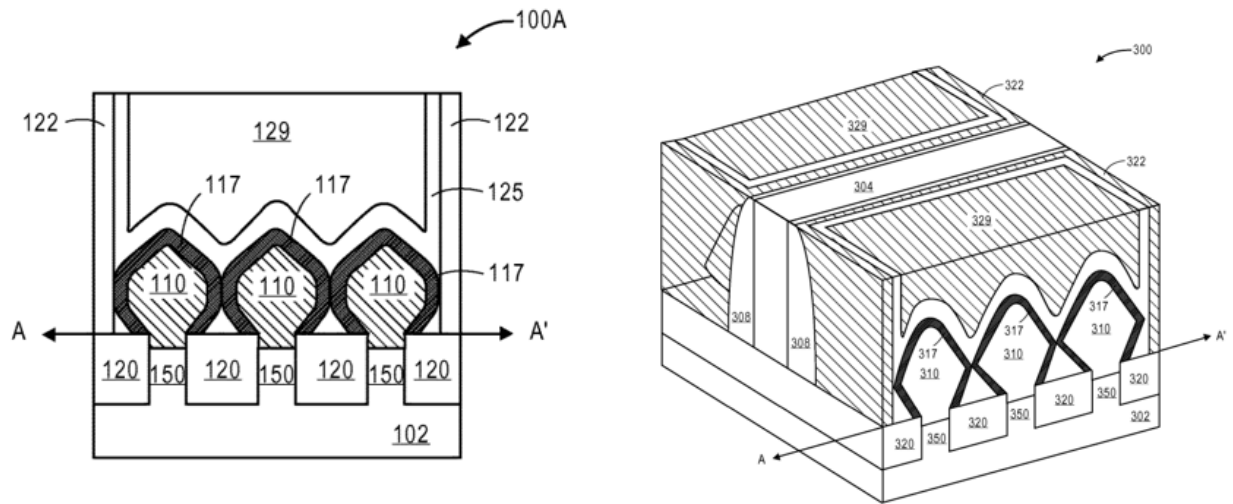
B. Independent Claim 1

1. Preamble [1P]³

Glass’s Figure 1A shows “an example **finFET** architecture.” (TSMC-1005, 3:36-37.) “[A] FinFET is a transistor built around a thin strip of **semiconductor material** generally referred to as the fin.” (TSMC-1005, 3:18-20.) Glass’s FinFET is therefore a “*semiconductor device*” [1P]. (TSMC-1003, ¶66; TSMC-1005, Figures 1A, 3I (below), 7:4-6 (describing channel in semiconductor fin

³ Claim language is indicated by italics throughout.

(surrounded by the gate) and source/drain regions disposed on fin portions on opposite sides of the channel), 7:7-18, 11:15-17 (relating Figure 3I to Figure 1A).)



Glass, Figure 1A (left), Figure 3I (right)

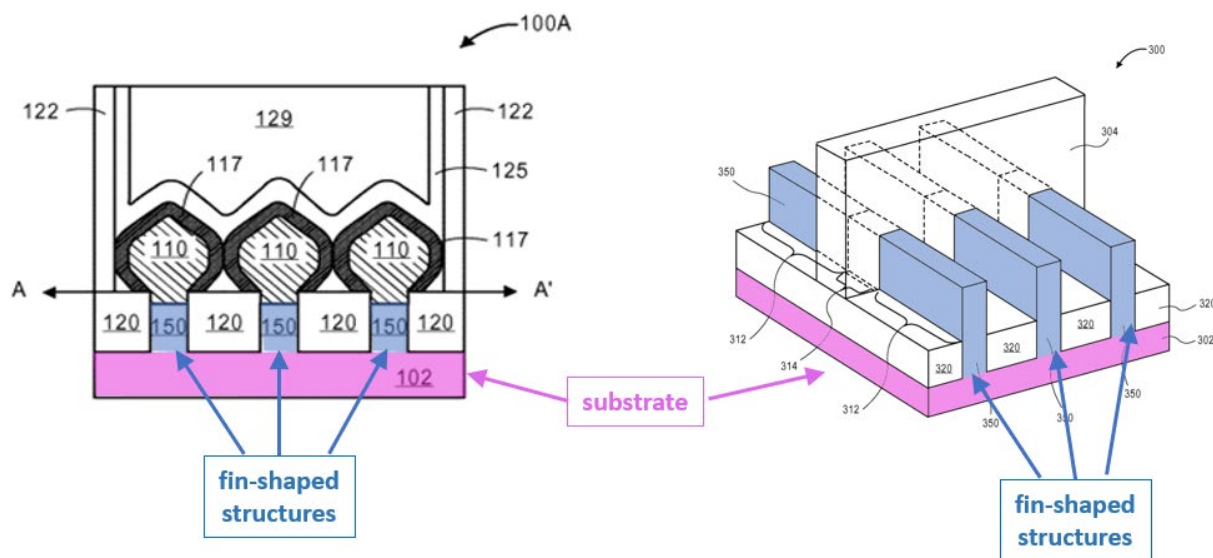
2. Basic FinFET Components [1A]-[1C]

Independent claim 1 recites three basic FinFET components: “*at least two fin-shaped structures*” [1A], “*gate structure*” [1B], and “*at least two epitaxial structures*” [1C]. The original PO acknowledged these components were known during prosecution of the parent ’805 patent. (TSMC-1019, 92; §IV.C.) Glass also discloses these features.

a) Limitation [1A]

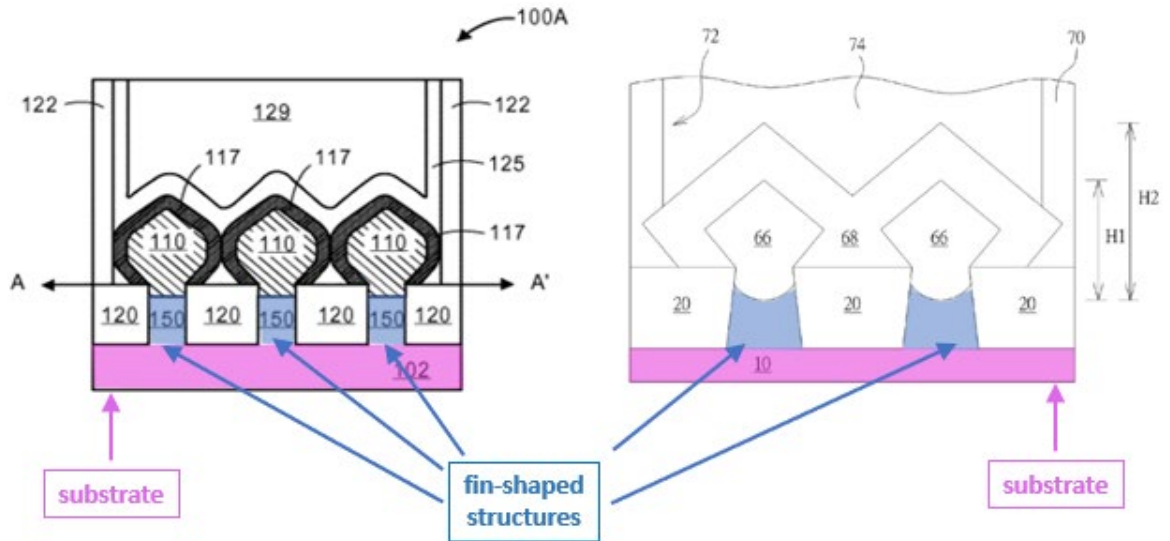
Glass’s fins 350 (blue) are “formed, for example, from a substrate that is bulk silicon or from the top layer of a substrate having a silicon-on-insulator configuration.” (TSMC-1005, 7:7-9, 3:36-42, Figure 3A (below-right), 11:15-17

(associating Figure 1A with structures of Figures 3A-3I), 6:61-65.) The “**source/drain portion of fins 350**” are then “**etched** below the surface of STI [shallow trench isolation] regions 320.” (*Compare* TSMC-1005, 7:49-53 with TSMC-1001, 5:4-8, Figure 4.) Glass’s final FinFET device includes substrate 102 (pink) multiple “fin[s] 150 [blue] extending from the substrate 102.” (TSMC-1005, 3:44-48, Figure 1A (below-left).) Glass discloses “*at least two fin-shaped structures disposed on a substrate*” [1A]. (TSMC-1003, ¶68.)



Glass, Figures 1A (left), 3A (right)

Glass is consistent with the '193 patent’s disclosure, as highlighted in the side-by-side depiction of Glass’s FinFET (Figure 1A, below-left) and the '193 patent’s device (Figure 8, below-right). (TSMC-1001, 2:51-67.)



Glass, Figure 1A (left); '193 Patent, Figure 8 (right)

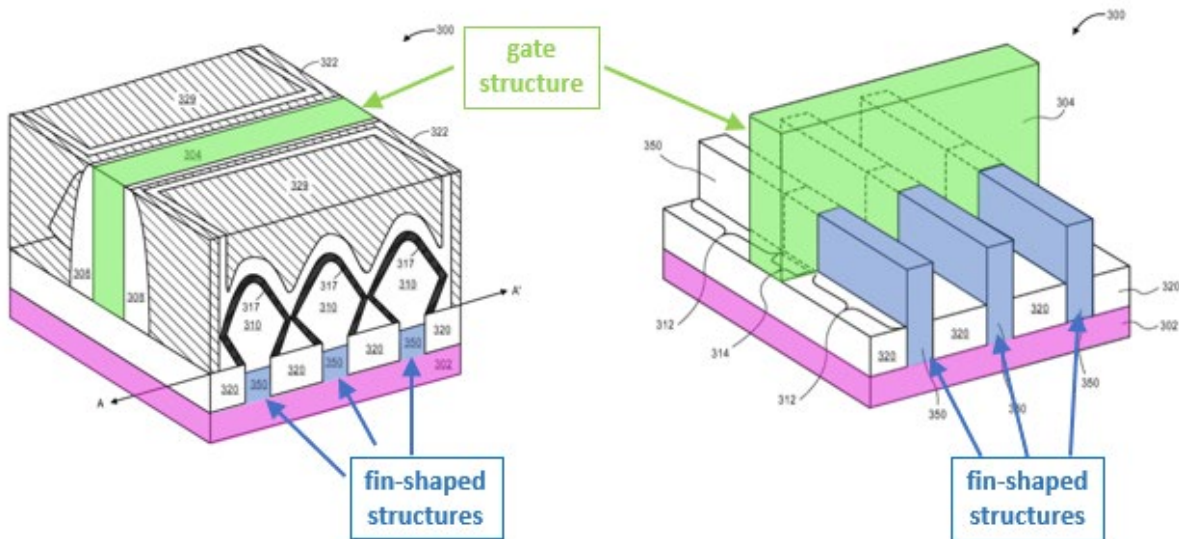
b) Limitation [1B]

Glass's Figure 1A/3A-I embodiment discloses “a gate structure, covering the fin-shaped structures” [1B]. (TSMC-1003, ¶70.)

During formation of Glass's device, gate stack 304 (green) is formed over the plurality of fins 350. (TSMC-1005, 6:66-7:4, Figure 3A (below-right); compare TSMC-1001, 3:59-61 (“[t]he gate structure 30 crosses over at least two fin-shaped structures 12”).) Although obscured by other device features, Glass's final device also includes a gate structure,⁴ labeled 304. (TSMC-1005, Figure 3A, 8:41-67 (describing optional RMG process), 7:4-5 (“[g]ate stack 304 defines a channel

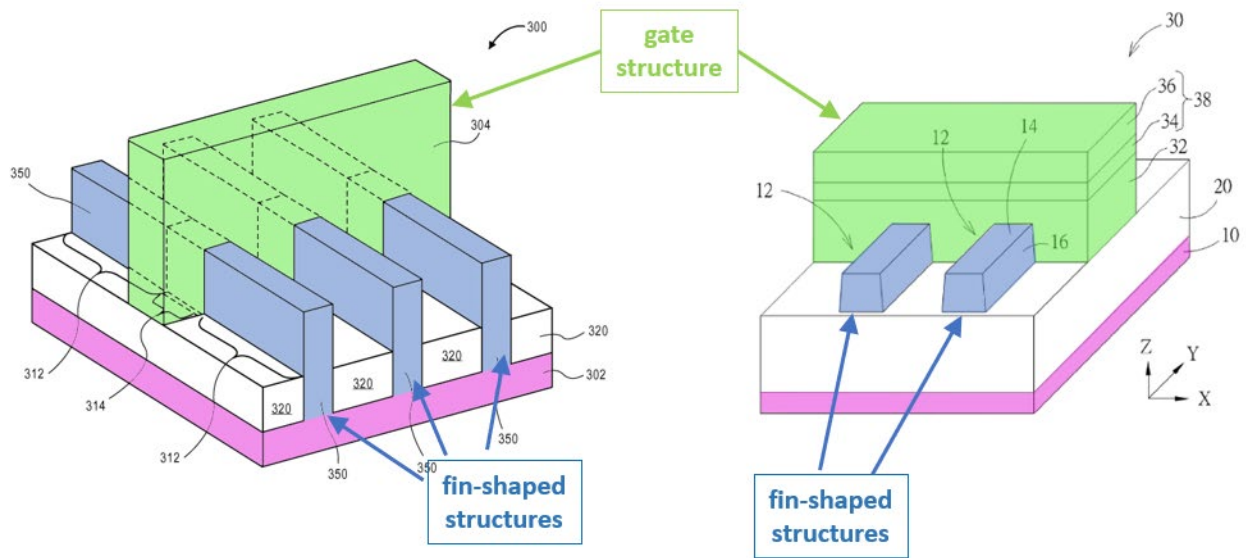
⁴ Glass describes using “a replacement metal gate (RMG) process” performed after “blanket depositing” an interlayer dielectric. (TSMC-1005, 8:19-67.)

region 314 in fins 350”), 7:53-55 (describing “channel portion of fin 350 has not been etched”), 11:15-17.)



Glass, Figures 3I (left), 3A (right)

Glass’s gate structure covering the plurality of fin-shaped structures (Figure 3A, below-left) is consistent with the gate structure of the ’193 patent (Figure 2, below-right). (TSMC-1001, 4:16-52, 6:20-38 (describing optional RMG process).)

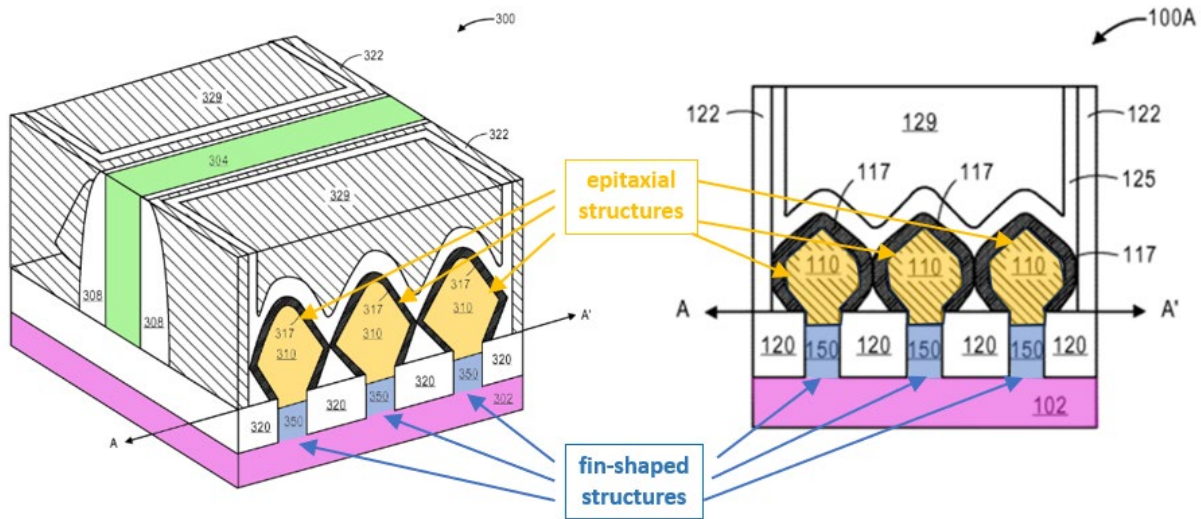


Glass, Figure 3A (left); '193 Patent, Figure 2 (right)

c) Limitation [1C]

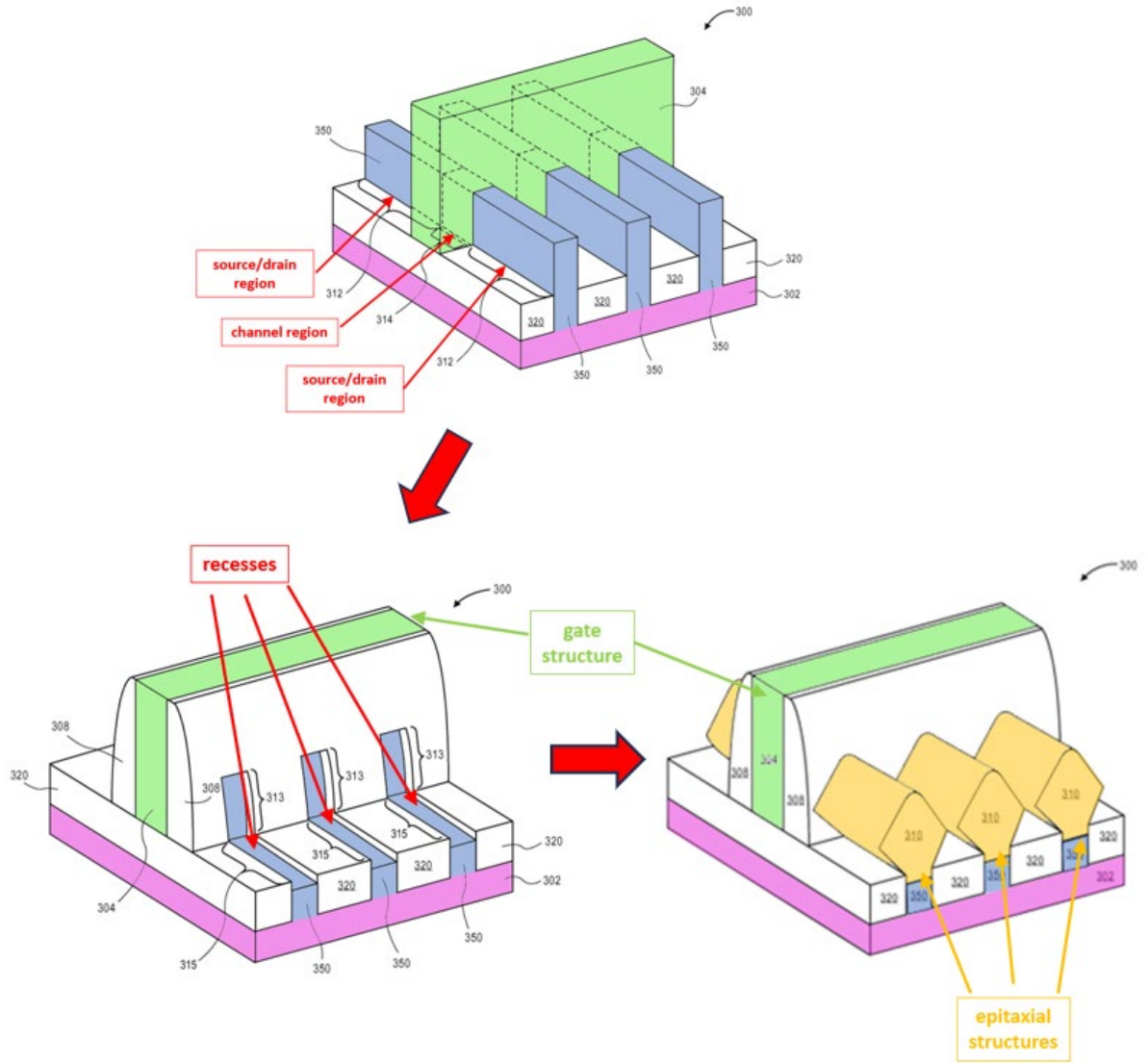
Glass's Figure 1A/3A-I embodiment discloses “*at least two epitaxial structures, disposed at one side of the gate structure and respectively directly contacting each fin-shaped structure, wherein the epitaxial structures are spaced apart from each other*” [1C]. (TSMC-1003, ¶¶72-76.)

In Figures 1A (left) and 3I (right), “**epitaxially grown source/drain layers 110** [yellow] are formed on the top surface of fins 150, which have been etched below the surface of STI regions 120.” (TSMC-1005, 3:58-61.) Epitaxially grown source/drain layers 110 on the multiple fins are “*at least two epitaxial structures.*” (TSMC-1003, ¶72.)



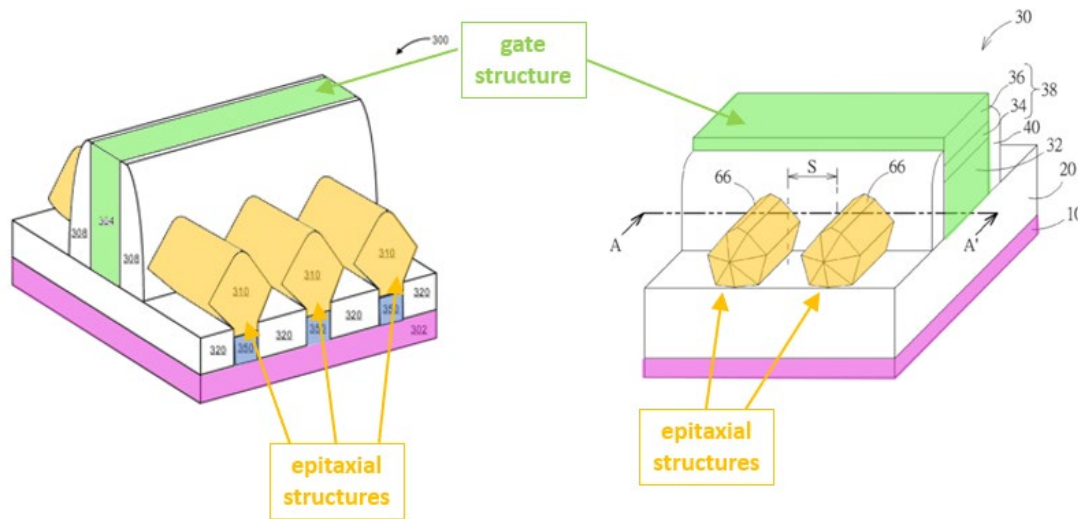
Glass, Figures 3I (left), 1A (right)

Glass’s “**source/drain portion of fins 350**” are “**etched** below the surface of STI [shallow trench isolation] regions 320 to provide cavities 315 as well as respective tip areas 313 which undercut the gate spacers 308 and the gate dielectric portion of gate stack 304.” (*Compare* TSMC-1005, 7:49-53, Figure 3C (below/bottom-left), *with* TSMC-1001, 5:4-8, Figure 4.) Epitaxially grown source/drain layers 110 “are formed **on the top surface of the [etched] fins 150**” and therefore are “*disposed at one side of the gate structure*” and “*directly contact[] each fin-shaped structure.*” (TSMC-1005, 3:59-61 (source/drain regions 312 are “disposed on opposite sides of the channel region 314”), 7:56-58, 11:15-17, Figure 3D (below/bottom-right), Figures 3I, 1A (above); TSMC-1003, ¶¶73-74.)



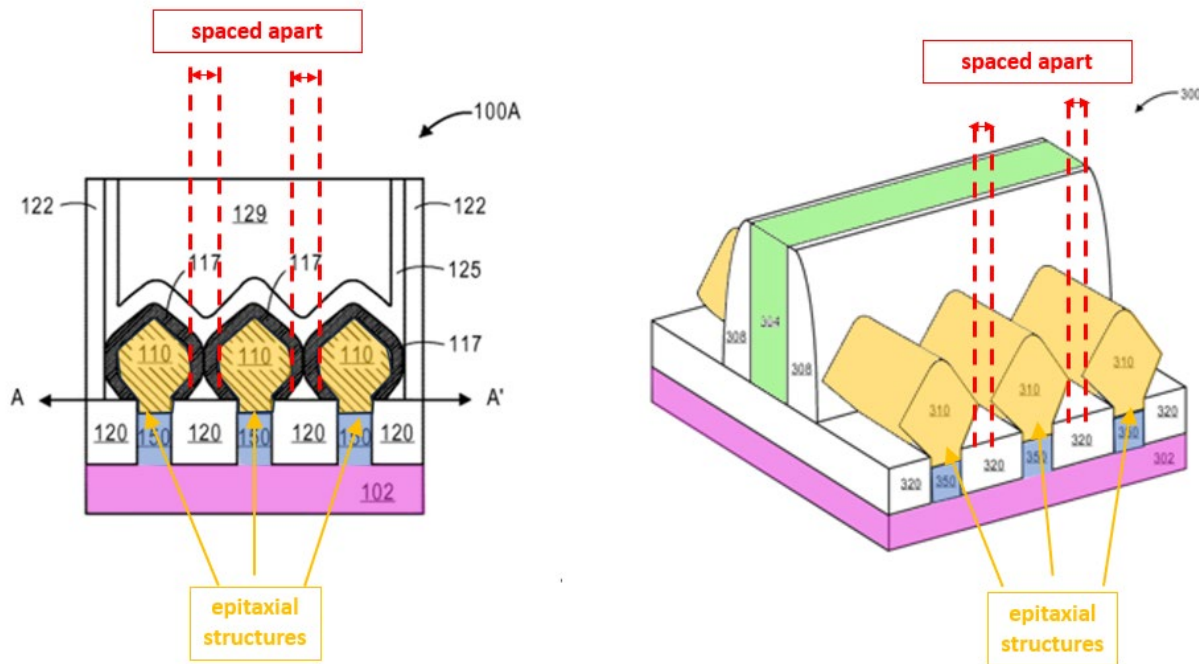
Glass, Figures 3A (top), 3C (bottom-left), 3D (bottom-right)

Glass's disclosure is consistent with the '193 patent's disclosure regarding formation of the epitaxial structures, as illustrated by the side-by-side figures below. (TSMC-1003, ¶75.)



Glass, Figure 3D (left); '193 Patent, Figure 5 (right)

As shown in Glass's Figure 1A and Figure 3D below, "*the epitaxial structures*" do not touch. (TSMC-1003, ¶76; *see also*, §V.B.3); *Unified Pats., LLC v. Oceana Innovations LLC*, No. IPR2020-01463, 2022 WL 500391, *17 (P.T.A.B. Feb. 14, 2022) ("[A] patent drawing may serve as prior art 'without referring to the surrounding description' if 'the prior art features are clearly disclosed by the drawing.'").) Thus, Glass teaches or suggests "*the epitaxial structures are spaced apart from one another.*" (TSMC-1003, ¶76.)

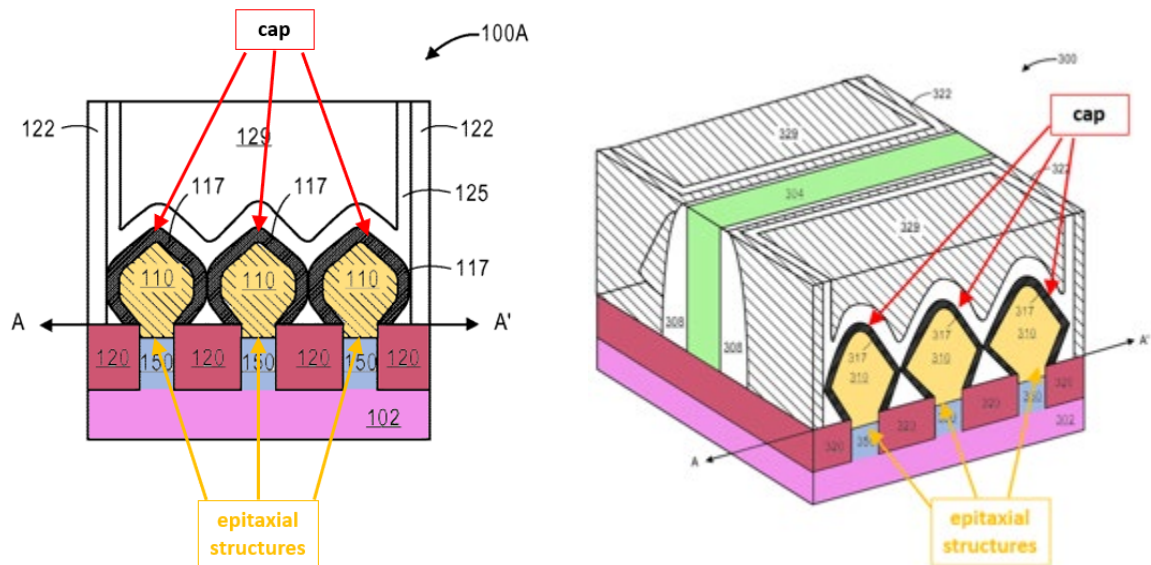


Glass, Figures 1A (left), 3D (right)

3. Limitation [1D]

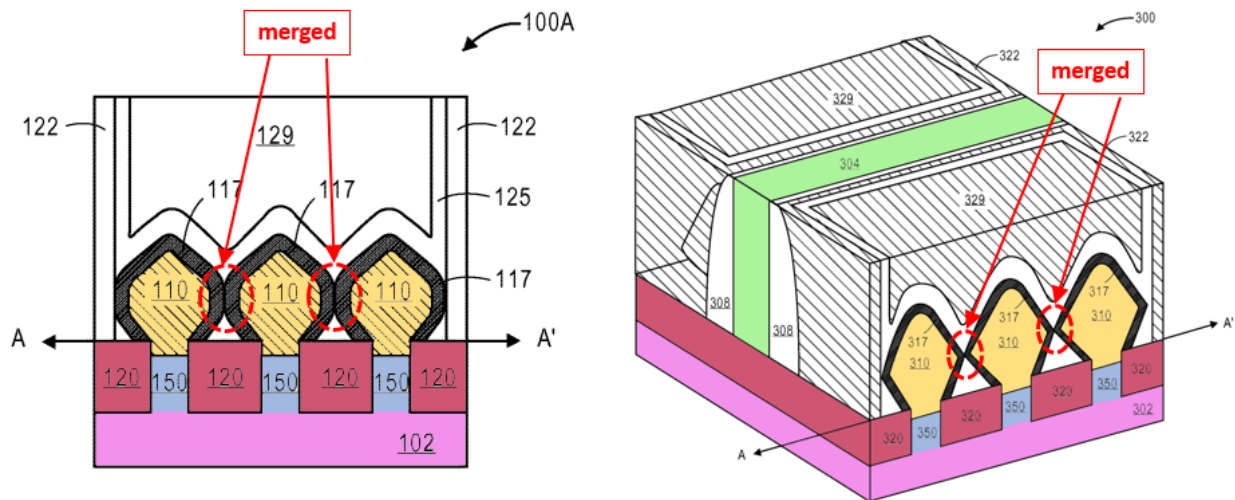
Glass's Figure 1A/3A-I embodiment discloses or renders obvious "*at least two caps, respectively surrounding the epitaxial structures, wherein at least two adjacent caps are merged together*" [1D]. (TSMC-1003, ¶¶77-84.) Glass's device includes boron-doped germanium-tin alloy layer 117 (black) "disposed between the source/drain layer ["*epitaxial structures*"] and a source/drain contact stack" (contact metal 125 and metal plug 129). (TSMC-1005, 3:50-54, 9:8-10, 44-54 (describing contact fabrication process).) Boron-doped germanium-tin alloy layer 117 surrounding each source/drain layer 110 ("*epitaxial structure*") is a "*cap*" and

therefore Glass discloses “*at least two caps, respectively surrounding the epitaxial structures.*” (TSMC-1003, ¶¶77-78.)



Glass, Figures 1A (left), 3I (right)

In Glass’s device (shown above), individual “*caps ... surrounding the epitaxial structures*” merge with adjacent caps because the caps are deposited concurrently and made from the same material. (TSMC-1003, ¶79; TSMC-1025 (merge means “to cause to combine, unite, or coalesce”); *Unified*, 2022 WL 500391, *17.)

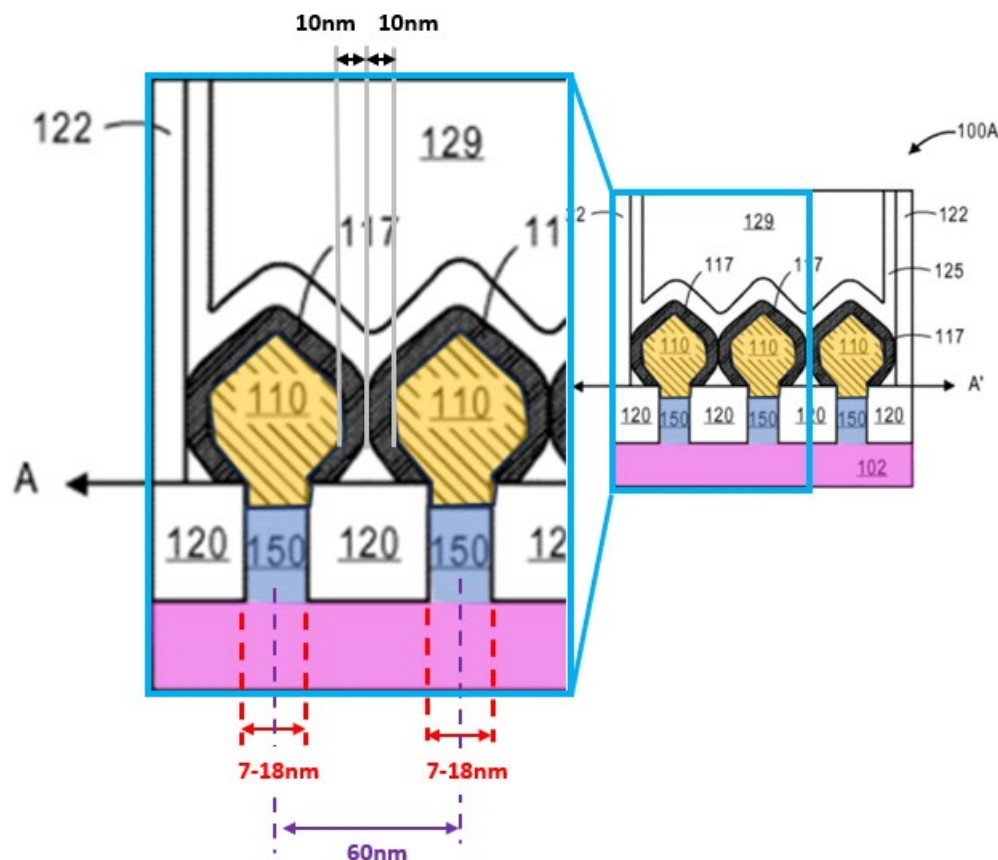


Glass, Figures 1A (left), 3I (right)

Glass explicitly discloses “*at least two adjacent caps are merged together*” [1D] as shown in Figures 1A and 3I above. Should PO contend Glass does not expressly disclose “*at least two adjacent caps are merged together,*” this feature would have been obvious based on the teachings of Glass and a POSITA’s semiconductor knowledge. (TSMC-1003, ¶¶80-84.)

The thickness of Glass’s “boron-doped germanium-tin alloy layer 317 may have a thickness in the range, for example of 10 to 500 Å” (between 1 nm and 50 nm). (TSMC-1005, 9:38-41.) Details regarding fin width or fin pitch were well-known prior to the ’193 patent. For example, a POSITA would have known exemplary values based on products and documents available prior to the ’193 patent. For example, the Intel 22nm Ivy Bridge processor included a FinFET with a fin pitch of 60 nm and a fin width of 7 nm-18 nm). Applying these exemplary

values to Glass's device, a POSITA would have understood that Glass's adjacent "*epitaxial structure[s]*" merge in the same manner disclosed in the '193 patent. (TSMC-1001, 6:8-11 ("For example, when the distance S ranges from 10 nm to 20 nm, the thickness T1 of the silicon cap 68 may range from 6 nm to 11 nm or may be greater than 11 nm"); TSMC-1003, ¶82.)



Glass, Figure 1A with Enlargement

Moreover, a POSITA would have known before the '193 patent merging adjacent source/drain structures increases the contact area between the source/drain regions and the source/drain contact, which reduces the source/drain contact

resistance. (TSMC-1012, 100; TSMC-1003, ¶83.) Importantly, a POSITA would have been motivated to use a thickness for the less resistive boron-doped germanium-tin layer 317 that allows cap layers from adjacent epitaxially grown source/drain regions to merge for an additional reason—a larger total area translates to a larger landing area for the source/drain contact, which relaxes the photolithography requirements when patterning source/drain contacts. (TSMC-1012, 100; TSMC-1018, 2; TSMC-1003, ¶83.)

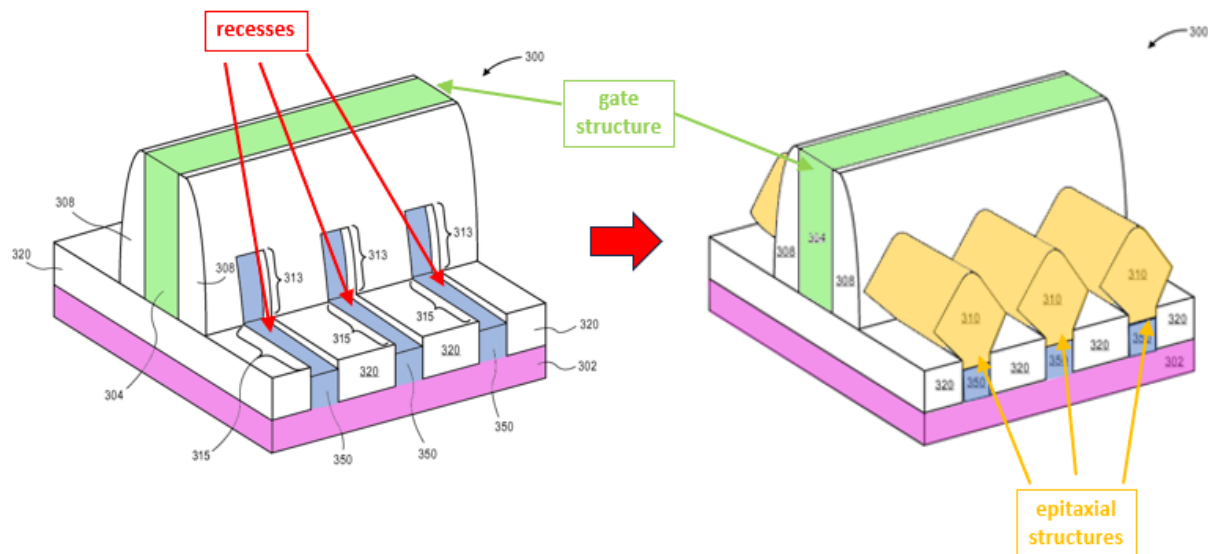
Therefore, a POSITA would have known that implementing a less resistive germanium-tin layer that causes merging between adjacent S/D epitaxial structures is a desirable feature that would reduce the source/drain contact resistance and promote gate pitch scaling. (TSMC-1003, ¶84.) Accordingly, based on Glass and his/her own knowledge, a POSITA would have understood boron-doped germanium-tin layers 317 (“*cap*”) deposited on adjacent “*epitaxial structure[s]*” would also merge to further source/drain contact resistance reduction. (*Id.*)

C. Dependent Claims

1. Claims 2-3

Glass’s Figure 1A/3A-3I embodiment discloses “*at least two recesses, respectively disposed at an end of each of the fin-shaped structures, wherein each of the epitaxial structures respectively fills up each of the recesses*” [2]. (TSMC-1003, ¶¶86-87.)

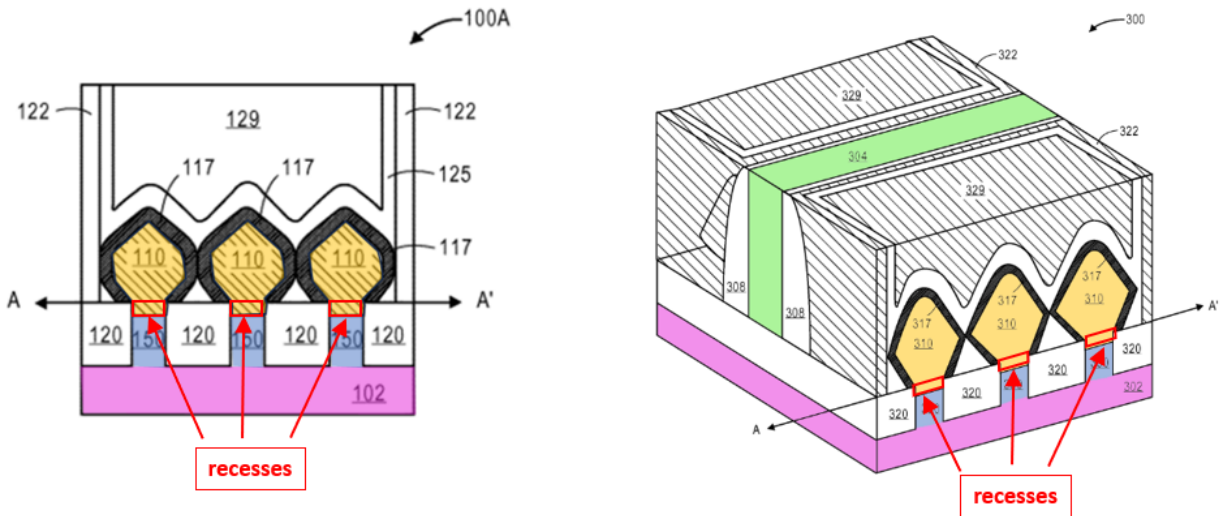
During formation of Glass's source/drain layers 310 (*"epitaxial structures"*), source/drain portions of fins 350 are "etched below the surface of STI regions 320 to provide cavities 315." (TSMC-1005, 7:49-53, Figure 3(C) (below-left); *compare* TSMC-1001, 5:4-8.) The cavities resulting from etching are "*at least two recesses.*" Because the recesses are formed by etching the fin-shaped structures in the source/drain regions, which are "disposed on opposite sides of the channel region", the recesses are "*disposed at an end of each of the fin-shaped structures.*" (TSMC-1005, 7:4-6; *compare* TSMC-1005, Figure 3C, with TSMC-1001, Figure 4; TSMC-1003, ¶86.)



Glass, Figures 3C (fleft), 3D (right)

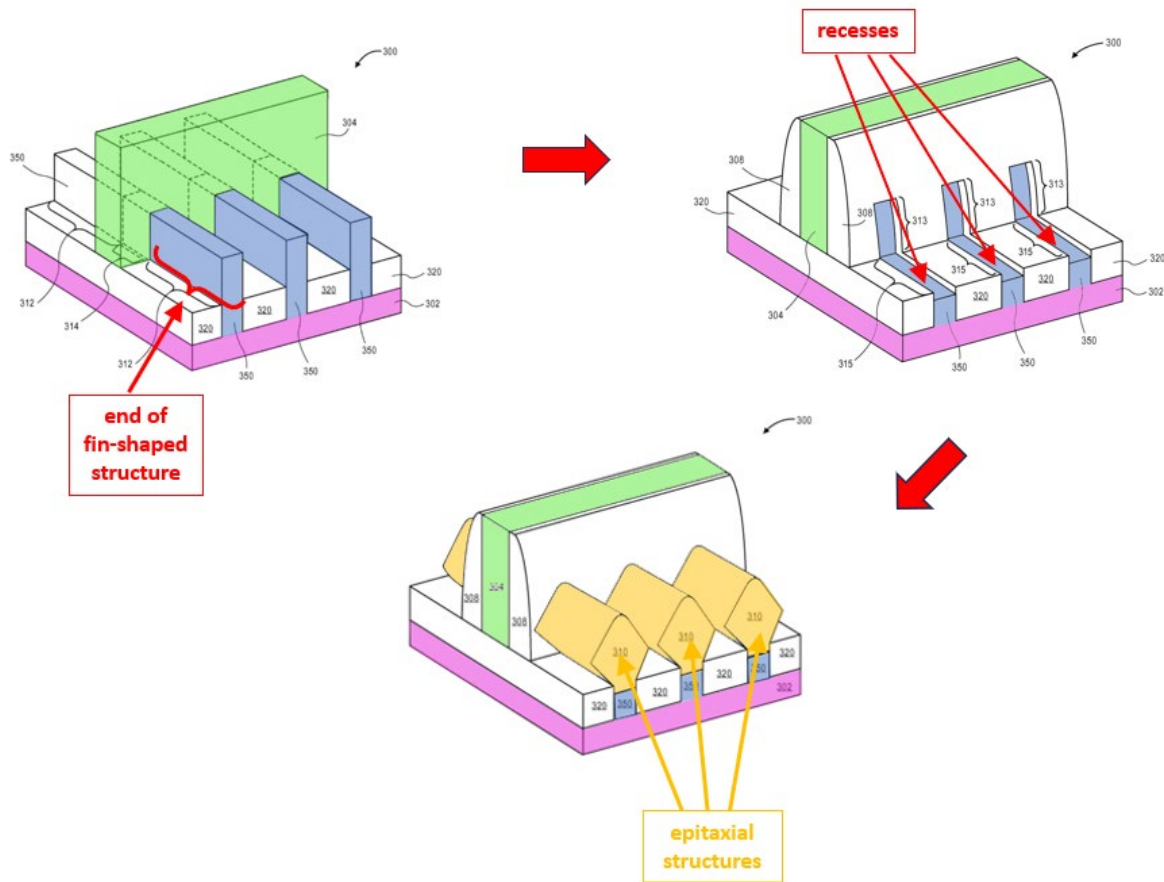
Epitaxial material is grown "**from the top of the source/drain portion of each fin 350** to provide source/drain layers 310" (yellow). (TSMC-1005, 7:56-59,

Figure 3D (top-right); *compare* TSMC-1001, 5:20-22, Figure 5.) Because the source/drain portions of the fins are etched below the STI and then source/drain layers are epitaxially grown from these etched portions, the “*epitaxial structures*” (yellow) fill the recesses, as shown in Figures 1A/3I below. (TSMC-1003, ¶87.)



Glass, Figures 1A (left), 3I (right)

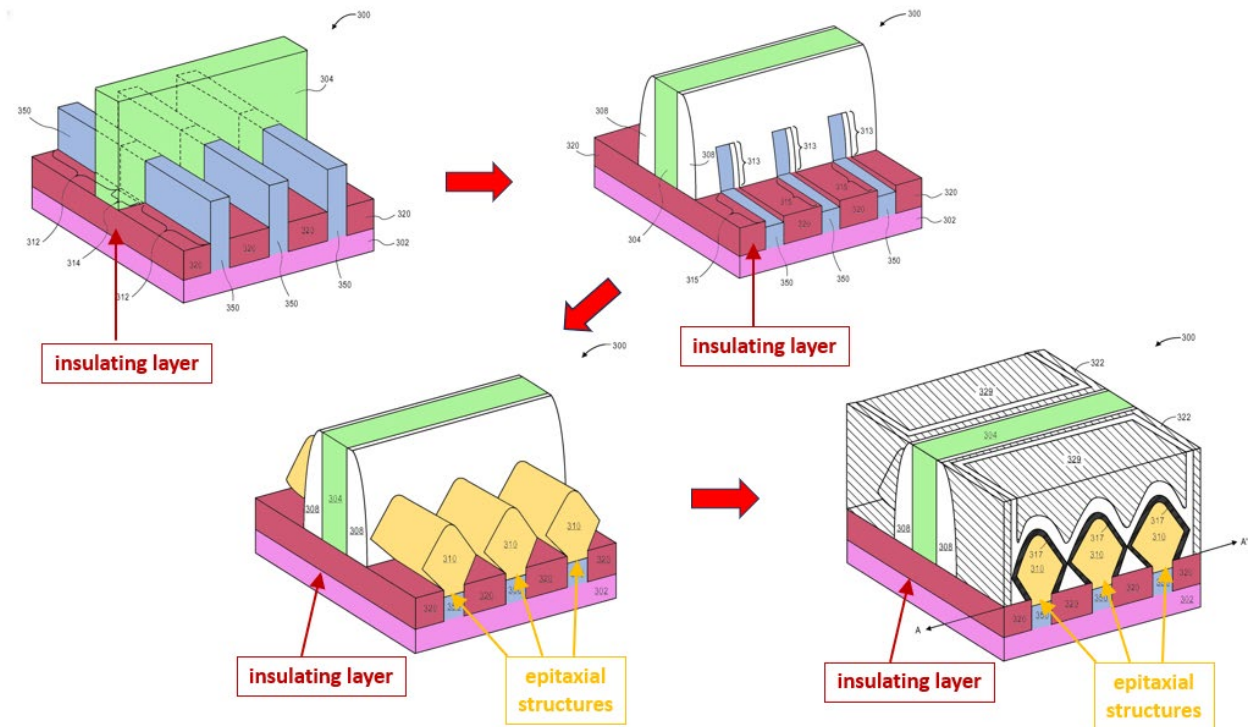
Because source/drain layers “**are formed on the top surface of fins 150**,” which have been etched below the surface of STI regions 120 at “*an end of each of the fin-shaped structures*” [2],” “*the epitaxial structures respectively cover an end of each of the fin-shaped structures*” [3]. (TSMC-1005, 3:58-61, Figure 3D (below-bottom), TSMC-1003, ¶88.)



Glass, Figures 3A (top-left), 3C (top-right), 3D (bottom)

2. Claim 4

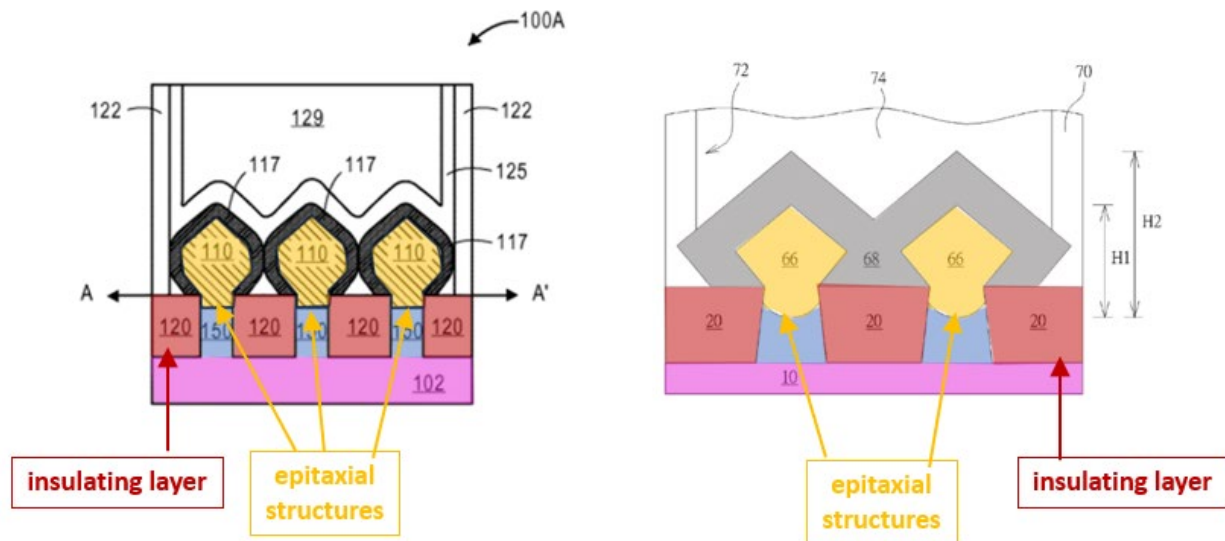
In Glass's device, "fins 350 extend through STI regions 320 [red]", as shown in Figure 3A (below/top-left). (TSMC-1005, 7:19-20, 3:46-48.) STI regions 320 are "made from any suitable **insulating material**, such as SiO₂." (TSMC-1005, 7:23-24.) STI regions are therefore "*an insulating layer.*"



**Glass, Figures 3A (top-left), 3C (top-right),
3D (bottom-left), 3I (bottom-right)**

Epitaxially grown source/drain layers 110 (“*epitaxial structures*”; yellow)
“are formed **on the top surface of fins 150, which have been etched below the surface of STI regions 120.**” (TSMC-1005, 3:58-61.) Thus, a portion of each
“*epitaxial structure*” fills the cavity (recess) between the STI regions (“*insulating layer*”). (See §V.C.1.) As a result, Glass’s device, shown in Figures 3D
(above/bottom-left) and 3I (above/bottom-right), includes “*at least an insulating layer, disposed between the epitaxial structures*” [4]. (TSMC-1003, ¶¶89-91.)

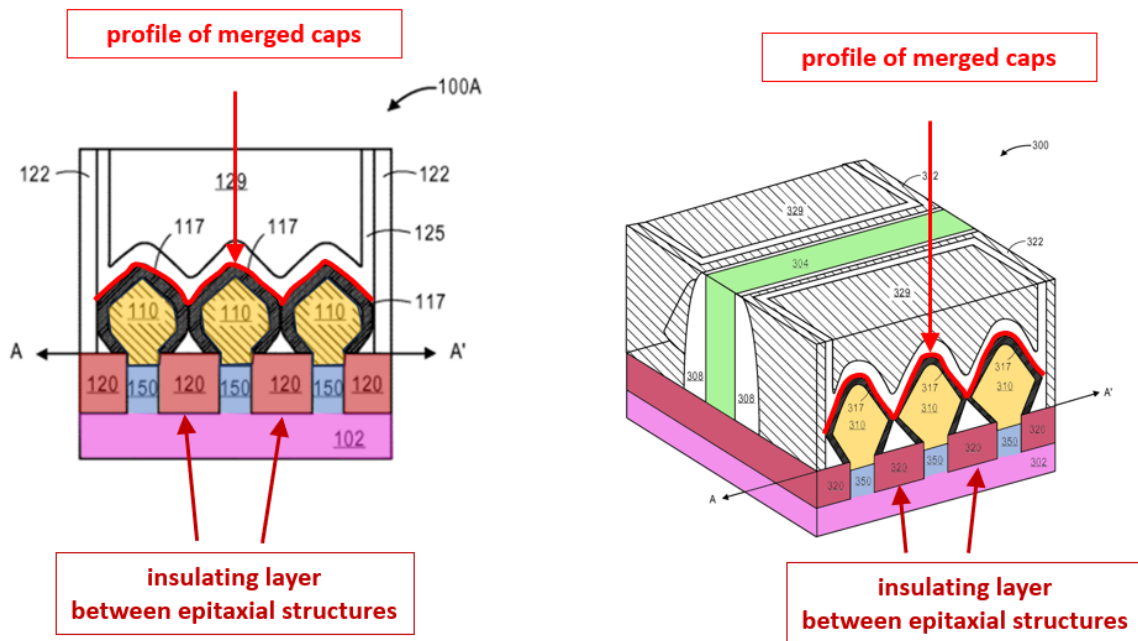
Glass's disclosure is consistent with the '193 patent's disclosure, as highlighted by the depiction of Glass's final device and the final structure of the '193 patent. (TSMC-1001, 3:39-46.)



Glass, Figure 1A (left); '193 Patent, Figure 8 (right)

3. Claim 5

As discussed in §V.B.3, boron-doped germanium-tin alloy layers 117/317 (“caps”) surrounding each source/drain layer 110/310 (“*epitaxial structures*”) “*are merged together.*” As a result, the merged “[adjacent] caps directly cover the insulating layer between the epitaxial structure.” (TSMC-1003, ¶92; TSMC-1027 (defining cover as “something that protects, shelters, or guards; something that is placed over or about another thing; something that conceals or obscures”).) As shown in Figures 1A/3I below, since “adjacent caps” merge, the resulting surface of the merged caps directly covers the underlying STI regions. (TSMC-1003, ¶92.)



Glass, Figures 1A (left), 3I (right)

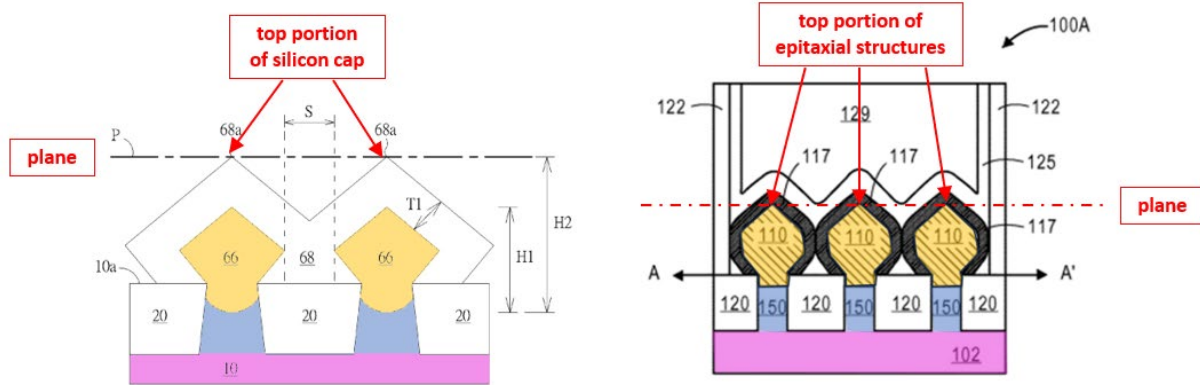
Should PO contend “*directly cover*” requires direct contact between the “*cap*” and “*insulating layer*”, neither the claim nor the specification supports such a narrowing. Applicant used the term “*directly contacting*”/ “*direct contact*” in limitations [1C] and [11B], respectively, to indicate when two components “touch” one another. Here, Applicant intentionally used a different term—“*directly cover*.” Accordingly, the terms should not have identical meanings. (See TSMC-1003, ¶93.) Regardless, as shown in the figures above, Glass’s boron-doped germanium-tin alloy layers 117/317 (“*caps*”, black) are in direct contact with the underlying insulating layers 120. (*Id.*)

4. Claim 7

Glass's source/drain layers 110 ("*epitaxial structures*") "may be silicon, germanium, or **silicon germanium**." (TSMC-1005, 3:61-64, 7:59-61 ("SiGe" may be used for source/drain layers.) Thus, Glass discloses the "*composition of each of the epitaxial structures comprises silicon germanium, silicon phosphide or silicon carbide*" [7]. (TSMC-1003, ¶93.)

5. Claim 8

Glass's Figure 1A/3A-3I embodiment discloses or renders obvious "*each of the epitaxial structures comprises a top portion and the top portions are substantially in the same plane*" [8]. (TSMC-1003, ¶¶95-96.) The '193 patent lacks disclosure related to epitaxial structures each having a top portion in the same plane. The '193 patent merely mentions "**merged silicon cap 68** may have top portions 68a having the same height H2 or being in the same plane P." (TSMC-1001, 6:15-17, Figure 7 (below-left).) Consistent with this disclosure, the "*top portion*" of the "*epitaxial structures*" encompasses the upper most portion of the structure located at the height of the structures (e.g., H1 in '193 patent, Figure 7).



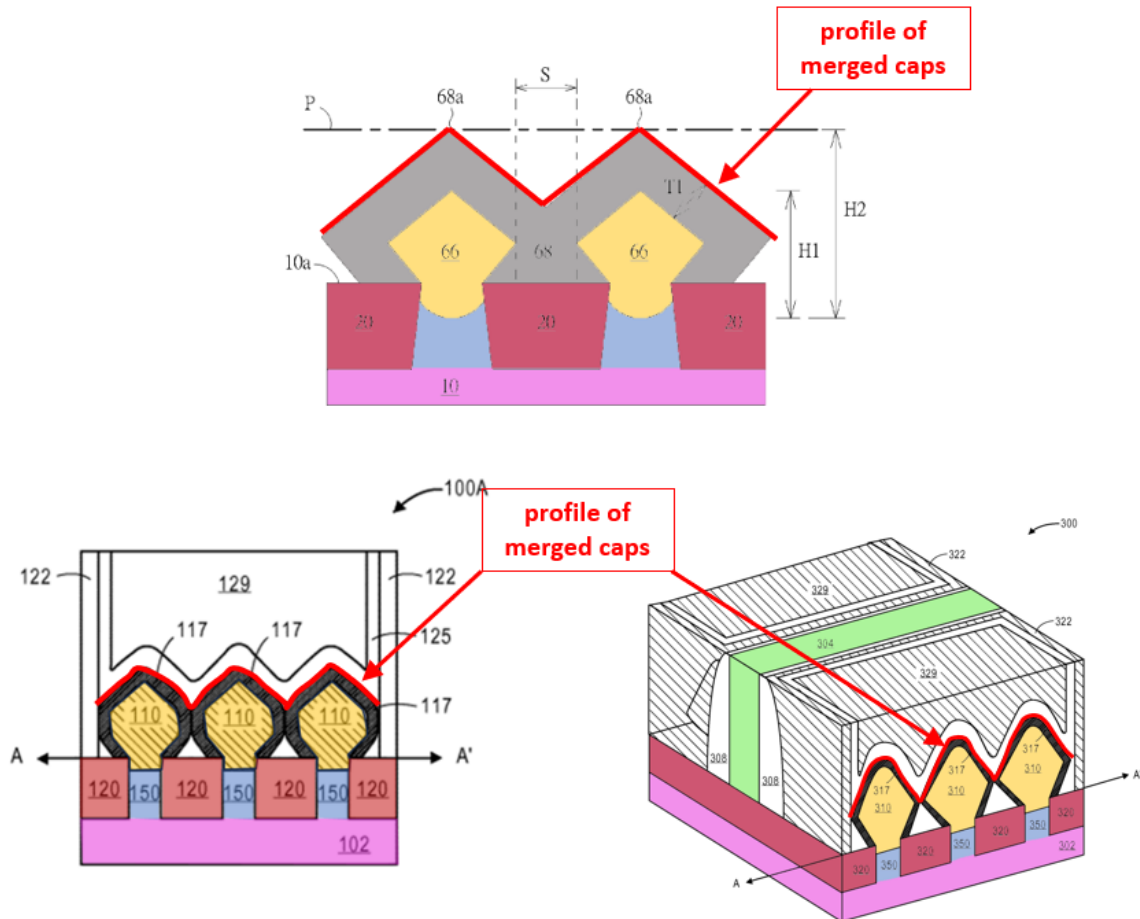
'193 Patent, Figure 7 (left); Glass, Figure 1A (right)

As shown in Figure 1A (above-right), Glass's source/drain layers 110 (“*epitaxial structures*”) each has a “*top portion*” having the same height. (TSMC-1003, ¶96; §V.B.3; *Unified*, 2022 WL 500391, *17.) Thus, Glass teaches or renders obvious claim 8.

6. Claim 9

Glass discloses “*the caps have a concavo-convex profile*” [9], consistent with the '193 patent's disclosure. (TSMC-1003, ¶97.) Referring to Figure 7 (below/top), the '193 patent states “merged silicon cap 68 may cover the entire surface of the epitaxial structures 66 and has an **approximately periodic concavo-convex profile.**” (TSMC-1001, 6:13-15.) The '193 patent thus associates a concavo-convex profile to a repeating pattern alternating between concave and convex shapes. (TSMC-1003, ¶97.) Glass's merged boron-doped germanium-tin

alloy layers 117 (“caps”) surrounding source/drain layers 110 also have an approximately periodic concavo-convex profile. (*Id.*)

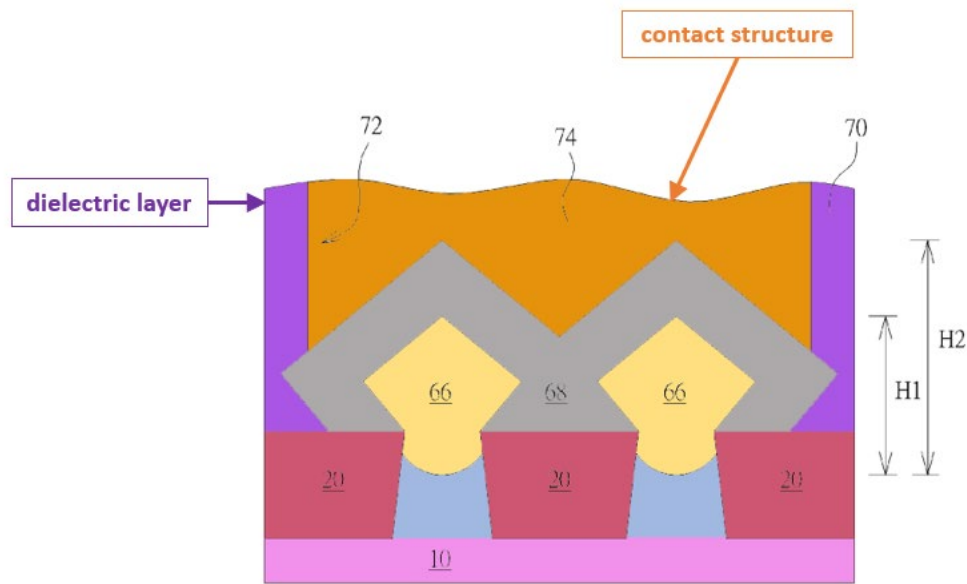


**'193 Patent, Figure 7 (top);
Glass, Figures 1A (bottom-left), 3I (bottom-right)**

7. Claim 11

Glass's Figure 1A/3A-3I embodiment discloses “a dielectric layer, covering the gate structure and the cap” [11A] and “at least a contact structure, disposed in the dielectric layer and in direct contact with the caps” [11B], to the extent disclosed in the '193 patent. (TSMC-1003, ¶¶98-102.)

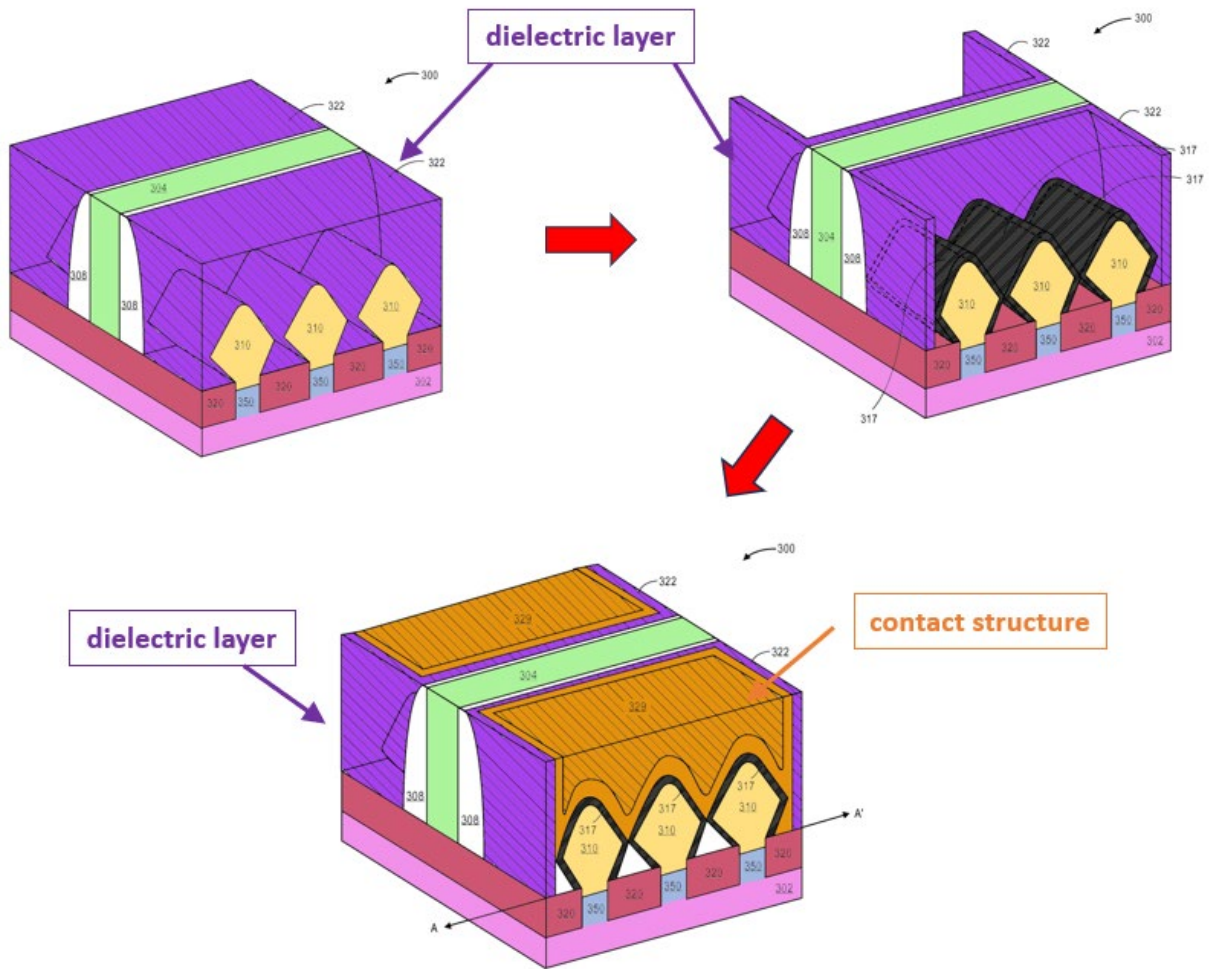
To form “contact structures” to “electrically connect the epitaxial structures 66 to the subsequently formed external circuit,” the ’193 patent teaches that a contact hole is formed “in the interlayer dielectric 70 so as to expose the corresponding silicon cap 68.” (TSMC-1001, 6:39-48.) A conductive layer is then deposited, resulting in “contact plug 74 [orange] filling up the contact hole 72.” (TSMC-1001, 6:48-53, Figure 8 (below).)



’193 Patent, Figure 8

Glass’s fabrication process includes similar steps. (TSMC-1003, ¶100.) During Glass’s process, “interlayer dielectric 322 [purple] is **blanket** deposited over the gate structure 304 and the source/drain regions of the finFET device.” (TSMC-1005, 8:23-26; Figure 3E (below/top-left). Source/drain contact trenches are then formed. (TSMC-1005, 8:1-4; Figure 3G (below/top-right).) Thus,

consistent with the '193 patent's disclosures, Glass discloses “a dielectric layer, covering the gate structure and the cap” [11A]. (TSMC-1003, ¶100.)



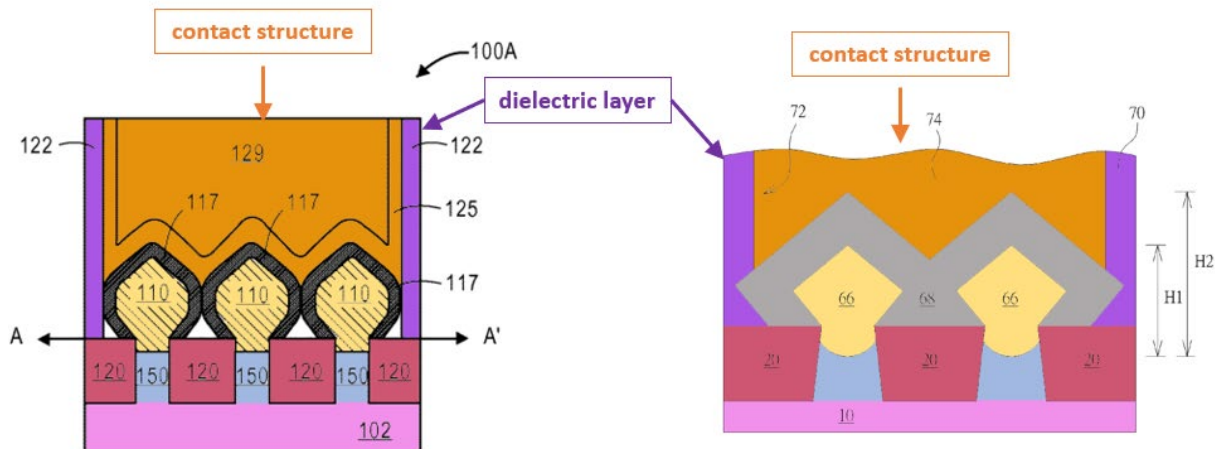
Glass, Figures 3E (top-left), 3G (top-right), 3I (bottom)

A contact metal (orange) is then deposited and source/drain contact plugs 329 (orange) are deposited over the contact metal. (TSMC-1005, 10:51-11:17; Figure 3I (above/bottom).) Contact metal 325 and contact plug 329 (“source/drain contact stack”) are collectively a “*contact structure*.” (TSMC-1005, 4:36-39.)

Contact metal 125 lines the trench in the interlayer dielectric and is “**in contact with alloy layer 117** [“*cap*”] on source/drain layers 110.” (TSMC-1005, 4:39-41.)

Thus, Glass discloses “*at least a contact structure, disposed in the dielectric layer and in direct contact with the caps*” [11B]. (TSMC-1003, ¶101.)

As highlighted by the side-by-side depiction of Glass's Figure 1A and Figure 8 of the '193 patent, Glass's dielectric layer and contact structure are consistent with the dielectric layer and contact structure of the '193 patent.



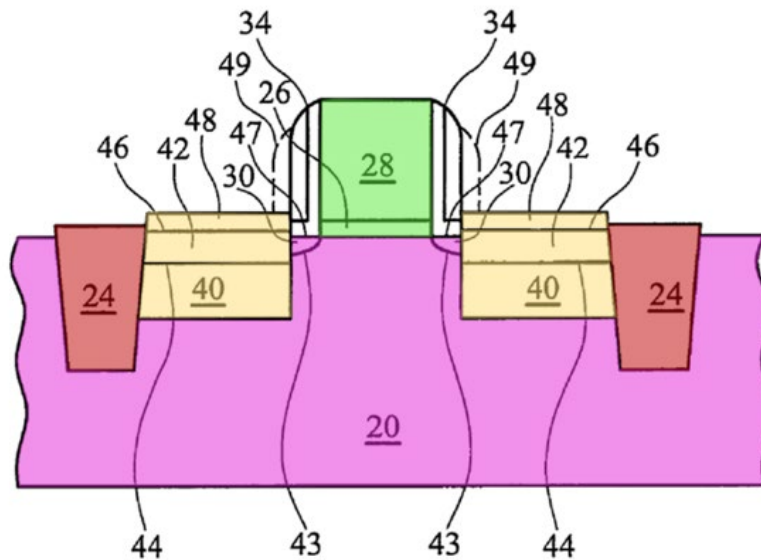
Glass, Figure 1A (left); '193 Patent, Figure 8 (right)

VI. GROUND 2: Glass-Tsai Combination Renders Claim 6 Obvious.

Glass does not expressly disclose “*each of the epitaxial structures comprises a low doped epitaxial layer, a high doped epitaxial layer and a liner*” [6]. Tsai discloses this feature.

A. Overview of Tsai

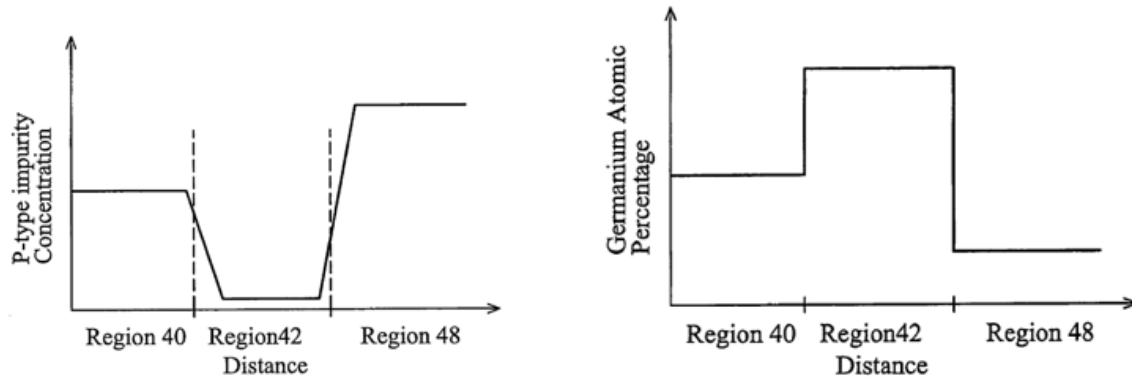
Tsai's device includes substrate 20 (pink), STI regions 24 (red), and gate stack 12 (green). (TSMC-1006, 4:6-17, Figure 6 (below).) The device also includes “epitaxy regions, often referred to as SiGe stressors” having “a sandwich structure with three stacked layers 40, 42, and 48.” (TSMC-1006, 5:5-7.)



Tsai, Figure 6

SiGe regions 40 are “epitaxially grown in recesses 36, preferably by selective epitaxial growth (SEG).” (TSMC-1006, 5:8-9.) The “[p]rocess conditions for the epitaxy process are then changed to form second SiGe regions 42 on SiGe regions 40.” (TSMC-1006, 5:28-29.) SiGe regions 48 “are then formed on second SiGe regions 42.” (TSMC-1006, 6:18-19.) The three SiGe regions have different concentrations of a p-type impurity, as shown for one embodiment in Figure 7C

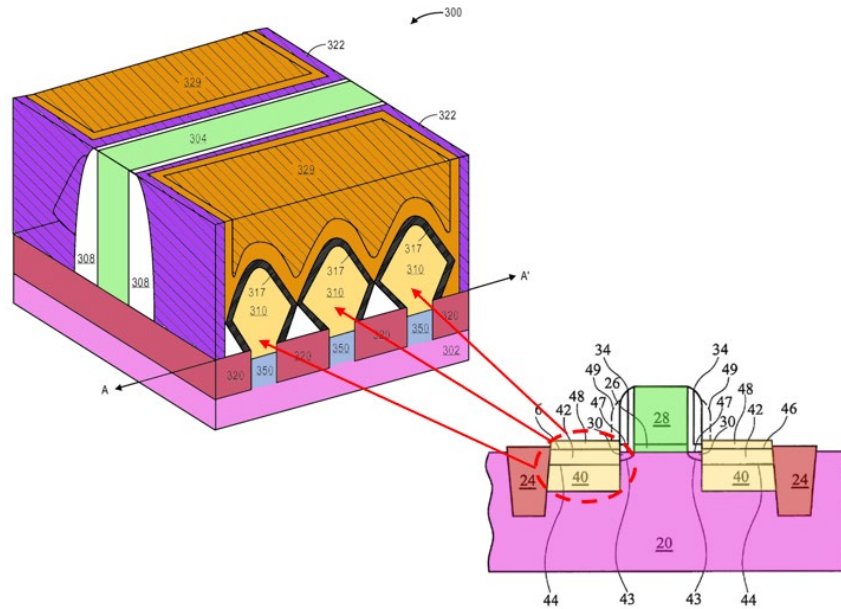
(below-left), and different germanium concentrations, as shown for one embodiment in Figure 8C (below-right). (TSMC-1006, 2:19-33.)



Tsai, Figures 7C (left), 8C (right)

B. Glass-Tsai Combination

A POSITA would have been motivated to combine Tsai’s three-region source/drain stressor teachings with Glass’s device. (TSMC-1003, ¶¶107, 115-117.) Specifically, as illustrated below, a POSITA would have been motivated to use a three-layer stressor, as taught by Tsai, to form Glass’s source/drain layers 310 (“*epitaxial structures*”). (TSMC-1003, ¶107.)

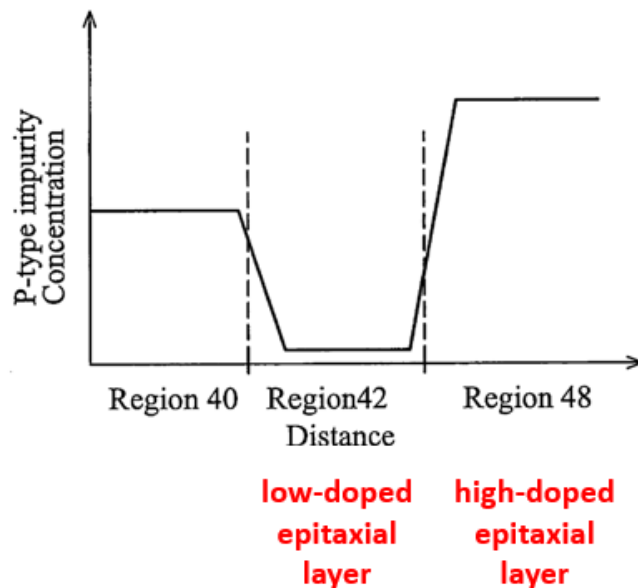


Glass, Figure 3I (top); Tsai, Figure 6 (bottom)

The above Glass-Tsai combination renders claim 6 obvious. Tsai's "SiGe regions 40 preferably have a lattice spacing greater than the lattice spacing of substrate 20." (TSMC-1006, 5:9-11.) SiGe regions 40 also advantageously "have a relatively low germanium concentration" and therefore "the lattice constant of Si Ge regions 40 will be closer to the lattice constant in substrate 20" leading "to a reduced interface stress." (TSMC-1006, 7:41-45.) Second SiGe regions 42 are formed on SiGe regions 40. (TSMC-1006, 5:28-29.) The germanium in SiGe regions 42 has "a greater atomic percentage than in SiGe regions 40." (TSMC-1006, 5:29-31.) A POSITA would understand SiGe regions 40 act as a transition layer enabling the higher Ge-concentration regions 42 to be formed in the source/drain regions with reduced interfacial stress and fewer defects. (TSMC-

1003, ¶109.) Tsai's epitaxial layer 40 in the Glass-Tsai combination is therefore a "liner" [6C]. (*Id.*)

Tsai's Figure 7C (below) "illustrates a gradient profile of in-situ doped p-type impurities" where the "Y-axis indicates schematic impurity concentration, while the X-axis represents vertical distances between bottom surfaces of SiGe regions 40 and points in SiGe regions 40, 42 and 48." (TSMC-1006, 6:60-61, 6:35-38.) As shown, the "impurity concentration in the interface regions between SiGe regions 42 and SiGe regions 40 and/or 48 may be gradually changed" by, for example, "gradually changing the dosage of the impurity implantation when forming the interface regions." (TSMC-1006, 6:61-65.)

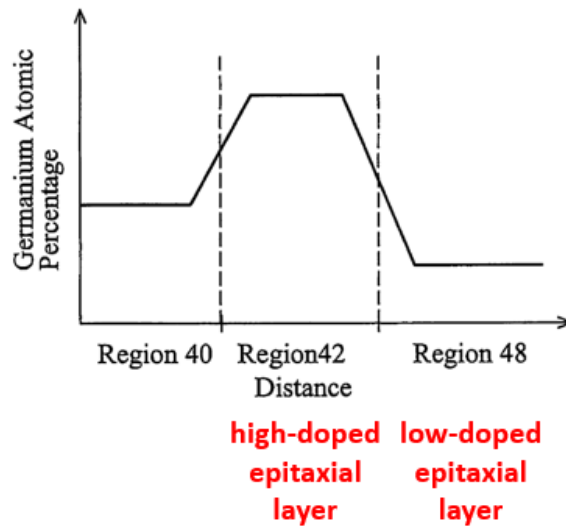


Tsai, Figure 7C

SiGe region 42, having a low impurity percentage, is a “*low doped epitaxial layer*” [6A] and SiGe region 48, having a high percentage, is a “*high doped epitaxial layer*” [6B]. (TSMC-1003, ¶¶110-112.) Tsai explains “having a low impurity percentage in SiGe regions 42 has two advantageous features.” (TSMC-1006, 6:66-67.) First, SiGe regions 42 “act as a sink, or a diffusion barrier, for laterally diffused p-type impurity ... to the channel region, and thus the short channel characteristics are improved.” (TSMC-1006, 6:67-7:2.) Second, “the commonly used p-type impurities, such as boron, has the effect of reducing the lattice constant of SiGe regions 42, and thus with less p-type impurities in SiGe regions 42, the adverse effect to the stress applied to the channel region is reduced”, meaning “the high channel stress can be preserved, since boron will adversely reduce the compressive channel stress.” (TSMC-1006, 7:2-11.)

Should PO argue “*low doped epitaxial layer*” [6A] and “*high doped epitaxial layer*” [6B] refer to epitaxial layers with an alleged low and high Ge concentration (TSMC-1001, 5:35-58), Tsai still discloses these limitations. Tsai’s Figure 8C (below) “schematically illustrate[s] distributions of germanium in SiGe regions 40, 42 and 48” with the “Y-axis indicates germanium atomic percentages, while the X-axis also represents a vertical distance from the bottom surface of SiGe regions 40 to points in stress regions 40, 42 and 48.” (TSMC-1006, 7:18-22.) As illustrated in Figure 8C, “SiGe regions 42 have a higher germanium

concentration than SiGe regions 40 and 48.” (TSMC-1006, 7:34-35.) Accordingly, SiGe region 42 is “a *high doped epitaxial layer*” [6B] and SiGe region 48 is “a *low doped epitaxial layer*” [6A]. (TSMC-1003, ¶113.) As discussed above, SiGe region 40 is a “*liner*” [6C]. (*Id.*)



Tsai, Figure 8C

C. Motivation to Combine

A POSITA would have been motivated to combine Glass and Tsai. Tsai and Glass are in the same field as the '193 patent—FET semiconductor devices.

(TSMC-1001, 1:15-17; TSMC-1005, 1:11-13; TSMC-1006, 1:11-13.)

Additionally, Tsai is pertinent to the problem the '193 patent is concerned with—using strained-silicon technology to improve device performance. (TSMC-1003, ¶115; TSMC-1001, 1:32-34; TSMC-1005, 1:32-52.) It was well understood the fabrication of FinFET devices use “conventional planar MOSFET technology”,

e.g., as taught in one of the first FinFET patents and in Tsai. (TSMC-1017, Abstract; *see also* TSMC-1005, 11:43-64; TSMC-1003, ¶115.) Indeed, Glass refers to a FinFET fabrication method when describing its planar MOSFET. (TSMC-1005, 11:43-64 (“planar method is similar to the method described with reference to FIG. 2 and the finFET structure in FIGS. 3A-H”).) Accordingly, Tsai’s teachings are highly pertinent to Glass. (TSMC-1003, ¶115.)

Tsai motivates the combination. Glass discloses the dopant of the epitaxial source/drain layer includes boron. (TSMC-1005, 7:59-65.) Tsai teaches conventional stressor formation, using boron as p-type impurity for source/drain regions, suffers drawbacks. (TSMC-1006, 1:52-55.) As an example, “a high boron concentration results in more boron laterally diffused into channel regions, and the short channel characteristics are adversely affected.” (TSMC-1006, 1:59-62.) Tsai further teaches “having a low impurity percentage in SiGe region 42” improves short-channel characteristics because these regions “act as a sink, or a diffusion barrier, for laterally diffused p-type impurity” and preserve “the high channel stress.” (TSMC-1006, 6:67-7:2.) Based on Tsai’s teachings, a POSITA would have been motivated to use Tsai’s layered epitaxial layer teaching in Glass’s source/drain layers (“*epitaxial structures*”) to improve short-channel characteristics without sacrificing channel stress for devices. (TSMC-1003, ¶116.)

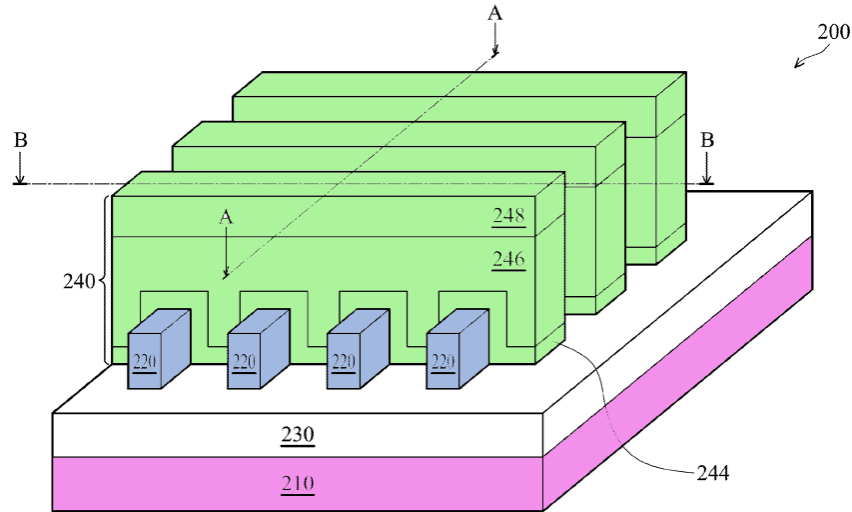
Moreover, the combination is nothing more than the combination of known prior art elements (Glass's FinFET with Tsai's varying concentration epitaxial layers) according to known methods for the above reasons. (TSMC-1003, ¶117; *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 416-17 (2007).) The results of the combination would have been predictable, and a POSITA would have had a reasonable expectation of success, because Tsai uses conventional functionality to perform its epitaxy. (TSMC-1003, ¶117.)

VII. GROUND 3: Kelly-Murthy Combination Renders Claims 1-10 Obvious.

A. Combination Overview

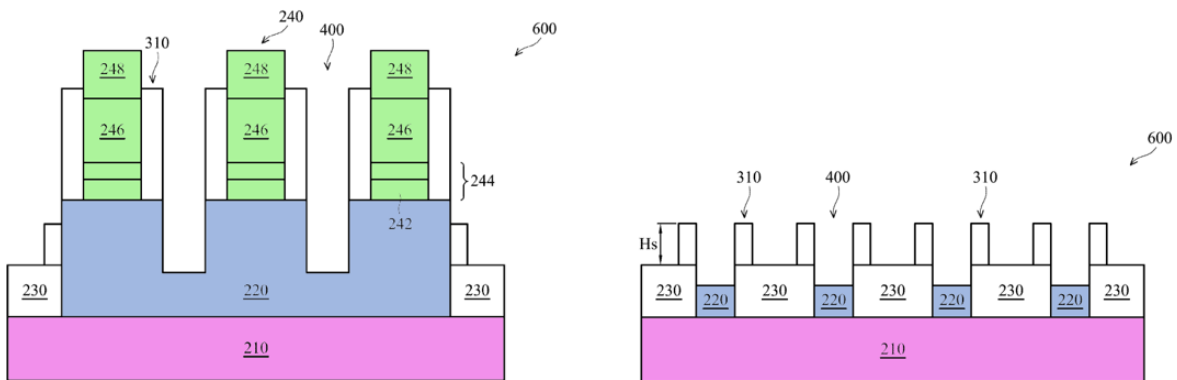
1. Kelly

Kelly's FinFET fabrication method receives FinFET precursor 200 including substrate 210 (pink), multiple fins 220 (blue), and gate stacks 240 (green) "formed over the substrate 210 including over (wrapping) a portion of the fin 220." (TSMC-1009, 2:31-33, 2:66-67, 3:48-49, Figure 2 (below).)



Kelly, Figure 2

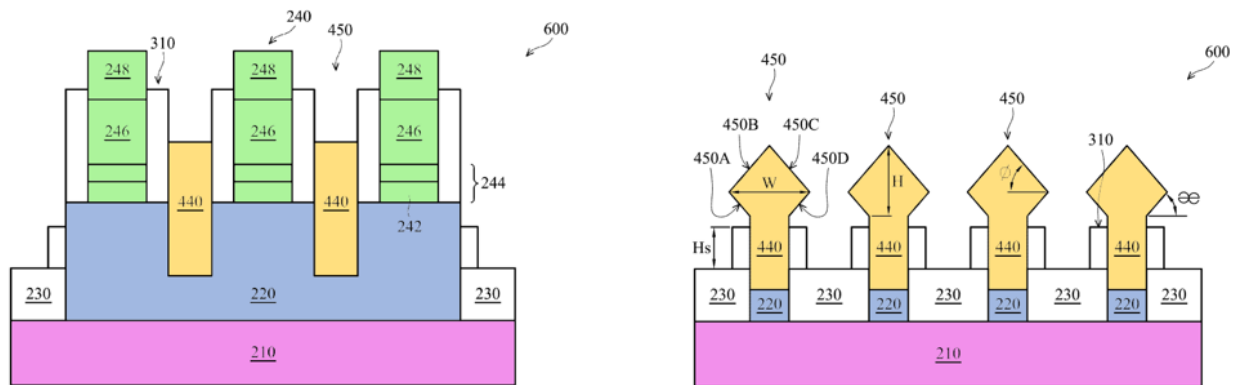
Sidewall spacers 310 are formed “along the gate stack 240 and the fin 220.” (TSMC-1009, 4:44-47.) Fins 220 are etched to form recessing trench 400 having “the sidewall spacer as its upper portion.” (TSMC-1009, 4:63-66, Figures 5A-5B (below).)



**Kelly, Figures 5A, Cross-Section Along A-A (left),
5B, Cross-Section Along B-B⁵ (right)**

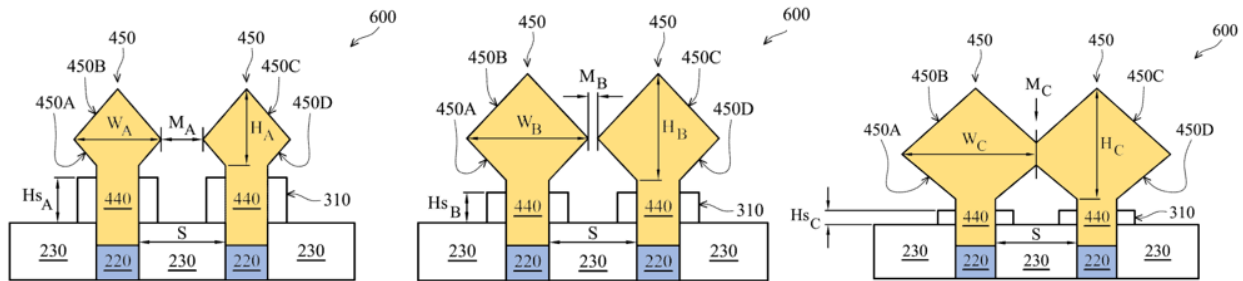
⁵ Line B-B is between adjacent gate structures.

Source/drain epitaxial structures 450 are then formed “above the recessing trench 400” “by epitaxially growing a semiconductor material 440.” (TSMC-1009, 5:23-36, Figures 6A-6B (below).)



**Kelly, Figures 6A, Cross-Section Along A-A (left),
6B, Cross-Section Along B-B (right)**

Kelly describes embodiments of its FinFET with a fixed spacing distance (S) between two adjacent fins 220 and different fin-spacer-heights (Hs), resulting in epitaxial structures 450 with different heights [H] and widths [W] and different merging distance (M) between two adjacent epitaxial structures 450. (TSMC-1009, Figures 7A-7C (below), 5:65-6:1, 6:1-3 (M is “distance between two nearest vertexes of two adjacent epitaxial structures 450”).) “[T]wo adjacent vertexes merge together”, as shown in Figure 7C, when “M has a value from zero to a negative value.” (TSMC-1009, 6:3-5.)

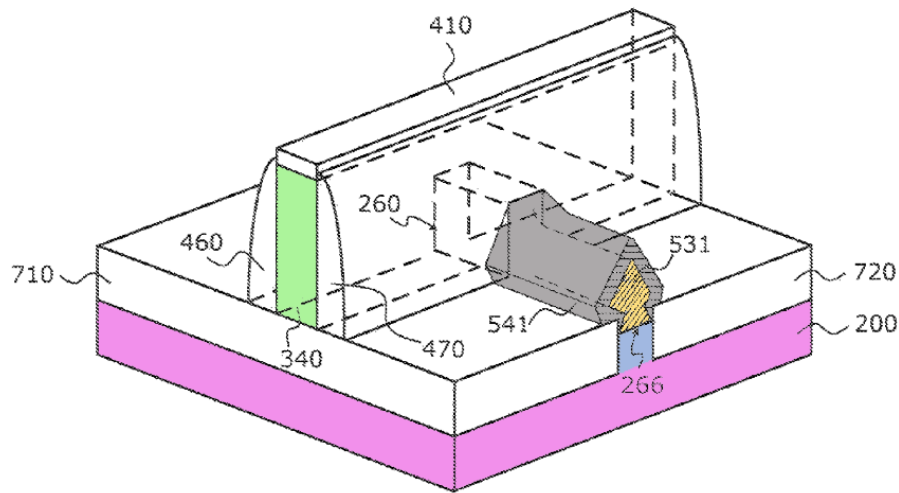


Kelly, Figures 7A (left), 7B (middle), 7C (right)

Kelly’s FinFET device may further “include additional features” such as “various contacts/vias/lines and multilayer interconnect features” that are “formed by subsequent processing.” (TSMC-1009, 6:35-40.)

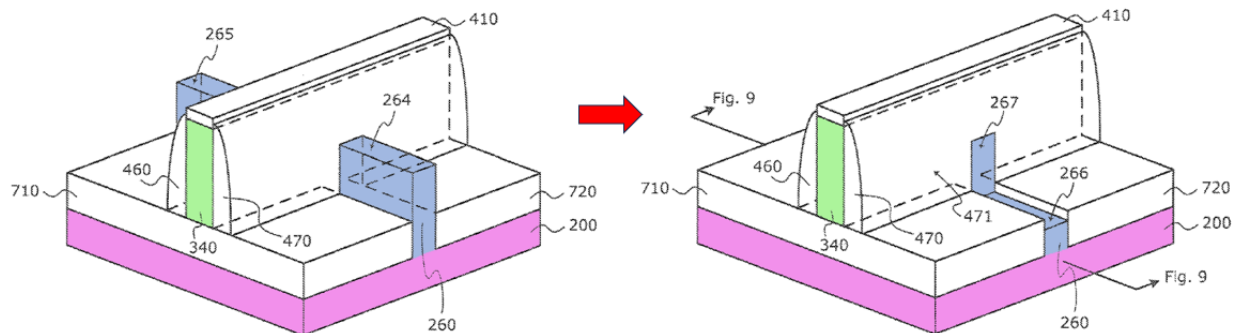
2. Murthy

Murthy describes a semiconductor tri-gate (FinFET) device “having doped epitaxial regions.” (TSMC-1010, 1:7-9.) Murthy’s FinFET includes substrate 200 having fin 260 (represented by dashed lines) and gate electrode 340 (green) “formed over 3 surfaces of the fin 260.” (TSMC-1010, 4:44-48.) The device’s source/drain region comprises a structure having “epitaxial region 531 [yellow] formed on a recessed source interface 266 and on a fin 260 sidewall” and outer “cap layer 541” (grey) “deposited over” epitaxial region 531. (TSMC-1010, 4:50-53.)



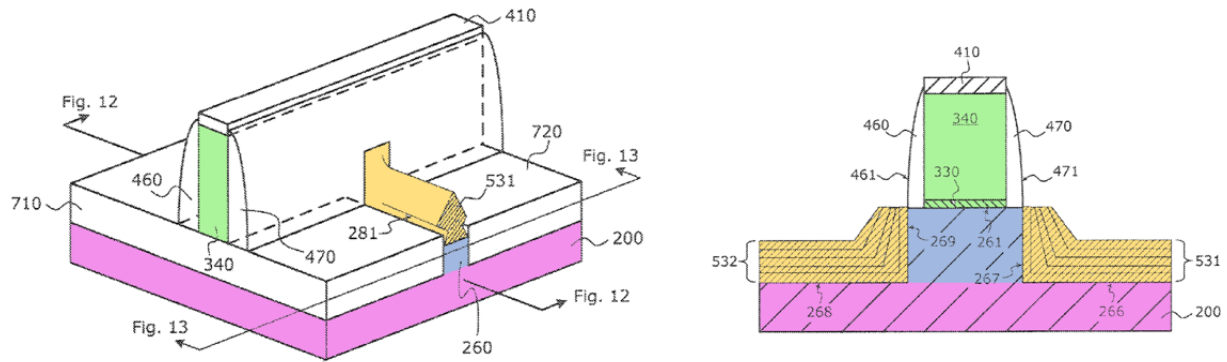
Murthy, Figure 4

During fabrication, to form these source/drain structures (epitaxial layer 531 and cap layer 541), exposed portions 264, 265 of the fin 260 are etched to create recesses. (TSMC-1010, 13:52-53, Figure 8E (right).)



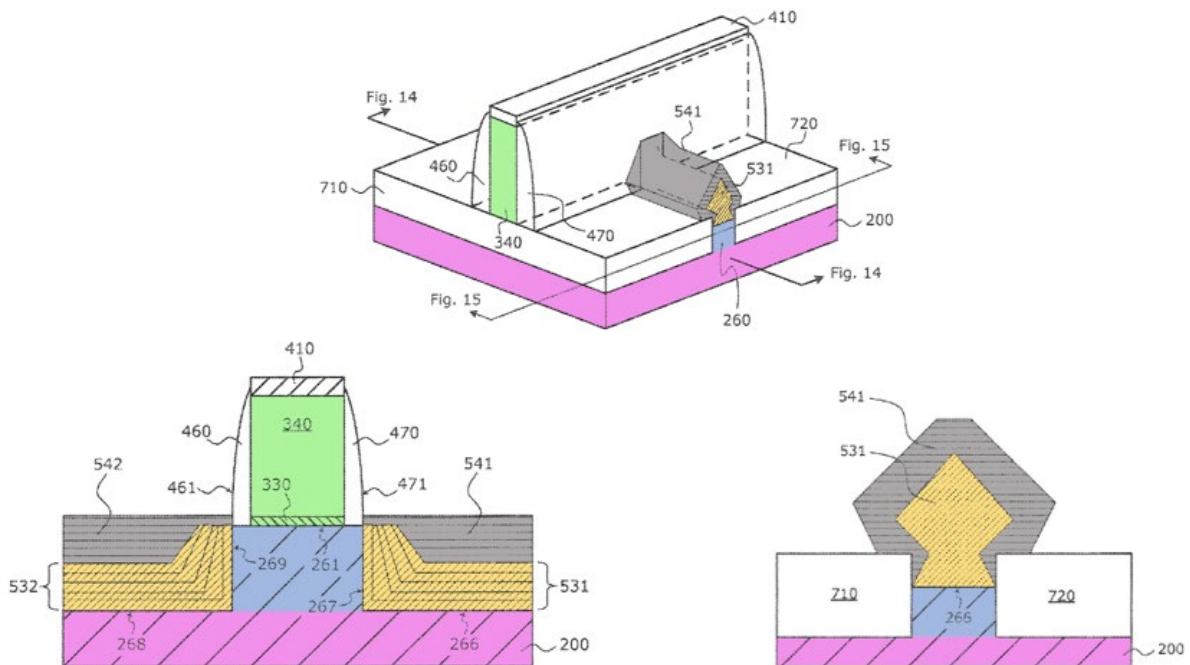
Murthy, Figures 8D (left), 8E (right)

Epitaxial regions 531/532 are then formed through a series of deposition-etch cycles until the “desired number of epitaxial films are deposited.” (TSMC-1010, 14:50-56, Figure 12 (below-right; showing epitaxial regions 531/532 comprising five epitaxial films).)



Murthy, Figures 8H (left), 12 (right)

After formation of epitaxial regions 531/532, epitaxial “cap layers 541, 542 are selectively deposited” over epitaxial regions 531/532 “in a sing[l]e deposition process.” (TSMC-1010, 15:17-20, 3:34-36 (cap layers “are epitaxial layers”), Figure 8I (top), Figure 14 (bottom-left), Figure 15 (bottom-right).)

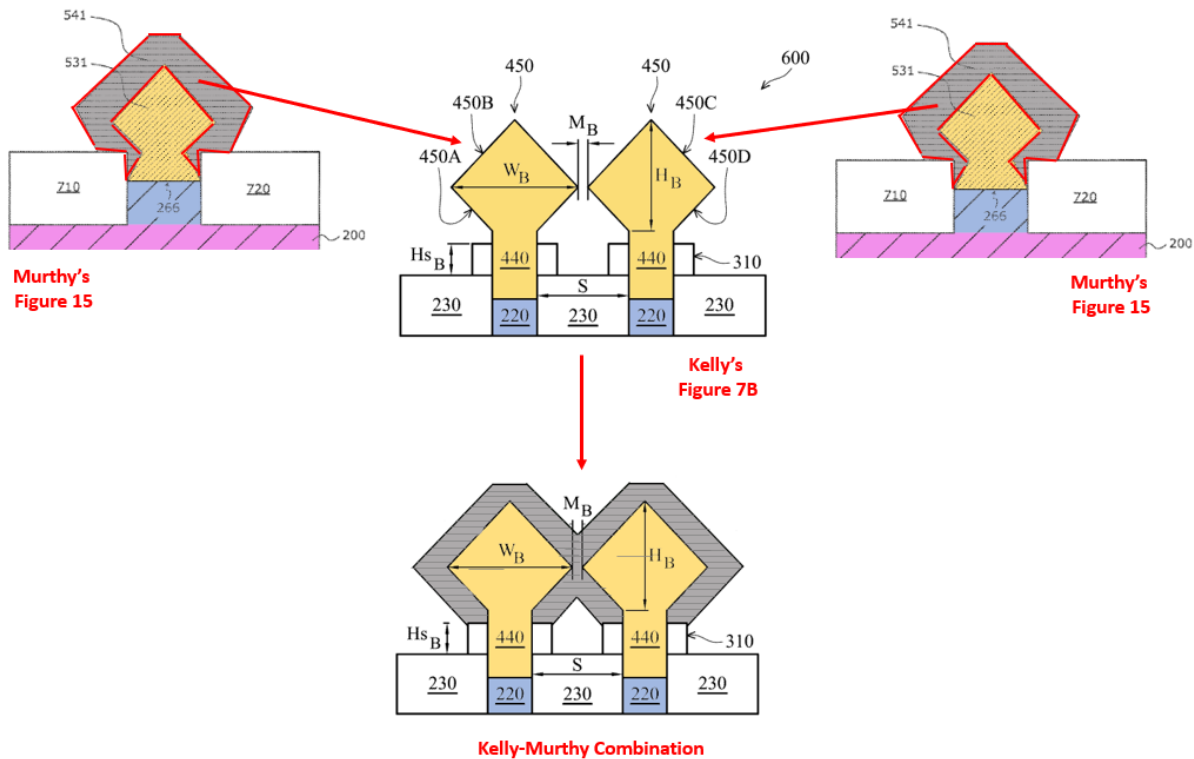


Murthy, Figures 8I (top), 14 (bottom-left), 15 (bottom-right)

3. Kelly-Murthy Combinations

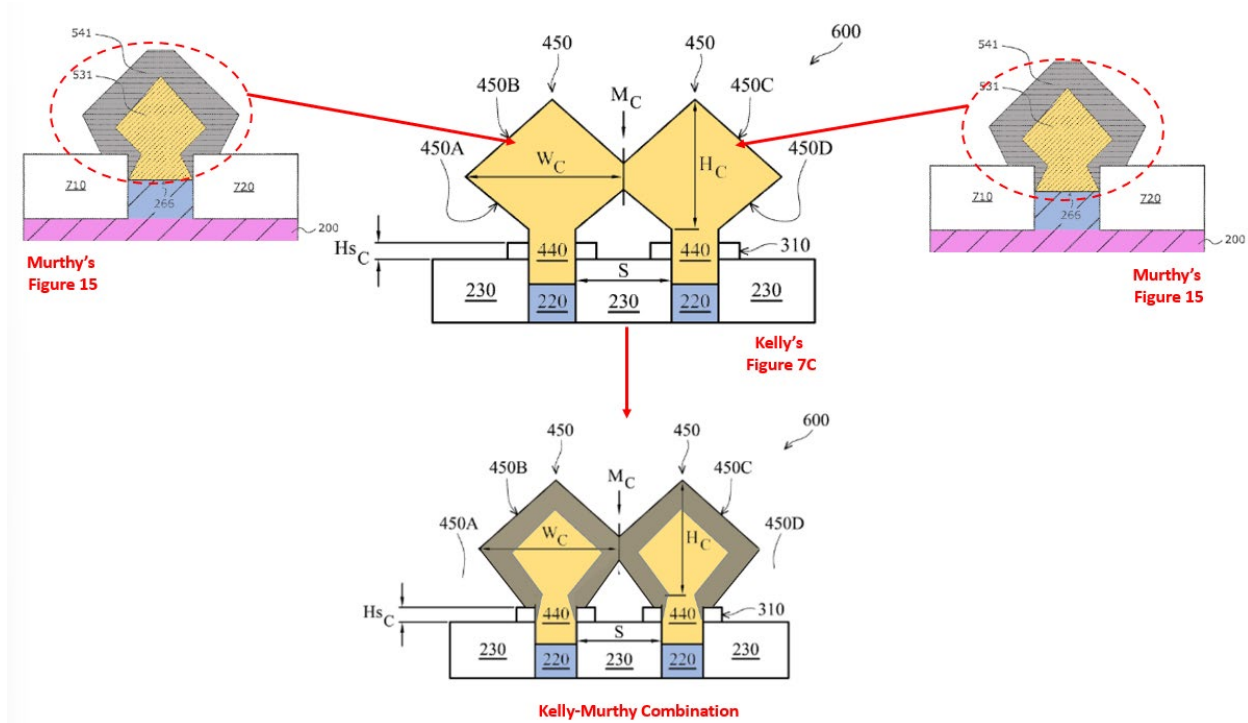
Petitioner's presents two combinations: (1) Kelly's FinFET with the source/drain arrangement of Figure 7B structures and Murthy ("first combination"); and (2) Kelly's FinFET with the source/drain arrangement of Figure 7C and Murthy ("second combination"). Should PO argue Petitioner is combining embodiments in Kelly, Petitioner disagrees. Regardless, a POSITA would have been motivated to use the source/drain structures of either Figure 7B or Figure 7C in Kelly's FinFET. (TSMC-1003, ¶126.)

A POSITA would have been motivated to combine Murthy's teachings regarding use of source/drain structures including an epitaxial region and a cap with Kelly's multi-fin device embodiments of Figures 7B or 7C. (TSMC-1003, ¶¶127-133.) Specifically, for the first combination, a POSITA would have been motivated to grow Murthy's cap 541/542 on the epitaxial structures 450 of Kelly's Figure 7B. (TSMC-1003, ¶127.) The bottom figure depicts an exemplary combination of Murthy and Kelly (first combination). (*Id.*) In the combined device, caps 541/542 of adjacent source/drain structures merge during epitaxial growth; the underlying epitaxial structures 450 remain separated. (*Id.*)



First Kelly-Murthy Combination

In the second combination, a POSITA would have been motivated to use Murthy's source/drain structure having epitaxial region 531/532 and cap 541/542 as Kelly's epitaxial structures 450 of Figure 7C. (TSMC-1003, ¶128.) The bottom figure depicts an exemplary combination of Murthy and Kelly (second combination). (*Id.*) In the combined device, because the source/drain structures merge, caps 541/542 (which surround the epitaxial regions 531/532) merge during epitaxial growth; the underlying epitaxial regions 531/532 remain separated. (*Id.*)



Second Kelly-Murthy Combination

A POSITA would have been motivated to combine Kelly and Murthy in both ways. (TSMC-1003, ¶¶129-133.) First, Kelly expressly motivates adding a cap layer to its epitaxial structure (first combination) or using both Murthy's epitaxial region and cap (second combination), stating that Kelly's FinFET device may further "include additional features" such as "various contacts/vias/lines and multilayer interconnect features" that are "formed by subsequent processing." (TSMC-1009, 6:35-40.) One such additional feature would be a cap layer over the epitaxial structures 450 that reduces "parasitic resistance provided by very high phosphorus doping in the ($\text{Si}_y\text{P}_{1-y}$) epitaxial cap layer," as taught in Murthy. (TSMC-1010, 2:16-21, 4:38-42, 15:28-32; TSMC-1003, ¶129.)

Second, a POSITA would have been motivated to grow Murthy's cap layer on Kelly's Figure 7B epitaxial structures 450 to create a merged source/drain structure (first combination) or to use Murthy's source/drain structure having an epitaxial region and cap layer in Kelly's epitaxial structure 450 of Figure 7C (second combination) to improve device performance. (TSMC-1003, ¶130.) Murthy teaches its epitaxial region and cap "provide[] a dramatic transistor performance gain due to combined effects of increased electron mobility gain at channel region, reduced short-channel effects (due to carbon suppressing phosphorus diffusion), and reduced parasitic resistance provided by very high phosphorus doping in the ($\text{Si}_y\text{P}_{1-y}$) epitaxial cap layer." (TSMC-1010, 2:16-21, 4:38-42, 15:28-32 ("phosphorus doped silicon cap layers 541, 542 provide an advantage of inducing tensile stress on the channel region of the semiconductor fin 260, which increases the electron mobility and improves the device performance").) Indeed, Kelly stresses a goal of its method is to "improve[] FinFET device performance." (TSMC-1009, 6:46-52.) A POSITA would have also understood the resulting merged source/drain structure of the first combination and the second combination increases the source/drain contact area which in turn reduces the contact resistance and eliminates the need for source/drain pads which degrade the layout efficiency of FinFETs. (TSMC-1012, 100-101.)

Third, Kelly states that epitaxial structures 450 “may be formed by **one or more epitaxy or epitaxial (epi) processes**, such that **one or more epitaxial features**, such as Si features, SiGe features, and/or other suitable features can be formed in a crystalline state on the recessed fin 220.” (TSMC-1009, 5:46-50; *see also* TSMC-1009, claims 4 and 19 (reciting “epitaxial structures are formed by **multiple deposition processes**”).) However, Kelly does not provide further details regarding multiple epitaxial processes and features. (TSMC-1003, ¶131.) A POSITA would have therefore been led to Murthy, which is in the same field of endeavor as Kelly and the ’193 patent (FET semiconductor devices) and is directed to “a semiconductor device having doped epitaxial regions”, to provide additional details. (TSMC-1010, 1:8-10, 3:34-36, 4:41-43; TSMC-1001, 1:15-17; TSMC-1009, 2:4-15; TSMC-1003, ¶131.)

Fourth, the first combination is merely use of a known technique (addition of a cap layer) to a known device (Kelly’s Figure 7B FinFET) ready for improvement to yield predictable results, discussed below. The second combination is merely the simple substitution of one known element (Murthy’s source/drain structure having an epitaxial region and cap) for another (Kelly’s epitaxial structure) to obtain predictable results. (TSMC-1003, ¶132, *KSR*, 550 U.S. at 416-17.)

Finally, the results of either combination would have been predictable, and a POSITA would have had a reasonable expectation of success in both

combinations. (TSMC-1003, ¶133.) Both Kelly and Murthy disclose a FinFET having a substrate, fin, and gate covering the fin. (§§VII.A.1, 2.) Both Kelly and Murthy form epitaxial source/drain regions on one side of the gate that directly contact the fin. (§§VII.A.1, 2.) Kelly further teaches “[w]here an N-type FET (NFET) device is desired, the source/drain epitaxial structures 450 may include an epitaxially growing silicon (epi Si) 440” which “may be doped with carbon to form Si:C source/drain features, phosphorous to form Si:P source/drain features, or both carbon and phosphorous to form SiCP source/drain features.” (TSMC-1009, 5:36-41, 6:13-16.) Similarly, Murthy teaches epitaxial regions 531/532 “are crystalline films having silicon and carbon doped with phosphorus” and “cap layers 541, 542 are epitaxial layers containing silicon doped with phosphorus.” (TSMC-1010, 8:42-48.) Further, both Kelly and Murthy disclose commonly used deposition methods for their epitaxial layers. (*See, e.g.*, TSMC-1009, 5:50-53 (disclosing “epitaxial processes include CVD deposition techniques ..., molecular beam epitaxy, and/or other suitable processes”); TSMC-1010, 2:7-11 (providing “cyclical deposition-etch process”).) Based on the similarities between Kelly’s and Murthy’s devices and use of known fabrication techniques for both, a POSITA would have had a reasonable expectation of success in the combination and the results would have been predictable. (TSMC-1003, ¶133.)

B. Independent Claim 1

1. Preamble [1P]

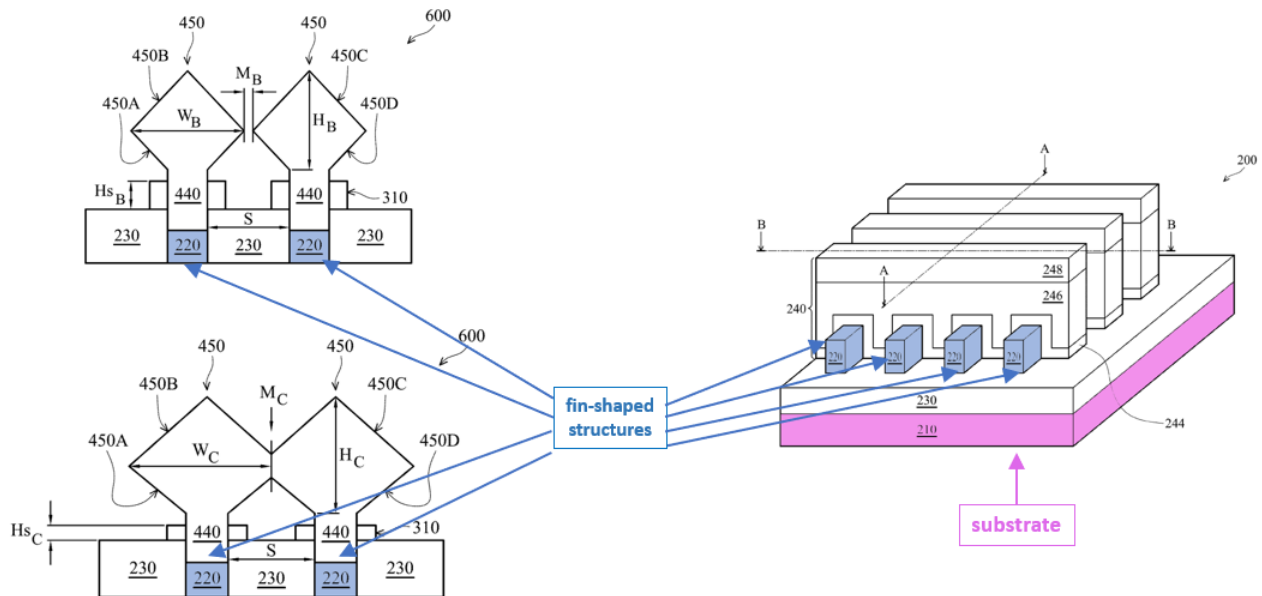
The first and second Kelly-Murthy combinations each discloses a “*semiconductor device*” [1P]. (TSMC-1003, ¶134.) Kelly’s FinFET device having the source/drain structure arrangement of either Kelly’s Figure 7B or Figure 7C is a semiconductor device, for example, “a complementary metal-oxide-semiconductor (CMOS) device comprising a P-type metal-oxide-semiconductor (PMOS) FinFET device and an N-type metal-oxide-semiconductor (NMOS) FinFET device.” (TSMC-1009, 2:4-10, 2:16-24; *see also* TSMC-1005, 3:36-37 (“As is known, a FinFET is a transistor built around a thin strip of semiconductor material generally referred to as the fin”).)

2. Basic FinFET Components [1A]-[1B]

a) Limitation [1A]

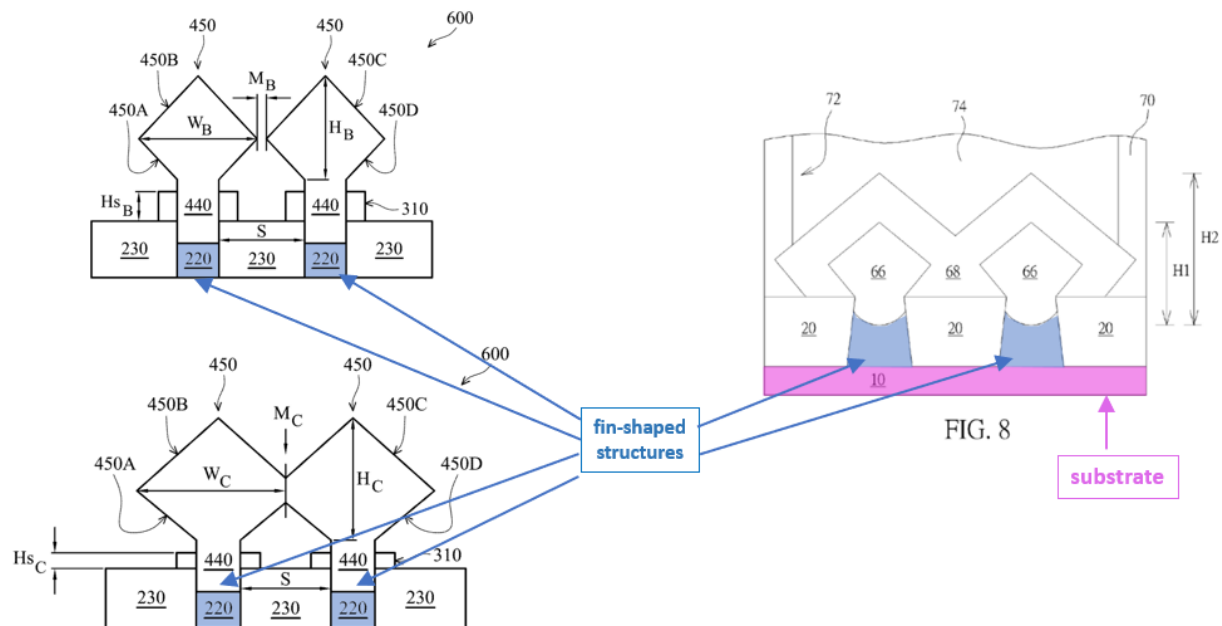
The first and second Kelly-Murthy combinations each discloses a device having “*at least two fin-shaped structures disposed on a substrate*” [1A]. (TSMC-1003, ¶¶135-137.) During Kelly’s fabrication process, a “FinFET precursor” is provided having substrate 210 and multiple fins 220 with a spacing distance (S) to each other.” (TSMC-1009, 2:31-33 (method “receiv[es] FinFET precursor 200, as shown in FIGS. 2, 3A and 3B”), 2:65-67, Figure 2 (below-right).) While omitted from Figures 7B-7C, Kelly’s FinFET device 600 having either the Figure 7B or

Figure 7C source/drain structure arrangement includes substrate 210 (depicted in Figures 2-6). (TSMC-1009, Figures 7B-7C (below-left), 1:49-50 (relating Figures 6B and 7B-7C); claims 1, 10, 20 (reciting fabricating a device including “fin structure on the substrate” having “fins spaced apart from each other [by] a spacing distance”), 1:49-50 (stating Figures 6B and 7C “illustrate cross sectional views of a FinFET device along line B-B in FIG.2”); TSMC-1010, 4:44-46.)



Kelly, Figures 7B-7C (left), 2 (right)

Kelly is consistent with the '193 patent, as highlighted in the side-by-side depiction of Kelly's Figures 7B-7C FinFET structures and the '193 patent's semiconductor device.



Kelly, Figures 7B-7C (left); '193 Patent, Figure 8

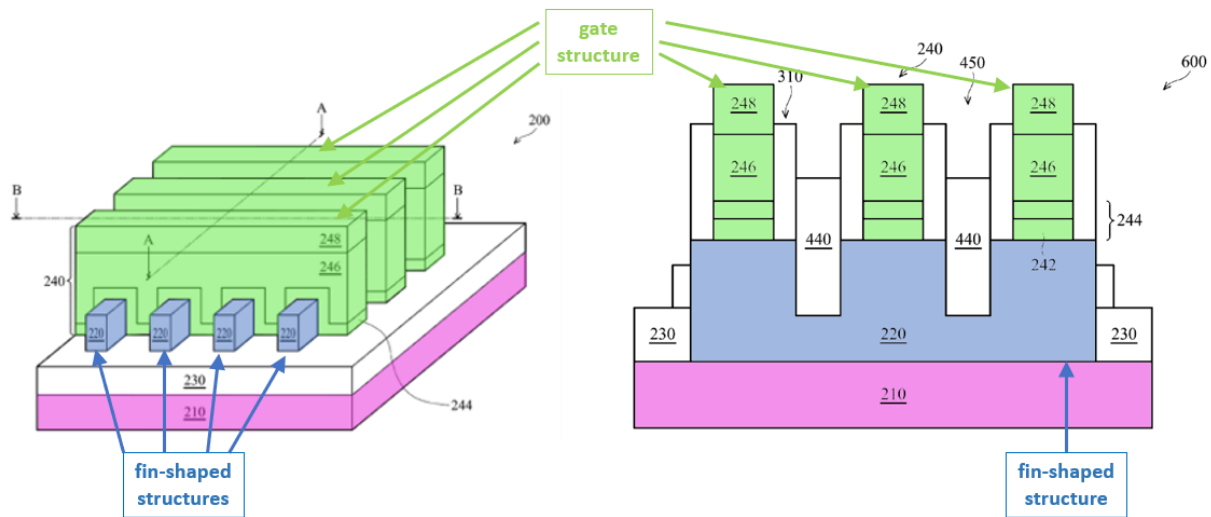
Thus, Kelly discloses a device including “*at least two fin-shaped structures disposed on a substrate*” [1A] and therefore the device of the first combination and the device of the second combination discloses limitation [1A].

b) Limitation [1B]

The first and second Kelly-Murthy combination each discloses a device having “*a gate structure, covering the fin-shaped structures*” [1B]. (TSMC-1003, ¶138.) In Kelly’s FinFET having either the Figure 7B or the Figure 7C source/drain structure arrangement, “[o]ne or more **gate stacks 240** [green] [that] are **formed over the substrate 210** [pink], **including over (wrapping) a portion of the fin 220** [blue].” (TSMC-1009, Figure 2 (intermediate structure), Figure 6A

(showing final device along line A-A⁶), 3:48-49, 1:45-46, claims 10 and 20

(reciting “a gate stack on the substrate”).) As shown, Kelly’s gate stack 240 “include[s] a dielectric layer 244, a gate electrode layer 246 and a hard mask layer 248.” (TSMC-1009, 3:49-51.) Gate stack 240 is a “*gate structure*” that “*cover[s] the fin-shaped structures*” [1B].

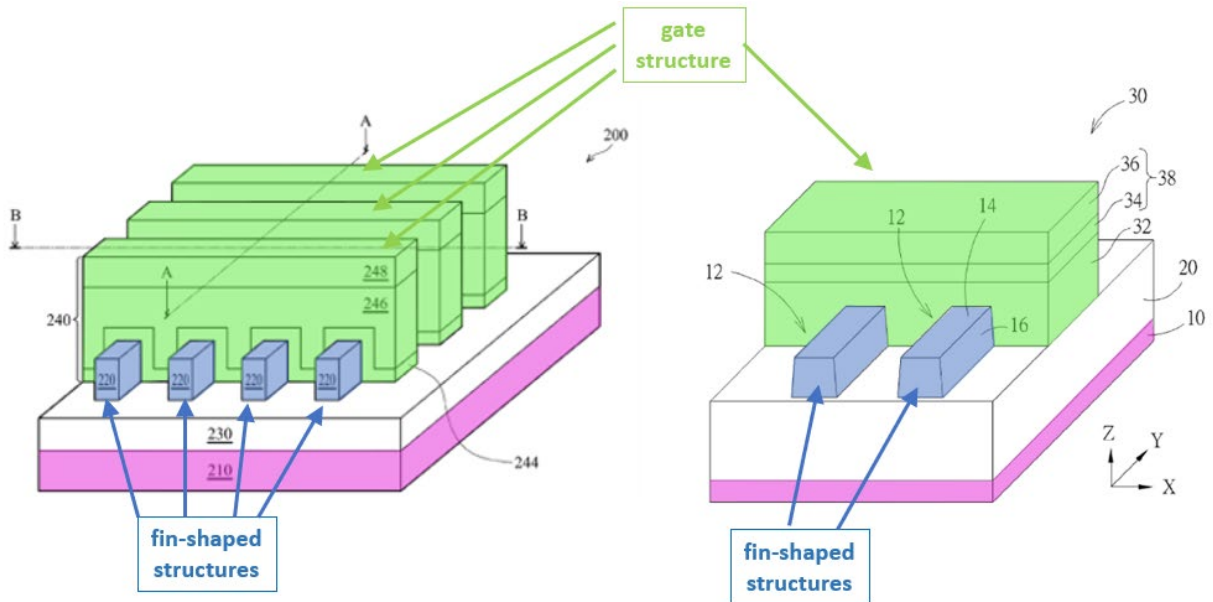


Kelly, Figures 2 (left), 6A (right)

Kelly's gate structure, illustrated in Figure 2 (below-left), is consistent with the '193 patent's gate structure, illustrated in '193 patent's Figure 2 (below-right). Thus, Kelly discloses a device including “*a gate structure, covering the fin-shaped*

⁶ Because Figure 6A is along line A-A, it illustrates a single fin. Because line B-B is a cross-section taken through fins between gates, the gate is not shown in Figures 6B, 7A-7C.

structures” [1B] and therefore the first combination and the second combination each discloses limitation [1B].

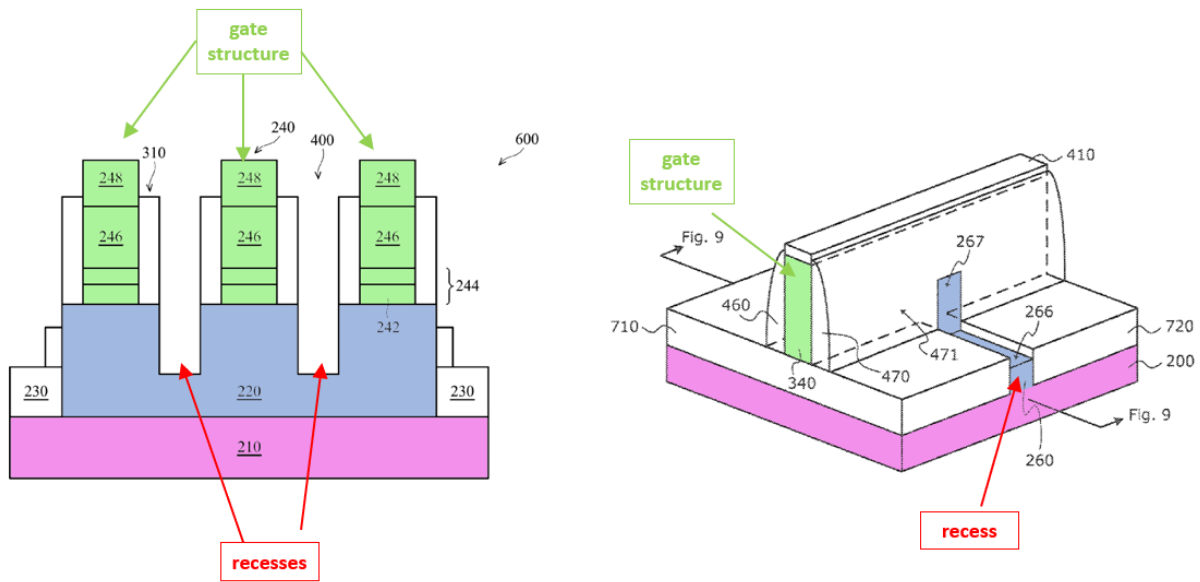


Kelly, Figure 2 (left); '193 Patent, Figure 2 (right)

3. Limitations [1C]-[1D]

The first and second Kelly-Murthy combination each discloses limitations [1C]-[1D]. (TSMC-1003, ¶¶140-155.)

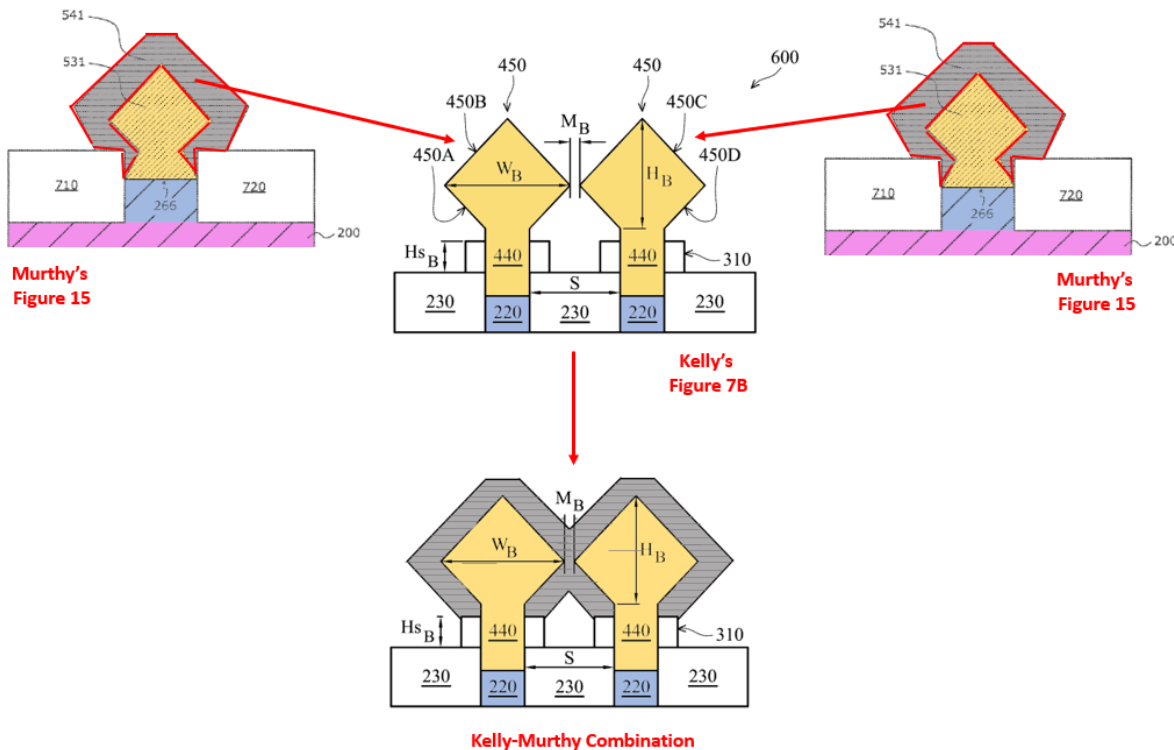
The source/drain structures 450 of each combination are formed by first “recessing fins 220 to form a recessing trench”, illustrated in Kelly’s Figure 5A and Murthy’s Figure 8E. (TSMC-1009, 4:63-64, 5:25-41, 13:22-26, 13:52-54; TSMC-1010, 13:32-26, 13:52-53.) The recesses are located “*at one side of the gate structure.*” (TSMC-1003, ¶141.) The source/drain structures are formed in the recesses differently in each combination, as discussed below.



Kelly, Figure 5A (left); Murthy, Figure 8E (right)

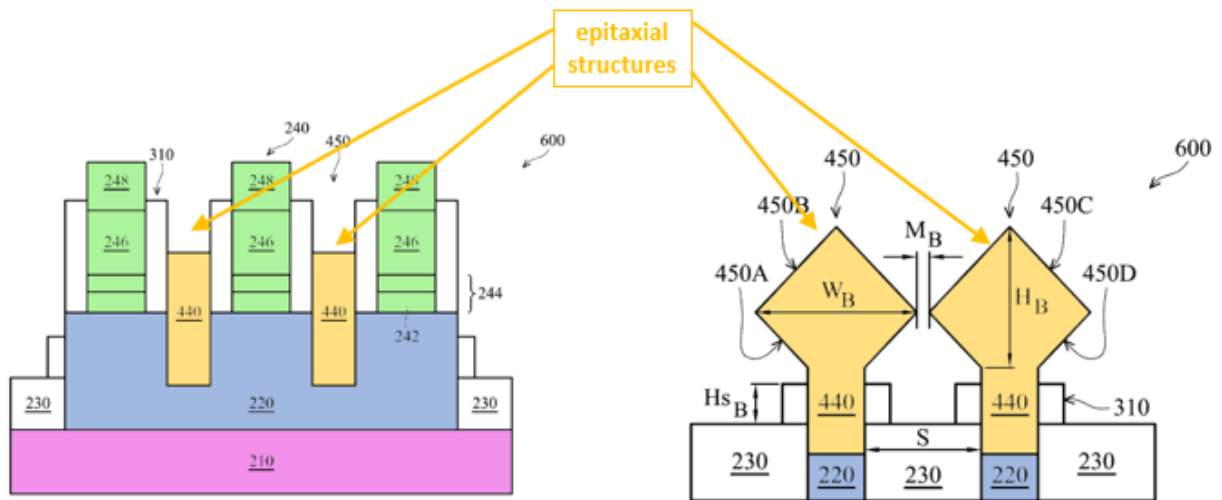
a) First Combination

As discussed in §VII.A.3, in the first Kelly-Murthy combination, Murthy's cap 541/542 is formed on epitaxial structures 450.



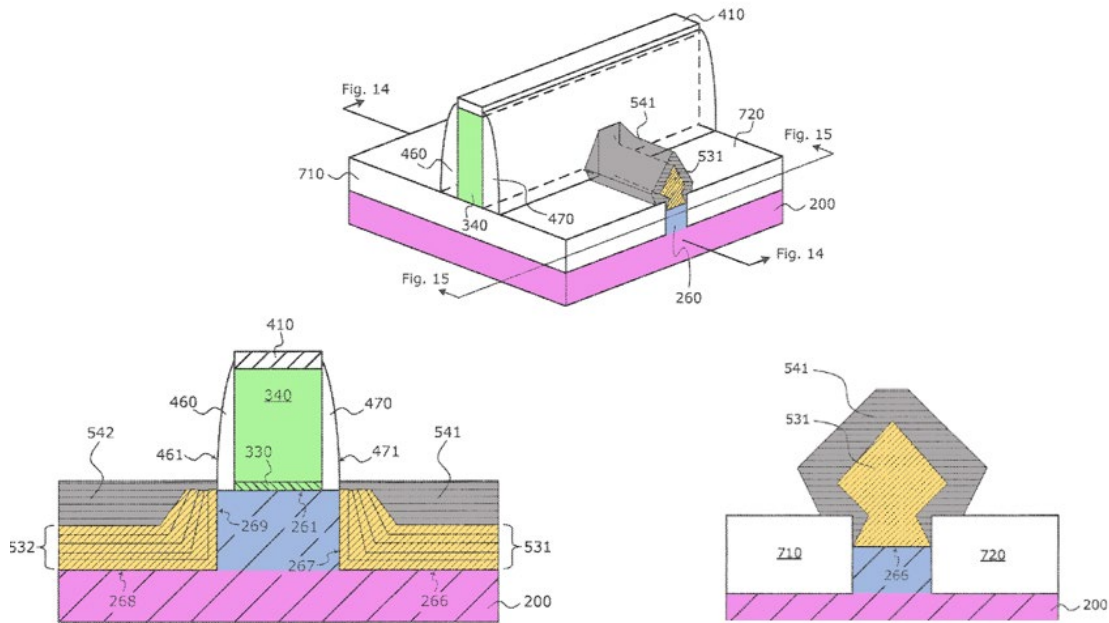
First Kelly-Murthy Combination

In this combination, “semiconductor material 440 epitaxi[a]lly grows on the recessed fins 220 in the recessing trench 400” to form epitaxial structures 450. (TSMC-1009, 5:42-45, Figures 6A, 7B.) The multiple epitaxial structures 450 of Kelly’s Figure 7B FinFET (below) are the “*at least two epitaxial structures.*” And because Kelly’s epitaxial structures 450 are formed in the recesses created adjacent to the gate, the epitaxial structures are “*disposed at one side of the gate structure and respectively directly contacting each fin-shaped structure*” [1C].



Kelly, Figure 6A (left), Figure 7B (right)

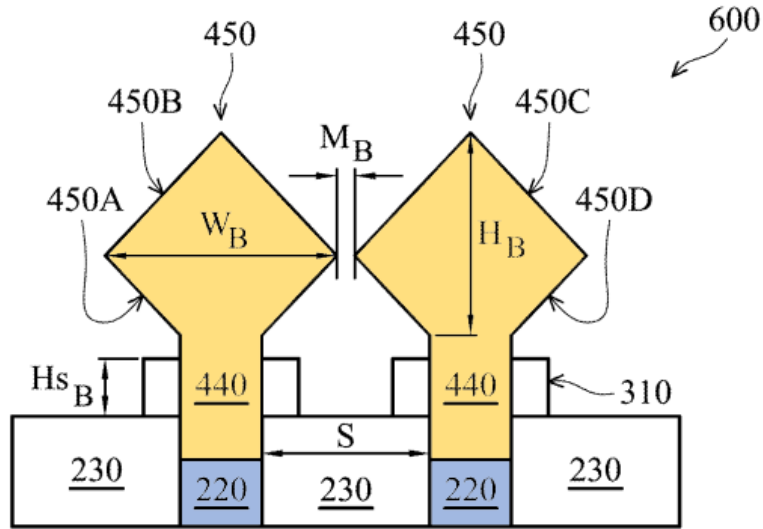
In the first combination, “cap layers 541, 542 are selectively deposited over” Kelly’s epitaxial structures “in a sing[l]e deposition process,” as taught by Murthy. (TSMC-1010, 8:35-37, 11:14-16; Figures 8I, 14-15 below). Murthy’s cap 541/542 surrounds each epitaxial structure 450 in Kelly’s Figure 7B FinFET and therefore, in the combined device, caps 541/542 are the “*at least two caps*” that “*surround[] the epitaxial structures*” [1D]. (TSMC-1003, ¶145.)



Murthy, Figures 8I (top), 14 (bottom left), 15 (bottom right)

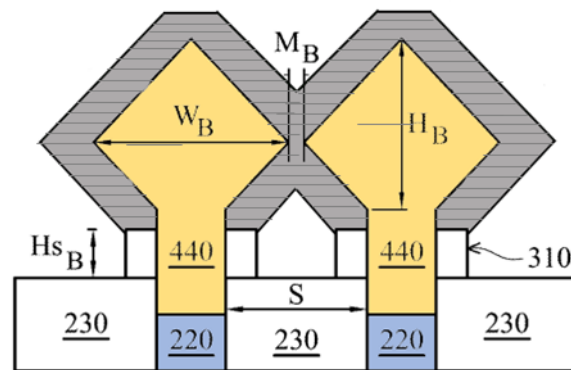
Kelly tunes the merging distance (M^7) of its source/drain epitaxial structures by, e.g., adjusting the fin-spacer-height (H_s). (TSMC-1009, 6:46-50). Specifically, Kelly maintains “fixed spacing distance (S) between adjacent fins 220” but provides embodiments with different merging distances. (TSMC-1009, 5:64-6:1.) In Figure 7B arrangement, the epitaxial structures are separated by a merging distance of M_B greater than zero. Thus, the first combination discloses “*the epitaxial structures are spaced apart from each other*” [1C]. (TSMC-1003, ¶146.)

⁷ M “is defined as the distance between two nearest vertexes of two adjacent epitaxial structures 450.” (TSMC-1009, 6:1-3.)



Kelly, Figure 7B

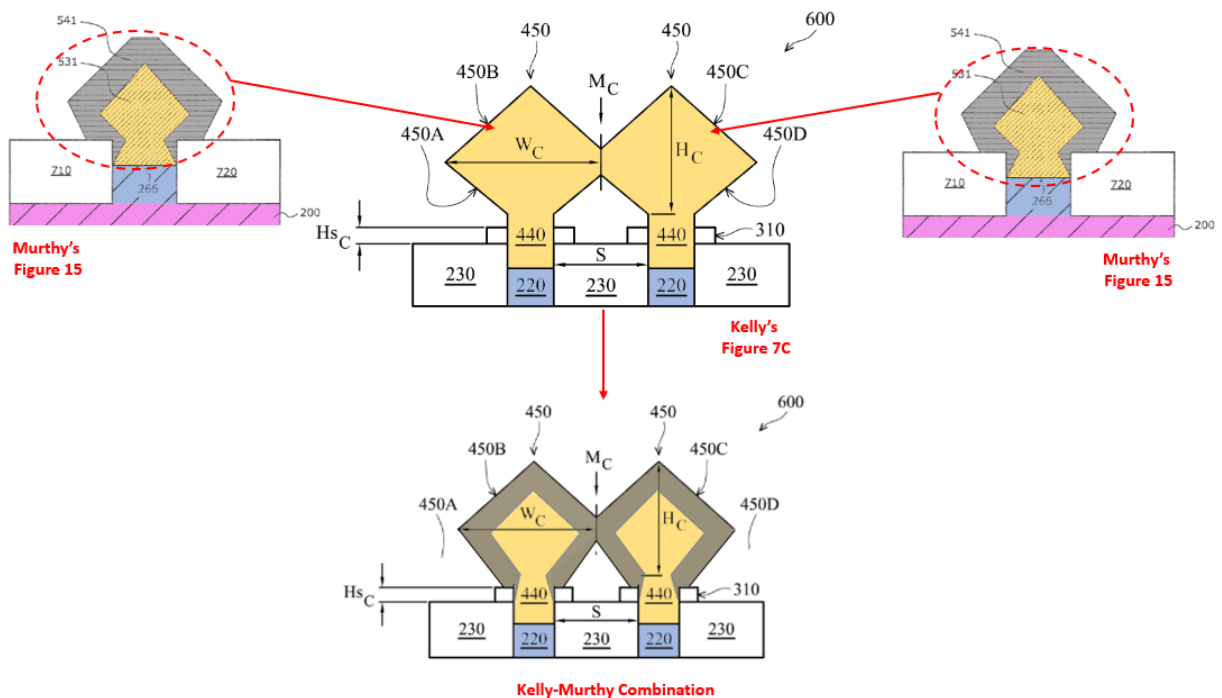
Cap layers “are grown to have a thickness of about 50 to 500 Angstroms” (5nm-50nm) on Kelly’s epitaxial structures 450, as taught by Murthy. (TSMC-1010, 6:36-37, 9:3-4.) A POSITA would have understood that when M_B is less than the thickness of the caps or close to zero, the deposition of the cap layer on each structure 450 causes the caps to merge, as illustrated in the exemplary combination figure below. (TSMC-1003, ¶147.) A POSITA would have been motivated to grow the cap to a thickness such that the adjacent cap layers the merge in the first (Figure 7B) combination to improve the operation of the device, as discussed above in §VII.A.3. Accordingly, the first combination renders obvious the “*at least two adjacent caps are merged together*” [1D]. (TSMC-1003, ¶147.)



First Kelly-Murthy Combination

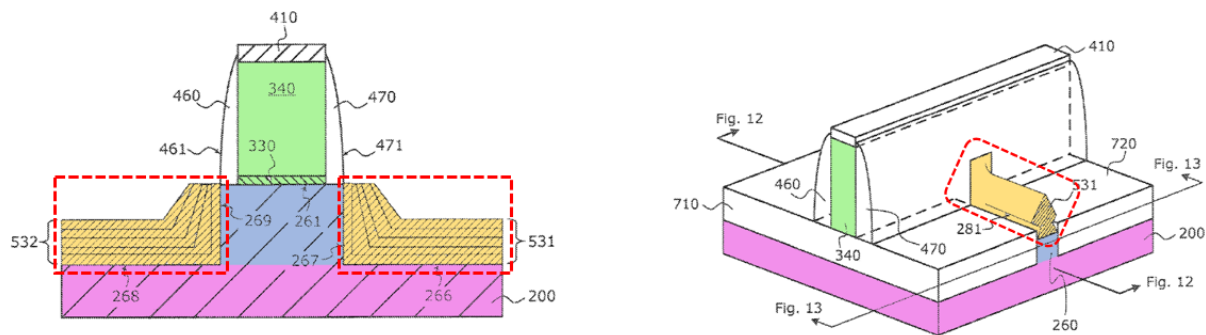
b) Second Combination

As discussed in §VII.A.3, in the second combination, Kelly’s source/drain structures 450 comprise Murthy’s epitaxial region and cap.



Second Kelly-Murthy Combination

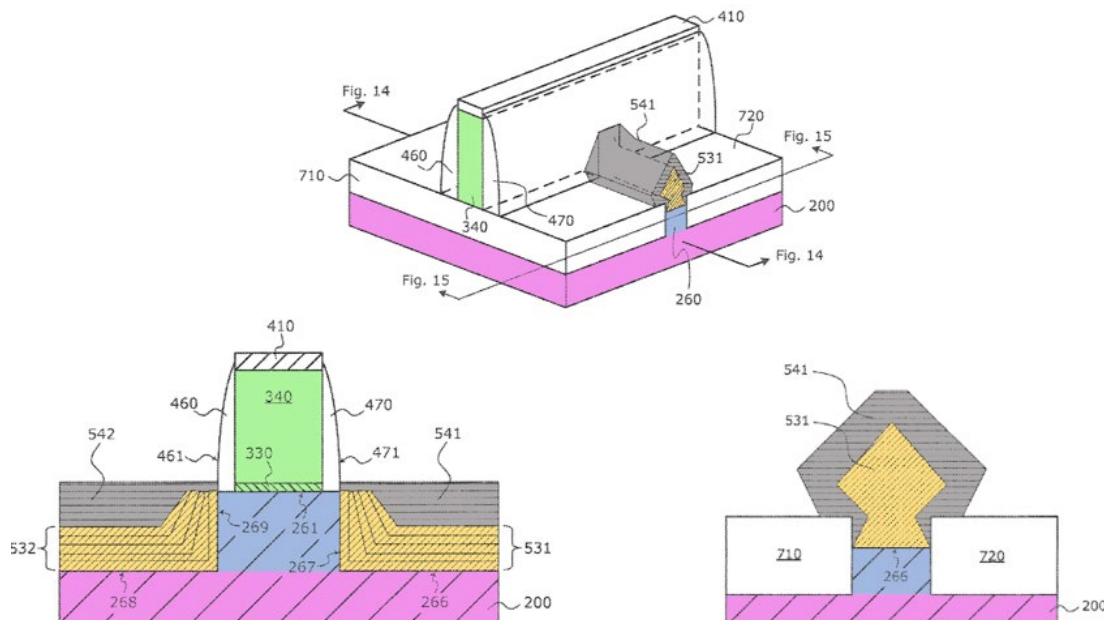
In this combination, Murthy's epitaxial regions 531/532 are formed through a series of deposition-etch cycles until the "desired number of epitaxial films are deposited." (TSMC-1010, 14:50-54; *see* TSMC-1010, Figures 8I, 14-15, 14:55-56; TSMC-1003, ¶149.) Murthy's epitaxial region 531/532 (yellow below) is an "*epitaxial structure.*" Because Kelly's Figure 7C FinFET includes multiple epitaxial source/drain structures, the combination includes "*at least two epitaxial structures*" [1C]. (TSMC-1003, ¶149.)



Murthy, Figure 12 (left), Figure 8H (right)

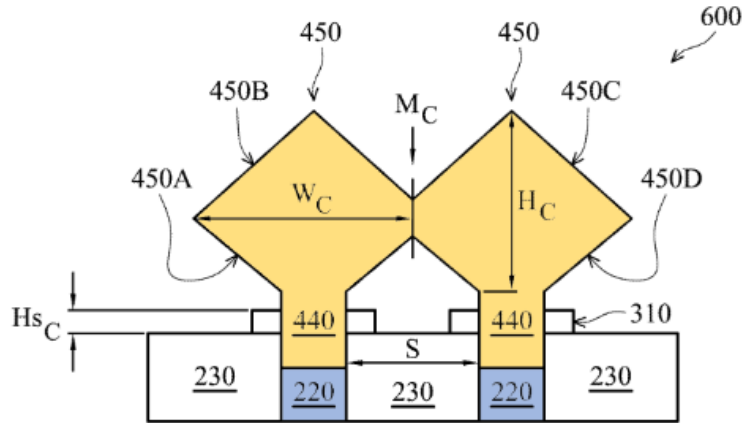
Murthy's epitaxial regions 531/532 are "deposited over each of the recessed source and drain interfaces 266, 268" as discussed above. (*See* TSMC-1009, 4:63-64; TSMC-1010, 10:17-20, Figures 8H, 12). Accordingly, the second combination discloses the epitaxial structures are "*disposed at one side of the gate structure and respectively directly contacting each fin-shaped structure*" [1C]. (TSMC-1003, ¶150.)

As taught by Murthy, cap layers 541/542 “are selectively deposited over the epitaxial regions 531, 532 in a sing[l]e deposition process.” (TSMC-1010, 15:17-20, Figures 8I, 14-15, 15:25-26 (“crystalline surfaces of the epitaxial regions 531, 532 allow epitaxial growth of cap layers 541, 542 thereon”).) Murthy’s caps 541/542 surround epitaxial regions 531/532 and therefore, cap 541/542 of each source/drain structure shown in Kelly’s Figure 7C (“*at least two caps*”) “*surround[] the epitaxial structures.*” (TSMC-1003, ¶151.)



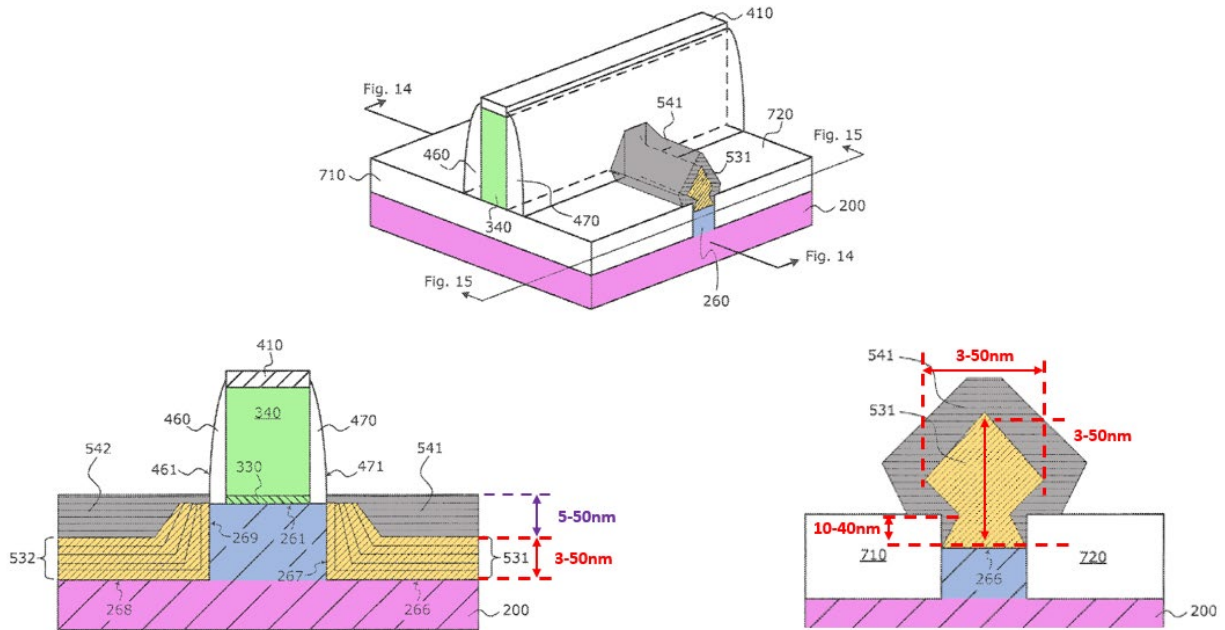
Murthy, Figure 8I (top), Figure 14 (bottom-left), Figure 15 (bottom-right)

As discussed above, Kelly tunes the merging distance of its epitaxial structures. (TSMC-1009, 6:46-50). In Kelly’s Figure 7C embodiment, “M has a value from zero to a negative value.” (TSMC-1009, 6:3-5.)



Kelly, Figure 7C

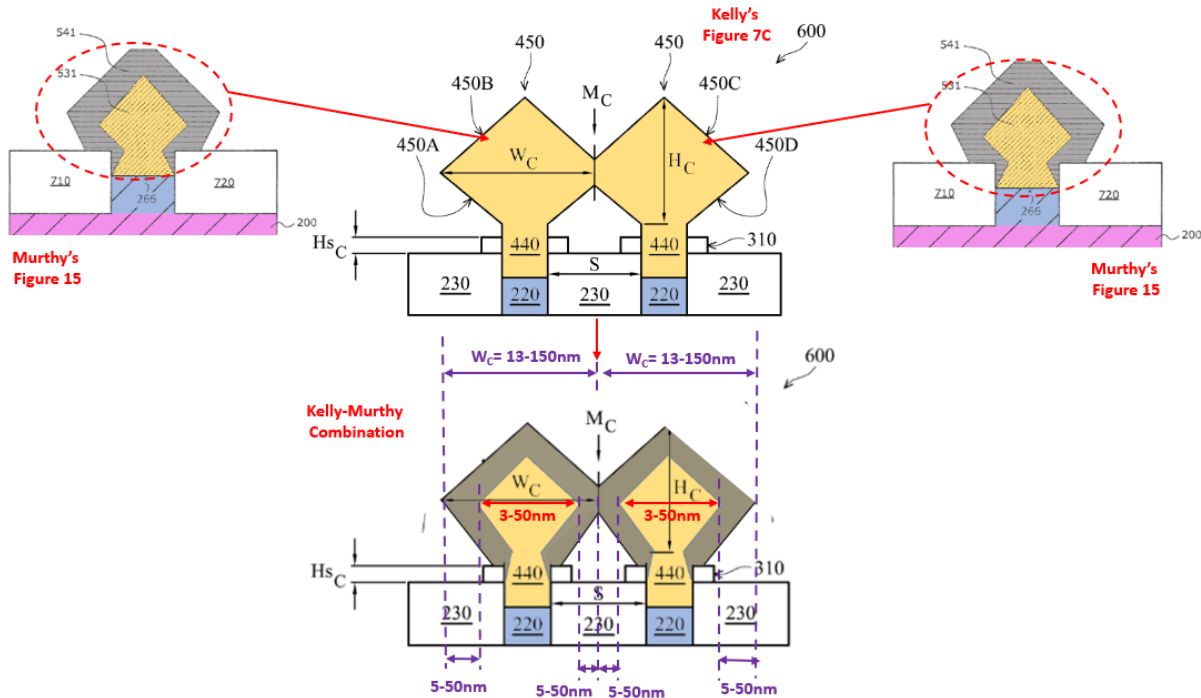
When forming source/drain structures 450 in the second combination, “epitaxial films 511, 512 are grown to have a thickness of about 6 to 100 Angstroms” and cap layers “are grown to have a thickness of about 50 to 500 Angstroms.” (TSMC-1010 (Murthy), 6:36-37, 9:3-4.) Therefore, in the embodiment having 5 epitaxial film layers shown in Figures 12, 14 and 15 of Murthy, the epitaxial region 531/532 has a thickness of 30 to 500 Angstroms (3nm to 50nm). (TSMC-1003, ¶153.)



Murthy, Figures 8I (top), 14 (bottom-left), 15 (bottom-right)

Based on these disclosures, a POSITA would have understood the total width and height of each source/drain structure 450 in the second combination device accounts for the thickness of Murthy's epitaxial regions 531/532 **and** cap layer 541/542, as highlighted in the figures below depicting an exemplary combination. (TSMC-1003, ¶154.) In this second combination, when M has a zero value (as shown in Kelly's Figure 7C) and the thickness of Murthy's cap layer (grey in Murthy's Figure 8I) is between 50 and 500 Angstroms (5nm -50nm) over the epitaxial regions which have a thickness of 30 to 500 Angstroms (3nm-50nm), the cap layers of adjacent source/drain structures in the second Kelly-Murthy combination merge and their associated epitaxial regions ("*epitaxial structures*")

do not touch (i.e., are spaced apart from each other). (TSMC-1003, ¶154; TSMC-1026, 13 (exemplary fin spacing of 60nm).)



Second Kelly-Murthy Combination

The second Kelly-Murthy combination therefore renders obvious “*the epitaxial structures are spaced apart from each other*” [1C] and “*at least two adjacent caps are merged together*” [1D]. (TSMC-1003, ¶¶148-155.)

C. Dependent Claims

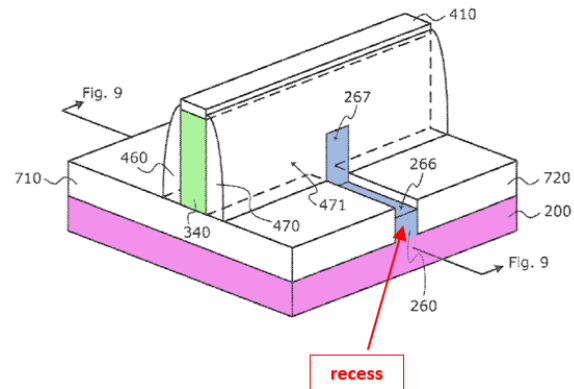
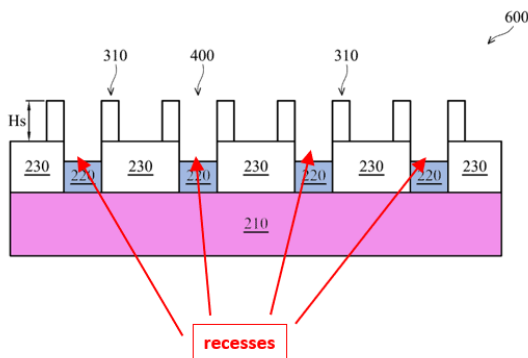
1. Claims 2-3

The first and second Kelly-Murthy combinations each discloses “*at least two recesses, respectively disposed at an end of each of the fin-shaped structures,*

wherein each of the epitaxial structures respectively fills up each of the recesses”

[2]. (TSMC-1003, ¶¶156-161.)

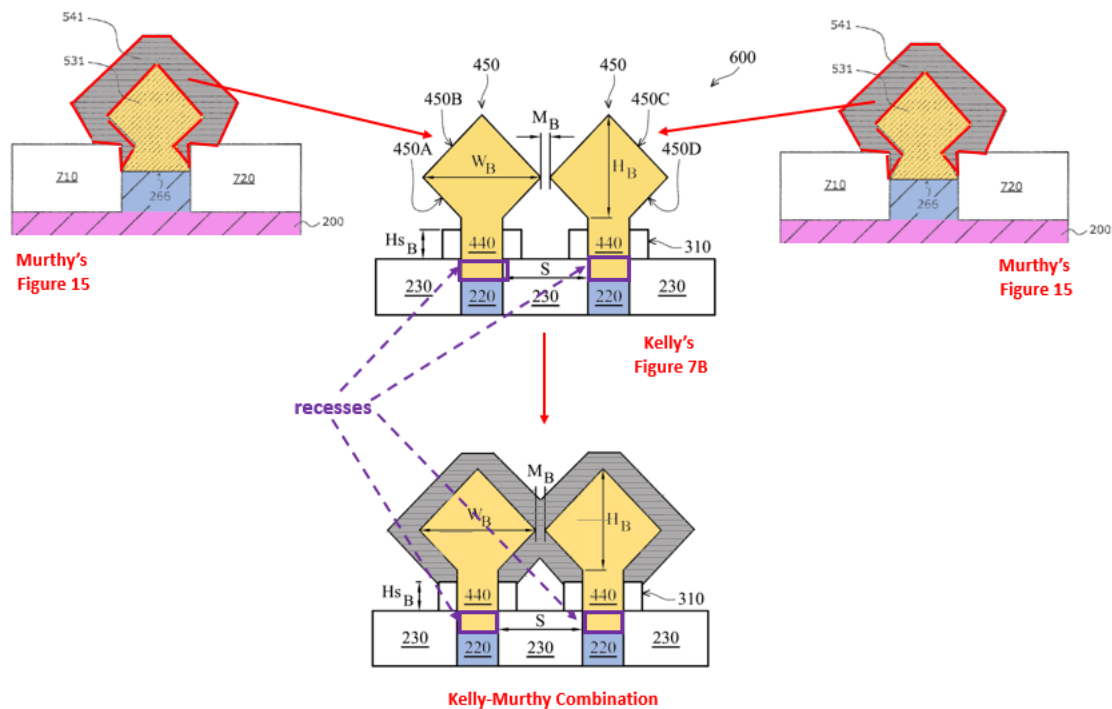
As discussed in §VII.B.3, in both combinations, Kelly’s source/drain structures 450 are formed by first “recessing fins 220 to form a recessing trench.” (TSMC-1009, 4:63-64, Figure 5A; TSMC-1010, 13:52-53 (“Next, an etching is performed on the substrate 200 to **recess the exposed portions 264, 265 of the fin 260**”), Figure 8E.) Thus, the device of each combination has “*at least two recesses.*” (TSMC-1003, ¶157.)



Kelly, Figure 5B (left); Murthy, Figure 8E (right)

Because the recesses are formed by etching the fin-shaped structures adjacent to the gate (in the source/drain regions), the recesses are “*disposed at an end of each of the fin-shaped structures.*” (TSMC-1003, ¶158; compare TSMC-1010, Figure 8E, with TSMC-1001, Figure 4.)

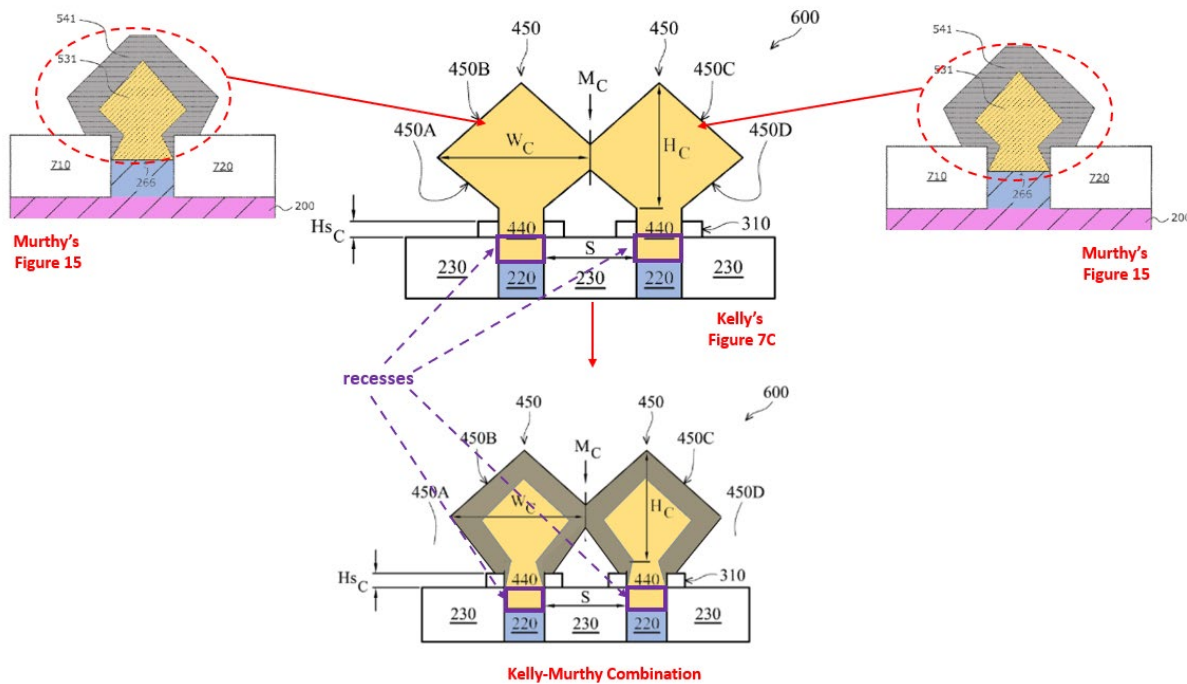
As discussed in §VII.B.3.a, in the first combination, epitaxial region 450 is formed “on the recessed fins 220 in the recessing trench 400.” (TSMC-1009, 5:42-45.) Thus, the “*epitaxial structures*” fill the recesses. (TSMC-1003, ¶159.)



First Kelly-Murthy Combination

As discussed in §VII.B.3.b, in the second combination, epitaxial regions 531/532 are “deposited over each of the recessed source and drain interfaces 266,

268⁸” as taught by Murthy. (TSMC-1010, 14:19-22.) Thus, the “*epitaxial structures*” of the second combination also fill the recesses. (TSMC-1003, ¶160.)



Second Kelly-Murthy Combination

Accordingly, the first and second combinations each renders claim 2 obvious.

Kelly's structures 450 (in the combination of Kelly's Figure 7B and Murthy) and Murthy's epitaxial regions 531/532 (in the combination of Kelly's Figure 7C and Murthy) are formed in the recesses on top of the fins. (TSMC-1009 (Kelly),

⁸ Element 268 is not shown in Murthy's figures. However, a POSITA would have understood that interface 268 is opposite interface 266 with respect to the gate (i.e., behind the gate in Figure 8E).

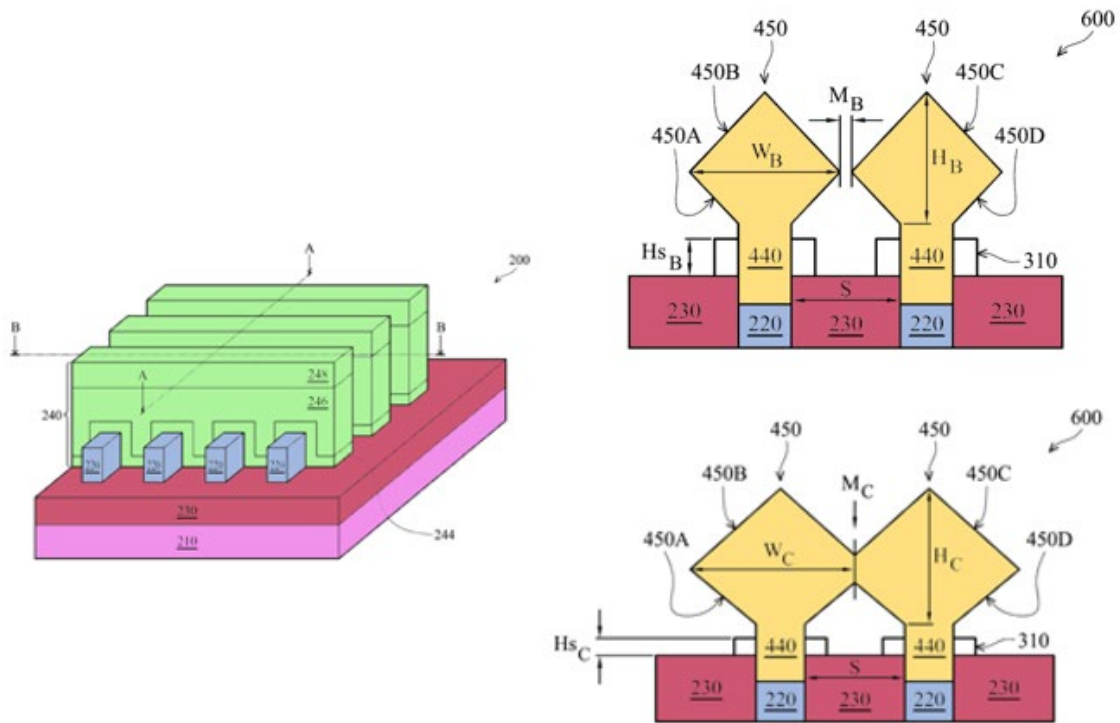
5:42-45; TSMC-1010 (Murthy), 14:19-54 (describing deposition-etch process to form epitaxial structures).) Thus, as shown in the figures above, the first and second combination each discloses “*the epitaxial structures respectively cover an end of each of the fin-shaped structures*” [3].

2. Claim 4

The first and second combinations each discloses “*at least an insulating layer, disposed between the epitaxial structures*” [4]. (TSMC-1003, ¶¶163-XX.)

In Kelly’s Figures 7B device and Figure 7C device, “[i]solation regions 230 [red] are formed on the substrate 210 to isolate active regions of the substrate 210, and may be further used to separate the fins 220.” (TSMC-1009, 3:28-30, Figures 2, 7B-7C (below).) Isolation region 230 “comprises silicon oxide, silicon nitride, silicon oxynitride, an air gap, other suitable materials, or combinations thereof.” (TSMC-1009, 3:33-35.) Isolation regions 230 are therefore “*an insulating layer.*”

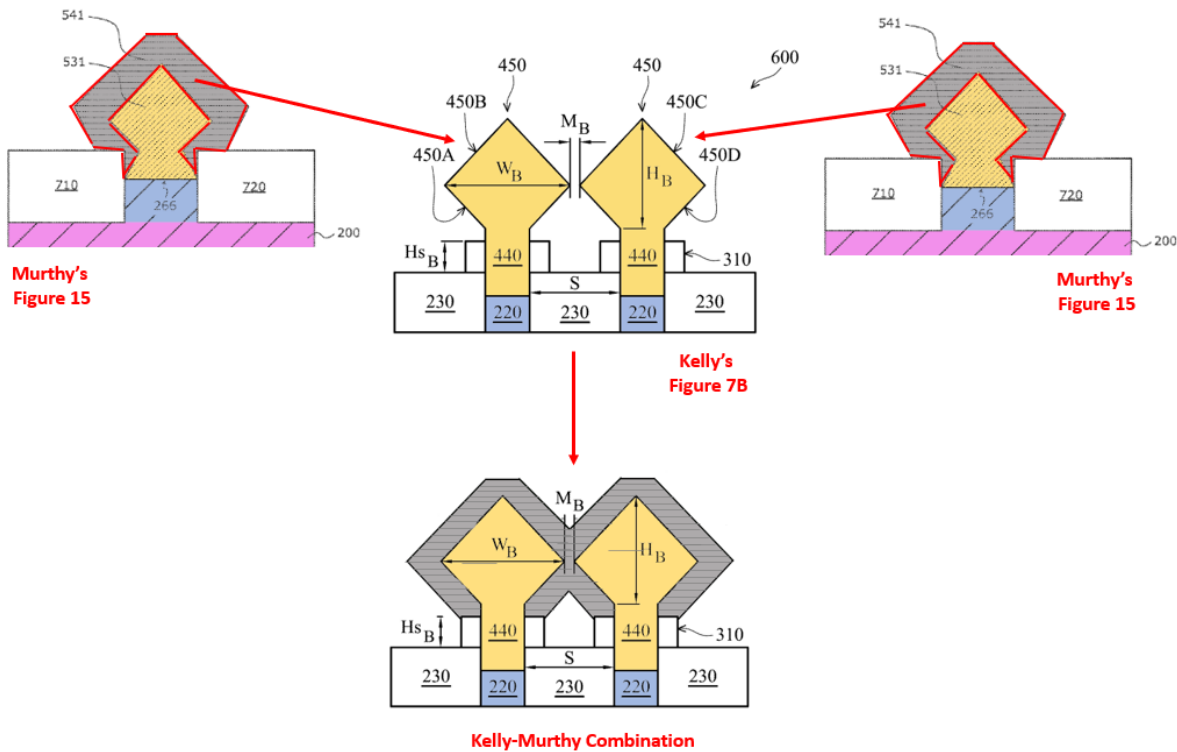
(TSMC-1003, ¶164.)



Kelly, Figures 2 (left), 7B, 7C (right)

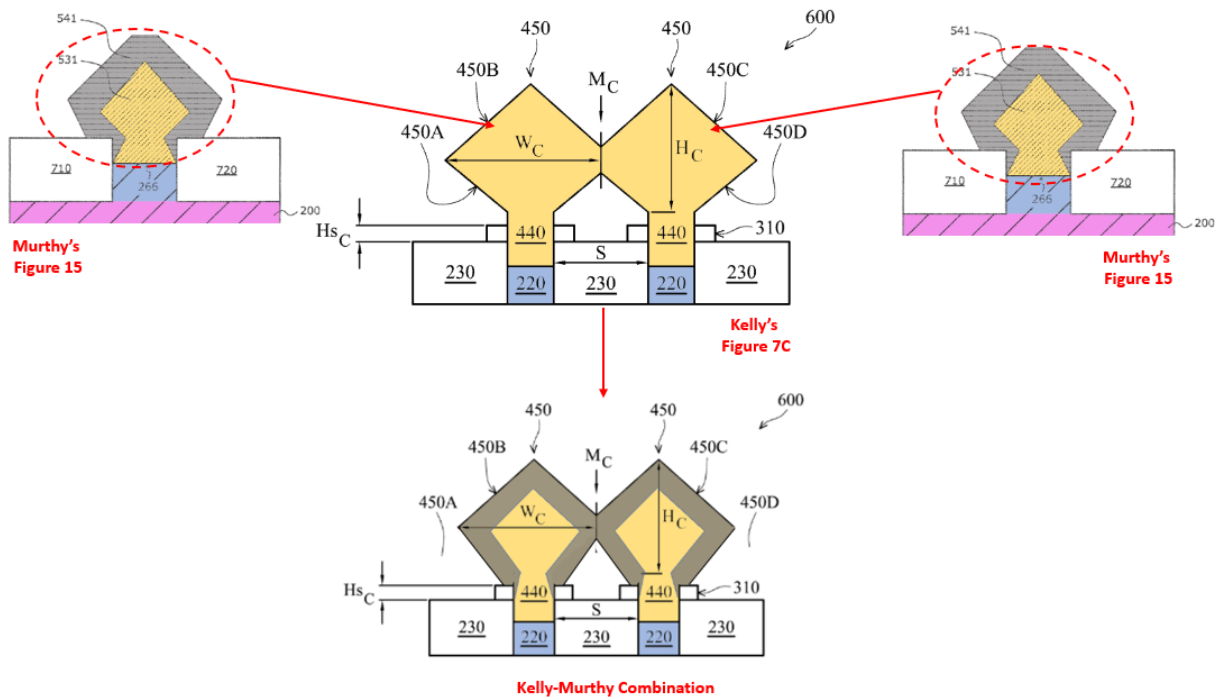
Kelly’s source/drain structures 450 in both combinations are formed by first “recessing fins 220 to form a recessing trench” (TSMC-1009, 4:63-64), such that the top of the recessed fin is lower than the surrounding isolation regions 230, which “may be further used to separate the fins 220.” (TSMC-1009, 3:29-31, 4:63-64, Figures 2, 7B-7C; *Unified Pats.*, 2022 WL 500391, *17.)

As discussed in §VII.C.1 for claim 2 and shown below, in the first combination, epitaxial structures 450 “fill[] up each of the recesses.”



First Kelly-Murthy Combination

Then, as discussed in §VII.C.1 for claim 2 and shown below, in the second combination, epitaxial regions 531/532 of source/drain structures 450 “fill[] up each of the recesses.”



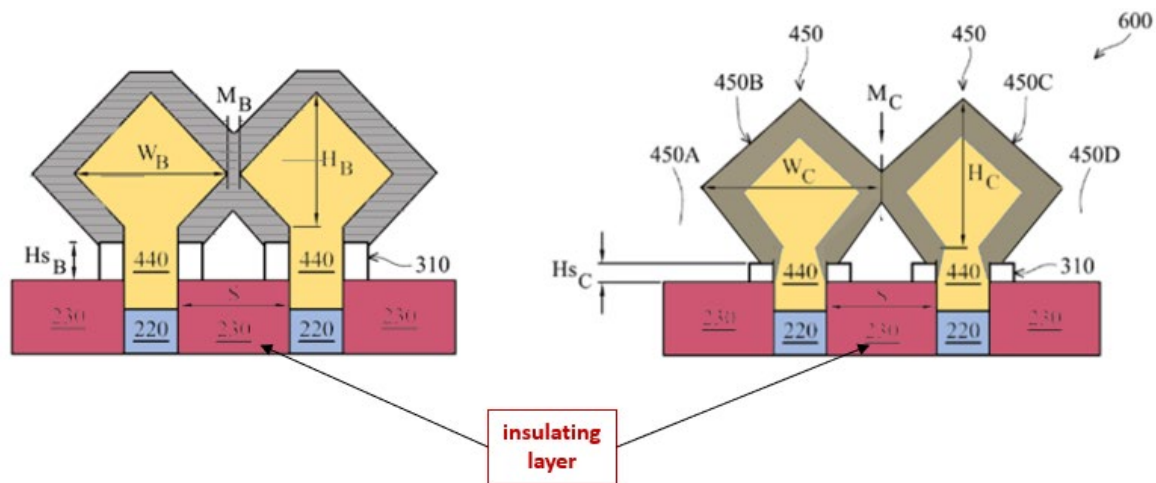
Second Kelly-Murthy Combination

As a result, the first and second combinations each discloses “*at least an insulating layer between the epitaxial structures*” [4]. (TSMC-1003, ¶167.)

3. Claim 5

The first and second Kelly-Murthy combination each discloses “*the caps directly cover the insulating layer between the epitaxial structures*” [5]. (TSMC-1003, ¶168.) As discussed in §§VII.A.3, B.3, Murthy’s caps 541/542 (“*caps*”) surrounding the “*epitaxial structures*” (epitaxial structures 450 in the first Kelly-Murthy combination; epitaxial regions 531/532 in the second Kelly-Murthy combination) “*are merged together.*” As a result, the merged “[adjacent] *caps directly cover the insulating layer between the epitaxial structure.*” (TSMC-1003,

¶168; TSMC-1027 (defining cover as “something that protects, shelters, or guards; something that is placed over or about another thing; something that conceals or obscures”).) The covering of the isolation regions 230 (“*insulating layer*”) in each Kelly-Murthy combination is illustrated below. As shown, since the “*adjacent caps*” merge, the resulting surface of the merged caps directly covers the underlying isolation regions 230. (TSMC-1003, ¶168.)



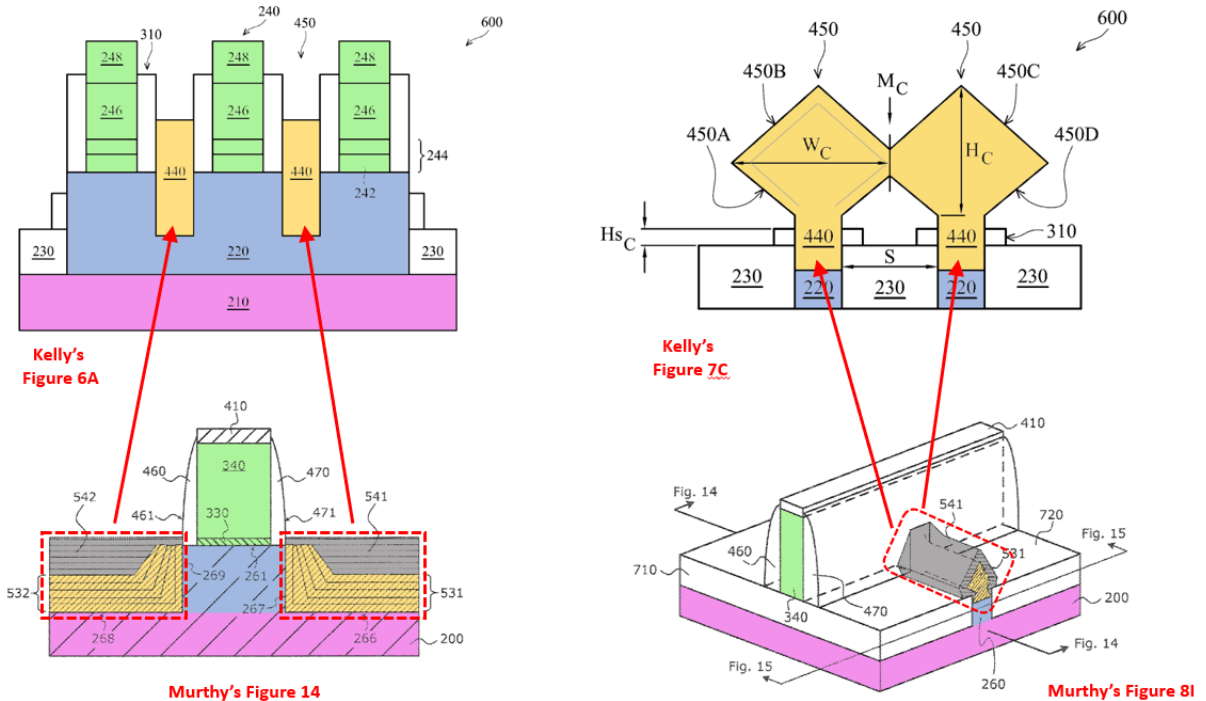
First Combination (left); Second Combination (Right)

Should PO contend “*directly cover*” requires direct contact between the “*cap*” and “*insulating layer*”, the claim does not support such a narrowing, as discussed in §V.C.3.

4. Claim 6

The second Kelly-Murthy combination renders obvious “*each of the epitaxial structures comprises a low doped epitaxial layer, a high doped epitaxial*

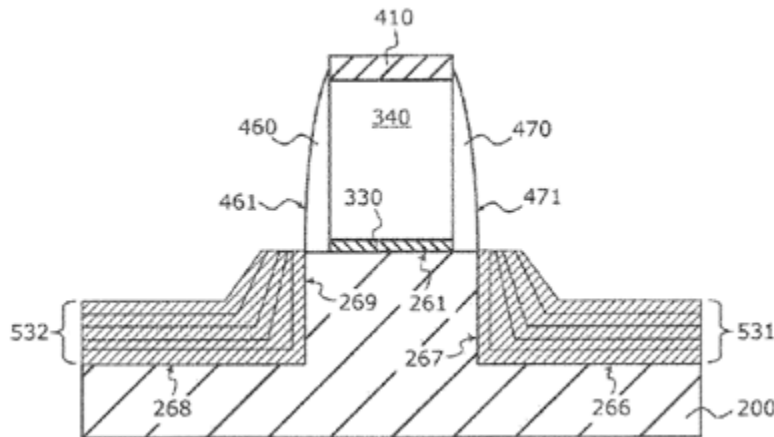
layer and a liner” [6], to the extent disclosed in the ’193 patent. (TSMC-1003, ¶¶170-174; §VI.B.) As discussed in §VII.A.3 and illustrated below, the second combination uses Murthy’s multi-layer epitaxial regions 531/532 (the “*epitaxial structures*”) as part of Kelly’s source/drain regions (structures 450).



**Kelly, Figures 6A (top-left), 7C (top-right);
Murthy, Figures 14 (bottom-left), 8I (bottom-right)**

Murthy discloses that, in preparation for the epitaxial growth, “[a]n optional surface pre-treatment can be performed on the substrate 200 before exposing it to the first precursor to facilitate epitaxial growth and reduce surface defects.” (TSMC-1010, 6:45-47.) The pre-treatment includes a hydrogen bake treatment that “desorbs oxygen and renders surface reconstruction so that the epitaxial films 511,

epitaxial regions 531/532 are deposited by “a graded concentration of carbon or phosphorus.” (TSMC-1010, 14:56-59.)



Murthy, Figure 12 (cross-sectional view)

In a first example, Murthy’s epitaxial regions 531/532 “are deposited with a graded **carbon concentration** of around 0.5 atomic % for the lowest epitaxial film and are gradually increased to a desired level of about 2 atomic % for the uppermost epitaxial film.” (TSMC-1010, 24:60-64.) Accordingly, the lowest epitaxial film in epitaxial regions 531/532 (e.g., epitaxial film directly above the first epitaxial layers 511/512) is a “*low doped epitaxial layer*” [6A] with a low carbon concentration and the uppermost epitaxial film in epitaxial regions 531/532 is a “*high doped epitaxial layer*” [6B] with a high carbon concentration. (TSMC-1003, ¶173.)

In an alternate example, Murthy discloses epitaxial regions 531/532 “are deposited with a graded phosphorus concentration level of around $8\text{E}19\text{ cm}^{-3}$ for

the lowest epitaxial film and are gradually increased to a desired level of around $2E21\text{ cm}^{-3}$ for the uppermost epitaxial film.” (TSMC-1010, 14:64-15:1.)

Accordingly, the lowest epitaxial film in epitaxial regions 531/532 (e.g., epitaxial film directly above the first epitaxial layers 511/512) is a “*low doped epitaxial layer*” [6A] with low phosphorus levels, and the uppermost epitaxial film in epitaxial regions 531/532 is a “*high doped epitaxial layer*” [6B] with high phosphorus levels. (TSMC-1003, ¶174.)

5. Claim 7

In the first Kelly-Murthy combination, Kelly’s epitaxial structures 450 are made of “semiconductor alloy, such as **silicon germanium (SiGe)**.” (TSMC-1009, 5:25-31.)

In the second Kelly-Murthy combination, Murthy’s epitaxial regions 531/532 (“*epitaxial structures*”) “comprise silicon and carbon doped with phosphorus.” (TSMC-1010, 3:17-19.) In one embodiment, “the epitaxial regions 531, 532 comprise silicon having a carbon concentration of 2.2 atomic % and a phosphorus concentration of $2E20\text{ cm}^{-3}$.” (TSMC-1010, 3:25-27.) The substitutional carbon (over 2 atomic %) in this composition “impart[s] hydrostatic stress on the channel region, which enhances electron mobility” and “suppresses any phosphorus diffusion during any subsequent thermal anneals, thus reducing short channel effects.” (TSMC-1010, 3:27-33.) A POSITA would understand this

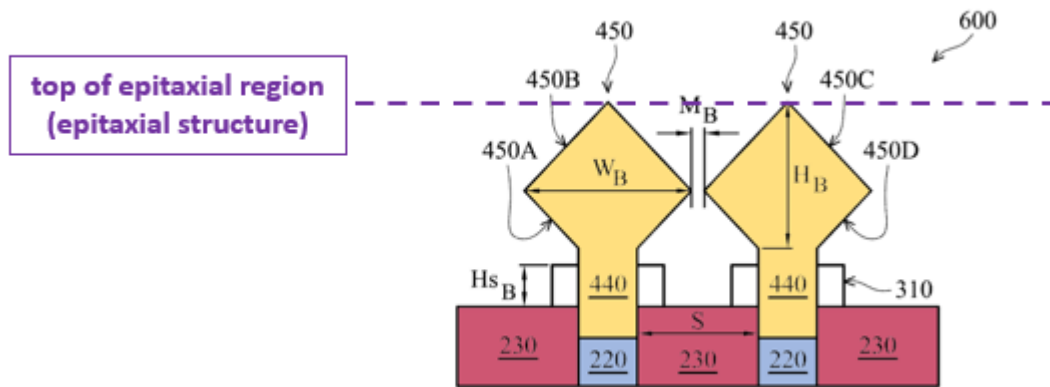
composition to be phosphorus-doped silicon carbide (SiC), consistent with the disclosures of the '193 patent. (TSMC-1003, ¶¶177-178; TSMC-1028, S184 (noting that “[p]hosphorous should ... be the dopant of choice for SiC strained NMOS transistors” because, as recognized in Murthy, “P diffusion is suppressed in the presence of substitutional carbon”); TSMC-1001, 1:44 (identifying “carbon-doped silicon” as “SiC”); 5:59-63 (composition of epitaxial structure may include “phosphorous-doped silicon carbide”).)

The first and second Kelly-Murthy combinations each renders obvious “*a composition of each of the epitaxial structures comprises silicon germanium, silicon phosphide or silicon carbide.*” (TSMC-1003, ¶179.)

6. Claim 8

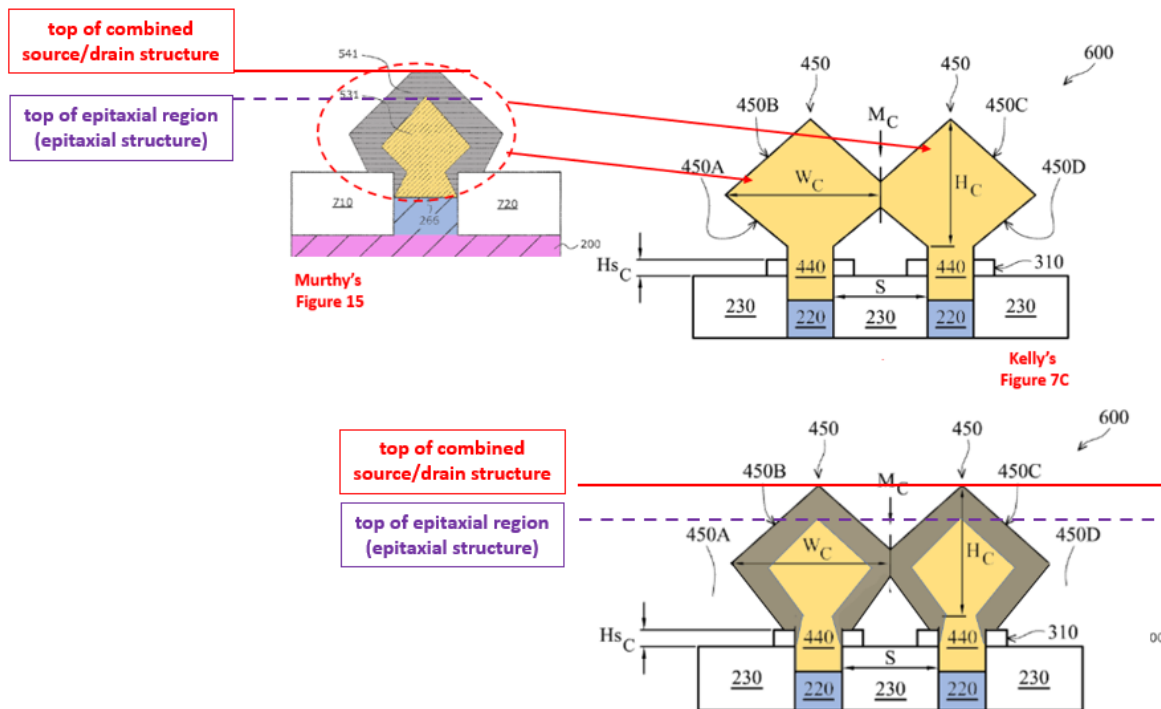
The first and second Kelly-Murthy combination each renders obvious “*each of the epitaxial structures comprises a top portion and the top portions are substantially in the same plane*” [8], consistent with the disclosure in the '193 patent. (TSMC-1001, 6:15-17, Figure 3; §V.C.5; TSMC-1003, ¶¶180-183.)

In the first combination, the height of each epitaxial structure 450 (“*epitaxial structure*”) is H_B and therefore the “*top portions are substantially in the same plane.*” (TSMC-1009, Figure 7B.)



Kelly, Figure 7B

In the second combination, source/drain structure 450 of Figure 7C includes epitaxial region 531/532 (“*epitaxial structure*”) and cap 541/542 (“*cap*”). The height of epitaxial region 531/532 is therefore H_C minus the thickness of Murthy’s cap 541/542. (TSMC-1003, ¶182.) Because the cap is conformally formed on the structures (e.g., as shown in Figure 8I of Murthy) and merged with adjacent caps, each of the “*epitaxial structures*” in structures 450 has the same height and therefore the “*top portions are substantially in the same plane.*” (TSMC-1003, ¶¶182-183.)

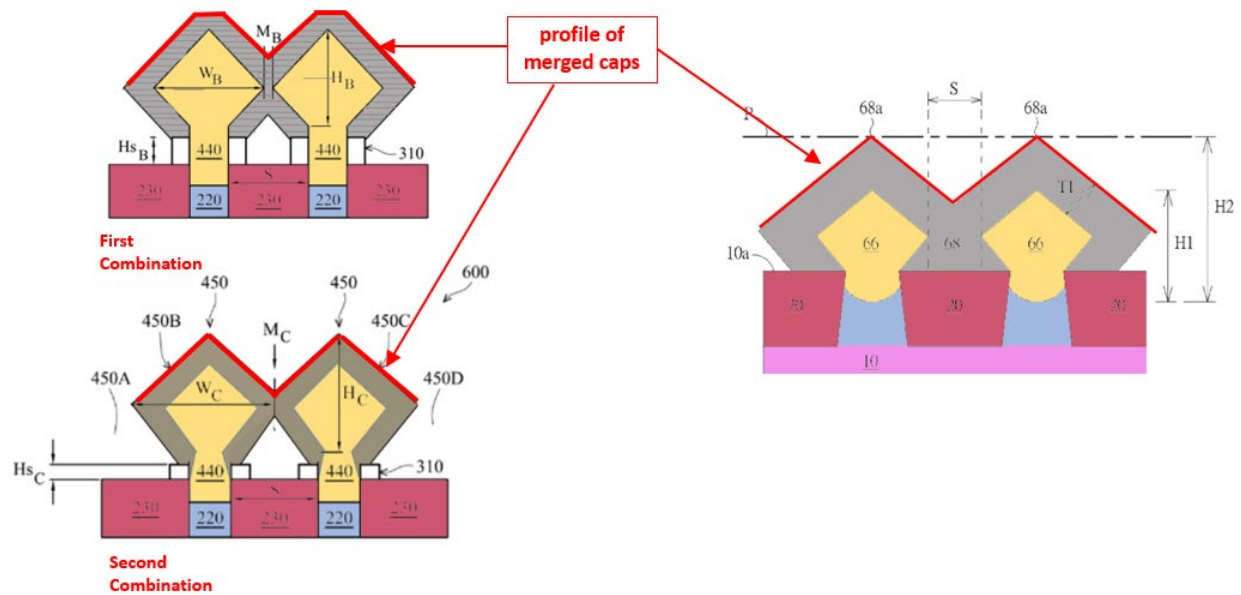


Second Kelly-Murthy Combination

7. Claim 9

The first and second Kelly-Murthy combinations each discloses “*the caps have a concavo-convex profile*” [9]. (TSMC-1003, ¶184.) Merged caps 541/542 have an approximately periodic concavo-convex profile, consistent with the ’193 patent’s disclosure, as shown in the side-by-side comparison of exemplary

combinations of Kelly-Murthy and '193 patent-Figure 7. (*Id.*)



Kelly-Murthy Combinations (left); '193 Patent, Figure 7 (right)

8. Claim 10

The second Kelly-Murthy combination renders obvious the “*caps are made of monocrystalline silicon*” [10]. (TSMC-1003, ¶¶185-188.) As discussed in §VII.B.3, the source/drain structures 450 of the second combination FinFET each include Murthy’s epitaxial region and cap.

Kelly's substrate 210 "may be a bulk silicon substrate" or alternatively, "may comprise an elementary semiconductor, such as silicon or germanium in a crystalline structure." (TSMC-1009, 2:32-36.) Murthy's substrate "is made of monocrystalline silicon." (TSMC-1010, 5:58-59.) Further, Kelly's fins 220 are "formed by patterning and etching a portion of the silicon substrate 210." (TSMC-

1009, 3:11-12.) Thus, the fins are the same material as the substrate, monocrystalline silicon. (TSMC-1003, ¶186.) Accordingly, “the recessed source and drain interfaces 220, 230 are monocrystalline surfaces that allow epitaxial growth of the epitaxial films 511, 512 thereon.” (TSMC-1010, 5:58-62.)

Murthy teaches the “crystalline surface of the epitaxial layers 531, 532 allow epitaxial growth of cap layers 541, 542 thereon.” (TSMC-1010, 6:45-47.) And because “the deposited epitaxial films 511, 512 are **crystalline** films containing silicon and carbon doped with phosphorus (i.e. in-situ carbon and phosphorus doped silicon layer)” (TSMC-1010, 6:40-43), a POSITA would have understood epitaxial films 511/512, which are grown through another **epitaxial** process on a monocrystalline surface, inherit the monocrystalline orientation of the underlying surface (i.e., source and drain interfaces 220, 230). (TSMC-1003, ¶187.) The “crystalline surfaces of the epitaxial layers 531, 532 allow **epitaxial** growth of cap layers 541, 542 thereon, and as a result, **the cap layers 541, 542 are epitaxial layers containing silicon doped with phosphorus.**” (TSMC-1010: 11:18-25.) For at least the same reasons epitaxial films 511/512 inherit the monocrystalline orientation of source and drain interfaces 220/230, additional epitaxial films 511/512 in epitaxial structure 531/532 and cap layers 541/542 **also** inherit the monocrystalline orientation of source and drain interfaces 220/230. (TSMC-1003, ¶187.)

Accordingly, the second combination renders obvious “*wherein the caps are made of monocrystalline silicon*” [10]. (TSMC-1003, ¶¶185-188.)

VIII. GROUND 4: Kelly-Murthy-Liaw Combination Renders Claim 11 Obvious.

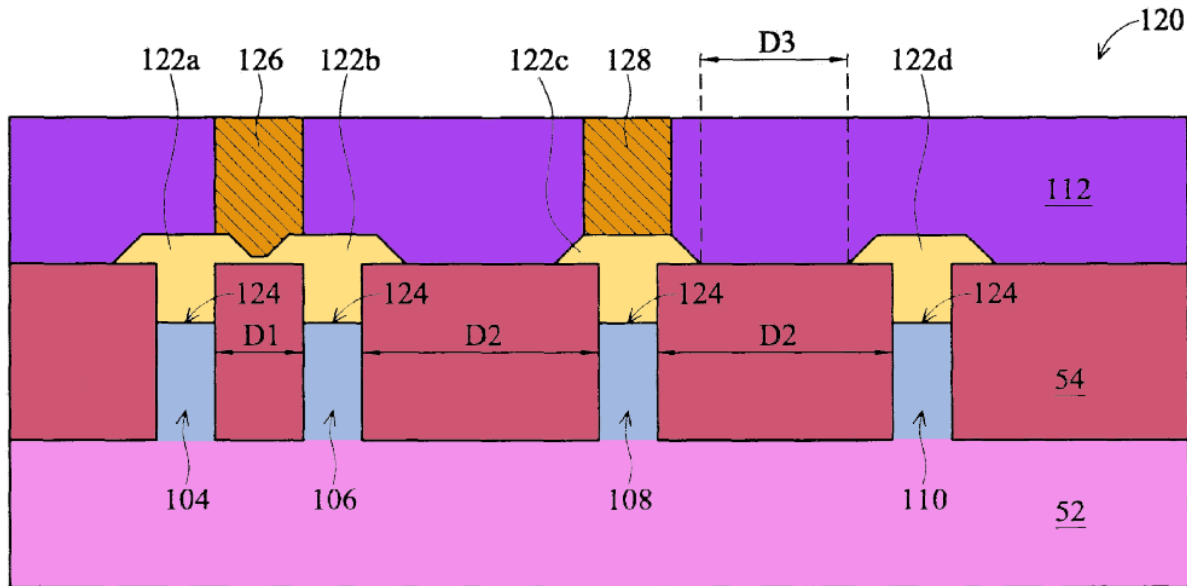
Each Kelly-Murthy combination fails to explicitly disclose claim 11. These features are disclosed by Liaw.

A. Liaw Overview

Liaw’s FinFET includes substrate 52 (pink) and isolation features 54 (e.g., STI regions, red). (TSMC-1008, 7:14-16, 3:25-27, Figure 4 (below).) The FinFET further includes “various fin active regions 104, 106, 108 and 110” having “a first portion [blue] extended from the semiconductor substrate 52 and a second portion formed on the first portion as epitaxy features 122 [yellow].” (TSMC-1008, 7:16-21.) Liaw explains “[w]hen the epitaxy features 122 are formed on the respective fin active regions, lateral epitaxy growth will enlarge the dimension of the fin active regions and narrow the spacing.” (TSMC-1008, 7:55-58.) For fin active regions with the first spacing, D1⁹, “the respective epitaxy features have a narrow

⁹ Liaw contains a typographical error referring to the first spacing as D2 rather than D1. (See TSMC-1008, 7:62-65.) A POSITA would understand based on Liaw’s disclosure the first spacing is the narrow spacing labeled D1 in Figure 4. (TSMC-1003, ¶189, n.18.)

spacing or are even laterally merged (bridged) together” to “form a continuous landing feature.” (TSMC-1008, 7:62-67.)



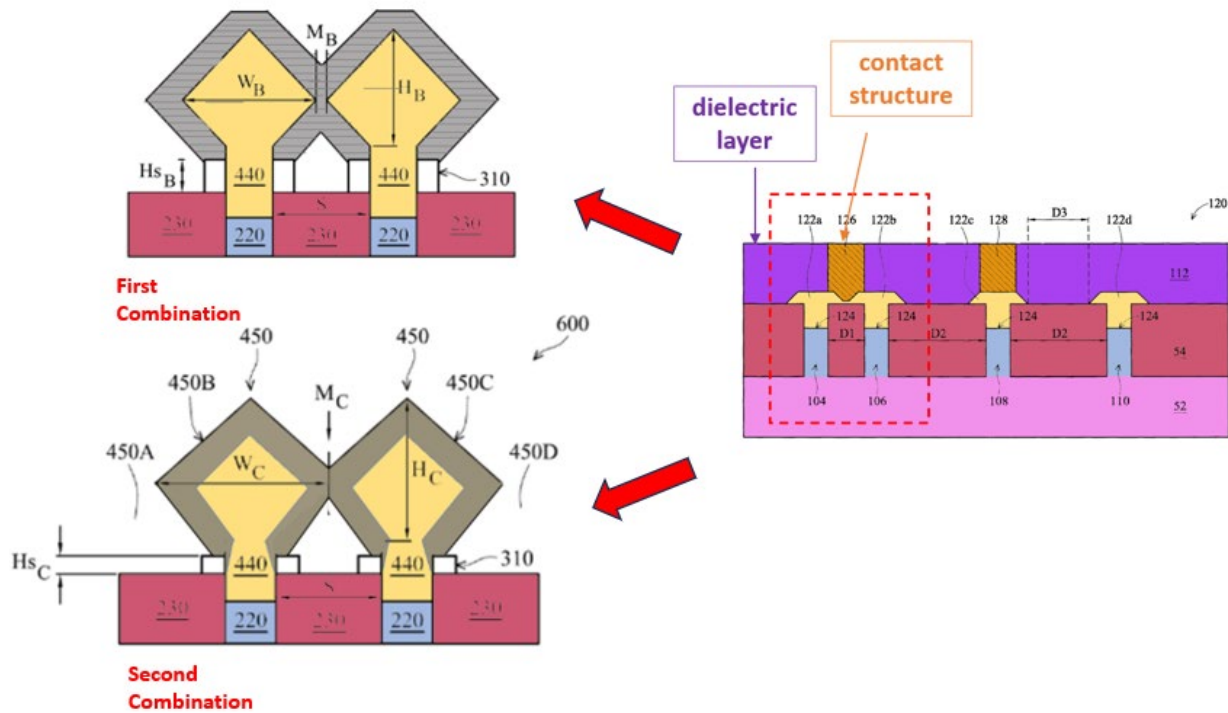
Liaw, Figure 4

Liaw’s device further “includes an interlayer dielectric (ILD) 112 disposed on the fin active regions and the isolation features.” (TSMC-1008, 8:5-7.) Contacts 126, 128 (orange) are “formed in the ILD 112 and configured to provide electrical routing.” (TSMC-1008, 8:10-12.) The contacts are formed by “forming contact holes in the ILD 112 and filling the contact hole with a conductive material.” (TSMC-1008, 8:25-28.)

B. Kelly-Murthy-Liaw Combinations

A POSITA would have been motivated to combine the teachings of Kelly and Murthy regarding a multi-fin device having merged epitaxially grown cap

structures of both the first and second combination with Liaw's teachings regarding the metallization features of a final device. (TSMC-1003, ¶191.) A POSITA would have understood that, in each Kelly-Murthy combination, (1) fins 220, (2) Kelly's structures 450 (in the first combination) or Murthy's epitaxial region 531/532 (in the second combination) ("*epitaxial structures*"), and (3) Murthy's cap 541/542 are collectively a "fin active region" as the term is used in Liaw. (*Id.*) A POSITA would have been motivated to include an interlayer dielectric on the fin active regions of each Kelly-Murthy combination, as taught by Liaw (Figure 4 (below-right)), "for providing isolation to interconnections [including the contacts "which are a portion of the multilayer interconnect for wiring"] formed thereafter." (TSMC-1008, 5:6-8, 5:26-27; TSMC-1003, ¶191.) A POSITA would have further been motivated to form a contact hole in the ILD and fill the contact hole with a conductive material, as taught by Liaw, to form the contacts "to electrically connect **sources, drains and gate electrodes** to metal lines." (TSMC-1008, 5:24-26; TSMC-1003, ¶191.)



Kelly-Murthy Combinations (left); Liaw, Figure 4 (right)

Thus, each Kelly-Murthy-Liaw combination provides “a dielectric layer, covering the gate structure and the cap” [11A], to the extent disclosed in the ’193 patent. (TSMC-1003, ¶192.) As discussed above, Liaw’s device “includes an **interlayer dielectric (ILD)** disposed on the fin active regions and the isolation features.” (TSMC-1008, 8:5-7.) In each Kelly-Murthy-Liaw combination, the ILD is also formed on the fin active regions (consisting of the fin, epitaxial regions 531/532 (“*epitaxial structure*”), and cap layers 541/542), isolation regions 230, and the gate electrode because the ILD formation, which “is providing isolation to interconnections” (including the contacts “which are a portion of the multilayer

interconnect for wiring” and “electrically connect **sources, drains and gate electrodes** to metal lines”), occurs after the epitaxy growth and the gate electrode formation, as taught by Liaw. (TSMC-1008, 5:24-27; TSMC-1003, ¶192.)

Each Kelly-Murthy-Liaw combination provides “*at least a contact structure, disposed in the dielectric layer and in direct contact with the caps*” [11B].

(TSMC-1003, ¶193.) Liaw discloses forming contacts in the ILD “to provide electrical routing,” which a POSITA would understand is necessary for a final, functional MOSFET device. (TSMC-1008, 8:10-12; TSMC-1003, ¶193.) As discussed above, a contact hole is formed in the ILD and filled “with a conductive material” (“*contact structure*”). (TSMC-1008, 8:25-28.) The contact “is configured to land on the merged epitaxy features 122a and 122b.” (TSMC-1008, 8:15-17.)

Kelly’s structures 450 with Murthy’s cap layers 541/542 (in the first combination) and Murthy’s epitaxial regions 531/532 and cap layers 541/542 (in the second combination) are equivalent to Liaw’s epitaxy feature 122. (TSMC-1003, ¶193.) A POSITA would therefore understand that, in the combination, the conductive material (“*contact structure*”) is in direct contact with the cap layer 541/542 because (1) it is the outermost layer of the structure 450 and (2) is part of the combined device’s fin active region (i.e., source/drain region) and therefore must be contacted to form the device’s source/drain contact. (*Id.*; *see also* TSMC-1007, ¶¶3, 24, claim 21 (“source/drain region [comprising] ... an extension of the

semiconductor fin; and an epitaxy layer on a top surface and sidewalls of the extension of the semiconductor fin”); TSMC-1005, 4:39-51 (describing a contact in contact with a cap).)

C. Motivation to Combine

A POSITA would have been motivated to combine the teachings of Kelly-Murthy and Liaw because Kelly explicitly suggests the combination. (TSMC-1003, ¶194.) Kelly discloses its FinFET device “may include additional features, which may be formed by subsequent processing” which include, e.g., “various contacts/vias/lines and multilayer interconnect features (e.g., metal layers and interlayer dielectrics) [] formed over the substrate, configured to connect the various features or structures of” the FinFET. (TSMC-1009, 6:35-40.) Kelly, however, does not disclose details regarding these contacts and interconnect features. Nor does Murthy. A POSITA would have been motivated to search for references disclosing this additional information and been led to Liaw, which is in the same field of endeavor as Kelly, Murthy, and the ’193 patent—FET semiconductor devices. (TSMC-1001, 1:15-17; TSMC-1009, 2:4-15; TSMC-1010, 1:8-10, 4:41-43; TSMC-1008, Abstract; *see also* TSMC-1003, ¶194; TSMC-1022, 401.)

A POSITA would further have been motivated to combine Kelly-Murthy and Liaw to provide the features necessary so the device operates as intended, as a

transistor in an integrated circuit. (TSMC-1009, 1:16-28.) Liaw teaches “contacts and other interconnect features” are needed “to electrically configure the FinFETs to functional circuits.” (TSMC-1008, 6:12-15.) Indeed, the desirability of using epitaxial growth to merge epitaxial layers on adjacent fins “[t]o eliminate the contact to fin pitch matching requirement” was already known before the ’193 patent. (TSMC-1003, ¶195; TSMC-1012, 100.) A POSITA would have therefore been motivated to search for a reference disclosing a technique to provide a contact on the merged caps on the epitaxial structures of the Kelly-Murthy combination (epitaxial regions 531/532 and cap layers 541/542) and been led to Liaw’s teaching which recognized a similar benefit and provided a contact for merged adjacent epitaxial layers. (TSMC-1008, 8:15-17.)

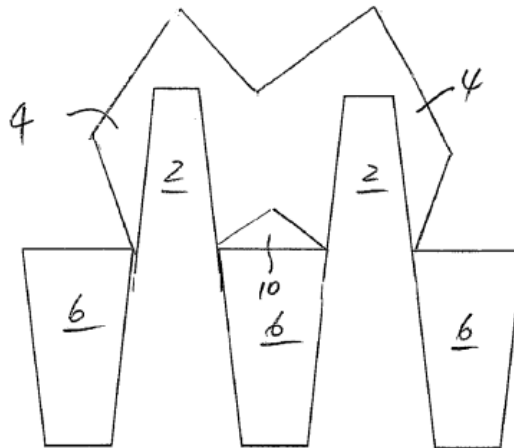
A POSITA would have further been motivated to combine Kelly-Murthy and Liaw because the combination merely combines known prior art elements (the FinFET device of the Kelly-Murthy combination with Liaw’s contact structure) according to known methods (metallization). (TSMC-1003, ¶196; *KSR*, 550 U.S. at 416-17.) The results of the combination would have been predictable, and a POSITA would have had a reasonable expectation of success in the combination. (TSMC-1003, ¶196.) A POSITA would have recognized the similarities between Liaw’s FinFET device and the Kelly-Murthy FinFET device and would have understood that Liaw’s contact formation process is applicable to the Kelly-Murthy

device. (*Id.*) Moreover, the process of metallization was well-known long before the '193 patent. (TSMC-1022, 401-434; TSMC-1012, 98-100; TSMC-1003, ¶196.)

IX. GROUND 5: Su Renders Claims 1, 7, 10 Obvious.

A. Su Overview

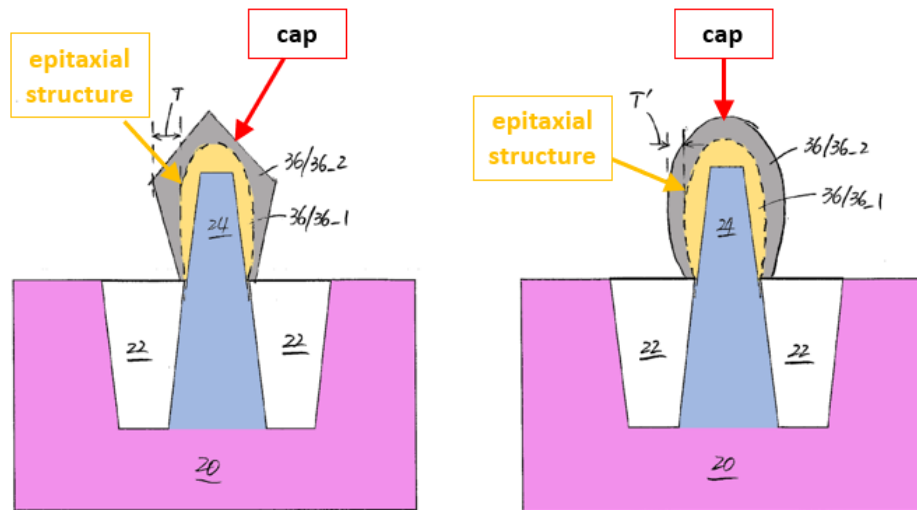
Su recognized existing epitaxial processes used to form multi-fin FinFETs “suffer from drawbacks.” (TSMC-1007, ¶4.) For example, a void is “undesirably generated as a result of the merging of epitaxy layers 4 grown from neighboring fins 2.” (*Id.*, Figure 2 (below).)



Su, Figure 2

Su therefore developed a method in which an epitaxy layer (layer 36_1), “is deposited, for example, epitaxially grown on the exposed portion of fin 24 by selective epitaxial growth (SEG).” (TSMC-1007, ¶¶17, 20.) The epitaxial growth is stopped and “an etch step is performed”, resulting in the structure having “an ellipse shape.” (TSMC-1007, ¶21.) In an embodiment, a second deposition-etch

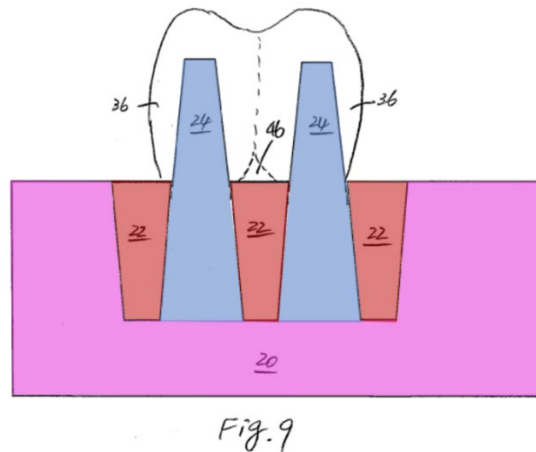
cycle is performed during which “epitaxy layer 36_2 is epitaxially grown on the remaining portion of epitaxy layer 36_1.” (TSMC-1007, ¶22, Figures 6-7 (below).)



Su, Figures 6 (left), 7 (right)

In Su’s method, “epitaxy layers 36 grown from neighboring fins 24 merge with each other to form a single epitaxy region.” (TSMC-1007, ¶25, Figure 8.)

According to Su, “due to the deposition-etch process, void 46 (if formed at all) caused by the merging of epitaxy layers 36 will be at least reduced, and possibly be eliminated.” (TSMC-1007, ¶25.)



Su, Figure 9

B. Independent Claim 1

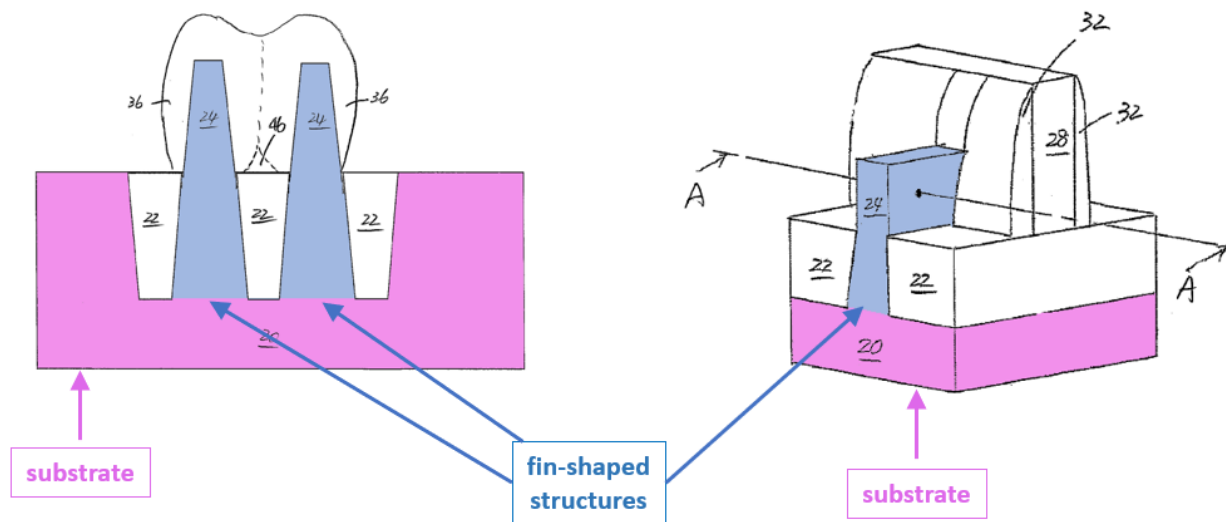
1. Preamble [1P]

Su discloses a “*semiconductor device*” [1P]. Su “relates generally to **semiconductor devices**, and more particularly to structures and formation methods of **semiconductor fins** and fin field-effect transistors (FinFETs).” (TSMC-1007, ¶1; *see also* TSMC-1007, Abstract, ¶13.)

2. Limitation [1A]

As shown in Figure 9 (below-left), “epitaxy layers 36 grown from **neighboring fins** [24] merge with each other.” (TSMC-1007, ¶25.) Su’s fin 24 “may be formed by removing top portions of STI regions 22, so that a portion of substrate 20 between neighboring STI regions 22 becomes a fin” or “fin 24 may be formed on top of substrate 20 by an epitaxial growth.” (TSMC-1007, ¶14, Figure 3 (below-right) (illustrating single-fin); *Google LLC v. Jenam Tech, LLC*, IPR2021-

00630, 2022 WL 4287797, *9 n.9 (P.T.A.B. Sept. 16, 2022) (applying same disclosures where “figures refer to corresponding features using the same reference numbers”).) Fins 24 in Su’s multi-fin FinFET are “two *fin-shaped structures* disposed on a substrate.” (TSMC-1003, ¶201.)

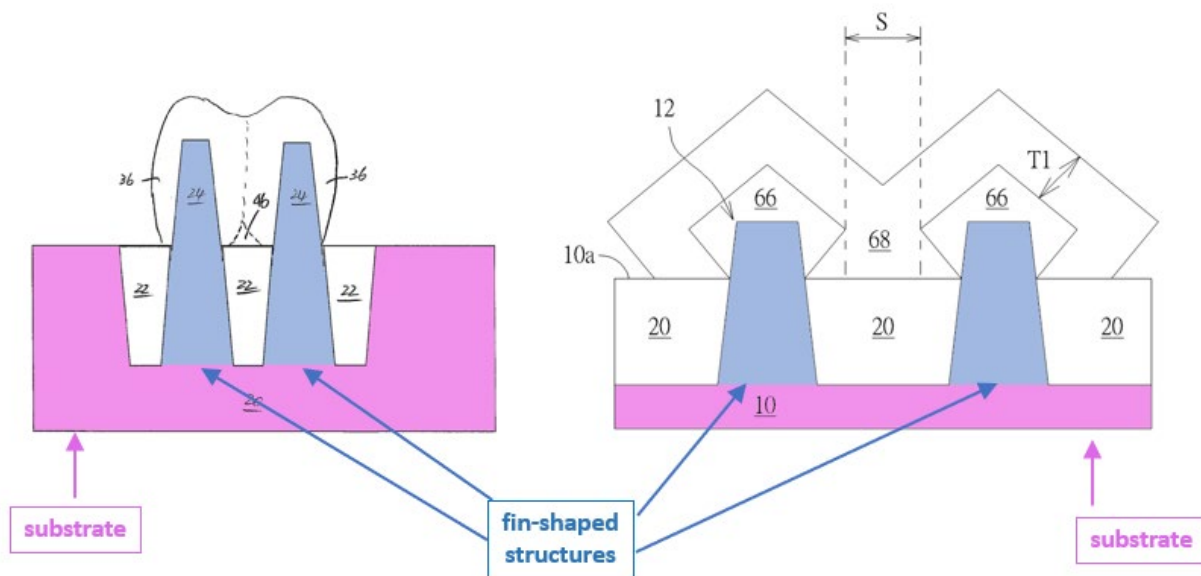


Su, Figures 9 (left), 3 (right)

Should PO argue the disclosures associated with Figures 3-8’s single-fin FinFET are directed to a different embodiment than Figure 9, it would have been obvious to a POSITA to combine the teachings of Figures 3-8 with Figure 9’s multi-fin FinFET because Su expressly suggests the combination. *Boston Sci. Scimed, Inc. v. Cordis Corp.*, 554 F. 3d 982, 991 (Fed. Cir. 2009) (“[c]ombining two embodiments disclosed adjacent to each other in a prior art patent does not require a leap of inventiveness”), TSMC-1003, ¶202. Su refers to elements of Figure 9 using the same label numbers as used in Figures 3-8, indicating the same

components are used. (TSMC-1003, ¶202.) Su also explicitly states its disclosure relates “to structures and formation methods of semiconductor fins [plural].” (TSMC-1007, ¶1.) And importantly, Su is directed to overcoming drawbacks of the epitaxial processes performed during the fabrication of multi-fin FinFETs. (TSMC-1007, ¶4, Figure 2.)

Su’s disclosure is consistent with the ’193 patent’s disclosure, as highlighted in the side-by-side figures below.

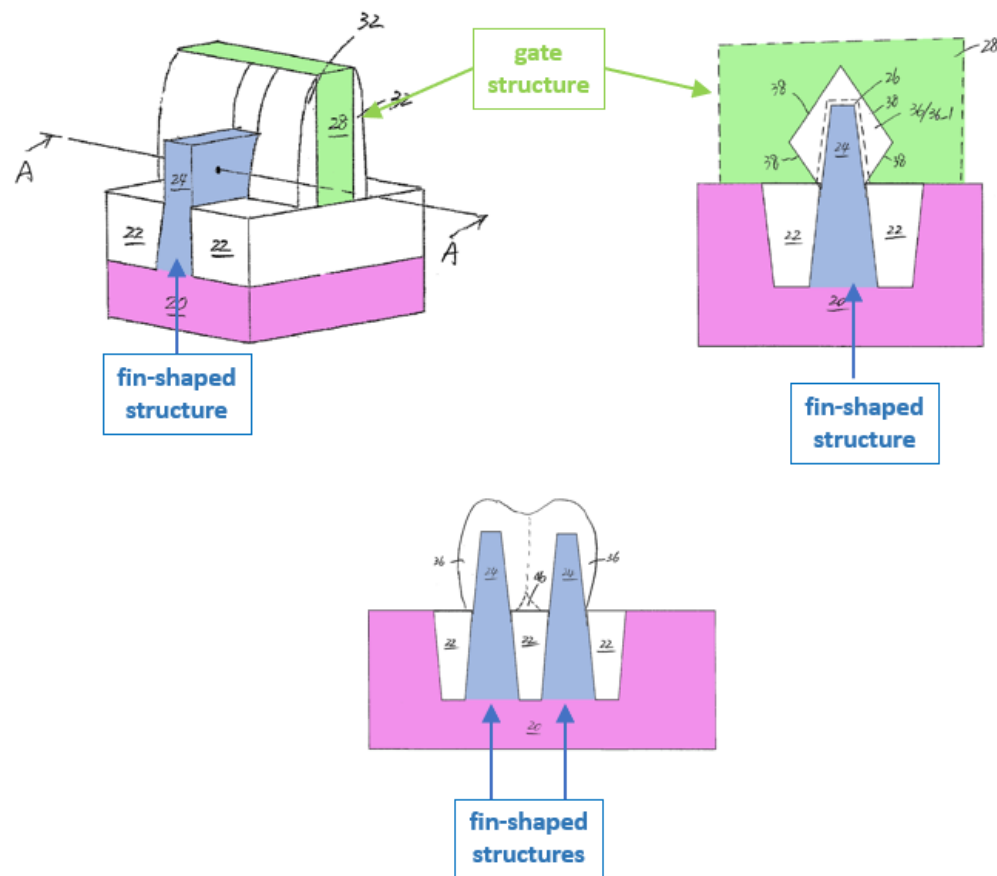


Su, Figure 9 (left); '193 Patent, Figure 11 (right)

3. Limitation [1B]

In Su’s device, gate dielectric 26 “is formed on the top surface and sidewalls of fin 24,” and “[g]ate electrode 28 is formed on gate dielectric 26.” (TSMC-1007, ¶15, Figure 3 (below/top-left), Figure 4A (below/top-right).) In Su, “[f]or

simplicity, in subsequent drawings, gate dielectric and gate electrode 28 are not illustrated” and therefore Figure 9 (below) does not show the gate outline included in Figure 4A. (TSMC-1007, ¶18.) Su’s multi-fin FinFET includes a “*gate structure, covering the fin-shaped structures*” [1B]. (TSMC-1003, ¶¶204-205); *Google*, 2022 WL 4287797, *9 n.9; *Boston Sci.*, 554 F.3d at 991.

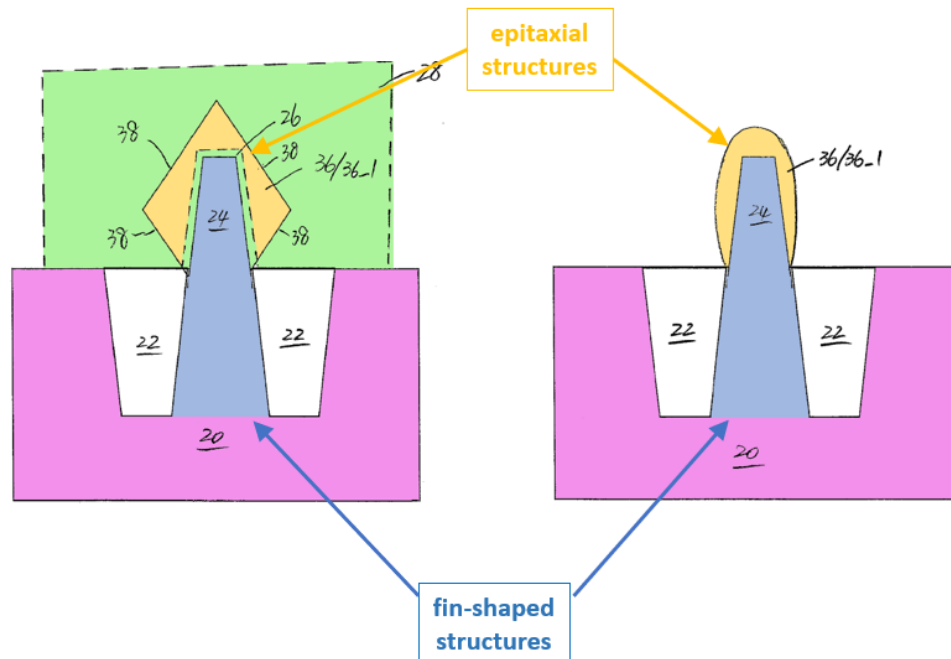


Su, Figures 3 (top-left), 4A (top-right), 9 (bottom)

4. Limitations [1C]-[1D]

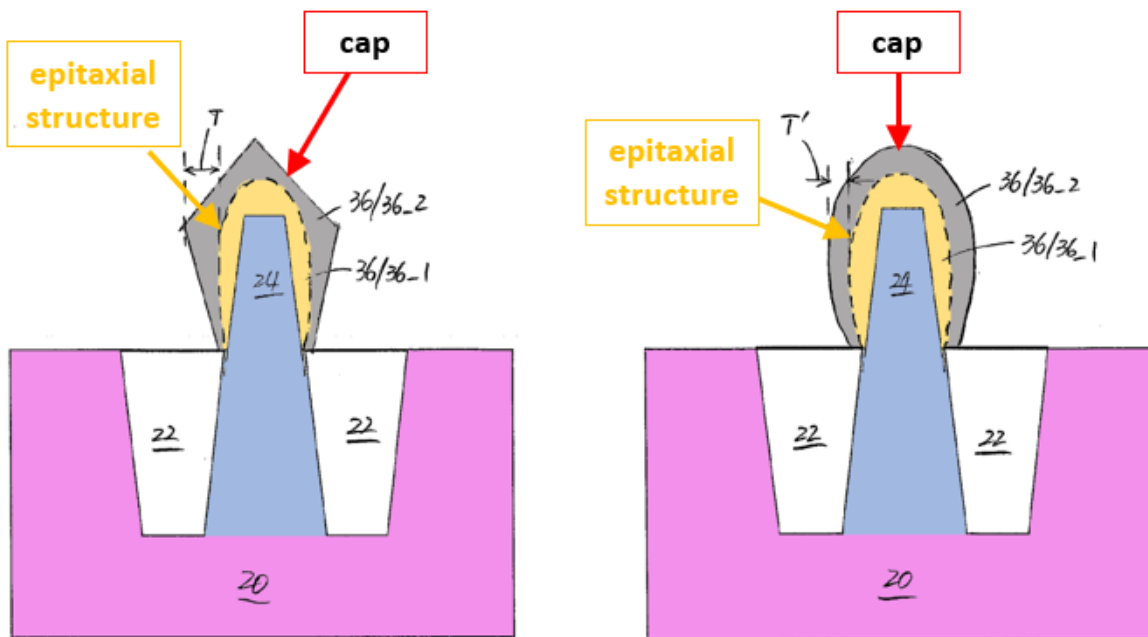
a) “Epitaxial Layer”/“Cap”

During Su’s fabrication process, a first deposition-etch cycle is performed during which epitaxy layer 36_1 “is deposited, for example, epitaxially grown on the exposed portion of fin 24 by selective epitaxial growth (SEG).” (TSMC-1007, ¶17; Figure 4A (below-left).) The epitaxial growth of epitaxy layer 36_1 is then stopped “and an etch step is performed.” (TSMC-1007, ¶21.) During the etch step, “the corners of epitaxy layer 36_1 are removed more than planar portions, and hence the surface profile of epitaxy layer 36_1 is rounded.” (TSMC-1007, ¶21, Figure 5 (below-right).)



Su, Figures 4A (left), 5 (right)

Su performs a second deposition-etch process,¹⁰ where “epitaxy layer 36_2 is epitaxially grown on the remaining portion of epitaxy layer 36_1.” (TSMC-1007, ¶22.) After the second etch step, “the thickness of the added portion of epitaxy layer 36 is reduced to T’”, as shown in Figure 7 (below-right). (TSMC-1007, ¶23.)

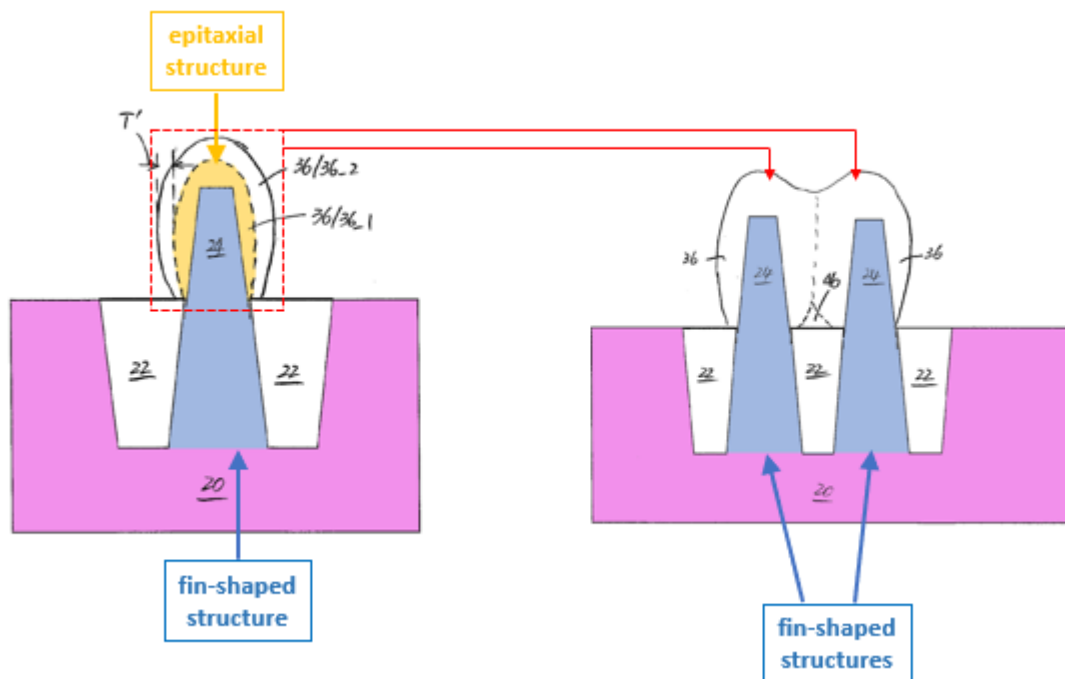


Su, Figures 6 (left), 7 (right)

A POSITA would have been motivated to combine Su’s multi-layer epitaxial structure teachings with the multi-fin embodiment, as illustrated in the figures below. (TSMC-1003, ¶¶208-209; *Boston Sci.*, 554 F.3d at 991.) First, Su

¹⁰ In Su, “[m]ore deposition-etch cycles may be repeated to further increase the depth of epitaxy layer 36.” (TSMC-1007, ¶22.)

motivates the combination, using label “36” in Figure 9 and stating “[t]hroughout the description, epitaxy layers 36_1 and 36_2 in combination are referred to as epitaxy layer 36.” (TSMC-1007, ¶22.) This convention is illustrated in Figure 7, which shows a dashed line representing the boundary line between epitaxy layers 36_1 and 36_2. Additionally, Su teaches “[a]dvantageously, by dividing one deposition-etch cycle into a plurality of deposition-etch cycles, the profile of epitaxy layer 36 may be more conformal.” (TSMC-1007, ¶22.) A POSITA would have been motivated to use a plurality of deposition-etch cycles in Figure 9’s multi-fin embodiment to achieve its goal of eliminating a void in the merged structure, reducing defects. (TSMC-1007, ¶25; TSMC-1003, ¶209.)



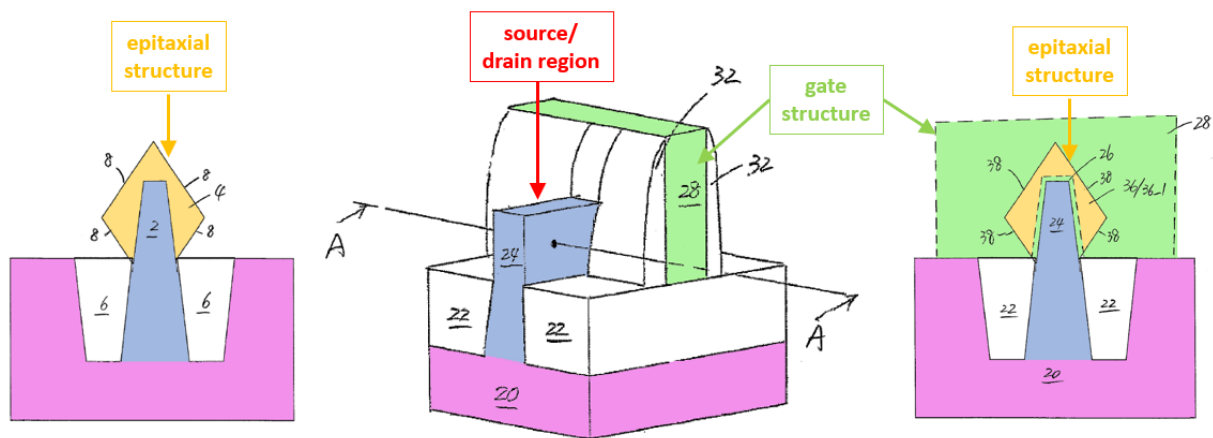
Su, Figures 7 (left), 9 (right)

In Su's multi-fin embodiment, epitaxy layers 36 "are grown from neighboring fins 24." (TSMC-1007, ¶25.) As discussed above, layer 36 on each fin includes **first** epitaxy layer 36_1 and **second** epitaxy layer 36_2. (TSMC-1003, ¶210.) Su's multi-fin embodiment therefore discloses "*at least two epitaxial structures* [epitaxy layer 36_1 on each fin]" [1C] and a "*cap, surrounding the epitaxial structure []* [epitaxy layer 36_2]." (TSMC-1003, ¶210; TSMC-1007, claim 4 ("performing a second deposition step to epitaxially grow a second epitaxy layer over and contacting the remaining portion of the epitaxy layer"); *Google*, 2022 WL 4287797, *9 n.9.)

Su's "epitaxy layer 36_1 is selectively **grown on** fin 24." (TSMC-1007, ¶20; *see also* TSMC-1007, ¶17.) Thus, epitaxy layer 36_1 "*directly contact[s] each fin-shaped structure.*" (TSMC-1003, ¶211.)

Su's multi-fin FinFET has "*epitaxial structures ... disposed at one side of the gate structure*" [1C]. (TSMC-1003, ¶212; *see also* TSMC-1007, claim 21 ("an epitaxy layer on a top surface and sidewalls of the extension of the semiconductor fin").) Figure 9 shows a cross-section, and a POSITA would understand the multi-fin FinFET uses the same basic structure as the single-fin FinFET, illustrated in Figure 1 including "source/drain region 2 (which is part of the original fin) and epitaxy layer 4 epitaxially grown on source/drain region." (TSMC-1007, ¶4; TSMC-1003, ¶212.) In Su's FinFET, epitaxy layer 36 is similarly deposited on the

exposed portions of fin 24,¹¹ which are a source region and a drain region located on respective sides of the gate structure. (TSMC-1007, ¶¶17, 24 (“After the formation of epitaxy layer 36, a source/drain implantation is performed, so that epitaxy layer 36 [which is formed on the exposed portion of the fin] becomes part of the source/drain region of the resulting FinFET 60”), claim 21 (reciting source/drain region comprises “an extension of the semiconductor fin” and “an epitaxy layer on a top surface and sidewalls of the extension of the semiconductor fin”), Figure 4A (cross-section “in the source/drain plane”); TSMC-1003, ¶212.)

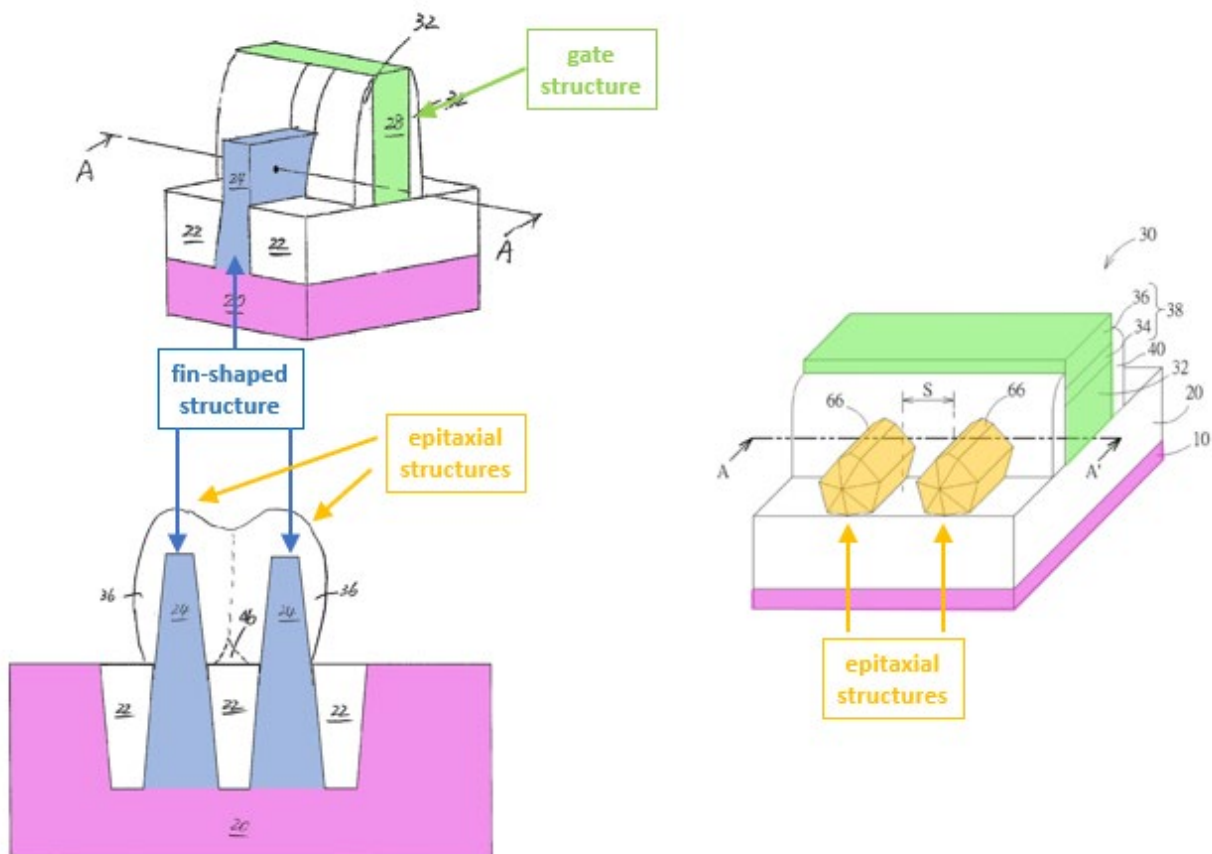


**Su, Figure 1 (left), Figure 3 (middle),
Figure 4a (right)**

As discussed above, Su forms epitaxy layers 36_1 on the exposed portion of neighboring fins which become the source/drain region of the FinFET. The

¹¹ Exposed portions are the fin portions not covered by the gate structure (e.g., the fin ends) as shown in Figure 3 (middle).

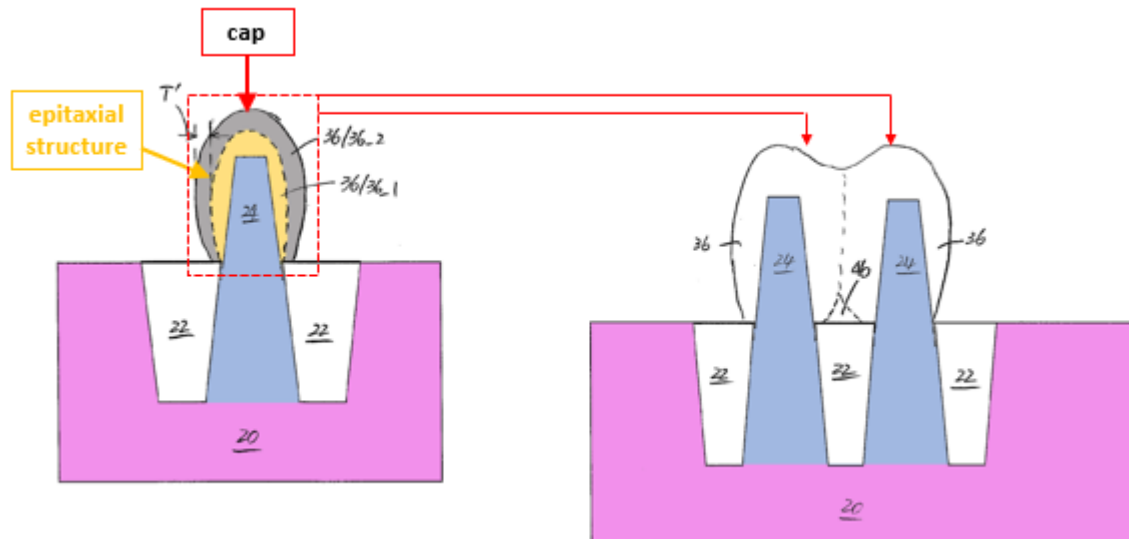
exposed portion of the fins are adjacent to the gate structure, i.e., on one side of the gate structure. (TSMC-1003, ¶213.) Accordingly, Su discloses “*two epitaxial structures, disposed at one side of the gate structure,*” consistent with Figure 5 of the '193 patent (below-right), depicting two epitaxial structures on the same side of the gate. (*Id.*)



**Su, Figures 3 (left-top), 9 (left-bottom);
'193 Patent, Figure 5 (right)**

b) Epitaxial Structures “Spaced Apart” and Caps “Merged”

Su performs a deposition/etch cycle to form epitaxy layer 36_1 (“*epitaxial structure*”) with “an ellipse shape.” (TSMC-1007, ¶21, Figures 5, Figure 7 (below-left).) In Su’s multi-fin FinFET, “epitaxy layers 36 grown from neighboring fins 24 merge with each other to form a single epitaxy region.” (TSMC-1007, ¶25, Figure 9 (below-right), *see also* TSMC-1007, ¶11(Figure 9 illustrates “merging of two epitaxy layers growing from neighboring semiconductor fins”).)



Su, Figures 7 (left), 9 (right)

A POSITA would ascertain the dashed line in Su’s Figure 9 represents the merging boundary of epitaxy layer 36_2 (“*cap*”) (TSMC-1007, ¶22), while the neighboring portions of the inner epitaxy layers 36_1 (“*epitaxial structures*”) remain unmerged. (TSMC-1003, ¶215.) A POSITA would understand if adjacent

epitaxy layers 36_1 were allowed to merge before formation of “cap” epitaxy layer 36_2, they could no longer be etched back to a rounded profile (e.g., be shaped like an ellipse) as originally intended by Su; and such merging of the outer surfaces of adjacent epitaxy layers 36_1 would form substantial voids between the merged epitaxy layers 36_1 and the STI, which Su aims to mitigate, if not eliminate. (TSMC-1007, ¶4; TSMC-1003, ¶215.) Indeed, Su discloses epitaxy layer 36_2 is “epitaxially grown on the remaining portion of epitaxy layer 36_1” (TSMC-1007, ¶22), such that a POSITA would ascertain the dashed line in Su’s Figure 9 represents the merging boundary of the epitaxy layer 36_2. (TSMC-1003, ¶215.) Further, the width of epitaxial layer 36_1 is less than half the width of the STI region, indicating the inner epitaxial layers (36_1) are not thick enough to merge and therefore do not touch. (TSMC-1003, ¶215.)

Accordingly, Su’s device discloses or renders obvious “*the epitaxial structures [epitaxial layers 36_1] are spaced apart from each other*” [1C] and “*at least two adjacent caps [epitaxial layers 36_2] are merged together*” [1D]. (TSMC-1003, ¶216.)

C. Dependent Claims

1. Claim 7

Su discloses the “*composition of each of the epitaxial structures [epitaxy layer 36_1] comprises silicon germanium ...*” [7]: “epitaxy layer 36_1 may

comprise **silicon germanium (SiGe)**, silicon carbon (SiC), or the like.” (TSMC-1107, ¶17.)

2. Claim 10

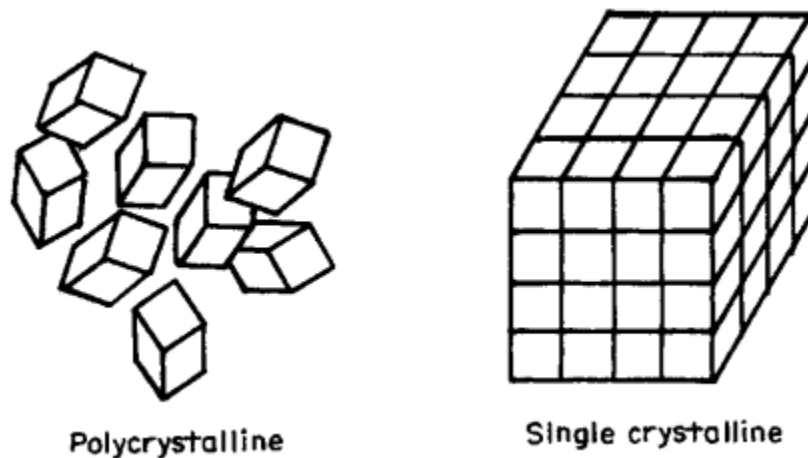
Su renders obvious “*the caps are made of monocrystalline silicon*” [10]. (TSMC-1003, ¶¶218-227.) The ’193 patent states, without further explanation, “silicon cap 68 composed of monocrystalline silicon, may be formed on the surface of each of the epitaxial structures 66 through another epitaxial growth process.” (TSMC-1001, 5:64-6:1.) The patent therefore assumes a POSITA’s base knowledge regarding materials and deposition technology to fill in missing details. Petitioner provides a brief technical background below and demonstrates claim 10 would have been obvious to a POSITA having this assumed background knowledge. (TSMC-1003, ¶¶218-223.)

a) Technical Background

In materials such as silicon and germanium, “atoms are arranged into a very definite structure that repeats throughout the materials”—these materials are called crystals. (TSMC-1022, 53.) One level of organization within a crystal relates to unit cell organization. When the unit cells are neatly and regularly arranged relative to each of the others (Figure 3.5 (below-right)), “materials have a single (or mono-) crystalline structure.” (TSMC-1022, 54.) A monocrystalline structure is formed “[w]hen the chemical reactants are controlled and the system parameters

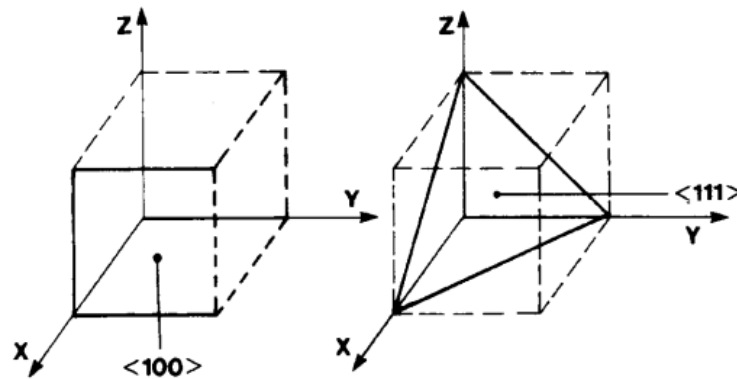
set correctly, [such that] the depositing atoms arrive at the wafer surface with sufficient energy to move around on the surface to orient themselves to the crystal arrangement of the wafer atoms.” (TSMC-1022, 386.)

On the other hand, when unit cells are not in a regular arrangement with each other (Figure 3.5 (below-left)), the material has a polycrystalline structure. (TSMC-1022, 54.) If the semiconductor substrate surface “has a thin layer of silicon dioxide, an amorphous surface layer, or contamination, the depositing atoms have no structure to which they can align,” and the “resulting film structure is polysilicon.” (TSMC-1022, 386; *see also* TSMC-1024, 367.)



Van Zant, Figure 3.5

A crystal’s planes “are identified by a series of three numbers known as Miller Indices.” (TSMC-1022, 55.) Figure 3.6 below illustrates a plane with a $\langle 100 \rangle$ orientation (left) and a plane with a $\langle 111 \rangle$ orientation (right). (TSMC-1022, 55-56.)



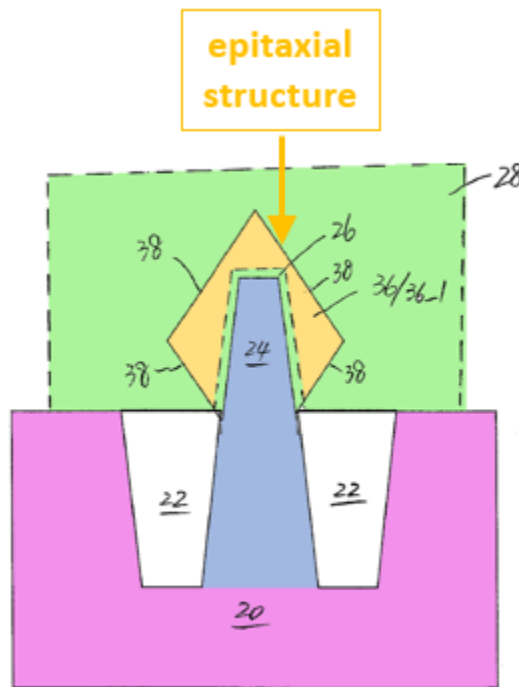
Van Zant, Figure 3.6

b) Su Renders Claim 10 Obvious.

Su's substrate 20 "may be a bulk silicon substrate" with "a surface orientation of (100)." (TSMC-1007, ¶¶14-15.) In this embodiment, "fin 24 extends along the <110> direction." (TSMC-1007, ¶15.) Thus, Su's substrate and fins, formed from the substrate, are "monocrystalline silicon." (TSMC-1022, 55; TSMC-1023, 17-38; TSMC-1003, ¶224.)

Su further teaches epitaxy layer 36_1 ("*epitaxial structure*") is formed of the same semiconductor material as fin 24, for example, "formed of substantially pure silicon." (TSMC-1007, ¶17.) Su notes "the growth rate on surfaces having (111) surface orientations (referred to as (111) planes) is lower than that on other planes, such as (110) and (100) planes", thereby forming the facets shown in Figure 4A below. If "epitaxy layer 36_1 is grown freely, eventually, fac[e]ts 38 will have the (111) surface orientations (in other word[s], on (111) planes)." (TSMC-1007, ¶19.) Because the fin is monocrystalline silicon and epitaxy layer 36_1 is the same

material formed by homoepitaxial growth, layer 36_1 has a crystal structure with a high degree of alignment with the substrate fin on which it is grown and, therefore, is also “monocrystalline silicon.” (TSMC-1003, ¶225; TSMC-1022, 386; TSMC-1023, 152; TSMC-1024, 367.)



Su, Figure 4A

Su further teaches epitaxy layer 36_2 (“cap”) is “formed of the same material as epitaxy layer 36_1.” (TSMC-1007, ¶22; *see also* TSMC-1007, ¶25 (discussing facets of epitaxy layer 36).) Because epitaxy layer 36_1 is monocrystalline silicon and epitaxy layer 36_2 is the same material formed by homoepitaxial growth, epitaxy layer 36_2 has a crystal structure with a high degree of alignment with layer 36_1 on which it is grown and, therefore, is also

“monocrystalline silicon.” (TSMC-1003, ¶226; TSMC-1022, 386; TSMC-1023, 152; TSMC-1024, 367.)

Su, as informed by knowledge of a POSITA, renders obvious claim 10.
(TSMC-1003, ¶227.)

X. Mandatory Notices

A. Real Party in Interest

The Petitioner and real party in interest is Taiwan Semiconductor Manufacturing Company Limited.

B. Related Matters

Petitioner is not aware of any reexamination certificates, or petitions for *inter partes* review for the '193 patent. Petitioner is not aware of any civil actions involving the subject matter of the '193 patent.

C. Notice of Counsel and Service Information

Pursuant to 37 C.F.R. §§42.8(b)(3), 42.8(b)(4) and 42.10(a), Petitioner appoints the following lead and backup counsel:

Lead Counsel	Back Up Counsel
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XI. Conclusion

IPR is respectfully requested.

Respectfully submitted,

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Date: August 20, 2025

CERTIFICATE OF WORD COUNT

Pursuant to 37 C.F.R. §42.24(a), Petitioner hereby certifies that portions of the above-captioned **PETITION FOR *INTER PARTES* REVIEW OF U.S. PATENT 9,337,193**, in accordance with and reliance on the word count provided by the word-processing system used to prepare this Petition, that the number of words in this paper is 13,941. Pursuant to 37 C.F.R. §42.24(a), this word count is in compliance and excludes the table of contents, table of authorities, mandatory notices under §42.8, certificate of service, certificate of word count, appendix of exhibits, and any claim listing. This word count was prepared using Microsoft Word.

Respectfully submitted,

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CERTIFICATE OF SERVICE

The undersigned hereby certifies, in accordance with 37 C.F.R. § 42.105, that the foregoing **PETITION FOR *INTER PARTES* REVIEW OF U.S. PATENT 9,337,193**, TSMC's Power of Attorney, and all supporting exhibits were served via FedEx International Priority on August 20, 2025, in their entirety on the Patent Owner as detailed below:

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