

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

TAIWAN SEMICONDUCTOR MANUFACTURING COMPANY LTD.,
Petitioner,

v.

MARLIN SEMICONDUCTOR LTD.,
Patent Owner.

Case No. IPR2025-01054
U.S. Patent No. 9,337,193

**DECLARATION OF JOSEPH C. MCALEXANDER III REGARDING
PATENT OWNER'S PRELIMINARY RESPONSE FOR *INTER PARTES*
REVIEW OF U.S. PATENT NO. 9,337,193**

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TABLE OF EXHIBITS

Exhibit	Description
2002	Peter Van Zant, <i>Microchip Fabrication, A Practical Guide to Semiconductor Processing</i> , (4 th ed. 2000)
2003	<i>Curriculum Vitae</i> of Joseph C. McAlexander III

I. Qualifications

1. I am a Registered Professional Engineer (#79454) and the President of M^cAlexander Sound, Inc. I hold a Bachelor of Science degree in Electrical Engineering from North Carolina State University. I have been associated with the integrated circuit and electronics industry as a designer and consultant for the past 53 years and am a named inventor on 31 U.S. patents and a number of foreign patents, many of which are directly related to the design and operation of transistors and circuits incorporating transistors, including control, addressing, comparing and sensing, and fabrication.

2. My skills and experience are in areas of circuit design and analysis, device and board fabrication and assembly, testing, marketing, control system design and analysis, manufacturing operations, and respective areas of quality, reliability, and defect/failure analysis. Specifically, I have:

- designed memories, including Dynamic Random Access Memories (DRAMs), Static Random Access Memories (SRAMs), Charge Coupled Devices (CCDs), Shift Registers (SRs), and functional circuits including I/O buffers for address and data, decoders, clocks, sense amplifiers, fault tolerant (incorporating both non-volatile EPROM and random access memory components), parallel-to-serial data paths for video applications, level shifters, converters, pumps, and logic, as well as wireless communication systems and MEMs;
- managed operations including engineering, training, and quality assurance for device fabrication, assembly, test, analysis, and reliability assessment, as well as manufacturing control, each of which involved both volatile and non-volatile memory; testing,

analysis, and control involved use of mechanical calibration and measuring equipment, including optical, scanning e-beam, IR, capacitive, and laser using phase contrast and FFT for HARI applications;

- taught courses in solid-state device physics, integrated circuit design, integrated circuit fabrication, and statistical control;
- provided expert services, investigating both process and design technologies of various devices (microprocessor and controller, volatile and non-volatile memory, programmable logic, card, tag, module, mixed signal, custom, and other), systems (PC and peripheral, computer, control, laser measurement, switch, architecture, software, and other), and consumer products (medical, TV, telephone, VCR, facsimile, copier, lighting, game, and other); and
- designed and managed development, testing, and evaluation of memory devices and systems incorporating such devices, including simulation of operation. I have also had experience in programming, erasing, and wearout of electrically programmable and erasable non-volatile memories.

3. Because of my background, training, and experience, I am qualified as an expert to opine on the challenged patent. A more detailed account of my work experience and other qualifications is listed in my Curriculum Vitae, which is submitted as Exhibit 2003.

II. Overview

4. Each of the five asserted grounds in the Petition fails to disclose multiple limitations of the challenged claims of U.S. Patent Number 9,337,193 (“the ’193 patent”).

5. For example, the challenged claims recite “at least two epitaxial structures... wherein the epitaxial structures are ***spaced apart*** from each other” and “at least two caps, respectively surrounding the epitaxial structures, wherein at least two adjacent caps are ***merged*** together.” None of the Petition’s asserted grounds disclose or render obvious these claim elements. The ’193 patent specification explains that “[d]uring the epitaxial growth process for the silicon cap 68, the silicon cap 68 continuously grows on the surface of each of epitaxial structure 66 and gradually fills up the space between two adjacent epitaxial structures 66 until two adjacent silicon caps 68 merge together as shown in FIG. 7.” Ex. 1001, 6:1-6. That is, at least two adjacent caps 68a and 68a are formed on two different epitaxial structures 66 (which are spaced apart) to create a single merged cap 68, as depicted in Figure 7.

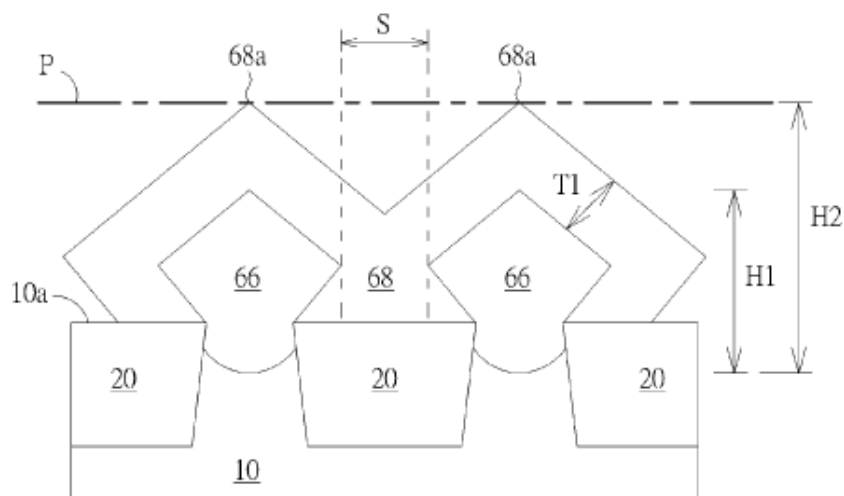
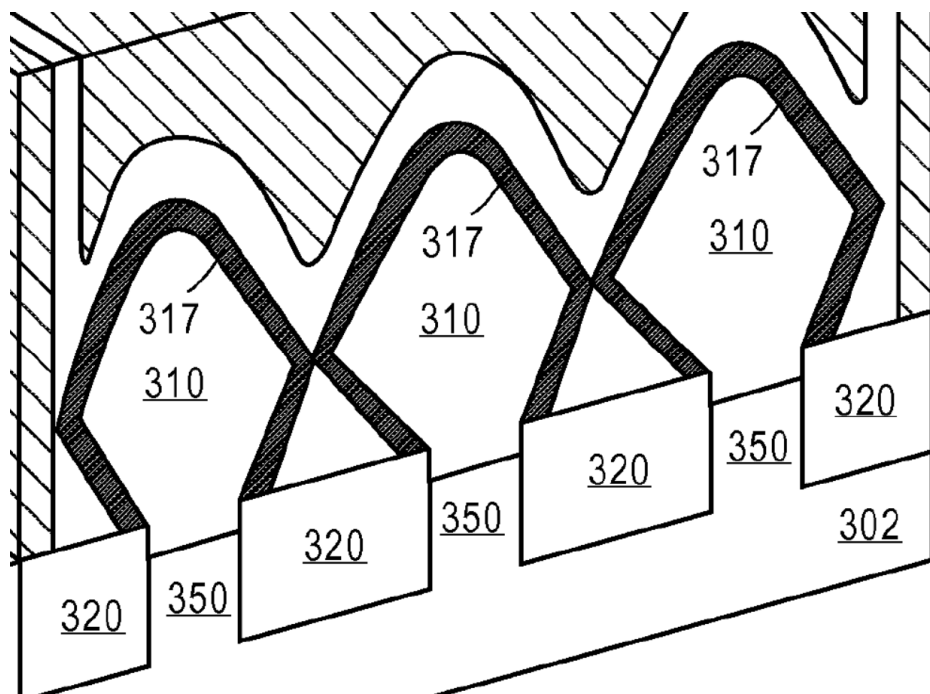


FIG. 7

Ex. 1001, Fig. 7. In contrast, none of the asserted prior art discloses or renders obvious at least two spaced apart epitaxial structures and that at least two adjacent caps are formed on the two epitaxial structures and then merged together.

Glass (US 10,535,735 B2, Ex. 1005) (Grounds 1 and 2):

6. The Glass reference does not disclose or render obvious that “at least two adjacent caps are merged together.”



Ex. 1005, Fig. 3I (partial). Glass’s alleged “caps” (317 in Fig. 3I) are not merged together. As seen above, the layers 317 are separate with, at most, a point contact between them, such that they cannot be said to be “merged.” Moreover, as explained below in § VII.A.1.b, the Petition fails to set forth any factual basis for its assertion that a POSITA would have been motivated to modify Glass to include “at least two adjacent caps [that] are merged together.”

Kelly (US 8,703,556 B2, Ex. 1009) and Murthy (US 8,598,003 B2, Ex. 1010)
(Grounds 3 and 4):

7. The Kelly reference discloses a device with two epitaxial structures that are spaced apart but no caps, much less that at least two adjacent caps are merged together.

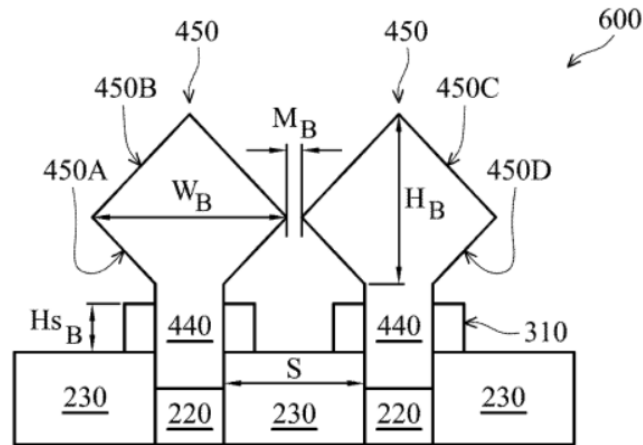


FIG. 7B

Ex. 1009, Fig. 7B.

8. The Murthy reference discloses a single epitaxial structure and a single cap layer.

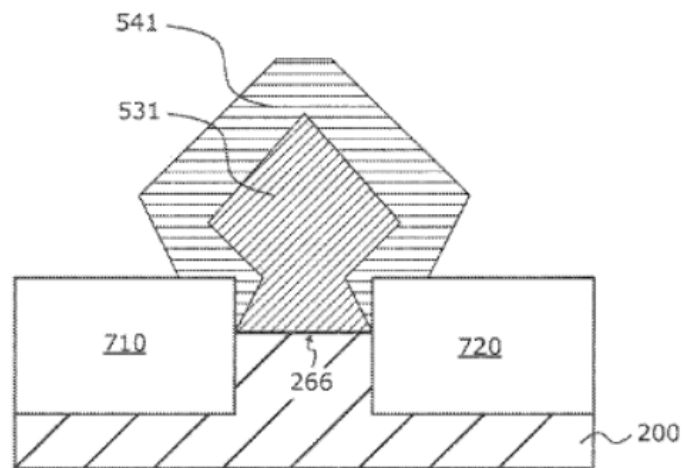
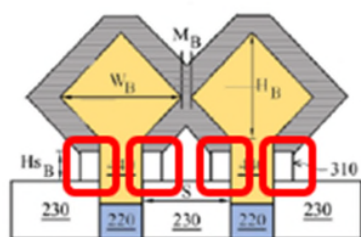


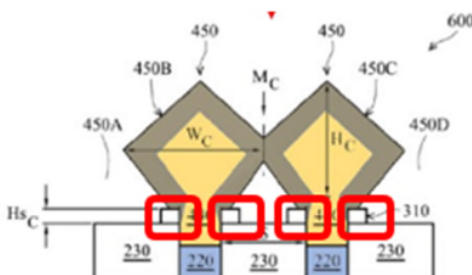
FIGURE 15

Ex. 1010, Fig. 15. The Petition alleges that a POSITA would have been motivated to combine Kelly and Murthy. However, as explained below in §§ VII.B.1-3, the Petition offers no rationale that a POSITA would have been motivated to implement the claimed feature: a merged cap. Nor could it, because since neither Kelly nor Murthy disclose a merged cap, neither can supply a rationale for implementing such a merged cap.

9. Grounds 3 and 4 also fail for an additional reason. Both of the Petition’s proposed Kelly-Murthy combinations include Kelly’s “sidewall spacers 310” on either side of each epitaxial structure and thus, the cap layers are not “respectively surrounding” the epitaxial structures.



Kelly-Murthy Combination



Kelly-Murthy Combination

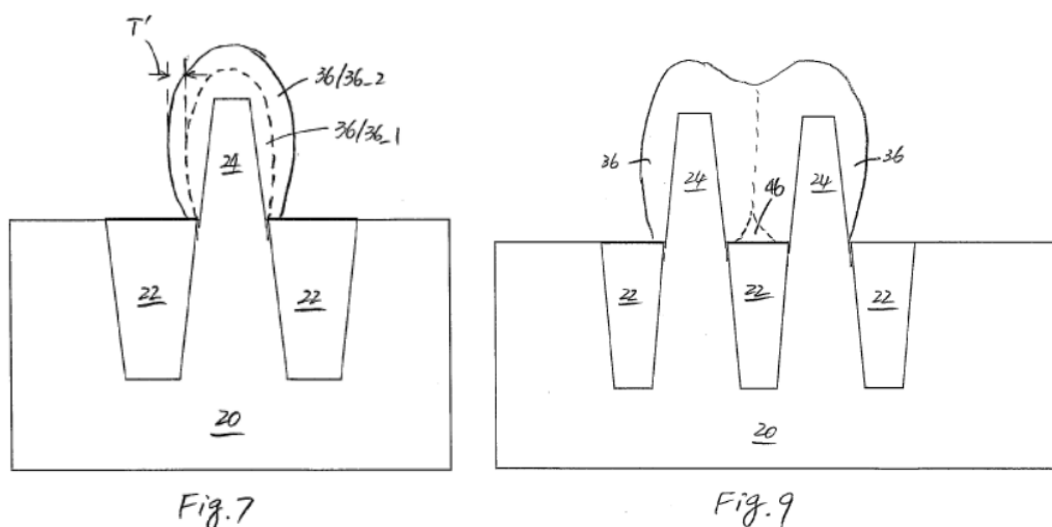
First Kelly-Murthy Combination

Second Kelly-Murthy Combination

Pet., 52-53 (annotated).

Su (US 2011/0210404 A1, Ex. 1007) (Ground 5):

10. The Su reference also fails to disclose a device with spaced-apart epitaxial structures and a merged cap. The Petition points to Su's Fig. 7, which depicts a device with two layers: one epitaxial structure (36_1) and one an alleged cap (36_2). In Figure 9, Petitioner argues, without support, that only outer layers 36_2 would be merged, and not inner layers 36_1.



Ex. 1007, Figs. 7 and 9. However, as explained below in § VII.C.1, the Petition fails to set forth a factual basis for why the combination would result in “spaced apart” epitaxial structures (36_1) and “merged” caps (36_2). Indeed, the reference is silent on the issue.

III. Materials Considered

11. In preparing this declaration, I have reviewed the Petition and the declaration of Petitioner's expert, as well as the materials that they cite, including the asserted prior art.

IV. Understanding Of The Law

12. In preparing and expressing my opinions and considering the subject matter of the challenged patent, I am relying on certain basic legal principles that counsel have explained to me. These principles are discussed below.

A. Claim Construction

13. I understand that the scope of a patent is defined by its claims. I understand that a claim can be:

- a. a method claim, which covers a process/activity, or
- b. an apparatus claim, which covers a physical machine, etc.

14. I understand that the first step in determining the validity of a claim is for the claim to be properly construed. I have been further advised that, in an inter partes review proceeding, the claims of a patent are typically given their ordinary and customary meaning as would be understood by one of ordinary skill in the art in the context of the claims and the patent disclosure (specification).

15. I further understand that an inventor can provide special definitions for specific claim term(s) within the patent. However, any special definition for a claim term must be set forth in the specification with reasonable clarity and precision.

B. Invalidity

16. I have been informed that a claim may be invalid as obvious if the subject matter described by the claim, as a whole, would have been obvious to a

POSITA at the time the claimed invention was made. I understand that the standard for obviousness in an inter partes review proceeding is by a preponderance of the evidence.

17. I have also been informed that a determination of obviousness involves an analysis of the scope and content of the prior art, the similarities between the claimed invention and the prior art, and the level of ordinary skill in the art. I have been informed and understand that a prior art reference should be viewed as a whole.

18. I have been informed that, in considering whether an invention for a claimed combination would have been obvious, I may assess whether there are apparent reasons to combine known elements in the prior art in the manner claimed in view of interrelated teachings of multiple prior art references, the effects of demands known to the design community or present in the market place, and/or the background knowledge possessed by a POSITA. I also understand that other principles may be relied on in evaluating whether a claimed invention would have been obvious.

19. I have been informed that, in making a determination as to whether or not the claimed invention would have been obvious to a POSITA, one is to consider certain objective indicators of non-obviousness if they are present, such as: commercial success of product(s) practicing the claimed invention; long-felt but

unsolved need; teaching away; unexpected results; copying; and praise by others in the field. I understand that, for such objective evidence to be relevant to the non-obviousness of claim, there must be a causal relationship (called a “nexus”) between the claim and the evidence. I also understand that this nexus must be based on a novel element of the claim rather than something available in the prior art.

20. I have also been informed and understand that, when considering the obviousness of a patent claim, one should consider whether a reason or motivation existed for combining the elements of the references in the manner claimed, and that the prior art must create a reasonable expectation of success in producing the claimed subject matter.

V. Semiconductor Transistor Technology Primer

21. The following is a brief primer of semiconductor transistors to establish a foundation of common terms and concepts that can be used in addressing the defects in the Petition. These terms and concepts focus on: (1) the basic components of transistors; (2) the difference between planar and three-dimensional (*e.g.*, fin) transistors; and (3) common process steps for creating transistors.

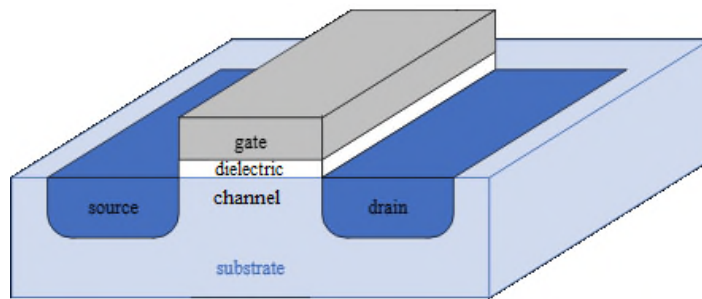
A. Basic Transistor Components

22. Today’s semiconductor devices trace their lineage back to the first computers of the 1940s, which used vacuum tubes to perform two key electrical functions: switching (*i.e.*, turning access to electrical current on and off) and

amplification (*i.e.*, increasing the amplitude of a signal while retaining its electrical characteristics). Ex. 2002 at 1-2. Where earlier tube devices used a vacuum tube to control the flow of electrons (turning electrical current on and off), today's semiconductor devices use transistors. Ex. 2002 at 3.

23. One type of transistor typically used in an integrated circuit (or “chip”) is a “field effect transistor,” or FET. Materials used to build such transistors are divided into three categories based on their ability to conduct electrical current: conductors, dielectrics, and semiconductors. Ex. 2002 at 29-34. In a conductor (*e.g.*, a metal), electric current can flow freely. Ex. 2002 at 29. A dielectric (*e.g.*, silicon dioxide) is an insulative material at the opposite end of the conductivity spectrum and has a high resistance to the flow of current. Ex. 2002 at 30. Semiconductors (*e.g.*, silicon) fall between conductors and dielectrics and have some conducting and some resisting ability. Ex. 2002 at 31-34.

24. The simplified FET below illustrates how these materials may be used to create a semiconductor transistor device. As shown, the transistor is built on a semiconductor substrate and comprises a source, a drain, a gate, and a channel. See, *e.g.*, Ex. 2002 at 510-511. The source, drain and channel comprise semiconductor material, the gate comprises a conductor, and the gate and channel are separated by a thin dielectric layer.

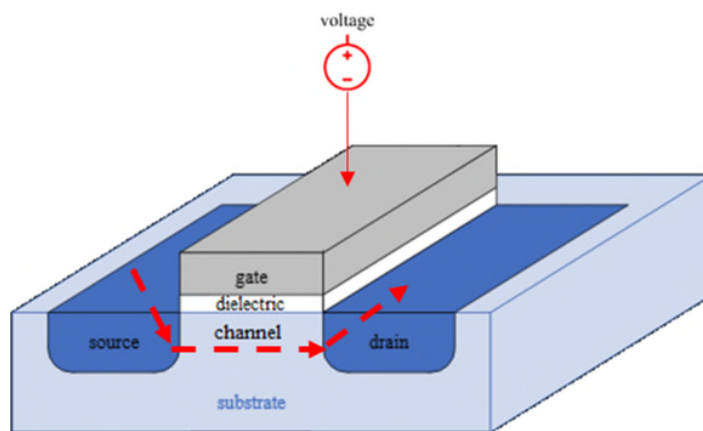


See, e.g., Ex. 2002 at 510-511.

25. The source and drain are regions in the semiconductor substrate that are either rich in electrons (a negative, or n-type, region) or rich in holes (a positive, or p-type, region). Ex. 2002 at 26-28, 427-28. The channel is a region under the gate and between the source and drain, and is of the opposite type to that of the source and drain. In other words, if the source and drain are n-type regions, then the channel will be a p-type region (and vice versa). Ex. 2002 at 510-511.

26. The gate is a conductor (or semiconductor) located above the channel. In this simplified version of a FET, there is a dielectric between the channel and the gate. Ex. 2002 at 510-511. When a voltage is applied to the gate, the dielectric prevents the flow of charge (electrons, holes) from the gate to the channel, but the applied voltage results in the creation of a “field effect” in the channel. Ex. 2002 at 510-511. This “field effect” either builds up or depletes the charges in the channel (depending on whether it is a p- or n-type channel). Ex. 2002 at 510-511.

27. As illustrated below, this field effect allows charge to flow from the source, through the channel, to the drain. Thus, selectively applying voltage to the gate switches the transistor on and off, starting and stopping source-to-drain electrical current.

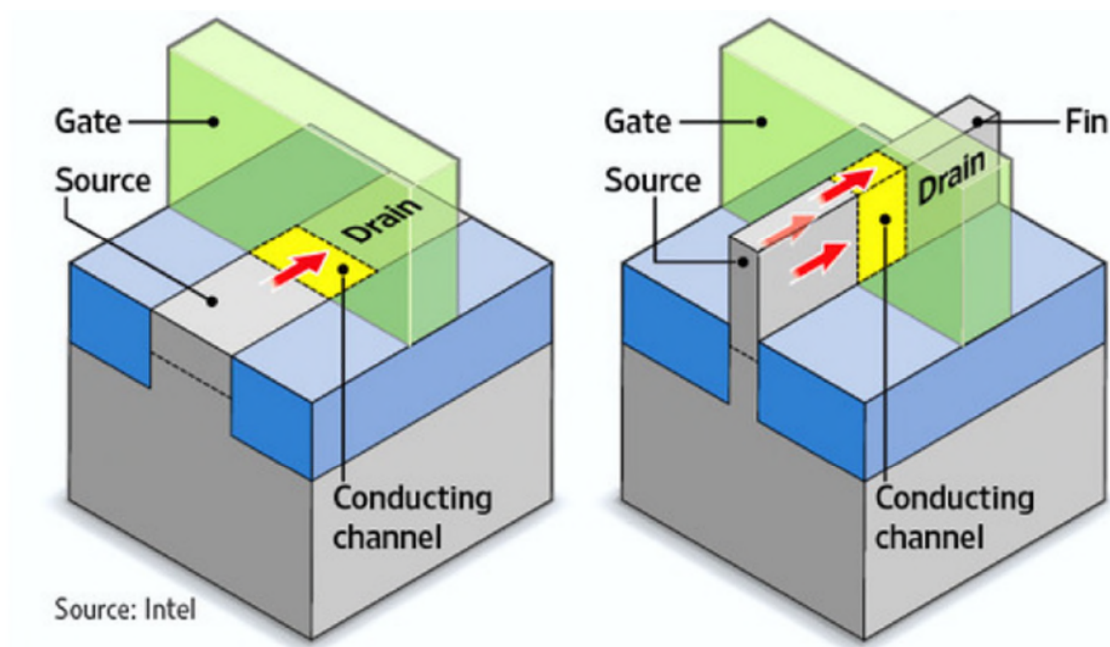


B. Planar vs. Three-Dimensional Transistors

28. Integrated circuit chips in modern computer systems are typically composed of millions and even billions of transistors. The first transistor prototypes in 1947 were several inches in size, and implementing even the simplest early computers required tens of thousands of gates or transistors. Given those numbers, and the correlation between an increased number of transistors and increased computing power, the desire to shrink transistor sizes to fit more on a chip has been consistent and widespread in industry. This desire led to the development of a new type of transistor, a “FinFET.”

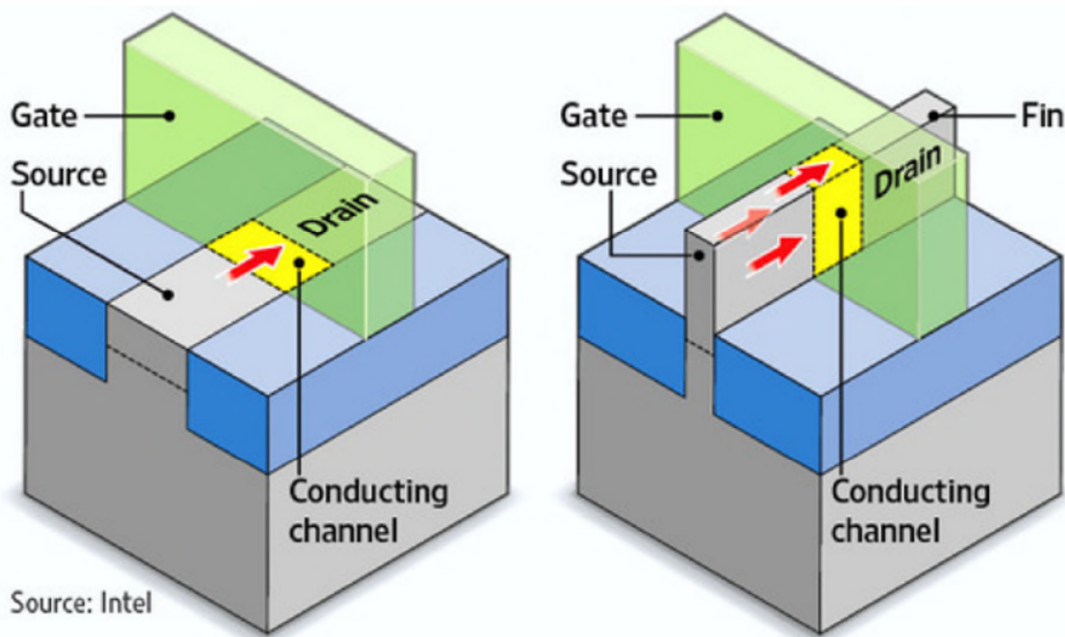
29. The simplified illustrative FET transistors illustrated in the previous section all feature a gate structure built on a flat semiconductor substrate; in other words, a “planar” FET. In the early 2010s, however, commercial gates evolved from such two-dimensional (2D) planar transistors to three-dimensional (3D) FinFET transistors.

30. In the below image, the figure on the left illustrates a 2D planar transistor built on a flat silicon substrate. In this traditional 2D planar transistor, the transistor forms a conducting channel in the silicon region under the gate.



31. In contrast, as illustrated below in the right figure, an exemplary 3D fin transistor design features a vertical semiconductor fin structure above the substrate that acts as a channel between the source and drain regions. In the resulting fin field

effect transistor (“FinFET”), the source and drain regions are formed at opposing regions of the fin, and the gate is wrapped over the fin surrounding the fin on the top and two sides.



32. Thus, where a planar gate has only a horizontal dimension, the FinFET gate has both horizontal and vertical dimensions, thereby allowing a FinFET transistor to take up less surface area than a planar transistor. This alone means that more FinFET transistors may fit on an integrated circuit chip compared to that of the planar transistor. In addition, because FinFETs typically leak less current than planar FET transistors, FinFETs may be more tightly packed on an integrated circuit chip. This, too, increases the number of FinFET transistors that may fit onto a single chip.

C. Processes For Manufacturing Integrated Circuits And Transistors

1. The Four Stages Of Fabricating Integrated Circuits

33. The intricate, complex manufacturing process developed over the years for achieving such highly-dense integrated circuits can be divided into four distinct stages: (1) material preparation; (2) wafer preparation; (3) wafer fabrication; and (4) packaging.

34. In the first stage, the semiconductor material itself is created. Ex. 2002 at 13. For a silicon semiconductor, the raw starting material is sand, which is converted to pure silicon with a polysilicon structure. Ex. 2002 at 13.

35. In the second stage, the semiconductor material is first formed into a silicon crystal with specific electrical and structural parameters, and it is then sliced into thin disks called “wafers.” Ex. 2002 at 13-14. A wafer acts as a semiconductor substrate on and in which transistors may be formed.

36. The third stage is wafer fabrication, during which individual integrated circuits are formed in and on the wafer semiconductor substrate. Ex. 2002 at 14. Thousands of integrated circuits can be formed on the substrate of a single wafer. Ex. 2002 at 14.

37. In the packaging stage, the wafer is separated into individual chips. Ex. 2002 at 14-15.

2. The Wafer Fabrication Stage

38. The third manufacturing stage, wafer fabrication, is the one most relevant here, and it can take several thousand steps, during which transistors and other devices are formed in and on the wafer's substrate. Ex. 2002 at 14. These steps are generally performed using three categories of materials (conductors, semiconductors, and dielectrics) in four basic operations (layering, patterning, doping, and heat treatments). See Ex. 2002 at 29-31, 71. For purposes of understanding the Petition and its deficiencies, the two most important basic operations are layering and patterning.

39. **Layering** is the operation used to add thin layers to the semiconductor substrate. Ex. 2002 at 72. The layers may be conductors, semiconductors, or dielectrics; and they can have a variety of functions and be made in a variety of ways. Ex. 2002 at 72.

40. For example, one way of adding a layer of material is to deposit that material onto the semiconductor substrate. Another way of adding a layer of material is to grow the material on the semiconductor substrate. After an initial layer is added to the semiconductor substrate, additional layers may be added to the earlier layers using similar growth or deposition processes. To illustrate, the transistor structure shown below shows a number of layers that have been added to the wafer's semiconductor substrate, some deposited, some grown. Ex. 2002 at 72.

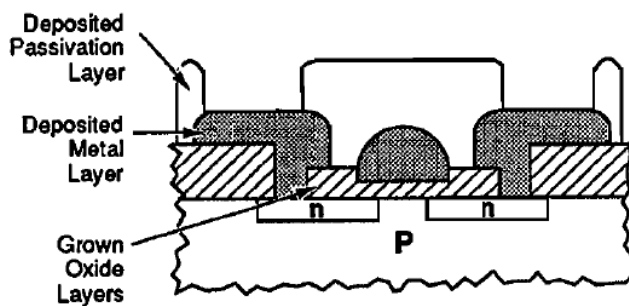


Figure 4.4 Cross section of completed metal gate MOS transistor with grown and deposited layers.

41. **Patterning** is the series of steps to remove (etch away) selected portions of the semiconductor substrate or one or more layers of materials that were added during one or more prior layering operations. Ex. 2002 at 72-73. This creates a pattern on the wafer surface. Ex. 2002 at 72-73.

42. The patterning may result in one or more holes in the layered material or one or more remaining islands of material. Ex. 2002 at 72-73. For example, the following figures illustrate the use of patterning to make (1) a hole in a previously formed layer: and (2) an island from a previously formed layer:

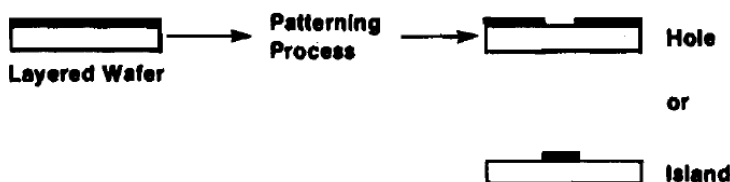


Figure 4.7 Patterning.

43. The repeated combination of layering and patterning in different sequences and variations is critical to the formation of transistors in and on the semiconductor wafer:

These parts are created one layer at a time by the combination of putting a layer on the surface and removing a portion, with a patterning process, to leave a specific shape. The goal of the patterning operations is to create the desired shapes in the exact dimensions (feature size) required by the circuit design, and to locate them in their proper location on the wafer surface and in relation to the other parts.

Ex. 2002 at 73.

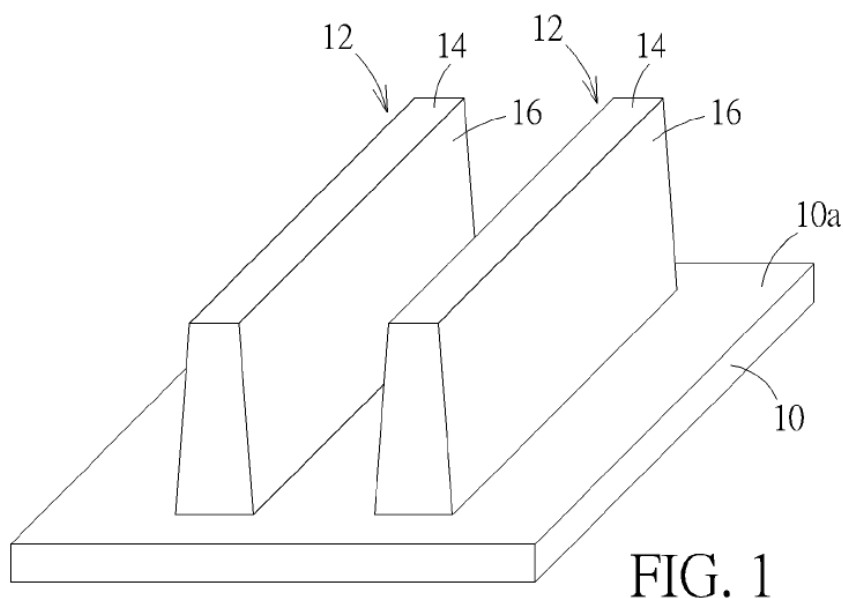
VI. The Challenged '193 Patent

44. The '193 patent “relates generally to non-planar semiconductor devices, and more particular to non-planar semiconductor devices with epitaxial structures.” Ex. 1001, 1:15-17. Specifically, the patent states that “one main technology generally used in the strained-silicon technology is to dispose epitaxial structures with lattice constants different from that of the crystal silicon in the source/drain regions of the semiconductor devices.” *Id.*, 1:39-43. “Since the epitaxial structures have lattice constants larger or smaller than that of the crystal silicon, carrier channel regions adjacent to those epitaxial structures could sense external stresses and both the lattice structure and the band structure within these

regions are altered. As a result, the carrier mobility and the performances of the corresponding semiconductor devices are improved effectively.”

45. The patent identifies weaknesses in the prior art in that “two adjacent epitaxial structures within the semiconductor device often generate unwanted lattice defects on their interfaces.” *Id.*, 1:36-42. The described invention is designed to solve those issues. *Id.*, 1:66:-2:2 (“One purpose of the present invention is to provide a semiconductor device with epitaxial structures, which has few lattice defects in the epitaxial structures and has enhanced stresses imposed onto the channel region.”).

46. “FIG. 1 is a schematic perspective view showing a semiconductor device at the beginning of the fabrication process. At this stage, a semiconductor device having a substrate 10 and a plurality of fin-shaped structures 12 disposed thereon is provided.” Ex. 1001, 2:51-55.



Ex. 1001, Fig. 1.

47. “FIG. 2 is a schematic perspective diagram showing the semiconductor device after the formation of a dummy gate structure.” Ex. 1001, 3:37-39. As shown, “[a]n isolating structure 20 is formed on the substrate 10 and the lower portion of each fin-shaped structure 12 is embedded in the isolating structure 20. In this way, subsequently-formed transistors may be electrically isolated from one another by the isolating structure 20.” Ex. 1001, 3:39-43. Then, a gate structure 30 is “formed to cover the substrate 10 and the fin-shaped structures 12” such that “gate structure 30 crosses over at least two fin-shaped structures 12 and covers the isolating structure 20 between them.” Ex. 1001, 3:51-61.

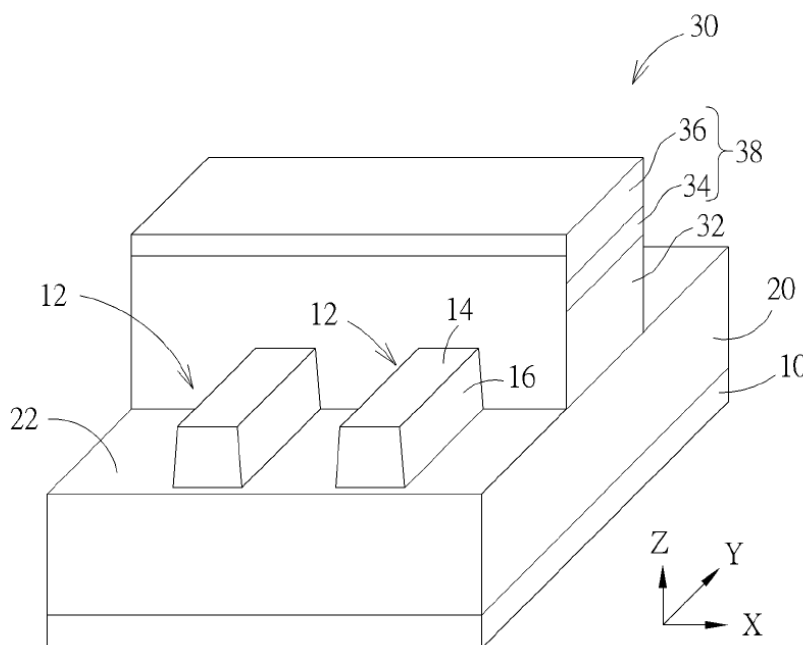


FIG. 2

Ex. 1001, Fig. 2.

48. After forming the gate structure, a spacer 40 is formed on the sides of the gate structure 30 to define the position of the epitaxial structures. Subsequently, an etching process is carried out to etch the fin-shaped structures. Ex. 1001, 5:6-8; Figs. 3 and 4. “After the etching process, recesses 60 may be respectively formed in each fin structure 12 at at least one side of the gate structure 30.” *Id.*, 5:8-10.

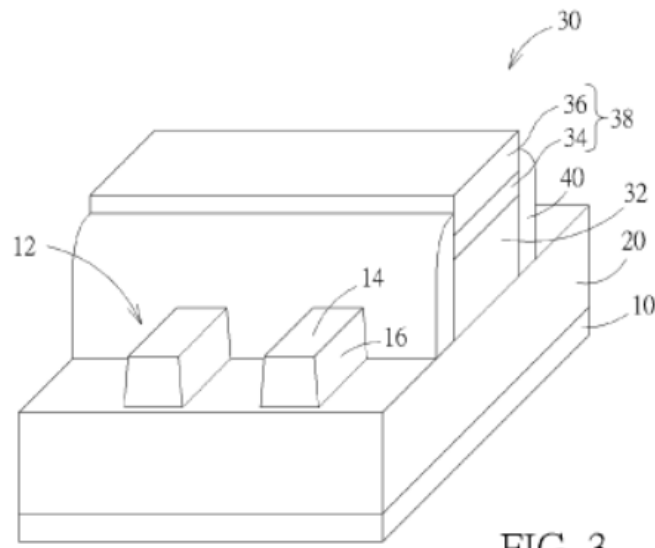


FIG. 3

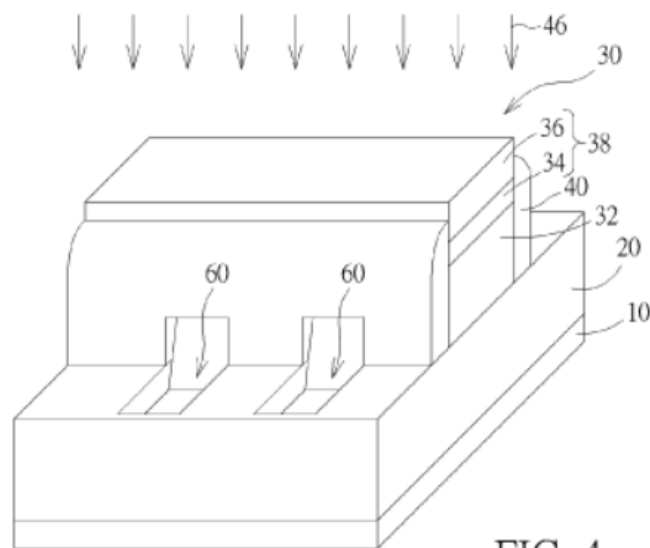
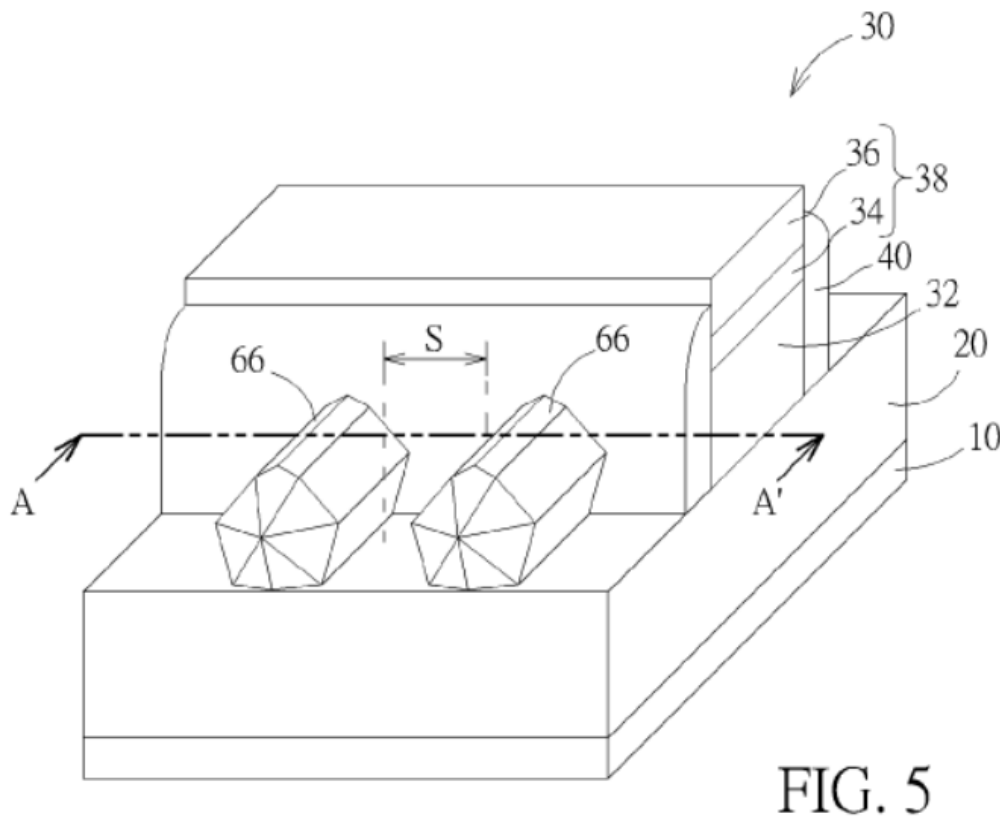


FIG. 4

Ex. 1001, Figs. 3 and 4.

49. The patent then describes the next step, forming the epitaxial structures. “FIG. 5 is a schematic perspective view showing the semiconductor device after the formation of epitaxial structure.” Ex. 1001, 5:20-22. “[A]fter the formation of the

optional recesses 60, epitaxial structures 66 are respectively formed in the corresponding recesses 60 through performing an epitaxial growth process. Preferably, two adjacent epitaxial structures 66 are disposed individually and spaced apart from each other so as to ensure that they don't merge together.” *Id.*, 5:24-30.



Ex. 1001, Fig. 5. That the epitaxial structures do not merge is a key element of the claimed invention. See Ex. 1001, claim 1[c] (reciting “wherein the epitaxial structures are spaced apart from each other”). Spacing apart the epitaxial structures in this manner mitigates unwanted lattice defects.

50. Finally, the patent describes forming merged caps that surround the epitaxial structures:

After the formation of the epitaxial structures 66, another epitaxial layer, such as a silicon cap 68 composed of monocrystalline silicon, may be formed on the surface of each of the epitaxial structures 66 through another epitaxial growth process. During the epitaxial growth process for the silicon cap 68, the silicon cap 68 continuously grows on the surface of each of epitaxial structure 66 and gradually fills up the space between two adjacent epitaxial structures 66 until two adjacent silicon caps 68 merge together as shown in FIG. 7.

Ex. 1001, 5:64-6:6; Fig. 7 (below).

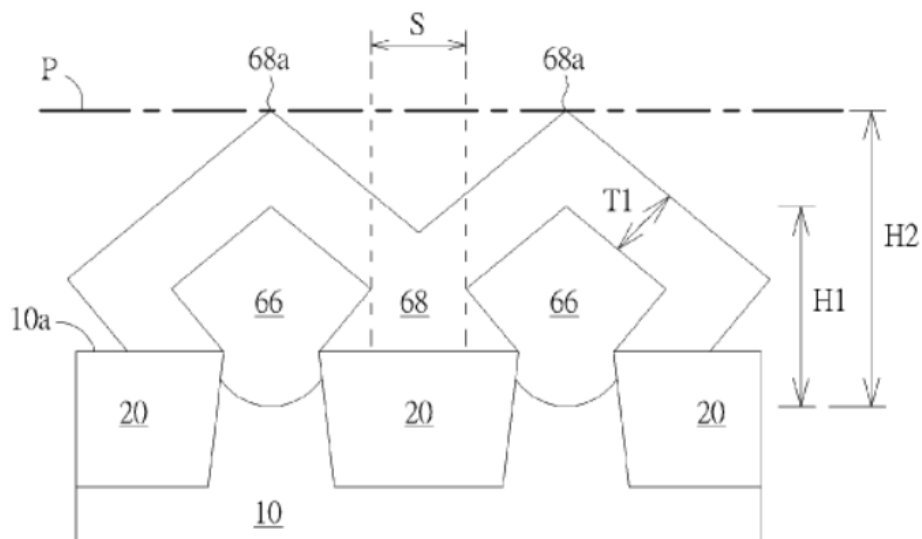
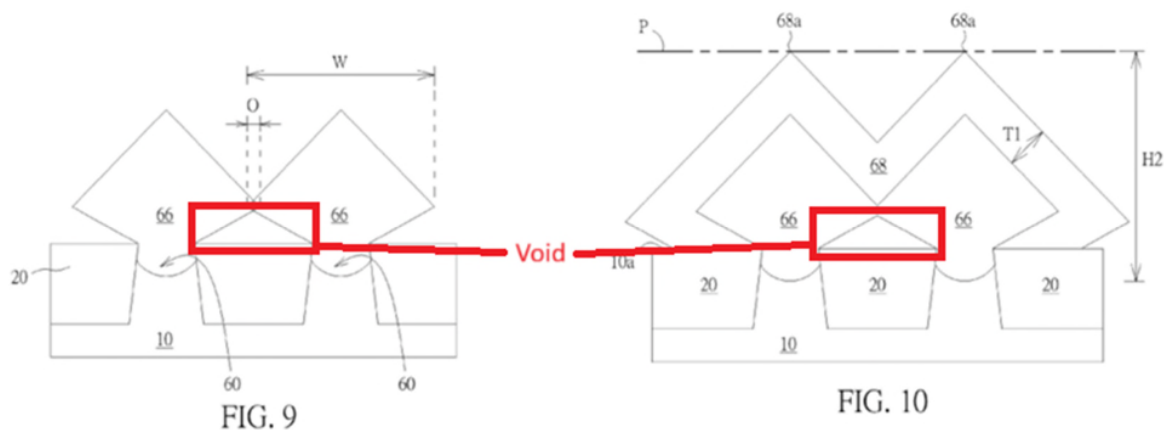


FIG. 7

51. As shown in Fig. 7 above, the merged caps 68 surround the epitaxial structures 66. That two adjacent caps surround the epitaxial structures and merge together is a key element of the claim. See Ex. 1001, claim 1 (“at least two caps, respectively surround the epitaxial structures, wherein at least two adjacent caps are merged together”). Using a two-layer process (e.g., cap layer over epitaxial structure layer) can reduce the continued propagation of a defect, such as the formation of a void between two epitaxial structures. For example, as shown in Figs. 9 and 10, if the epitaxial structures merge before the cap layer is added, then a void forms beneath the merged portion:



Ex. 1001, Figs. 9 and 10 (annotated). Such a void can negatively impact device performance, for example by reducing mechanical strength, hindering electrical conductivity, or causing shorts. In contrast, Fig. 7, which illustrates the claimed embodiment of spaced apart epitaxial structures and a merged cap, has no such void:

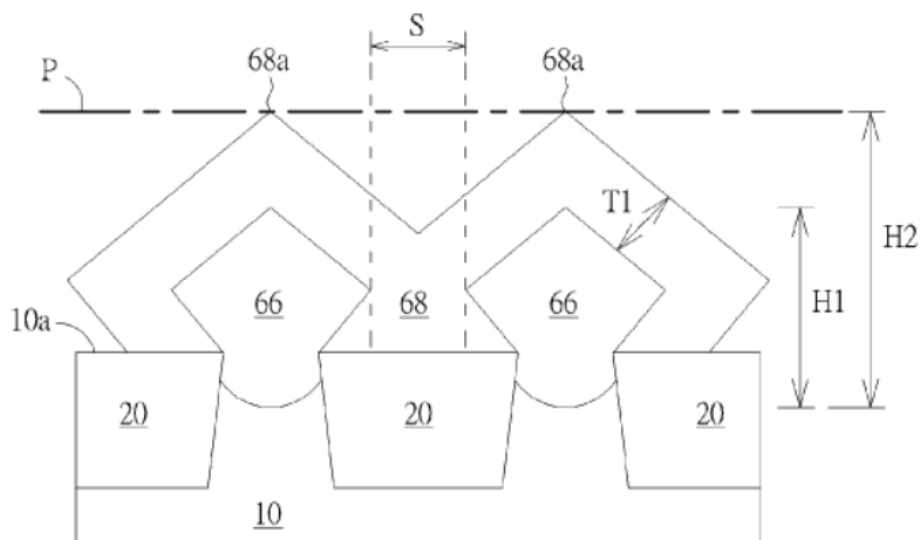


FIG. 7

Ex. 1001, Fig. 7. Thus, having the epitaxial structures spaced apart and then merging adjacent caps eliminates this issue. Moreover, merging adjacent caps together can also smooth the top surface contour or add height to the structure, for example for conduction purposes.

52. The above-described innovative aspects of the invention are embodied in all challenged claims via independent claim 1, which recites:

1. A semiconductor device, comprising:

at least two fin-shaped structures, disposed on a substrate;;

a gate structure, covering the fin-shaped structures;

at least two epitaxial structures, disposed at one side of the gate structure and respectively directly contacting

each fin-shaped structure, wherein the epitaxial structures are spaced apart from each other; and

at least two caps, respectively surrounding the epitaxial structures, wherein at least two adjacent caps are merged together.

Ex. 1001, claim 1.

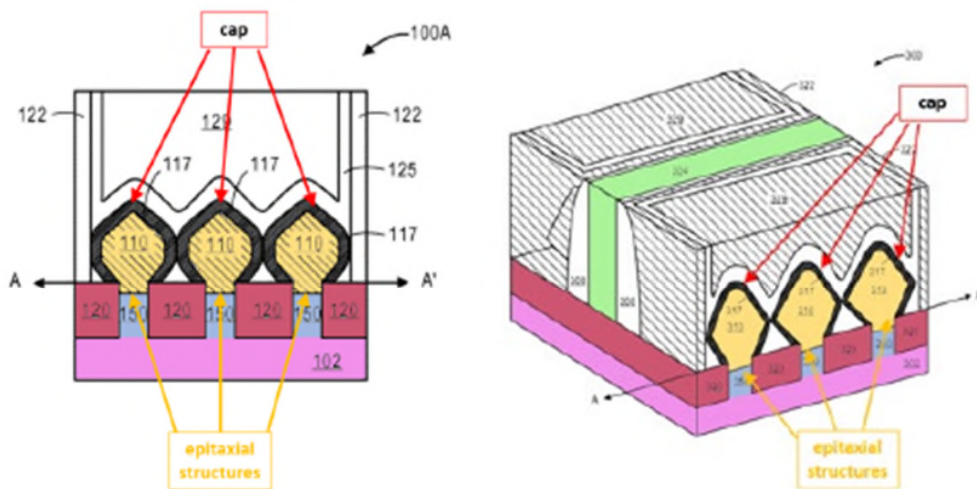
VII. Analysis Of The Grounds

A. Grounds 1 and 2

1. Ground 1 Fails To Disclose Or Render Obvious “Wherein At Least Two Adjacent Caps Are Merged Together” (Element 1[d])

53. Claim 1 requires that “at least two adjacent caps are merged together.”

Ex. 1001, claim 1. Ground 1 fails to disclose that feature. The Petition alleges that “Glass explicitly discloses ‘*at least two adjacent caps are merged together*’ [1D] as shown in Figures 1A and 3I”, pointing to Glass’s “boron-doped germanium-tin alloy layer” (117 in Fig. 1A and 317 in Fig. 3I) as the claimed cap. Pet., 23.



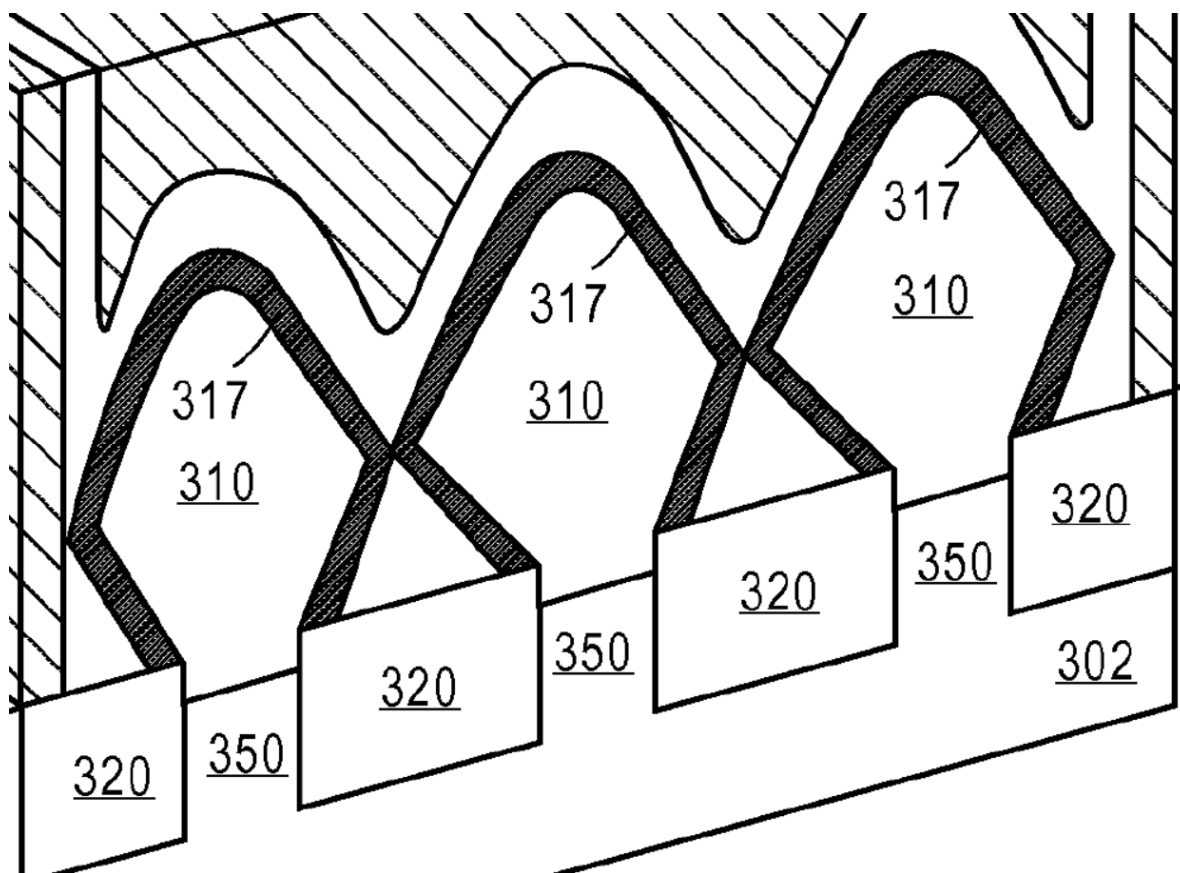
Glass, Figures 1A (left), 3I (right)

Pet., 22 (annotated Glass Figs. 1A and 3I). However, even if the alloy layer is considered a cap, Glass fails to disclose or render obvious “wherein at least two adjacent caps are merged together,” as required by element 1[d].

a. Glass Does Not Disclose Two Adjacent Caps Merged Together

54. First, the Petition alleges that “Glass explicitly discloses ‘*at least two adjacent caps are merged together*’ [1D] as shown in Figures 1A and 3I above.” Pet., 23 (citing Glass, Figs. 1A and 3I). The Petition does not even argue that any written description in Glass teaches or suggests that two adjacent caps are merged together. Pet., 23-25. Nor could it because the text of Glass simply does not describe or embody this feature. See Ex. 1005, 3:36-5:22 (describing Fig. 1A).

55. Moreover, neither Figure 1A nor Figure 3I of Glass discloses that two adjacent caps are merged together. As shown below, Figure 3I includes solid lines between adjacent alloy layers 317:



Ex. 1005, Fig. 3I (partial). Thus, at most, Figure 3I suggests that the boundary of one alloy layer 317 may abut the boundary of another, but not that two adjacent caps “merge together.” In contrast, the ’193 patent explains that “the silicon cap 68 continuously grows on the surface of each of epitaxial structure 66 and gradually

fills up the space between two adjacent epitaxial structures 66 until two adjacent silicon caps 68 merge together as shown in FIG. 7.” Ex. 1001, 6:1-6.

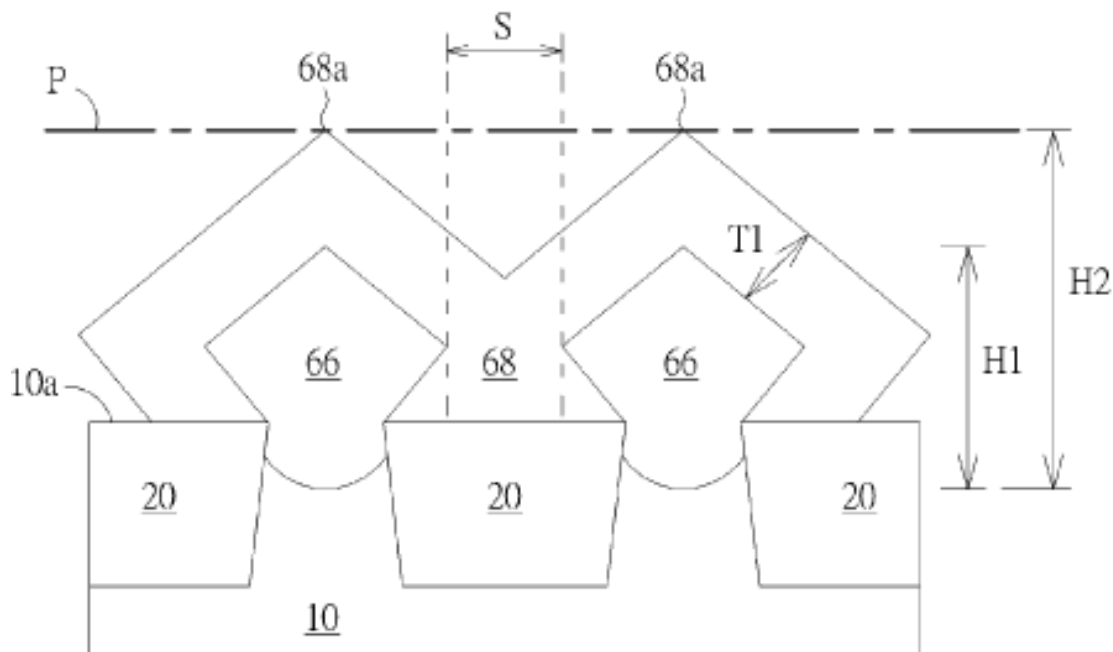
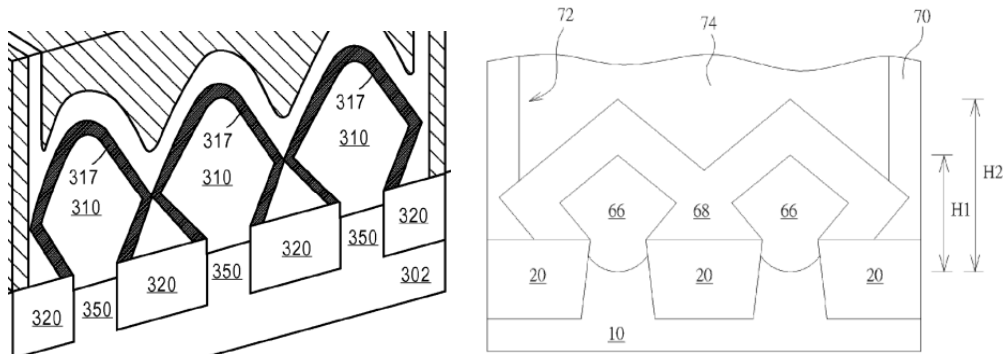


FIG. 7

Ex. 1001, Fig. 7. As shown above, the '193 patent's figures clearly illustrate that two adjacent caps are merged together, rather than simply abutting each other, as evidenced by the lack of any lines between adjacent caps. *Compare* Ex. 1005, Fig. 1A *with* Ex. 1001, Fig. 7. Moreover, as shown below, while the '193 patent's figures include only one "silicon cap 68," indicating that two adjacent caps merge together to form a single merged structure, Glass's Figure 3I includes separate labels 317 for each alloy layer, indicating that they remain separate structures. Thus, under

Petitioner's own proffered definition of "merge" ("to cause to combine, unite, or coalesce"), Glass does not disclose that two adjacent caps are "merged together."



Ex. 1005, Fig. 3I (left); Ex. 1001, Fig. 8 (right). Thus, Glass's Figure 1A does not disclose that "two adjacent caps are merged together," as required by claim 1.

56. Glass's Figure 1A fares no better. Figure 1A depicts the same device as Figure 3I from a different viewpoint. Ex. 1005, 3:40-44 ("An isometric view of the example finFET is shown in FIG. 3I, with the cross-sectional plane of FIG. 1A taken along line A-A' through one of a pair of source/drain regions of the device."). As such, and as shown below, all of Figure 3I's defects also appear in Figure 1A, because, as Glass states, they are the same device. In Figure 1A, the solid lines delineate the boundary between two adjacent alloy layers 117 and the figure depicts of each alloy layer 117 as a separate, un-merged structure, as further confirmed by Fig. 3I above:

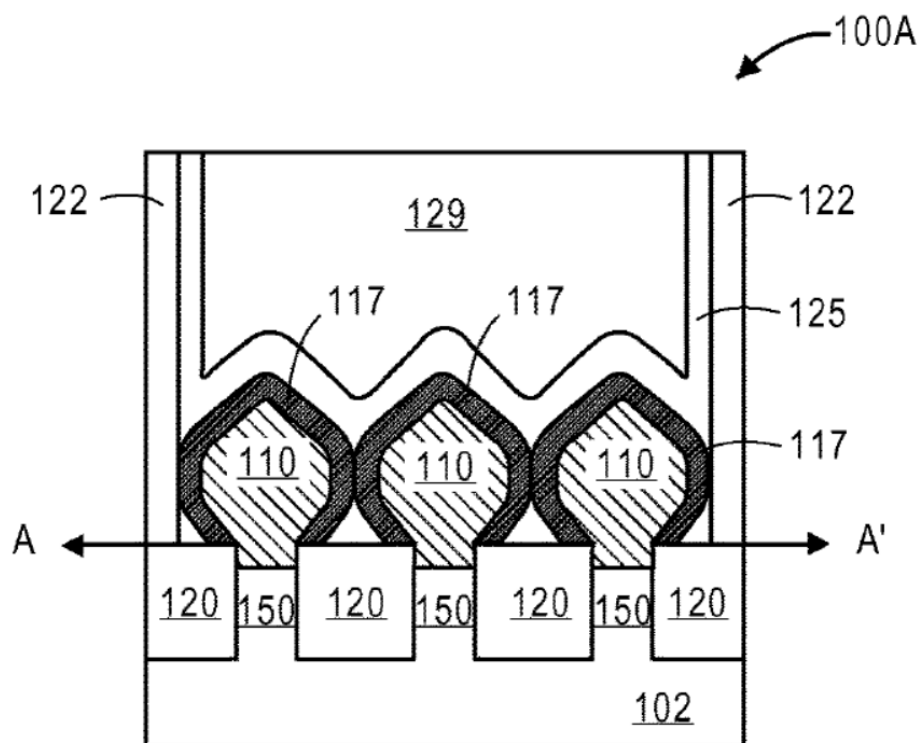


FIG. 1A

Ex. 1005, Fig. 1A. Thus, Glass's Figure 1A also fails to disclose that "two adjacent caps are merged together," as required by claim 1.

57. The Petition's allegations are further undercut by Glass's explicit statement that "the various embodiments shown in the figures are illustrative representations and are *not necessarily drawn to scale*." Ex. 1005, 1:60-62 (emphasis added). Here, Glass's figures fail to clearly show that two adjacent alloy layers are merged together and there is nothing in the specification to support that they are merged. As such, Glass does not disclose this feature.

b. Glass Does Not Render Obvious That Two Adjacent Caps Are Merged Together

58. The Petition next alleges that “this feature would have been obvious based on the teachings of Glass and a POSITA’s semiconductor knowledge.” Pet., 23. The only disclosure in Glass cited by the Petition for this obviousness argument is that the alloy layer 317 may have a thickness between 1 nm and 50 nm (500 Angstrom) and that a completely different processor, “the Intel 22nm Ivy Bridge processor included a FinFET with a fin pitch of 60 nm and a fin width of 7 nm-18 nm.” Pet., 23 (citing Ex. 1005, 9:38-41). Based on this one sentence in Glass, the Petition argues that because **one particular, wholly unrelated FinFET device** (a particular Intel processor) had a fin pitch of 60 nm and a fin width of 7 nm to 18 nm, a POSITA would have been motivated to employ an alloy layer thickness such that two adjacent alloy layers are merged. Pet., 23; Ex. 1003, ¶ 82 (citing Ex. 1026, 13).

59. As an initial matter, the Petition’s combination is purely speculative in that it arbitrarily uses dimensions of a specific FinFET device without providing any rationale for why a POSITA would consider the Intel processor relevant or use the dimensions of that particular device over any other. Pet., 23. The Intel processor dimensions are far from common or mandatory. For example, Petitioner’s own Exhibit 1018 describes FinFET devices with “[f]ins of 20 nm width and 120 nm pitch.” Ex. 1018, 1. Using these dimensions, the distance between adjacent fins

would be 100 nm, meaning that even at the highest alloy layer thickness disclosed by Glass (50 nm), the alloy layers would still not merge. *See* Ex. 1001, 6:6-8 (“[I]n order to obtain a merged silicon cap 68, the thickness T1 of the silicon cap 68 is at least greater than one-half of the distance S.”). Petitioner’s expert declaration likewise offers no rationale for using the specific dimensions identified by the Petition. Ex. 1003, ¶ 82.

60. Moreover, the Petition’s obviousness argument is further flawed because it ignores that the Intel Ivy Bridge (the specific FinFET device that the Petition purports to use in its obviousness combination) already includes a silicon cap that does not meet the requirements of claim 1 and thus has no use for a merged cap—not that the Petition even makes such an argument in the first place. For example, Ex. 1026, Figure 2.3.3.22 depicts “source/drain silicon caps”:

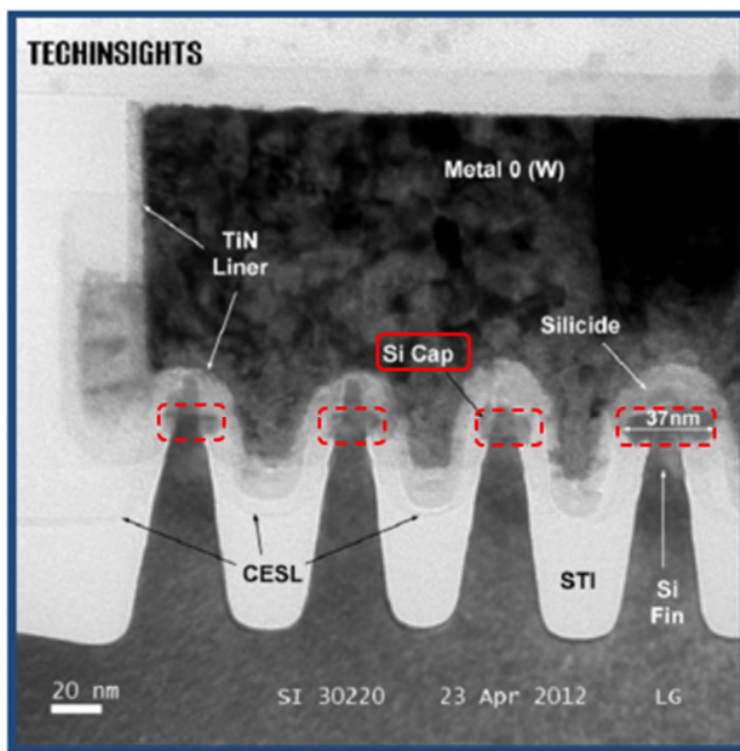


Figure 2.3.3.22: Source/drain silicon caps of NMOS transistor, high magnification TEM cross-section.

Ex. 1026, 110. As shown, the silicon caps do not even come close to merging together. Moreover, the above figure shows a total width of the silicon cap (including the width of the fin itself) of 37 nm. Ex. 1026, 110. The width of the top of the fin is 7 nm. Ex. 1026, 13. Thus, the thickness of the cap in any direction would be approximately 15 nm. Conveniently, the Petition ignores this dimension of the Intel Ivy Bridge despite alleging that “a POSITA would have known exemplary values based on products and documents available prior to the ’193 patent.” Pet., 23. In short, the Petition’s obviousness argument is speculative and conclusory. It is premised on a POSITA’s knowledge of certain specific dimensions

of an arbitrary specific FinFET device while completely disregarding the one dimension (cap thickness) of the device that is determinative in whether two adjacent caps merge together.

61. Finally, the Petition fails to offer a motivation to merge together adjacent caps, as required by the claims. The Petition alleges that “a POSITA would have known before the ’193 patent merging adjacent source/drain structures increases the contact area between the source/drain regions and the source/drain contact, which reduces the source/drain contact resistance.” Pet., 24-25. However, increasing the contact area between the source/drain regions and the source/drain contact can be done by simply increasing the size of the source/drain structures without any merging—thus, this does not provide a reason to merge together two adjacent caps, as required by the claims. Similarly, the Petition alleges that “a POSITA would have been motivated to use a thickness for the less resistive boron-doped germanium-tin layer 317 that allows cap layers from adjacent epitaxially grown source/drain regions to merge for an additional reason—a larger total area translates to a larger landing area for the source/drain contact, which relaxes the photolithography requirements when patterning source/drain contacts.” Pet., 25. Again, a larger total area can be achieved without merging the caps; for instance, a device could have two larger but farther apart source/drain structures which would

increase the total area without any merging of the structures. Thus, this too fails to supply a reason to merge together two adjacent caps, as required by the claims. Accordingly, the Petition's motivation to combine arguments fail to explain why a person of ordinary skill in the art would have combined elements from specific references *in the way the claimed invention does*.

62. Accordingly, Glass does not disclose or render obvious that “two adjacent caps are merged together,” as required by claim 1. Thus, Ground 1 fails.

2. Ground 2 Fails For The Same Reasons As Ground 1

63. Ground 2 adds the Tsai reference to address an additional limitation of dependent claim 6, which depends from independent claim 1. Pet., 37. Ground 2 does not provide any further analysis regarding claim 1. Pet., 37-45. Thus, Ground 2 fails for the same reasons as Ground 1.

B. Grounds 3 and 4

64. In Ground 3, the Petition alleges that the combination of Kelly and Murthy renders obvious claims 1-10. Pet., 45. In Ground 4, the Petition alleges Kelly, Murthy, and Liaw render obvious dependent claim 11, which depends from claim 1. Pet., 90.

65. Neither Kelly nor Murthy discloses “at least two caps,” much less two caps “respectively surrounding the epitaxial structures, wherein at least two adjacent caps are merged together.” Specifically, Kelly discloses multiple epitaxial structures

but no caps, and Murthy discloses a single epitaxial structure and cap layer. Exs. 1009, 1010. As such, the combination of Kelly and Murthy does not disclose at least that “at least two adjacent caps are merged together,” as explained in more detail below.

66. Thus, both of Grounds 3 and 4 fail because the combination of Kelly and Murthy does not disclose or render obvious claim 1.

1. The Petition Fails To Provide A Motivation To Combine Kelly and Murthy To Form Merged Caps

67. The Petition presents two different Kelly-Murthy combinations: “(1) Kelly’s FinFET with the source/drain arrangement of Figure 7B structures and Murthy (‘first combination’); and (2) Kelly’s FinFET with the source/drain arrangement of Figure 7C and Murthy (‘second combination’).” The Petition offers various reasons that would allegedly motivate a POSITA to combine Kelly and Murthy. Pet., 53-56. However, these reasons, at the very most, establish only that a POSITA would be motivated to add Murthy’s cap layer to Kelly’s epitaxial structures, rather than that a POSITA would be motivated to implement the claimed feature: a merged cap. *See id.* Nor could the Petition offer such a rationale, because since neither Kelly nor Murthy disclose a merged cap, neither can supply a rationale for implementing such a merged cap.

68. **First**, the Petition argues that “Kelly expressly motivates a cap layer to its epitaxial structure (first combination) or using both Murthy’s epitaxial region and cap (second combination)” because Murthy teaches that its cap layer reduces parasitic resistance. Pet., 53. But this does not provide a motivation to implement Murthy’s cap layer as a **merged** cap, like the claimed invention does.

69. **Second**, the Petition points to Murthy’s teaching that its epitaxial region and cap provide performance gains. Pet., 54. But again, these alleged performance gains are provided by Murthy’s single epitaxial region and cap; that is, they do not provide a motivation to create a merged cap.

70. **Third**, the Petition alleges that a POSITA would have looked to Murthy to provide additional details regarding epitaxial processes and features. Pet., 55. This, too, fails to provide any reason to form a merged cap.

71. **Fourth**, the Petition alleges that either combination would be a substitution of a known technique (addition of a cap layer) or element (Murthy’s source/drain structure having an epitaxial region or cap) for another. Pet., 55. But neither Kelly nor Murthy teaches a merged cap; as such, a merged cap is not a “known element.” Thus, this also fails to supply a reason to implement a merged cap.

72. Thus, because the Petition fails to supply a sufficient motivation to combine elements in Kelly and Murthy in the way the claimed invention does, Ground 3 fails.

2. The First Kelly-Murthy Combination Does Not Render Obvious “Wherein At Least Two Adjacent Caps Are Merged Together” (Element 1[d])

73. For the first Kelly-Murthy combination, the Petition alleges that “a POSITA would have been motivated to grow Murthy’s cap 541/542 on the epitaxial structures 450 of Kelly’s Figure 7B.” Pet., 51. Figure 7B is shown below:

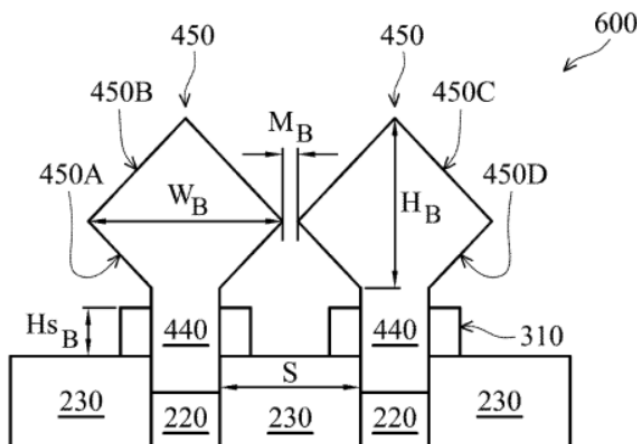


FIG. 7B

Ex. 1009, Fig. 7B. Regarding element 1[d], the Petition alleges that “[a] POSITA would have understood that *when M_B [the distance between the epitaxial structures 450B and 450C] is less than the thickness of the caps or close to zero,*

the deposition of the cap layer on each structure 450 causes the caps to merge.” Pet., 66. But Kelly never discloses that M_B is less than the thickness of the caps or close to zero. See Ex. 1009, 5:64-6:9. It says nothing anywhere about the value of M_B . Moreover, Kelly explicitly states that “in accordance with the standard practice in the industry, various features are not drawn to scale.” *Id.*, 1:34-35. As such, the Petition fails to set forth a factual basis that the first Kelly-Murthy would result in merged caps.

3. The Second Kelly-Murthy Combination Does Not Render Obvious “Wherein The Epitaxial Structures Are Spaced Apart From Each Other” (Element 1[c]) And “At Least Two Caps, Respectively Surrounding The Epitaxial Structures, Wherein At Least Two Adjacent Caps Are Merged Together” (Element 1[d])

74. For the second Kelly-Murthy combination, the Petition alleges that “a POSITA would have been motivated to use Murthy’s source/drain structure having epitaxial region 531/532 and cap 541/542 as Kelly’s epitaxial structures 450 of Figure 7C.” Pet., 51. Figure 7C is shown below:

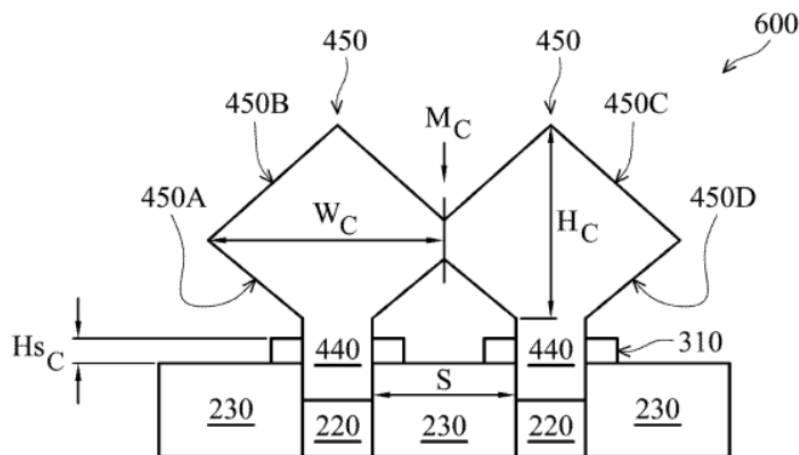
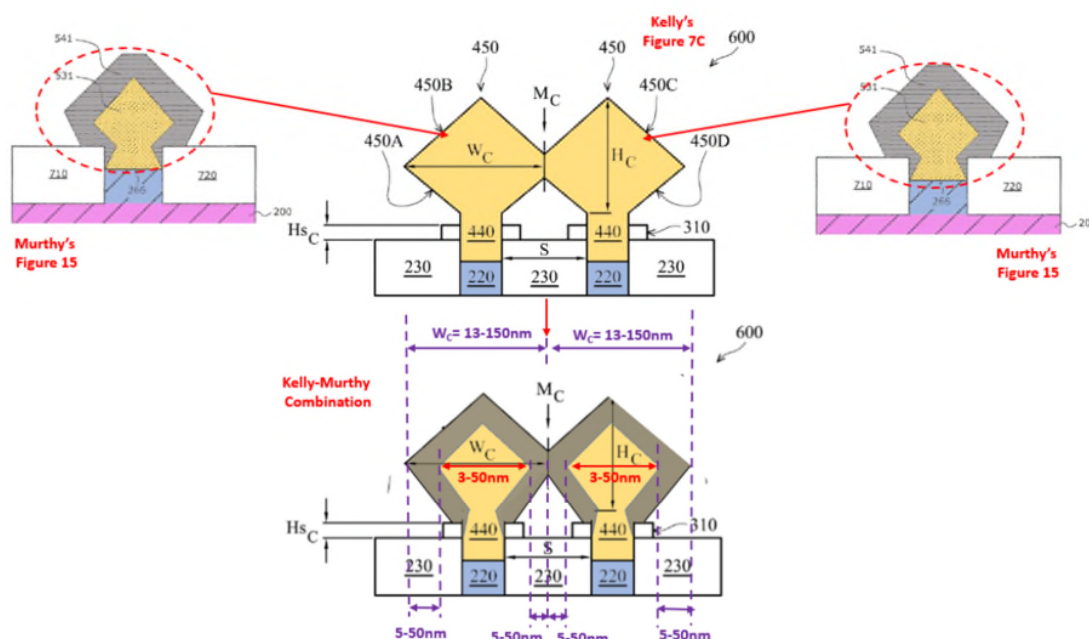


FIG. 7C

Ex. 1009, Fig. 7C. As shown, Kelly's Figure 7C embodiment includes two merged epitaxial structures. Thus, the epitaxial structures are not "spaced apart from each other," as required by claim 1[c].

75. The Petition alleges that a POSITA would have been motivated to substitute Kelly's merged epitaxial structure for Murthy's epitaxial region and cap, resulting in spaced apart epitaxial structures but a merged cap layer. Pet., 53.



Second Kelly-Murthy Combination

Pet., 72.

76. But as explained above in § VII.B.1, the Petition offers no rationale that would support a motivation to combine Kelly and Murthy in such a way. Moreover, a POSITA would have specifically **not** been motivated to modify Kelly's Figure 7C embodiment in such a way because the entire point of Figure 7C (as compared to Figures 7A and 7B) is that adjacent epitaxial structures are **not** spaced apart. See Ex. 1009, 5:64-6:9 ("Referring to FIGS. 7A-7C, with a fixed spacing distance (S) between two adjacent fins 220, different fin-spacer-heights (Hs) may result in... a different merging distance (M) between two adjacent epitaxial structure 450.... When two adjacent vertexes merge together, the M has a value from zero to a

negative value.”). That is, Kelly explicitly discloses a tunable merging distance between adjacent epitaxial structures and Figure 7C illustrates an embodiment in which the epitaxial structures are not spaced apart. *Id.*; *see also id.*, claim 7 (reciting “wherein a merging spacing (M) between two adjacent epitaxial structures is tunable by Hs with a fixed S.”). A POSITA, therefore, would have understood that having two adjacent ***epitaxial structures*** (rather than caps) merge together would confer some advantage or tradeoff the inventors deemed important, for example, that merging epitaxial structures reduces undesirable stress which can increase speed. A POSITA would also have understood that having two adjacent epitaxial structures merge would cause a short, whereas having the epitaxial structures spaced apart, as claimed in the ’193 patent, would not. Thus, a POSITA would not have been motivated to combine Kelly and Murthy as proposed by the Petition’s second Kelly-Murthy combination because it would undercut the design and performance tradeoffs provided by Kelly’s Figure 7C embodiment.

77. Figure 7C thus specifically teaches away from doing what the Petition proposes, which is shrinking and thus separating the epitaxial structures so that they are not merged, especially given that it is intended to provide an alternative to Figures 7A and 7B, where the epitaxial structures are not merged. As such, a POSITA would not have been motivated to modify Kelly’s Figure 7C embodiment

in such a way that would result in the adjacent epitaxial structures not merging together, as that would circumvent the entire purpose of the Figure 7C embodiment.

4. Both Kelly-Murthy Combinations Fail To Disclose Or Render Obvious “At Least Two Caps, Respectively Surrounding The Epitaxial Structures” (Element 1[d])

78. Additionally, both Kelly-Murthy combinations fail to disclose or render obvious “at least two caps, respectively surrounding the epitaxial structures,” as required by element 1[d]. Both of these combinations involve using Kelly’s epitaxial structures. Pet., 51-52. As shown below, Kelly’s FinFET device includes “sidewall spacers 310” on either side of each epitaxial structure:

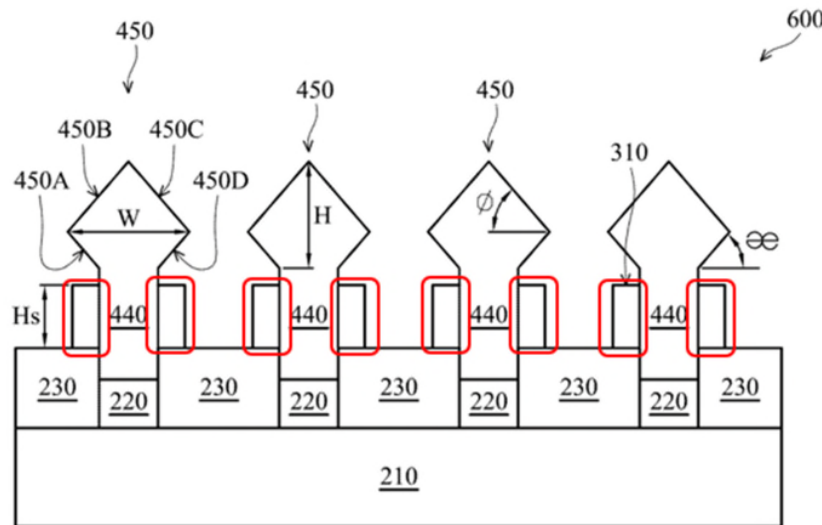
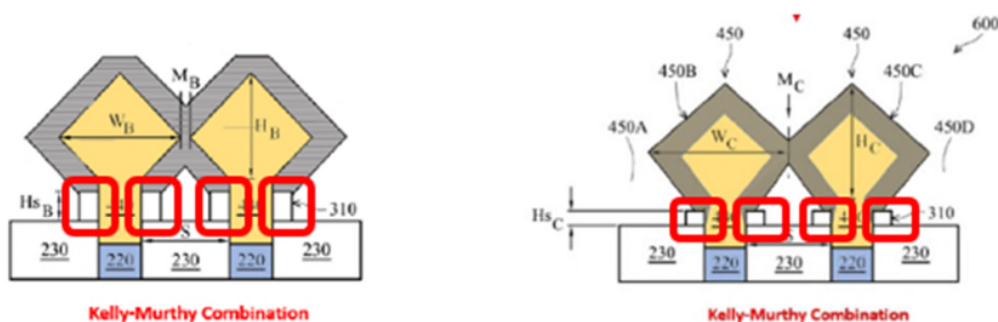


FIG. 6B

Ex. 1009, Fig. 6B (annotated). As such, even if caps were added to Kelly’s epitaxial structures, the caps would still not “respectively surround[] the epitaxial structures,”

as required by element 1[d], because portions of the epitaxial structures would instead be covered by the sidewall spacers. Indeed, the Petition's illustrations of the proposed Kelly-Murthy combinations confirm this fact, showing that the caps do not surround the epitaxial structures due to the placement of the sidewall spacers:



First Kelly-Murthy Combination

Second Kelly-Murthy Combination

Pet., 52-53 (annotated). In contrast, the '193 patent discloses that "[d]uring the epitaxial growth process for the silicon cap 68, the silicon cap 68 continuously grows on the surface of each epitaxial structure 66 and gradually fills up the space between two adjacent epitaxial structures 66 until two adjacent silicon caps 68 merge together as shown in FIG. 7." Ex. 1001, 6:1-6. As shown in Figure 7 below, the claimed semiconductor device does not include spacers on the sides of the epitaxial structures, allowing the caps to grow from the entirety of the exposed surface of the epitaxial structures and surround the epitaxial structures.

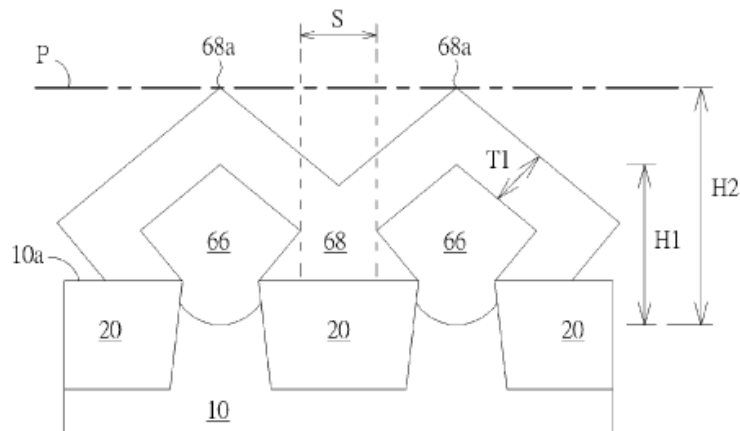


FIG. 7

Ex. 1001, Fig. 7. Accordingly, neither Kelly-Murthy combination discloses or renders obvious “at least two caps, respectively surrounding the epitaxial structures,” as required by element 1[d].¹

5. Ground 4 Fails For The Same Reasons As Ground 3

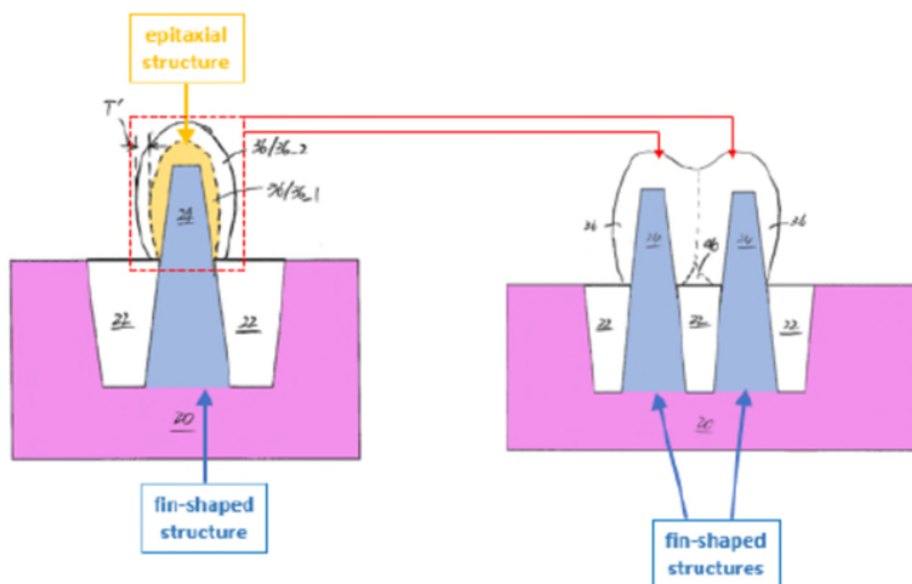
79. Ground 4 adds the Liaw reference to address an additional limitation of dependent claim 11, which depends from independent claim 1. Pet., 90. Ground 4 does not provide any further analysis regarding claim 1. Pet., 90-97. Thus, Ground 4 fails for the same reasons as Ground 3.

¹ Kelly’s spacers 310 are not to be confused with the gate spacers 40 of the ‘193 patent. The spacers 40 of the ‘193 patent run alongside the gate, perpendicular to the fins. The spacers 310 in Kelly run alongside the fins, *perpendicular* to the gates. Unlike Kelly’s spacers 310, the spacers of the ‘193 patent are not present alongside the epitaxy at the source/drains outside of the gates and any gate spacers and, therefore, do not surround the epitaxy.

C. Ground 5

1. Su Does Not Render Obvious Elements 1[c] and 1[d]

80. The Petition alleges that “[a] POSITA would have been motivated to combine Su’s multi-layer epitaxial structure teachings with the multi-fin embodiment, as illustrated in the figures below.” Pet., 104.



Su, Figures 7 (left), 9 (right)

Pet., 105. According to the Petition, Su’s “multi-layer epitaxial structure” (illustrated in Fig. 7) includes both the claimed “epitaxial structures” and the claimed “caps” because the inner layer is the “epitaxial structure” and the outer layer is the “cap.” Pet., 103-104.

81. First, a POSITA would not have been motivated to combine Su's Figure 7 with Figure 9, because they represent embodiments that are incompatible with one another. Su explains that "FIGS. 3 through 8 are a perspective view and cross-sectional views of intermediate stages in the manufacturing of a FinFET in accordance with an embodiment." Ex. 1007, ¶ [0010]. That is, Su's Figures 3 through 8 illustrate a specific embodiment of a process of forming an epitaxial structure on a fin. With respect to this embodiment, Su states that "FIG. 8 illustrates the formation of a single-fin FinFET, *wherein epitaxy layer 36 grown from one fin 24 does not merge with the epitaxy layer grown from other fins.*" Ex. 1007, ¶ [0025] (emphasis added). Thus, Su explicitly states that in its Figure 7 embodiment, its epitaxial layers 36 *do not merge* with epitaxy layers from other fins. In contrast, Su states that "FIG. 9 illustrates that epitaxy layers 36 grown from neighboring fins 24 merge with each other to form a single epitaxy region." Ex. 1007, ¶ [0025]. As such, the Petition essentially argues that a POSITA would have been motivated to combine two wholly incompatible embodiments: one in which epitaxy regions do not merge with another in which epitaxy regions do merge.

82. Additionally, Su fails to render obvious elements 1[c] and 1[d] because the Petition's explanation for why the alleged combination would result in "spaced apart" epitaxial structures and "merged" caps makes no sense. The Petition alleges

that, in the merged image of Figure 9, only the outermost layers 36_2 are merged and the inner layers, 36_1 are not. Pet., 109. But Su does not say that. The Petition alleges that inner layers 36_1 are not merged because “[a] POSITA would understand if adjacent epitaxy layers 36_1 were allowed to merge before formation of the ‘cap’ epitaxy layer 36_2, they could no longer be etched back to a rounded profile (e.g., be shaped like an ellipse) as originally intended by Su; and such merging of the outer surfaces of adjacent epitaxy layers 36_1 would form substantial voids between the merged epitaxy layers 36_1 and the STI, which Su aims to mitigate, if not eliminate.” Pet., 109-110.

83. The Petition’s allegation that “if adjacent epitaxy layers 36_1 were allowed to merge before formation of the ‘cap’ epitaxy layer 36_2, they could no longer be etched back to a rounded profile (e.g., be shaped like an ellipse) as originally intended by Su” is incorrect. If the inner layers 36_1 were allowed to merge before the formation of the outer layers 36_2, the outer layers could still be etched into a rounded shape.

84. Moreover, both of these alleged issues (“could no longer be etched back to a rounded profile” and “form substantial voids”), even if true, would be a problem for the outermost layer, 36_2, just as much as they would for the inner layer, 36_1.

First, as shown in Su's Figures 6 and 7, the growth of epitaxy layer 36_2 is in a pentagonal shape (Fig. 6) and is etched into a rounded shape (Fig. 7):

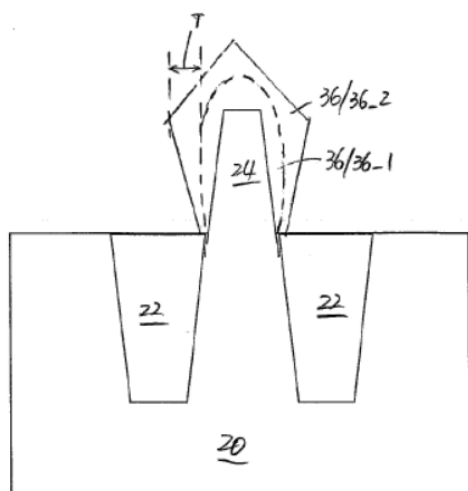


Fig. 6

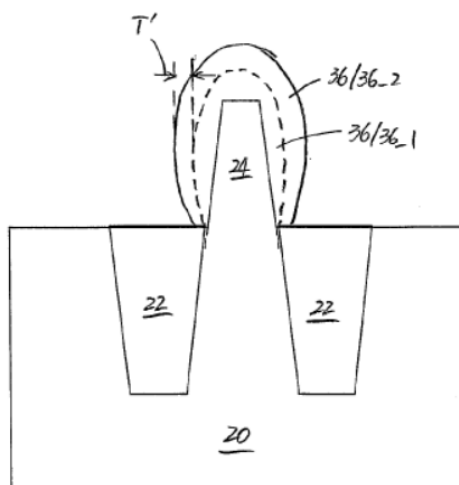


Fig. 7

Ex. 1007, Figs. 6 and 7. Specifically, Su discloses that:

FIGS. 6 and 7 illustrate the structure results from the second deposition-etch cycle. In FIG. 6, epitaxy layer 36_2 is epitaxially grown on the remaining portion of epitaxy layer 36_1.... In an embodiment, in the deposition step in each of the deposition-etch cycles, the thickness of the added portion of the epitaxy layer is denoted as T (refer to FIG. 6). After the etch step, the thickness of the added portion of epitaxy layer 36 is reduced to T' (refer to FIG. 7). The ratio of T'/T reflects the percentage of epitaxy layer 36 removed in the etch step.

Ex. 1007, ¶¶ [0022]-[0023]. As such, the Petition’s allegation that “[a] POSITA would understand if adjacent epitaxy layers 36_1 were allowed to merge before formation of the ‘cap’ epitaxy layer 36_2, they could no longer be etched back to a rounded profile” from the pentagonal shape makes no sense, because this would apply equally to epitaxy layers 36_2 if *they* were allowed to merge. And so the Petition’s reasoning is self-defeating. If the outer layers 36_2 can be merged (as required by the claims) and still “be etched back to a rounded profile,” then so can the inner layers 36_1 (as prohibited by the claims), and absent any description that they are not merged, there is no reason to think they are not, certainly not the Petition’s logic.

85. **Second**, as shown in Su’s Figure 9, allowing adjacent epitaxy layers 36 to merge will result in the formation of void 46:

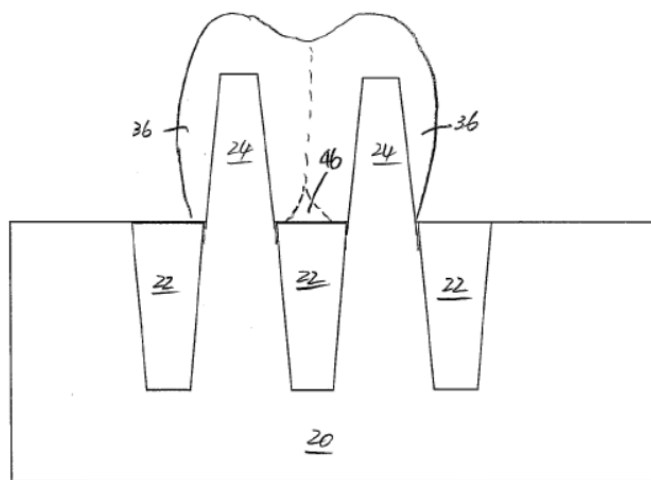
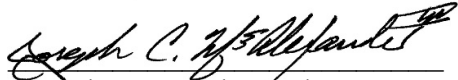


Fig. 9

Ex. 1007, Fig. 9. Whether the epitaxial structures merge before or after the second epitaxy layer 36_2 is grown does not affect whether the void is formed. As such, the Petition's allegation that "merging of the outer surfaces of adjacent epitaxy layers 36_1 would form substantial voids" is misguided, because that would apply equally if epitaxy layers 36_2 were allowed to merge, and would be reduced if 36_1 additionally merged.

86. Thus, the Petition fails to set forth any factual basis for why the proposed modification would result in "spaced apart" epitaxial structures and "merged" caps, as required by elements 1[c] and 1[d]. Thus, Ground 5 fails.

Dated: November 25, 2025



Joseph C. McAlexander, III