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CL480PC MPEG-1 System Decoder

The CL480PC is the newest member of the PlayCD family of MPEG-1 audio/video decoders. Based on a common silicon device, the products in the PlayCD family target specific consumer-oriented applications such as portable VideoCD players and multimedia add-in cards for personal computers. Downloadable microcode implements the target application in the PlayCD family.

In October 1994, C-Cube introduced the CL480VCD, the first member of the PlayCD family, for VideoCD applications. With the introduction of the CL480PC, C-Cube enables the development of the next generation of multimedia add-in cards for personal computers in both the home and business environments. The CL480PC includes the features that developers need to simplify system design and shorten the time to market.

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8.1 Features

The main features of the CL480PC include the following:

- Broad standards support, including OM-1, Microsoft Win95, VideoCD 2.0 and 1.1, Karaoke CD 1.0 and CD-i Green Book linear play
- Highly integrated architecture:
  - Video decoding (NTSC and PAL)
  - Audio decoding
  - Full audio/video synchronization
  - System-layer demultiplexing
- Optimized for low overall system cost:
  - Tunable interfaces allow developers to program audio and video modes
  - Only 4 Mbits of 80-ns DRAM required for all operating features
  - Glueless interface to DRAM and video and audio DACs
- Outstanding video and audio quality:
  - Dedicated post-processing unit includes multitap horizontal and vertical filtering
  - Support for high-resolution still images up to 704 x 576 (VideoCD 2.0)
  - Advanced error concealment greatly improves audio and video quality
- Suitable for portable use:
  - Low-voltage operation (2.7 to 3.6 volts)
  - Low power consumption (less than one watt at 3.3 volts)
  - Mixed 5/3.3 volt operation
  - Packaged in a 128-pin, small-outline PQFP (18mm x 18mm body size)
- Decoding and synchronization of SIF-resolution MPEG video and two channels (one stream) of MPEG Layer 1 or 2 audio
  - Resolutions include 352 x 240 at 30 Hz, 352 x 288 at 25 Hz, and 384 x 240 at 24 Hz
  - Audio sample rates include 32, 44.1 and 48 kHz
- Extensive developer support:
  - Complete documentation
  - Microcode application program interface (API) includes high-level commands such as Play, Pause, SlowMotion, and Scan

8.2 Functional Overview

The CL480PC decodes audio and video using a combination of hardwired co-processors and a programmable RISC CPU (see Figure 8-1).

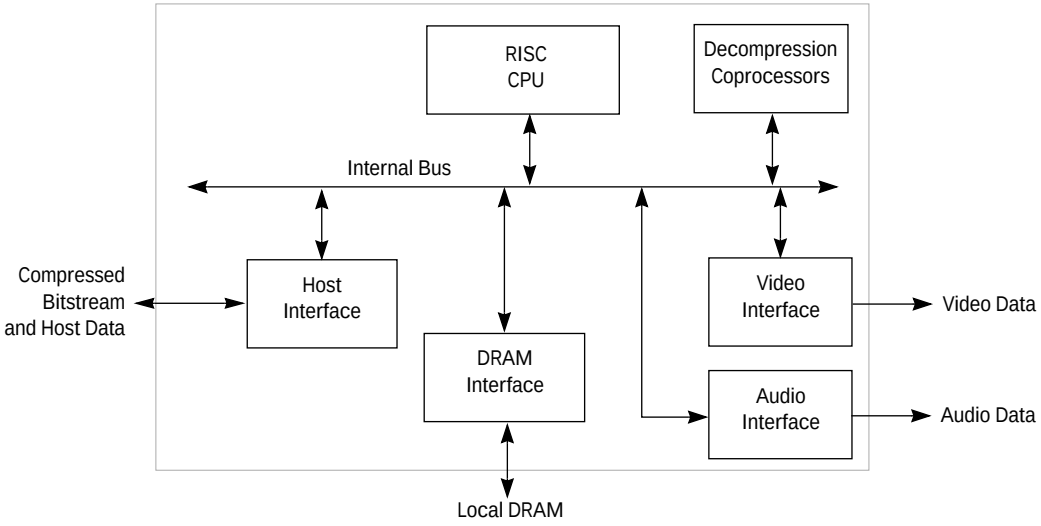

Figure 8-1 CL480PC BIock Diagram

The coprocessors contain special-purpose logic to efficiently perform operations such as Huffman decoding. The RISC CPU is a general-purpose processor that controls the coprocessors and assists in the decoding process.

The microcode for the CPU is stored in DRAM and is loaded into on-chip memory as needed. During power-up, the microcode is loaded into DRAM by the host processor.

The CL480PC receives an MPEG-1 system stream from its host interface. The host controls the CL480PC by sending high-level commands (see Table 8-1) to a command FIFO in the CL480PC's DRAM. After being given the Play command, the CL480PC can decode MPEG audio and video without additional control.

8.2.1 Host Interface

The CL480PC's host interface is an eight-bit data bus that minimizes pins while allowing the host to access DRAM, the coded-data input FIFO, and on-

chip registers. These accesses are performed by writing the selected internal address to a series of three, one-byte host address registers. Data is then read from or written to two, one-byte data registers (All internal transactions are 16 bits wide).

The host interface features an autoincrement mode for accessing sequential DRAM locations. This mode allows fast transfers of data without having to update the target address. The CL480PC also contains a pin (CFLEVEL) that signals when the coded data FIFO has room for more compressed data.

8.2.2 DRAM Interface

The DRAM interface provides a glueless interface between the CL480PC and external memory. It connects directly to 80-ns, fast-page-mode DRAM, which is typically either one 256K x 16 DRAM or four 256K x 4 DRAM's.

8.2.3 Video Interface

The video interface performs both horizontal and (optionally) vertical interpolation of decoded video. It accepts decompressed video data from the local DRAM and outputs it in these modes:

- 24-bit RGB mode (formatted as RGB-RGB)
- 15-bit RGB mode
- 16-bit YCbCr mode (formatted as CbY-CrY)
- 8-bit YCbCr mode (formatted as Cb-Y-Cr-Y)

In YCbCr mode, pixels are output in 4:2:2 format, meaning luminance (Y) has twice the horizontal resolution of chrominance (Cb and Cr). The 15-bit RGB mode is internally dithered from the original 24-bit data.

8.2.4 Audio Interface

The audio interface outputs decoded audio samples in bit-serial format and has a left/right signal to indicate which channel is being output. The polarity of the left/right signal and the order and number of bits per audio sample are programmable so that any of the popular stereo audio DACs can be used.

8.3 The PC Microcode

The microcode for the CL480PC is stored in DRAM and is loaded into on-chip memory as needed. During power-up, the microcode is written by a host into the CL480.

Table 8-1 lists the high-level commands that are supported by the CL480PC. These commands are used by external devices to control the operation of the CL480.

Table 8-1 CL480PC Command Summary

Command	Function
Play	Decode sand displays at normal rate
SlowMotion	Decodes and displays at slower rate
SingleStep	Decodes and displays next single picture
Scan	Decodes and displays next I-picture
Replay	Restarts the previous Play command
DisplayStill	Decodes/displays hi-res. still picture w/ audio
DisplayDigest	Decodes a single I-picture digest display
DisplayDigest(start)	Same as above but specifies starting point
Pause	Freezes display and decoding process
Freeze	Freezes display but continues audio decoding
SetStreams	Selects which system streams to decode
SetVideoFormat	Sets format to NTSC, PAL, or progressive
Abort	Sets processing state to IDLE
InquireBufferEmptiness	Measures data in bitstream buffers
Reset	Initializes the CL480PC and its microcode

8.4 External Interface

The signals that comprise the external interface to the CL480PC are shown in Figure 8-2 and summarized in Table 8-2. Note that the pinout for the CL480PC is identical to that of the CL480VCD (see Figure 7-2) with these exceptions:

- The $\overline{\text{MCE}}$[1:0] and MA[18:10] signals are deleted in the CL480PC.
- The ROM_ENA signal is deleted in the CL480PC.
- The CD interface signals are deleted in the CL480PC.

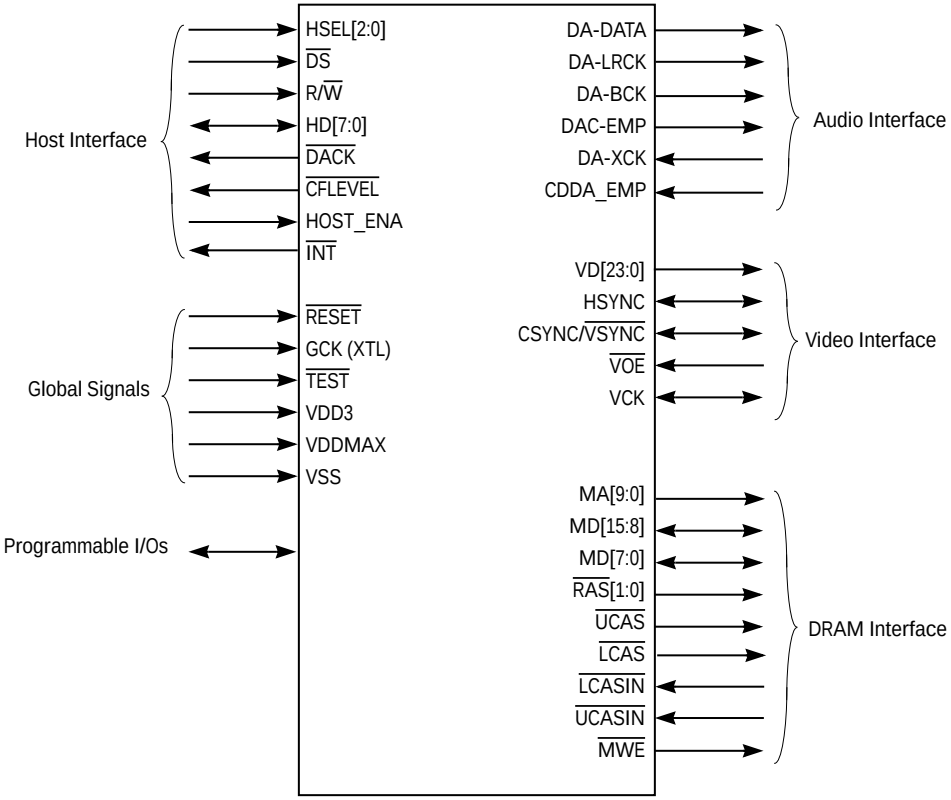

Figure 8-2 CL480PC, External Interface Signals

Table 8-2 CL480PC, Pin Descriptions

Mnemonic	Description	I/O
Host Interface		
HSEL[2:0]	Host address bus	I
DS	Data strobe	I
R/W	Host data bus	I
HD[7:0]	Read/write	I/O
DTACK	Host data acknowledge	O
CFLEVEL	Coded data FIFO level status	O
HOST_ENA	Host enable	I
INT	Interrupt request	O

Table 8-2 CL480PC, Pin Descriptions (Continued)

Mnemonic	Description	I/O
DRAM Interface		
MA[9:0]	Memory address bus	O
MD[15:0]	Memory data bus	I/O
$\overline{\text{RAS}}$[1:0]	Row-address strobes	O
$\overline{\text{UCAS}}$, $\overline{\text{LCAS}}$	Upper and lower column address strobes	O
$\overline{\text{UCASIN}}$, $\overline{\text{LCASIN}}$	Upper and lower data latch enable	I
$\overline{\text{MWE}}$	Write enable	O
ROM_ENA	Boot ROM enable	I
Video Interface		
VD[23:0]	Pixel data bus	O
$\overline{\text{HSYNC}}$	Horizontal synchronization	I/O
$\overline{\text{VSYNC}}$	Vertical synchronization[1]	I/O
$\overline{\text{VOE}}$	Video output enable	I
VCK	Video clock	I/O
Audio Interface		
DA-DATA	Audio data	O
DA-LRCK	Audio left-right clock	O
DA-BCK	Audio bit clock	O
DAC_EMP	Output emphasis flag	O
DA-XCK	External audio frequency clock	I
CDDA-EMP	Input emphasis flag	I
Global Interface		
$\overline{\text{RESET}}$	Hardware reset	I
GCK	Global clock	I
$\overline{\text{TEST}}$	Test mode	I
VDD3, VSS, VDDMAX	Power connections	I

1. $\overline{\text{VSYNC}}$ can also be used as the composite sync signal, CSYNC.

8.5 Typical Application

Figure 8-3 shows the CL480PC as it can be used in a typical multimedia plug-in PC board application.

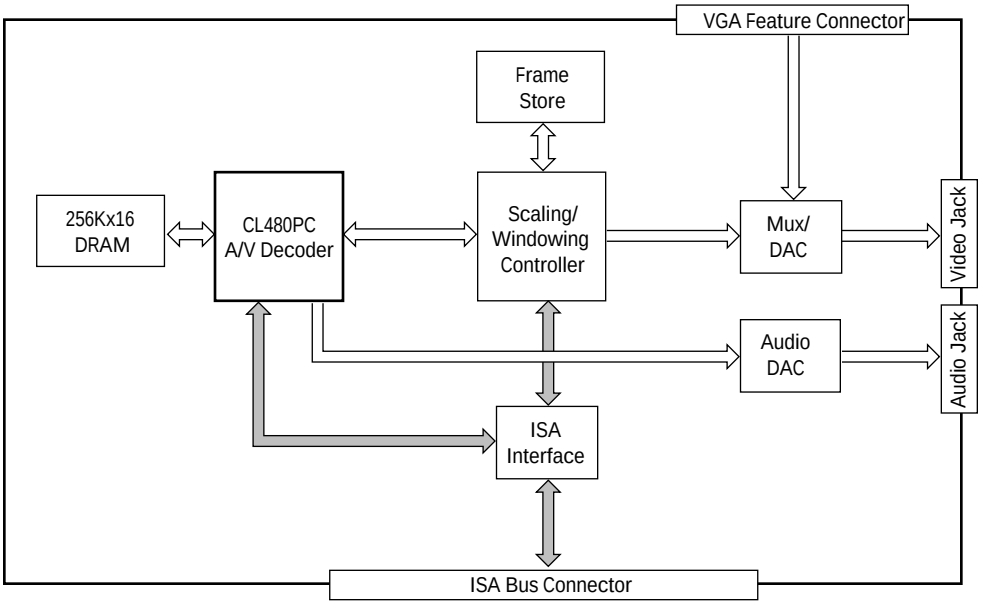

Figure 8-3 CL480PC in Typical Personal Computer Product