

Filed on behalf of:

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Petitioner

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UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE PATENT TRIAL AND APPEAL BOARD

UNITED MICROELECTRONICS CORPORATION,
AND
UMC GROUP (USA),
Petitioner,

v.

ADVANCED INTEGRATED CIRCUIT PROCESS LLC,
Patent Owner.

Case IPR2025-01076
U.S. Patent No. 7,579,227

**PETITION FOR *INTER PARTES* REVIEW OF
U.S. PATENT No. 7,579,227
UNDER 35 U.S.C. §§ 311, 312 AND 37 C.F.R. § 42.104**

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EXHIBIT LIST

Exhibit No.	Description
1001	U.S. Patent No. 7,579,227 to Hirase, et al. (“the ’227 patent”)
1002	File History of U.S. Patent No. 7,579,227 (“’227 File History”)
1003-1008	RESERVED
1009	U.S. Patent Application Publication No. 2003/0025135 A1 to Matsumoto, et al. (“Matsumoto”)
1010	JP2003-258241 to Kajiyama (“JP-Kajiyama”)
1011	Certified Translation of JP2003-258241 to Kajiyama (“Kajiyama”)
1012	U.S. Patent Application Publication No. 2006/0131672 A1 to Wang, et al. (“Wang”)
1013	U.S. Patent Application Publication No. 2005/0051856 A1 to Ono, et al. (“Ono”)
1014-1017	RESERVED
1018	Wilk, G. D., et al., “High-k gate dielectrics: Current status and materials properties considerations,” Journal of Applied Physics, Vol. 89, No. 10, pp. 5243-75, May 15, 2001 (“Wilk”)
1019	U.S. Patent Application Publication No. 2005/0045938 A1 to Mutou, et al. (“Mutou”)
1020-1051	RESERVED
1101	Declaration of Dr. Sanjay Banerjee
1102	Curriculum Vitae of Sanjay Banerjee, PhD

Exhibit No.	Description
1103	“Stress Memorization Technique (SMT) by Selectively Strained-Nitride Capping for Sub-65nm High-Performance Strained-Si Device Application,” Chen et al., 2004 Symposium on VLSI Technology Digest of Technical Papers (2004) (“Chen-2004”)
1104	“35% Drive Current Improvement from Recessed-SiGe Drain Extensions on 37 nm Gate Length PMOS,” Chidambaram et al., 2004 Symposium on VLSI Technology Digest of Technical Papers (2004) (“Chidambaram-2004”)
1105	“Self-Aligned Ultra Thin HfO ₂ CMOS Transistors with High Quality CVD TaN Gate Electrode,” Lee et al., 2002 Symposium On VLSI Technology Digest of Technical Papers (2002) (“Lee-2002”)
1106	“Delaying Forever: Uniaxial Strained Silicon Transistors in a 90nm CMOS Technology,” Mistry et al., 2004 Symposium on VLSI Technology Digest of Technical Papers (2004) (“Mistry-2004”)
1107	“Effects of High-Temperature Forming Gas Anneal on HfO ₂ MOSFET Performance,” Onishi et al., 2002 Symposium On VLSI Technology Digest of Technical Papers (2002) (“Onishi-2002”)
1108	“Low Standby Power CMOS with HfO ₂ Gate Oxide for 100-nm Generation,” 2002 Symposium On VLSI Technology Digest of Technical Papers (2002) (“Pidin-2002”)
1109	“Mobility Enhancement in Strained Si NMOSFETs with HfO ₂ Gate Dielectrics,” Rim et. al., 2002 Symposium On VLSI Technology Digest of Technical Papers (2002) (“Rim-2002”)
1110	“Metal Gate MOSFETs with HfO ₂ Gate Dielectric,” Samavedam et al., 2002 Symposium On VLSI Technology Digest of Technical Papers (2002) (“Samavedam-2002”)

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Exhibit No.	Description
1111	“55nm high mobility SiGe(:C) pMOSFETs with HfO ₂ gate dielectric and TiN metal gate for advanced CMOS,” Weber et al., 2004 Symposium on VLSI Technology Digest of Technical Papers (2004) (“Weber-2004”)
1112-1210	RESERVED
1211	Van Zant, “Microchip Fabrication”(Fifth Ed. 2004) (“Van Zant”)
1212	RESERVED
1213	Houssa, M., “High-k Dielectrics”to Houssa (IOP Publishing Ltd. 2004) (“Houssa”)
1214-1215	RESERVED
1216	“International Technology Roadmap for Semiconductors: Process Integration, Devices, and Structures”(2007 Edition) (“ITRS-PIDS”)
1217-1222	RESERVED
1223	“Semiconductor Devices: Physics and Technology” by Sze (Second Edition, 2002) (“Sze-2002”)
1224-1225	RESERVED
1226	U.S. Patent No. 7,709,331 to Karve, et al. (“Karve”)
1227	U.S. Patent No. 8,017,469 to Luo, et al. (“Luo”)
1228	RESERVED
1229	Wolf, “Silicon Processing for the VLSI Era, Volume 3 – The Submicron MOSFET”(1995) (“Wolf-3”)
1230-1304	RESERVED
1305	Translated Excerpts from JP File History
1306-1322	RESERVED

Exhibit No.	Description
1323	U.S. Patent No. 6,306,712 to Rodder, et al. (“Rodder”)
1324-1332	RESERVED
1333	Plummer, J., et al., “Silicon VLSI Technology: Fundamentals, Practice and Modeling” (Prentice Hall 2000) (“Plummer”)
1334	Wolf, S., “Silicon Processing for the VLSI Era, Volume 4 – Deep-Submicron Process Technology” (Lattice 2002) (“Wolf-4”)
1335-1336	RESERVED
1337	Lee, S. J., et al. “High Quality Ultra Thin CVD HfO ₂ Gate Stack with Poly-Si Gate Electrode,” Digest of International Electron Devices Meeting, pp. 31-34, Dec. 10-13, 2000 (“Lee-2000”)
1338	Campbell, “The Science and Engineering of Microelectronic Fabrication”, Second Edition (2001) (“Campbell”)
1339	RESERVED
1340	Japanese Patent Publication JP2005-064190 to Ono with certified translation (“JP-Ono”)
1341	N. Weste and D. Harris, “CMOS VLSI Design: A Circuits and Systems Perspective”, Third Edition (Pearson/Addison Wesley, 2005) (“Weste”)
1342-1348	RESERVED
1349	Lee, B.H., et al., “Ultrathin Hafnium Oxide with Low Leakage and Excellent Reliability for Alternative Gate Dielectric Application,” Digest of International Electron Devices Meeting, pp. 133-36, Dec. 5-8, 1999 (“Lee-1999”)
1350-1405	RESERVED
1406	U.S. Patent Application Publication No. 2007/0249069 A1 to Alvarez et al. (“Alvarez”)

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Exhibit No.	Description
1407-1412	RESERVED
1413	S.M. Sze, Physics of Semiconductor Devices (2d ed. 1981) (excerpted) ("Sze-1981")
1414-1418	RESERVED
1419	U.S. Patent Application Publication No. 2006/0286729 A1 to Kavalieros et al. ("Kavalieros729")
1420-1428	RESERVED
1429	U.S. Patent Application Publication 2004/0262784 A1 to Doris et al. ("Doris")
1430	U.S. Patent No. 6,797,556 B2 to Murthy et al. ("Murthy556")
1431	U.S. Patent Application Publication No. 2007/0134870 A1 to Lee et al. ("Lee870")
1432	U.S. Patent Application Publication No. 2005/0260810 A1 to Cheng et al. ("Cheng810")
1433	U.S. Patent Application Publication No. 2009/0020820 A1 to Baik et al. ("Baik")
1434	U.S. Patent Application Publication No. 2008/0293207 A1 to Koutny et al. ("Koutny")
1435	U.S. Patent Application Publication No. 2010/0075476 A1 to Miyashita ("Miyashita")
1436-1505	RESERVED
1506	U.S. Patent Application Publication 2007/0235823 A1 to Hsu et al. ("Hsu823")

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Exhibit No.	Description
1507-1511	RESERVED
1512	International Technology Roadmap for Semiconductors: Front End Processes (2007 ed.) ("ITRS_FEP")
1513-1515	RESERVED
1515	U.S. Patent Application Publication No. 2006/0022277 A1 to Kavalieros et al. ("Kavalieros277")
1516	K. Mistry, et al., "A 45nm Logic Technology with High-k+Metal Gate Transistors, Strained Silicon, 9 Cu Interconnect Layers, 193nm Dry Patterning, and 100% Pb-Free Packaging," Technical Digest of the of the 2007 IEEE International Electron Devices Meeting (IEDM), pp. 247-50 (Dec. 2007) ("Mistry2007")
1517	K. Mistry, et al., "A 45nm Logic Technology with High-k+Metal Gate Transistors, Strained Silicon, 9 Cu Interconnect Layers, 193nm Dry Patterning, and 100% Pb-Free Packaging," presented at 2007 IEEE International Electron Devices Meeting (IEDM), pp. 1-37 (Dec. 2007) ("Mistry_Presentation")
1518	U.S. Patent No. 6,881,631 B2 to Saito et al. ("Saito631")
1519	U.S. Patent No. 7,812,414 B2 to Hou et al. ("Hou")
1520	U.S. Patent Application Publication No. 2005/0258468 A1 to Colombo et al. ("Colombo")
1521	U.S. Patent No. 6,849,511 B2 to Iriyama et al. ("Iriyama")
1522	U.S. Patent Application Publication No. 2002/0037615 A1 to Matsuo ("Matsuo")

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Exhibit No.	Description
1523	S.E. Thompson et al., “A 90-nm Logic Technology Featuring Strained Silicon,” IEEE Transactions on Electron Devices, vol. 51. No. 11, pp. 1790-97 (Nov. 2004) (“Thompson-2004”)
1524	Y. Sun et al., “Physics of Strain Effects in Semiconductors and Metal-Oxide-Semiconductor Field-Effect Transistors,” Journal of Applied Physics, vol. 101, Art. No. 104503 (22 pages) (May 2007) (“Sun-2007”)
1525	D. James, “2004 –The Year of 90-nm: A Review of 90 nm Devices,” 2005 IEEE/SEMI Advanced Semiconductor Manufacturing Conference, pp. 72-77 (2005) (“James”)
1526	U.S. Patent Application Publication No. 2006/0148151 A1 to Murthy et al. (“Murthy151”)
1527	U.S. Patent Application Publication No. 2004/0262683 A1 to Bohr et al. (“Bohr”)
1528	P. Morin et al., “Extensive Study of the Correlation between Contact Etch Stop Nitride Material Properties and Negative Bias Temperature Instabilities Measured in pMOSFETS,” ECS Transactions, vol. 6, no. 3, pp. 355-69 (2007) (“Morin-2007”)
1529	U.S. Patent Application Publication No. 2005/0170104 A1 to Jung et al. (“Jung”)
1530	RESERVED
1531	U.S. Patent Application Publication No. 2008/0145984 A1 to Ke et al. (“Ke”)

Exhibit No.	Description
1532	P. Bai et al., “A 65nm Logic Technology Featuring 35nm Gate Lengths, Enhanced Channel Strain, 8 Cu Interconnect Layers, Low-k ILD and 0.57 μm^2 SRAM Cell,” Technical Digest of the 2004 IEEE International Electron Devices Meeting (IEDM), pp. 657-60 (Dec. 2004) (“Bai-2004”)

Under 35 U.S.C. §§311, 312 and 37 C.F.R. §42.104, United Microelectronics Corporation and UMC Group (USA) (collectively, “Petitioner”) request *inter partes* review (“IPR”) of claims 1-2, 7-8, and 14 (“Challenged Claims”) of U.S. Patent No. 7,579,227 (Ex.1001, “the ’227 patent”).

I. Introduction

The ’227 patent relates “to techniques for improving the driving power and reliability of a MISFET [metal insulator semiconductor field-effect transistor]” by (1) extending a high-k gate insulating film from under the gate electrode to under a sidewall and (2) making the high-k film thicker under the gate electrode than under the sidewall. Ex.1001, 1:8-14, 2:1-10, 2:31-38. These basic concepts were known before the ’227 patent, a fact corroborated by the Examiner and acquiesced to by the Applicant during Japanese prosecution. Petitioner, supported by the Declaration of Dr. Sanjay Banerjee (Ex.1101), demonstrates the Challenged Claims are unpatentable.

II. Certification of Grounds for Standing

Petitioner certifies under 37 C.F.R. §42.104(a) that the ’227 patent is available for IPR and Petitioner is not barred or estopped from requesting IPR of the Challenged Claims on the Grounds identified in this Petition.

III. Identification of Challenge and Requested Relief

A. Prior Art

The '227 patent was filed on July 24, 2006 and claims priority to Japan Patent Application No. JP2005- 227457 (“JP application”), filed August 5, 2005. Petitioner does not acquiesce the '227 patent is entitled to priority of the JP application. Regardless, each applied reference identified below was filed or published before August 5, 2005 and is prior art to the '227 patent.

1. U.S. Patent Application Publication No. 2003/0025135 A1 to Matsumoto, et al. (“Matsumoto”; Ex.1009), published February 6, 2003, is prior art under 35 U.S.C. §102(b).¹
2. JP2003-258241 to Kajiyama (“JP-Kajiyama”; Ex.1010), published September 12, 2003, is prior art under 35 U.S.C. §102(b). A certified translation of JP-Kajiyama (“Kajiyama”) is provided as Ex.1011.
3. U.S. Patent Application Publication No. 2006/0131672 A1 to Wang, et al. (“Wang”; Ex.1012), filed April 27, 2005, is prior art under 35 U.S.C. §102(e).
4. U.S. Patent Application Publication No. 2005/0045938 A1 to Mutou, et al. (“Mutou”; Ex.1019), published March 3, 2005, is prior art under 35 U.S.C. §102(b).
5. U.S. Patent Application Publication No. 2005/0051856 A1 to Ono, et al. (“Ono”; Ex.1013), published March 10, 2005, is prior art under 35 U.S.C. §102(b).

¹ Pre-AIA 35 U.S.C. §102 applies.

B. Grounds for Challenge

The specific Grounds of the challenge are set forth below and are supported by the Declaration of Sanjay Banerjee, Ph.D. (Ex.1101).

Ground	Basis	Challenged Claims	Prior Art Reference(s)
I	§103 ²	1-2	Matsumoto (Ex.1009)
II	§103	7-8, 14	Matsumoto (Ex.1009)-Wang (Ex.1012)
III	§103	7-8	Matsumoto (Ex.1009)-Mutou (Ex.1019)
IV	§103	14	Matsumoto (Ex.1009)-Ono (Ex.1013)
V	§102	1-2	Kajiyama (Ex.1010/1011)
VI	§103	14	Kajiyama (Ex.1010/1011)

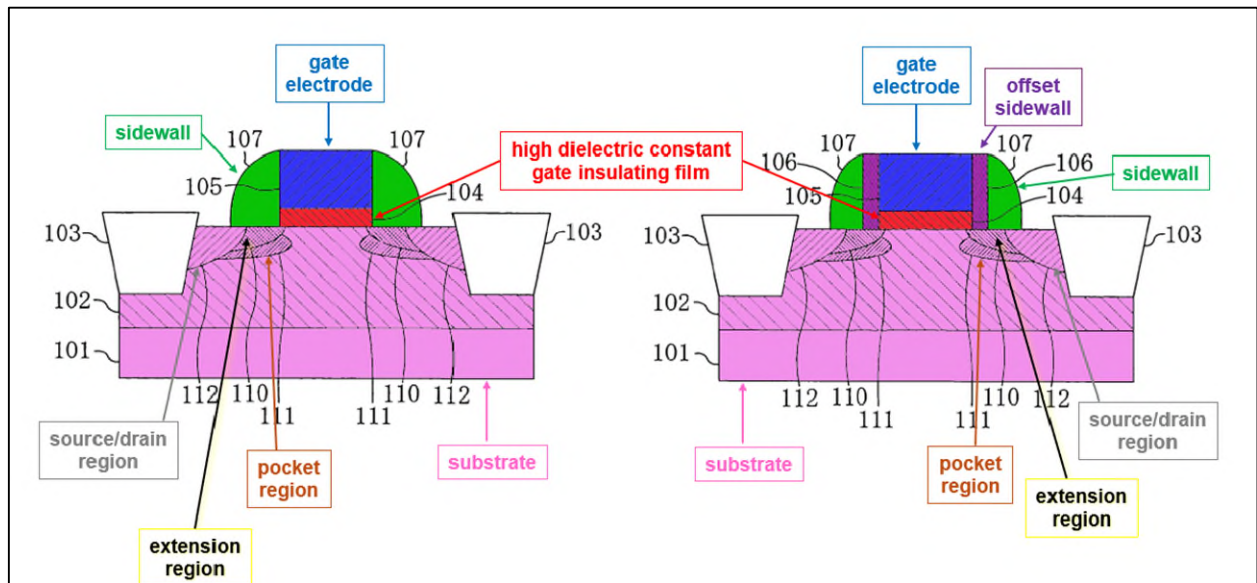
IV. The '227 Patent

A. Applicant Admitted Prior Art (“AAPA”)

The '227 patent recognized that, prior to August 2005, semiconductor devices had used “a high dielectric constant film formed of a Hf based oxide, Al based oxide or the like” as a gate insulating film. Ex.1001, 1:17-25. It describes two exemplary prior art metal insulator semiconductor field-effect transistors (MISFETs), depicted in Figures 16A and 16B (see below), each including a high dielectric constant gate

² Cites to 35 U.S.C. §§102 and 103 are to the pre-America Invents Act (pre-AIA).

insulating film³ 104 (shaded red) interposed between a gate electrode 105 (shaded blue) and the substrate 101. *Id.*, 1:26-38. In the Figure 16A device, an insulating sidewall 107 (shaded green) is formed on each side of gate electrode 105. *Id.*, 1:37-38. In the Figure 16B device, an additional insulating offset sidewall 106 (shaded purple) is interposed between sidewall 107 and gate electrode 105. *Id.*, 1:46-49.



Id., FIG. 16A (left), 16B (right).⁴

In these prior art devices, the “side end portions” of the high-k gate insulating film “are in direct contact with sidewalls.” Ex.1001, 1:56-59. The ’227 patent

³ The terms “gate dielectric” and “gate insulating film” are used interchangeably. The term “high dielectric constant” is also referred to as “high-k” in this Petition and prior art documents.

⁴ All shading and annotations in figures are added, unless otherwise noted.

purports to address issues with this arrangement by extending the high-k film under the “sidewalls to prevent end portions of the [high-k] film from being in contact with the sidewalls.” *Id.*, 2:5-11. It also purports to make the high-k film thicker under the gate than under the sidewalls. *Id.*, 2:31-38.

However, these basic concepts were well-known. *See, e.g.*, §§IV.B.2, IV.D.2, V, IX.

B. Technical Background

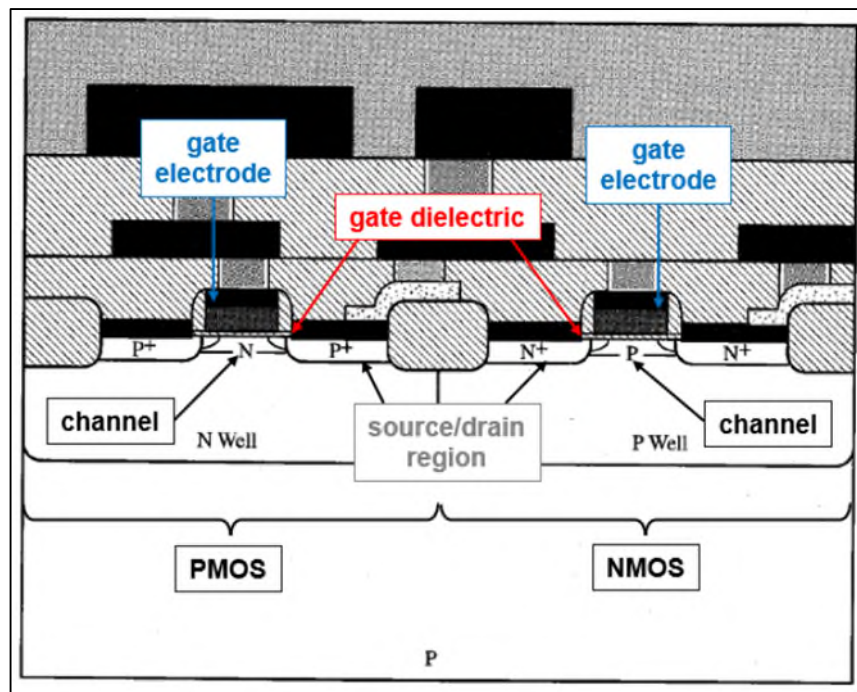
A semiconductor device, at its most basic, exploits the properties of semiconductor materials such as silicon or germanium. Ex.1101, ¶37. Many types of semiconductor devices exist including, *e.g.*, diodes and metal oxide semiconductor (MOS) transistors (*e.g.*, field effect transistors (FETs)). *See e.g., id.*; Ex.1333, 33-41. For ease of discussion, Petitioner describes FET devices in further detail below. A POSITA would understand the basic concepts in §IV.B also apply to other types of semiconductor devices.

1. MISFET/MOSFET

MISFETs⁵ have a **source/drain** for current input/output. Ex.1101, ¶38; Ex.1333, 76-82. MISFETs like the ones at issue here also have a **gate** above a

⁵ The terms “MISFET” and “MOSFET” (“Metal-**Oxide**-Semiconductor Field-Effect Transistor”) are interchangeable. Ex.1101, ¶38)

channel region between the source and drain. Ex.1101, ¶38; Ex.1333, 71-76. The **gate** includes a **gate electrode** and **gate dielectric** (also referred to as a gate insulating film) separating the gate electrode from the channel region. *Id.* Applying voltage to the gate electrode controls the channel region to connect (ON state) or disconnect (OFF state) the source and drain. Ex.1101, ¶38; Ex.1341, 8-9. Generally, source/drain regions are **doped** with either a **p-type** or **n-type** impurity. Ex.1101, ¶39; Ex.1333, 76-82. MISFETs with n-type source/drain regions are called **NMOS**, and MISFETs with p-type source/drain regions are called **PMOS**, as illustrated below. Ex.1101, ¶39; Ex.1333, 13, Fig. 1-11 (below).

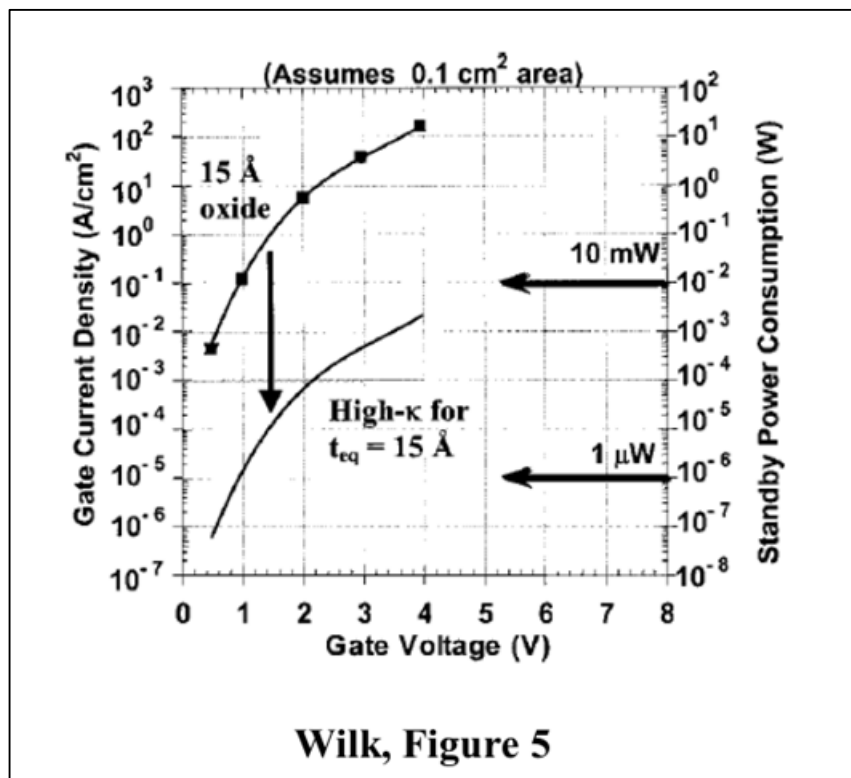


2. Gate Insulating Film

a. Materials

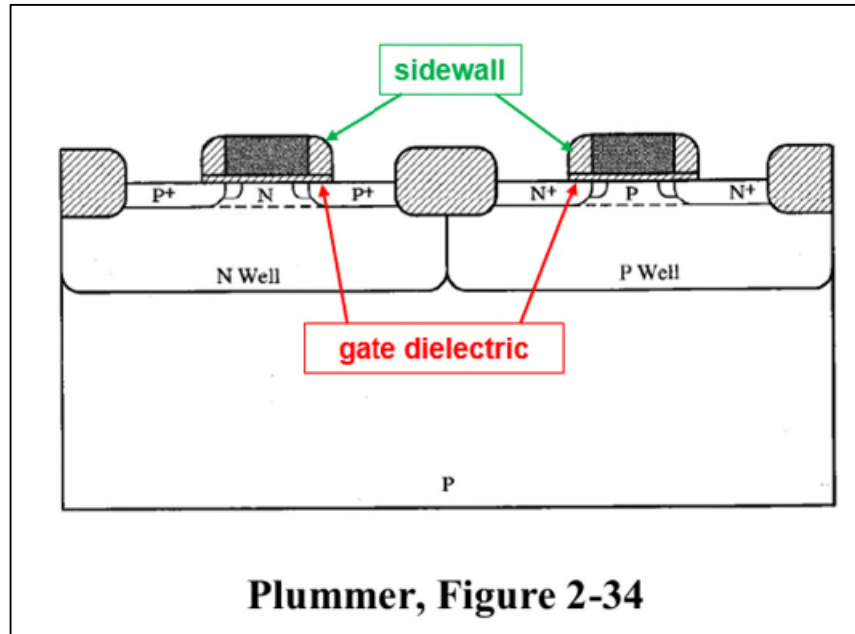
A common feature of a FET is the gate dielectric. Ex.1333, 288. For decades prior to the '227 patent, silicon dioxide (SiO_2) was the primary material used for gate dielectrics in MOSFETs. Ex.1101, ¶50; Ex.1333, 53 (“ SiO_2 is essentially a perfect insulator and provides the needed [electrical] isolation.”); Ex.1213, 3-4. As gate dielectric layers continued to shrink in thickness (*e.g.*, below 1.5 nm), use of SiO_2 became untenable, because the amount of gate-to-channel tunneling leakage-current passing through the gate dielectric prevents the gate electrode from effectively controlling the ON/OFF states of the FET. Ex.1101, ¶¶51-56; Ex.1334, 4-5.

High-k dielectrics, like Hf-based oxides, Ta_2O_5 , or ZrO_2 , replaced SiO_2 to address these challenges. Ex.1101, ¶56; Ex.1334, 146. For example, it was known by 2005 that, as compared to SiO_2 , high-k materials significantly reduce the amount of leakage current and, thus, improve energy efficiency. Ex.1101, ¶¶56-61; Ex.1018, 5250, Fig. 5 (below); Ex.1334, 146-47.



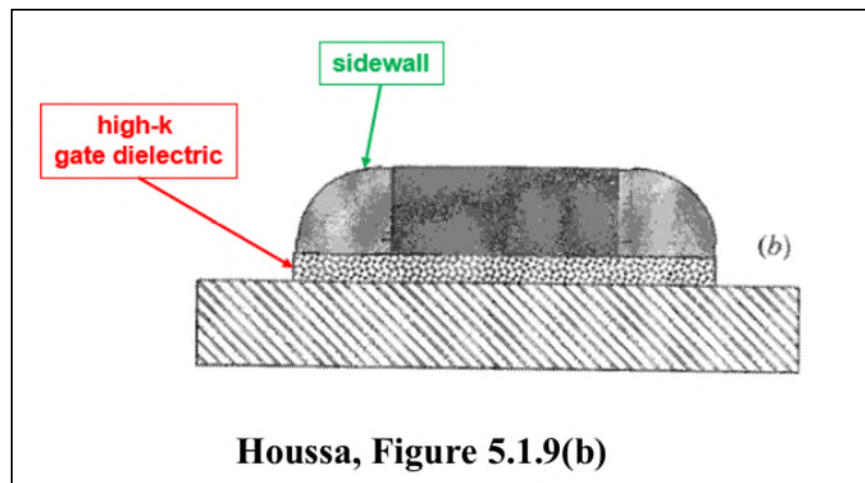
b. Extended Gate Insulating Films

Prior to 2005, it was common practice to extend the gate dielectric from under the gate electrode to under the gate sidewalls. For example, Plummer depicts a CMOS device having an extended gate dielectric in the NMOS and PMOS transistors. Ex.1101, ¶62; Ex.1333, Fig. 2-34 (below), 82-83.

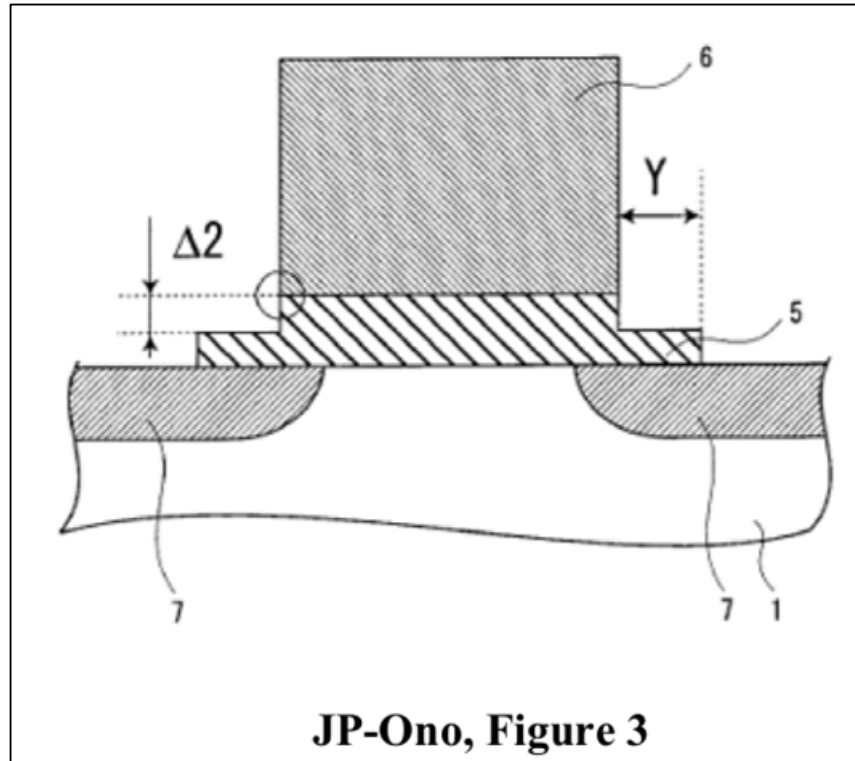


Houssa discloses another example using a high-k material as the gate insulating film that extends from under the gate electrode to under the sidewalls.

Ex.1101, ¶63; Ex.1213, 510, Fig. 5.1.9(b) (below).



JP Publication No. 2005-064190 (“JP-Ono”⁶; Ex.1340), filed two years before the earliest priority date of the ’227 patent, also describes extending the gate dielectric and varying its thickness. Specifically, JP-Ono adjusts both the reduction in thickness of the gate dielectric ($\Delta 2$) outside the gate electrode and the length of the gate dielectric from the outer edge of the gate electrode (Y) (*i.e.*, how far the gate dielectric protrudes from under the gate electrode). Ex.1340, ¶35, Fig. 3 (below); Ex.1101, ¶¶64-68.

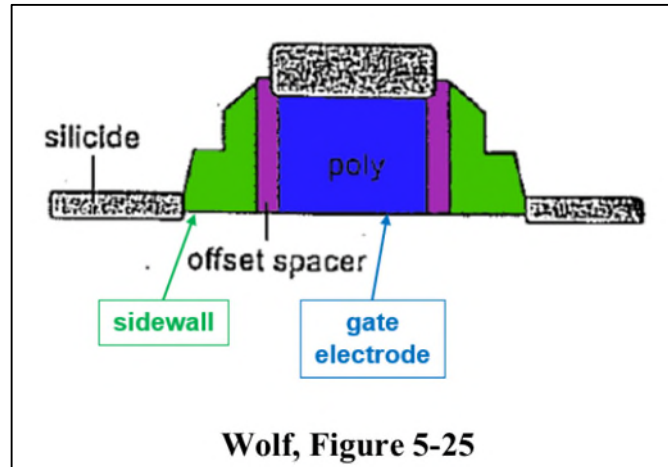


⁶ A certified translation of JP-Ono is included with Ex.1340.

3. Sidewall Structures

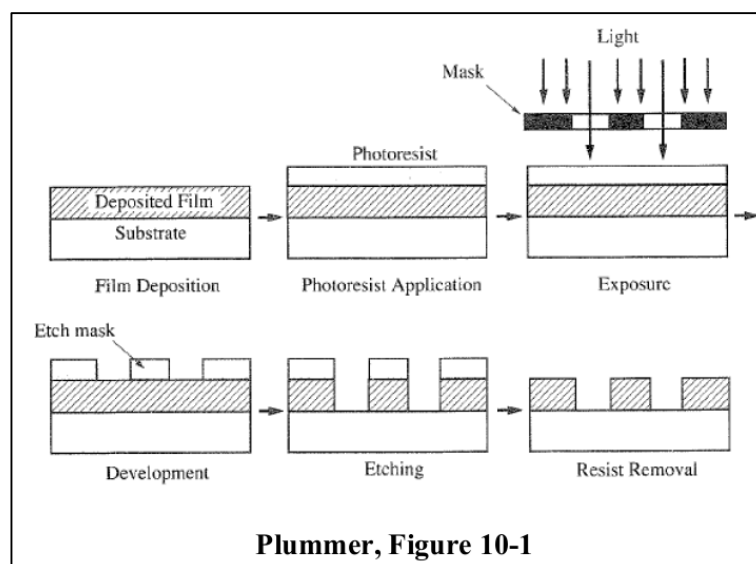
Another common feature of a semiconductor device is sidewalls, vertical insulating structures formed on or proximate to the side surfaces of a gate electrode. Sometimes, the terms “sidewall,” “spacer,” and “sidewall spacer” are used interchangeably. Ex.1101, ¶69. Sidewalls serve a variety of purposes and functions in a semiconductor device such as defining the source/drain region, providing isolation, protecting the gate during subsequent fabrication, and controlling the width of the gate in the gate length direction. *Id.*

As an example, sidewalls may be used for “[c]ontrolling the position of the edge of the SDE [source/drain extension] region with respect to the gate edge” so as to achieve optimal amount of overlap between the SDE and the gate edge. Ex.1334, 217. As shown below, “an offset-spacer is fabricated on the side of the gate after the gate-poly is etched (but before the SDE implant step is carried out ...,” with offset-spacer width “varied from zero (no-spacer) to some upper-bound (e.g., 50-nm)” to achieve optimum device characteristics. *Id.*, 217, Fig. 5-25 (below); Ex.1101, ¶70.

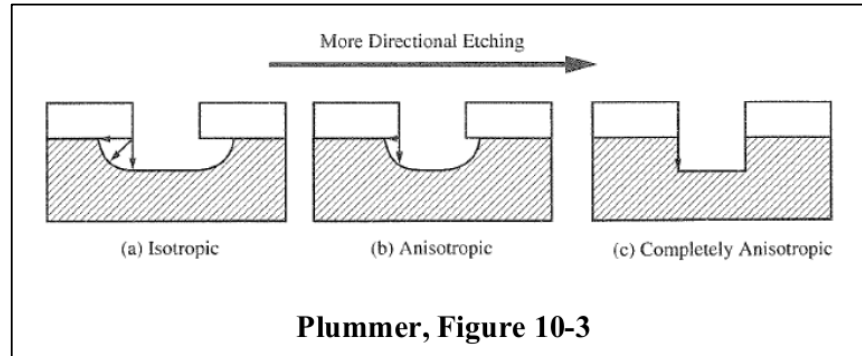


4. Etching Properties

In semiconductor devices, thin films are often first deposited on the wafer surface and then selectively removed by etching to leave the desired pattern of the film. Ex.1101, ¶71; Ex.1333, 609-11. The desired pattern is often defined by placing a mask on the surface before etching; the mask is removed after etching. Ex.1101, ¶71; Ex.1333, 609-10, Fig. 10-1 (below).



Etching is performed in a “wet” or “dry” environment. Ex.1101, ¶73; Ex.1333, 609, 612-37. Wet etching involves the use of liquid etchants (*e.g.*, hydrofluoric acid), whereas dry etching involves the use of gas-phase etchants in a plasma. Ex.1101, ¶73; Ex.1333, 609. Etching processes are also described based on the relative etch rates in different directions. Ex.1101, ¶74; Ex.1333, 610-11. Isotropic etching occurs when the etch rate is the same in all directions, resulting in a semicircular etch profile as shown in Figure 10-3(a) below.



Ex.1333, Fig. 10-3. Most wet chemical etchants etch isotropically. *Id.*, 610-13. Anisotropic etching occurs where there is little or no etching in the lateral direction. *Id.*, 611, Figure 10-3(b), (c) (above). For anisotropic etching, the amount of lateral etching may vary, such that the etched surface may be curved or sloped (*see id.*, Fig. 10-3(b) (above)) to completely vertical (*see id.*, Fig. 10-3(c) (above)). Ex.1101, ¶74.

C. '227 Patent Overview

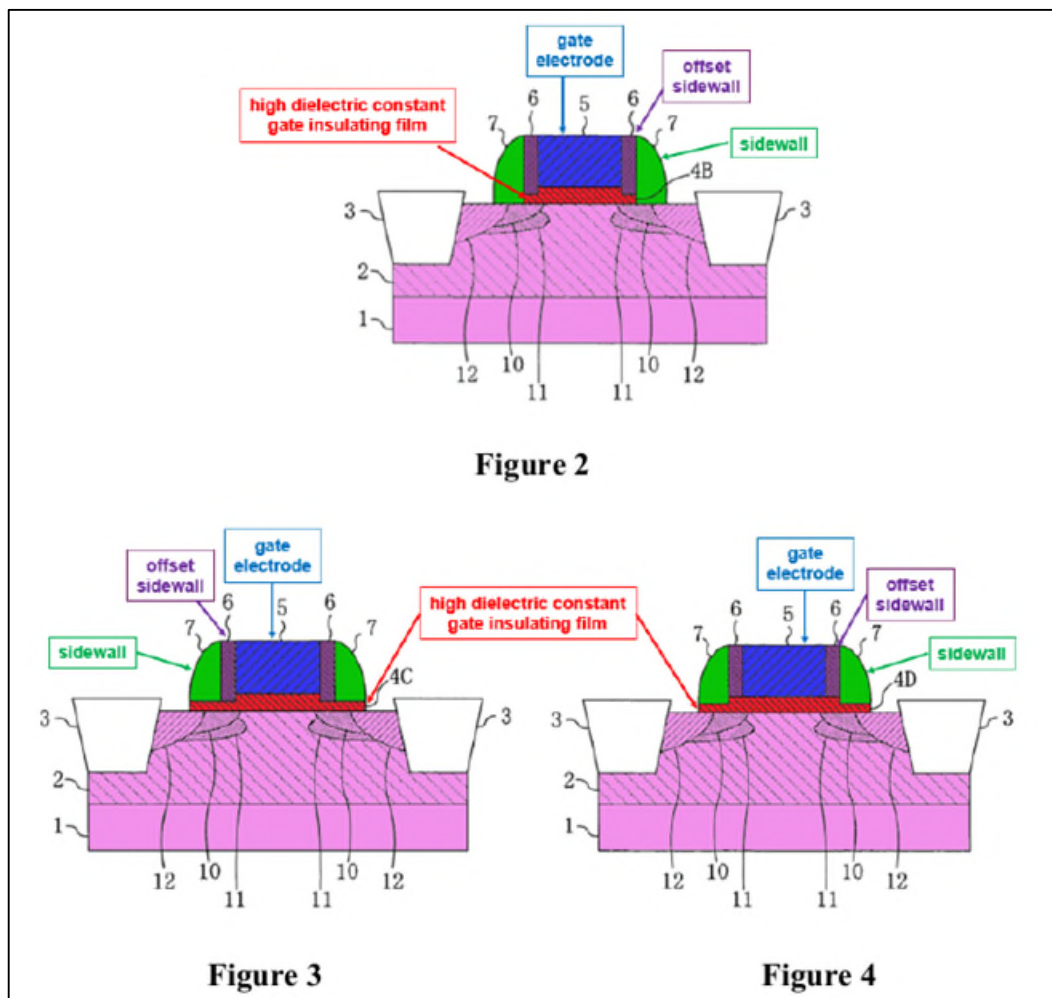
The four semiconductor device embodiments presented in the '227 patent can be separated into two groups—single sidewall devices (first/fourth embodiments) and double sidewall devices (second/third embodiments). The '227 patent's claims

are directed to double sidewall devices and cover different alternatives for varying the thickness of the high-k gate insulating film.

In the second embodiment (*see* Ex.1001, FIG. 2 (below, top)), the high-k gate insulating film (shaded red) extends only under inner (i.e., offset or first) sidewall 6 (shaded purple) and has a smaller thickness under inner sidewall 6 than under gate electrode 5 (shaded blue), corresponding, e.g., to claims 1 and 2. Ex.1001, 7:44-55. In a modification (*see id.*, FIG. 3 (below, bottom-left), the thickness of the high-k gate insulating film is the same under both inner sidewall 6 and outer (i.e., second) sidewall 7 and is thinner under both sidewalls than under gate electrode 5, corresponding to claims 1 and 3.⁷ *Id.*, 8:58-63. In another modification (*see id.*, FIG. 4 (below, bottom-right)), the thickness of the high-k gate insulating film is the same under gate electrode 5 and inner sidewall 6 but is thinner under outer sidewall 7, corresponding to claim 5.⁸ *Id.*, 9:40-51.

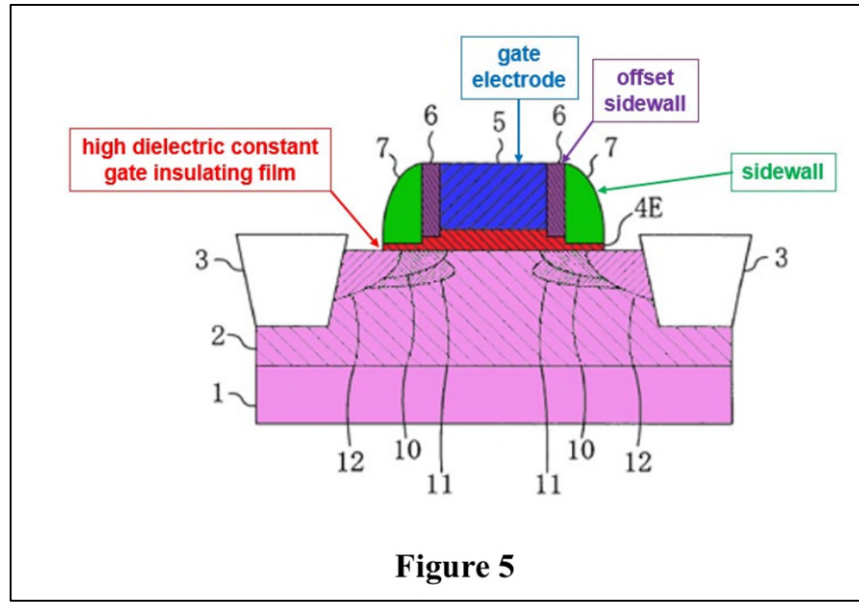
⁷ Claim 3 is not challenged in this IPR.

⁸ Claim 5 is not challenged in this IPR.



In the third embodiment device (see Ex.1001, FIG. 5 (below)), the high-k gate insulating film has declining thicknesses under gate electrode 5, under offset sidewall 6, and under sidewall 7 and corresponds to claims 1 and 4.⁹ *Id.*, 10:49-58.

⁹ Claim 4 is not challenged in this IPR.



D. Prosecution History

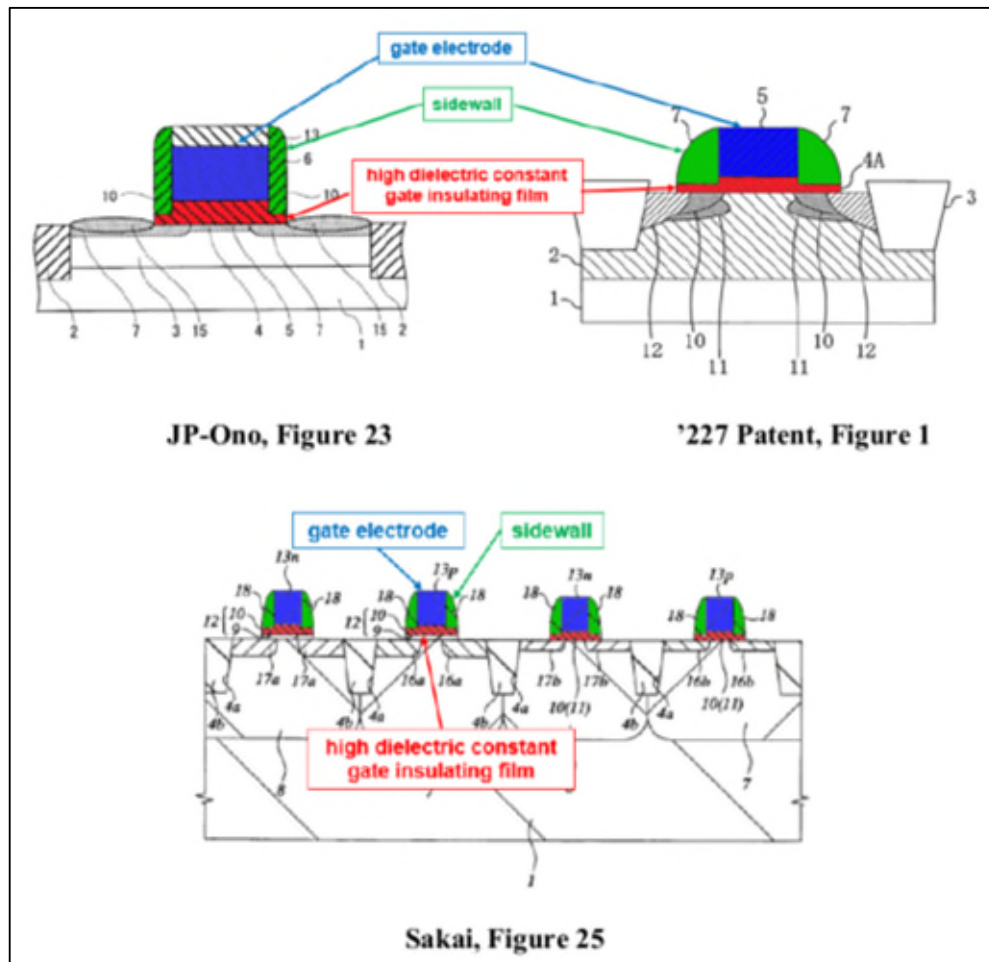
1. '227 Patent

The corresponding U.S. application was filed with one independent device claim reciting a high-k gate insulating film with a smaller thickness under the sidewall than under the gate electrode. Ex.1002, 44. The Examiner rejected this claim as anticipated by U.S. Patent No. 6,992,358 to Hieda et al. Ex.1101, ¶116; Ex.1002, 122-23. In response, Applicant narrowed the claim to recite (1) the sidewall has a “first insulating sidewall” and a “second insulating sidewall,” thus, narrowing the claims to only the double sidewall embodiments, and (2) part of the high-k gate insulating film “under the first insulating sidewall has a smaller thickness than a thickness of part of the” high-k gate film under the gate electrode. Ex.1101, ¶117; Ex.1002, 147-48. Applicant also rewrote pending dependent claim 6 (issued claim

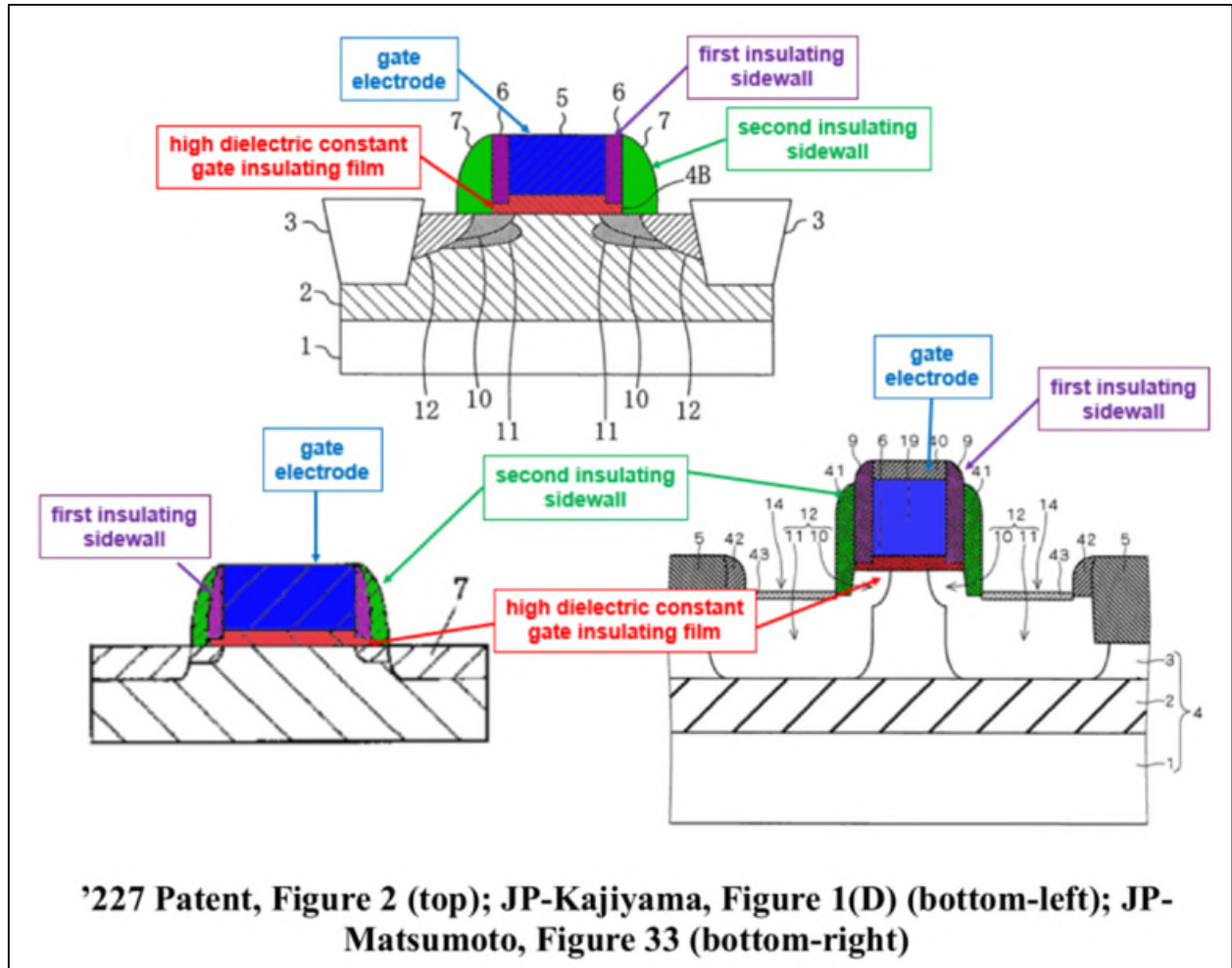
5) into independent form. Ex.1002, 149. The Examiner allowed the amended claims. *Id.*, 162-64.

2. JP Application

The JP priority application was filed with the same device claim originally filed with the counterpart U.S. application. Ex.1305, 1. On September 16, 2011, the JP-Examiner found this claim scope unpatentable, citing JP-Ono discussed above (see Ex.1340, Fig. 23 (below, top-left)) and WO2004/017418 to Sakai, et al. (“Sakai”; see FIG. 25 (below, bottom)), which both teach a high-k gate insulating film with a smaller thickness under the sidewall than under the gate electrode, like e.g., the ’227 patent’s single sidewall embodiments (see Ex.1001, FIG. 1 (below, top-right)). Ex.1305, 4-6.



In response, Applicant narrowed the claim to recite (1) a double sidewall structure with a high-k film having a smaller thickness under a first sidewall than under the gate electrode and (2) extension and source/drain regions. Ex.1305, 8. The JP-Examiner rejected the amended claim based on both JP Application No. 2003-258241 to Kajiyama (“JP-Kajiyama”; Ex.1010, Fig. 1(D) (below, bottom-left)) and JP Application No. 2004-241755 to Matsumoto (“JP-Matsumoto”; Fig. 33 (below, bottom-right)), which each teaches the same basic structure as the '227 patent's Figure 2. Ex.1305, 14-16; *compare* Ex.1001, FIG. 2 (below, top).



In response, Applicant further narrowed the claim to recite the thickness of the high-k gate insulating film under the second sidewall is smaller than the thickness under the first sidewall, which is smaller than the thickness under the gate electrode. Ex.1305, 18. The JP-Examiner allowed the claim based on this amendment. *Id.*, 20.

In short, to secure allowance over the prior art, PO acquiesced during JP prosecution that the scope of at least issued claim 1 of the '227 patent was known in the art.

E. Claim Construction

Petitioner does not believe any claims require construction to resolve the patentability disputes in this proceeding. *See Vivid Techs., Inc. v. Am. Sci. & Eng'g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999).

F. Level of Ordinary Skill in the Art

A POSITA would have had at least a Master's degree in electrical engineering, physics, chemistry, materials science, or related fields, and three years of work experience in semiconductor manufacturing. Ex.1101, ¶¶118-20. Additional graduate education could substitute for work experience, and additional work experience/training could substitute for formal education. *Id.*

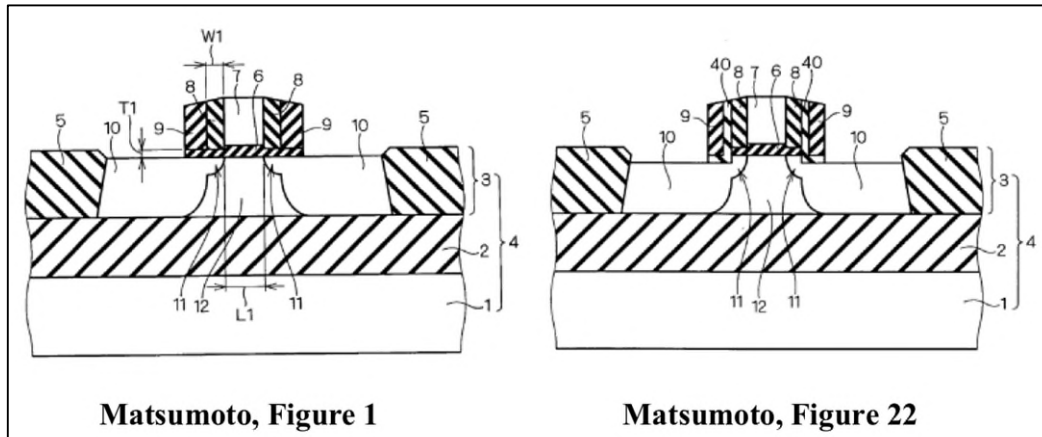
V. GROUND I: Matsumoto Renders Claims 1-2¹⁰ Obvious.

A. Overview

Matsumoto relates “to a semiconductor device” and more specifically to a MOSFET. Ex.1009, ¶2; Ex.1101, ¶124. Matsumoto presents seven embodiments of its semiconductor device. This Petition focuses on Matsumoto's first and fourth embodiment MOSFETs, which each includes a multilayer sidewall structure and a gate insulating film 6 extending from under a gate electrode. In the first embodiment, gate insulating film 6 extends under both films 8 and 9 of the sidewall structure formed on the gate electrode's side surfaces. *See* Ex.1009, ¶¶102-121, FIG. 1 (below,

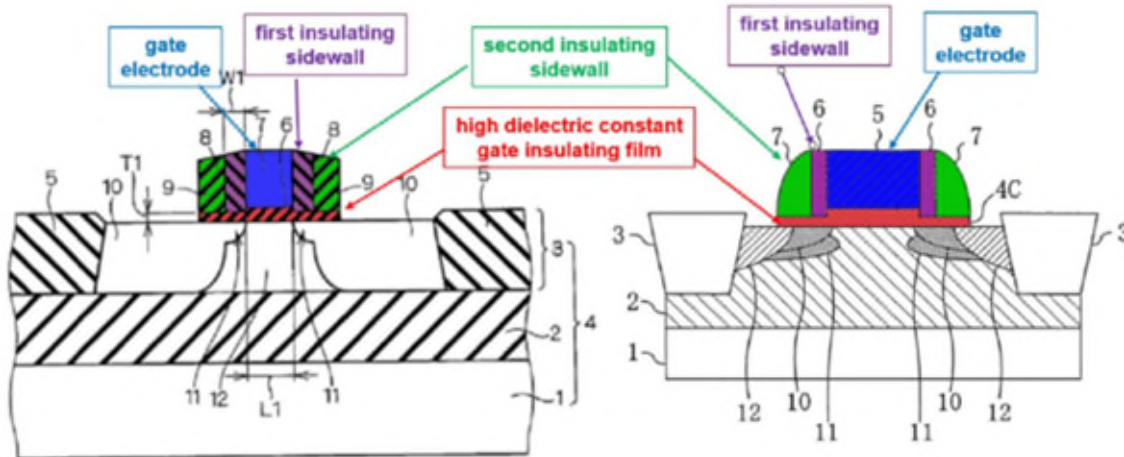
¹⁰ A listing of Challenged Claims is provided in the Appendix.

left). In the fourth embodiment, gate insulating film 6 extends under only film 8 of the sidewall. See *id.*, ¶¶137-140, FIG. 22 (below, right).



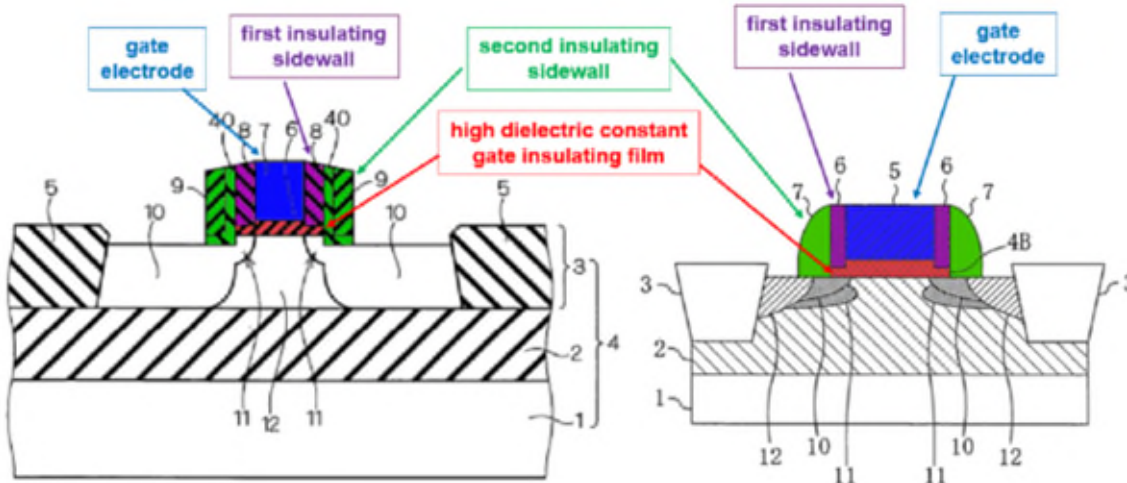
B. Independent Claim 1

Matsumoto's first and fourth embodiment devices each renders claim 1 obvious, as illustrated by the side-by-side figures below. Ex.1101, ¶142; Ex.1009, FIGS. 1 (below, top-left), 22 (below, bottom-left); Ex.1001 FIGS. 3 (below, top-right), 2 (below, bottom-right).



**Matsumoto, Figure 1
First Embodiment**

'227 Patent, Figure 3



**Matsumoto, Figure 22
Fourth Embodiment**

'227 Patent, Figure 2

1. Preamble

Matsumoto’s first embodiment (*see* Ex.1009, FIG. 1) and fourth embodiment (*see id.*, FIG. 22) each discloses a “*semiconductor device*”¹¹: “The present invention relates to a **semiconductor device**.”¹² Ex.1009, ¶¶2, 102, 137; Ex.1101, ¶143.

2. Limitation 1[a]

Matsumoto’s first and fourth embodiments each teaches “*a high dielectric constant gate insulating film formed on an active region in a substrate*” 1[a].

Ex.1101, ¶¶144-51.

Both embodiments include “*a substrate*.” Ex.1101, ¶144. Each device has a multi-layer SOT **substrate** 4 (*see* Ex.1009, FIGS. 1 (below, left), 22 (below, right) (shaded pink)) with silicon substrate 1, BOX layer 2 and single-crystalline silicon layer 3 “stacked in the order named.” Ex.1009, ¶102, ¶¶137, 140 (relating fourth embodiment to first embodiment);¹³ *Google LLC v. Jenam Tech, LLC*, IPR2021-

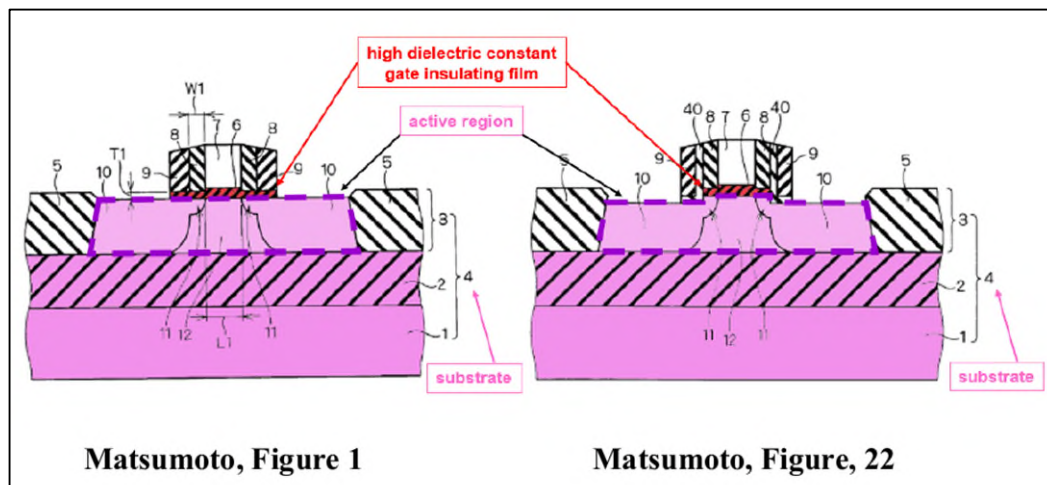
¹¹ Claim language is indicated by italics throughout.

¹² Unless otherwise noted, all emphasis added.

¹³ Although Matsumoto discloses several embodiments, many of the fabrication steps are discussed in relation to the first embodiment. Ex.1101, ¶125; Ex.1009, ¶137. Thus, Petitioner at times also relies on disclosures from Matsumoto’s first embodiment when discussing the fourth embodiment.

00630, 2022 WL 4287797, *9 n.9 (P.T.A.B. Sept. 16, 2022) (applying same disclosure where “figures refer to corresponding features using the same reference numbers”).

Isolating insulation film structures 5 “extend[ing] from the upper surface of silicon layer 3 to the upper surface of BOX layer 2” define a “**device region.**” Ex.1009, ¶¶102-03, FIG. 1 (below, left), ¶¶137, 140, FIG. 22 (below-right). The device region, identified by isolation regions, is an “*active region in a substrate*” and includes source/drain regions 10. Ex.1009, ¶¶105, 139; Ex.1101, ¶145; see Ex.1001, 1:34-35 (“region of the well 102 surrounded by the STI serves as an active region of a substrate 101”), 7:26-43 (active region includes source/drain regions surrounded by STI structures).



In both embodiments, film 6 (see Ex.1009, FIGS. 1 (above, left), 22 (above, right) (shaded red)) “is formed partially on the upper surface of the silicon layer 3” in the device region with gate electrode 7 “formed partially” thereon. *Id.*, ¶103, ¶137

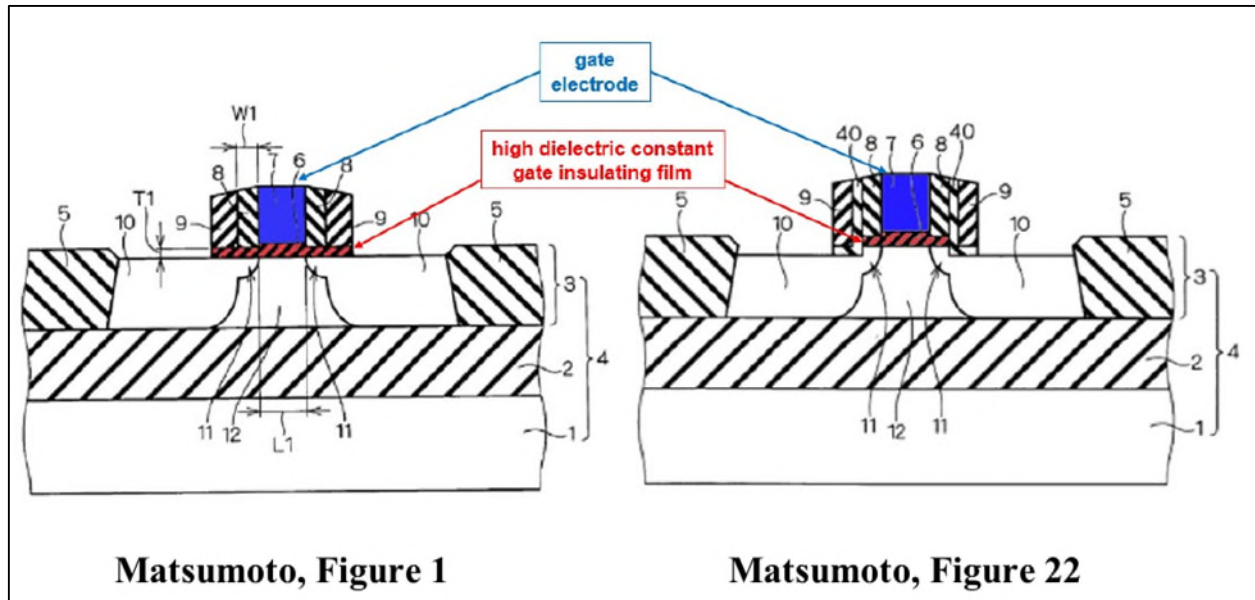
(fourth embodiment's gate electrode "formed by the process described in the first preferred embodiment"), FIG. 22 (elements 6, 7). "A silicon oxynitride film, a metal oxide film such as Al_2O_3 or a ferroelectric film such as Ta_2O_5 and BST may be formed in place of the silicon oxide film 13," which is etched during fabrication to form film 6. *Id.*, ¶¶107, 114, 138, FIGS. 1, 9-10, 18-19, 22. Al_2O_3 , Ta_2O_5 , and BST are high-k dielectrics. Ex.1101, ¶149; see Ex.1001, 1:21-25 ("a **high dielectric constant film** formed of a Hf based oxide, Al based oxide or the like, which has a relative dielectric constant of 10 or more"); Ex.1018, Table I (identifying Al_2O_3 , Ta_2O_5 as high-k dielectrics). A POSITA would have been motivated to use a high-k dielectric in Matsumoto's device to address the well-documented issues with scaling SiO_2 to thicknesses needed for large scale device integration. See Ex.1213, 3-12; Ex.1334, 4-5, 146-47; Ex.1101, ¶¶150-51.

Film 6, present in both Matsumoto's first and fourth embodiments, is therefore "*a high dielectric constant gate insulating film formed on an active region in a substrate*" 1[a]. Ex.1101, ¶151; see, e.g., Ex.1009, ¶103 (disclosing that a portion of film 6, which "lies under the gate electrode 7 functions as a gate insulation film").

3. Limitation 1[b]

Matsumoto's first and fourth embodiments each teaches "*a gate electrode formed on the high dielectric constant gate insulating film*" 1[b]. Ex.1101, ¶¶152-53.

In both embodiments (illustrated below), “**gate electrode 7** [shaded blue] made of polysilicon **is formed partially**” on high-k insulating film 6. Ex.1009, ¶¶103, ¶107 (describing formation of high-k insulating film and gate electrode) 137-38, FIGS. 1 (below, left), 22 (below, right).



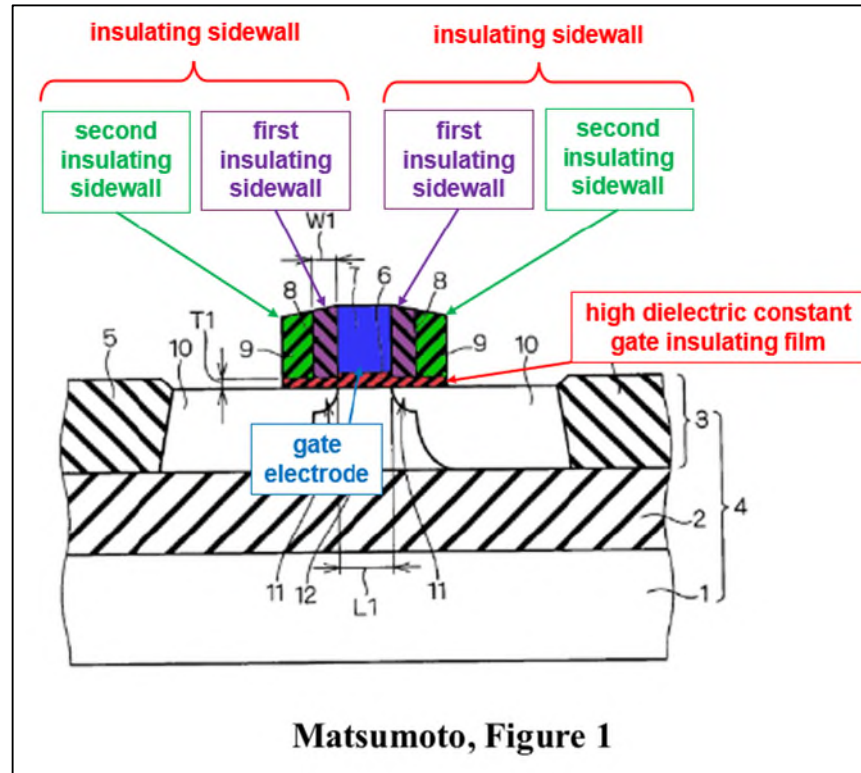
4. Limitations 1[c]/1[f]

Limitation 1[c] recites “*an insulating sidewall formed on each side surface of the gate electrode.*” Limitation 1[f] narrows this limitation, reflecting the claimed insulating sidewall includes two sidewalls: “*the insulating sidewall includes a **first insulating sidewall** formed on a side surface of the gate electrode and a **second insulating sidewall** formed on the side surface of the gate electrode with the first insulating sidewall interposed therebetween.*” Matsumoto’s first and fourth embodiments teach these limitations. Ex.1101, ¶¶154-162.

In Matsumoto's first embodiment, "silicon nitride film 9 is formed on each side surface of the gate electrode 7, with a silicon oxide film 8 therebetween." Ex.1009, ¶103, FIG. 1 (below). Matsumoto refers to film 9 as a "sidewall insulation film" but does not refer to film 8 as a "sidewall." See *id.*, ¶114 (describing nitride films 9a/9b "serving as **sidewall** insulation films"). A POSITA would have understood film 8 also to be a sidewall. *Id.*, ¶¶104, 110, 40 ("the semiconductor device further includes a second sidewall formed on the side surface of the gate electrode, with the first sidewall therebetween"); Ex.1101, ¶155. Because silicon oxide and silicon nitride are both insulators, silicon oxide film 8 and silicon nitride film 9, as illustrated below, are collectively "*an insulating sidewall formed on each side surface of the gate electrode*" 1[c] with film 8 (see Ex.1009, FIG. 1 (below) (shaded purple)) being "*a first insulating sidewall formed on¹⁴ a side surface of the gate electrode*" and film 9 (see *id.*, FIG. 1 (below) (shaded green)) being the "*second insulating sidewall formed on the side surface of the gate electrode with the first insulating sidewall interposed therebetween*" 1[f]. See Ex.1009, ¶¶110 (describing the formation of silicon oxide films 8a/8b on the side surfaces of the gate electrodes), 114, claim 1 (referring to "**insulation** films" formed on side surfaces on gate

¹⁴ The '227 patent uses the term "*formed on*" generally to refer to location and does not require contact. See, *e.g.*, Ex.1001, 1:31-33, 7:28-32; Ex.1101, ¶158)

electrode); Ex.1001, 3:17-22 (referring to two components collectively as an insulating sidewall); Ex.1101, ¶¶157-58.



In Matsumoto’s fourth embodiment, silicon oxide film 40 and silicon nitride film 9 are formed “on the outer side surfaces of” film 8, as illustrated in Figure 22. See Ex.1009, ¶¶110, 139, FIG. 22 (below). Silicon oxide film 8, silicon oxide film 40, and silicon nitride film 9 are collectively “an insulating sidewall” 1[c] with film 8 (see Ex.1009, FIG. 22 (below) (shaded purple)) being “a first insulating sidewall” and film 9 (see *id.*, shaded green)) alone, film 40 (see *id.* (shaded green)) alone, or their combination being “a second insulating sidewall formed on the side surface of the gate electrode with the first insulating sidewall interposed therebetween” 1[f],



5. Limitations 1[d]-1[e]/1[g]-1[h]

Limitation 1[d] recites “*the high dielectric constant gate insulating film is continuously formed so as to extend from under the gate electrode **to under the insulating sidewall***” and limitation 1[e] recites “*at least part of the high dielectric*

¹⁵ The '227 patent uses the term “insulating sidewall” to refer to a single component (Ex.1001, 5:66-67), a collective structure of two components (*id.*, 3:17-22), and a component having multiple layers (*id.*, 21:5-15).

*constant gate insulating film located **under the insulating sidewall** has a smaller thickness than a thickness of part of the high dielectric constant gate insulating film located under the gate electrode.”*

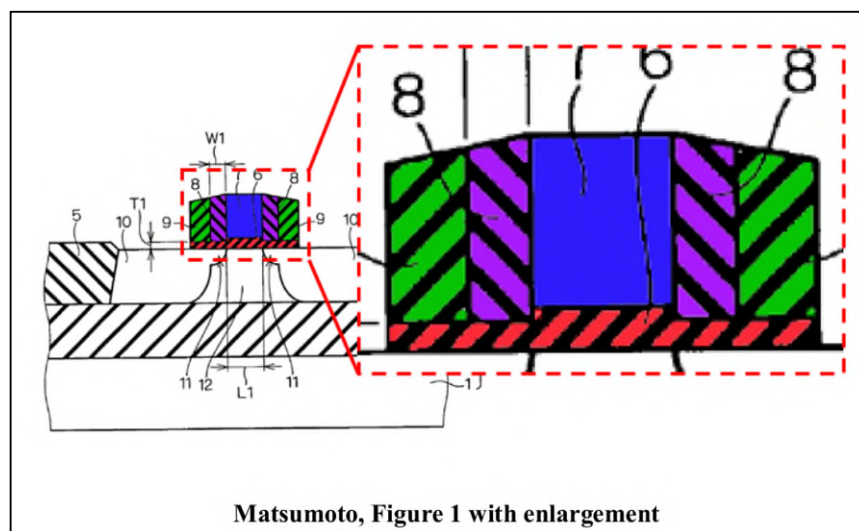
Limitations [1G]-[1H] narrow and largely repeat 1[d]-1[e], reflecting the claimed insulating sidewall includes two sidewalls: “*the high dielectric constant gate insulating film is continuously formed so as to extend from under the gate electrode **to under the first insulating sidewall**” 1[g] and “*part of the high dielectric constant gate insulating film located **under the first insulating sidewall** has a smaller thickness than a thickness of part of the high dielectric constant gate insulating film located under the gate electrode” 1[h].**

Matsumoto’s first and fourth embodiments teach these limitations, for the reasons explained in detail below. Ex.1101, ¶¶165-176.

a. First Embodiment

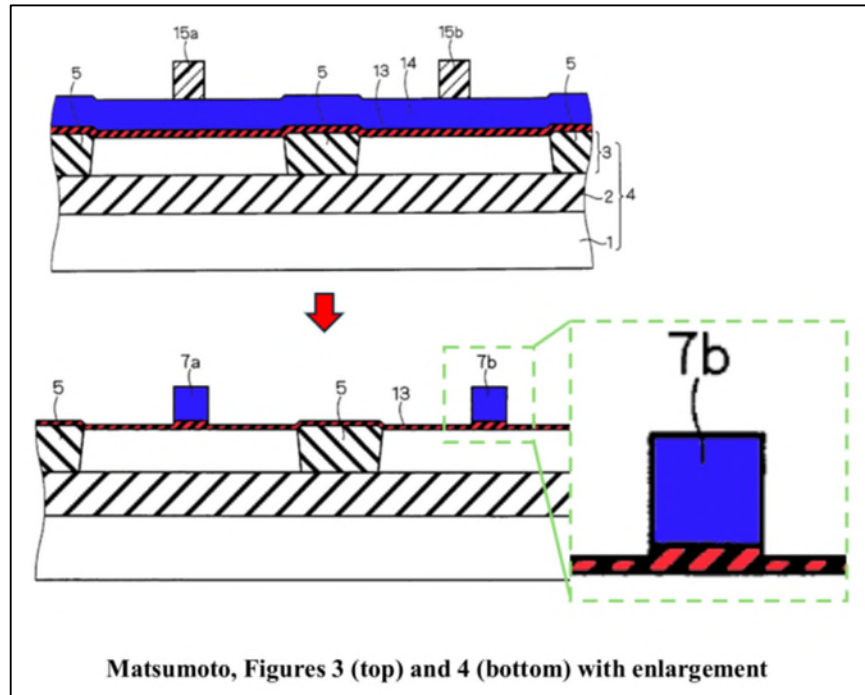
As shown in the enlargement of Matsumoto’s Figure 1, and confirmed by Matsumoto’s fabrication process teachings, high-k gate insulating film 6 (see Ex.1009, FIG. 1 (below) (shaded red)) is an uninterrupted layer (as evidenced by the absence of gaps) that extends from under the gate electrode 7 to under film 8 (“*first insulating sidewall*”; see *id.*, FIG. 1 (below) (shaded purple)), which is part of the collective “*insulating sidewall*” (films 8 and 9). The high-k film 6 is thinner under film 8 (“*first insulating sidewall*”) than it is under the gate electrode 7 (see *id.*, FIG.

1 (below) (shaded blue)). Matsumoto’s first embodiment device therefore discloses limitations 1[d]-1[e]/1[g]-1[h]. *Unified Pats., LLC v. Oceana Innovations LLC*, IPR2020-01463, 2022 WL 500391, *17 (P.T.A.B. Feb. 14, 2022) (“[A] patent drawing may serve as prior art ‘without referring to the surrounding description’ if ‘the prior art features are clearly disclosed by the drawing.’”) (citations omitted); Ex.1101, ¶¶165-67.

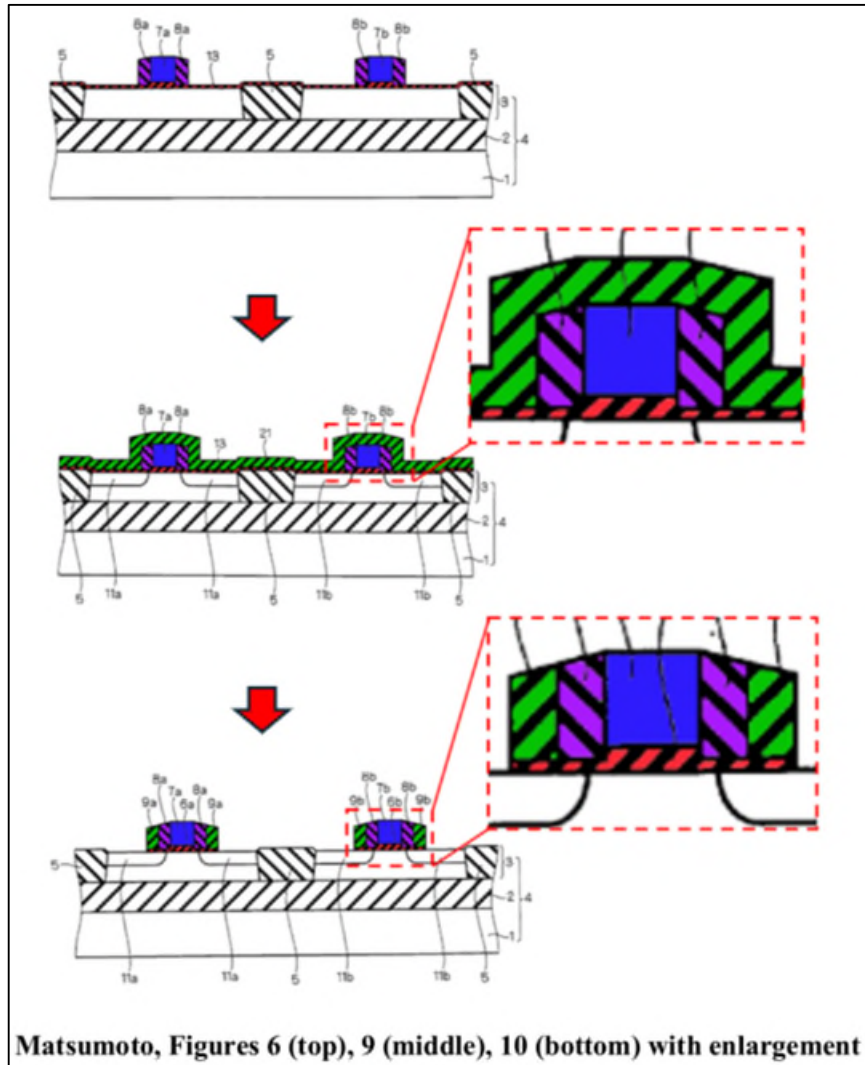


The fabrication of the first embodiment device confirms the Figure 1 device structure. During fabrication, high-k dielectric film 13 (*see* Ex.1009, FIGS. 3-4 (below) (shaded red)) is formed on the substrate and polysilicon film 14 (*see id.* (shaded blue)) is formed on high-k dielectric film 13. *See id.*, ¶107. The etching process used to form the gate electrode “slightly etches the upper surface of” film 13, resulting in a high-k dielectric film with a larger thickness under the gate

electrode than in the areas not under the gate electrode. Ex.1009, ¶108, FIG. 4 (below, bottom); Ex.1101, ¶¶168-69.



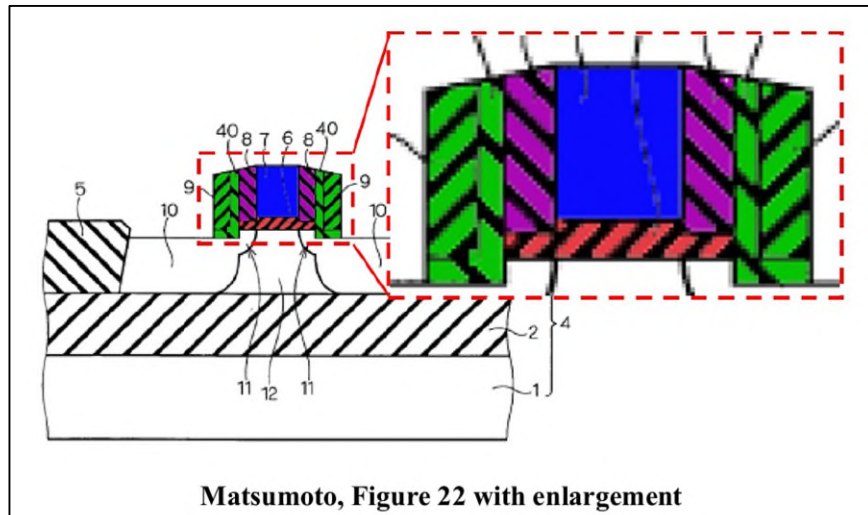
After formation of sidewalls 8a/8b (“*first insulating sidewall*”; see Ex.1009, FIGS. 6, 9-10 (shaded purple)), silicon nitride film 21 is “formed on the entire top surface” of the intermediate structure. *Id.*, ¶¶109-10, 114, FIGS. 6 (below, top), 9 (below, middle). Film 21 and film 13 are etched “until the upper surface of the silicon layer 3 is exposed,” forming sidewalls 9a/9b (“*second insulating sidewall*”; see *id.*, FIGS. 6, 9 (below) (shaded green)). Ex.1009, ¶114. After this etching, the high-k dielectric film (see *id.*, FIGS. 6, 9-10 (below) (shaded red)) remains under the gate electrode and first and second sidewalls. Ex.1101, ¶¶168-69.



b. Fourth Embodiment

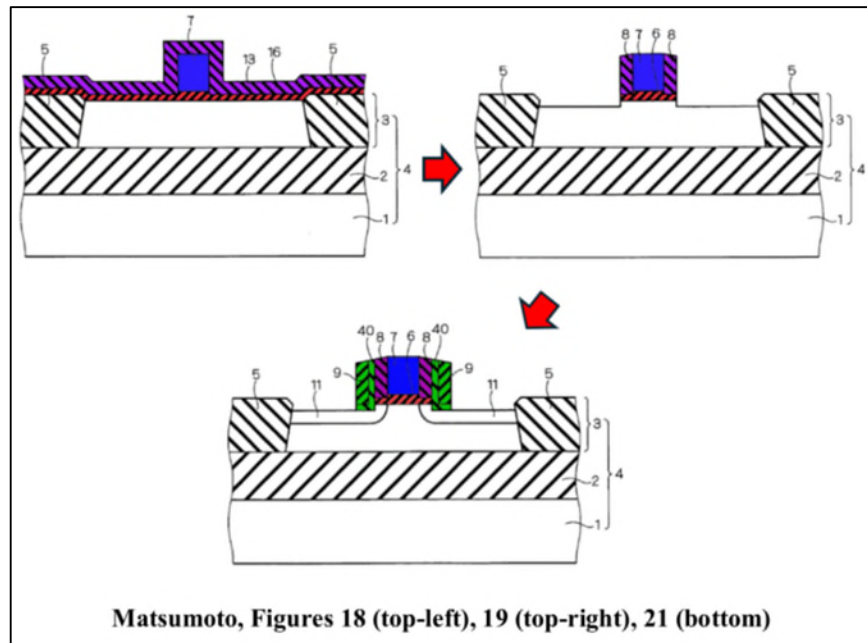
As shown in the enlargement of Matsumoto’s Figure 22 and confirmed by Matsumoto’s fabrication process teachings, high-k gate insulating film 6 (see Ex.1009, FIG. 22 (below) (shaded red)) is an uninterrupted layer (as evidenced by the absence of gaps) that extends from under the gate electrode to under only film 8 (“*first insulating sidewall*”), which is part of the collective “*insulating sidewall*” (films 8, 9, and 40). The high-k film 6 is thinner under the film 8 (“*first insulating*

sidewall”; *see id.* (shaded purple)) than it is under the gate electrode 7 (*see id.* (shaded blue)). Matsumoto’s fourth embodiment device therefore discloses limitations 1[d]-1[e]/1[g]-1[h]. *See Unified*, 2022 WL 500391, at *17; Ex.1101, ¶170.



The fabrication process of Matsumoto’s fourth embodiment device confirms the Figure 22 device structure. During fabrication, “gate electrode 7 is formed by the process described” in Matsumoto’s first embodiment, resulting in high-k dielectric film 13 having a larger thickness under the gate electrode (*see* Ex.1009, FIG. 18 (below, top-left). *See id.*, ¶¶137, 107-08; Ex.1101, ¶172. The etching process that forms sidewall 8 (“*the first insulating sidewall*”; *see* Ex.1009, FIGS. 18-19, 21 (below) (shaded purple)) “overetch[es] the upper surface of the silicon layer 3” and as a result, the high-k dielectric film (*see id.*, FIGS. 18-19, 21 (below) (shaded red)) remains only under the gate electrode and sidewall 8. *Id.*, ¶138, FIG. 19 (below, top-right); Ex.1101, ¶173. Film 40 and film 9 (alone or in combination the “*second*

insulating sidewall” (see Ex.1009, FIG. 21 (below, bottom) (shaded green)) are then formed on the outer side surfaces of film 8 and on the substrate surface. *Id.*, ¶139; Ex.1101, ¶¶174-75.

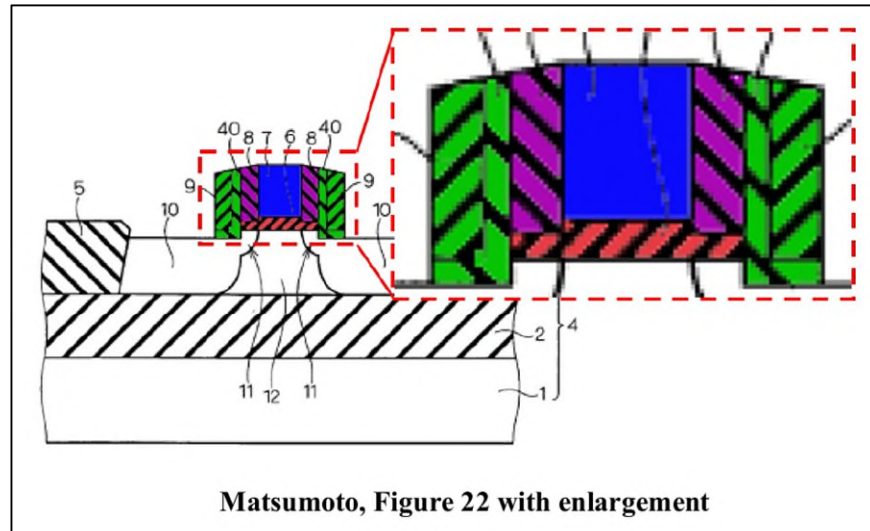


C. Claim 2

Matsumoto’s fourth embodiment teaches “*the high dielectric constant gate insulating film is formed so as not to be located under the second insulating sidewall*” [2]. Ex.1101, ¶¶176-78.

As shown in the enlargement of Matsumoto’s Figure 22 below, and discussed in §V.B.5.b, high-k gate insulating film 6 (shaded red) extends only under film 8 (“*first insulating sidewall*”) and is not located under films 40 and 9 (alone or collectively the “*second insulating sidewall*”). See *Unified*, 2022 WL 500391, at *17; Ex.1009, FIG. 22 (below). Matsumoto’s fabrication process of the fourth

embodiment, discussed in §V.B.5.b, confirms the Figure 22 device structure. See Ex.1009, ¶¶138-39, Ex.1101, ¶¶176-78.



VI. GROUND II: Combination of Matsumoto and Wang Renders Claims 7-8, and 14 Obvious.

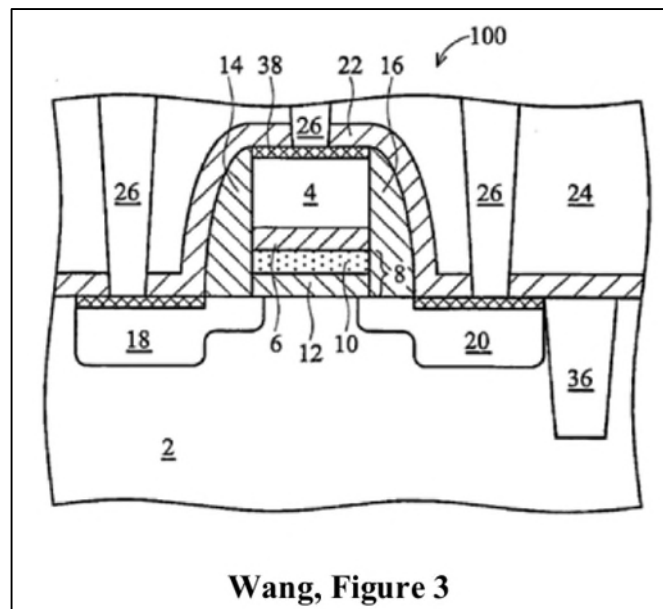
PO may argue that Matsumoto does not expressly disclose “a buffer insulating film,” recited in claims 7-8. While Matsumoto discloses exemplary high-k dielectrics, PO may also argue that it does not explicitly disclose a high-k film “formed of a Hf based oxide” [14]. Wang discloses these limitations. Ex.1101, ¶¶179-94.

A. Wang

Wang “relates to an improved input/output transistor device having a composite gate dielectric comprising a nitrogen containing, high-k dielectric, and an underlying dielectric layer having a nitrogen containing portion in contact with the high-k dielectric layer and a non-nitrogen containing portion that is in contact with

the substrate.” Ex.1012, ¶2. Wang and Matsumoto are in the same field as the ’227 patent, “a semiconductor device and a method for fabricating.” Ex.1001, 1:8-9; Ex.1009, ¶2; Ex.1012, ¶2; Ex.1101, ¶129.

Wang’s transistor 100 includes a gate stack with high-k dielectric layer 6 formed on dielectric layer 8 comprising a nitrided portion 10 and a non-nitrided/substantially nitrogen-free portion 12. Ex.1012, ¶¶22, 24, 48, FIG. 3 (below). Wang presents a list of alternatives for its high-k gate dielectric including Hf-based dielectrics (e.g., HfO₂, HfSiO, HfON, or HfSiON). Ex.1012, ¶¶9, 25; Ex.1101, ¶¶130-31.

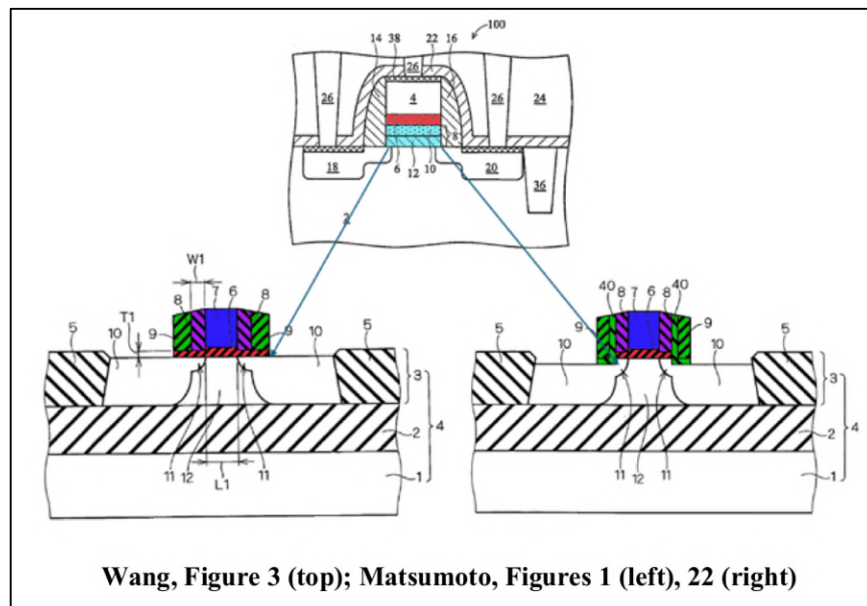


B. Claims 7-8

The combination of Matsumoto’s first and/or fourth embodiments and Wang discloses “a buffer insulating film between the substrate and the high dielectric

constant gate insulating film” [7] where “*the buffer insulating film is a silicon oxide film or a silicon oxynitride film*” [8]. Ex.1101, ¶¶180-89.

A POSITA would have been motivated to combine Wang’s teachings regarding use of a dielectric layer between a high-k gate insulating film and the silicon substrate with Matsumoto’s first and fourth embodiment devices. Ex.1101, ¶180. For example, a POSITA would have been motivated to integrate Wang’s underlying dielectric layer 8 (see Ex.1012, FIG. 3 (below) (shaded aqua)) between the substrate and Matsumoto’s high-k dielectric (see Ex.1009, FIGS. 1 (below left), 22 (below right) (shaded red)) in the first embodiment device (Figure 1) and fourth embodiment device (Figure 22). Ex.1101, ¶¶180.



Wang’s underlying dielectric 8 is “preferably formed of silicon oxide” and “has a first, nitrided portion 10 that is in contact with high-k dielectric layer 6 and a second non-nitrided, or substantially nitrogen-free, portion 12 that is in contact with

the underlying substrate 2.” Ex.1012, ¶48. Underlying dielectric 8 is therefore a “*buffer insulating film*,” a “*silicon oxide film*” (e.g., in non-nitrided portion 12), and a “*silicon oxynitride film*” (e.g., in nitrided portion 10). Ex.1101, ¶¶181-82; Ex.1338, 88-89 (describing use of “nitrided oxides” including SiO_xN_y). Alternatively, either portion 10 or portion 12 is the “*buffer insulating film*.” Ex.1101, ¶¶183. In the combination, Wang’s underlying dielectric 8 is between the substrate and Matsumoto’s high-k gate insulating film 6.

Wang explicitly motivates the above combination, teaching that “[d]ue to the undesirable interactions between high-k dielectrics and the underlying semiconductor material (usually silicon, germanium, silicon germanium, and the like) to degrade carrier mobility, a thin silicon oxide layer is typically employed as part of the gate dielectric even when a high-k gate dielectric is employed.” Ex.1012, ¶3; Ex.1101, ¶¶184-89. This is consistent with the purpose of the buffer insulating film in the ’227 patent. Ex.1001, 12:9-15 (by using a buffer insulating film, “deterioration of an interface between a substrate and a gate insulating film can be suppressed”). Wang further stresses that “underlying dielectric layer 8 advantageously provides higher mobility and higher reliability for the high-k peripheral (or I/O) device.” Ex.1012, ¶28. A POSITA would have therefore been motivated to use Wang’s buffer insulating layer to improve carrier mobility and performance of Matsumoto’s first and/or fourth embodiment device. Ex.1101, ¶185;

Ex.1009, ¶13 (describing objective to reduce malfunctions and operating characteristic variations).

Applying Wang's buffer layer to Matsumoto's first and/or fourth embodiment device is merely the use of a known technique (Wang's buffer insulating layer) to improve similar devices in the same way for the above reasons. See *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 416-17 (2007); Ex.1101, ¶¶186-88. A POSITA would have had a reasonable expectation of success in the combination and the results of the combination would have been predictable because Wang uses established methods for forming the underlying dielectric and its high-k gate dielectric. Ex.1012, ¶22 (describing "thermally grown oxide"), ¶24 (describing use of CVD, ALD and PVD for deposition of high-k film); see also Ex.1009, ¶107 (describing use of CVD for high-k film deposition); Ex.1101, ¶¶186-89.

C. Claim 14

The combination of Matsumoto's first and/or fourth embodiments and Wang discloses "*the high dielectric constant gate insulating film is formed of a Hf based oxide*" [14]. Ex.1101, ¶¶190-94.

Matsumoto teaches use of a high-k film "such as Al₂O₃ or a ferroelectric film such as Ta₂O₅ and BST" as a gate insulating film. Ex.1009, ¶107. Wang teaches use of similar high-k dielectrics (e.g., Al₂O₃ and Ta₂O₅) and others including "HfO₂" which is a Hf-based oxide. Ex.1012, ¶¶9, 12, 25. Ex.1101, ¶¶190-91. By 2005, a

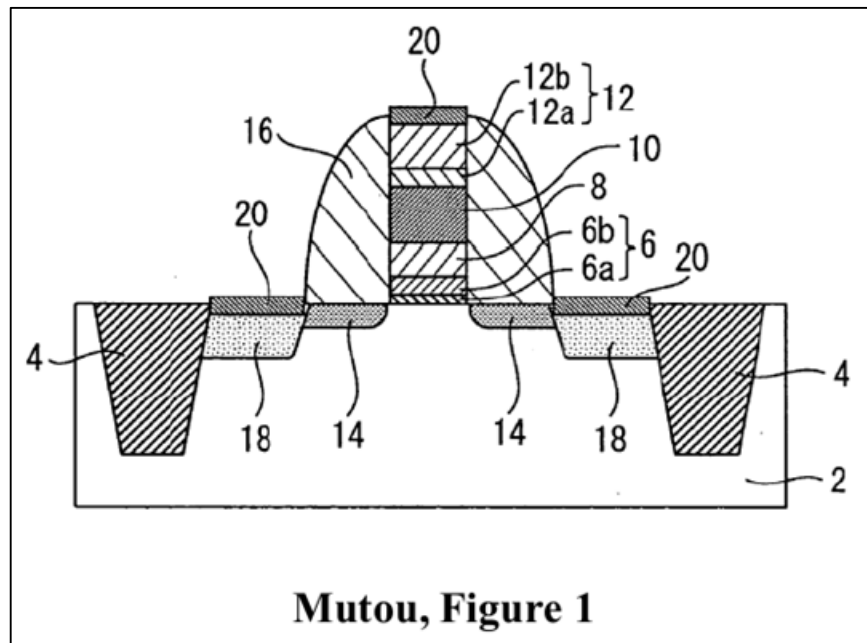
POSITA would have been motivated to select HfO₂ given its known benefits, including, for example, “its superior thermal stability with poly-Si and reasonable band alignment.” Ex.1337, 2.4.1; *see also* Ex.1213, 207 (HfO₂ “combines a high k (15-26) with a bandgap of 5.6 eV, with favourable conduction and valence band offsets with respect to Si ...”); Ex.1349, 6.1.2 (“Excellent dielectric properties ... suggest that HfO₂ is a promising material for the future gate dielectric application.”); Ex.1101, ¶193. Another benefit that would have been known to a POSITA is that HfO₂ can be scaled down to a smaller EOT. *See* Ex.1213, 207; Ex.1101, ¶193.

VII. GROUND III: Combination of Matsumoto and Mutou Renders Claims 7 and 8 Obvious.

Should an argument be made that the combination of Matsumoto and Wang fails to render claims 7-8 obvious, Mutou also explicitly describes a “*buffer insulating film*,” and the combination of Matsumoto with Mutou renders claims 7-8 obvious. Ex.1101, ¶¶195-204.

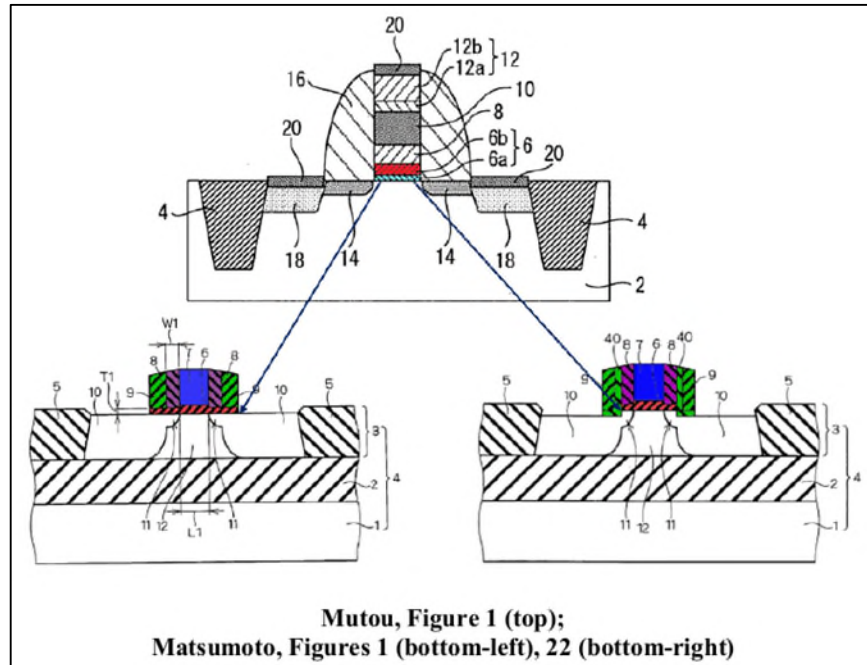
A. Mutou

Mutou’s device includes a silicon substrate 2 and a gate stack comprising interfacial layer 6a, high-k dielectric film 6b, and a multilayer gate electrode. Ex.1019, ¶¶40-41, 44, FIG. 1 (below). Mutou and Matsumoto are in the same field as the ’227 patent, “a semiconductor device and a method for fabricating.” Ex.1001, 1:8-9; Ex.1009, ¶2; Ex.1019, Abstract, ¶¶2, 4; Ex.1101, ¶¶132-133.



B. Motivation to Combine

A POSITA would have been motivated to integrate Mutou's underlying interfacial layer 6a ("*buffer insulating film*") (see Ex.1019, FIG. 1 (below, top) (shaded aqua)) under Matsumoto's high-k dielectric (see Ex.1009, FIGS. 1 (below, bottom-left), 22 (below, bottom-right) (shaded red)) in the first embodiment (Figure 1) and fourth embodiment (Figure 22) devices, as shown below. Ex.1101, ¶196.



Mutou expressly motivates the combination, teaching that “[t]he underlying interfacial layer 6a is acted to inhibit interfacial reaction between the silicon substrate 2 and the high-k dielectric film 6b.” Ex.1019, ¶42. Inhibiting such reactions between the substrate and the high-k film decreases degradation of the high-k film and, thus, improves performance of the device. Ex.1101, ¶¶197-200; *see also* Ex.1001, 12:9-15 (by using a buffer insulating film, “deterioration of an interface between a substrate and a gate insulating film can be suppressed”). This furthers the goal of Matsumoto “to provide a semiconductor device which achieves reductions in malfunctions and operating characteristic variations.” Ex.1009, ¶13. Based on these disclosures, a POSITA would have been motivated to make the above combination to inhibit interfacial reaction between the substrate and the high-k film and improve performance of Matsumoto’s devices. Ex.1101, ¶¶197-200.

The above combination is nothing more than the use of a known technique (Mutou's underlying interfacial layer) to improve similar devices in the same way for the reasons discussed above. *See KSR*, 550 U.S. at 416-17; Ex.1101, ¶201. A POSITA would have had a reasonable expectation of success in the combination and the results of the combination would have been predictable because Mutou uses conventional processes to form the underlying interfacial layer and deposit the high-k gate insulating film on top. Ex.1019, ¶¶53-54; *see also* Ex.1009, ¶107; Ex.1101, ¶¶201-04.

C. Claims 7 and 8

Mutou's interfacial layer 6a is formed on the silicon substrate 2 and high-k dielectric film 6b is formed on interfacial layer 6a. Ex.1019, ¶41. Mutou's interfacial layer 6a, as used in Matsumoto's first and fourth embodiment devices, is "*a buffer insulating film.*" Ex.1101, ¶197. Underlying interfacial layer 6a may be, "for example, a SiO₂ film, a Si₃N₄ film, or a SiON film" Ex.1019, ¶42.

Thus, the combination of Matsumoto's first and/or fourth embodiments and Mutou discloses "*a buffer insulating film between the substrate and the high dielectric constant gate insulating film*" [7] where "*the buffer insulating film is a silicon oxide film or a silicon oxynitride film*" [8]. Ex.1101, ¶204.

VIII. GROUND IV: Combination of Matsumoto and Ono Renders Claim 14 Obvious.

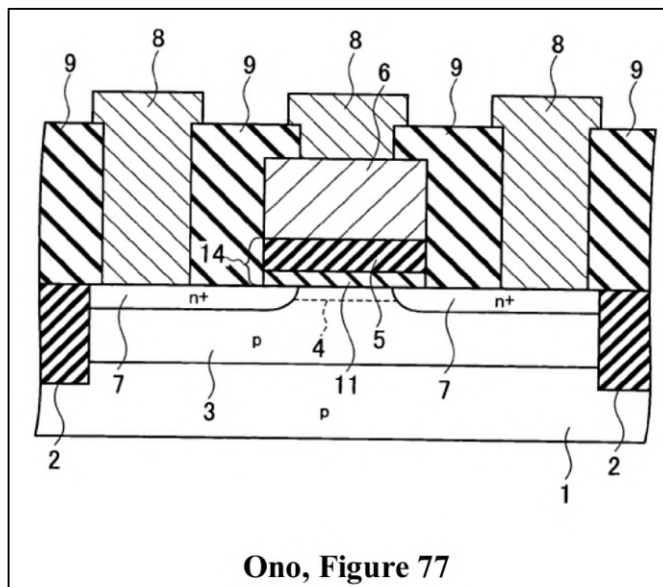
PO may argue that Matsumoto's first and fourth embodiment devices do not expressly disclose that the high-k gate insulating film "*is formed of a Hf based oxide*" [14]. This feature is disclosed in Ono, and the combination of Matsumoto and Ono renders claim 14 obvious. Ex.1101, ¶¶205-08.

A. Ono¹⁶

Ono's second embodiment FET includes a gate stack comprising gate insulator film 5 "made of a metal oxide" and gate insulator film 11 "made of a metal

¹⁶ None of the ground references was applied by the Examiner during prosecution of the '227 patent. Applicant cited JP-Ono on an information disclosure statement ("IDS"). However, JP-Ono has no familial relationship to Ono, is not a foreign counterpart to JP-Ono, does not have the same specification as Ono, and was filed by different inventors than Ono. See Ex.1340, cover ("Ono Tamashiro"); compare Ex.1013, cover ("Mizuki Ono"). JP-Ono was not applied by the Examiner and thus was not evaluated during examination. Significantly, Applicant supplied JP-Ono with its IDS in the Japanese language with only an English language abstract. See Ex.1340. Even assuming JP-Ono was evaluated by the Examiner, which the record does not support, the Examiner erred in allowing the claims over JP-Ono and by failing to recognize its teachings relating to the side end of the gate insulating film,

oxide with a higher dielectric constant than the gate insulator film 5.” Ex.1013, ¶207, FIG. 77 (below). Gate insulator film 5 is made of a “HfO₂ film.” *Id.*, ¶209. Gate electrode 6 is formed on gate insulator film 5 and can have gate sidewalls. Ex.1013, ¶¶207, 181 (in the first embodiment, “gate sidewalls are not mentioned; however, sidewalls may be provided to the gate electrode”), 210 (“Various modifications as described in the first embodiment are also possible with this [second] embodiment, and the same effects may be obtained.”), FIG. 77; Ex.1101, ¶¶134-35. Ono and Matsumoto are in the same field as the ’227 patent, “a semiconductor device and a method for fabricating.” Ex.1001, 1:8-9; Ex.1009, ¶2; Ex.1013, Abstract, ¶¶3-7; Ex.1101, ¶134.



which is understandable in view of the limited English language content of JP-Ono submitted by the Applicant.

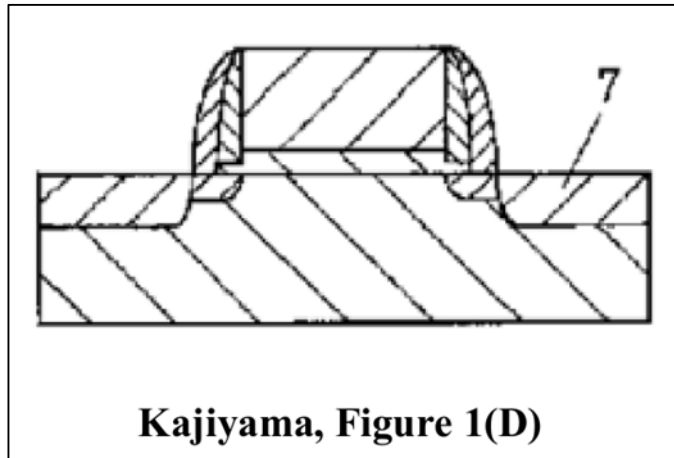
B. Claim 14

The combination of Matsumoto's first and/or fourth embodiments and Ono discloses "*the high dielectric constant gate insulating film is formed of a Hf based oxide*" [14]. Ex.1101, ¶¶205-06. Ono teaches that its gate insulator film 5 is made of "HfO₂ film." Ex.1013, ¶209. A POSITA would have been motivated to use a Hf-based oxide as a gate insulating layer as taught by Ono in Matsumoto's first and/or fourth embodiments for the reasons discussed in §VI.C with respect to the combination of Matsumoto and Wang, including HfO₂'s superior thermal stability, reasonable band alignment, and ability to be scaled down to a smaller EOT. Ex.1101, ¶¶207-08; Ex.1337, 2.4.1; Ex.1213, 207; Ex.1349, 6.1.2.

IX. GROUND V: Kajiyama Anticipates Claims 1 and 2.

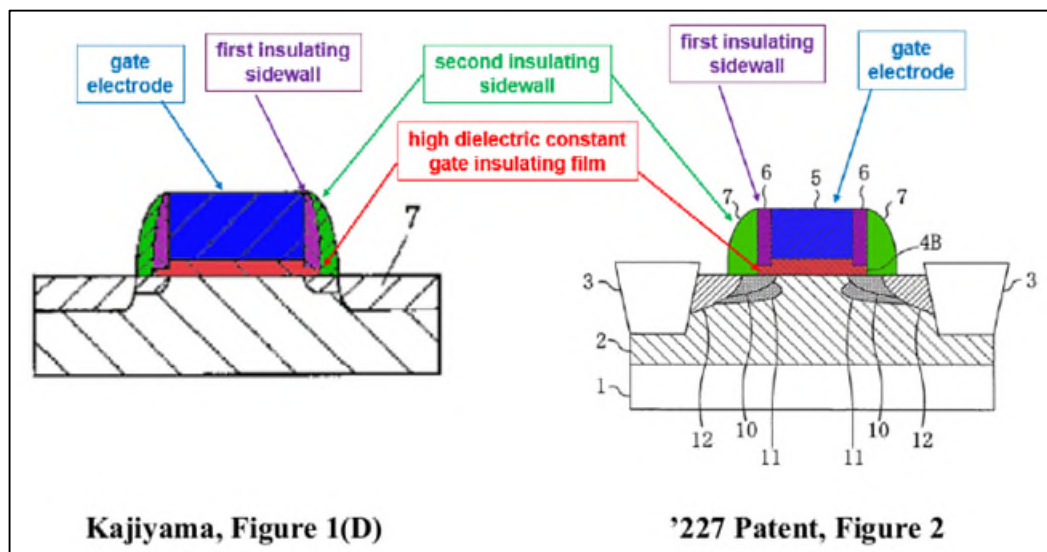
A. Kajiyama

Kajiyama is directed to "semiconductor devices" and "in particular to insulating gate type field effect transistors having a gate dielectric film (high dielectric constant material)." Ex.1011, ¶1. Kajiyama discloses two embodiments of its semiconductor device. This Petition focuses on Kajiyama's first embodiment FET (shown in Figure 1(D) below), which includes a gate electrode with two sidewalls. A high-k gate insulating film extends from under the gate electrode to under only the first sidewall. Ex.1011, ¶¶1, 28, FIG. 1(D) (below). Ex.1101, ¶¶138-39;



B. Independent Claim 1

Kajiyama's first embodiment device anticipates claim 1, as illustrated by the side-by-side figures below. Ex.1011, FIG. 1(D) (below, left); Ex.1011, FIG. 2, (below, right).



1. Preamble [1P]

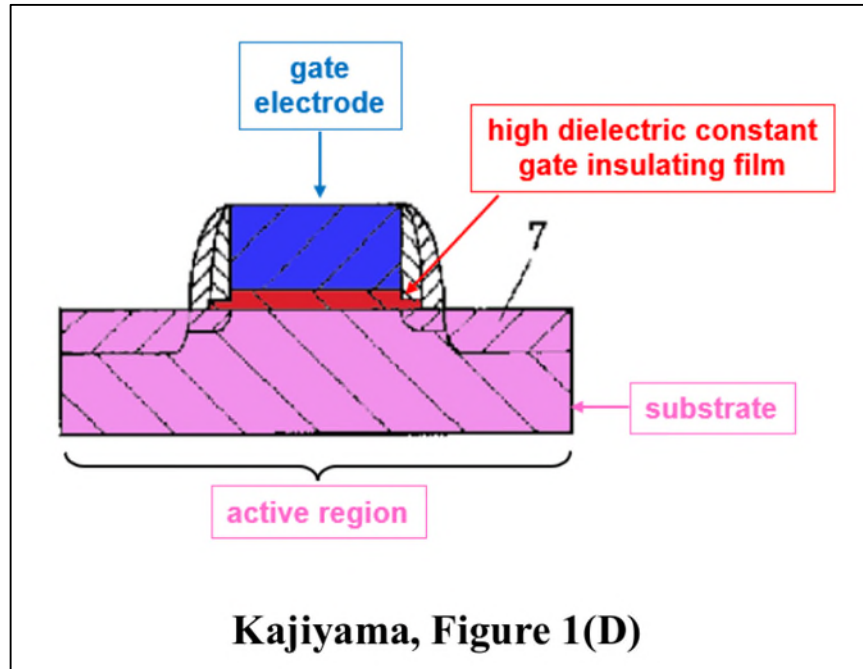
Kajiyama's first embodiment discloses a "*semiconductor device*": "[t]he present invention relates to semiconductor devices and manufacturing methods thereof, and in particular to insulating gate type field effect transistors having a gate

dielectric film (high dielectric constant material).” Ex.1011, ¶1; *see also* Ex.1011, ¶27; Ex.1101, ¶¶211-12.

2. Limitations 1[a]-1[b]

Kajiyama teaches “a high dielectric constant gate insulating film formed on an active region in a substrate” 1[a] and “a gate electrode formed on the high dielectric constant gate insulating film” 1[b]. Ex.1101, ¶¶213-219.

Kajiyama’s device has a “p-type Si **substrate** [shaded pink]” with an “element separation layer (not shown) on the Si substrate 1.” Ex.1011, ¶¶28-29, FIG. 1(D) (below). Kajiyama’s element separation layer is equivalent to the ’227 patent’s STI structures. Ex.1011, ¶¶5, 29; Ex.1001, 7:26-43 (showing active region with source/drain regions surrounded by STI structures 3); Ex.1101, ¶¶213-14. In Kajiyama, within the region defined by the element separation layer, an n-type LDD diffusion layer 4 is formed and, in a subsequent process step, an n⁺ source drain diffusion layer 7 is formed. Ex.1011, ¶¶29, 32, FIGS. 1(A), 1(D). The region defined by Kajiyama’s element separation layer is “an active region in a substrate.” Ex.1101, ¶214.



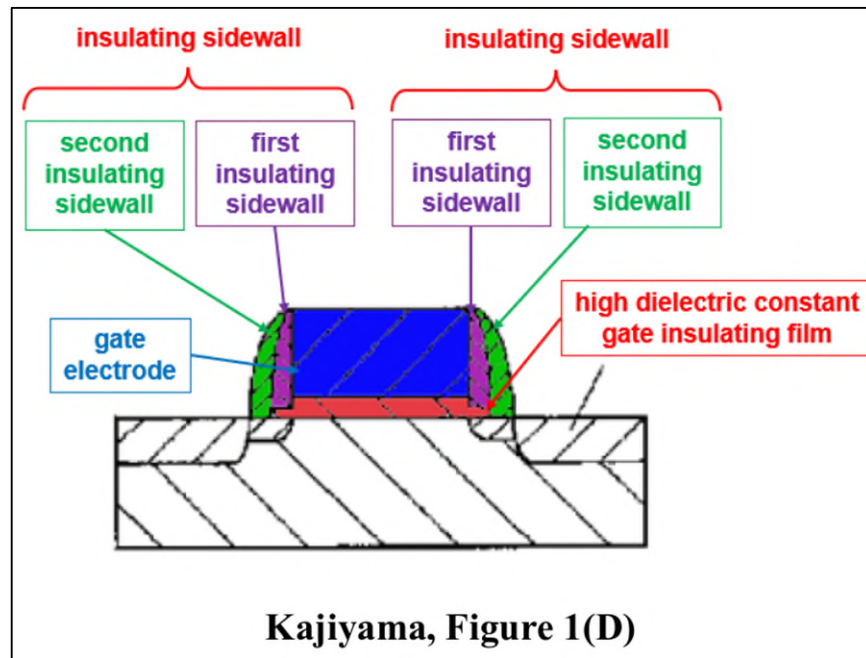
Kajiyama’s “device comprises a gate insulating film [labeled 2 in Figure 1(A)] consisting of a high dielectric film¹⁷ [shaded red] formed on a semiconductor substrate.” Ex.1011, ¶¶14, 28, claim 1 (reciting “a gate insulating film consisting of a high dielectric film formed on a semiconductor substrate, a gate electrode consisting of a conductive film formed on the gate insulating film”), FIG. 1(D) (above). The high-k film, formed on the substrate within the element separation layer, is therefore the “*high dielectric constant gate insulating film formed on an active region in a substrate*” 1[a]. Ex.1011, ¶29; Ex.1101, ¶¶215-16.

¹⁷ Kajiyama also refers to the high-k film 2 as “ZrO₂ film 2.” See, e.g., Ex.1011, ¶29.

Gate electrode 3 (see Ex.1011, FIG. 1(D) (above) (shaded blue)) “consisting of a conductive film [is] formed on [the] gate insulating film.” Ex.1011, ¶14. Kajiyama’s device thus includes “*a gate electrode formed on the high dielectric constant gate insulating film*” 1[b]. Ex.1101, ¶¶218-19.

3. Limitations 1[c]/1[f]

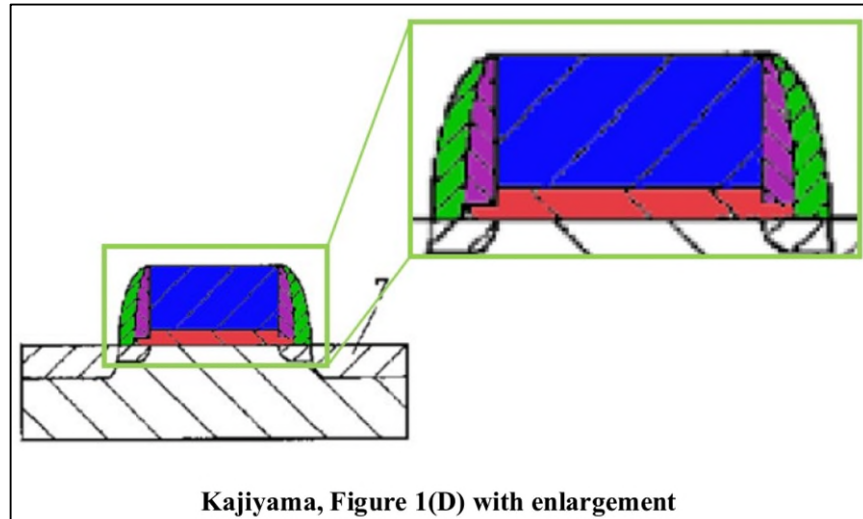
Kajiyama’s device includes “a first sidewall [labeled 5 in Figure 1(B), shaded purple below] consisting of a dielectric film formed on a sidewall of the gate electrode, and a second sidewall [labeled 6 in Figure 1(C), shaded green below] ... formed to cover the first sidewall.” Ex.1011, ¶¶14, 28, FIG. 1(D) (below). Kajiyama teaches that first sidewall 5 “consist[s] of ZrO₂ film (**insulation** film)” while also noting that “the effects of the present invention can be obtained even with other dielectric films [for first sidewall 5], such as TEOS films, BPSG films, or SiON films.” Ex.1011, ¶¶28, 47. TEOS, BPSG, and SiON are each silicon-based oxides and known insulating materials. Ex.1101, ¶¶220-21. First sidewall 5 is therefore a “*first insulating sidewall formed on a side surface of the gate electrode...*” 1[f]. *Id.* Second sidewall 6 is a silicon nitride film (referred to as Si₃N₄ film) and is therefore a “*second insulating sidewall formed on the side surface of the gate electrode with the first insulating sidewall interposed therebetween*” 1[f]. Ex.1011, ¶28. First sidewall 5 and second sidewall 6 are collectively “*an insulating sidewall formed on each side surface of the gate electrode*” 1[c]. Ex.1101, ¶¶222-24.



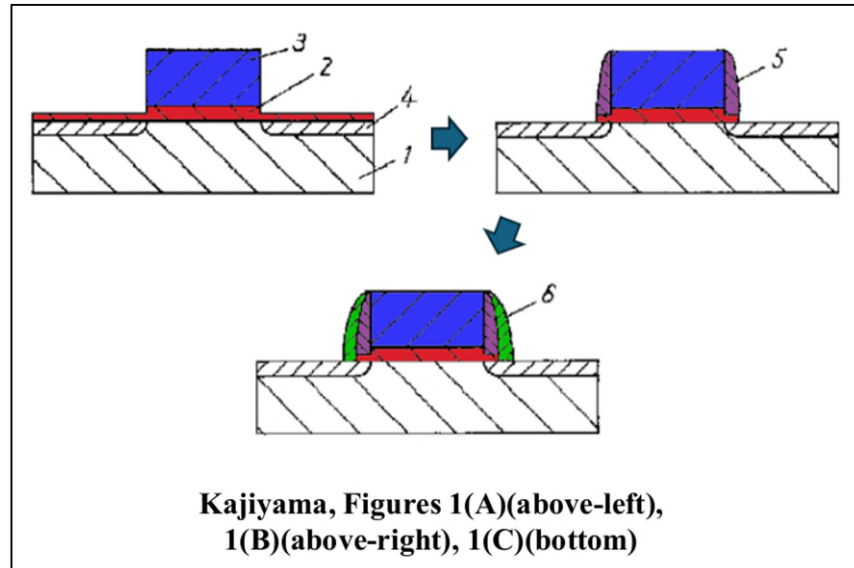
4. Limitations 1[d]-1[e]/1[g]-1[h]

As shown in the enlargement of Kajiyama’s device, and confirmed by the disclosed process, high-k film 2 (see Ex.1011, FIG. 1(D) (below) (shaded red)) is an uninterrupted layer (as evidenced by the absence of gaps) that extends from under the gate electrode to under first sidewall 5 (“*first insulating sidewall*”; see *id.* (shaded purple)) which is part of the collective “*insulating sidewall*” (sidewall 5 and sidewall 6). The high-k film is thinner under sidewall 5 (“*first insulating sidewall*”) than it is under the gate electrode (see *id.*, FIG. 1(D) (below) (shaded blue)). Kajiyama’s device therefore discloses that “*the high dielectric constant gate insulating film is continuously formed so as to extend from under the gate electrode to under the insulating sidewall*” 1[d], “*at least part of the high dielectric constant gate insulating film located under the insulating sidewall has a smaller thickness than a thickness*

*of part of the high dielectric constant gate insulating film located under the gate electrode” 1[e], “the high dielectric constant gate insulating film is continuously formed so as to extend from under the gate electrode to under the first insulating sidewall” 1[g], and “part of the high dielectric constant gate insulating film located under the first insulating sidewall has a smaller thickness than a thickness of part of the high dielectric constant gate insulating film located under the gate electrode” 1[h]. Ex.1101, ¶¶225-26, 230; see Unified, 2022 WL 500391, at *17.*



Kajiyama’s fabrication process confirms the Figure 1(D) structure. During fabrication, an n-type polySi film is deposited on high-k film 2 and etched “to form a gate electrode 3.” Ex.1011, ¶29. High-k film 2 “is also etched to reduce the film.” Ex.1011, ¶29, FIG. 1(A) (below, top-left). As a result of this process, the thickness of high-k film 2 is larger under the gate electrode than elsewhere. Ex.1101, ¶¶227-28.

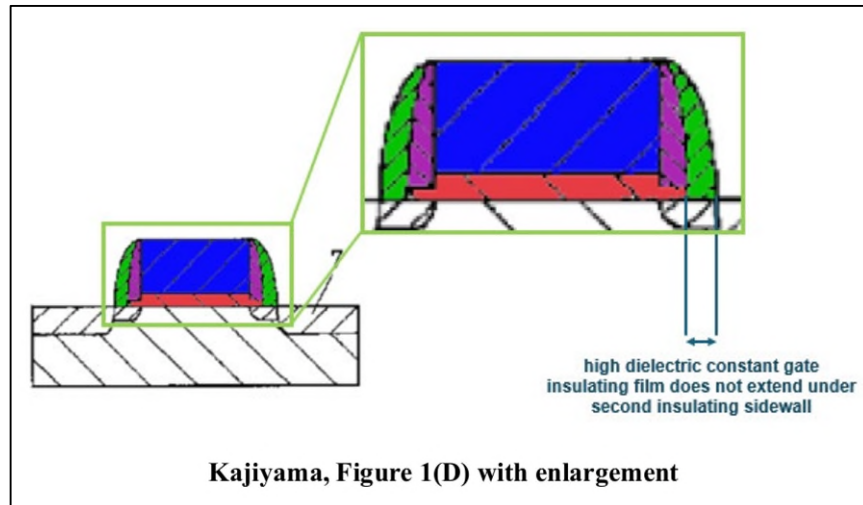


First sidewall 5 (see Ex.1011, FIG. 1(B) (above, top-right) (shaded purple)) is then formed on the side of gate electrode 3 and over the thinner portion of the high-k film. Ex.1011, ¶30. The high-k film is then etched “to remove all.” Ex.1011, ¶30. That is, the high-k film outside the outer edge of sidewall 5 is removed. Ex.1101, ¶¶229. Next, second sidewall 6 (see Ex.1011, FIG. 1(C) (above, bottom) (shaded green)) is formed “to cover the first sidewall 5 [shaded purple] provided on the sidewall of the gate electrode 3 [shaded blue].” Ex.1011, ¶31. As shown above, a portion of the high-k dielectric film (see *id.*, FIGS. 1(A)-(C) (above) (shaded red)) remains under the gate electrode and first sidewall 5 but does not extend under sidewall 6. Ex.1101, ¶¶229.

C. Claim 2

As shown in the enlargement of Figure 1(D) below, the high-k dielectric film (see Ex.1011, FIG. 1(D) (below) (shaded red)) remains under only the gate electrode

and the first sidewall—it is not “*located under the second insulating sidewall*” [2] (sidewall 6, shaded green). See *Unified*, 2022 WL 500391, at *17; Ex.1101, ¶¶231. The fabrication process, discussed in §IX.B.4, confirms the structure illustrated in Figure 1(D). See Ex.1011, ¶¶30-31; Ex.1101, ¶¶232-33.



X. GROUND VI: Kajiyama Renders Claim 14 Obvious.

A. Claim 14

Kajiyama renders “*the high dielectric constant gate insulating film is formed of a Hf based oxide*” [14] obvious. Ex.1101, ¶¶234-38.

Kajiyama discloses that, while the gate insulating film 2 in the first embodiment is a ZrO_2 film, “other high dielectric films, such as a **HfO₂** film, a Ta_2O_5 film, or Al_2O_3 film, can be used instead to obtain the effects of the invention.” Ex.1011, ¶45. A POSITA would have been motivated to select HfO_2 as the high-k material for Kajiyama’s gate dielectric for the reasons discussed in §VI.C with

Petition for *Inter Partes* Review of U.S. Patent No. 7,579,227

respect to the combination of Matsumoto and Wang. Ex.1101, ¶¶236-38; Ex.1337, 2.4.1; Ex.1213, 207; Ex.1349, 6.1.2.

XI. Mandatory Notices

A. Real Party-in-Interest (37 C.F.R. §42.8(b)(1))

The Petitioner and real parties-in-interest are United Microelectronics Corporation and UMC Group (USA).

B. Related Matters (37 C.F.R. §42.8(b)(2))

To the best of Petitioner's knowledge, the '227 patent is subject of the following active proceedings:

- *Advanced Integrated Circuit Process LLC v. United Microelectronics Corporation*, Civil Action No. 2:24-cv-00730 in the Eastern District of Texas (Lead Case), filed September 6, 2024;
- *Advanced Integrated Circuit Process LLC v. Taiwan Semiconductor Manufacturing Company Limited*, Civil Action No. 2:24-cv-00623 in the Eastern District of Texas (Consolidated Member Case), filed August 1, 2024; and
- *Taiwan Semiconductor Manufacturing Company, Ltd. v. Advanced Integrated Circuit Process LLC*, IPR2025-00828 in the U.S. Patent and Trademark Office, Patent Trial and Appeal Board, filed April 15, 2025.

C. Lead and Back-up Counsel (37 C.F.R. §42.8(b)(3))

Pursuant to 37 C.F.R. §§42.8(b)(3) and 42.10(a), Petitioner appoints the following lead and back-up counsel:

Lead Counsel	Back Up Counsel
Tim Tingkang Xia (No. 45,242) Tim.Xia@troutman.com TROUTMAN PEPPER LOCKE LLP 600 Peachtree Street, NE, Suite 3000 Atlanta, GA 30308 Telephone: (404) 870-4698	Emma A. Bennett (No. 80,631) Emma.Bennett@troutman.com TROUTMAN PEPPER LOCKE LLP 600 Travis Street, Suite 2800 Houston, TX 77002 Telephone: (713) 226-1549

D. Service Information (37 C.F.R. §42.8(b)(4))

Service information is provided in the designation of counsel above. Petitioner consents to electronic service by email to Tim.Xia@troutman.com and Emma.Bennett@troutman.com.

E. Payment of Fees (37 C.F.R. §42.103)

The Office is authorized to charge the fee set forth in 37 C.F.R. §42.15(a)(1) for this Petition to Deposit Account No. DA201507. Review of five claims is requested. The undersigned further authorizes payment for any additional fees that may be due in connection with this Petition.

XII. Conclusion

For the reasons set forth above, *Inter Partes* Review of the Challenged Claims of the '227 patent is respectfully requested.

Petition for *Inter Partes* Review of U.S. Patent No. 7,579,227

Respectfully submitted,

Date: June 2, 2025

/s/ Tim Tingkang Xia
Tim Tingkang Xia (Lead Counsel)
Registration No. 45,242
Counsel for Petitioner

CERTIFICATE OF COMPLIANCE WITH WORD COUNT

Pursuant to 37 C.F.R. §42.24(d), I certify that this Petition complies with the type-volume limits of 37 C.F.R. §42.24(a)(1)(i) because it contains 7,864 words, according to the word-processing system used to prepare this Petition, excluding the parts of this Petition that are exempted by 37 C.F.R. §42.24(a)(1) (table of contents, table of authorities, mandatory notices under §42.8, certificate of service, certificate of word count, or appendix of exhibits or claim listing).

Date: June 2, 2025

/s/ Tim Tingkang Xia
Tim Tingkang Xia (Lead Counsel)
Registration No. 45,242
Counsel for Petitioner

CERTIFICATE OF SERVICE

Pursuant to 37 C.F.R. §42.6(e), this is to certify that on this 2nd day of June 2025, I caused to be served on a USB thumb drive a true and correct copy of the foregoing Petition for *Inter Partes* Review of U.S. Patent No. 7,579,227 Under 35 U.S.C. §§311, 312 and 37 C.F.R. §42.104 (with Exs. 1001-1002, 1009-1013, 1018, 1019, 1101-1111, 1211, 1213, 1216, 1223, 1226-1227, 1229, 1305, 1323, 1333-1334, 1337-1338, 1340-1341, 1349, 1406, 1413, 1419, 1429-1435, 1506, 1512, 1515-1529, 1531-1532) via Federal Express Priority Overnight at the Correspondence Address for Patent Owner:

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/s/ Tim Tingkang Xia
Tim Tingkang Xia (Lead Counsel)
Registration No. 45,242
Counsel for Petitioner

Appendix: Challenged Claims Listing

1. **Preamble:** A semiconductor device comprising:

Limitation 1[a]: a high dielectric constant gate insulating film formed on an active region in a substrate;

Limitation 1[b]: a gate electrode formed on the high dielectric constant gate insulating film; and

Limitation 1[c]: an insulating sidewall formed on each side surface of the gate electrode,

Limitation 1[d]: wherein the high dielectric constant gate insulating film is continuously formed so as to extend from under the gate electrode to under the insulating sidewall,

Limitation 1[e]: at least part of the high dielectric constant gate insulating film located under the insulating sidewall has a smaller thickness than a thickness of part of the high dielectric constant gate insulating film located under the gate electrode,

Limitation 1[f]: the insulating sidewall includes a first insulating sidewall formed on a side surface of the gate electrode and a second insulating sidewall formed on the side surface of the gate electrode with the first insulating sidewall interposed therebetween,

Limitation 1[g]: the high dielectric constant gate insulating film is continuously formed so as to extend from under the gate electrode to under the first insulating sidewall, and

Limitation 1[h]: part of the high dielectric constant gate insulating film located under the first insulating sidewall has a smaller thickness than a thickness of part of the high dielectric constant gate insulating film located under the gate electrode.

2. **Limitation 2:** The semiconductor device of claim 1, wherein the high dielectric constant gate insulating film is formed so as not to be located under the second insulating sidewall.
7. **Limitation 7:** The semiconductor device of claim 1, further comprising a buffer insulating film between the substrate and the high dielectric constant gate insulating film.
8. **Limitation 8:** The semiconductor device of claim 7, wherein the buffer insulating film is a silicon oxide film or a silicon oxynitride film.
14. **Limitation 14:** The semiconductor device of claim 1, wherein the high dielectric constant gate insulating film is formed of a Hf based oxide.