EXHIBIT 227-02: Invalidity of U.S. Patent No. 7,579,227 (the ’227 Patent) Based on *Kajiyama*

The following list illustrates certain grounds for invalidity based on:

- Japanese Application JP2003-258241 to Kajiyama (“JP-Kajiyama”), published September 12, 2003, is prior art to U.S. Patent No. 7,579,227 (the “’227 patent”) under at least 35 U.S.C. §102(b). A certified translation of JP-Kajiyama (“*Kajiyama*”) is provided.

Kajiyama, including any material incorporated by reference into *Kajiyama*, anticipates at least claims 1-2, 7-8, and 14 of the ’227 patent under pre-AIA 35 U.S.C. §102(b).

To the extent any limitation is found not to be expressly or inherently disclosed in *Kajiyama*, such a limitation would have been obvious either based on *Kajiyama* alone, given the state of the art, or in combination with one or more of the references cited in Exhibits 227-01 and 227-03 through 227-13, because the ’227 patent is merely a collection of prior art elements that fails to meet the statutory requirement of non-obviousness under 35 U.S.C. § 103, and the factors delineated in *KSR Int’l Co. v. Teleflex, Inc.*, 550 U.S. 398 (2007), weigh against a finding of non-obviousness.

In particular, any disclosures identified for each limitation of the ’227 patent in the aforementioned Exhibits may be combined with the disclosures of *Kajiyama* identified below for the same limitation to render that limitation obvious. A POSITA would have found such a combination / modification obvious for the reasons discussed herein and in Defendant’s cover pleading.[1]

The citations to portions of any reference in this chart are exemplary only. Citations to the written description should be interpreted to include the figures associated with or relevant to the cited passages. Similarly, citations to a figure should be understood to encompass any description, text, or discussion of that figure. Defendant reserves the right to use the entirety of any reference cited in this chart to

[1] Plaintiff appears in many instances to be pursuing overly broad constructions of limitations of the asserted claims in an effort to piece together an infringement claim where none exists. This claim chart accounts for overly broad construction of the claim limitations. Any assertion that a particular limitation is disclosed by a prior art reference or references may be based on Plaintiff’s apparent constructions and is not intended to be, and is not, an admission that such constructions are supportable or proper. Defendant is investigating this prior art and has not yet completed discovery from third parties, who may have relevant information concerning the prior art. Therefore, Defendant reserves the right to supplement this chart after additional discovery is received. To the extent that any of the prior art discloses the same or similar functionality or feature(s) of any of the accused products, Defendant reserves the right to argue that said feature or functionality does not practice any limitation of any of the asserted claims, and to argue, in the alternative, that if said feature or functionality is found to practice any limitation of any of the asserted claims, then the prior art reference teaches the limitation and that the claim is not patentable.

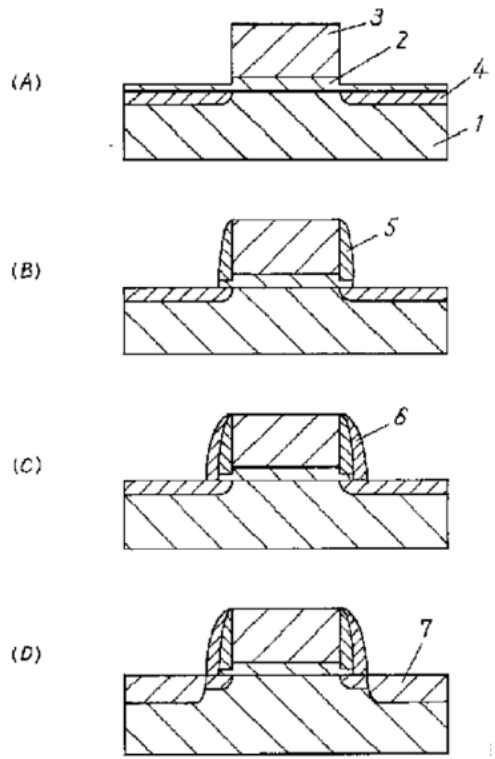
show that the asserted claims are anticipated and/or are obvious. Citations presented for one claim limitation are expressly incorporated by reference into all other limitations for that claim as well as all limitations of all claims on which that claim depends.

U.S. Patent No. 7,579,227	**Exemplary Disclosures Relevant to *Kajiyama***
Claim 1	
[1pre] A semiconductor device comprising:	*Kajiyama*, alone or in combination with one or more references, discloses or suggests a semiconductor device. For example, *Kajiyama* discloses the following at Title: SEMICONDUCTOR DEVICE AND ITS MANUFACTURING METHOD *Kajiyama* discloses the following at Summary: The task aimed to be solved is to provide semiconductor devices and manufacturing methods that suppress pressure resistance defects and reliability degradation of high dielectric gate dielectric films, and prevent the reduction of high specific dielectric constants. *Kajiyama* discloses the following at claim 1: In a semiconductor device that functions as a MOSFET, A semiconductor device characterized … *Kajiyama* discloses the following at claims 5, 8: A/In method for manufacturing a semiconductor device that functions as a MOSFET

U.S. Patent No. 7,579,227	Exemplary Disclosures Relevant to *Kajiyama*
	Kajiyama discloses the following at ¶ 1: The present invention relates to a semiconductor device and a method for manufacturing the same, and more particularly to an insulated gate field effect transistor having a gate insulating film made of a high dielectric constant material (high dielectric constant material). *Kajiyama* discloses the following at ¶ 13: The present invention is made in consideration of the above problems, and is intended to provide semiconductor devices and manufacturing methods thereof that suppress pressure resistance defects and reliability degradation of high dielectric gate insulating films and prevent the reduction of high specific dielectric constants. *Kajiyama* discloses the following at ¶ 14: To achieve the above objectives, the semiconductor device of the present invention is characterized in that in a semiconductor device that functions as a MOSFET, the semiconductor device comprises ….
[1A] a high dielectric constant gate insulating film formed on an active region in a substrate;	*Kajiyama*, alone or in combination with one or more references, discloses or suggests a high dielectric constant gate insulating film formed on an active region in a substrate. For example: *Kajiyama* discloses the following at claim 1: A semiconductor device characterized in that it comprises a gate insulating film consisting of a high dielectric film formed on a semiconductor substrate

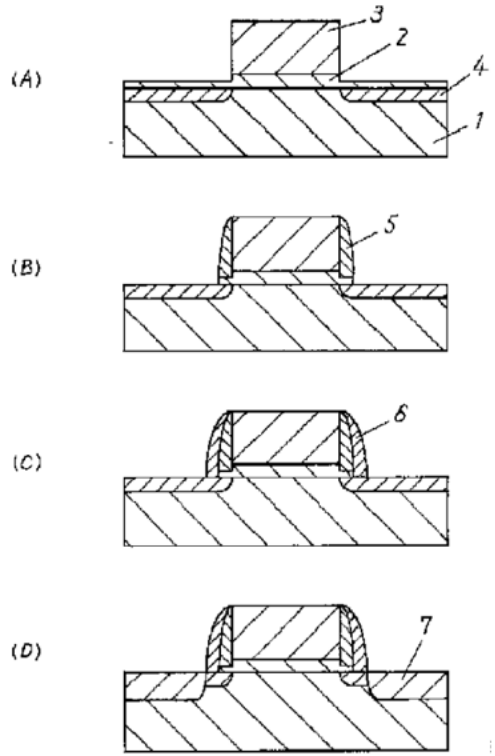
	Kajiyama discloses the following at claim 8: > forming a gate insulating film made of a high dielectric film on a semiconductor substrate; *Kajiyama* discloses the following at ¶ 2: > To avoid this problem, research is being conducted on MOSFETs that have a gate insulating film (hereinafter referred to as a high dielectric gate insulating film) consisting of a high dielectric using a zirconium oxide film (hereinafter referred to as a ZrO_2 film) or the like. *Kajiyama* discloses the following at ¶ 14: > In order to achieve the above object, the semiconductor device of the present invention is characterized in that, in a semiconductor device functioning as a MOSFET, it comprises a gate insulating film made of a high dielectric film formed on a semiconductor substrate, a gate electrode made of a conductive film formed on the gate insulating film, a first sidewall made of a dielectric film formed on the side wall of the gate electrode, and a second sidewall made of an oxidation-resistant film formed so as to cover the first sidewall. *Kajiyama* discloses the following at ¶ 15: > With this configuration, pressure resistance failure and reliability deterioration due to loss of film or damage of high dielectric gate insulating film can be suppressed. Furthermore, since an ultra-thin SiO2 film is not formed at the Si interface in a later process, it is possible to prevent a decrease in the specific dielectric constant of the high dielectric gate insulating film. *Kajiyama* discloses the following at ¶¶ 27-28:

U.S. Patent No. 7,579,227	Exemplary Disclosures Relevant to *Kajiyama*
	Fig. 1 is a cross-sectional view illustrating a manufacturing process of a semiconductor device that functions as an n-type MOSFET according to a first embodiment of the present invention. In Fig. 1, 1 is a p-type Si substrate, 2 is a high dielectric gate insulating film consisting of ZrO_2 film, 3 is a gate electrode consisting of n-type polySi film, 4 is an LDD diffusion layer consisting of n-type, 5 is a first sidewall consisting of ZrO_2 film (insulation film), 6 is a silicon nitride film (oxidation resistant film, hereinafter referred to as Si_3N_4 film), and 7 is an n+-type source drain diffusion layer. *Kajiyama* discloses the following at ¶ 29: First, as shown in Fig. 1(A), after forming an element separation layer (not shown) on the Si substrate 1 having a (100) surface, reactive sputtering is performed on the metal target consisting of Zr in the atmosphere of a mixture of argon gas and oxygen gas to form a ZrO_2 film 2 on the Si substrate 1 that becomes a high dielectric gate insulating film, for example, at a thickness of about 5 nm. *Kajiyama* discloses the following at ¶ 5: First, as shown in Figure 4(A), after forming an element separation layer (not shown) on the Si substrate 21 consisting of a silicon monocrystalline of type p having a (100) surface, the Si substrate 21 is thermally oxidized to form a SiO_2 film 22 that becomes a gate insulating film.

	Kajiyama discloses the following at Figures 1(A)-(D):  *Kajiyama* discloses the following at ¶ 45: In the first to second embodiments, a ZrO_2 film was used for the high dielectric gate insulating film, but it goes without saying that other high dielectric films, such as a HfO_2 film, a Ta_2O_5 film, or a Al_2O_3 film, can be used instead to obtain the effects of the invention. Furthermore, the effects of the present invention can also be obtained by using a silicate film consisting of a high dielectric and a silicon triage compound in a high dielectric gate insulating film.

U.S. Patent No. 7,579,227	Exemplary Disclosures Relevant to *Kajiyama*
[1B] a gate electrode formed on the high dielectric constant gate insulating film; and	*Kajiyama*, alone or in combination with one or more references, discloses or suggests a gate electrode formed on the high dielectric constant gate insulating film. For example: *Kajiyama* discloses the following at claim 1: A semiconductor device characterized in that it comprises a gate insulating film consisting of a high dielectric film formed on a semiconductor substrate, a gate electrode consisting of a conductive film formed on the gate insulating film, *Kajiyama* discloses the following at claim 5: A method for manufacturing a semiconductor device that functions as a MOSFET, comprising the steps of: (a) forming a gate insulating film made of a high dielectric film on a semiconductor substrate; (b) forming a gate electrode made of a conductive film on the gate insulating film; *Kajiyama* discloses the following at ¶ 14: In order to achieve the above object, the semiconductor device of the present invention is characterized in that, in a semiconductor device functioning as a MOSFET, it comprises a gate insulating film made of a high dielectric film formed on a semiconductor substrate, a gate electrode made of a conductive film formed on the gate insulating film, a first sidewall made of a dielectric film formed on the side wall of the gate electrode, and a second sidewall made of an oxidation-resistant film formed so as to cover the first sidewall.

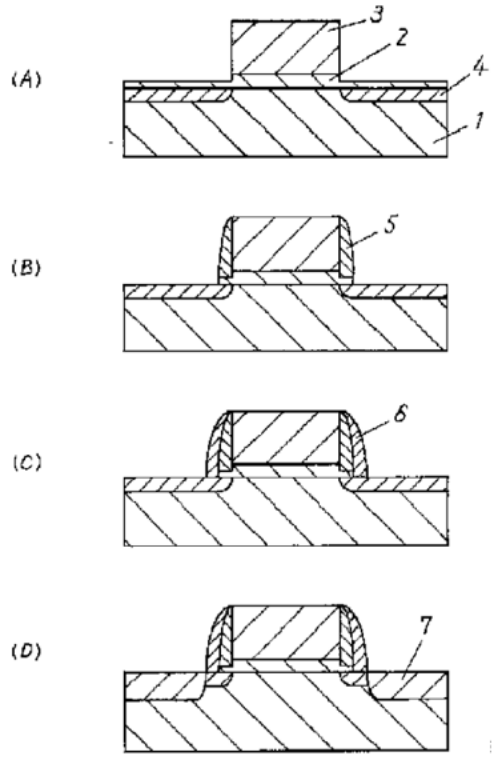
	Kajiyama discloses the following at ¶ 28: In Fig. 1, 1 is a p-type Si substrate, 2 is a high dielectric gate insulating film consisting of ZrO_2 film, 3 is a gate electrode consisting of n-type polySi film, 4 is an LDD diffusion layer consisting of n-type, 5 is a first sidewall consisting of ZrO_2 film (insulation film), 6 is a silicon nitride film (oxidation resistant film, hereinafter referred to as Si_3N_4 film), and 7 is an n+-type source drain diffusion layer. *Kajiyama* discloses the following at ¶ 29: First, as shown in Fig. 1(A), after forming an element separation layer (not shown) on the Si substrate 1 having a (100) surface, reactive sputtering is performed on the metal target consisting of Zr in the atmosphere of a mixture of argon gas and oxygen gas to form a ZrO_2 film 2 on the Si substrate 1 that becomes a high dielectric gate insulating film, for example, at a thickness of about 5 nm. Thereafter, an n-type polySi film is deposited on the ZrO_2 film 2 by C VD method, for example at a film thickness of about 200 to 300 nm, and then a resist film (not shown) is RIEd to the mask to form a gate electrode 3 on the ZrO_2 film 2. At this time, the ZrO_2 film 2 of the base film is also etched to reduce the film as in the conventional case. Also, etch damage causes damage to the surface of ZrO_2 film 2. After removing the resist membrane, gate electrode 3 is ion-implanted with, for example, arsenic to the mask to form an n-type L DD diffusion layer 4 on the surface of Si substrate 1. *Kajiyama* discloses the following at Figures 1(A)-(D):

U.S. Patent No. 7,579,227	Exemplary Disclosures Relevant to *Kajiyama*
	

U.S. Patent No. 7,579,227	Exemplary Disclosures Relevant to *Kajiyama*
[1C] an insulating sidewall formed on each side surface of the gate electrode,	*Kajiyama*, alone or in combination with one or more references, discloses or suggests an insulating sidewall formed on each side surface of the gate electrode. For example: *Kajiyama* discloses the following at [Solution method]: > As a first sidewall consisting of a dielectric film is formed on the sidewall after the formation of a gate electrode, it is possible to suppress pressure resistance defects and reliability deterioration due to loss of the film or damage of the high dielectric gate insulating film. In addition, a second sidewall consisting of an oxidative resistant film is formed over the first sidewall, so that an ultra-thin SiO_2 film is not formed at the Si interface in a later step. *Kajiyama* discloses the following at claim 1: > A semiconductor device characterized in that it comprises a gate insulating film consisting of a high dielectric film formed on a semiconductor substrate, a gate electrode consisting of a conductive film formed on the gate insulating film, a first sidewall consisting of a dielectric film formed on a sidewall of the gate electrode, and a second sidewall consisting of an oxidizing resistant film formed over the first sidewall. *Kajiyama* discloses the following at claim 8: > forming a first sidewall consisting only of a dielectric film on a sidewall of the gate electrode (d); > forming a second sidewall (e) consisting of an oxidation resistant film over the first sidewall.

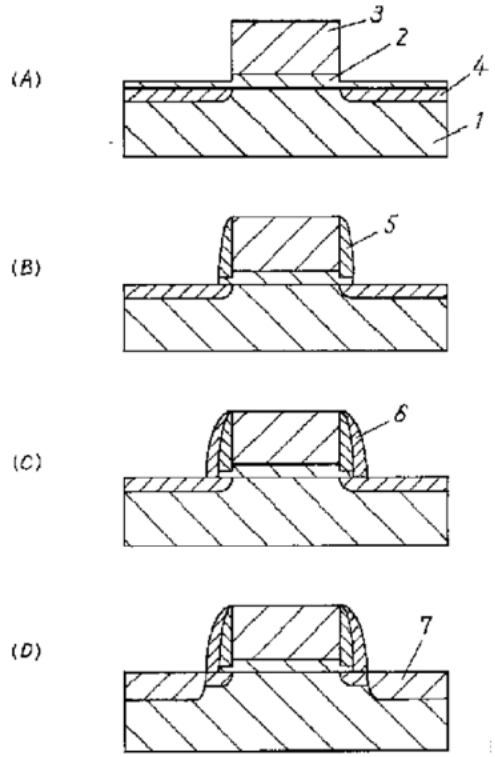
	Kajiyama discloses the following at ¶ 14: In order to achieve the above object, the semiconductor device of the present invention is characterized in that, in a semiconductor device functioning as a MOSFET, it comprises a gate insulating film made of a high dielectric film formed on a semiconductor substrate, a gate electrode made of a conductive film formed on the gate insulating film, a first sidewall made of a dielectric film formed on the side wall of the gate electrode, and a second sidewall made of an oxidation-resistant film formed so as to cover the first sidewall. *Kajiyama* discloses the following at ¶ 28: In Fig. 1, 1 is a p-type Si substrate, 2 is a high dielectric gate insulating film consisting of ZrO_2 film, 3 is a gate electrode consisting of n-type polySi film, 4 is an LDD diffusion layer consisting of n-type, 5 is a first sidewall consisting of ZrO_2 film (insulation film), 6 is a silicon nitride film (oxidation resistant film, hereinafter referred to as Si_3N_4 film), and 7 is an n+-type source drain diffusion layer. *Kajiyama* discloses the following at ¶ 30: Next, as shown in Fig. 1(B), after depositing a ZrO_2 film that is reactive sputtering and becomes an insulating film over the gate electrode 3 at a film thickness of, for example, about 20 to 100 nm, RIE is performed on this ZrO_2 film to form a first sidewall 5 consisting of a ZrO_2 film on the side of the gate electrode 3. *Kajiyama* discloses the following at ¶ 31: Next, as shown in Fig. 1(C), after depositing a Si_3N_4 film that becomes an oxidizing resistant film over the gate electrode 3 by means of a CVD method at a film thickness of, for example, about 50 to 200 nm, a RIE is performed on the Si_3N_4 film to form a second sidewall 6 to cover the first sidewall 5 provided on the sidewall of the gate electrode 3. In this way, the sidewalls of the gate electrode 3 are covered by a second sidewall 6 consisting of a Si_3N_4 film, such that heat treatment or deposition of an

U.S. Patent No. 7,579,227	Exemplary Disclosures Relevant to *Kajiyama*
	insulating film in an atmosphere comprising oxidation or oxygen gas after this step does not form an ultra-thin SiO_2 film at the Si interface. *Kajiyama* discloses the following at ¶ 33: As described above, according to the first embodiment, a first sidewall consisting of a ZrO_2 film is formed in the sidewall after the formation of gate electrode 3, so that pressure resistance failure and reliability deterioration due to film loss and damage of the high dielectric gate insulating film can be suppressed. Furthermore, a second sidewall 6 consisting of Si_3N_4 films is formed to cover the first sidewall 5, so that an ultra-thin SiO_2 film is not formed at the Si interface in a later step. *Kajiyama* discloses the following at ¶ 47: Also described using the same ZrO_2 film as the high dielectric gate insulating film on the first sidewall, but instead, the effects of the present invention can be obtained even with other dielectric films, such as TEOS films, BPSG films, or SiO N films.

U.S. Patent No. 7,579,227	Exemplary Disclosures Relevant to *Kajiyama*
	Kajiyama discloses the following at Figures 1(A)-(D): 

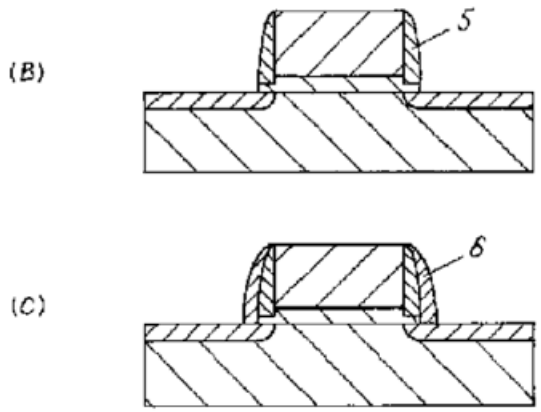
U.S. Patent No. 7,579,227	Exemplary Disclosures Relevant to *Kajiyama*
[1D] wherein the high dielectric constant gate insulating film is continuously formed so as to extend from under the gate electrode to under the insulating sidewall,	*Kajiyama*, alone or in combination with one or more references, discloses or suggests the high dielectric constant gate insulating film is continuously formed so as to extend from under the gate electrode to under the insulating sidewall. For example: *Kajiyama* discloses the following at ¶ 29: > First, as shown in Fig. 1(A), after forming an element separation layer (not shown) on the Si substrate 1 having a (100) surface, reactive sputtering is performed on the metal target consisting of Zr in the atmosphere of a mixture of argon gas and oxygen gas to form a ZrO_2 film 2 on the Si substrate 1 that becomes a high dielectric gate insulating film, for example, at a thickness of about 5 nm. Thereafter, an n-type polySi film is deposited on the ZrO_2 film 2 by C VD method, for example at a film thickness of about 200 to 300 nm, and then a resist film (not shown) is RIEd to the mask to form a gate electrode 3 on the ZrO_2 film 2. At this time, the ZrO_2 film 2 of the base film is also etched to reduce the film as in the conventional case. Also, etch damage causes damage to the surface of ZrO_2 film 2. After removing the resist membrane, gate electrode 3 is ion-implanted with, for example, arsenic to the mask to form an n-type L DD diffusion layer 4 on the surface of Si substrate 1. *Kajiyama* discloses the following at ¶ 30: > Next, as shown in Fig. 1(B), after depositing a ZrO_2 film that is reactive sputtering and becomes an insulating film over the gate electrode 3 at a film thickness of, for example, about 20 to 100 nm, RIE is performed on this ZrO_2 film to form a first sidewall 5 consisting of a ZrO_2 film on the side of the gate electrode 3. At this time, the ZrO_2 film 2 of the base film is also etched at the same time to remove all. In this way, the film loss is eliminated because the ZrO_2 film is again deposited on the ZrO_2 film 2 that has been reduced by etching at the lower edge of the gate electrode 3. In addition, damage to the surface of the ZrO_2 film 2 is restored by redeposition. Therefore, as with

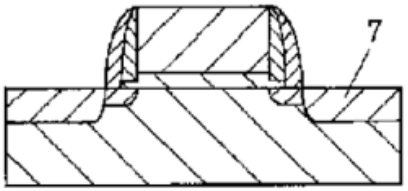
U.S. Patent No. 7,579,227	Exemplary Disclosures Relevant to *Kajiyama*
	conventional examples of forming gate birds beaks, it is possible to suppress pressure resistance defects and reliability degradation of high dielectric gate insulating films. *Kajiyama* discloses the following at ¶ 31: Next, as shown in Fig. 1(C), after depositing a Si_3N_4 film that becomes an oxidizing resistant film over the gate electrode 3 by means of a CVD method at a film thickness of, for example, about 50 to 200 nm, a RIE is performed on the Si_3N_4 film to form a second sidewall 6 to cover the first sidewall 5 provided on the sidewall of the gate electrode 3. In this way, the sidewalls of the gate electrode 3 are covered by a second sidewall 6 consisting of a Si_3N_4 film, such that heat treatment or deposition of an insulating film in an atmosphere comprising oxidation or oxygen gas after this step does not form an ultra-thin SiO_2 film at the Si interface. Therefore, it is possible to prevent a decrease in the specific dielectric constant due to the formation of an ultra-thin SiO_2 film, which is problematic in the case of a high dielectric gate insulating film.

U.S. Patent No. 7,579,227	Exemplary Disclosures Relevant to *Kajiyama*
	Kajiyama discloses the following at Figures 1(A)-(D): 
[1E] at least part of the high dielectric constant gate insulating film located under the insulating sidewall has a smaller thickness than a thickness of	*Kajiyama*, alone or in combination with one or more references, discloses or suggests at least part of the high dielectric constant gate insulating film located under the insulating sidewall has a smaller

U.S. Patent No. 7,579,227	Exemplary Disclosures Relevant to *Kajiyama*
part of the high dielectric constant gate insulating film located under the gate electrode,	thickness than a thickness of part of the high dielectric constant gate insulating film located under the gate electrode. For example, *see* limitation 1[D], *supra*.
[1F] the insulating sidewall includes a first insulating sidewall formed on a side surface of the gate electrode and a second insulating sidewall formed on the side surface of the gate electrode with the first insulating sidewall interposed therebetween,	*Kajiyama*, alone or in combination with one or more references, discloses or suggeststhe insulating sidewall includes a first insulating sidewall formed on a side surface of the gate electrode and a second insulating sidewall formed on the side surface of the gate electrode with the first insulating sidewall interposed therebetween. For example: *See* limitation [1C]. *Kajiyama* discloses the following at ¶ 30: > Next, as shown in Fig. 1(B), after depositing a ZrO_2 film that is reactive sputtering and becomes an insulating film over the gate electrode 3 at a film thickness of, for example, about 20 to 100 nm, RIE is performed on this ZrO_2 film to form a first sidewall 5 consisting of a ZrO_2 film on the side of the gate electrode 3. At this time, the ZrO_2 film 2 of the base film is also etched at the same time to remove all. In this way, the film loss is eliminated because the ZrO_2 film is again deposited on the ZrO_2 film 2 that has been reduced by etching at the lower edge of the gate electrode 3. In addition, damage to the surface of the ZrO_2 film 2 is restored by redeposition. Therefore, as with conventional examples of forming gate birds beaks, it is possible to suppress pressure resistance defects and reliability degradation of high dielectric gate insulating films. *Kajiyama* discloses the following at ¶ 31: > Next, as shown in Fig. 1(C), after depositing a Si_3N_4 film that becomes an oxidizing resistant film over the gate electrode 3 by means of a CVD method at a film thickness

U.S. Patent No. 7,579,227	Exemplary Disclosures Relevant to *Kajiyama*
	of, for example, about 50 to 200 nm, a RIE is performed on the Si_3N_4 film to form a second sidewall 6 to cover the first sidewall 5 provided on the sidewall of the gate electrode 3. In this way, the sidewalls of the gate electrode 3 are covered by a second sidewall 6 consisting of a Si_3N_4 film, such that heat treatment or deposition of an insulating film in an atmosphere comprising oxidation or oxygen gas after this step does not form an ultra-thin SiO_2 film at the Si interface. Therefore, it is possible to prevent a decrease in the specific dielectric constant due to the formation of an ultra-thin SiO_2 film, which is problematic in the case of a high dielectric gate insulating film. *Kajiyama* discloses the following at ¶ 33: As described above, according to the first embodiment, a first sidewall consisting of a ZrO_2 film is formed in the sidewall after the formation of gate electrode 3, so that pressure resistance failure and reliability deterioration due to film loss and damage of the high dielectric gate insulating film can be suppressed. Furthermore, a second sidewall 6 consisting of Si_3N_4 films is formed to cover the first sidewall 5, so that an ultra-thin SiO_2 film is not formed at the Si interface in a later step.

U.S. Patent No. 7,579,227	Exemplary Disclosures Relevant to *Kajiyama*
	Kajiyama discloses the following at Figures 1(B)-(C): 
[1G] the high dielectric constant gate insulating film is continuously formed so as to extend from under the gate electrode to under the first insulating sidewall, and	*Kajiyama*, alone or in combination with one or more references, discloses or suggests the high dielectric constant gate insulating film is continuously formed so as to extend from under the gate electrode to under the first insulating sidewall. For example, *see* limitation 1[D] *supra*.
[1H] part of the high dielectric constant gate insulating film located under the first insulating sidewall has a smaller thickness than a thickness of part of the high dielectric constant gate insulating film	*Kajiyama*, alone or in combination with one or more references, discloses or suggests part of the high dielectric constant gate insulating film located under the first insulating sidewall has a smaller thickness than a thickness of part of the high dielectric constant gate insulating film located under the gate electrode. For example, *see* limitations 1[D] and 1[E] *supra*.

U.S. Patent No. 7,579,227	Exemplary Disclosures Relevant to *Kajiyama*
located under the gate electrode.	
Claim 2	
2. The semiconductor device of claim 1, wherein the high dielectric constant gate insulating film is formed so as not to be located under the second insulating sidewall.	*Kajiyama*, alone or in combination with one or more references, discloses or suggests the semiconductor device of claim 1. *See* claim 1, *supra*. *Kajiyama*, alone or in combination with one or more references, discloses or suggests the high dielectric constant gate insulating film is formed so as not to be located under the second insulating sidewall. For example, *Kajiyama* discloses the following at Figure 1(D): (D)  *See also* limitations 1[D] and 1[E], *supra*.
Claim 7	
7. The semiconductor device of claim 1, further comprising a buffer insulating film between the substrate and the high	*Kajiyama*, alone or in combination with one or more references, discloses or suggests the semiconductor device of claim 1. *See* claim 1, *supra*. *Kajiyama*, alone or in combination with one or more references, discloses or suggests a buffer insulating film between the substrate and the high dielectric constant gate insulating film.

U.S. Patent No. 7,579,227	Exemplary Disclosures Relevant to *Kajiyama*
dielectric constant gate insulating film.	
Claim 8	
8. The semiconductor device of claim 7, wherein the buffer insulating film is a silicon oxide film or a silicon oxynitride film.	*Kajiyama*, alone or in combination with one or more references, discloses or suggests the semiconductor device of claim 7. *See* claim 7, *supra*. *Kajiyama*, alone or in combination with one or more references, discloses or suggests the buffer insulating film is a silicon oxide film or a silicon oxynitride film.
Claim 14	
14. The semiconductor device of claim 1, wherein the high dielectric constant gate insulating film is formed of a Hf based oxide.	*Kajiyama*, alone or in combination with one or more references, discloses or suggests the semiconductor device of claim 1. *See* claim 1, *supra*. *Kajiyama*, alone or in combination with one or more references, discloses or suggests the high dielectric constant gate insulating film is formed of a Hf based oxide. For example: *Kajiyama* discloses the following at ¶ 45: > In the first to second embodiments, a ZrO_2 film was used for the high dielectric gate insulating film, but it goes without saying that other high dielectric films, such as a HfO_2 film, a Ta_2O_5 film, or a Al_2O_3 film, can be used instead to obtain the effects of the invention. Furthermore, the effects of the present invention can also be obtained by using a silicate film consisting of a high dielectric and a silicon triage compound in a high dielectric gate insulating film.