

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

TAIWAN SEMICONDUCTOR MANUFACTURING COMPANY LTD.,

Petitioner,

v.

ADVANCED INTEGRATED CIRCUIT PROCESS LLC,

Patent Owner.

IPR2025-00828

U.S. Patent 7,579,227

**PETITION FOR *INTER PARTES* REVIEW OF
U.S. PATENT 7,579,227**

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EXHIBIT LIST

Exhibit	Description
1001	U.S. Patent 7,579,227 to Hirase, et al. (“the ’227 patent”)
1002	File History of U.S. Patent 7,579,227 (“’227 File History”)
1003	Declaration of Dr. Jack Lee in Support of IPR Petition
1004	CV of Dr. Jack Lee
1005	Translated Excerpts from JP File History
1006	Reserved
1007	Reserved
1008	Reserved
1009	U.S. Publication 2003/0025135 to Matsumoto, et al. (“Matsumoto”)
1010	JP2003-258241 to Kajiyama (“JP-Kajiyama”)
1011	Certified Translation of JP2003-258241 to Kajiyama (“Kajiyama”)
1012	U.S. Publication 2006/0131672 to Wang, et al. (“Wang”)
1013	U.S. Publication 2005/0051856 to Ono, et al. (“Ono”)
1014	Reserved
1015	Reserved
1016	Reserved
1017	Reserved
1018	Wilk, G. D., et al., “High-k gate dielectrics: Current status and materials properties considerations,” Journal of Applied Physics, Vol. 89, No. 10, pp. 5243-75, May 15, 2001 (“Wilk”)

Exhibit	Description
1019	U.S. Publication 2005/0045938 to Mutou, et al. (“Mutou”)
1020	Reserved
1021	Reserved
1022	Reserved
1023	U.S. Patent 6,306,712 to Rodder, et al. (“Rodder”)
1024	Reserved
1025	Reserved
1026	Reserved
1027	Reserved
1028	Reserved
1029	Reserved
1030	Reserved
1031	Reserved
1032	Houssa, M., “High-κ Gate Dielectrics” (CRC Press 1st Ed. 2003) (“Houssa”)
1033	Plummer, J., et al., “Silicon VLSI Technology: Fundamentals, Practice and Modeling” (Prentice Hall 2000) (“Plummer”)
1034	Wolf, S., “Silicon Processing for the VLSI Era, Volume 4 – Deep-Submicron Process Technology” (Lattice 2002) (“Wolf”)
1035	Reserved
1036	Reserved

Exhibit	Description
1037	Lee, S. J., et al. “High Quality Ultra Thin CVD HfO ₂ Gate Stack with Poly-Si Gate Electrode,” Digest of International Electron Devices Meeting, pp. 31-34, Dec. 10-13, 2000 (“Lee”)
1038	Campbell, “The Science and Engineering of Microelectronic Fabrication”, Second Edition (2001) (“Campbell”)
1039	Reserved
1040	JP2005-064190 to Ono with certified translation (“JP-Ono”)
1041	N. Weste and D. Harris, “CMOS VLSI Design: A Circuits and Systems Perspective”, Third Edition (Pearson/Addison Wesley, 2005) (“Weste”)
1042	U.S. Patent 7,807,990 to Koyama, et al. (“Koyama 990”)
1043	Reserved
1044	Reserved
1045	Reserved
1046	Reserved
1047	Reserved
1048	Reserved
1049	Lee, B.H., et al., “Ultrathin Hafnium Oxide with Low Leakage and Excellent Reliability for Alternative Gate Dielectric Application,” Digest of International Electron Devices Meeting, pp. 133-36, Dec. 5-8, 1999 (“Lee-1999”)
1050	Reserved
1051	U.S. Publication 2005/0139932 to Cho, et al. (“Cho”)

I. Introduction

Taiwan Semiconductor Manufacturing Company Ltd. (“Petitioner” or “TSMC”) petitions for *inter partes* review of claims 1-3, 6-9, and 14 of U.S. Patent 7,579,227 (“the ’227 patent”; TSMC-1001).

The ’227 patent relates “to techniques for improving the driving power and reliability of a MISFET [metal insulator semiconductor field-effect transistor]” by (1) extending a high-k gate insulating film from under the gate electrode to under a sidewall and (2) making the high-k film thicker under the gate electrode than under the sidewall. (TSMC-1001, 1:8-14, 2:1-10, 2:31-38.) These basic concepts were known before the ’227 patent, a fact corroborated by the Examiner and acquiesced to by the Applicant during Japanese prosecution.

Petitioner, supported by the declaration of Dr. Jack Lee, having over three decades of experience, demonstrates the challenged claims are unpatentable.

II. Grounds for Standing

Petitioner certifies the ’227 patent is available for IPR and it is not barred or estopped from requesting IPR on the grounds herein.

III. Identification of Challenge

A. Prior Art

The ’227 patent was filed on July 24, 2006 and claims priority to JP2005-227457 (“JP application”), filed August 5, 2005. Petitioner does not acquiesce the

'227 patent is entitled to priority of the JP application. Regardless, each applied reference was filed or published before August 5, 2005.

1. **U.S. Publication 2003/0025135 to Matsumoto, et al.** (“Matsumoto”; TSMC-1009), published February 6, 2003, is prior art under 35 U.S.C. §102(b).¹

2. **JP2003-258241 to Kajiyama** (“JP-Kajiyama”; TSMC-1010), published September 12, 2003, is prior art under 35 U.S.C. §102(b). A certified translation of JP-Kajiyama (“Kajiyama”) is provided as TSMC-1011.

3. **U.S. Publication 2006/0131672 to Wang, et al.** (“Wang”; TSMC-1012), filed April 27, 2005, is prior art under 35 U.S.C. §102(e).

4. **U.S. Publication 2005/0045938 to Mutou, et al.** (“Mutou”; TSMC-1019), published March 3, 2005, is prior art under 35 U.S.C. §102(b).

5. **U.S. Publication 2005/0051856 to Ono, et al.** (“Ono”; TSMC-1013), published March 10, 2005, is prior art under 35 U.S.C. §102(b).

B. Grounds for Challenge

Ground		Claims	Prior Art
1	103	1-3	Matsumoto
2	103	7-8, 14	Matsumoto + Wang
3	103	7-8	Matsumoto + Mutou

¹ Pre-AIA 35 U.S.C. §102 applies.

Ground		Claims	Prior Art
4	103	6, 14	Matsumoto + Ono
5	102	1, 2	Kajiyama
6	103	9, 14	Kajiyama
7	103	6	Kajiyama + Ono

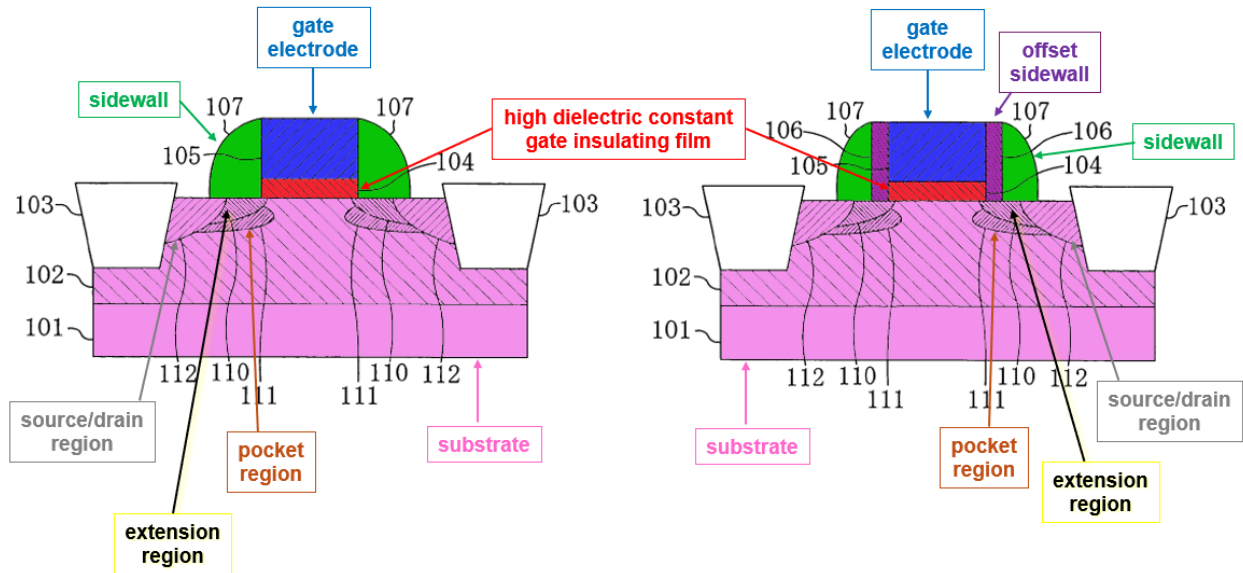
IV. The '227 Patent

A. Applicant Admitted Prior Art (“AAPA”)

The '227 patent recognized that, prior to August 2005, semiconductor devices had used “a high dielectric constant film formed of a Hf based oxide, Al based oxide or the like” as a gate insulating film. (TSMC-1001, 1:17-25.) It describes two exemplary prior art metal insulator semiconductor field-effect transistors (MISFETs), depicted in Figures 16A and 16B, each including a high dielectric constant gate insulating film² 104 (shaded red) interposed between a gate electrode 105 (shaded blue) and the substrate. In the Figure 16A device, an insulating sidewall 107 (shaded green) is formed on each side of gate electrode 105. (TSMC-1001, 1:37-38.) In the Figure 16B device, an additional insulating

² The terms “gate dielectric” and “gate insulating film” are used interchangeably. The term “high dielectric constant” is also referred to as “high-k” in this Petition and prior art documents.

offset sidewall 106 (shaded purple) is interposed between sidewall 107 and gate electrode 105. (TSMC-1001, 1:46-49.)



'227 Patent, Figure³ 16A

'227 Patent, Figure 16B

In these prior art devices, the “side end portions” of the high-k gate insulating film “are in direct contact with sidewalls.” (TSMC-1001, 1:56-59.) The '227 patent purports to address issues with this arrangement by extending the high-k film under the “sidewalls to prevent end portions of the [high-k] film from being in contact with the sidewalls.” (TSMC-1001, 2:5-11.) It also purports to make the high-k film thicker under the gate than under the sidewalls. (TSMC-1001, 2:31-38.)

³ All shading and annotations in figures are added, unless otherwise noted.

However, these basic concepts were well-known. (*See, e.g.*, §§IV.B.2, IV.D.2, V, IX.)

B. Technical Background

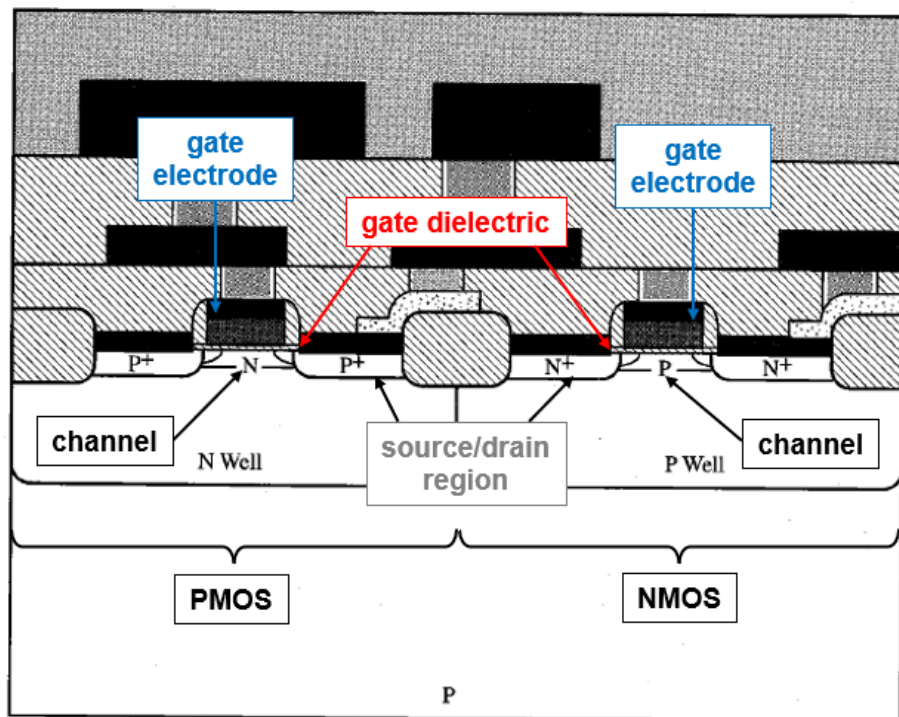
A semiconductor device, at its most basic, exploits the properties of semiconductor materials such as silicon. Many types of semiconductor devices exist including, e.g., diodes and MOS transistors (e.g., field effect transistors (FETs)). (*See, e.g.*, TSMC-1033, 33-41.) For ease of discussion, Petitioner describes FET devices in further detail below. A POSITA would understand the basic concepts in §IV.B apply to other types of semiconductor devices.

1. MISFET/MOSFET

MISFETs⁴ have a **source/drain** for current input/output. (TSMC-1003, ¶36; TSMC-1033, 76-82.) MISFETs like the ones at issue here also have a **gate** above a **channel** region between the source and drain. (TSMC-1003, ¶36; TSMC-1033, 71-76.) The **gate** includes a **gate electrode** and a **gate dielectric** (also referred to as a gate insulating film) that separates the gate electrode from the channel region. (TSMC-1003, ¶37; TSMC-1033, 71-76.) Applying voltage to the gate electrode controls the channel region to connect (ON state) or disconnect (OFF state) the

⁴ The terms “MISFET” and “MOSFET” (“Metal-**Oxide**-Semiconductor Field-Effect Transistor”) are interchangeable. (TSMC-1003, ¶36.)

source and drain. (TSMC-1003, ¶37; TSMC-1041, 8-9.) Generally, source/drain regions are **doped** with either a **p-type** or **n-type** impurity. (TSMC-1003, ¶38; TSMC-1033, 76-82.) MISFETs with n-type source/drain regions are called **NMOS**, and MISFETs with p-type source/drain regions are called **PMOS**. (TSMC-1003, ¶44; TSMC-1033, 13, Figure 1-11.)



TSMC-1033, Figure 1-11

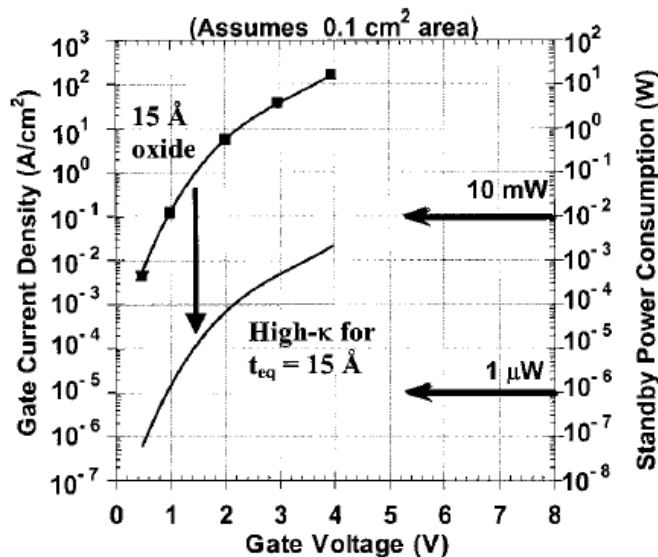
2. Gate Insulating Film

a. Materials

A common feature of a FET is the gate dielectric. (TSMC-1033, 288.) For decades prior to the '227 patent, silicon dioxide (SiO_2) was the primary material used for gate dielectrics in MOSFETs. (TSMC-1003, ¶46; TSMC-1033, 53 (“ SiO_2

is essentially a perfect insulator and provides the needed [electrical] isolation.”); TSMC-1032, 3-4.) However, as gate dielectric layers continued to shrink in thickness (e.g., below 1.5 nm), use of SiO₂ became untenable, because the amount of gate-to-channel tunneling leakage-current passing through the gate dielectric prevents the gate electrode from effectively controlling the ON and OFF states of the FET. (TSMC-1003, ¶46; TSMC-1034, 4-5.)

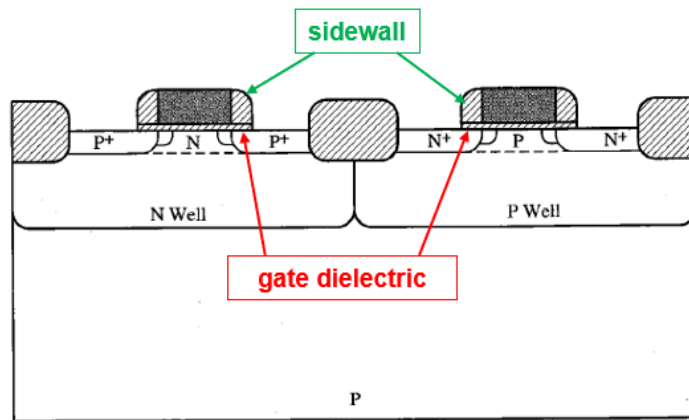
High-k dielectrics, like Hf-based oxides, Ta₂O₅, or ZrO₂, replaced SiO₂ to address these challenges. (TSMC-1003, ¶¶47-48; TSMC-1034, 146.) For example, it was known by 2005 that, as compared to SiO₂, high-k materials significantly reduce the amount of leakage current and, thus, improve energy efficiency. (TSMC-1003, ¶49; TSMC-1018, 5250, Figure 5 (below); TSMC-1034, 146-47.)



Wilk, Figure 5

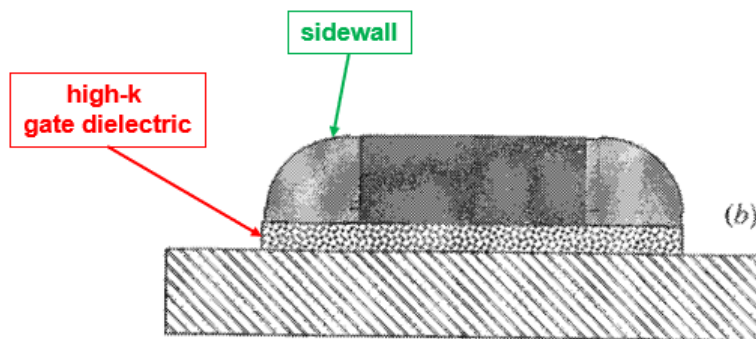
b. Extended Gate Insulating Films

Prior to 2005, it was common practice to extend the gate dielectric from under the gate electrode to under the gate sidewalls. For example, Plummer depicts a CMOS device having an extended gate dielectric in both the NMOS and PMOS transistors. (TSMC-1003, ¶50; TSMC-1033, 82-83.)



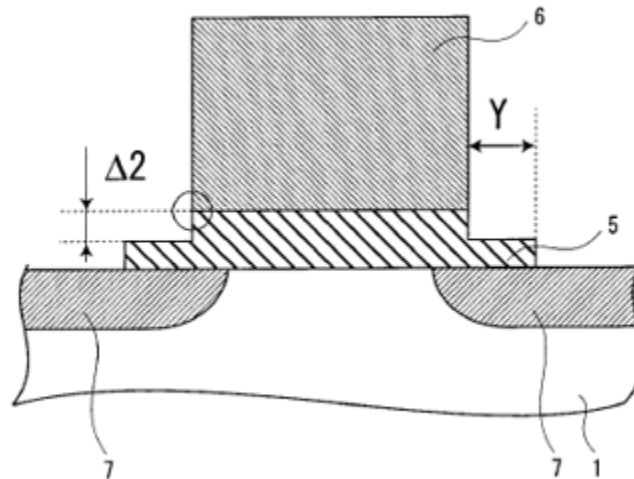
Plummer, Figure 2-34

Houssa discloses another example that uses a high-k material as the gate insulating film that extends from under the gate electrode to under the sidewalls. (TSMC-1032, 510.)



Houssa, Figure 5.1.9(b)

JP Publication 2005-064190 by Ono, et al. (“JP-Ono”⁵; TSMC-1040), filed two years before the earliest priority date of the ’227 patent, also describes extending the gate dielectric and varying its thickness. Specifically, JP-Ono adjusts both the reduction in thickness of the gate dielectric ($\Delta 2$) outside the gate electrode and the length of the gate dielectric from the outer edge of the gate electrode (Y) (i.e., how far the gate dielectric protrudes from under the gate electrode). (TSMC-1040, ¶35, Figure 3 (below); TSMC-1003, ¶¶53-54.)



JP-Ono, Figure 3

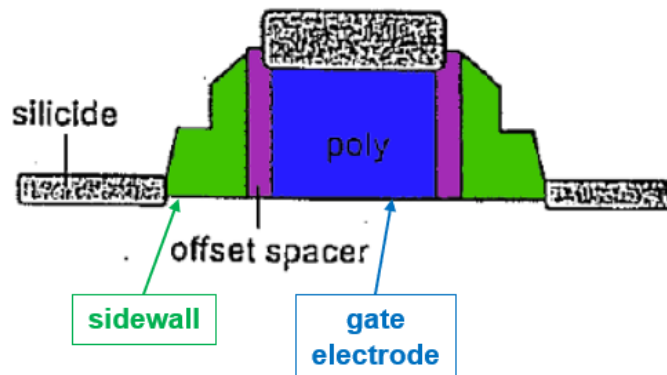
3. Sidewalls

Another common feature of a semiconductor device are sidewalls, vertical insulating structures formed on or proximate to the side surfaces of a gate

⁵ A certified translation of JP-Ono is included with TSMC-1040.

electrode. Sometimes, the terms “sidewall,” “spacer,” and “sidewall spacer” are used interchangeably. (TSMC-1003, ¶58.) Sidewalls serve a variety of purposes and functions in a semiconductor device such as defining the source/drain region, providing isolation, protecting the gate during subsequent fabrication, and controlling the width of the gate in the gate length direction. (*Id.*)

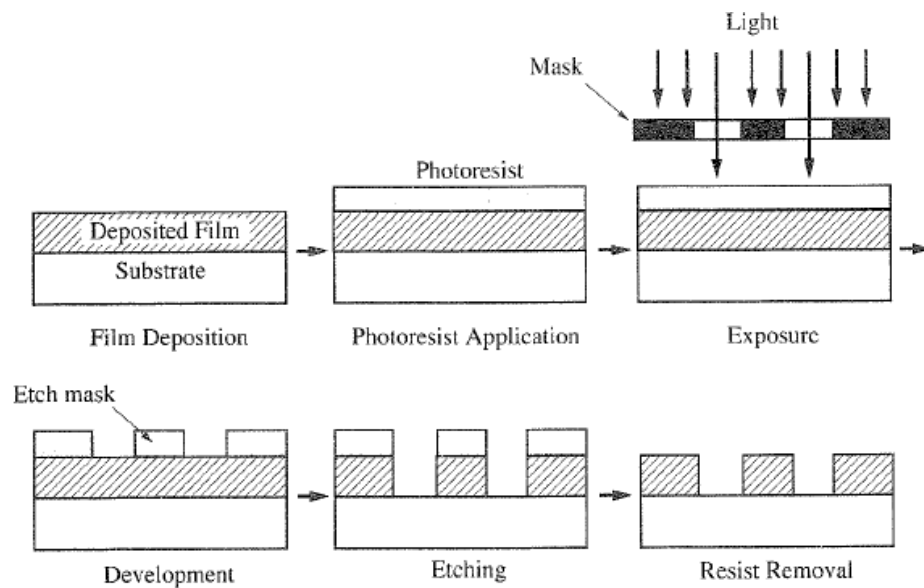
As a non-limiting example, spacers may be used for “[c]ontrolling the position of the edge of the SDE [source/drain extension] region with respect to the gate edge” so as to achieve the optimal amount of overlap between the SDE and the gate edge. (TSMC-1034, 217.) As shown in Wolf’s Figure 5-25 below, “an offset-spacer is fabricated on the side of the gate after the gate-poly is etched (but before the SDE implant step is carried out ...),” with offset-spacer width “varied from zero (no-spacer) to some upper-bound (e.g., 50-nm)” to achieve optimum device characteristics. (TSMC-1034, 217; TSMC-1003, ¶59.)



Wolf, Figure 5-25

4. Etching Properties

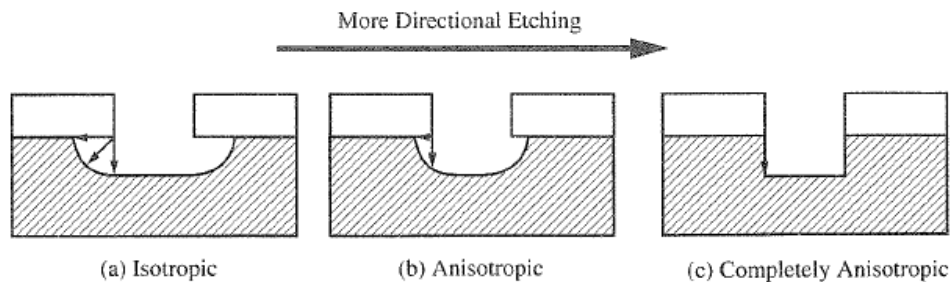
In semiconductor devices, thin films are often first deposited on the wafer surface and then selectively removed by etching to leave the desired pattern of the film. (TSMC-1003, ¶60; TSMC-1033, 609-11.) The desired pattern is often defined by placing a mask on the surface before etching; the mask is removed after etching. (TSMC-1003, ¶60; TSMC-1033, 609-10, Figure 10-1 (below).)



Plummer, Figure 10-1

Etching is performed in a “wet” or “dry” environment. (TSMC-1003, ¶61; TSMC-1033, 609, 612-37.) Wet etching involves the use of liquid etchants (e.g., hydrofluoric acid), whereas dry etching involves the use of gas-phase etchants in a plasma. (TSMC-1003, ¶61; TSMC-1033, 609.) Etching processes are also described based on the relative etch rates in different directions. (TSMC-1003, ¶62; TSMC-1033, 610-11.) Isotropic etching occurs when the etch rate is the same in all

directions, resulting in a semicircular etch profile as shown in Figure 10-3(a) below. Most wet chemical etchants etch isotropically. (TSMC-1033, 610-13.) Anisotropic etching occurs where there is little or no etching in the lateral direction. (TSMC-1033, 611, Figure 10-3(b), (c) (below).) For anisotropic etching, the amount of lateral etching may vary, such that the etched surface may be curved or sloped (TSMC-1033, Figure 10-3(b)) to completely vertical (TSMC-1033, Figure 10-3(c)). (TSMC-1003, ¶63.)



Plummer, Figure 10-3

C. '227 Patent Overview

The four semiconductor device embodiments presented in the '227 patent can be separated into two groups—single sidewall devices (first/fourth embodiments) and double sidewall devices (second/third embodiments). The '227 patent's claims are directed to double sidewall devices and cover different alternatives for varying the thickness of the high-k gate insulating film.

In the second embodiment (Figure 2; top), the high-k gate insulating film (shaded red) extends only under inner sidewall 6 (shaded purple) and has a smaller

thickness under inner sidewall 6 than under gate electrode 5 (shaded blue), corresponding, e.g., to claims 1 and 2. (TSMC-1001, 7:44-55.) In a modification (Figure 3; bottom-left), the thickness of the high-k gate insulating film is the same under both inner sidewall 6 and outer sidewall 7 and is thinner under both sidewalls than under gate electrode 5, corresponding to claims 1 and 3. (TSMC-1001, 8:58-63.) In another modification (Figure 4; bottom-right), the thickness of the high-k gate insulating film is the same under gate electrode 5 and inner sidewall 6 but is thinner under outer sidewall 7, corresponding to claim 5.⁶ (TSMC-1001, 9:40-51.)

⁶ Claim 5 is not challenged in this IPR.

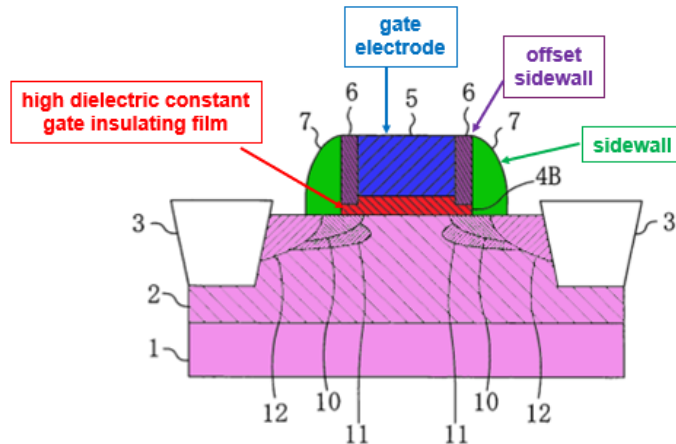


Figure 2

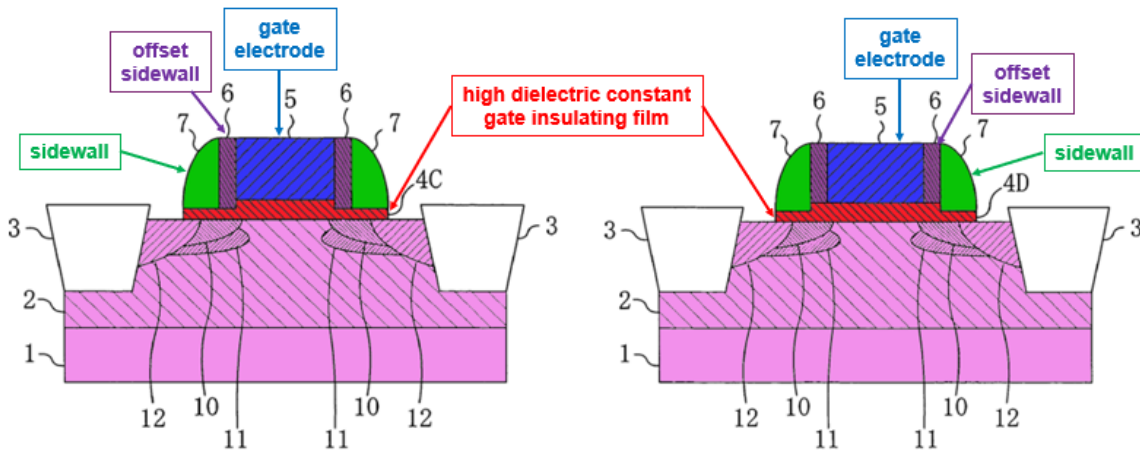


Figure 3

Figure 4

In the third embodiment device (Figure 5 below), the high-k gate insulating film has declining thicknesses under gate electrode 5, under offset sidewall 6, and under sidewall 7 and corresponds to claims 1 and 4.⁷ (TSMC-1001, 10:49-58.)

⁷ Claim 4 is not challenged in this IPR.

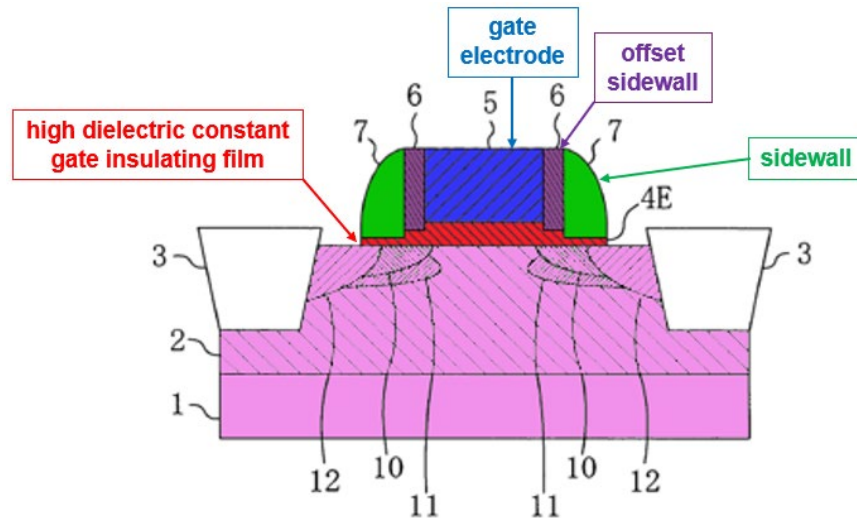


Figure 5

D. Prosecution History

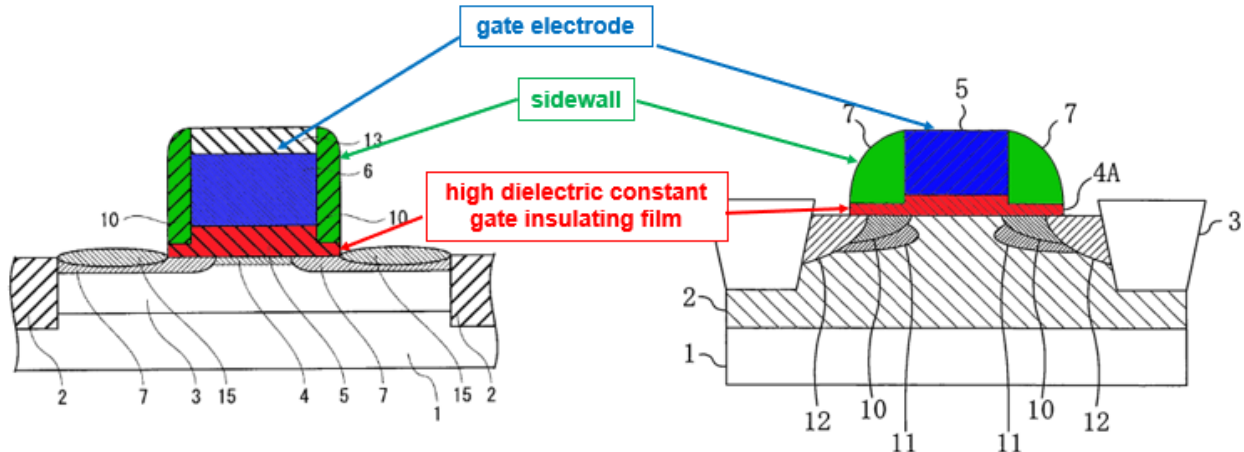
1. '227 Patent

The corresponding U.S. application was filed with one independent device claim reciting a high-k gate insulating film with a smaller thickness under the sidewall than under the gate electrode. (TSMC-1002, 7-8.) The Examiner rejected this claim as anticipated by U.S. Patent 6,992,358 to Hieda. (TSMC-1002, 122-23.) In response, Applicant narrowed the claim to recite (1) the sidewall has a “first insulating sidewall” and a “second insulating sidewall”, thus, narrowing the claims to only the double sidewall embodiments, and (2) part of the high-k gate insulating film “under the first insulating sidewall has a smaller thickness than a thickness of part of the” high-k gate film under the gate electrode. (TSMC-1002, 147-48.) Applicant also rewrote pending dependent claim 6 (issued claim 5) into

independent form. (TSMC-1002, 149.) The Examiner allowed the amended claims.
(TSMC-1002, 164.)

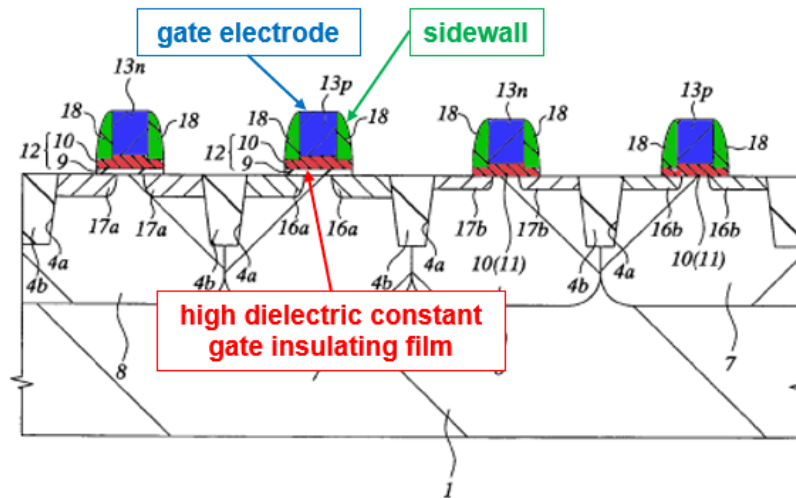
2. JP Application

The JP priority application was filed with the same device claim originally filed with the U.S. application. (TSMC-1005, 1.) On September 16, 2011, the JP-Examiner found this claim scope unpatentable, citing JP-Ono discussed above (Figure 23, top-left) and WO2004/017418 to Sakai, et al. (“Sakai”; Figure 25, below-bottom) which both teach a high-k gate insulating film with a smaller thickness under the sidewall than under the gate electrode, like e.g., the ’227 patent’s single sidewall embodiments. (TSMC-1005, 4-6; *see* TSMC-1001, Figure 1 (top-right).)



JP-Ono, Figure 23

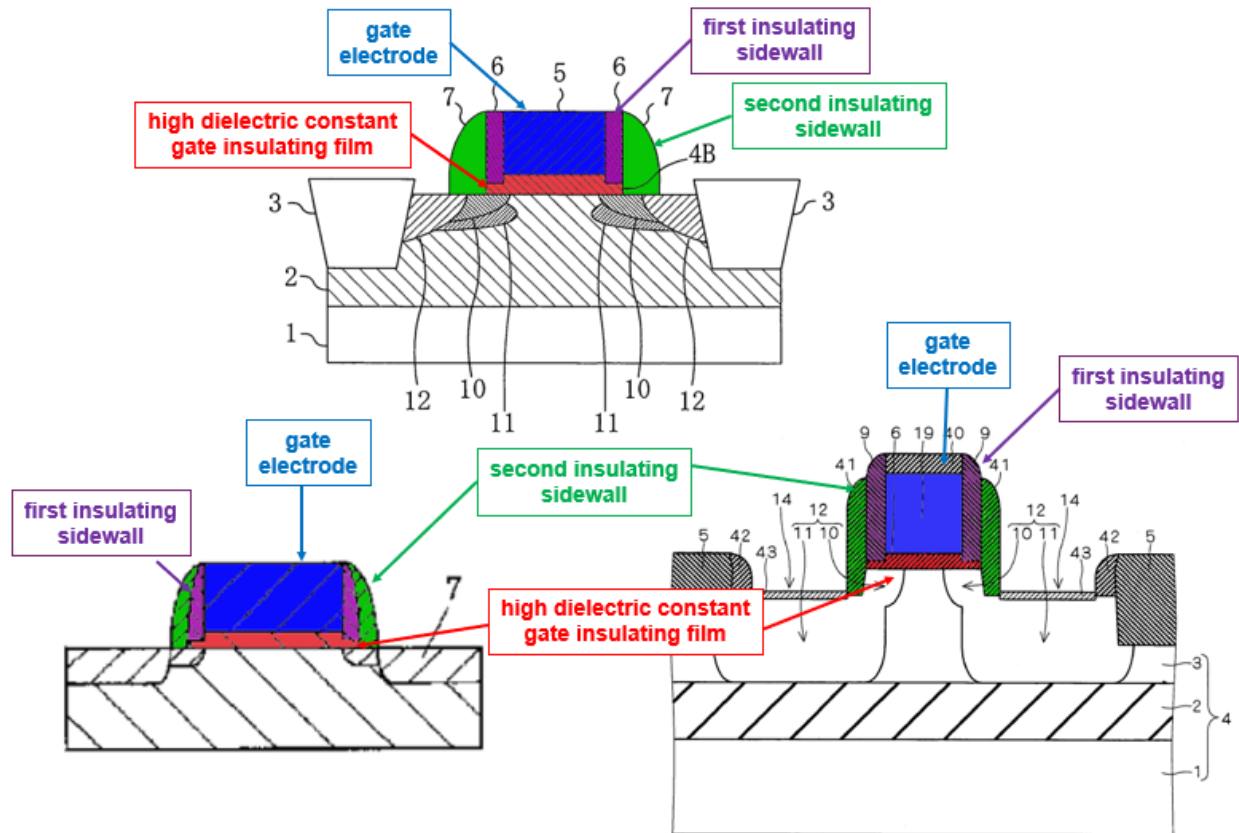
'227 Patent, Figure 1



Sakai, Figure 25

In response, Applicant narrowed the Japanese claim to recite (1) a double sidewall structure with a high-k film having a smaller thickness under a first sidewall than under the gate electrode and (2) extension and source/drain regions. (TSMC-1005, 8.) The JP-Examiner rejected the amended claim based on both JP 2003-258241 to Kajiyama (JP-Kajiyama (TSMC-1010); bottom-left) and JP 2004-

241755 to Matsumoto (“JP-Matsumoto”; bottom-right) which each teaches the same basic structure as the ’227 patent’s Figure 2. (TSMC-1005, 14-16; *compare* TSMC-1001, Figure 2 (top).)



’227 Patent, Figure 2 (top); JP-Kajiyama, Figure 1(D) (bottom-left); JP-Matsumoto, Figure 33 (bottom-right)

In response, Applicant further narrowed the claim to recite the thickness of the high-k gate insulating film under the second sidewall is smaller than the thickness under the first sidewall which is smaller than the thickness under the gate electrode. (TSMC-1005, 18.) The JP-Examiner allowed the claim based on this amendment. (TSMC-1005, 20.)

In short, to secure allowance over the prior art, PO acquiesced during JP prosecution that the scope of at least issued claim 1 of the '227 patent was known in the art.

E. Claim Construction

Petitioner does not believe any claims require construction to resolve the patentability disputes in this proceeding. *See Vivid Techs., Inc. v. Am. Sci. & Eng'g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999).

F. Level of Ordinary Skill in the Art

A POSITA would have had at least a Master's degree in electrical engineering, physics, chemistry, materials science, or related fields, and three years of work experience in semiconductor manufacturing. (TSMC-1003, ¶31.) Additional graduate education could substitute for work experience, and additional work experience/training could substitute for formal education. (*Id.*)

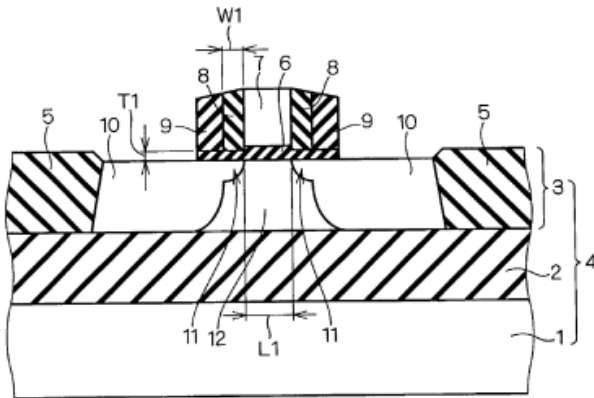
V. GROUND 1: Matsumoto Renders Claims 1-3⁸ Obvious.

A. Overview

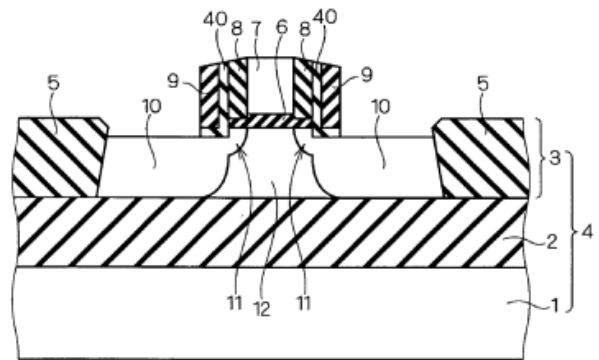
Matsumoto relates “to a semiconductor device” and more specifically to a MOSFET. (Matsumoto, ¶2; TSMC-1003, ¶86.) Matsumoto presents seven embodiments of its semiconductor device. This Petition focuses on Matsumoto's

⁸ A listing of challenged claims is provided in the Appendix.

first and fourth embodiment MOSFETs, which each includes a multilayer sidewall structure and a gate insulating film 6 extending from under a gate electrode. In the first embodiment, gate insulating film 6 extends under both films 8 and 9 of the sidewall structure formed on the gate electrode's side surfaces. (See TSMC-1009, ¶¶102-121, Figure 1 (below-left).) In the fourth embodiment, gate insulating film 6 extends under only film 8 of the sidewall. (See TSMC-1009, ¶¶137-140, Figure 22 (below-right).)



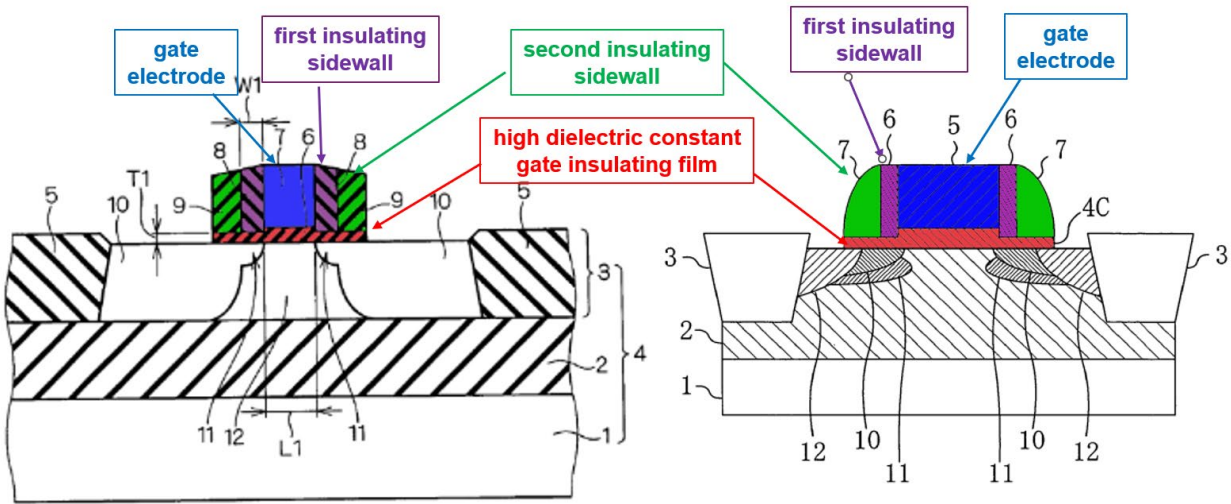
Matsumoto, Figure 1



Matsumoto, Figure 22

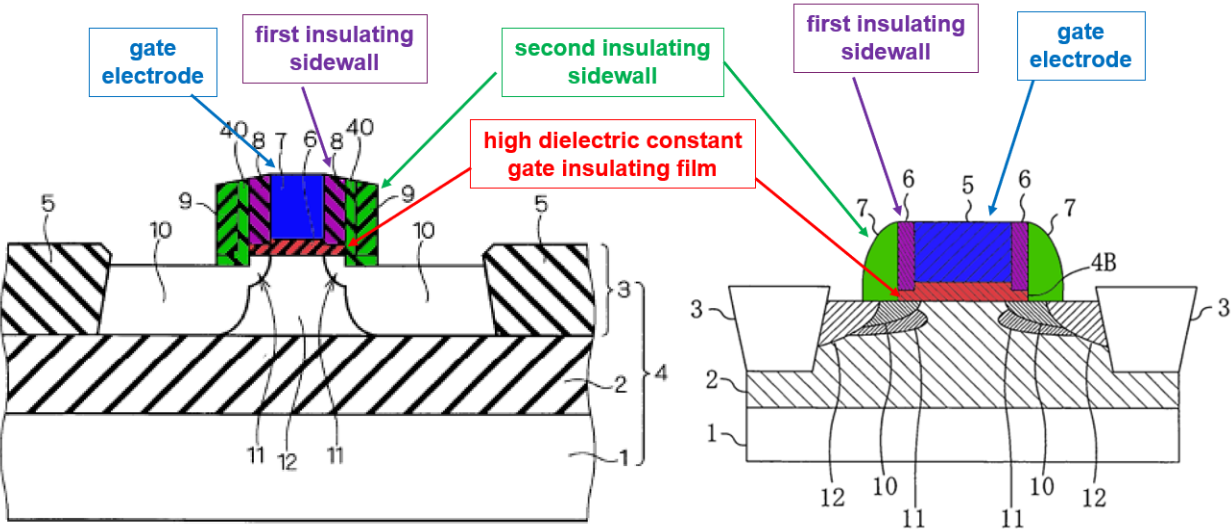
B. Independent Claim 1

Matsumoto's first and fourth embodiment devices each renders claim 1 obvious, as illustrated by the side-by-side figures below. (TSMC-1003, ¶89.)



**Matsumoto, Figure 1
First Embodiment**

'227 Patent, Figure 3



**Matsumoto, Figure 22
Fourth Embodiment**

'227 Patent, Figure 2

1. Preamble [1P]

Matsumoto's first embodiment (Figure 1) and fourth embodiment (Figure 22) each discloses a "*semiconductor device*"⁹: "The present invention relates to a **semiconductor device**."¹⁰ (TSMC-1009, ¶¶2, 102, 137; TSMC-1003, ¶91.)

2. Limitation [1A]

Matsumoto's first and fourth embodiments each teaches "*a high dielectric constant gate insulating film formed on an active region in a substrate*" [1A]. (TSMC-1003, ¶¶92-99.)

Both embodiments include "*a substrate*." (TSMC-1003, ¶93.) Each device has a multi-layer SOI **substrate** 4 (shaded pink) with silicon substrate 1, BOX layer 2 and single-crystalline silicon layer 3 "stacked in the order named." (TSMC-1009, ¶102, ¶¶137, 140 (relating fourth embodiment to first embodiment));¹¹ *Google LLC v. Jenam Tech, LLC*, IPR2021-00630, 2022 WL 4287797, *9 n.9

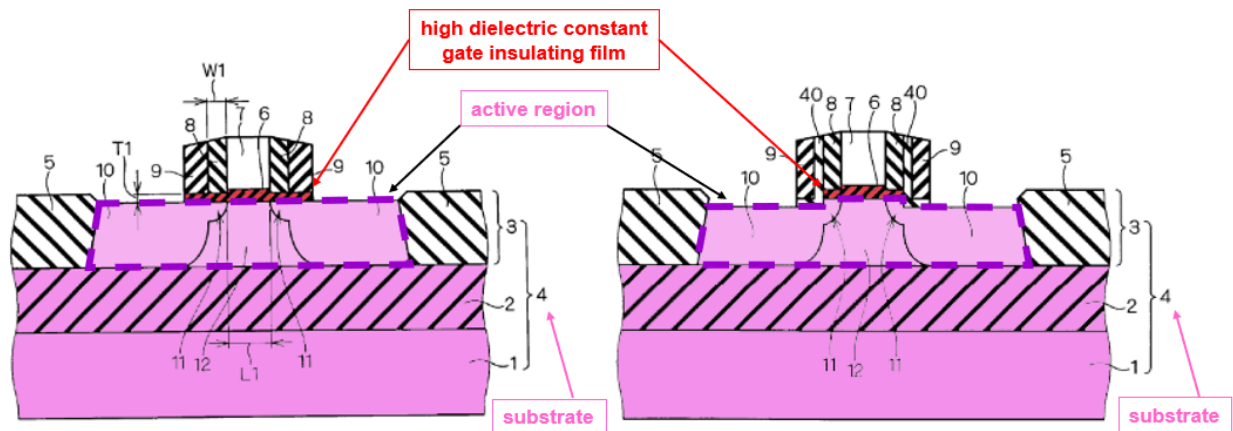
⁹ Claim language is indicated by italics throughout.

¹⁰ Unless otherwise noted, all emphasis added.

¹¹ Although Matsumoto discloses several embodiments, many of the fabrication steps are discussed in relation to the first embodiment. (TSMC-1003, ¶86 n.5; TSMC-1009, ¶137.) Thus, Petitioner at times also relies on disclosures from Matsumoto's first embodiment when discussing the fourth embodiment.

(P.T.A.B. Sept. 16, 2022) (applying same disclosure where “figures refer to corresponding features using the same reference numbers”).)

Isolating insulation film structures 5 “extend[ing] from the upper surface of silicon layer 3 to the upper surface of BOX layer 2” define a “**device region.**” (TSMC-1009, ¶¶102-03, Figure 1 (below-left), ¶¶137, 140, Figure 22 (below-right).) The device region, identified by isolation regions, is an “*active region in a substrate*” and includes source/drain regions 10. (TSMC-1009, ¶¶105, 139; TSMC-1003, ¶94; *see* TSMC-1001, 1:34-35 (“region of the well 102 surrounded by the STI serves as an active region of a substrate 101”), 7:26-43 (active region includes source/drain regions surrounded by STI structures).)



Matsumoto, Figure 1

Matsumoto, Figure, 22

In both embodiments, film 6 (shaded red) “is formed partially on the upper surface of the silicon layer 3” in the device region with gate electrode 7 “formed partially” thereon. (TSMC-1009, ¶103, ¶137 (fourth embodiment’s gate electrode

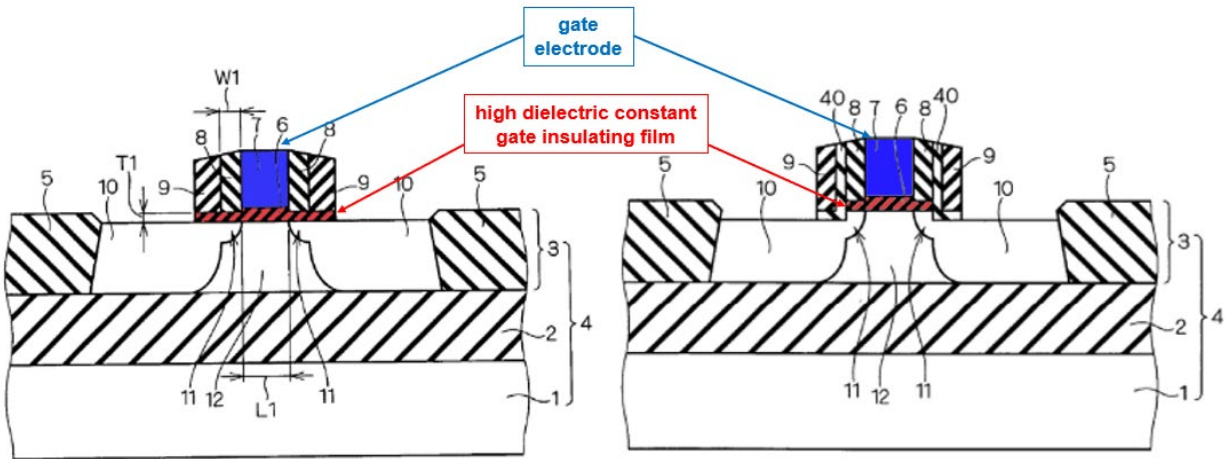
“formed by the process described in the first preferred embodiment”), Figure 22 (elements 6, 7).) “A silicon oxynitride film, a metal oxide film such as Al_2O_3 or a ferroelectric film such as Ta_2O_5 and BST may be formed in place of the silicon oxide film 13” which is etched during fabrication to form film 6. (TSMC-1009, ¶¶107, 114, Figures 1, 9-10, ¶138, Figures 18-19, 22.) Al_2O_3 , Ta_2O_5 , and BST are high-k dielectrics. (TSMC-1003, ¶97; *see* TSMC-1001, 1:21-25 (“a **high dielectric constant film** formed of a Hf based oxide, Al based oxide or the like, which has a relative dielectric constant of 10 or more”); TSMC-1018, Table I (identifying Al_2O_3 , Ta_2O_5 as high-k dielectrics).) A POSITA would have been motivated to use a high-k dielectric in Matsumoto’s device to address the well-documented issues with scaling SiO_2 to thicknesses needed for large scale device integration. (*See* TSMC-1032, 3-12; TSMC-1034, 4-5, 146-47; TSMC-1003, ¶98.)

Film 6, present in both the first and fourth embodiments, is therefore “*a high dielectric constant gate insulating film formed on an active region in a substrate*” [1A]. (TSMC-1003, ¶99; *see, e.g.*, TSMC-1009, ¶103 (portion of film 6 “which lies under the gate electrode 7 functions as a gate insulation film”).)

3. Limitation [1B]

Matsumoto’s first and fourth embodiments each teaches “*a gate electrode formed on the high dielectric constant gate insulating film*” [1B]. (TSMC-1003, ¶¶100-01.)

In both embodiments (illustrated below), “**gate electrode 7** [shaded blue] made of polysilicon **is formed partially**” on high-k insulating film 6. (TSMC-1009, ¶103, ¶107 (describing formation of high-k insulating film and gate electrode), Figure 1 (left), ¶¶137-138, Figure 22 (right).)



Matsumoto, Figure 1

Matsumoto, Figure 22

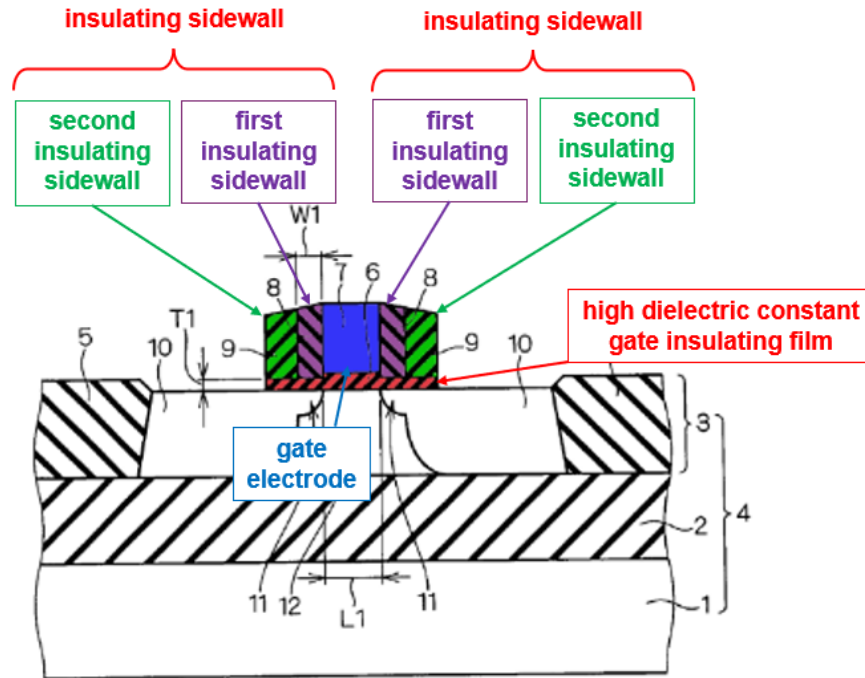
4. Limitations [1C]/[1F]

Limitation [1C] recites “*an insulating sidewall formed on each side surface of the gate electrode.*” Limitation [1F] narrows this limitation, reflecting the claimed insulating sidewall includes two sidewalls: “*the insulating sidewall includes a first insulating sidewall formed on a side surface of the gate electrode and a second insulating sidewall formed on the side surface of the gate electrode with the first insulating sidewall interposed therebetween.*” Matsumoto’s first and fourth embodiments teach these limitations. (TSMC-1003, ¶¶102-07.)

In Matsumoto's first embodiment, "silicon nitride film 9 is formed on each side surface of the gate electrode 7, with a silicon oxide film 8 therebetween." (TSMC-1009, ¶103, Figure 1 (below).) Matsumoto refers to film 9 as a "sidewall insulation film" but does not refer to film 8 as a "sidewall." (See TSMC-1009, ¶114 (describing nitride films 9a/9b "serving as **sidewall** insulation films").) A POSITA would have understood film 8 also to be a sidewall. (TSMC-1009, ¶¶104, 110, 40 ("the semiconductor device further includes a second sidewall formed on the side surface of the gate electrode, with the first sidewall therebetween"); TSMC-1003, ¶104.) Because silicon oxide and silicon nitride are both insulators, silicon oxide film 8 and silicon nitride film 9, as illustrated below, are collectively "*an insulating sidewall formed on each side surface of the gate electrode*" [1C] with film 8 (shaded purple) being "*a first insulating sidewall formed on¹² a side surface of the gate electrode*" and film 9 (shaded green) being the "*second insulating sidewall formed on the side surface of the gate electrode with the first insulating sidewall interposed therebetween*" [1F]. (See TSMC-1009, ¶¶110

¹² The '227 patent uses the term "*formed on*" generally to refer to location and does not require contact. (See, e.g., TSMC-1001, 1:31-33, 7:28-32; TSMC-1003, ¶107 n.5.)

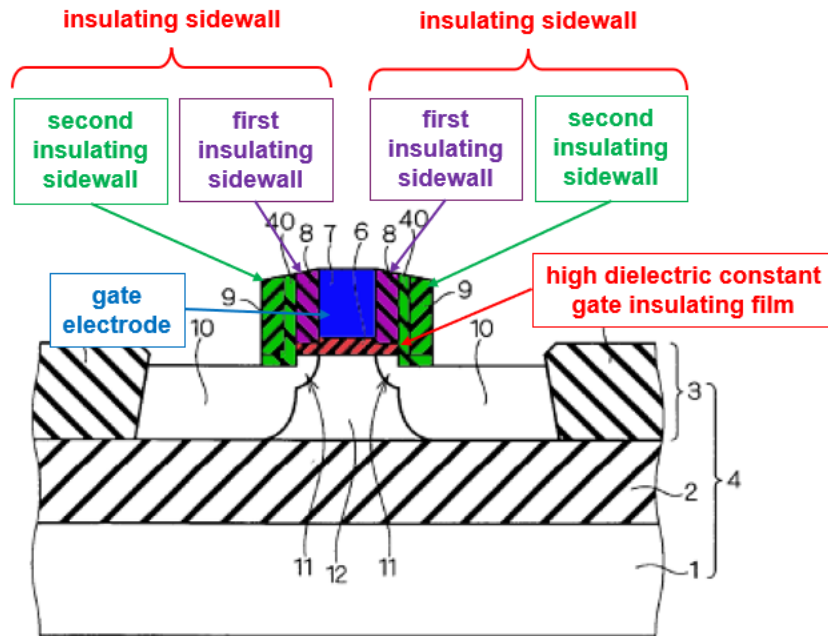
(describing the formation of silicon oxide films 8a/8b on the side surfaces of the gate electrodes), 114; *see also* TSMC-1009, claim 1 (referring to “**insulation films**” formed on side surfaces on gate electrode); TSMC-1001, 3:17-22 (referring to two components collectively as an insulating sidewall); TSMC-1003, ¶104-05.)



Matsumoto, Figure 1

In the fourth embodiment, silicon oxide film 40 and silicon nitride film 9 are formed “on the outer side surfaces of” film 8, as illustrated in Figure 22. (*See* TSMC-1009, ¶139, Figure 22 (below); *see also* TSMC-1009, ¶110.) Silicon oxide film 8, silicon oxide film 40, and silicon nitride film 9 are collectively “an *insulating sidewall*” [1C] with film 8 (shaded purple) being “a *first insulating sidewall*” and film 9 (shaded green) alone, film 40 (shaded green) alone, or their

combination being “a second insulating sidewall formed on the side surface of the gate electrode with the first insulating sidewall interposed therebetween” [1F], consistent with the disclosures of the ’227 patent.¹³ (TSMC-1001, 3:17-22, 21:5-15; TSMC-1003, ¶¶106-07.)



Matsumoto, Figure 22

¹³ The ’227 patent uses the term “insulating sidewall” to refer to a single component (TSMC-1001, 5:66-67), a collective structure of two components (TSMC-1001, 3:17-22), and a component having multiple layers (TSMC-1001, 21:5-15).

5. Limitations [1D]-[1E]/[1G]-[1H]

Limitation [1D] recites “*the high dielectric constant gate insulating film is continuously formed so as to extend from under the gate electrode **to under the insulating sidewall***” and limitation [1E] recites “*at least part of the high dielectric constant gate insulating film located **under the insulating sidewall** has a smaller thickness than a thickness of part of the high dielectric constant gate insulating film located under the gate electrode.*”

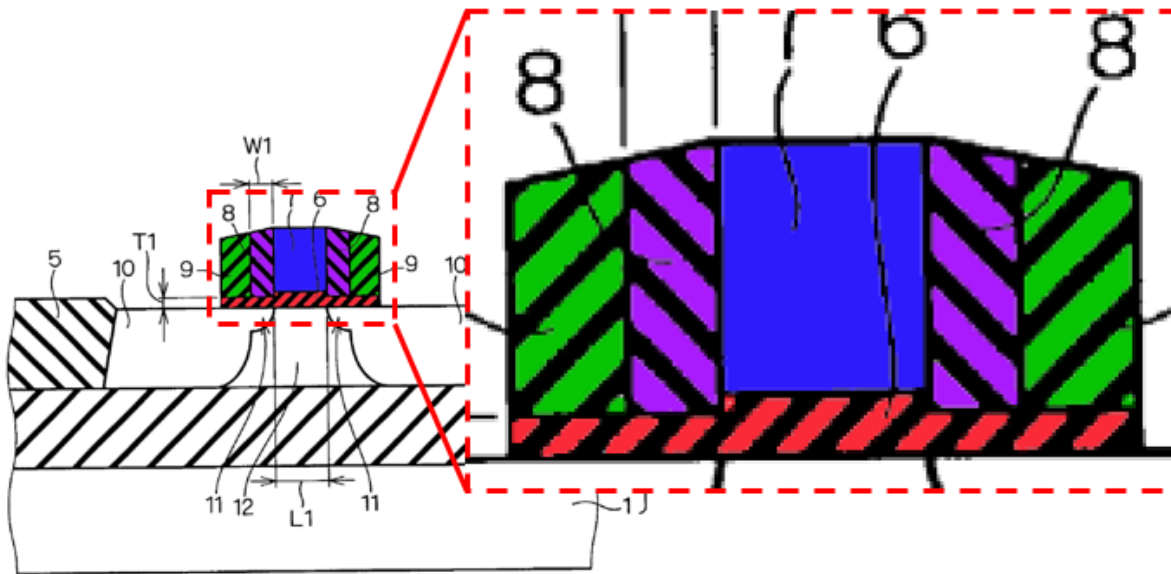
Limitations [1G]-[1H] narrow and largely repeat [1D]-[1E], reflecting the claimed insulating sidewall includes two sidewalls: “*the high dielectric constant gate insulating film is continuously formed so as to extend from under the gate electrode **to under the first insulating sidewall***” [1G] and “*part of the high dielectric constant gate insulating film located **under the first insulating sidewall** has a smaller thickness than a thickness of part of the high dielectric constant gate insulating film located under the gate electrode*” [1H].

Matsumoto’s first and fourth embodiments teach these limitations. (TSMC-1003, ¶¶108-20.)

a. First Embodiment

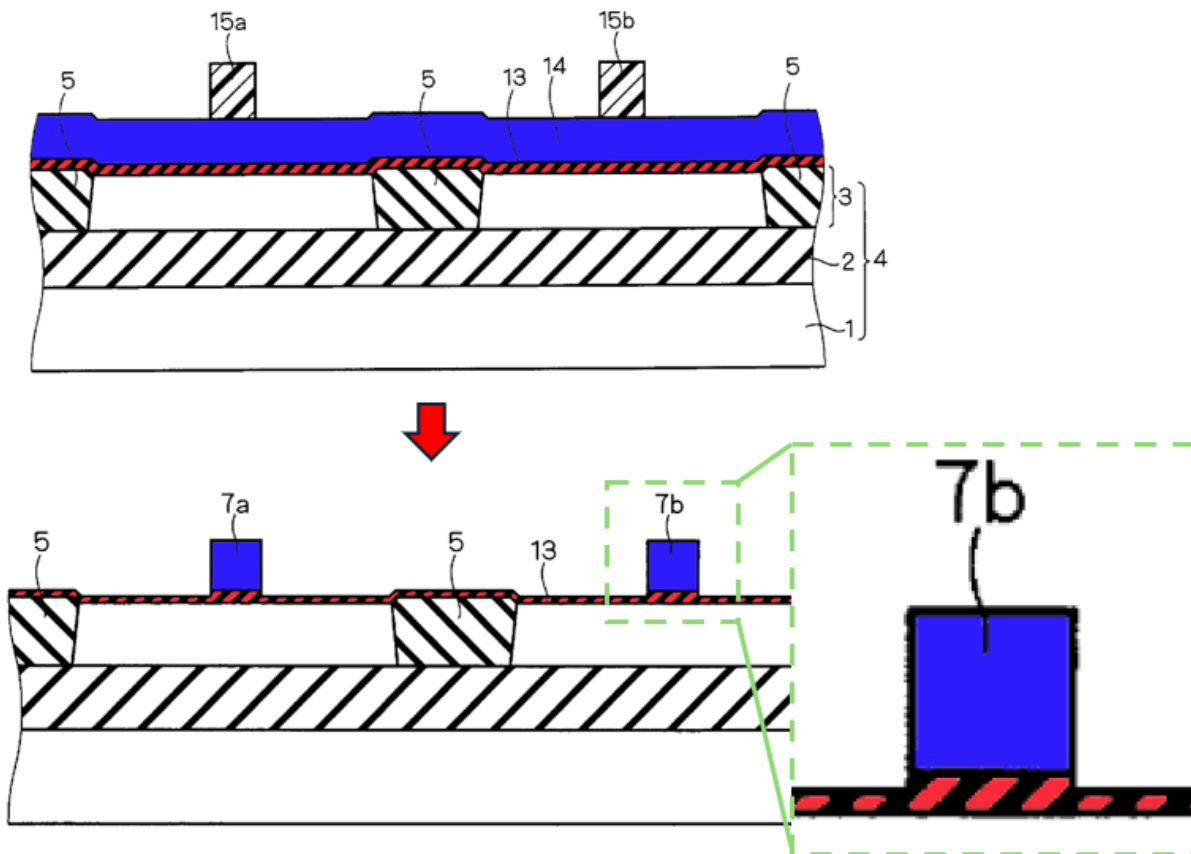
As shown in the enlargement of Matsumoto’s Figure 1 and confirmed by Matsumoto’s fabrication process, high-k gate insulating film 6 (shaded red) is an uninterrupted layer (as evidenced by the absence of gaps) that extends from under

the gate electrode 7 to under film 8 (“*first insulating sidewall*”; shaded purple) which is part of the collective “*insulating sidewall*” (films 8 and 9). The high-k film 6 is thinner under film 8 (“*first insulating sidewall*”) than it is under the gate electrode 7 (shaded blue). Matsumoto’s first embodiment device therefore discloses limitations [1D]-[1E]/[1G]-[1H]. *Unified Pats., LLC v. Oceana Innovations LLC*, IPR2020-01463, 2022 WL 500391, *17 (P.T.A.B. Feb. 14, 2022) (“[A] patent drawing may serve as prior art ‘without referring to the surrounding description’ if ‘the prior art features are clearly disclosed by the drawing.’”) (citations omitted); TSMC-1003, ¶¶111-12.



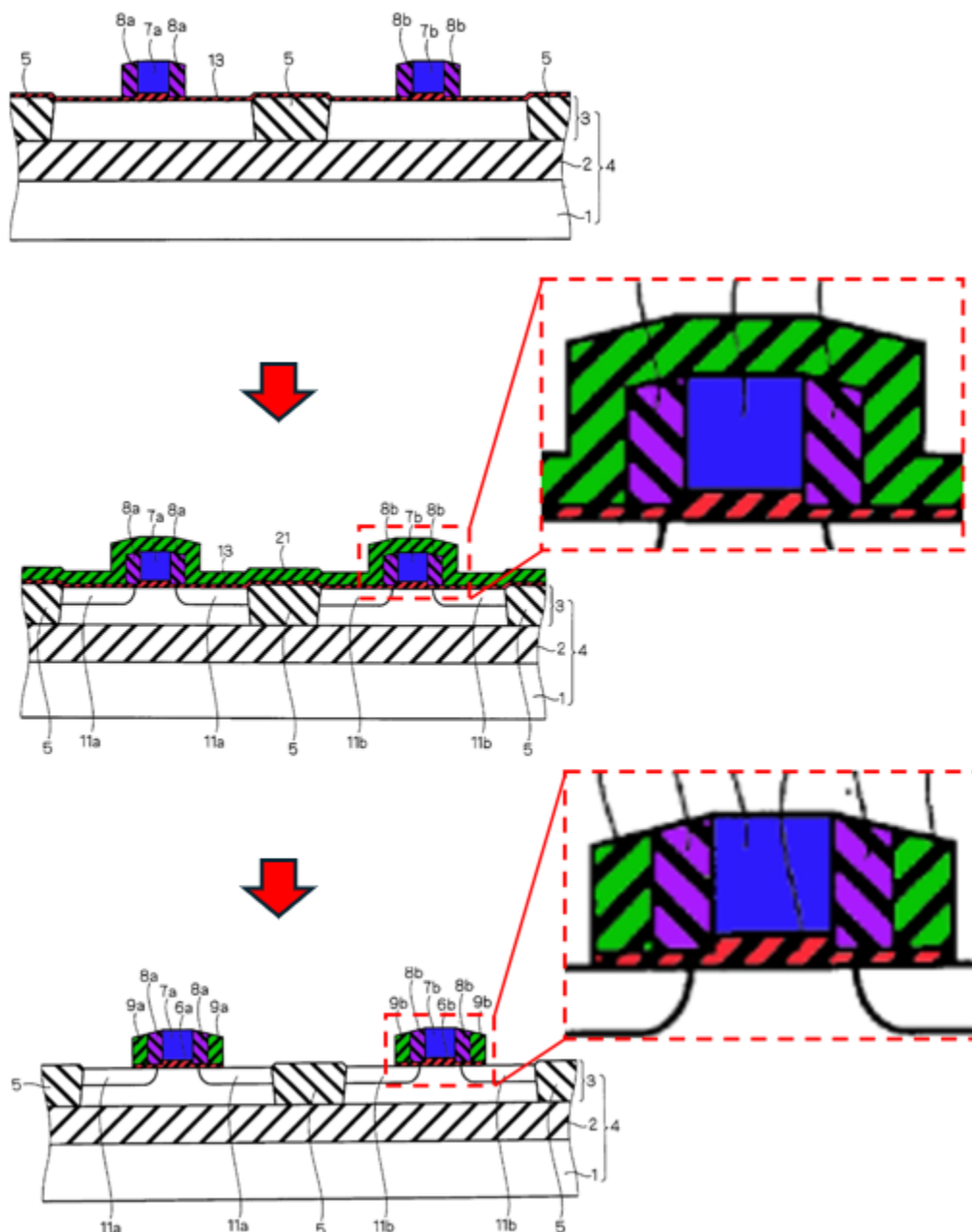
Matsumoto, Figure 1 with enlargement

The fabrication of the first embodiment device confirms the Figure 1 device structure. During fabrication, high-k dielectric film 13 (shaded red) is formed on the substrate and polysilicon film 14 (shaded blue) is formed on high-k dielectric film 13. (See TSMC-1009, ¶107, Figure 3 (top).) The etching process used to form the gate electrode “slightly etches the upper surface of” film 13, resulting in a high-k dielectric film with a larger thickness under the gate electrode than in the areas not under the gate electrode. (TSMC-1009, ¶108, Figure 4 (bottom); TSMC-1003, ¶113.)



Matsumoto, Figures 3 (top) and 4 (bottom) with enlargement

After formation of sidewalls 8a/8b (“*first insulating sidewall*”; shaded purple), silicon nitride film 21 is “formed on the entire top surface” of the intermediate structure. (TSMC-1009, ¶¶109-10, 114, Figure 6 (below-top), Figure 9 (below-middle).) Film 21 and film 13 are etched “until the upper surface of the silicon layer 3 is exposed”, forming sidewalls 9a/9b (“*second insulating sidewall*”; shaded green). (TSMC-1009, ¶114, Figure 10 (below-bottom).) After this etching, the high-k dielectric film (shaded red) remains under the gate electrode and first and second sidewalls. (TSMC-1003, ¶¶114-15.)

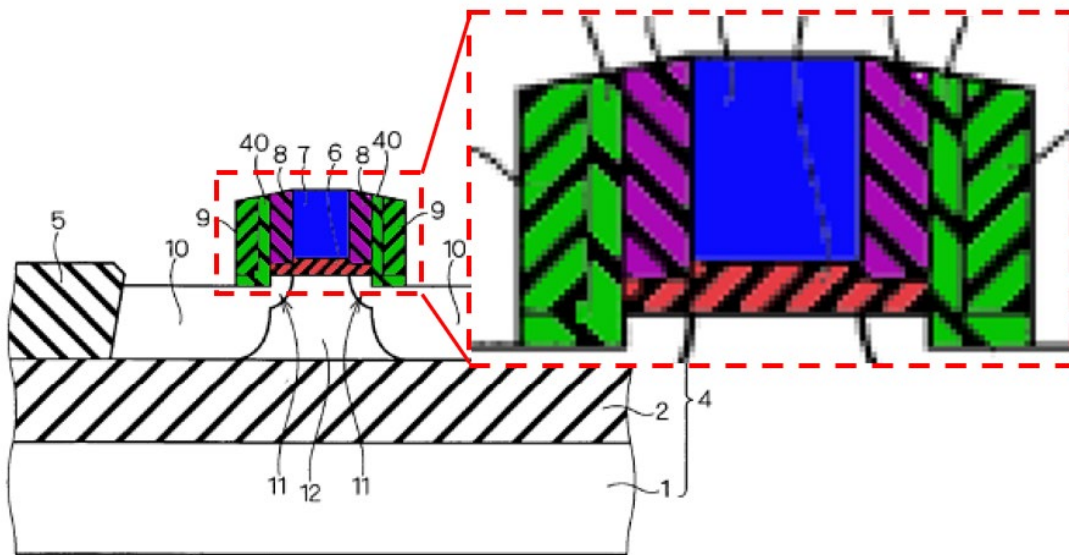


Matsumoto, Figures 6 (top), 9 (middle), 10 (bottom) with enlargement

b. Fourth Embodiment

As shown in the enlargement of Matsumoto's Figure 22 and confirmed by Matsumoto's fabrication process, high-k gate insulating film 6 (shaded red) is an

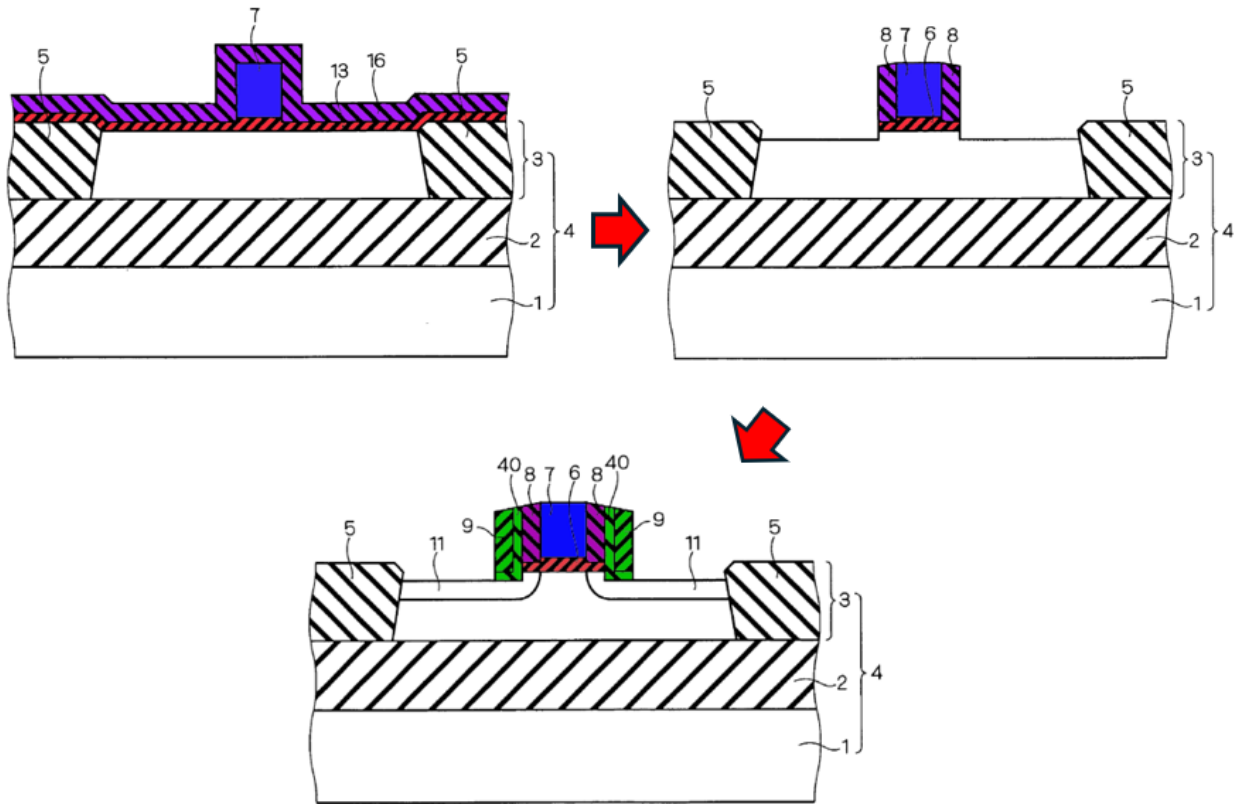
uninterrupted layer (as evidenced by the absence of gaps) that extends from under the gate electrode to under only film 8 (“*first insulating sidewall*”) which is part of the collective “*insulating sidewall*” (films 8, 9, and 40). The high-k film 6 is thinner under the film 8 (“*first insulating sidewall*”; shaded purple) than it is under the gate electrode 7 (shaded blue). Matsumoto’s fourth embodiment device therefore discloses limitations [1D]-[1E]/[1G]-[1H]. *See Unified*, 2022 WL 500391, at *17; TSMC-1003, ¶¶116-17.



Matsumoto, Figure 22 with enlargement

The fabrication process of the fourth embodiment device confirms the Figure 22 device structure. During fabrication, “gate electrode 7 is formed by the process described” in the first embodiment, resulting in high-k dielectric film 13 having a larger thickness under the gate electrode (Figure 18 (top-left)). (*See* TSMC-1009, ¶¶137, 107-08; TSMC-1003, ¶118.) The etching process that forms

sidewall 8 (“*the first insulating sidewall*”; shaded purple) “overetch[es] the upper surface of the silicon layer 3” and as a result, the high-k dielectric film (shaded red) remains only under the gate electrode and sidewall 8. (TSMC-1009, ¶138, Figure 19 (top-right); TSMC-1003, ¶119.) Film 40 and film 9 (alone or in combination the “*second insulating sidewall*” (shaded green)) are then formed on the outer side surfaces of film 8 and on the substrate surface. (TSMC-1009, ¶139; TSMC-1003, ¶119.)

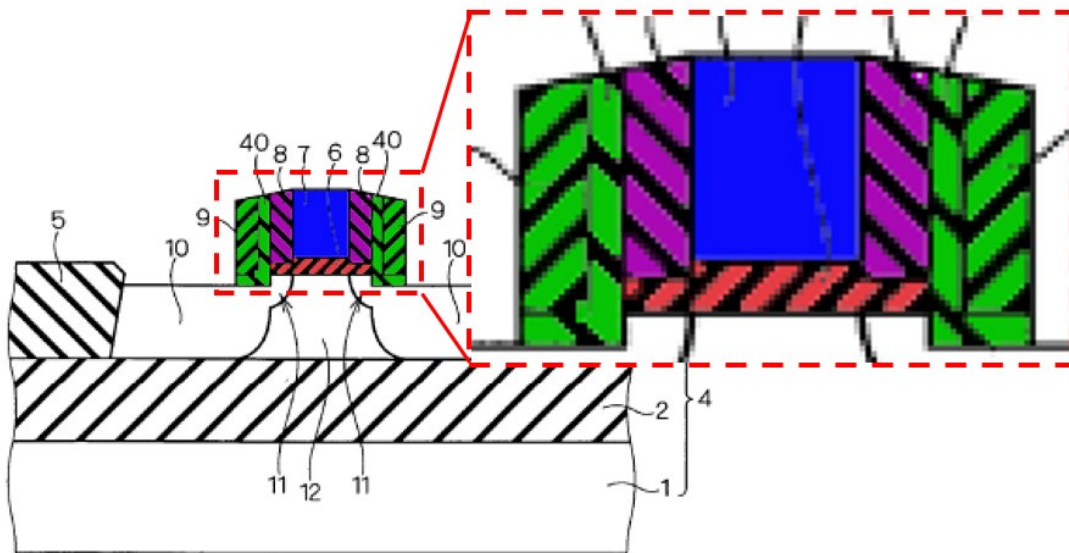


Matsumoto, Figures 18 (top-left), 19 (top-right), 21 (bottom)

C. Claim 2

Matsumoto's fourth embodiment teaches "*the high dielectric constant gate insulating film is formed so as not to be located under the second insulating sidewall*" [2]. (TSMC-1003, ¶¶121-24.)

As shown in the enlargement of Matsumoto's Figure 22 below and discussed in §V.B.5.b, high-k gate insulating film 6 (shaded red) extends only under film 8 ("first insulating sidewall") and is not located under films 40 and 9 (alone or collectively the "second insulating sidewall"). See *Unified*, 2022 WL 500391, at *17. The fabrication process of the fourth embodiment, discussed in §V.B.5.b, confirms the Figure 22 device structure. (See TSMC-1009, ¶¶138-39, TSMC-1003, ¶¶118-19.)

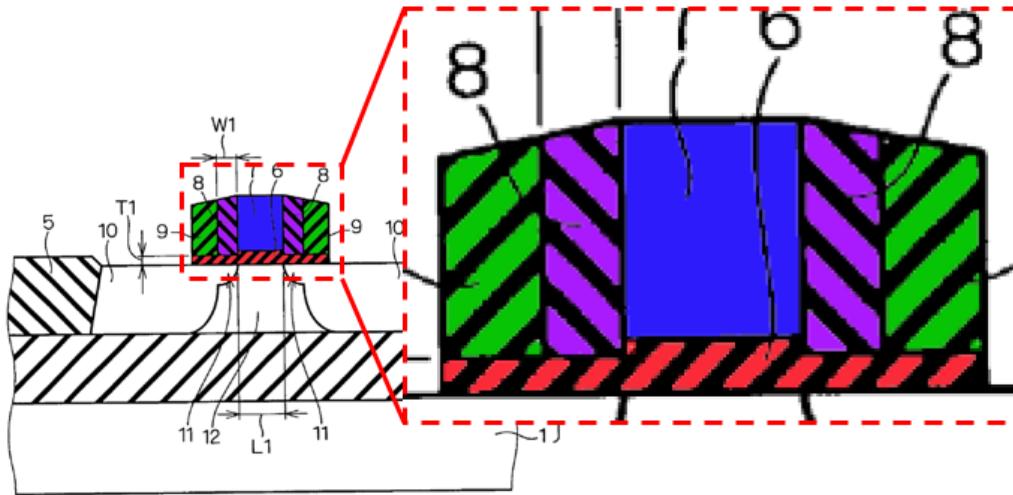


Matsumoto, Figure 22 with enlargement

D. Claim 3

Matsumoto's first embodiment teaches "*the high dielectric constant gate insulating film is continuously formed so as to extend to **under the second insulating sidewall***" and "*part of the high dielectric constant gate insulating film located under the second insulating sidewall has the same thickness as a thickness of part of the high dielectric constant gate insulating film located under the first insulating sidewall*" [3]. (TSMC-1003, ¶¶125-28.)

As shown in the enlargement of Matsumoto's Figure 1, high-k gate insulating film 6 (shaded red) is an uninterrupted layer that extends from under the gate to under both film 8 ("*first insulating sidewall*") and film 9 ("*second insulating sidewall*"). The thickness of high-k film 6 is the same under the film 8 ("*first insulating sidewall*") and film 9 ("*second insulating sidewall*"). (TSMC-1003, ¶¶127-28; *Unified*, 2022 WL 500391, at *17.) The fabrication process of the first embodiment, discussed in §V.B.5.a, confirms the Figure 1 device structure. (See also TSMC-1009, ¶¶107-10, 114-15; TSMC-1003, ¶¶113-15.)



Matsumoto, Figure 1 with enlargement

VI. GROUND 2: Combination of Matsumoto and Wang Renders Claims 7-8, 14 Obvious.

Matsumoto does not expressly disclose “a buffer insulating film”, recited in claims 7-8. And while Matsumoto discloses exemplary high-k dielectrics, it does not explicitly disclose a high-k film “formed of a Hf based oxide” [14]. Wang discloses these teachings.

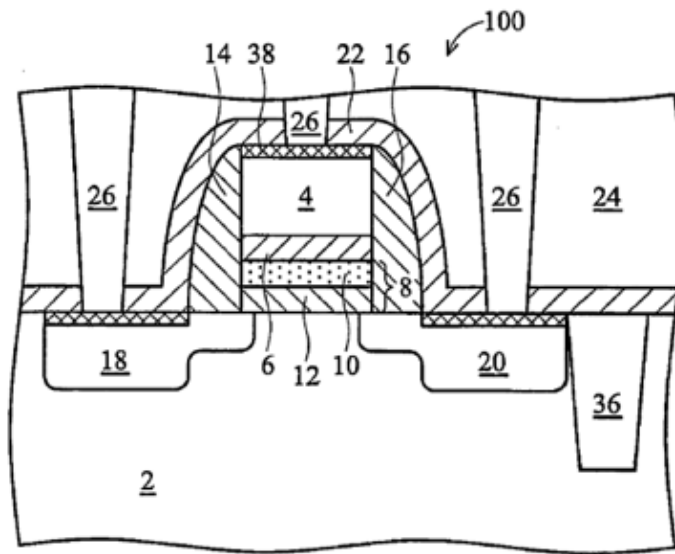
A. Wang

Wang “relates to an improved input/output transistor device having a composite gate dielectric comprising a nitrogen containing, high-k dielectric, and an underlying dielectric layer having a nitrogen containing portion in contact with the high-k dielectric layer and a non-nitrogen containing portion that is in contact with the substrate.” (TSMC-1012, ¶2.) Wang and Matsumoto are in the same field

as the '227 patent, “a semiconductor device and a method for fabricating.”

(TSMC-1001, 1:8-9; TSMC-1009, ¶2; TSMC-1012, ¶2; TSMC-1003, ¶130.)

Wang’s transistor 100 includes a gate stack with high-k dielectric layer 6 formed on dielectric layer 8 comprising a nitrided portion 10 and a non-nitrided/substantially nitrogen-free portion 12. (TSMC-1012, ¶¶22, 24, 48, Figure 3 (below).) Wang presents a list of alternatives for its high-k gate dielectric including Hf-based dielectrics (e.g., HfO₂, HfSiO, HfON, or HfSiON). (TSMC-1012, ¶¶9, 25.)



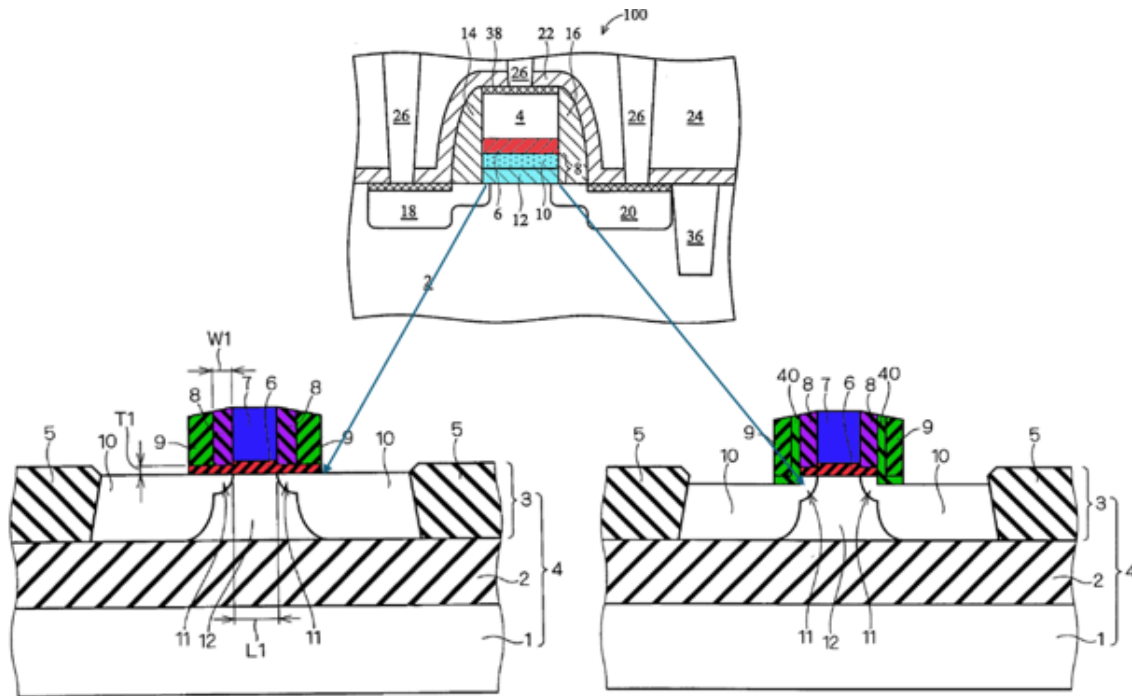
Wang, Figure 3

B. Claims 7-8

The combination of Matsumoto (first/fourth embodiments) and Wang discloses “a buffer insulating film between the substrate and the high dielectric

constant gate insulating film” [7] where “*the buffer insulating film is a silicon oxide film or a silicon oxynitride film*” [8]. (TSMC-1003, ¶¶133-36.)

A POSITA would have been motivated to combine Wang’s teachings regarding use of a dielectric layer between a high-k gate insulating film and the silicon substrate with Matsumoto’s first and fourth embodiment devices. (TSMC-1003, ¶¶133, 137.) For example, a POSITA would have been motivated to integrate Wang’s underlying dielectric layer 8 (shaded aqua) between the substrate and Matsumoto’s high-k dielectric (shaded red) in the first embodiment device (Figure 1) and fourth embodiment device (Figure 22). (*Id.*)



Wang, Figure 3 (top); Matsumoto, Figures 1 (left), 22 (right)

Wang's underlying dielectric 8 is "preferably formed of silicon oxide" and "has a first, nitrided portion 10 that is in contact with high-k dielectric layer 6 and a second non-nitrided, or substantially nitrogen-free, portion 12 that is in contact with the underlying substrate 2." (TSMC-1012, ¶48.) Underlying dielectric 8 is therefore a "*buffer insulating film*", a "*silicon oxide film*" (e.g., in non-nitrided portion 12) and a "*silicon oxynitride film*" (e.g., in nitrided portion 10). (TSMC-1003, ¶¶134-35; TSMC-1038, 88-89 (describing use of "nitrided oxides" including SiO_xN_y).) Alternatively, either portion 10 or portion 12 is the "*buffer insulating film*." (TSMC-1003, ¶135.) In the combination, Wang's underlying dielectric 8 is between the substrate and Matsumoto's high-k gate insulating film 6.

Wang explicitly motivates the above combination, teaching that "[d]ue to the undesirable interactions between high-k dielectrics and the underlying semiconductor material (usually silicon, germanium, silicon germanium, and the like) to degrade carrier mobility, a thin silicon oxide layer is typically employed as part of the gate dielectric even when a high-k gate dielectric is employed." (TSMC-1012, ¶3.) This is consistent with the purpose of the buffer insulating film in the '227 patent. (TSMC-1001, 12:9-15 (by using a buffer insulating film, "deterioration of an interface between a substrate and a gate insulating film can be suppressed").) Wang further stresses that "underlying dielectric layer 8 advantageously provides higher mobility and higher reliability for the high-k

peripheral (or I/O) device.” (TSMC-1012, ¶28.) A POSITA would have therefore been motivated to use Wang’s buffer insulating layer to improve carrier mobility and performance of the Matsumoto’s first or fourth embodiment device. (TSMC-1003, ¶¶137-38; TSMC-1009, ¶13 (describing objective to reduce malfunctions and operating characteristic variations).)

Applying Wang’s buffer layer to Matsumoto’s first or fourth embodiment device is merely the use of a known technique (Wang’s buffer insulating layer) to improve similar devices in the same way for the above reasons. *See KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 416-17 (2007); TSMC-1003, ¶139. A POSITA would have had a reasonable expectation of success in the combination and the results of the combination would have been predictable because Wang uses established methods for forming the underlying dielectric and its high-k gate dielectric. (TSMC-1012, ¶22 (describing “thermally grown oxide”), ¶24 (describing use of CVD, ALD and PVD for deposition of high-k film); *see also* TSMC-1009, ¶107 (describing use of CVD for high-k film deposition); TSMC-1003, ¶¶140-42.)

C. Claim 14

The combination of Matsumoto (first/fourth embodiments) and Wang discloses “*the high dielectric constant gate insulating film is formed of a Hf based oxide*” [14]. (TSMC-1003, ¶¶143-47.)

Matsumoto teaches use of a high-k film “such as Al_2O_3 or a ferroelectric film such as Ta_2O_5 and BST” as a gate insulating film. (TSMC-1009, ¶107.) Wang teaches use of similar high-k dielectrics (e.g., Al_2O_3 and Ta_2O_5) and others including “ HfO_2 ” which is a Hf-based oxide. (TSMC-1012, ¶12; *see also* TSMC-1012, ¶¶9, 25.) By 2005, a POSITA would have been motivated to select HfO_2 given its known benefits, including, for example, “its superior thermal stability with poly-Si and reasonable band alignment.” (TSMC-1037, 2.4.1; *see also* TSMC-1032, 207 (HfO_2 “combines a high k (15-26) with a bandgap of 5.6 eV, with favourable conduction and valence band offsets with respect to Si ...”); TSMC-1049, 6.1.2 (“Excellent dielectric properties ... suggest that HfO_2 is a promising material for the future gate dielectric application.”); TSMC-1003, ¶146.) Another known benefit is that HfO_2 can be scaled down to a smaller EOT. (*See* TSMC-1032, 207; TSMC-1003, ¶146.)

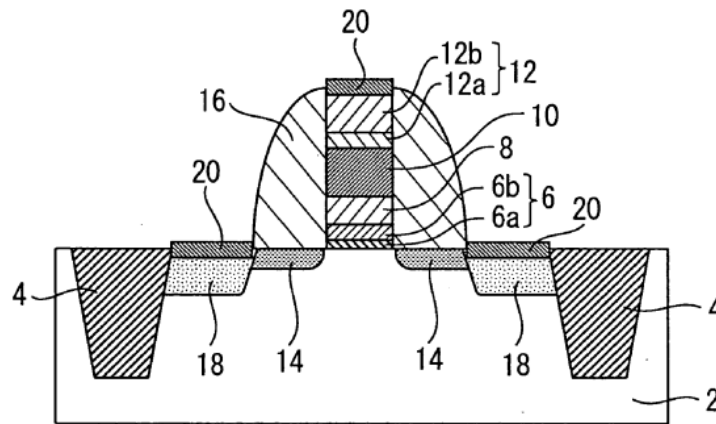
VII. GROUND 3: Combination of Matsumoto and Mutou Renders Claims 7-8 Obvious.

Should an argument be made that the combination of Matsumoto and Wang fails to render claims 7-8 obvious, Mutou also explicitly describes a “*buffer insulating film*,” and the combination of Matsumoto with Mutou renders claims 7-8 obvious. (TSMC-1003, ¶148.)

A. Mutou

Mutou's device includes a silicon substrate 2 and a gate stack comprising interfacial layer 6a, high-k dielectric film 6b, and a multilayer gate electrode.

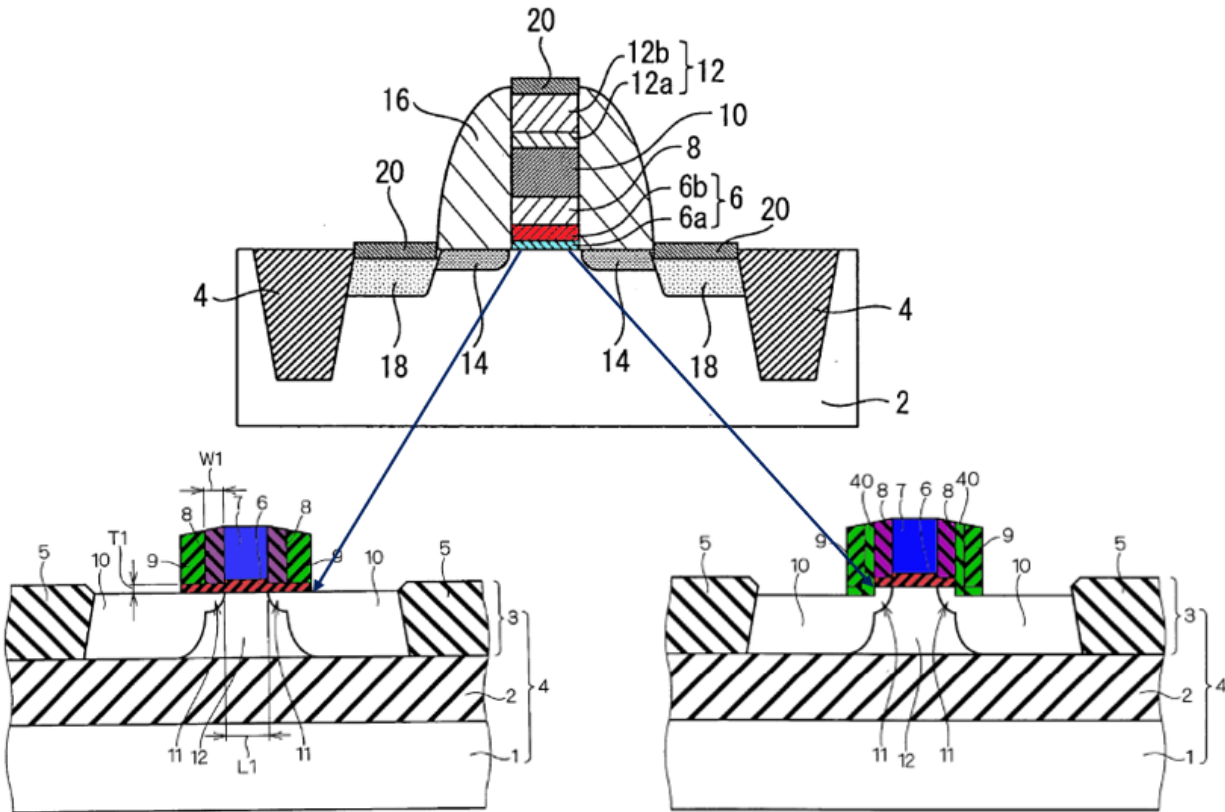
(TSMC-1019, ¶¶40-41, 44, Figure 1 (below).) Mutou and Matsumoto are in the same field as the '227 patent, “a semiconductor device and a method for fabricating.” (TSMC-1001, 1:8-9; TSMC-1009, ¶2; TSMC-1019, Abstract, ¶¶2, 4; TSMC-1003, ¶130.)



Mutou, Figure 1

B. Motivation to Combine

A POSITA would have been motivated to integrate Mutou’s underlying interfacial layer 6a (“*buffer insulating film*”) (shaded aqua) under Matsumoto’s high-k dielectric (shaded red) in the first embodiment (Figure 1) and fourth embodiment (Figure 22) devices, as shown below. (TSMC-1003, ¶151.)



**Mutou, Figure 1 (top);
Matsumoto, Figures 1 (bottom-left), 22 (bottom-right)**

Mutou expressly motivates the combination, teaching that “[t]he underlying interfacial layer 6a is acted to inhibit interfacial reaction between the silicon substrate 2 and the high-k dielectric film 6b.” (TSMC-1019, ¶42.) Inhibiting such reactions between the substrate and the high-k film decreases degradation of the high-k film and, thus, improves performance of the device. (TSMC-1003, ¶154; *see also* TSMC-1001, 12:9-15 (by using a buffer insulating film, “deterioration of an interface between a substrate and a gate insulating film can be suppressed”).) This furthers the goal of Matsumoto “to provide a semiconductor device which

achieves reductions in malfunctions and operating characteristic variations.”

(TSMC-1009, ¶13.) Based on these disclosures, a POSITA would have been motivated to make the above combination to inhibit interfacial reaction between the substrate and the high-k film and improve performance of Matsumoto’s devices. (TSMC-1003, ¶154.)

The above combination is nothing more than the use of a known technique (Mutou’s underlying interfacial layer) to improve similar devices in the same way for the reasons discussed above. *See KSR*, 550 U.S. at 416-17; TSMC-1003, ¶155. A POSITA would have had a reasonable expectation of success in the combination and the results of the combination would have been predictable because Mutou uses conventional processes to form the underlying interfacial layer and deposit the high-k gate insulating film on top. (TSMC-1019, ¶¶53-54; *see also* TSMC-1009, ¶107; TSMC-1003, ¶¶156-58.)

C. Claims 7-8

Mutou’s interfacial layer 6a is formed on the silicon substrate 2 and high-k dielectric film 6b is formed on interfacial layer 6a. (TSMC-1019, ¶41.) Mutou’s interfacial layer 6a, as used in Matsumoto’s first and fourth embodiment devices, is “a buffer insulating film.” (TSMC-1003, ¶¶152-53.) Underlying interfacial layer 6a may be, “for example, a SiO₂ film, a Si₃N₄ film, or a SiON film” (TSMC-1019, ¶42.)

Thus, the combination of Matsumoto (First/Fourth Embodiments) and Mutou discloses “*a buffer insulating film between the substrate and the high dielectric constant gate insulating film*” [7] where “*the buffer insulating film is a silicon oxide film or a silicon oxynitride film*” [8]. (TSMC-1003, ¶¶152-53.)

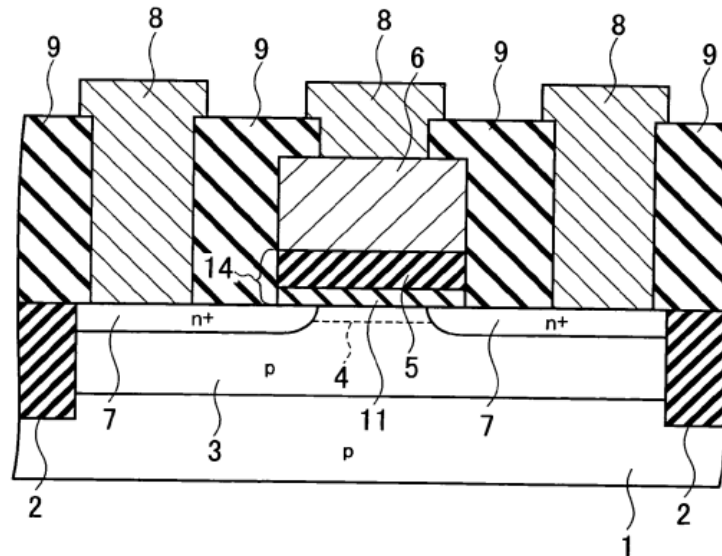
VIII.GROUND 4: Combination of Matsumoto and Ono Renders Claims 6 and 14 Obvious.

Matsumoto’s first and fourth embodiment devices do not expressly disclose that the high-k gate insulating film “*includes a notch at a side end portion*” [6] or “*is formed of a Hf based oxide*” [14]. These features are disclosed in Ono, and the combination of Matsumoto and Ono renders claims 6 and 14 obvious.

A. Ono

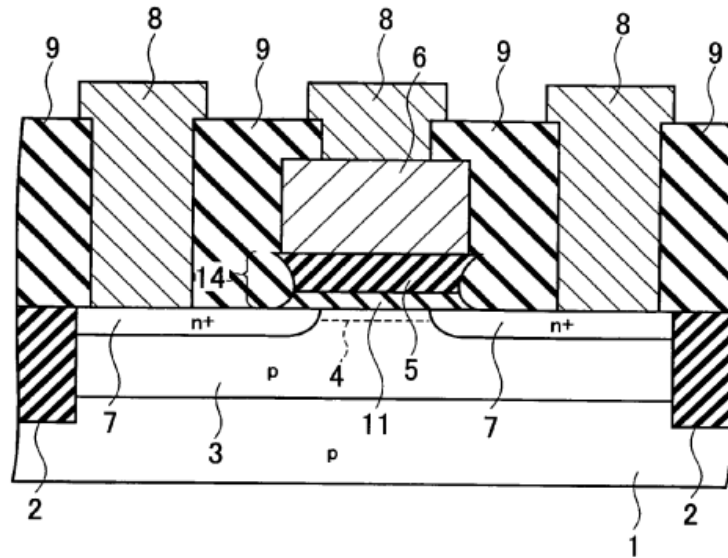
Ono’s second embodiment FET includes a gate stack comprising gate insulator film 5 “made of a metal oxide” and gate insulator film 11 “made of a metal oxide with a higher dielectric constant than the gate insulator film 5.” (TSMC-1013, ¶207, Figure 77.) Gate insulator film 5 is made of a “HfO₂ film.” (TSMC-1013, ¶209.) Gate electrode 6 is formed on gate insulator film 5 and can have gate sidewalls. (TSMC-1013, ¶¶207, 181 (in the first embodiment, “gate sidewalls are not mentioned; however, sidewalls may be provided to the gate electrode”), 210 (“Various modifications as described in the first embodiment are also possible with this [second] embodiment, and the same effects may be obtained.”), Figure 77; TSMC-1003, ¶¶160-63.) Ono and Matsumoto are in the

same field as the '227 patent, “a semiconductor device and a method for fabricating.” (TSMC-1001, 1:8-9; TSMC-1009, ¶2; TSMC-1013, Abstract, ¶¶3-7; TSMC-1003, ¶160.)



Ono, Figure 77

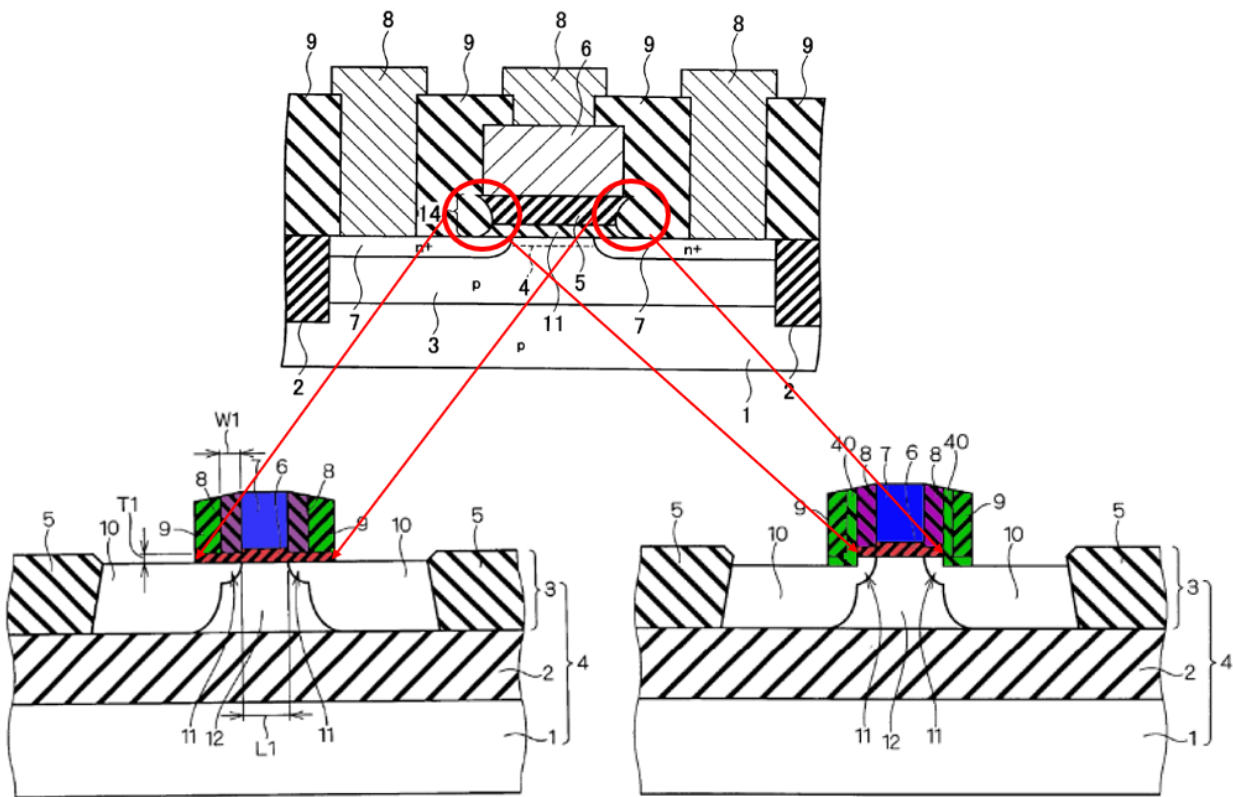
Ono discloses a modification of its second embodiment device where the sidewalls of its gate insulating film “may curve.” (TSMC-1013, ¶216.) Ono discloses numerous examples of such curved end portions (Figures 104-123). (*Id.*) Petitioner focuses its analysis on the structure depicted in Figure 108 (below), although other structures are equally applicable.



Ono, Figure 108

B. Motivation to Combine

A POSITA would have been motivated to apply Ono's teaching of curving the end portion of a gate insulating film to Matsumoto's first and fourth embodiment devices, as shown below. (TSMC-1003, ¶167.) Thus, in the combination, the side ends of Matsumoto's gate insulating film have a semicircular shape, as taught by Ono.



**Ono, Figure 108 (top);
Matsumoto, Figures 1 (bottom-left), 22 (bottom-right)**

Ono expressly suggests the combination, teaching that using curved side surfaces for the gate insulating film “reduc[es] the scattering of carriers as well as enhanc[es] the controllability of the gate electrode with respect to the potential of the channel region” and therefore provides “an advantage of optimization.” (TSMC-1013, ¶216; *see also* TSMC-1013, ¶200 (noting, for the first embodiment, that by using curved side surfaces for the gate insulating film, “the electrical capacitance between the gate electrode 6 and the source/drain regions 7 may be adjusted,” resulting in “an advantage of optimization”). A POSITA would have

therefore been motivated to curve the end of Matsumoto's gate insulating film to optimize parasitic resistance and parasitic capacitance, improving device performance. (TSMC-1003, ¶¶169-71; TSMC-1040, ¶108; §IV.B.2.)

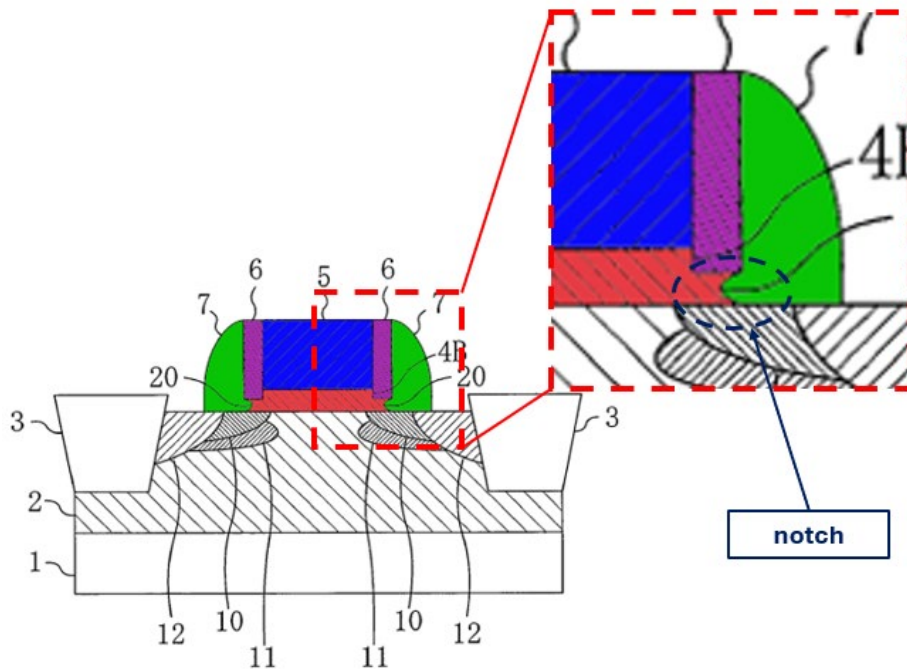
The combination of Ono and Matsumoto is merely the application of a known technique (Ono's curved film ends) to improve similar devices in the same way for the reasons discussed above. *See KSR*, 550 U.S. at 416-17; TSMC-1003, ¶172. A POSITA would have had a reasonable expectation of success in the combination and the results of the combination would have been predictable. (TSMC-1003, ¶172.) Matsumoto and Ono both use high-k gate insulating films that extend under the gate electrode and the insulating sidewall, a concept well-known before the '227 patent. (*See* §§IV.B.2.b, IV.D.2, V.B.5, VIII.A.) And both form their high-k dielectrics using conventional techniques. (TSMC-1009, ¶114; TSMC-1013, ¶167; TSMC-1003, ¶172.)

C. Claim 6

The combination of Matsumoto (first/fourth embodiments) and Ono discloses "*the high dielectric constant gate insulating film includes a notch at a side end portion.*" (TSMC-1003, ¶¶166-72.)

In the devices of the combination of Matsumoto (first/fourth embodiments) and Ono, the end portion of Matsumoto's gate insulating film has a semicircular shape under the sidewall, as taught by Ono in, e.g., Figure 108. The combination of

Matsumoto (first/fourth embodiments) and Ono therefore discloses “*the high dielectric constant gate insulating film includes a notch at a side end portion*” [6], consistent with the disclosure of the ’227 patent. (See, e.g., TSMC-1001, 8:31-36 (referring to notch 20 of Figure 7), Figure 7 (depicting notch 20 having a semicircular shape); TSMC-1003, ¶168.)



'227 Patent, Figure 7 with enlargement

D. Claim 14

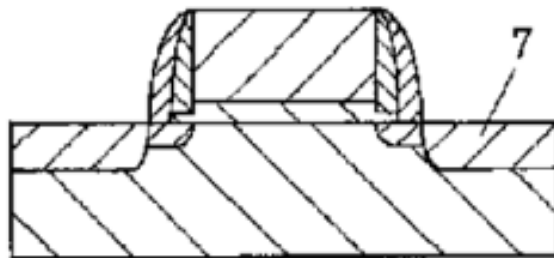
The combination of Matsumoto (first/fourth embodiments) and Ono further discloses “*the high dielectric constant gate insulating film is formed of a Hf based oxide*” [14]. (TSMC-1003, ¶¶173-75.) Ono teaches that its gate insulator film 5 is made of “HfO₂ film.” (TSMC-1013, ¶209.) A POSITA would have been motivated to use a Hf-based oxide as a gate insulating layer as taught by Ono in Matsumoto’s

first and fourth embodiments for the reasons discussed in §VI.C, including HfO₂'s superior thermal stability, reasonable band alignment, and ability to be scaled down to a smaller EOT. (TSMC-1003, ¶174; TSMC-1037, 2.4.1; TSMC-1032, 207; TSMC-1049, 6.1.2.)

IX. GROUND 5: Kajiyama Anticipates Claims 1-2.

A. Kajiyama

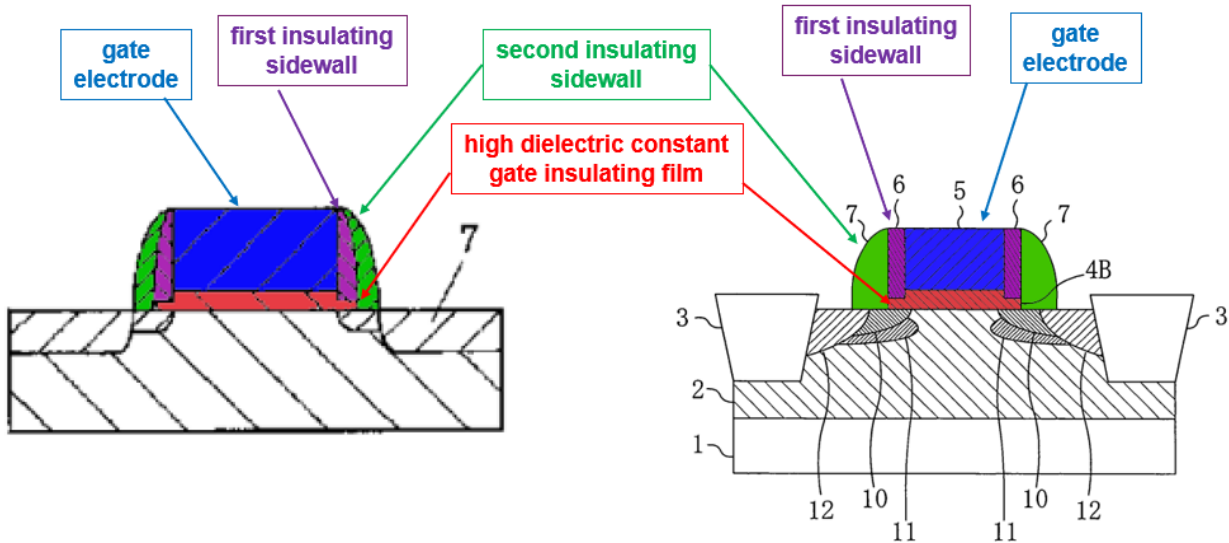
Kajiyama is directed to “semiconductor devices” and “in particular to insulating gate type field effect transistors having a gate dielectric film (high dielectric constant material).” (TSMC-1011, ¶1.) Kajiyama discloses two embodiments of its semiconductor device. This Petition focuses on Kajiyama's first embodiment FET (shown in Figure 1(D) below), which includes a gate electrode with two sidewalls. A high-k gate insulating film extends from under the gate electrode to under only the first sidewall. (TSMC-1011, ¶¶1, 28, Figure 1(D) (below).)



Kajiyama, Figure 1(D)

B. Independent Claim 1

Kajiyama's first embodiment device anticipates claim 1, as illustrated by the side-by-side figures below.



Kajiyama, Figure 1(D)

'227 Patent, Figure 2

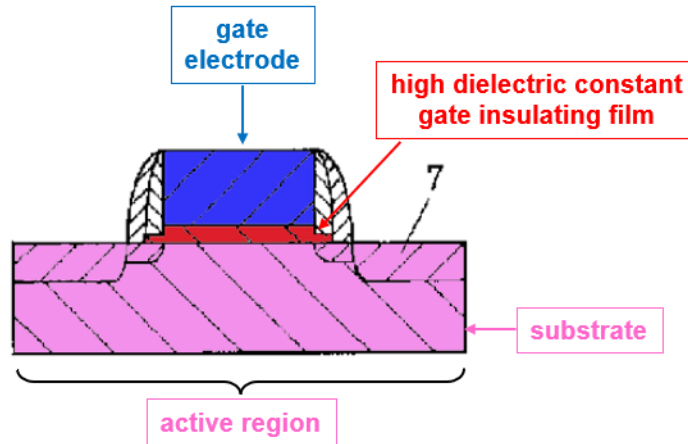
1. Preamble [1P]

Kajiyama's first embodiment discloses a "*semiconductor device*": "[t]he present invention relates to semiconductor devices and manufacturing methods thereof, and in particular to insulating gate type field effect transistors having a gate dielectric film (high dielectric constant material)." (TSMC-1011, ¶1; *see also* TSMC-1011, ¶27; TSMC-1003, ¶180.)

2. Limitations [1A]-[1B]

Kajiyama teaches “*a high dielectric constant gate insulating film formed on an active region in a substrate*” [1A] and “*a gate electrode formed on the high dielectric constant gate insulating film*” [1B]. (TSMC-1003, ¶¶181-86.)

Kajiyama’s device has a “p-type Si **substrate** [shaded pink]” with an “element separation layer (not shown) on the Si substrate 1.” (TSMC-1011, ¶¶28-29, Figure 1(D) (below).) Kajiyama’s element separation layer is equivalent to the ’227 patent’s STI structures. (TSMC-1011, ¶¶5, 29; TSMC-1001, 7:26-43 (showing active region with source/drain regions surrounded by STI structures 3); TSMC-1003, ¶183.) In Kajiyama, within the region defined by the element separation layer, an n-type LDD diffusion layer 4 is formed and, in a subsequent process step, an n⁺ source drain diffusion layer 7 is formed. (TSMC-1011, ¶¶29, 32, Figures 1(A), 1(D).) The region defined by Kajiyama’s element separation layer is “*an active region in a substrate.*” (TSMC-1003, ¶183.)



Kajiyama, Figure 1(D)

Kajiyama’s “device comprises a gate insulating film [labeled 2 in Figure 1(A)] consisting of a high dielectric film¹⁴ [shaded red] formed on a semiconductor substrate.” (TSMC-1011, ¶¶14, 28, claim 1 (reciting “a gate insulating film consisting of a high dielectric film formed on a semiconductor substrate, a gate electrode consisting of a conductive film formed on the gate insulating film”), Figure 1(D) (above).) The high-k film, formed on the substrate within the element separation layer, is therefore the “*high dielectric constant gate insulating film formed on an active region in a substrate.*” (TSMC-1011, ¶29; TSMC-1003, ¶¶184-85.)

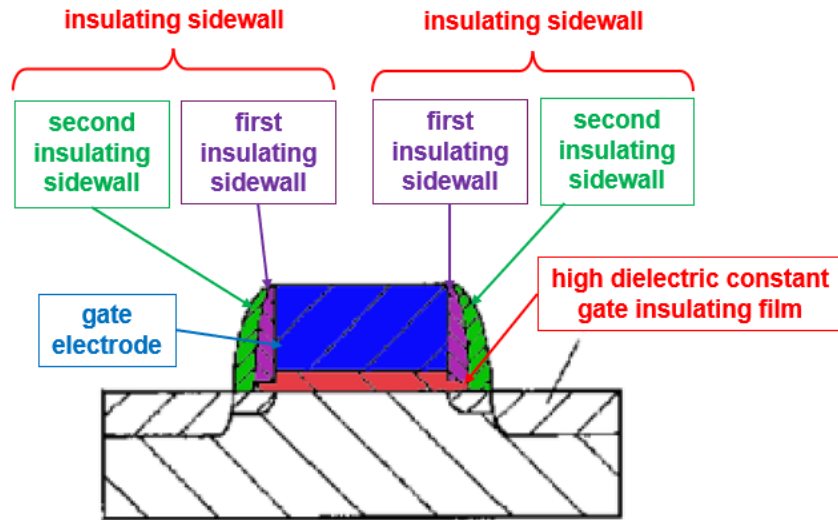
¹⁴ Kajiyama also refers to the high-k film 2 as “ZrO₂ film 2”. (See, e.g., TSMC-1011, ¶29.)

Gate electrode 3 (shaded blue) “consisting of a conductive film [is] formed on [the] gate insulating film.” (TSMC-1011, ¶14.) Kajiya’s device thus includes “*a gate electrode formed on the high dielectric constant gate insulating film*” [1B]. (TSMC-1003, ¶186.)

3. Limitations [1C]/[1F]

Kajiya’s device includes “a first sidewall [labeled 5 in Figure 1(B), shaded purple below] consisting of a dielectric film formed on a sidewall of the gate electrode, and a second sidewall [labeled 6 in Figure 1(C), shaded green below] ... formed to cover the first sidewall.” (TSMC-1011, ¶¶14, 28, Figure 1(D) (below).) Kajiya teaches that first sidewall 5 “consist[s] of ZrO₂ film (**insulation** film)” while also noting that “the effects of the present invention can be obtained even with other dielectric films [for first sidewall 5], such as TEOS films, BPSG films, or SiON films.” (TSMC-1011, ¶¶28, 47.) TEOS, BPSG, and SiON are each silicon-based oxides and known insulating materials. (TSMC-1003, ¶189.) First sidewall 5 is therefore a “*first insulating sidewall formed on a side surface of the gate electrode...*” [1F]. (*Id.*) Second sidewall 6 is a silicon nitride film (referred to as Si₃N₄ film) and is therefore a “*second insulating sidewall formed on the side surface of the gate electrode with the first insulating sidewall interposed therebetween*” [1F]. (TSMC-1011, ¶28.) First sidewall 5 and second

sidewall 6 are collectively “an insulating sidewall formed on each side surface of the gate electrode” [1C]. (TSMC-1003, ¶¶189-90.)

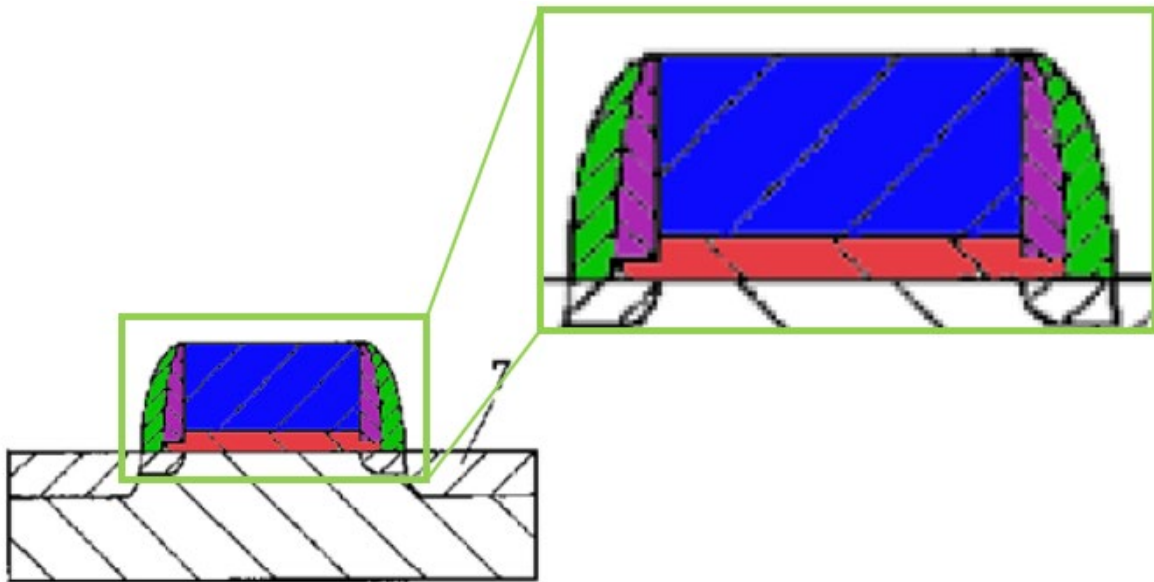


Kajiyama, Figure 1(D)

4. Limitations [1D]-[1E]/[1G]-[1H]

As shown in the enlargement of Kajiyama’s device and confirmed by the disclosed process, high-k film 2 (shaded red) is an uninterrupted layer (as evidenced by the absence of gaps) that extends from under the gate electrode to under first sidewall 5 (“*first insulating sidewall*”; shaded purple) which is part of the collective “*insulating sidewall*” (sidewall 5 and sidewall 6). The high-k film is thinner under sidewall 5 (“*first insulating sidewall*”) than it is under the gate electrode (shaded blue). Kajiyama’s device therefore discloses that “*the high dielectric constant gate insulating film is continuously formed so as to extend from under the gate electrode to under the insulating sidewall*” [1D], “*at least part of*

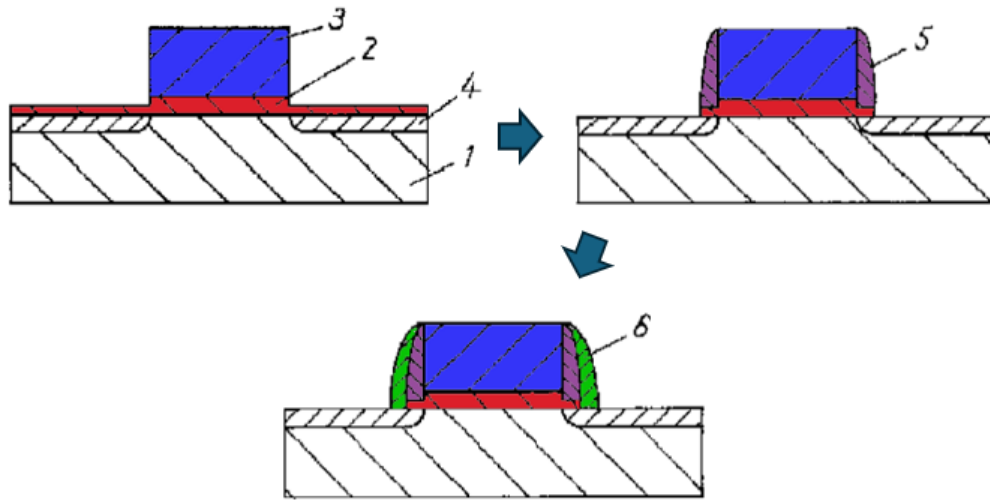
*the high dielectric constant gate insulating film located under the insulating sidewall has a smaller thickness than a thickness of part of the high dielectric constant gate insulating film located under the gate electrode” [1E], “the high dielectric constant gate insulating film is continuously formed so as to extend from under the gate electrode to under the first insulating sidewall” [1G], and “part of the high dielectric constant gate insulating film located under the first insulating sidewall has a smaller thickness than a thickness of part of the high dielectric constant gate insulating film located under the gate electrode” [1H]. (TSMC-1003, ¶¶191-96; see *Unified*, 2022 WL 500391, at *17.)*



Kajiyama, Figure 1(D) with enlargement

Kajiyama’s fabrication process confirms the Figure 1(D) structure. During fabrication, an n-type polySi film is deposited on high-k film 2 and etched “to form

a gate electrode 3.” (TSMC-1011, ¶29.) High-k film 2 “is also etched to reduce the film.” (TSMC-1011, ¶29, Figure 1(A) (top-left).) As a result of this process, the thickness of high-k film 2 is larger under the gate electrode than elsewhere. (TSMC-1003, ¶194.)



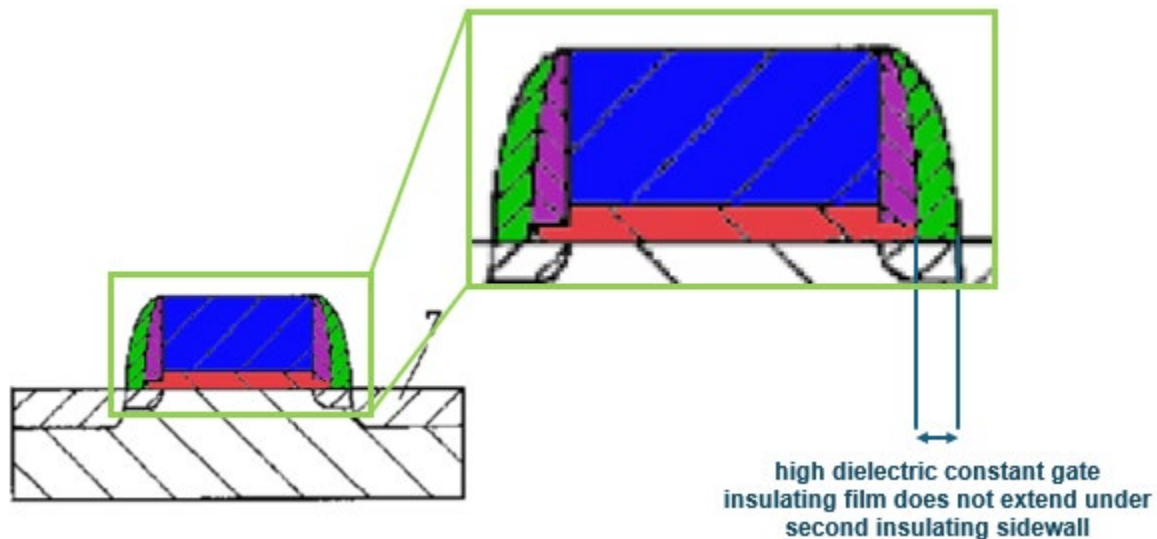
**Kajiyama, Figures 1(A)(above-left),
1(B)(above-right), 1(C)(bottom)**

First sidewall 5 (shaded purple) is then formed on the side of gate electrode 3 and over the thinner portion of the high-k film. (TSMC-1011, ¶30, Figure 1(B)(top-right).) The high-k film is then etched “to remove all.” (TSMC-1011, ¶30.) That is, the high-k film outside the outer edge of sidewall 5 is removed. (TSMC-1003, ¶¶195-96.) Next, second sidewall 6 (shaded green) is formed “to cover the first sidewall 5 [shaded purple] provided on the sidewall of the gate electrode 3 [shaded blue].” (TSMC-1011, ¶31, Figure 1(C) (bottom).) As shown above, a portion of the high-k dielectric film (shaded red) remains under the gate

electrode and first sidewall 5 but does not extend under sidewall 6. (TSMC-1003, ¶196.)

C. Claim 2

As shown in the enlargement of Figure 1(D) below, the high-k dielectric film (shaded red) remains only under the gate electrode and the first sidewall—it is not “*located under the second insulating sidewall*” [2] (sidewall 6, shaded green). See *Unified*, 2022 WL 500391, at *17; TSMC-1003, ¶¶197-99. The fabrication process, discussed in §IX.B.4, confirms the structure illustrated in Figure 1(D). (See TSMC-1011, ¶¶30-31.)



Kajiyama, Figure 1(D) with enlargement

X. GROUND 6: Kajiyama Renders Claims 9 and 14 Obvious.

A. Claim 9

Kajiyama renders obvious “*the gate electrode is a fully silicided gate electrode of which an entire region has been silicided*” [9]. (TSMC-1003, ¶¶200-01.) Specifically, Kajiyama teaches that “the effect of the present invention can be obtained by using another conductive film, such as W film, TiN film, WSi₂ film, etc., metal gate or **silicide gate** instead.” (TSMC-1011, ¶48.) A POSITA would have therefore been motivated to use a fully silicided gate in the first embodiment device based on this explicit teaching. (TSMC-1003, ¶¶200-01; *see also* TSMC-1042, 1:40-54 (describing benefits of full silicidation).)

B. Claim 14

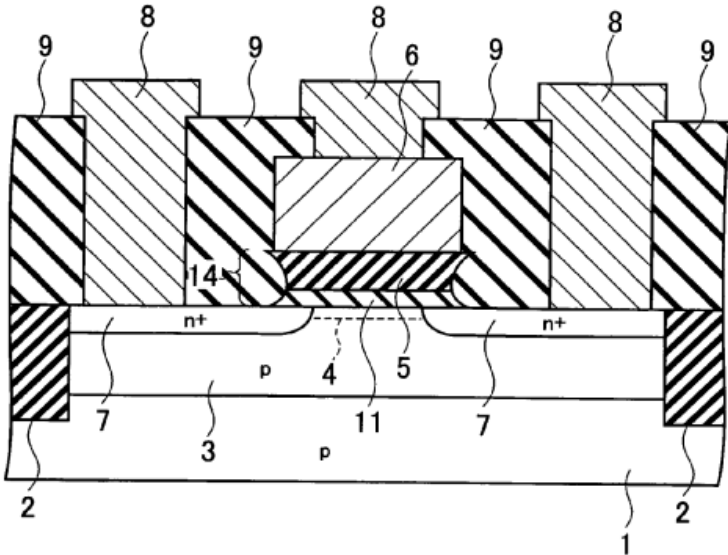
Kajiyama renders “*the high dielectric constant gate insulating film is formed of a Hf based oxide*” [14] obvious. (TSMC-1003, ¶202.)

Kajiyama discloses that, while the gate insulating film 2 in the first embodiment is a ZrO₂ film, “other high dielectric films, such as a **HfO₂** film, a Ta₂O₅ film, or Al₂O₃ film, can be used instead to obtain the effects of the invention.” (TSMC-1011, ¶45.) A POSITA would have been motivated to select HfO₂ as the high-k material for Kajiyama’s gate dielectric for the reasons discussed in §VI.C. (TSMC-1003, ¶202; TSMC-1037, 2.4.1; TSMC-1032, 207; TSMC-1049, 6.1.2.)

Obvious.

that high-k gate insulating film “*includes a notch at a side end portion*” [6]. Ono

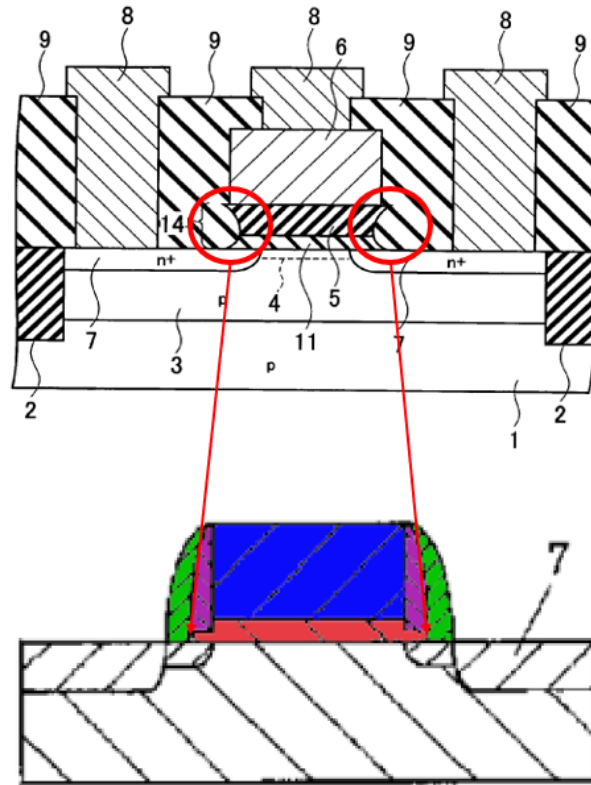
shown, e.g., in Figure 108 (below). (TSMC-1013, ¶216; §VIII.A; TSMC-1003,



Ono, Figure 108

the end portions of a gate insulating film to Kajiyama's high-k dielectric (shaded

red) in the first embodiment (Figure 1(D)), as illustrated below. (TSMC-1003, ¶205.) Thus, in the combination, the side ends of Kajiyama's gate insulating film have a semicircular shape, as taught by Ono.

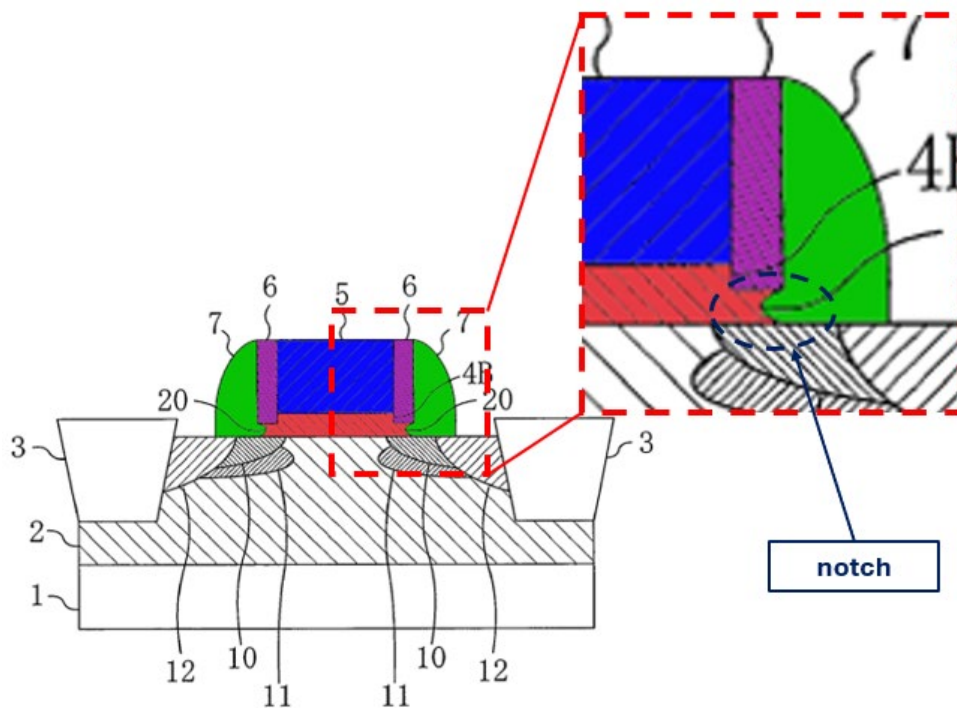


Ono, Figure 108 (top); Kajiyama, Figure 1(D) (bottom)

A POSITA would have been motivated to make the above combination because Ono expressly suggests the combination, as discussed in §VIII.B, and to improve performance of Kajiyama's first embodiment device by optimizing the electrical capacitance between the gate electrode and the source/drain regions. (TSMC-1013, ¶¶215-16; TSMC-1003, ¶207.)

The combination of Ono and Kajiyama is nothing more than the use of a known technique (Ono's use of curved side surfaces for a gate insulating film) to improve similar devices in the same way for the above reasons. *See KSR*, 550 U.S. at 416-17; TSMC-1003, ¶208. A POSITA would have had a reasonable expectation of success in the combination and the results of the combination would have been predictable. (TSMC-1003, ¶208.) Kajiyama and Ono both use high-k gate insulating films that extend under the gate electrode and the insulating sidewall, a concept well-known before the '227 patent. (*See* §§IV.B.2.b, IV.D.2, IX.B.4, VIII.A.) And both form their high-k dielectrics using conventional techniques. (TSMC-1011, ¶29; TSMC-1013, ¶167; TSMC-1003, ¶210.)

In the device of the combination of Kajiyama and Ono, the end portion of Kajiyama's gate insulating film has a semicircular shape, as taught by Ono. The combination of Kajiyama and Ono therefore discloses a device where "*high dielectric constant gate insulating film includes a notch at a side end portion*", consistent with the disclosure of the '227 patent. (*See, e.g.*, TSMC-1001, 8:31-36 (referring to notch 20 of Figure 7), Figure 7 (depicting notch 20 having a semicircular shape); TSMC-1003, ¶206.)



'227 Patent, Figure 7 with enlargement

XII. Discretionary Denial Is Not Appropriate.

A. 35 U.S.C. §314(a)

Pursuant to the Stewart Memorandum dated March 26, 2025, titled “Interim Process for PTAB Workload Management,” Petitioner will respond to any discretionary denial arguments Patent Owner may raise through the Board’s bifurcated briefing process.

Nevertheless, to simplify the *Fintiv* analysis, and following the precedential *Sotera* decision, Petitioner stipulates that, if IPR is instituted, Petitioner will not pursue in the related district court proceeding any ground that Petitioner raised or

reasonably could have raised against the challenged claims during the instituted IPR.

B. 35 U.S.C. §325(d)

The *Advanced Bionics* framework favors institution. *Advanced Bionics LLC v. MED-EL Elektromedizinische Gerate GmbH*, IPR2019-01469, Paper 6 (P.T.A.B. Feb. 13, 2020) (precedential). None of the applied references was applied by the Examiner during prosecution. Applicant cited a different JP publication to Ono (JP2005-064190; “JP-Ono”) on an information disclosure statement. While Petitioner disputes that JP-Ono is sufficiently similar to Ono to trigger *Advanced Bionics* Part 1, JP-Ono was not applied by the Examiner and thus was not evaluated during examination. Even assuming JP-Ono was evaluated (which the record does not support), the Office erred in allowing the claims. Petitioner relies on Ono only for dependent claims 6 and 14. Petitioner’s other cited art discloses all limitations of independent claim 1, including (1) a sidewall with first and second insulating sidewalls and (2) the thickness of the high-k film under the first insulating sidewall has a smaller thickness than the thickness of the high-k film under the gate electrode. (§§IV.D.1, V.B, IX.B.) The Petition therefore presents grounds never considered by the Office. The Petition’s evidence warrants consideration because it presents a compelling case of unpatentability never

considered by the Office. These circumstances weigh heavily against §325(d) discretionary denial.

XIII.Mandatory Notices

A. Real Party in Interest

The Petitioner and real party-in-interest is Taiwan Semiconductor Manufacturing Company Ltd.

B. Related Matters

To the best of Petitioner's knowledge, the '227 patent is involved in the following ongoing litigation:

- *Advanced Integrated Circuit Process LLC, v. Taiwan Semiconductor Manufacturing Company Limited*, No. 2:24-CV-623 (E.D.T.X.)
- *Advanced Integrated Circuit Process LLC, v. United Microelectronics Corporation*, No. 2:24-CV-730 (E.D.T.X.)

On April 15, 2025, Petitioner filed petitions for *inter partes* review of U.S. Patent 7,923,764 (IPR2025-00829), U.S. Patent 8,253,180 (IPR2025-00830), and U.S. Patent 8,587,076 (IPR2025-00831).

C. Notice of Counsel and Service Information

Pursuant to 37 C.F.R. §§42.8(b)(3), 42.8(b)(4) and 42.10(a), Petitioner appoints the following lead and backup counsel:

Lead Counsel	Back Up Counsel
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	<p>Theodoros Konstantakopoulos, Ph.D. (Reg. No. 74,155) Goodwin Procter LLP 620 Eighth Avenue New York, NY 10018 Phone: (212) 813-8800 Fax: (212) 355-3333 TKonstantakopoulos@goodwinlaw.com</p>
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	<p>Filippos Papadatos (Reg No. 78,834) Goodwin Procter LLP 620 Eighth Avenue New York, NY 10018 Phone: (212) 813-8800 Fax: (212) 355-3333 fpapadatos@goodwinlaw.com</p>

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XIV.Conclusion

Inter partes review of the challenged claims is respectfully requested.

Respectfully submitted,

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Date: April 15, 2025

CERTIFICATE OF WORD COUNT

Pursuant to 37 C.F.R. §42.24(a), Petitioner hereby certifies that portions of the above-captioned **PETITION FOR *INTER PARTES* REVIEW OF U.S. PATENT 7,579,227**, in accordance with and reliance on the word count provided by the word-processing system used to prepare this Petition, that the number of words in this paper is 8,939. Pursuant to 37 C.F.R. §42.24(a), this word count is in compliance and excludes the table of contents, table of authorities, mandatory notices under §42.8, certificate of service, certificate of word count, appendix of exhibits, and any claim listing. This word count was prepared using Microsoft Word.

Respectfully submitted,

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Date: April 15, 2025

CERTIFICATE OF SERVICE

The undersigned hereby certifies, in accordance with 37 C.F.R. § 42.105, that the foregoing **PETITION FOR *INTER PARTES* REVIEW OF U.S. PATENT 7,579,227**, TSMC's Power of Attorney, and all supporting exhibits were served via FedEx Next Business Day Delivery on April 15, 2025, in their entirety on the Patent Owner as detailed below:

Michael J. Cherskov & Szymon M. Gurda
Cherskov, Flaynik & Gurda, LLC
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Courtesy copies have been concurrently served by electronic mail on Patent Owner's litigation counsel at:

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Date: April 15, 2025

Appendix: Challenged Claims Listing

[1P] A semiconductor device comprising:

[1A] a high dielectric constant gate insulating film formed on an active region in a substrate;

[1B] a gate electrode formed on the high dielectric constant gate insulating film; and

[1C] an insulating sidewall formed on each side surface of the gate electrode,

[1D] wherein the high dielectric constant gate insulating film is continuously formed so as to extend from under the gate electrode to under the insulating sidewall,

[1E] at least part of the high dielectric constant gate insulating film located under the insulating sidewall has a smaller thickness than a thickness of part of the high dielectric constant gate insulating film located under the gate electrode,

[1F] the insulating sidewall includes a first insulating sidewall formed on a side surface of the gate electrode and a second insulating sidewall formed on the side surface of the gate electrode with the first insulating sidewall interposed therebetween,

[1G] the high dielectric constant gate insulating film is continuously formed so as to extend from under the gate electrode to under the first insulating sidewall, and

[1H] part of the high dielectric constant gate insulating film located under the first insulating sidewall has a smaller thickness than a thickness of part of the high dielectric constant gate insulating film located under the gate electrode.

[2] The semiconductor device of claim 1, wherein the high dielectric constant gate insulating film is formed so as not to be located under the second insulating sidewall.

[3] The semiconductor device of claim 1, wherein the high dielectric constant gate insulating film is continuously formed so as to extend to under the second insulating sidewall, and part of the high dielectric constant gate insulating film located under the second insulating sidewall has the same thickness as a thickness of part of the high dielectric constant gate insulating film located under the first insulating sidewall.

[6] The semiconductor device of claim 1, wherein the high dielectric constant gate insulating film includes a notch at a side end portion.

[7] The semiconductor device of claim 1, further comprising a buffer insulating film between the substrate and the high dielectric constant gate insulating film.

[8] The semiconductor device of claim 7, wherein the buffer insulating film is a silicon oxide film or a silicon oxynitride film.

[9] The semiconductor device of claim 1, wherein the gate electrode is a fully silicided gate electrode of which an entire region has been silicided.

[14] The semiconductor device of claim 1, wherein the high dielectric constant gate insulating film is formed of a Hf based oxide.