UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

TAIWAN SEMICONDUCTOR MANUFACTURING COMPANY LTD.,

Petitioner

v.

ADVANCED INTEGRATED CIRCUIT PROCESS LLC,

Patent Owner

Case IPR2025-00828
Patent 7,579,227

PATENT OWNER'S PRELIMINARY RESPONSE UNDER 37 C.F.R. § 42.107 TO PETITION FOR *INTER PARTES* REVIEW OF U.S. PATENT NO. 7,579,227

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EXHIBIT LIST

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EX2001	**Complaint for Patent Infringement,** Dkt. No. 1, *Advanced Integrated Circuit Process LLC v. Taiwan Semiconductor Manufacturing Company Limited,* Case No. 2:24-cv-00623, (E.D. Tex. Filed August 1, 2024)
EX2002	**Complaint for Patent Infringement,** Dkt. No. 1, *Advanced Integrated Circuit Process LLC v. United Microelectronics Corporation,* Case No. 2:24-cv-00730, (E.D. Tex. Filed September 6, 2024)
EX2003	**Consolidation Order,** Dkt. No. 12, *Advanced Integrated Circuit Process LLC v. United Microelectronics Corporation,* Consolidated Case Nos. 2:24-cv-00730, -00623, (E.D. Tex. Filed December 6, 2024)
EX2004	**Docket Sheet**, *Advanced Integrated Circuit Process LLC v. United Microelectronics Corporation,* Case No. 2:24-cv-00730, (E.D. Tex.) (Printed July 7, 2025)
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EX2006	**Second Docket Control Order**, Dkt. No. 55, *Advanced Integrated Circuit Process LLC v. United Microelectronics Corporation,* Consolidated Case Nos. 2:24-cv-00730, -00623, (E.D. Tex. Filed February 21, 2025)
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EX2008	**Third Amended Docket Control Order,** Dkt. No. 83, *Advanced Integrated Circuit Process LLC v. United Microelectronics Corporation,* Consolidated Case Nos. 2:24-cv-00730, -00623, (E.D. Tex. Filed April 9, 2025)
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EX2013	**Defendant Taiwan Semiconductor Manufacturing Company Limited's Notice of Compliance and Service of Invalidity Contentions**, Dkt. No. 104, *Advanced Integrated Circuit Process LLC v. United Microelectronics Corporation,* Consolidated Case Nos. 2:24-cv-00730, -00623, (E.D. Tex. Filed May 1, 2025)
EX2014	**Defendant United Microelectronic Corporation's Notice of Compliance and Service of Invalidity Contentions**, Dkt. No. 106 *Advanced Integrated Circuit Process LLC v. United Microelectronics Corporation,* Consolidated Case Nos. 2:24-cv-00730, -00623, (E.D. Tex. Filed May 2, 2025)
EX2015	**Scheduling Order**, Dkt. No. 28, *Advanced Integrated Circuit Process LLC v. United Microelectronics Corporation,* Case No. 2:24-cv-00730, (E.D. Tex. Filed December 11, 2024)
EX2016	**Defendant TSMC's Invalidity Contentions**, *Advanced Integrated Circuit Process LLC v. United Microelectronics Corporation,* Consolidated Case Nos. 2:24-cv-00730, -00623, (E.D. Tex. Served May 1, 2025)
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EX2019	**Protective Order**, Dkt. No. 71, *Advanced Integrated Circuit Process LLC v. United Microelectronics Corporation,* Consolidated Case Nos. 2:24-cv-00730, -00623, (E.D. Tex. Filed March 20, 2025)
EX2020	**Joint Notice Resolving Discovery Disputes Set for Hearing (Dkt.**

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	Nos. 78, 80, 89, 90), Dkt. No. 102, *Advanced Integrated Circuit Process LLC v. United Microelectronics Corporation,* Consolidated Case Nos. 2:24-cv-00730, -00623, (E.D. Tex. Filed April 30, 2025)
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EX2022	**United Microelectronics Corporation's Motion to Dismiss Plaintiff's Claims for Direct Infringement and Pre-Suit Indirect Infringement**, Dkt. No. 15, *Advanced Integrated Circuit Process LLC v. United Microelectronics Corporation,* Consolidated Case Nos. 2:24-cv-00730, -00623, (E.D. Tex. Filed December 6, 2024)
EX2023	**Defendant Taiwan Semiconductor Manufacturing Company Limited's Reply in Support of its Motion to Stay Pending *Inter Partes* Review**, Dkt. No. 109, *Advanced Integrated Circuit Process LLC v. United Microelectronics Corporation,* Consolidated Case Nos. 2:24-cv-00730, -00623, (E.D. Tex. Filed May 20, 2025)
EX2024	**Plaintiff's Opposition to Defendant Taiwan Semiconductor Manufacturing Company Limited's Motion to Stay,** Dkt. No. 108, *Advanced Integrated Circuit Process LLC v. United Microelectronics Corporation,* Consolidated Case Nos. 2:24-cv-00730, -00623, (E.D. Tex. Filed May 12, 2025)
EX2025	**Exhibit 227-01** to Defendant TSMC's Invalidity Contentions, *Advanced Integrated Circuit Process LLC v. United Microelectronics Corporation,* Consolidated Case Nos. 2:24-cv-00730, -00623 (E.D. Tex. Served May 1, 2025)
EX2026	**Exhibit 227-02** to Defendant TSMC's Invalidity Contentions, *Advanced Integrated Circuit Process LLC v. United Microelectronics Corporation,* Consolidated Case Nos. 2:24-cv-00730, -00623 (E.D. Tex. Served May 1, 2025)
EX2027	**Lex Machina Time-to-Trial Statistics Report** for trials before The Honorable Rodney Gilstrap, Federal District Judge in the Eastern District of Texas, during the period from July 1, 2024 to July 1, 2025
EX2028	**Notice of Allowance** in TSMC's U.S. Patent Application Ser. No. 12/757,241 (May 24, 2012)
EX2029	**U.S. Patent Application Publication No. 2011/0147857**

Exhibit	Description
EX2030	**Notice of Allowance** in TSMC's U.S. Patent Application Ser. No. 17/027,032 (November 24, 2023)
EX2031	**Redaction to TSMC's Sealed Motion for Issuance of Letter Rogatory for Nuvoton Technology Corporation – Japan,** Dkt. No. 119, *Advanced Integrated Circuit Process LLC v. United Microelectronics Corporation,* Consolidated Case Nos. 2:24-cv-00730, -00623 (E.D. Tex. Filed June 27, 2025)
EX2032	**Exhibit A to TSMC's Sealed Motion for Issuance of Letter Rogatory for Nuvoton Technology Corporation – Japan,** Dkt. No. 116-1, *Advanced Integrated Circuit Process LLC v. United Microelectronics Corporation,* Consolidated Case Nos. 2:24-cv-00730, -00623 (E.D. Tex. Filed June 20, 2025)
EX2033	**Exhibit B to TSMC's Sealed Motion for Issuance of Letter Rogatory for Nuvoton Technology Corporation – Taiwan,** Dkt. No. 114-2, *Advanced Integrated Circuit Process LLC v. United Microelectronics Corporation,* Consolidated Case Nos. 2:24-cv-00730, -00623 (E.D. Tex. Filed June 20, 2025)
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EX2035	**Recorded Assignment** from Panasonic Corporation to Panasonic Semiconductor Solutions Co., Ltd. (May 21, 2020)
EX2036	**Recorded Assignment by Change of Name** from Panasonic Semiconductor Solutions Co., Ltd. to Nuvoton Technology Corporation Japan
EX2037	Reserved
EX2038	Bashir, R., et al., "Reduction of Sidewall Defect Induced Leakage Currents by the Use of Nitrided Field Oxides in Silicon Selective Epitaxial Growth Isolation for Advanced Ultralarge Scale Integration," 18(2) J. Vac. Sci. Technol. B 695–699 (2000).

Advanced Integrated Circuit Technology, LLC ("Patent Owner") respectfully requests that the Board decline to institute *inter partes* review ("IPR") on the petition ("Petition") filed by Taiwan Semiconductor Manufacturing Company Ltd. ("Petitioner") because it fails to "show[] . . . a reasonable likelihood" that Petitioner would prevail with respect to any of the challenged claims. 35 U.S.C. § 314(a).

I. INTRODUCTION

Although the Petition's theories suffer from many infirmities, this preliminary response focuses on a single flaw fatal to all grounds.[1] All claims in United States Patent No. 7,579,227 ("the '227 patent") recite, directly or by dependency, an "active region ***in*** a substrate." Although the Petition offers no claim construction proposal for that phrase, Petitioner's expert and textbook assert that "substrate" means "silicon wafer." But whereas the '227 patent teaches a transistor isolation technology that (consistent with the claims) results in the transistor's active region being "in" the silicon wafer, the Petition's references disclose different, unusual transistor isolation technologies that result in the transistor's

[1] Because this flaw precludes a "reasonable likelihood" of success as to all challenged claims, 35 U.S.C. § 314(a), Patent Owner need not address the Petition's other flaws. If the Board institutes IPR, Patent Owner reserves the right to address each of these flaws.

active region being in layers that are "on" the silicon wafer. Simply accepting the Petition's evidence as true, the Petition cannot demonstrate that the claimed invention was known in, or obvious in view of, the asserted references.

II. BACKGROUND[2]

A. Technology Background

"Modern CMOS chips integrate millions of active devices . . . side by side in a common silicon substrate." EX1003 ¶ 45 (quoting EX1033 at 52). One such active device is a MISFET, which stands for "metal-insulator-semiconductor field effect transistor." *Id*. ¶ 36. The terms "MISFET" and "MOSFET" are interchangeable. *Id*. As exemplified by Petitioner's Weste reference Figure 1.8, EX1041 at 8 (shown below), "[a] typical MISFET device is a three-terminal

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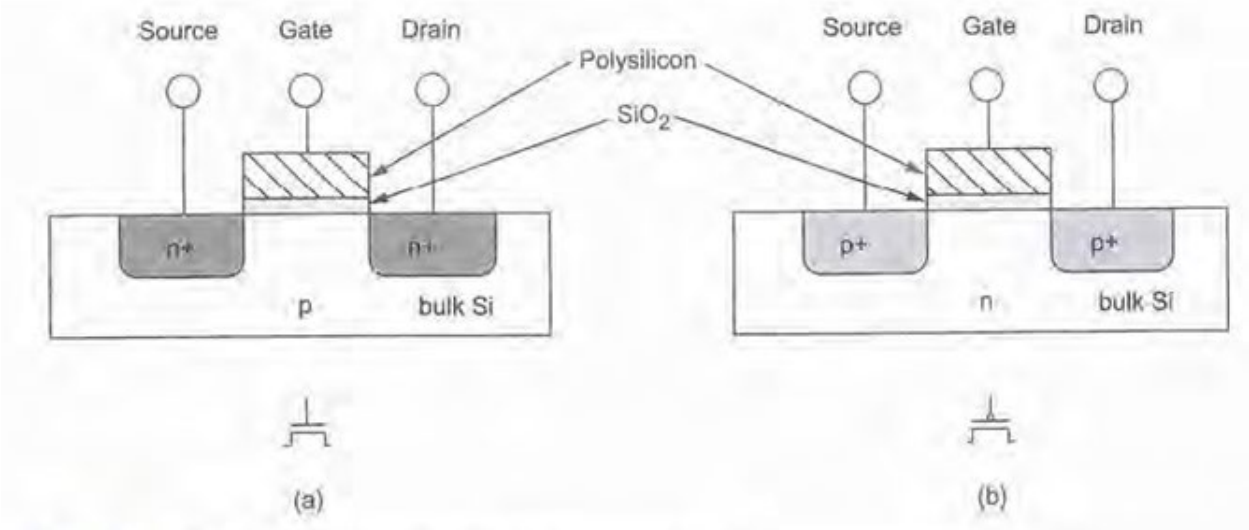
[2] The Petition submitted as evidence the expert declaration of Dr. Jack Lee (EX1003 or "Lee Declaration") and a copy of the reference text N. Weste and D. Harris, "CMOS VLSI Design: A Circuits and Systems Perspective", Third Edition (Pearson/Addison Wesley, 2005) (EX1041 or "Weste"). Patent Owner here accepts as true certain statements in these two references solely for purposes of demonstrating the flaws in the Petition. In the event the Board institutes IPR, Patent Owner reserves the right to submit its own evidence, including evidence contrary to the statements in the Lee Declaration and Weste.

structure with an input, referred to as the source, an output, referred to as the drain, and a control terminal, referred to as the gate electrode." EX1003 ¶ 36. "The source and drain regions, which are physically equivalent and therefore interchangeable, are formed by implanting dopants (either n-type or p-type) into the silicon substrate on either side of the gate electrode." *Id*. ¶ 40. "MISFETs with n-type source/drain regions are referred to as NMOS, and MISFETs with p-type source/drain regions are referred to as PMOS." *Id*. ¶ 44 (emphasis omitted).



Weste, Figure 1.8

As shown in Weste Figure 1.8(b) above, "a pMOS transistor requires an n-type body region" in which the transistor's source and drain are fabricated. EX1041

at 23. The CMOS fabrication process therefore typically[3] "begins with the creation of an n-well on a bare p-type silicon wafer." *Id*. at 25 More particularly, "[f]orming the n-well requires adding enough [n-type] dopants ***into the silicon substrate*** to change the substrate from p-type to n-type in the region of the well." *Id.* (emphasis added). This is accomplished "through a selective doping process known as ion implantation." EX1003 ¶ 40. In this process "dopant ions are accelerated through an electric field and blasted ***into the substrate***." EX1041 at 25 (emphasis added).[4]

The process for forming the n-well by selectively implanting dopants into the wafer surface typically proceeds as follows. First, to define which regions of the silicon wafer are n-wells, "a protective layer of oxide [is grown] over the entire wafer" and then selectively etched using photolithography "where we want the wells." *Id*. at 25. When the ion implantation step using n-type dopants is performed, "the oxide layer prevents dopant atoms from entering the substrate where no well is intended." *Id*. However, in regions of the wafer surface that are not covered by

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[3] As will be explained *infra*, certain transistor isolation technologies perform preprocessing on the silicon wafer before this step.

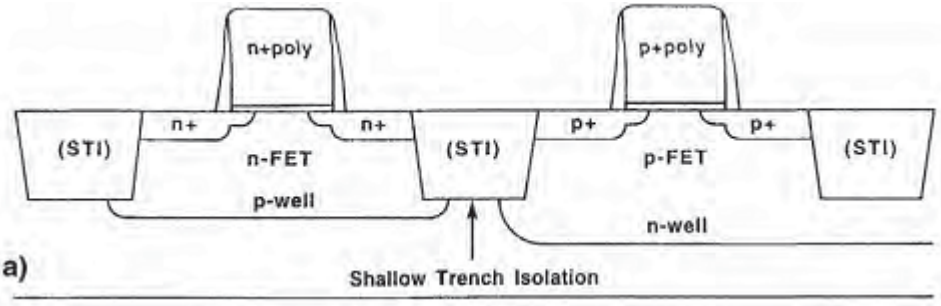
[4] *See also id*. at 117 ("Ion implantation involves subjecting the silicon substrate to highly energized donor or acceptor atoms. When these atoms impinge on the silicon surface, they travel below the surface of the silicon.").

oxide, the dopants "***enter the substrate*** and form the wells." *Id*. (emphasis added). This process is depicted graphically in Weste reference text Figure 1.36. *Id*. at 27. After the transistor's gate insulator and gate electrode have been formed, the source and drain regions can be formed in the silicon wafer (to the left and right of the gate electrode) using ion implantation, with the gate blocking the dopants from entering the channel beneath the gate. *Id*. at 28.

Although pure crystalline silicon is a semiconductor with "bulk electrical resistance somewhere between that of a conductor and an insulator," the doping in the source and drain regions can increase their conductivity by "several orders of magnitude." *Id*. at 114. Because transistors are arranged "side by side" on the silicon wafer, EX1003 ¶ 45, to avoid undesired electrical interactions between them, "individual devices in a CMOS process need to be isolated from one another." EX1041 at 119. Moreover, because the silicon wafer is itself somewhat conductive, *id*. at 114, it can be desirable to insulate the devices from the wafer as well. As explained in detail *infra*, several techniques have been developed for electrically isolating transistors from one another and/or from the underlying silicon wafer. Importantly, and as will be described, those techniques differ in terms of whether they form the transistor's active region "in" the silicon wafer or in a layer that is deposited or grown "on" the silicon wafer surface.

1. Shallow Trench Isolation

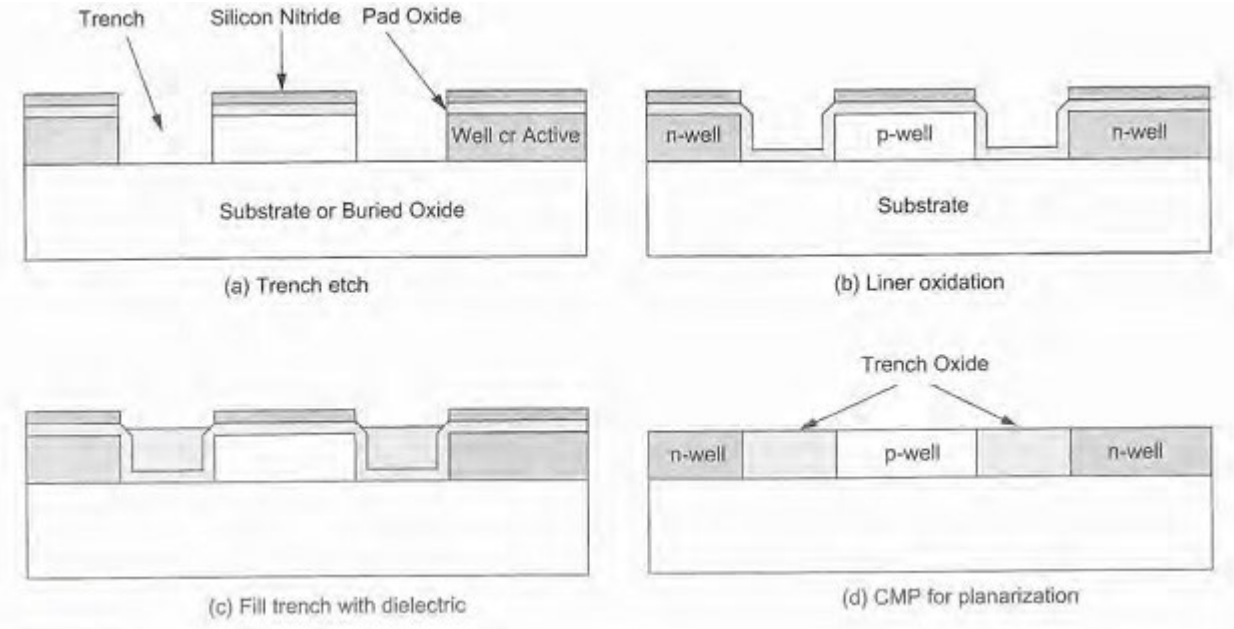
Shallow trench isolation ("STI") is a transistor isolation approach in which "a relatively shallow trench is first etched into the Si substrate (0.3-0.5-μm deep), which is then refilled with an insulator material." EX1034 at 433. It is the isolation technology of choice "in processes at and below the 180 nm node. . . . Typical trenches in a 90 nm process can be 140 nm wide by 400 nm deep." EX1041 at 119. Figure 9.1(a) from Petitioner's Wolf reference textbook (below) provides a graphical representation of a cross section of pMOS and nMOS transistors fabricated using STI. EX1034 at 434. "Trench isolation [] permits nMOS and pMOS transistors to be placed closer together because the isolation provides a higher source-drain breakdown voltage." EX1041 at 119 (emphasis omitted).



Wolf, Figure 9.1(a)

As depicted in Weste Figure 3.3 (below), STI can be performed directly into the silicon wafer or in conjunction with a silicon-on-insulator process (discussed in Section II(A)(2), *infra*) that employs a thin silicon layer above a buried oxide. EX1041 at 120. The STI process "starts with a pad oxide and a silicon nitride layer,

which act as the masking layers." *See id.* at 119-20 (two topmost layers in Figure 3.3(a)). "Openings in the pad oxide are then used to etch into the well or substrate region (this process can also be used for source/drain diffusion)." *Id*. "A liner oxide is then grown to cover the exposed silicon." *Id*. (Figure 3.3(b)). Next, "[t]he trenches are filled with SiO_2 using CVD." *Id*. (Figure 3.3(c)). Finally, "[t]he pad oxide and nitride are removed and a *Chemical Mechanical Polishing* (CMP) step is used to planarize the structure." *Id*. (Figure 3.3(d)).

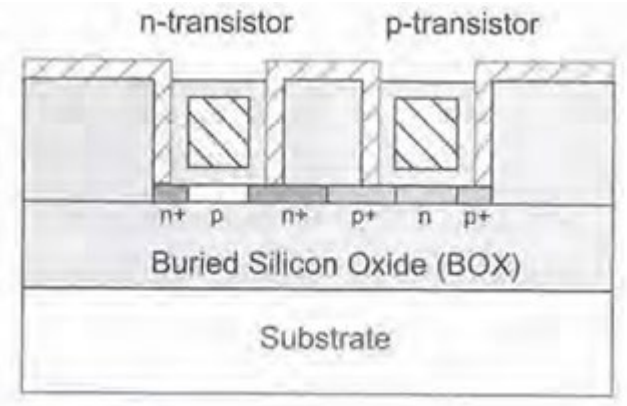


Weste, Figure 3.3

2. Silicon-On-Insulator Isolation

Silicon-on-insulator ("SOI") isolation is a "process where the transistors are fabricated on an insulator." EX1041 at 136. To accomplish this, as depicted in Figure 3.12 of Petitioner's Weste reference text (below), "a silicon substrate is used

and a buried oxide (BOX) is grown ***on top of the silicon substrate***. A thin silicon layer is then grown ***on top of the buried oxide*** and this is selectively implanted to form nMOS and pMOS transistor regions. Gate, source and drain regions are then defined in a similar fashion to a bulk process." *Id*. at 137 (emphasis added and omitted). Note that, consistent with the Weste reference's description, when SOI is used, the nMOS and pMOS transistor's active regions are not "in the substrate" but rather are in the "thin silicon layer" that is "grown on top of the buried oxide," which in turn is grown "on top of the silicon substrate." *Id*.

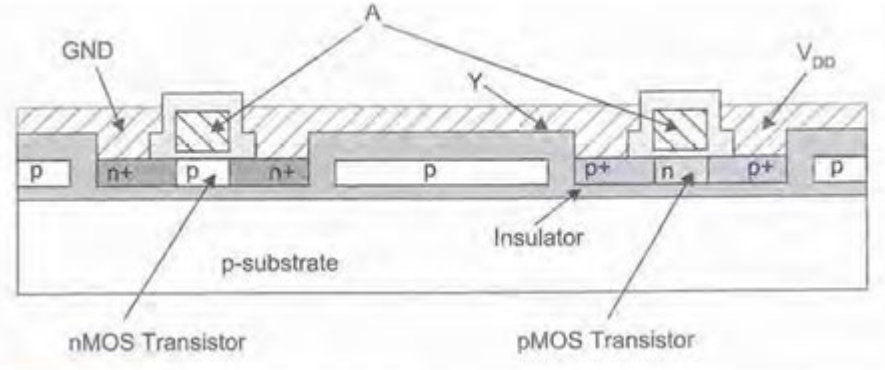


Weste, Figure 3.12

Because the foregoing process insulates the transistors from the silicon wafer below but does not provide lateral insulation between neighboring transistors located at the SOI surface, "[s]hallow trench isolation is used to surround each transistor by an oxide insulator." *Id*. at 370. As a result, "the transistor source, drain, and body are surrounded by insulating oxide rather than the conductive substrate or well (called the *bulk).*" *Id*. at 369; EX1034 at 501 (noting that, in SOI, integrated

circuits are "made from single-device islands dielectrically isolated from ***the substrate*** and each other.") (emphasis added).

Weste's Figure 6.69 (below) depicts the transistor structure for a typical CMOS inverter using SOI. EX1041 at 370. Note again that the active regions of the nMOS and pMOS transistor are located in the thin silicon layer located on the insulator that is stacked on top of the substrate. Weste teaches that this approach to transistor isolation "offers potential for higher performance and lower power consumption, but also has a higher manufacturing cost and some unusual transistor behavior that complicates circuit design." EX1041 at 369.



Weste, Figure 6.69

3. Selective Epitaxial Growth Isolation

Selective epitaxial[5] growth isolation ("SEGI") is an alternative to STI and SOI that affords electrical insulation between neighboring transistors through "the formation of isolated device islands." EX2038 ("Bashir")[6] at 695. Figure 4 in Bashir "shows a typical device isolation process using selective epitaxial growth." *Id*. at 695-96. First, a film of insulating silicon dioxide is grown on the silicon wafer surface and then transistor "active regions are defined" by performing an "active area etch" of the silicon dioxide in those areas where transistors will be fabricated. *Id*. at 696 (figure caption, Figure 4a). Next, "[s]elective epitaxial growth of silicon is performed [on the exposed regions of the silicon wafer] to form the active device regions." *Id*. (figure caption, Figure 4(b)). Because "[t]he epitaxy can overgrow the insulator regions, [t]he silicon overgrowth is polished off using chemical mechanical polishing." *Id*. (figure caption, Figure 4(c)).

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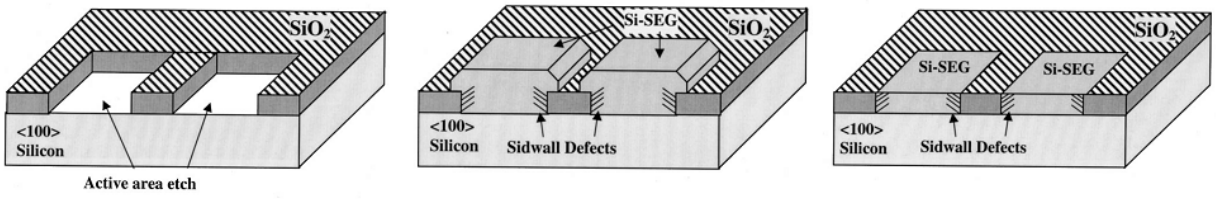
[5] "Epitaxy involves growing a single-crystal film on the silicon surface." EX1041 at 117.

[6] Bashir et al., "Reduction of Sidewall Defect Induced Leakage Currents By the Use of Nitrided Field Oxides in Silicon Selective Epitaxial Growth Isolation for Advanced Ultralarge Scale Integration," J. Vac. Sci. Technol. B 18(2), pp. 695-99, March/April 2000.



Bashir, Figures 4(a)-(c)

While SEGI is an alternative to STI, there are important differences. Most notably, SEGI results in active regions being "fabricated in [the] selective epitaxial silicon isolation structures." *Id*. at 699. Patent Owner is unaware of any commercially viable MISFET semiconductor device achieved through SEGI. "Defects in the near sidewall region in selective epitaxial growth of silicon have prevented its widespread use as a viable dielectric isolation technology." *Id*. at 695 (noting that the technique has not found widespread use because the epitaxial silicon "close to the sidewall insulator can have a high defect density"). Although a method exists for addressing these high defect rates for bipolar transistors, in "the case of MOSFETs" the approach "increases the leakage between the source and drain, resulting in poor yield." *Id*.

B. The '227 Patent Invention

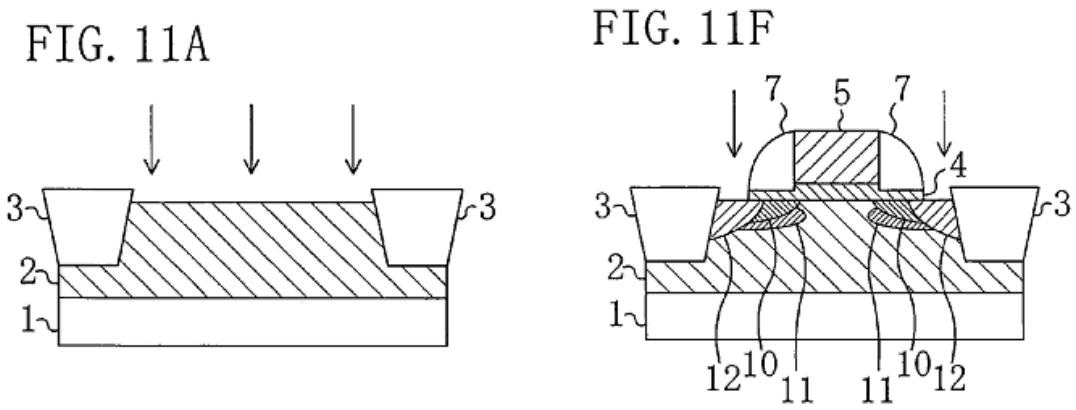
The '227 patent "relates to a structure of a MISFET (metal insulator semiconductor field-effect transistor) and a method for fabricating the MISFET and, more particularly, relates to techniques for improving the driving power and reliability of a MISFET." EX1001 at 1:10-14. The '227 patent has fifteen claims,

two of which—claims 1 and 5—are independent claims. *Id*. at 21:40-24:12. Both independent claims recite "an active region ***in*** a substrate." *Id*. at 21:43 (claim 1), 22:28 (claim 5) (emphasis added). Thus, all claims in the '227 patent require, directly or by dependency, this feature.

Although the '227 patent has several points of novelty over Petitioner's references, for purposes of this preliminary response Patent Owner will focus on its isolation technology. The '227 patent teaches STI as its preferred transistor isolation technology. *Id*. at 5:61-62 (discussing the first embodiment); *id*. at 7:28-29 (discussing the second embodiment); *id*. at 10:25-28 (discussing the third embodiment); *id*. at 13:31-34 (discussing fifth embodiment); *id*. at 15:5-9 (discussing sixth embodiment); 16:63-67 (discussing the seventh embodiment); *id*. at 18:43-48 (discussing the eighth embodiment). Although the term "STI" does not appear in the discussion of the fourth embodiment or modified fourth embodiment, *id*. at 11:55-13:20, Figure 9 corresponding to the fourth embodiment, *id*. at 11:60-63, depicts STI element 3. Each of the preferred embodiments in the '227 patent shows a finished MISFET with STI element 3 providing electrical isolation between neighboring transistors. *Id*. at Figures 1-15D.

Figures 11A and 11F (replicated below) corresponding to the '227 patent's fifth embodiment provides an example of how STI followed by ion implantation results in the formation of an active region ***in*** the substrate. First, as shown in

Figure 11A, after "a STI 3 which is to be an isolation region is selectively formed[,] . . . B (boron) is ion implanted ***into the substrate 1*** [such that] a p-type well 2 which is to be an active region is formed." *Id*. at 13:31-36 (emphasis added). Then, as shown in Figure 11F, after several additional processing steps, "As (arsenic) is ion implanted ***into the substrate 1*** . . . [and] n-type source/drain regions 12 are formed." *Id*. at 14:10-16 (emphasis added).



EX1001, Figures 11A and 11F

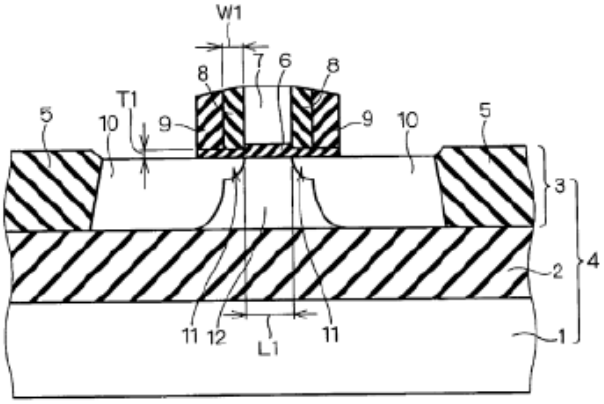
C. Petitioner's Primary References

1. Matsumoto

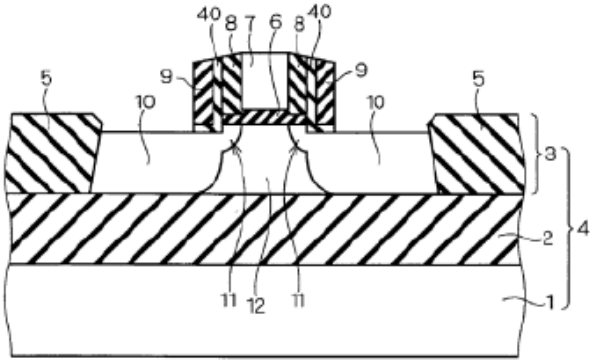
Matsumoto describes "a MOSFET (Metal Oxide Semiconductor Field Effect Transistor) employing an SOI (Silicon-On-Insulator) substrate and a method of manufacturing the same." EX1009 ¶ [0002]. The Petition asserts that although "Matsumoto presents seven embodiments of its semiconductor device," the Petition's theories "focus[] on Matsumoto's first and fourth embodiment MOSFETs

. . . .” Petition at 19-20. According to the Petition, those two embodiments—first and fourth—are reflected in Figures 1 and 22, respectively. *Id*. at 20. Accordingly, Patent Owner’s analysis centers on those same two embodiments and figures.

Matsumoto’s first embodiment, as reflected in Figure 1 (below), uses a “multi-layer structure such that a silicon substrate **1**, a BOX layer **2** and a single-crystalline silicon layer **3** are stacked in the order named.” EX1009 ¶ [0102]. Matsumoto describes that “[a] pair of source/drain regions 10 are formed ***in the silicon layer 3***” (*i.e.*, the layer on the BOX layer **2**, which in turn is above the silicon substrate **1**) and that the transistor’s “body region 12” is located “between the pair of source/drain regions 10.” *Id*. ¶ [0105] (emphasis added). Matsumoto’s fourth embodiment, as reflected in Figure 22 (below), contains the same multi-layer structure, with the source, drain, and body region located in single-crystalline silicon layer **3, *not*** in the silicon substrate **1**.



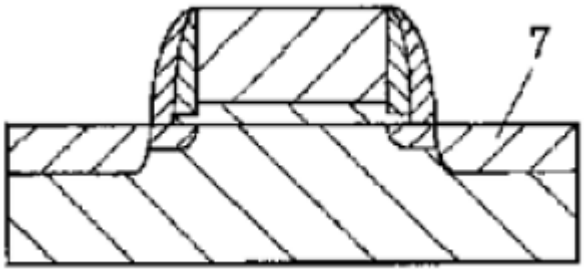
Matsumoto, Figure 1



Matsumoto, Figure 22

2. Kajiyama

Kajiyama is directed to "insulating gate type field effect transistors having a gate dielectric film." EX1011 ¶ [0001]. The Petition asserts that although "Kajiyama discloses two embodiments of its semiconductor device," the Petition's theories "focus[] on Kajiyama's first embodiment FET." Petition at 53. According to the Petition, that embodiment is reflected in Figure 1(D). *Id*. Therefore, Patent Owner's analysis centers on that same embodiment and figure.



Kajiyama, Figure 1(D)

The "[f]irst" step in the process leading to Kajiyama's Figure 1(D), reproduced below, is "forming an element separation layer [] ***on the Si substrate 1*** having a (100) surface." EX1011 ¶ [0029] (emphasis added). Although no further description of the "element separation layer" is provided in conjunction with the first embodiment, Kajiyama's description of the "[p]rior [a]rt" provides additional context. *Id.* ¶ [0002]. It states that the "element separation layer" "consist[s] of a silicon monocrystalline of type p having a (100) surface." *Id*. ¶ [0005] ("[A]fter forming an element separation layer (not shown) on the Si substrate 21 consisting of

a silicon monocrystalline of type p having a (100) surface, the Si substrate 21 is thermally oxidized to form a SiO_2 film 22 that becomes a gate insulating film."). Thus, at the conclusion of this first step in the process, the original silicon wafer surface is no longer exposed; instead, the exposed surface is the "silicon monocrystalline of type p having a (100) surface" that was deposited "on" the silicon wafer surface. *Id.* Kajiyama also explains that thereafter this epitaxial silicon film grown on the wafer surface is "referred to as a Si substrate." *Id*. ¶ [0004].

Figure 1(D) provides no ability to visualize the interface between the original wafer surface and the element separation layer because, as Kajiyama explains, the "element separation layer" is "not shown" in any of its three figure sets. *Id*. ¶¶ [0005], [0029], [0040]. In addition, Kajiyama provides no information regarding the thickness of the element separation layer grown on the silicon wafer, its relationship to the depth of the implants that give rise to the transistor's active region, or how the element separation layer achieves electrical isolation between transistors.

D. The Level of Ordinary Skill in the Art

Petitioner asserts that a person of ordinary skill in the art ("POSA") "would have had at least a Master's degree in electrical engineering, physics, chemistry, materials science, or related fields, and three years of work experience in semiconductor manufacturing. Additional graduate education could substitute for work experience, and additional work experience/training could substitute for

formal education." Petition at 19 (internal citation omitted). It is unnecessary for Patent Owner to propose a competing definition at this time because, even under Petitioner's proposed definition, Petitioner has failed to demonstrate a reasonable likelihood of success on any of the challenged claims. Patent Owner reserves the right to propose a different POSA definition if the Board institutes IPR.

III. LEGAL STANDARDS

"In an IPR, the petitioner has the burden from the onset to show with particularity why the patent it challenges is unpatentable." *Harmonic Inc. v. Avid Tech., Inc.*, 815 F.3d 1356, 1363 (Fed. Cir. 2016) (noting 35 U.S.C. § 312(a)(3) requires that petitions must identify "with particularity . . . the evidence that supports the grounds for the challenge to each claim"). To meet this burden, "the petition must specify where ***each element of the claim*** is found in the prior art patents or printed publications relied upon." 37 C.F.R. § 42.104(b)(4) (emphasis added). And "the Board must base its decision on arguments that were advanced by a party, and to which the opposing party was given a chance to respond." *In re Magnum Oil Tools Int'l, Ltd.*, 829 F.3d 1364, 1381 (Fed. Cir. 2016). The burden of persuasion on the petitioner never shifts to the patent owner. *See Dynamic Drinkware, LLC v. Nat'l Graphics, Inc.*, 800 F.3d 1375, 1378 (Fed. Cir. 2015). Applying the foregoing substantive standards and burdens, "[t]he Director may not authorize an *inter partes* review to be instituted unless the Director determines . . .

that there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition." 35 U.S.C. § 314(a).

IV. CLAIM CONSTRUCTION

"[A] petition ***must*** state how a challenged claim is to be construed and how each element of the construed claim is found in prior art patents or printed publications." *Samsung Electronics Co., Ltd. v. Blaze Mobile, Inc.*, IPR2021-01569, Paper 16, at 5 (citing 37 C.F.R. §§ 42.104(b)(3)-(4)) (emphasis added). Here, Petitioner flouted that requirement by not offering any proposed constructions for any claim terms in the '227 patent. Petition at 19.

Nevertheless, Petitioner, its expert, and Weste all assert that the claim term "substrate" means "silicon wafer." First, Weste repeatedly explains that the "silicon wafer" is "called the substrate." EX1041 at 8 ("[T]he ***silicon wafer*** [is] also called the ***substrate***, body, or bulk.") (emphasis added); *id*. at 23 ("Transistors are fabricated on thin ***silicon wafers . . . called the substrate***."). EX1041 at 23 (emphasis added). Second, Petitioner's expert also equates "silicon wafer" and "substrate." EX1003 ¶ 38 ("MISFETs are fabricated on ***silicon wafers*** that serve as the ***substrate***.") (emphasis added); EX1003 (Lee Decl.) ¶ 36 (quoting the Weste reference text for the principle that the "silicon wafer [is] also called the substrate, body or bulk"). Third, in one of its sister petitions, Petitioner uses "silicon wafer" and "substrate" synonymously. *Taiwan Semiconductor Manufacturing Co., Ltd v.*

Advanced Integrated Circuit Process LLC, IPR2025-00832, Paper 2 at 3 ("A metal-insulating-semiconductor transistor (MISFET or MOSFET) generally includes . . . '***the silicon wafer, also called the substrate***, body or bulk.'") (emphasis added) (quoting Weste).

Patent Owner need not formally adopt a position on the proper meaning of "substrate" in the context of the '227 patent at this time. At this stage, the relevant question is whether the Petition has met ***its burden*** of showing a "reasonable likelihood" of success under 35 U.S.C. § 314(a). Because Petitioner has not complied with its obligation under 37 C.F.R. § 42.104(b)(3) to propose a construction for "substrate" but has introduced evidence supporting the conclusion that "substrate" means "silicon wafer," Patent Owner relies on that meaning solely for purposes of rebutting the Petition's Grounds. In the event the Board institutes *inter partes* review on the Petition, Patent Owner reserves the right to advance and substantiate constructions for any terms in the '227 patent, including the term "substrate."

If IPR is instituted, Petitioner has no right to assert "substrate" means something other than what its expert and reference text say—namely, "silicon wafer." First, "the Board must base its decision on arguments that were advanced by a party, and to which the opposing party was given a chance to respond." *In re Magnum Oil*, 829 F.3d at 1381. Here, Petitioner waived any right to offer a different

construction for substrate by not offering any construction, Petition at 19, and then offering evidence supporting the conclusion that "substrate" means "silicon wafer." Second, even if Petitioner were permitted to now argue that "substrate" means something other than "silicon wafer," this would only highlight "Petitioner's failure to provide an interpretation in the face of claim language that is admittedly [per Petitioner] subject to some range of interpretations." *DJI Europe B.V. v. Textron Innovations Inc.*, IPR2023-01107, Paper 14 at 7 (PTAB February 13, 2024).

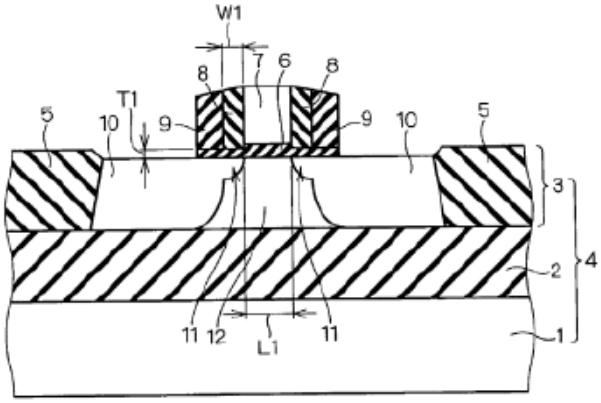
V. ARGUMENT

A. Grounds 1-4 Fail to Prove that Matsumoto Teaches "an Active Region in a Substrate"

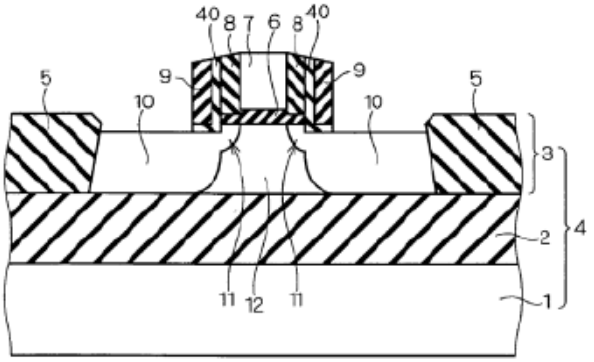
1. Ground 1 Fails

Ground 1 fails because, on the Petition's own record, Petitioner cannot show that Matsumoto describes "an active region in a substrate," a limitation required directly or by dependency in each claim in the '227 patent. EX1001 at 21:40-24:12. Although the Petition offers no proposed construction for the claim term "substrate," Petition at 19, Petitioner's evidence and argument support the conclusion that "substrate" means "silicon wafer." *See* Section IV *supra*. As explained *infra*, applying this construction, Matsumoto does not describe forming transistor active regions "in" the substrate but rather describes forming transistor active regions in a single-crystalline silicon layer that is stacked on a BOX (*i.e.*, buried oxide) layer, which is in turn stacked "on" the silicon wafer. Because

Matsumoto does not describe this claim limitation, Ground 1 fails. 37 C.F.R. § 42.104(b)(4) (requiring that the Petition identify where "***each element of the claim*** is found in the prior art patents or printed publications relied upon.") (emphasis added).



Matsumoto, Figure 1

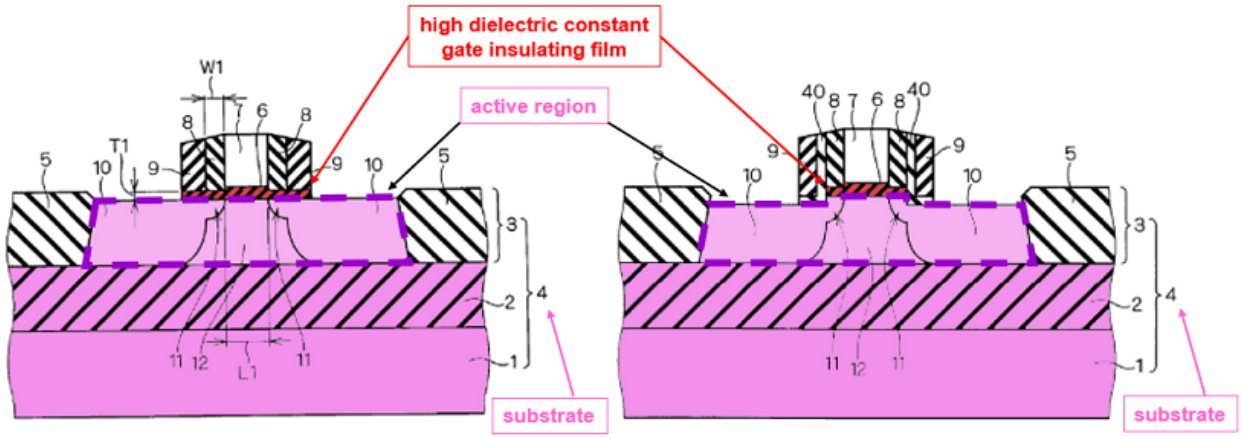


Matsumoto, Figure 22

Ground 1 is predicated on "Matsumoto's first and fourth embodiment MOSFETs," which are depicted graphically in Figures 1 and 22. Petition at 19-20. Both figures (reproduced above, Petition at 20) depict a "multi-layer structure such that a silicon substrate **1**, a BOX layer **2** and a single-crystalline silicon layer **3** are stacked in the order named." EX1009 ¶ [0102]. Matsumoto explains that the transistor's active region exists "in" silicon layer 3, not in silicon substrate 1. *Id*. ¶ [0105] ("A pair of source/drain regions 10 are formed ***in the silicon layer 3***") (emphasis added); *id*. (explaining that the transistor's "body region 12" is located "between the pair of source/drain regions 10"). Figure 22, above, contains the same

multi-layer structure, with the source, drain and body region located in silicon layer **3, *not*** in silicon substrate **1**.

Rather than dispute this point, the Petition embraces it. Specifically, Petitioner's annotated versions of Figure 1 and 22 (reproduced below) show the "active region" as located in single-crystalline silicon layer 3, which is "on" silicon substrate 1. Petition at 22-23. But the Petition ignores this deficiency in Matsumoto by labeling the entire "multi-layer structure" comprising elements 1-3 together as the "substrate." *Id.* ("Both embodiments . . . . ha[ve] a multi-layer SOI substrate 4 . . . .").



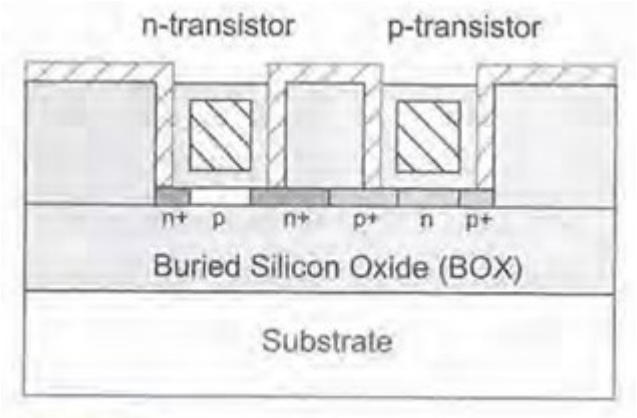
Matsumoto, Figures 1 and 22 (annotated), Petition at 23

Matsumoto also refers to the "multi-layer structure" as an "SOI substrate 4." Obviously, "SOI substrate" and "substrate" are different terms. Moreover, Matsumoto acts as its own lexicographer by coining the phrase "SOI substrate." Thus, Matsumoto's unique language is not relevant to the meaning of "substrate" in

the ’227 patent. Petitioner’s own record suggests that “substrate” does not mean a multi-layer SOI structure but rather means “silicon wafer.” Weste repeatedly explains that the “silicon wafer” is “called the substrate.” EX1041 at 8 (“[T]he ***silicon wafer*** [is] also called the ***substrate***, body, or bulk.”) (emphasis added); *id*. at 23 (“Transistors are fabricated on thin ***silicon wafers . . . called the substrate.”*** EX1041 at 23 (emphasis added). Moreover, Petitioner’s expert also equates “silicon wafer” and “substrate.” EX1003 ¶ 38 (“MISFETs are fabricated on ***silicon wafers*** that serve as the ***substrate***.”) (emphasis added); EX1003 (Lee Decl.) ¶ 36 (quoting the Weste reference text for the principle that the “silicon wafer [is] also called the substrate, body or bulk”). And Petitioner itself uses “silicon wafer” and “substrate” synonymously. *Taiwan Semiconductor Manufacturing Co., Ltd v. Advanced Integrated Circuit Process LLC*, IPR2025-00832, Paper 2 at 3 (“A metal-insulating-semiconductor transistor (MISFET or MOSFET) generally includes . . . ‘***the silicon wafer, also called the substrate***, body or bulk.”) (emphasis added) (quoting Weste).

Indeed, Weste rebuts any argument that a POSA would adopt Matsumoto’s “SOI substrate” language, which is different from “substrate.” Weste teaches that “a silicon substrate is used and a buried oxide (BOX) is grown ***on top of the silicon substrate***. A thin silicon layer is then grown ***on top of the buried oxide*** and this is selectively implanted to form nMOS and pMOS transistor regions.” EX1041 at 137 (emphasis added). And, in the accompanying Figure 3.12 (below), Weste does not

refer to the multi-layer SOI as the substrate but rather shows the "substrate" as a silicon wafer underlying the BOX and thin silicon layer. Because the Petition's evidence suggests that "substrate" means "silicon wafer," and because the Petition admits that in Matsumoto the transistor's active region is not "in" the silicon wafer but rather is in silicon layer 3 that is above the silicon wafer, the Petition has failed to meet its burden of showing that "***each element of the claim*** is found in the prior art patents or printed publications relied upon." 37 C.F.R. § 42.104(b)(4). Accordingly, Ground 1 does not present a "reasonable likelihood" of success as to any claim in the '227 patent. 35 U.S.C. § 314(a).



Weste, Figure 3.12

2. Grounds 2-4 Fail

The Petition concedes that Matsumoto "does not expressly disclose" the dependent claim limitations in claims 7, 8 and 14. Petition at 38. The theory underlying Ground 2 is that "Wang discloses these teachings," *id*., and that a POSA would be motivated to "[a]pply[] Wang's [teachings] to Matsumoto's first or fourth

embodiment." *Id*. at 42. The Petition does not rely upon Wang as teaching an "active region in a substrate" and thus the same flaw that is fatal to Ground 1 is also fatal to Ground 2.

Ground 3 simply substitutes Motou for Wang in the Matsumoto-Wang combination in Ground 2 in the event that "the combination of Matsumoto and Wang fails to render claims 7-8 obvious" because Mutou allegedly "also explicitly describes a '*buffer insulating film*.'" Petition at 43. The Petition does not rely upon Motou as teaching an "active region in a substrate" and thus the same flaw that is fatal to Ground 1 is also fatal to Ground 3.

Regarding Ground 4, the Petition concedes that Matsumoto "do[es] not expressly disclose" the limitations in dependent claim 6 and 14—namely, "that the high-k gate insulating film '*includes a notch at a side end portion*' [6] or '*is formed of a Hf based oxide*' [14]." Petition at 47 (emphasis in original). The theory underlying Ground 4 is that "[t]hese features are disclosed in Ono, and the combination of Matsumoto and Ono renders claims 6 and 14 obvious." *Id*. The Petition does not rely upon Ono as teaching an "active region in a substrate," which as explained in Patent Owner's Ground 1 analysis, is absent from Matsumoto, and thus the same flaw that is fatal to Ground 1 is also fatal to Ground 4.

B. Grounds 5-7 Fail to Prove that Kajiyama Teaches "an Active Region in a Substrate"

1. Ground 5 Fails

Ground 5 fails because, on the Petition's own record, Petitioner cannot show that Kajiyama describes "an active region ***in*** a substrate," a limitation required directly or by dependency in each claim in the '227 patent. EX1001 at 21:40-24:12 (emphasis added). Although the Petition offers no proposed construction for the claim term "substrate," Petition at 19, Petitioner's evidence and argument support the conclusion that "substrate" means "silicon wafer." *See* Section IV, *supra*. As explained *infra*, applying this construction, the Petition does not show that Kajiyama describes forming transistor active regions "in" the substrate especially given Kajiyama's teaching that they are formed in an "element separation layer" located on the silicon wafer. Because the Petition has failed to explain how Kajiyama teaches this claim limitation, Ground 5 fails. 37 C.F.R. § 42.104(b)(4) (requiring that the Petition identify where "***each element of the claim*** is found in the prior art patents or printed publications relied upon") (emphasis added).

One of the Petition's key errors in describing Kajiyama is its assertion that "Kajiyama's element separation layer is equivalent to the '227 patent's STI structures." Petition at 55. This is nonsense. On the one hand, and as its name suggests (and as Petitioner's text references teach), STI (or shallow trench

isolation) is composed of an electrical ***insulator***. EX1041 at 119 (teaching that "shallow trench isolation (STI)" comprises "***insulating*** trenches of SiO_2 that surround active areas") (emphasis added); EX1034 at 433 ("In STI a relatively shallow trench is first etched into the Si substrate (0.3-0.5μm deep), which is then refilled with an ***insulator*** material") (emphasis added). On the other hand, Kajiyama's "element separation layer . . . consist[s] of a silicon monocrystalline of type p." EX1011 ¶ [0005] ("[A]fter forming an element separation layer (not shown) on the Si substrate 21 consisting of a silicon monocrystalline of type p having a (100) surface, the Si substrate 21 is thermally oxidized to form a SiO_2 film 22 that becomes a gate insulating film."). Pure silicon is a "semiconductor," not an insulator. EX1041 at 114. And, when silicon is doped, as is the case for Kajiyama's element separation layer, the conductivity increases dramatically (up to "several orders of magnitude"). *Id*. Thus, Kajiyama's p-type single crystal silicon is a conductor, not an insulator, and cannot possibly be serving a role "equivalent" to STI as the Petition contends. Petition at 55.

Although Kajiyama's "element separation layer" is "not shown" in its

figures, *see* EX1011 ¶ [0005] and associated figures, a POSA might[7] suspect that Kajiyama employs SEGI as described in Bashir, especially in light of other ambiguities in Kajiyama. *See* Section II(A)(3), *supra*. Of the three isolation techniques discussed—STI, SOI, and SEGI—Kajiyama is only consistent with SEGI. Kajiyama is not consistent with STI because STI does not involve epitaxial silicon growth on the silicon wafer. *See* Section II(A)(1), *supra*. And Kajiyama cannot be reconciled with SOI because in SOI single crystal silicon is grown on the insulating BOX layer, *See* Section II(A)(2), *supra*, not directly on the silicon wafer surface as Kajiyama teaches, EX1011 ¶ [0005] (teaching "forming an element separation layer (not shown) on the Si substrate 21 consisting of a silicon monocrystalline of type p").

The Petition never explains how, in Kajiyama, the transistor's active region can be "in" the silicon wafer given that it is in the element separation layer.[8] In

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[7] Because Kajiyama confusingly discloses an "element separation layer" that is a conductor rather than an insulator, its teachings are entirely unclear. As a result, no POSA would rely upon this reference.

[8] Nothing in this Preliminary Response should be construed to suggest that transistors whose active areas are fabricated in epitaxially grown silicon are not "in" the silicon wafer. For example, one could epitaxially grow silicon on the entirety of

SEGI, the only isolation technique consistent with Kajiyama's disclosure, the transistors' active regions are fabricated in the element separation layer that is grown "on" the silicon wafer. As Bashir explains, its Figure 4 (reproduced below) "shows a typical device isolation process using selective epitaxial growth." EX2038 at 695-96. First, a film of insulating silicon dioxide is grown on the silicon wafer surface and then transistor "active regions are defined" by performing an "active area etch" of the silicon dioxide in those areas where transistors will be fabricated. *Id*. at 696 (Figure 4a). Next, "[s]elective epitaxial growth of silicon is performed [on the exposed regions of the silicon wafer] to form the active device regions." *Id*. (figure caption, Figure 4(b)). Because "[t]he epitaxy can overgrow the insulator regions, [] [t]he silicon overgrowth is polished off using chemical mechanical polishing." *Id*. (figure caption, Figure 4(c)).

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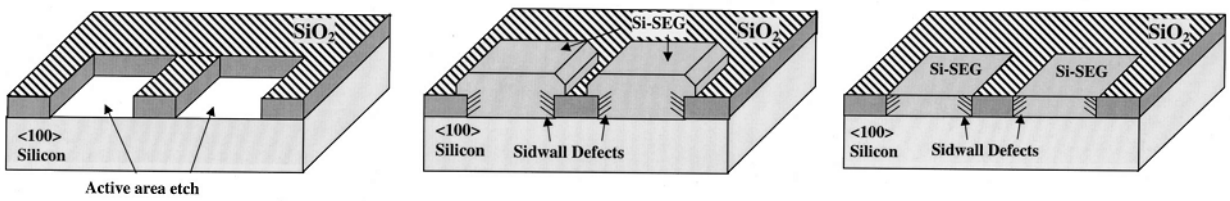
the wafer surface, thereby creating a thicker silicon wafer, and then form transistors in that thicker silicon wafer. In that instance, the transistor's active regions might well be both in the silicon wafer and in the epitaxial silicon. But that is distinct from forming transistor active regions in an inadequately described and cryptic "element separation layer," like the one mentioned but not described in Kajiyama, that is formed "on" the silicon wafer. EX1011 ¶ [0005].



Bashir, Figures 4(a)-(c)

It is Petitioner's burden to show that the active region of Kajiyama's transistor is "in" the "substrate" under the meaning of "substrate" supported by the Petition. Petitioner cannot meet this burden. While Kajiyama includes an internal definition that its "element separation layer" composed of "p-type silicon monocrystalline" is "hereinafter referred to as a Si substrate," EX1011 ¶ [0004], Kajiyama is not a reliable reference for matters of claim construction.

First, Kajiyama is a translated Japanese-language patent application that is likely not using standard English in developing its language and terms. Second, Kajiyama is not a reference textbook reflecting customarily accepted terminology. EX1011. Therefore, Kajiyama's language cannot show how a term is used in English. On the other hand, Weste is a reference textbook originally written in English, and is thus a more reliable source for matters of claim construction. Kajiyama's unconventional nomenclature is entitled to little weight relative to Weste and Petitioner's Expert's statements. *See* Section V(A)(1), *supra*.

2. Grounds 6-7 Fail

Ground 6 contends that Kajiyama renders dependent claims 9 and 14 obvious

because, based on the express teachings in Kajiyama, "[a] POSITA would have [] been motivated to" (1) "use a fully silicided gate in the first embodiment device [of Kajiyama]"; and "select HfO_2 as the high-k material for Kajiyama's gate dielectric." Petition at 62. Even if these assertions were true, Ground 6 does not establish that an "active region in a substrate" is disclosed in Kajiyama. As explained in Patent Owner's Ground 5 analysis, *supra*, because Petitioner cannot show an "active region in a substrate" in Kajiyama, the same flaw fatal to Ground 5 is also fatal to Ground 6.

Regarding Ground 7, the Petition concedes that "Kajiyama . . . does not explicitly disclose" the limitation in dependent claim 6 "that [*sic*] high-k gate insulating film '*includes a notch at a side end portion.*'" Petition at 63 (emphasis in original). The theory underlying Ground 7 is that "Ono discloses this teaching," *id.*, and that "[a] POSITA would have been motivated to" combine Ono's alleged teaching of a notch with Kajiyama's first embodiment. *Id.* at 63-64. The Petition does not rely upon Ono to disclose an "active region in a substrate." Thus, Ground 7 fails for the same reasons as Grounds 5 and 6.

For the foregoing reasons, Patent Owner respectfully requests that the Board decline to institute IPR.

Dated: August 13, 2025

Respectfully submitted,

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Russell A. Chorush (Reg. No. 55,869)
Attorney for Patent Owner
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CERTIFICATE OF SERVICE

The undersigned certifies that pursuant to 37 C.F.R. § 42.6(e), a copy of the foregoing PATENT OWNER'S PRELIMINARY RESPONSE UNDER 37 C.F.R. § 42.107 TO PETITION FOR INTER PARTES REVIEW OF U.S. PATENT NO. 7,579,227 was served to the following counsel of record for Petitioner as follows:

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CERTIFICATE OF COMPLIANCE

Pursuant to 37 C.F.R. § 42.24(d), the undersigned hereby certifies that this brief complies with the type-volume limitation of 37 C.F.R. § 42.24 because this brief contains 5,759 words.

Dated: August 13, 2025

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